

Pin Definition:

- | | |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate | 5. Drain |

Key Parameter Performance

Parameter	Value	Unit
V_{DS}	20	V
$R_{DS(on)}$ (max)	$V_{GS} = 4.5V$	20
	$V_{GS} = 2.5V$	25
	$V_{GS} = 1.8V$	31
Q_g	12.3	nC

Features

- Advanced High Cell Density Trench Technology.
- Low Gate Charge.

Application

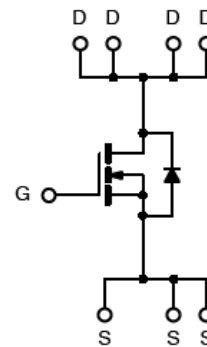
- Networking DC-DC Power System.
- Load Switch.

Ordering Information

Part No.	Package	Packing
TSM4806CS RLG	SOP-8	2.5kpcs / 13" Reel

Note: "G" denotes Halogen Free Product.

Block Diagram



N-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^a	I_D	28	A
Pulsed Drain Current ^b	I_{DM}	70	A
Continuous Source Current (Diode Conduction) ^{a,c}	I_S	28	A
Total Power Dissipation	P_D	2	W
Storage Temperature Range	T_{STG}	-55 to +150	$^{\circ}C$
Operating Junction Temperature Range	T_J	-55 to +150	$^{\circ}C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance Junction to Lead	$R\theta_{JL}$	40	$^{\circ}C/W$
Thermal Resistance Junction to Ambient	$R\theta_{JA}$	62.5	$^{\circ}C/W$

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$ surface mounted on FR4 Board, $t \leq 5s$.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Electrical Specifications

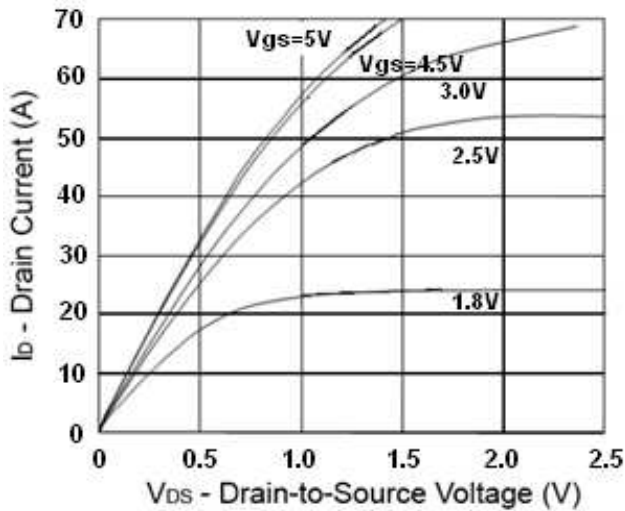
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.3	0.6	1.0	V
Gate-Source Leakage Current	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{DS} = 16V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 20A$	$R_{DS(ON)}$	--	16	20	m Ω
	$V_{GS} = 2.5V, I_D = 15A$		--	20	25	
	$V_{GS} = 1.8V, I_D = 10A$		--	25	31	
Forward Transconductance	$V_{DS} = 5V, I_D = 15A$	g_{fs}	--	27	--	S
Diode Forward Voltage	$I_S = 1A, V_{GS} = 0V$	V_{SD}	--	--	1.2	V
Dynamic^b						
Gate Resistance	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$	R_g	--	1.4	2.8	Ω
Total Gate Charge	$V_{DS} = 15V, I_D = 15A, V_{GS} = 4.5V$	Q_g	--	12.3	--	nC
Gate-Source Charge		Q_{gs}	--	1.95	--	
Gate-Drain Charge		Q_{gd}	--	3.08	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1MHz$	C_{iss}	--	961	--	pF
Output Capacitance		C_{oss}	--	92.3	--	
Reverse Transfer Capacitance		C_{rss}	--	80.4	--	
Reverse Recovery Time	$I_F = 15A, dI/dt = 100A/\mu s, T_J = 25^\circ C$	t_{rr}	--	6	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.38	--	nC
Switching^{b,c}						
Turn-On Delay Time	$V_{DD} = 10V, I_D = 15A, V_{GS} = 4.5V, R_G = 3.3\Omega$	$t_{d(on)}$	--	3.02	--	ns
Turn-On Rise Time		t_r	--	13.1	--	
Turn-Off Delay Time		$t_{d(off)}$	--	28	--	
Turn-Off Fall Time		t_f	--	8.3	--	

Notes:

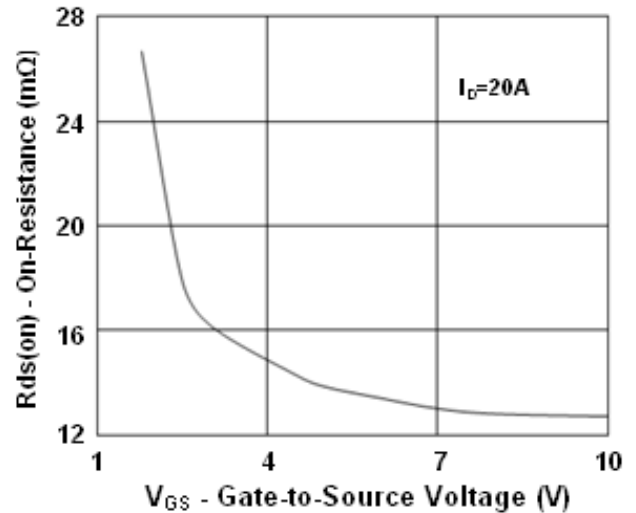
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

Electrical Characteristics Curve ($T_A=25^\circ\text{C}$, unless otherwise noted)

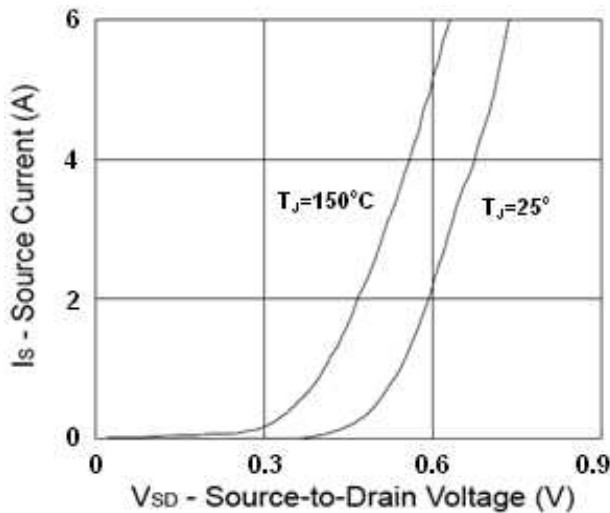
Output Characteristics



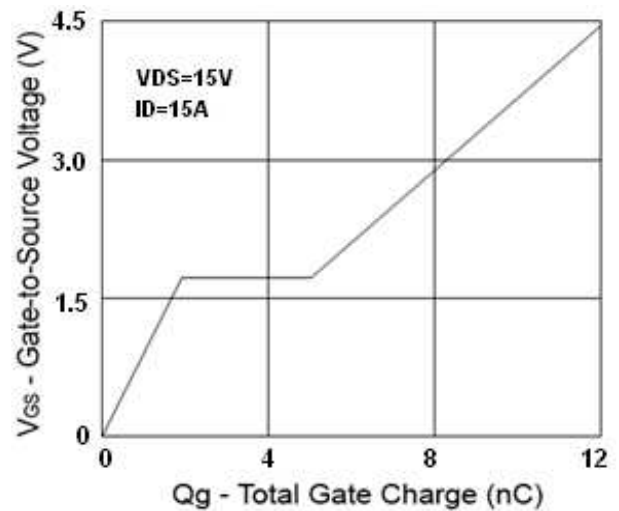
On-Resistance vs. Gate-Source Voltage



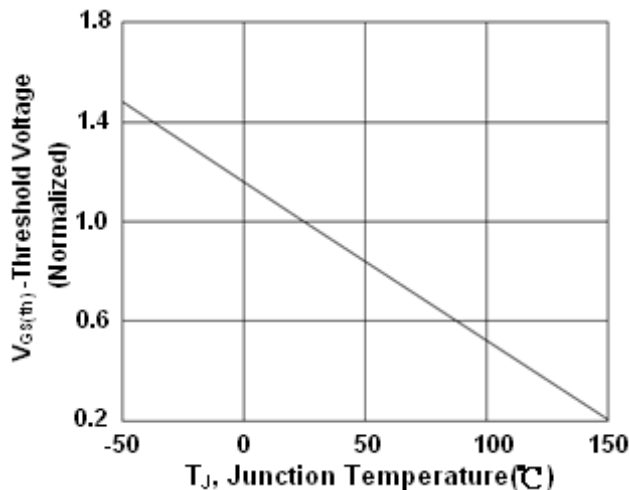
Source-Drain Diode Forward Voltage



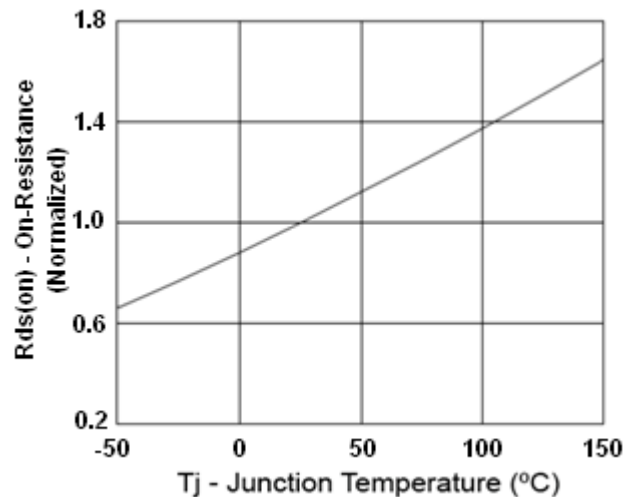
Gate Charge



Normalized $V_{GS(th)}$ vs. T_J

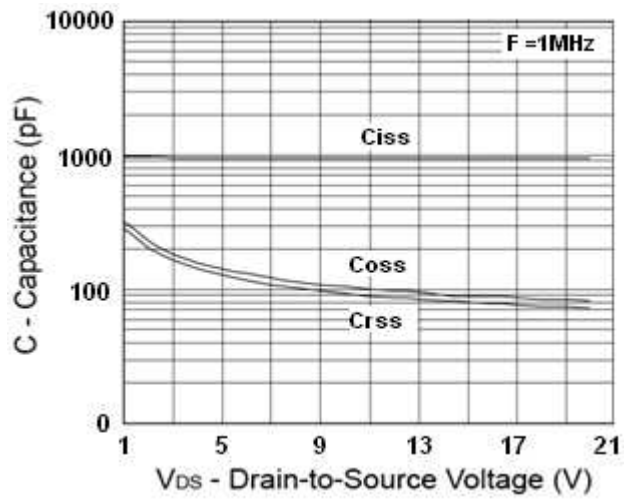


Normalized $R_{DS(on)}$ vs. T_J

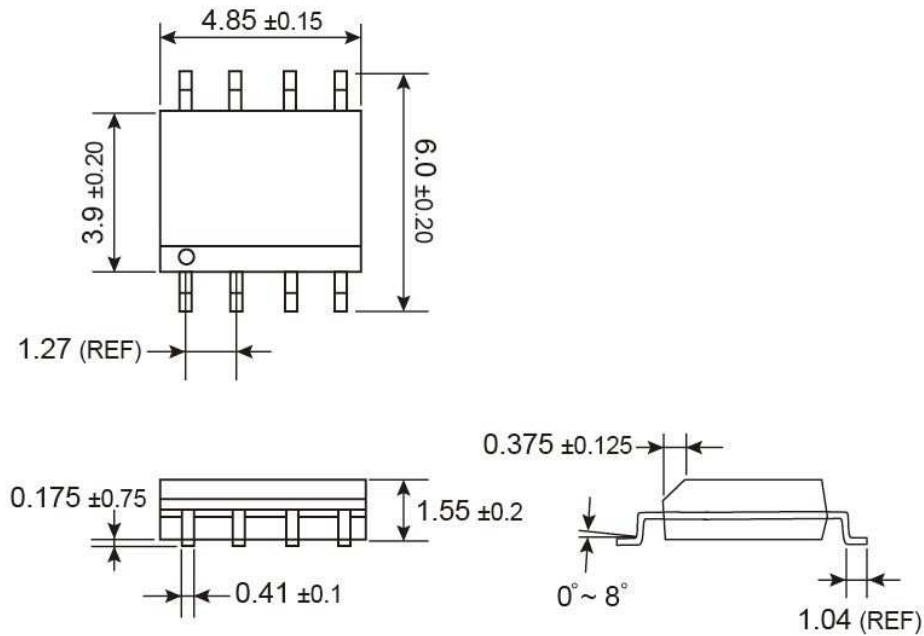


Electrical Characteristics Curve ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

Capacitance

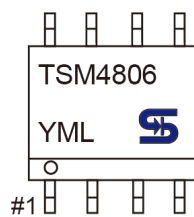


SOP-8 Mechanical Drawing



Unit: Millimeters

Marking Diagram



Y = Year Code

M = Month Code for Halogen Free Product

(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apr, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)

L = Lot Code

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