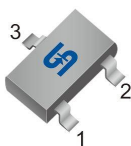


TSM650P02CX

20V P-Channel Power MOSFET

SOT-23



Pin Definition:

1. Gate
2. Source
3. Drain

Key Parameter Performance

Parameter		Value	Unit
V_{DS}		-20	V
$R_{DS(on)}$ (max)	$V_{GS} = -4.5V$	65	$m\Omega$
	$V_{GS} = -2.5V$	85	
	$V_{GS} = -1.8V$	130	
Q_g		6.4	nC

Features

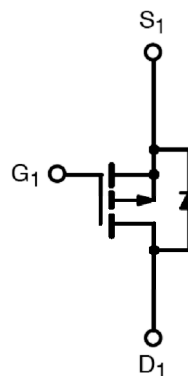
- χ Fast switching
- χ Suited for -1.8V gate drive applications
- χ Halogen-free

Ordering Information

Part No.	Package	Packing
TSM650P02CX RFG	SOT-23	3kcs / 70Reel

Note: Ⓐ denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Block Diagram



P-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 10	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	-4.1	A
	$T_C = 100^\circ C$		-2.6	A
Pulsed Drain Current ^(Note 1)		I_{DM}	-16.4	A
Power Dissipation @ $T_C = 25^\circ C$		P_D	1.56	W
Operating Junction Temperature		T_J	150	$^\circ C$
Storage Temperature Range		T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Ambient	R_{JA}	80	$^\circ C/W$

Electrical Specifications ($T_C = 25^\circ\text{C}$ unless otherwise noted)

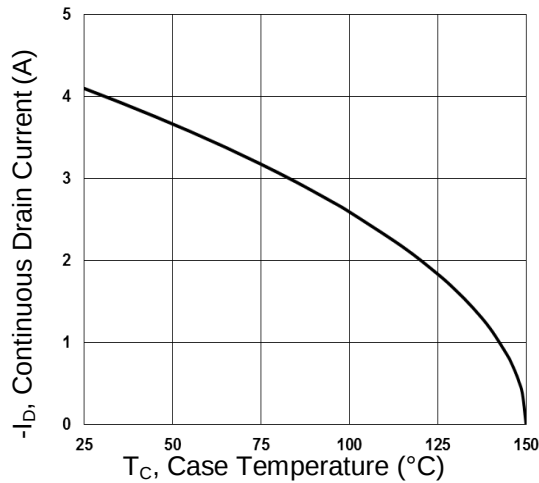
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-20	--	--	V
Drain-Source On-State Resistance	$V_{GS} = -4.5V, I_D = -3A$	$R_{DS(on)}$	--	52	65	m_{Ω}
	$V_{GS} = -2.5V, I_D = -2A$		--	73	85	
	$V_{GS} = -1.8V, I_D = -1.5A$		--	105	130	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-0.4	-0.6	-0.8	V
Zero Gate Voltage Drain Current	$V_{DS} = -20V, V_{GS} = 0V$	I_{DSS}	--	--	-1	μA
	$V_{DS} = -16V, T_J = 125^{\circ}C$		--	--	-10	
Gate Body Leakage	$V_{GS} = \pm 10V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Forward Transconductance ^(Note 2)	$V_{DS} = -10V, I_D = -3A$	g_{fs}	--	5.5	--	S
Dynamic						
Total Gate Charge ^(Note 2,3)	$V_{DS} = -10V, I_D = -3A,$ $V_{GS} = -4.5V$	Q_g	--	6.4	--	nC
Gate-Source Charge ^(Note 2,3)		Q_{gs}	--	0.9	--	
Gate-Drain Charge ^(Note 2,3)		Q_{gd}	--	1.6	--	
Input Capacitance	$V_{DS} = -10V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	515	--	pF
Output Capacitance		C_{oss}	--	55	--	
Reverse Transfer Capacitance		C_{rss}	--	20	--	
Switching						
Turn-On Delay Time ^(Note 2,3)	$V_{DD} = -10V, I_D = -1A,$ $V_{GS} = -4.5V, R_{GEN} = 25_{\Omega}$	$t_{d(on)}$	--	5	--	ns
Turn-On Rise Time ^(Note 2,3)		t_r	--	17.4	--	
Turn-Off Delay Time ^(Note 2,3)		$t_{d(off)}$	--	40.7	--	
Turn-Off Fall Time ^(Note 2,3)		t_f	--	11.4	--	
Source-Drain Diode Ratings and Characteristic						
Maximum Continuous Drain-Source Diode Forward Current	Integral reverse diode in the MOSFET	I_S	--	--	-4.1	A
Maximum Pulse Drain-Source Diode Forward Current		I_{SM}	--	--	-16.4	A
Diode-Source Forward Voltage	$V_{GS} = 0V, I_S = -1A$	V_{SD}	--	--	-1	V

Note:

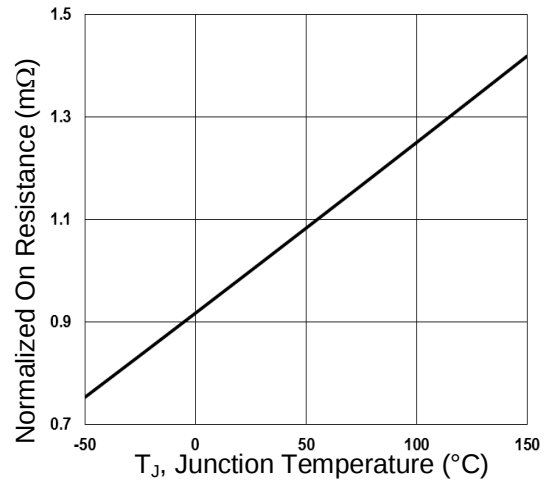
- Pulse width limited by safe operating area
- Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- Switching time is essentially independent of operating temperature.

Electrical Characteristics Curve

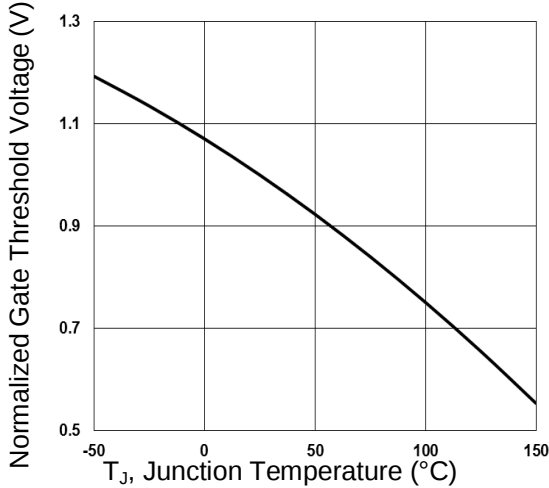
Continuous Drain Current vs. T_C



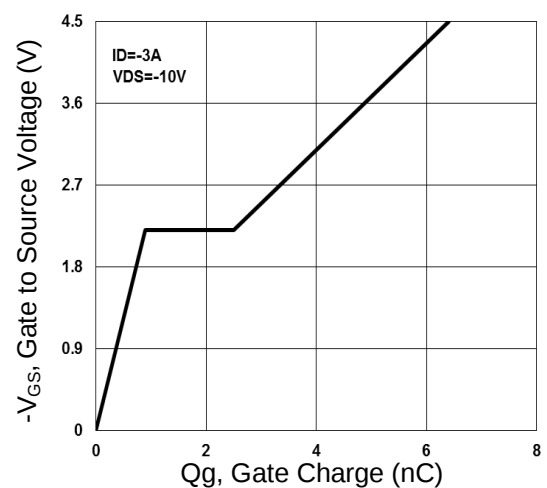
Normalized $R_{DS(on)}$ VS. T_J



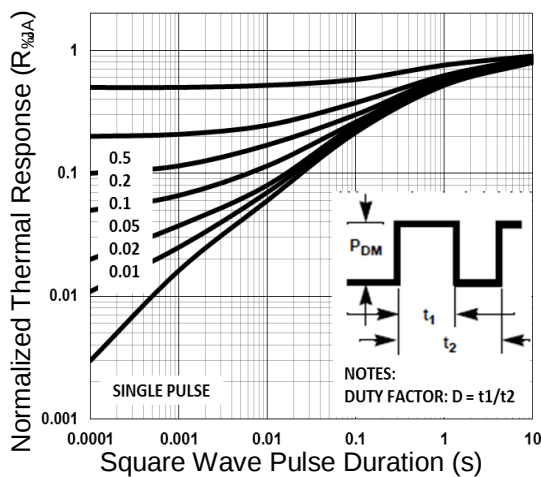
Threshold Voltage vs. Junction Temperature



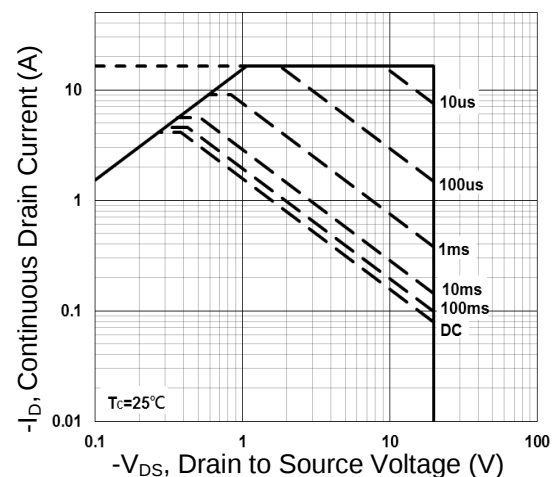
Gate Charge Waveform



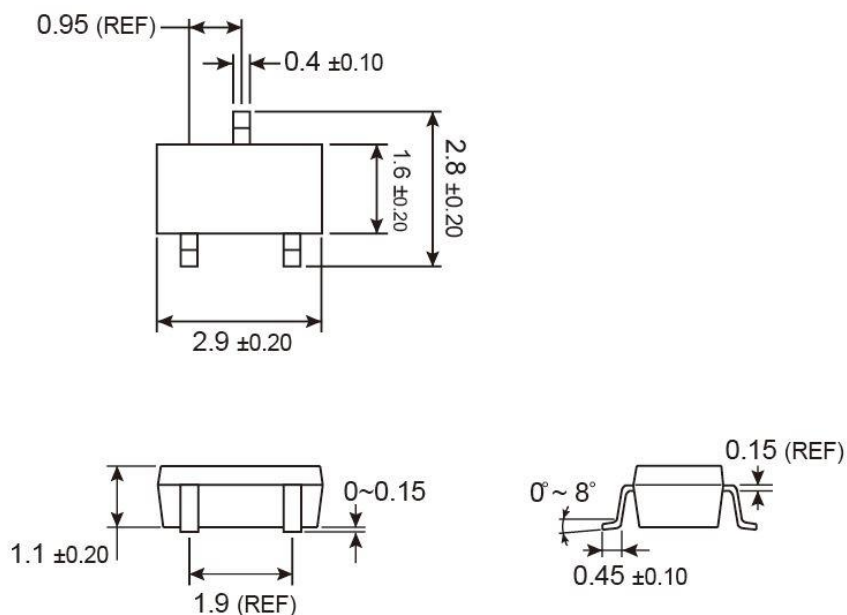
Normalized Thermal Transient Impedance Curve



Maximum Safe Operating Area

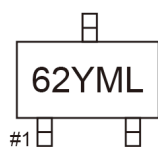


SOT-23 Mechanical Drawing



Unit: Millimeters

Marking Diagram



- 62** = Device Code
- Y** = Year Code
- M** = Month Code for Halogen Free Product
(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apr, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
- L** = Lot Code

TSM650P02CX

20V P-Channel Power MOSFET

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