# TSM7311D

## 20V Dual N-Channel MOSFET w/ESD Protected

**SOP-8**

**Pin Definition:**

| | |
|---|---|
| 1. Source 1 | 8. Drain 1 |
| 2. Gate 1 | 7. Drain 1 |
| 3. Source 2 | 6. Drain 2 |
| 4. Gate 2 | 5. Drain 2 |

### PRODUCT SUMMARY

| $V_{DS}$ (V) | $R_{DS(on)}$(mΩ) | $I_D$ (A) |
|---|---|---|
| 20 | 22 @ $V_{GS}$ = 4.5V | 6.5 |
| | 29 @ $V_{GS}$ = 2.5V | 5.5 |

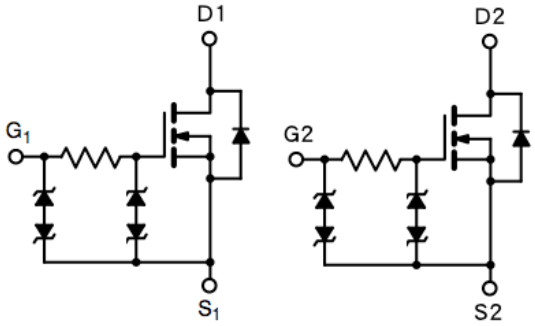
### Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- ESD Protect 2KV

### Application

- Specially Designed for Li-on Battery Packs
- Battery Switch Application

### Block Diagram




Dual N-Channel MOSFET

### Ordering Information

| Part No. | Package | Packing |
|---|---|---|
| TSM7311DCS RL | SOP-8 | 2.5Kpcs / 13" Reel |

### Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current, $V_{GS}$ @4.5V. | | $I_D$ | 6.5 | A |
| Pulsed Drain Current, $V_{GS}$ @4.5V | | $I_{DM}$ | 30 | A |
| Continuous Source Current (Diode Conduction)[a,b] | | $I_S$ | 1.4 | A |
| Maximum Power Dissipation | Ta = 25°C | $P_D$ | 8.5 | W |
| | Ta = 75°C | | 6.4 | |
| Operating Junction Temperature | | $T_J$ | +150 | °C |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +150 | °C |

### Thermal Performance

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Junction to Foot (Drain) Thermal Resistance | $R\Theta_{JF}$ | 30 | °C/W |
| Junction to Ambient Thermal Resistance (PCB mounted) | $R\Theta_{JA}$ | 62.5 | °C/W |

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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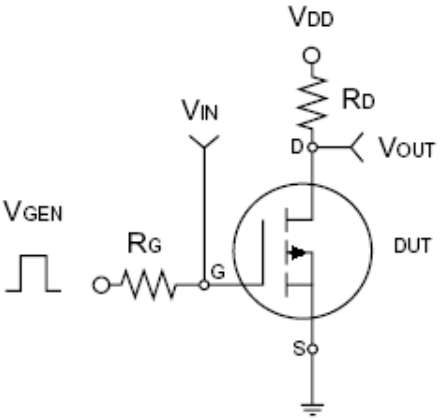
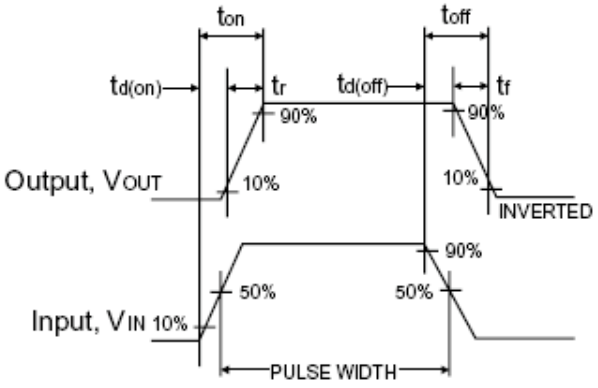
### Electrical Specifications (Ta = 25°C unless otherwise noted)

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250uA | $BV_{DSS}$ | 20 | -- | -- | V |
| Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250uA | $V_{GS(TH)}$ | 0.6 | 0.8 | 1.0 | V |
| Gate Body Leakage | $V_{GS}$ = ±12V, $V_{DS}$ = 0V | $I_{GSS}$ | -- | -- | ±10 | uA |
| Zero Gate Voltage Drain Current | $V_{DS}$ = 16V, $V_{GS}$ = 0V | $I_{DSS}$ | -- | -- | 1.0 | uA |
| On-State Drain Current | $V_{DS}$ =5V, $V_{GS}$ = 4.5V | $I_{D(ON)}$ | 30 | -- | -- | A |
| Drain-Source On-State Resistance | $V_{GS}$ = 4.5V, $I_D$ = 6.5A | $R_{DS(ON)}$ | -- | 15 | 22 | mΩ |
| | $V_{GS}$ = 2.5V, $I_D$ = 5.5A | | -- | 20 | 29 | |
| Forward Transconductance | $V_{DS}$ = 10V, $I_D$ = 6.5A | $g_{fs}$ | -- | 30 | -- | S |
| Diode Forward Voltage | $I_S$ = 1.7A, $V_{GS}$ = 0V | $V_{SD}$ | -- | 0.6 | 1.2 | V |
| **Dynamic**[b] | | | | | | |
| Total Gate Charge | $V_{DS}$ = 10V, $I_D$ = 6.5A, $V_{GS}$ = 4.5V | $Q_g$ | -- | 15 | 20 | nC |
| Gate-Source Charge | | $Q_{gs}$ | -- | 3.4 | -- | |
| Gate-Drain Charge | | $Q_{gd}$ | -- | 1.2 | -- | |
| Input Capacitance | $V_{DS}$ = 10V, $V_{GS}$ = 0V, f = 1.0MHz | $C_{iss}$ | -- | 950 | -- | pF |
| Output Capacitance | | $C_{oss}$ | -- | 450 | -- | |
| Reverse Transfer Capacitance | | $C_{rss}$ | -- | 135 | -- | |
| **Switching**[c] | | | | | | |
| Turn-On Delay Time | $V_{DD}$ = 10V, $R_L$ = 10Ω, $I_D$ = 1A, $V_{GEN}$ = 4.5V, $R_G$ = 6Ω | $t_{d(on)}$ | -- | 140 | 200 | nS |
| Turn-On Rise Time | | $t_r$ | -- | 210 | 250 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | -- | 3700 | 4800 | |
| Turn-Off Fall Time | | $t_f$ | -- | 2000 | 2600 | |

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.




Switching Test Circuit




Switchin Waveforms

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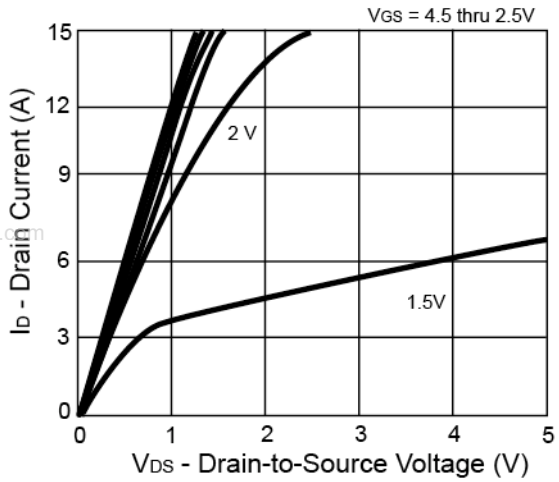
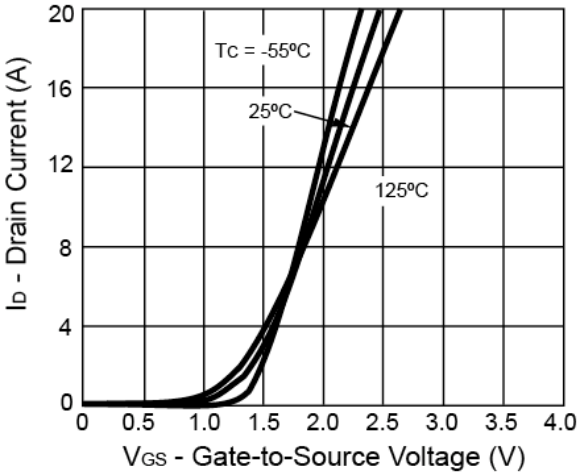
## Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

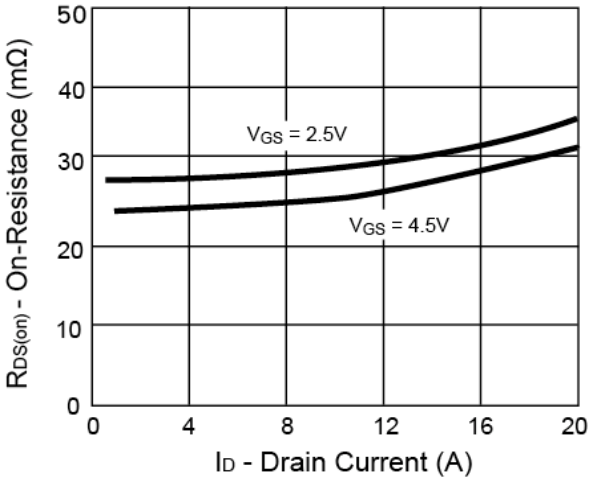
### Output Characteristics



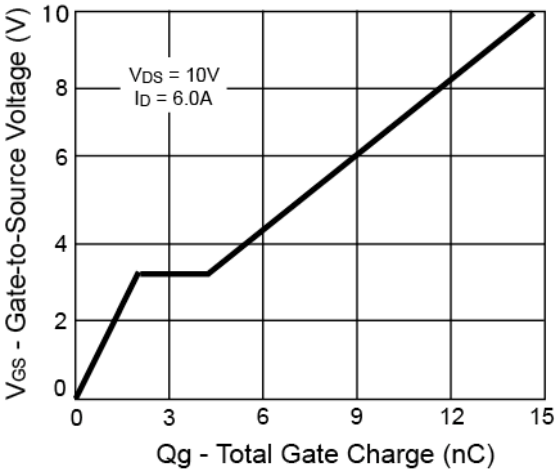

### Transfer Characteristics



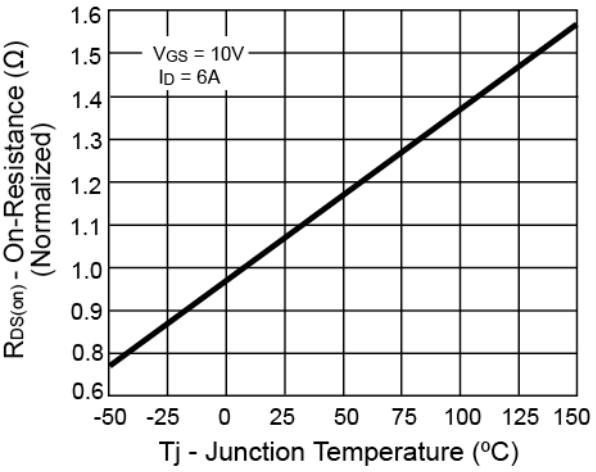

### On-Resistance vs. Drain Current



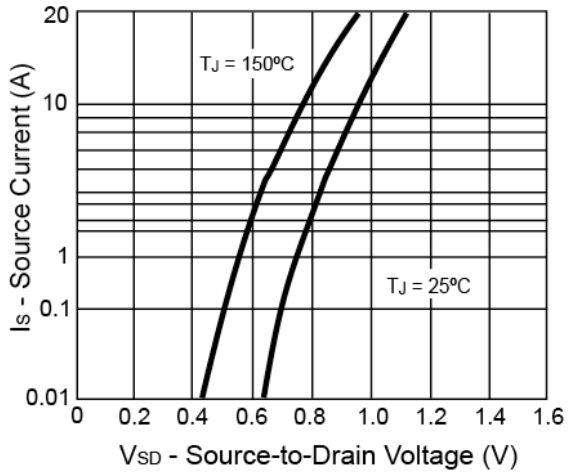

### Gate Charge




### On-Resistance vs. Junction Temperature

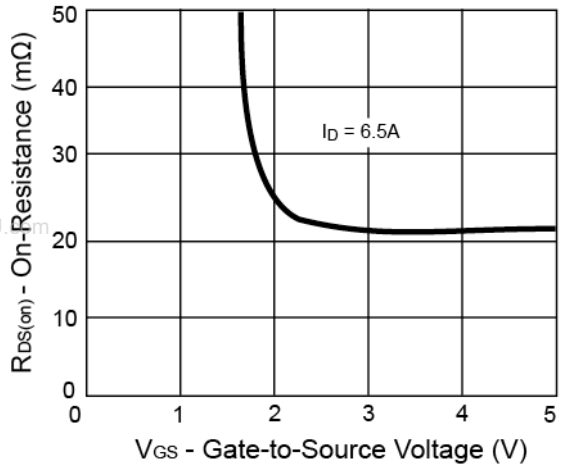



### Source-Drain Diode Forward Voltage

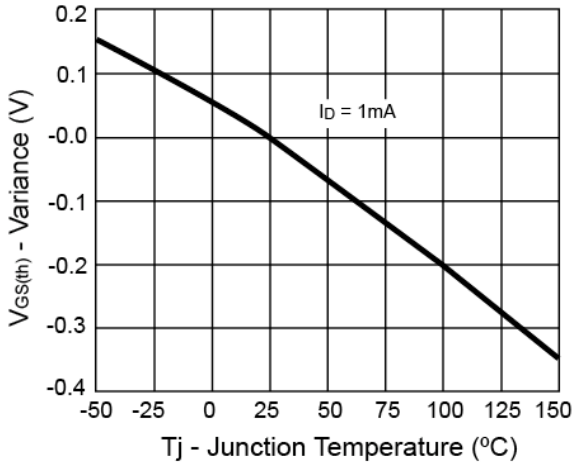


## Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

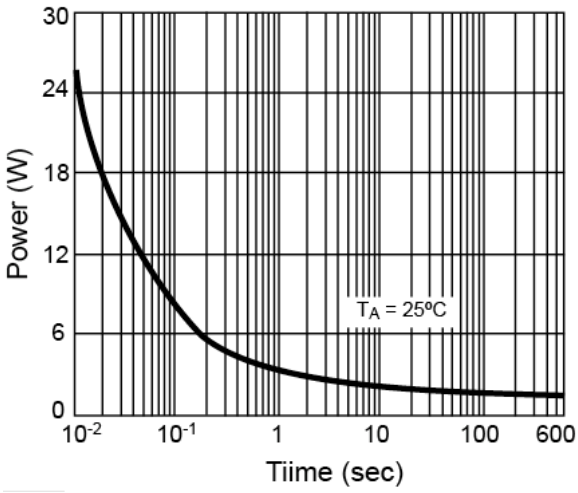
### On-Resistance vs. Gate-Source Voltage



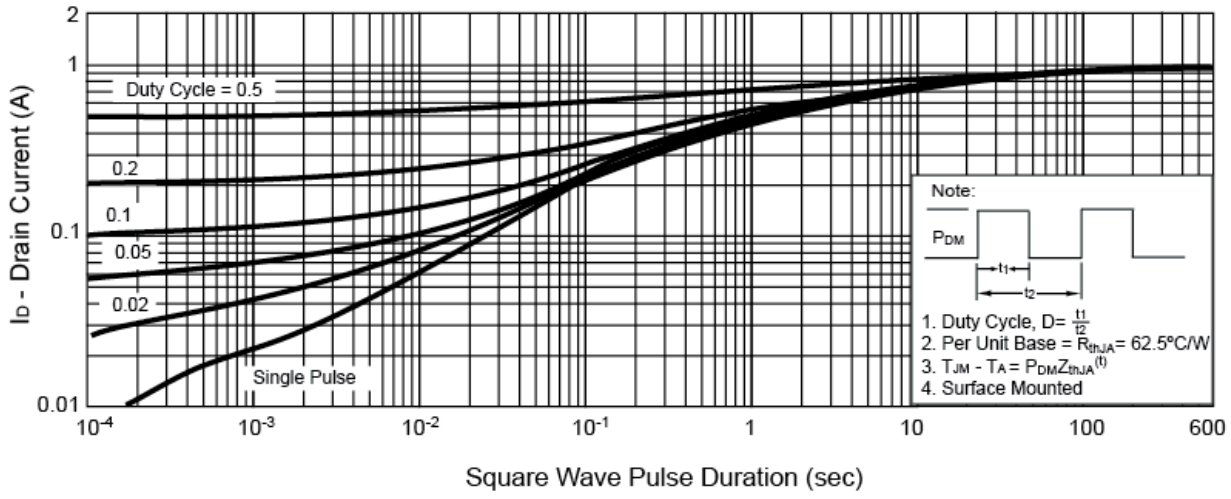

### Threshold Voltage




### Single Pulse Power




### Normalized Thermal Transient Impedance, Junction-to-Ambient



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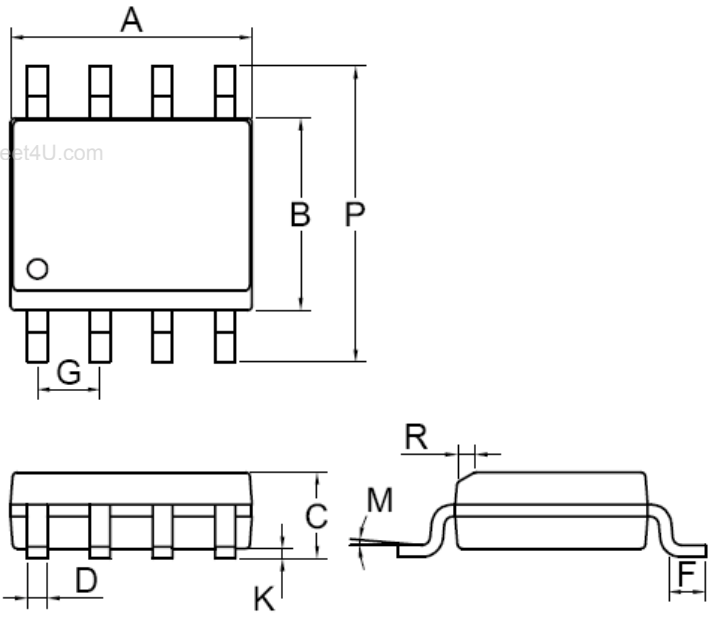
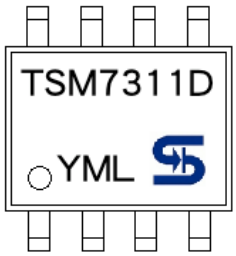
## SOP-8 Mechanical Drawing






| SOP-8 DIMENSION | | | | |
|---|---|---|---|---|
| DIM | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX. |
| A | 4.80 | 5.00 | 0.189 | 0.196 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27BSC | | 0.05BSC | |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0º | 7º | 0º | 7º |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## Marking Diagram




**Y** = Year Code
**M** = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
**L** = Lot Code

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