



TSP7N80M / TSF7N80M

800V N-Channel MOSFET

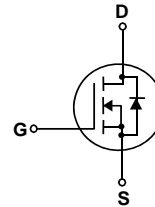
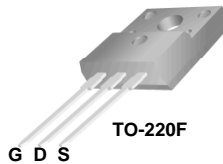
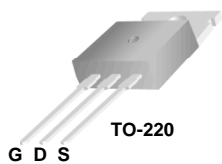
TSP7N80M / TSF7N80M

General Description

This Power MOSFET is produced using True semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 7.0A, 800V, $R_{DS(on)} = 1.9\Omega @ V_{GS} = 10V$
- Low gate charge (typical 40nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	TSP7N80M	TSF7N80M	Units
V_{DSS}	Drain-Source Voltage	800		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	7.0	7.0 *	A
		4.2	4.2 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	28	28 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	650		mJ
I_{AR}	Avalanche Current (Note 1)	7.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	16.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	167	56	W
		1.33	0.44	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	TSP7N80M	TSF7N80M	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	2.25	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

Electrical CharacteristicsT_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	800	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.8	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 640 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.5 A	--	1.4	1.9	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 3.5 A (Note 4)	--	5.7	--	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	1685	--	pF
C _{oss}	Output Capacitance		--	165	--	pF
C _{rss}	Reverse Transfer Capacitance		--	17	--	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 7.0 A, R _G = 25 Ω (Note 4, 5)	--	40	--	ns
t _r	Turn-On Rise Time		--	100	--	ns
t _{d(off)}	Turn-Off Delay Time		--	50	--	ns
t _f	Turn-Off Fall Time		--	60	--	ns
Q _g	Total Gate Charge	V _{DS} = 640 V, I _D = 7.0 A, V _{GS} = 10 V (Note 4, 5)	--	40	--	nC
Q _{gs}	Gate-Source Charge		--	9.0	--	nC
Q _{gd}	Gate-Drain Charge		--	16.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	7.0	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	28	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 7.0 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 7.0 A,	--	765	--	ns
Q _{rr}	Reverse Recovery Charge	di _F / dt = 100 A/us (Note 4)	--	6.8	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 25mH, I_{AS} = 7.0A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7.0A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

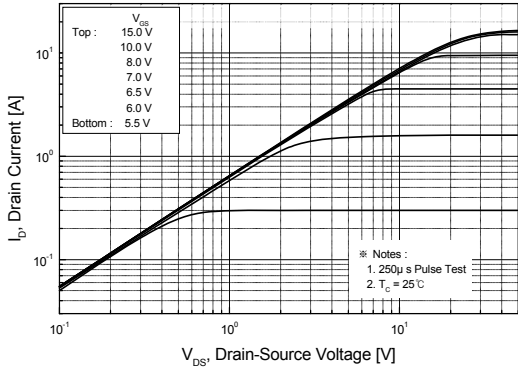


Figure 1. On-Region Characteristics

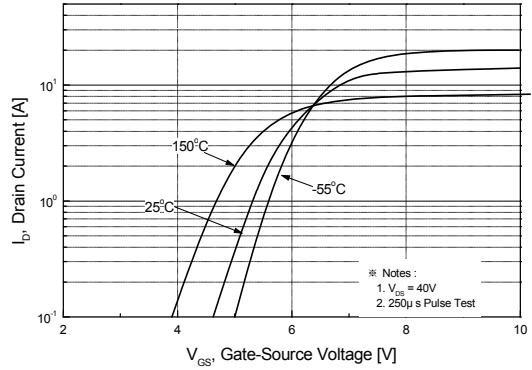


Figure 2. Transfer Characteristics

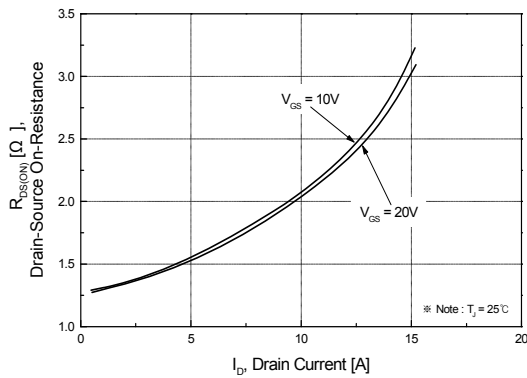


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

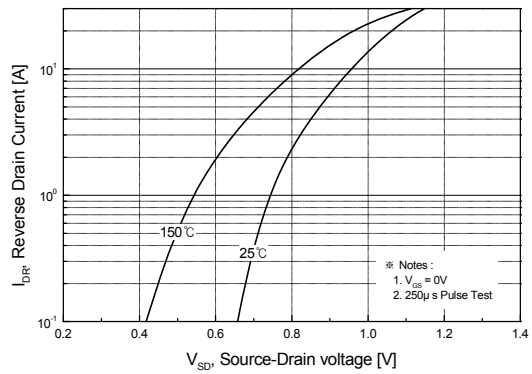


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

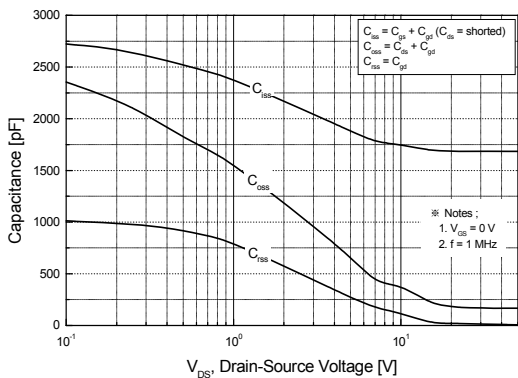


Figure 5. Capacitance Characteristics

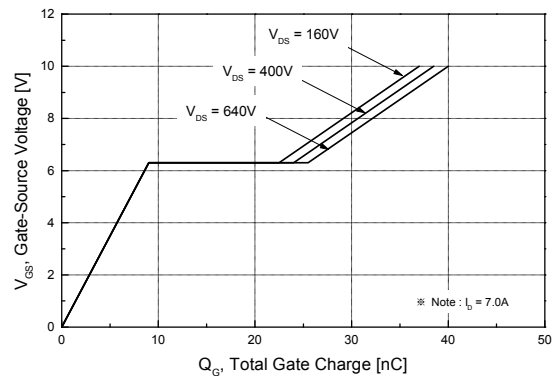


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

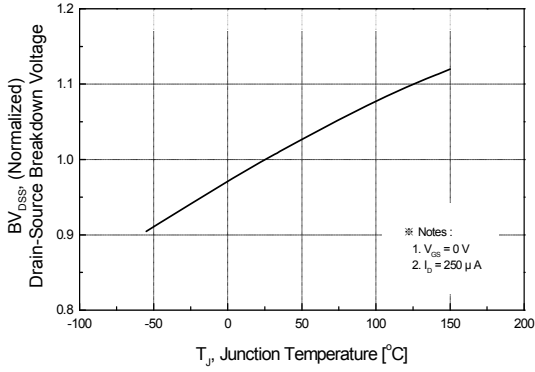


Figure 7. Breakdown Voltage Variation vs Temperature

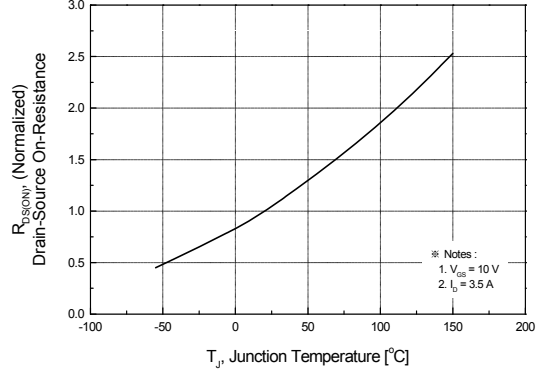


Figure 8. On-Resistance Variation vs Temperature

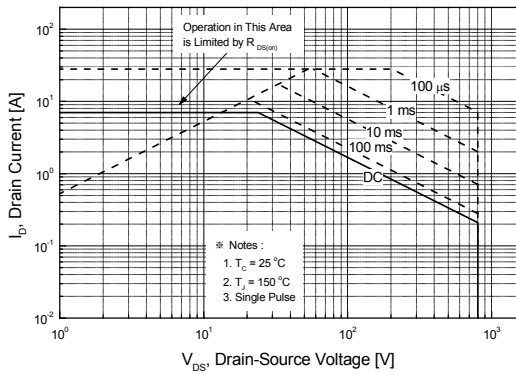


Figure 9-1. Maximum Safe Operating Area for TSP7N80M

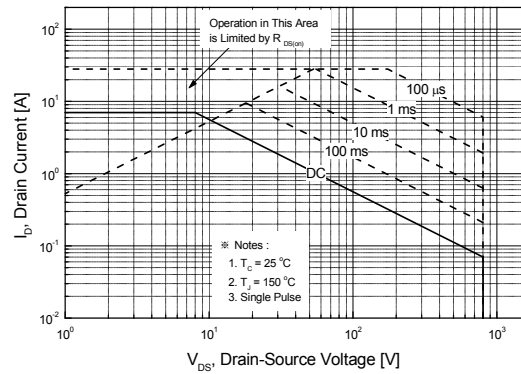


Figure 9-2. Maximum Safe Operating Area for TSF7N80M

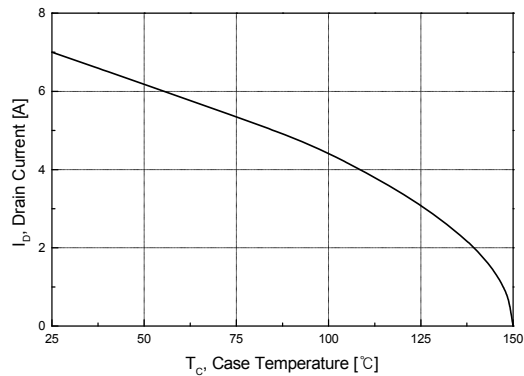


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

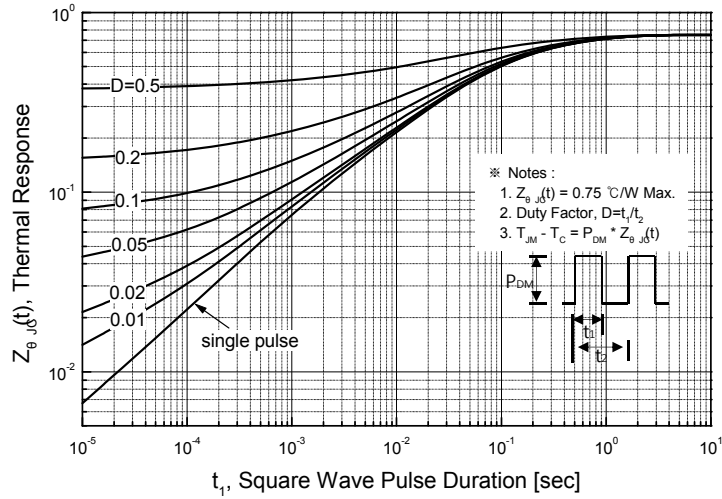


Figure 11-1. Transient Thermal Response Curve for TSP7N80M

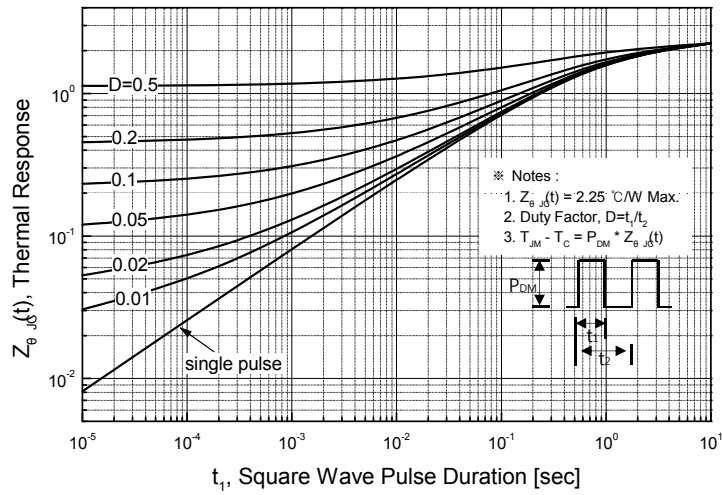
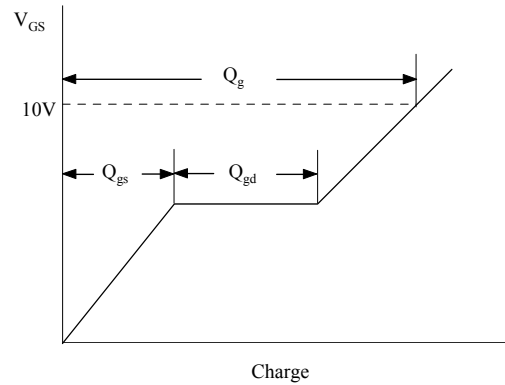
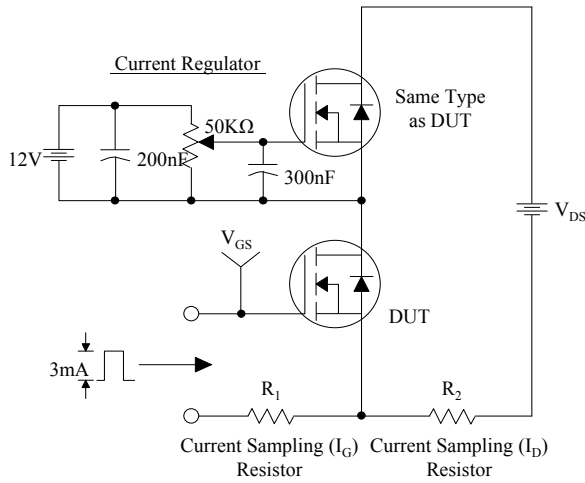
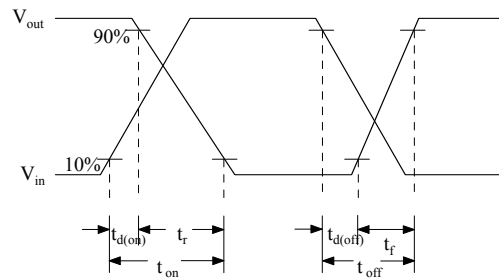
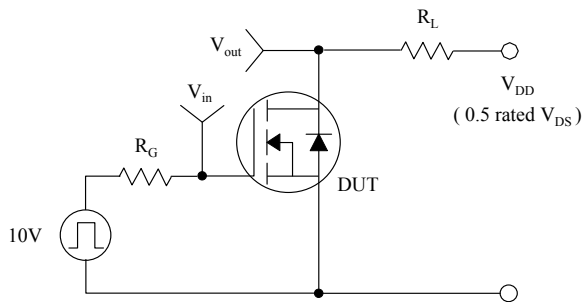


Figure 11-2. Transient Thermal Response Curve for TSF7N80M

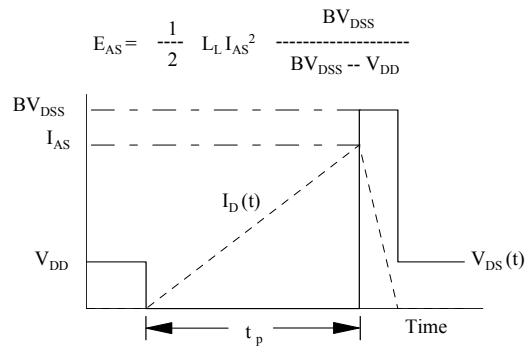
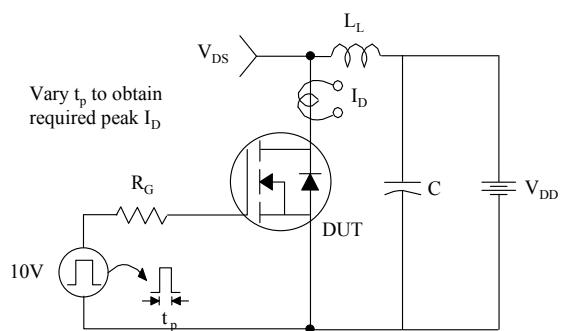
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

