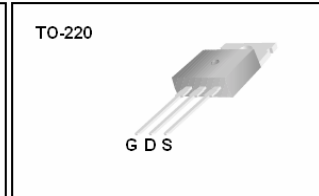
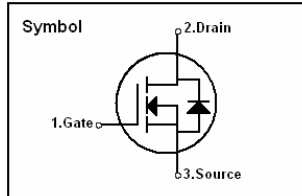


## 600V N-Channel MOSFET

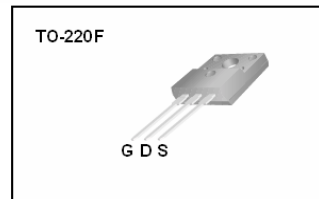
### Features

- 7.5A,600v,RDS(on)=1.2Ω@VGS=10V
- Gate charge (Typical 30nC)
- High ruggedness
- Fast switching
- 100% Avalanche Tested
- Improved dv/dt capability



### General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. These devices are well suited for high efficiency switch mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



### Absolute Maximum Ratings

Symbol	Parameter	TSP8N60M	TSF8N60M	Units
VDSS	Drain to Source Voltage	600		V
ID	Continuous Drain Current(@TC = 25°C)	7.5	7.5*	A
	Continuous Drain Current(@TC = 100°C)	4.5	4.5*	A
IDM	Drain Current Pulsed (Note 1)	30	30*	A
VGS	Gate to Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	285		mJ
EAR	Repetitive Avalanche Energy (Note 1)	15.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
PD	Total Power Dissipation(@TC = 25 °C)	165	55	W
	Derating Factor above 25 °C	1.21	0.4	W/°C
TSTG, TJ	Operating Junction Temperature & Storage Temperature	-55 ~ 150		°C
TL	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300		°C

### Thermal Characteristics

Symbol	Parameter	TSP8N60M	TSF8N60M	Units
RθJC	Thermal Resistance, Junction-to-Case	0.85	2.2	°C/W
RθCS	Thermal Resistance, Case-to-Sink Typ	0.5	--	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

# TSP8N60M/TSF8N60M

## Electrical Characteristics ( TC = 25 °C unless otherwise noted )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BVDSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = 250uA	600	--	--	V
$\Delta BVDSS / \Delta T_J$	Breakdown Voltage Temperature coefficient	ID = 250uA, referenced to 25 °C	--	0.57	--	V/°C
IDSS	Drain-Source Leakage Current	VDS = 600V, VGS = 0V	--	--	10	uA
		VDS = 480V, TC = 125 °C	--	--	100	uA
IGSS	Gate-Source Leakage, Forward	VGS = 30V, VDS = 0V	--	--	100	nA
	Gate-source Leakage, Reverse	VGS = -30V, VDS = 0V	--	--	-100	nA
<b>On Characteristics</b>						
VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250uA	2.0	--	4.0	V
RDS(ON)	Static Drain-Source On-state Resistance	VGS = 10 V, ID = 3.75A	--	1.0	1.2	$\Omega$
<b>Dynamic Characteristics</b>						
Ciss	Input Capacitance	VGS = 0 V, VDS = 25V, f = 1MHz	--	1255	--	pF
Coss	Output Capacitance		--	115	--	
Crss	Reverse Transfer Capacitance		--	14.2	--	
<b>Dynamic Characteristics</b>						
td(on)	Turn-on Delay Time	VDD = 300V, ID = 7.5A, RG = 25 $\Omega$ (Note 4, 5)	--	22	--	ns
tr	Rise Time		--	90	--	
td(off)	Turn-off Delay Time		--	76	--	
tf	Fall Time		--	44	--	
Qg	Total Gate Charge	VDS = 480V, VGS = 10V, ID = 7.5A (Note 4, 5)	--	30	--	nC
Qgs	Gate-Source Charge		--	5.2	--	
Qgd	Gate-Drain Charge(Miller Charge)		--	16.3	--	

## Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
IS	Continuous Source Current	Integral Reverse p-n Junction	--	--	7.5	A
ISM	Pulsed Source Current	Diode in the MOSFET	--	--	30	
VSD	Diode Forward Voltage	IS=7.5A, VGS =0V	--	--	1.5	V
trr	Reverse Recovery Time	IS=7.5A, VGS=0V,dIF/dt=100A/us	--	390	--	ns
Qrr	Reverse Recovery Charge	IS=7.5A, VGS=0V,dIF/dt=100A/us	--	3.3	--	uC

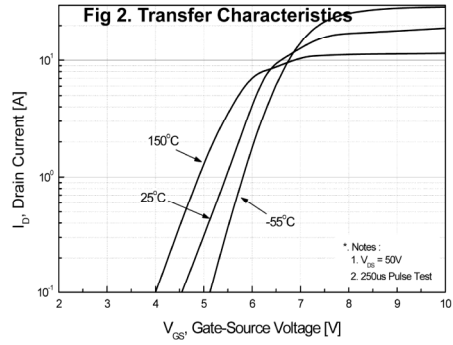
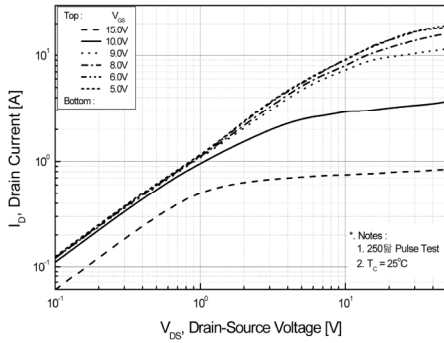
### ※ NOTES

1. Repeatability rating : pulse width limited by junction temperature
2. L = 20mH, IAS = 7.5A, VDD = 50V, RG = 50 $\Omega$  , Starting TJ = 25°C
3. ISD  $\leq$  7.5A, di/dt  $\leq$  200A/us, VDD  $\leq$  BVDSS, Starting TJ = 25°C
4. Pulse Test : Pulse Width  $\leq$  300us, Duty Cycle  $\leq$  2%
5. Essentially independent of operating temperature

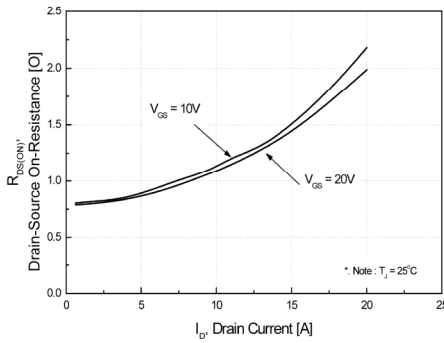


# TSP8N60M/TSF8N60M

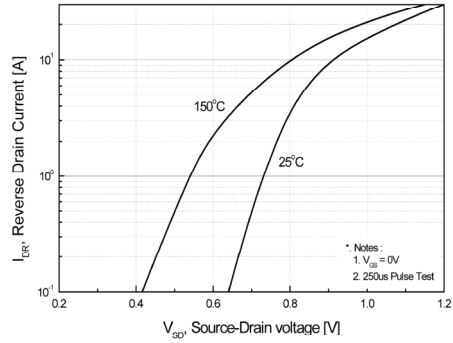
**Fig 1. On-State Characteristics**



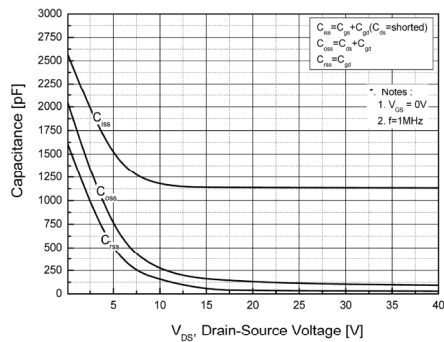
**Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage**



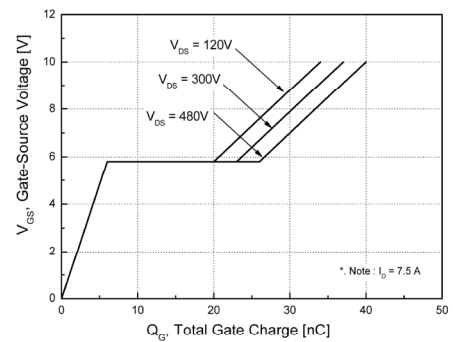
**Fig 4. On State Current vs. Reverse Drain Current**



**Fig 5. Capacitance Characteristics (Non-Repetitive)**

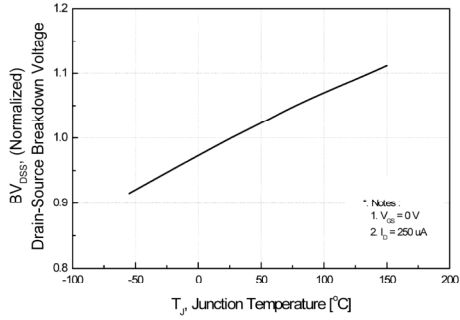


**Fig 6. Gate Charge Characteristics**

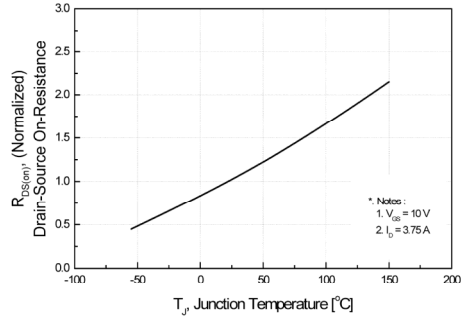


# TSP8N60M/TSF8N60M

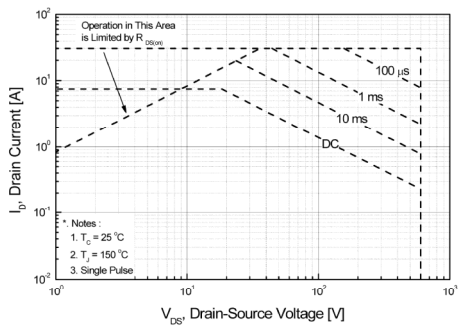
**Fig 7. Breakdown Voltage Variation vs. Junction Temperature**



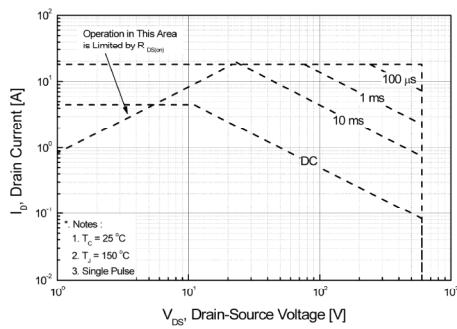
**Fig 8. On-Resistance Variation vs. Junction Temperature**



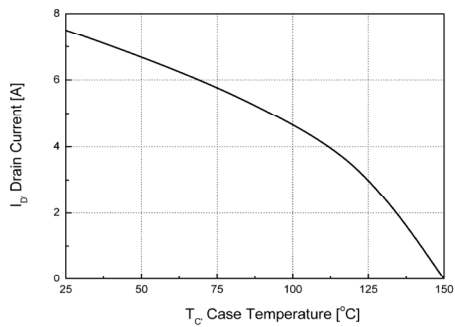
**Fig 9-1. Maximum Safe Operating Area for TSP8N60M**



**Fig 9-2. Maximum Safe Operating Area for TSF8N60M**



**Fig 10. Maximum Drain Current vs. Case Temperature**



# TSP8N60M/TSF8N60M

Fig 11-1 . Transient Thermal Response Curve for TSP8N60M

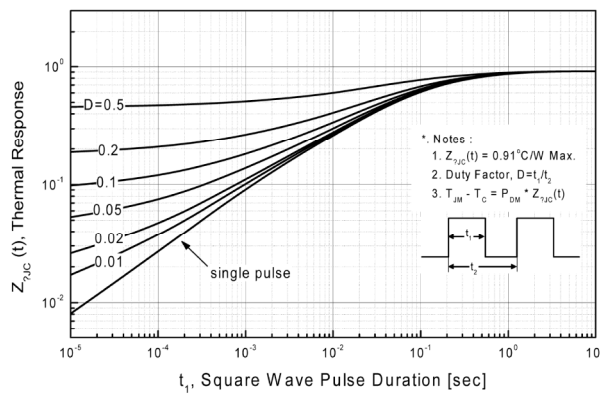
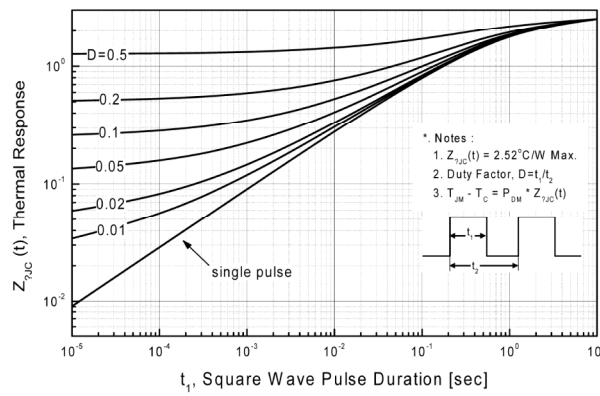


Fig 11-2 . Transient Thermal Response Curve for TSF8N60M



# TSP8N60M/TSF8N60M

Fig. 12. Gate Charge Test Circuit & Waveforms

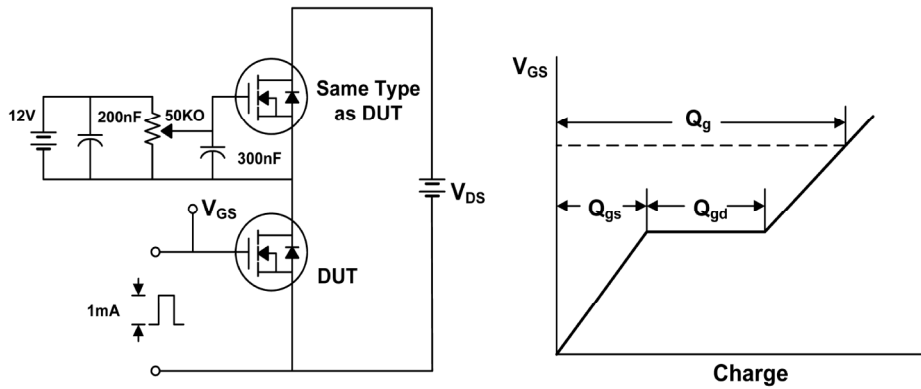


Fig. 13. Switching Time Test Circuit & Waveforms

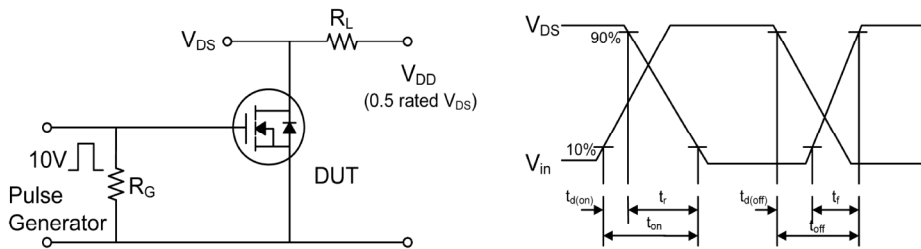
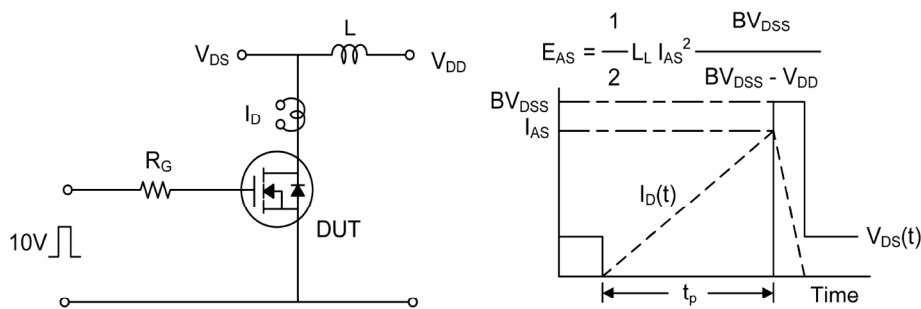


Fig. 14. Unclamped Inductive Switching Test Circuit & Waveforms



# TSP8N60M/TSF8N60M

Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

