

## FEATURES

### n Input Port

- RGB analog input port
- Full SOG and composite sync support, including copy protected signals
- High-speed 8-bit triple-ADC with low jitter PLL operates up to 220 MHz

### n Display Processing Engine

- Patent-pending Hybrid Image Resolution Converter
- Variable sharpness control
- Interlaced to progressive conversion
- Patent-pending Dynamic Frame-Rate generator (DFR) – short line storage frame extension technique eliminates short lines in output frames
- Media Window Enhancement (MWE)<sup>Note</sup>
- Peaking and coring functions for sharpness enhancement and noise reduction
- Brightness and contrast control
- Programmable 10-bit gamma correction
- sRGB support

### n Auto-Detection / Auto-Tune Support

- Auto input signal format (SOG, composite, separated HSYNC, and VSYNC)
- Input mode detection support analyzes input video signal (H/V polarity, H/V frequency, interlace/field detect) – extensive status registers support robust detection of all VESA and IBM modes

- Auto-tuning function including support for phase selection, image position, offset & gain and jitter detection

- Smart screen-fitting

### n On-screen display controller (OSD)

- Built-in OSD generator with 291 character font programmable RAM
- Internal OSD rotation degree of 90 and 270
- Supports 2/4/8 multi-color fonts
- Supports 8/16/256 color palette
- Supports 1K code attributes
- Gradient color function
- Hardware button animation function
- Pattern generator for production test
- Supports OSD MUX and alpha blending capability

### n Output Display Interface

- Supports 6/8-bit LVDS panel interface
- Supports up to SXGA display resolution with up to 135 MHz dot clock
- Spread spectrum output frequency for EMI suppression
- PWM backlight intensity control

### n DPMS Support

- Full green mode DPMS support
- Low standby power (< 16mA)

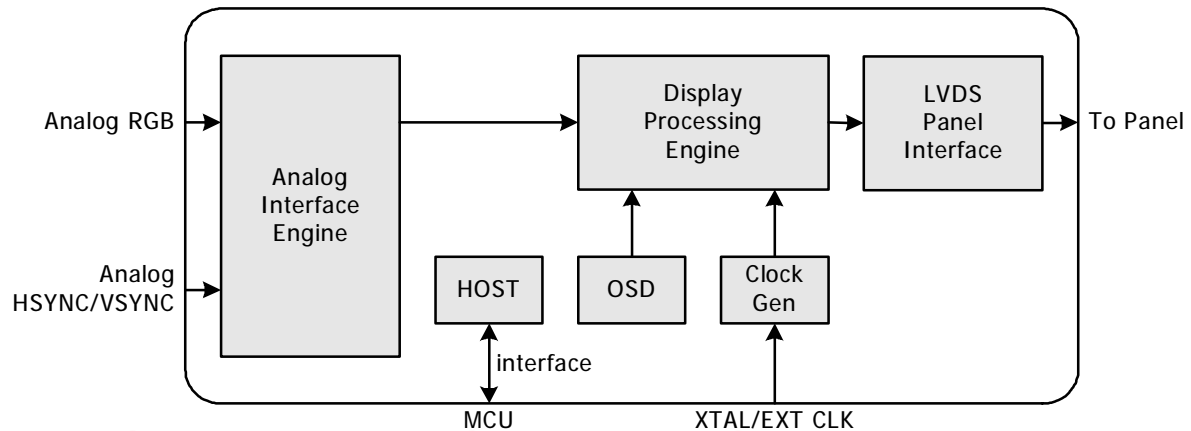
### n External Connection/Component

- Supports DDR direct bus (up to 40MHz) and serial bus (up to 400Kbit/sec)

#### Note:

The optional MWE function is available with TSU16AWK.

## BLOCK DIAGRAM



## GENERAL DESCRIPTION

The TSU16AK is total solution graphics processing IC for LCD monitors with panel resolutions up to SXGA. It is configured with a high-speed integrated triple-ADC/PLL, a high quality display processing engine, and an integrated output display interface that can support LVDS panel interface format. To further reduce system costs, the TSU16AK also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

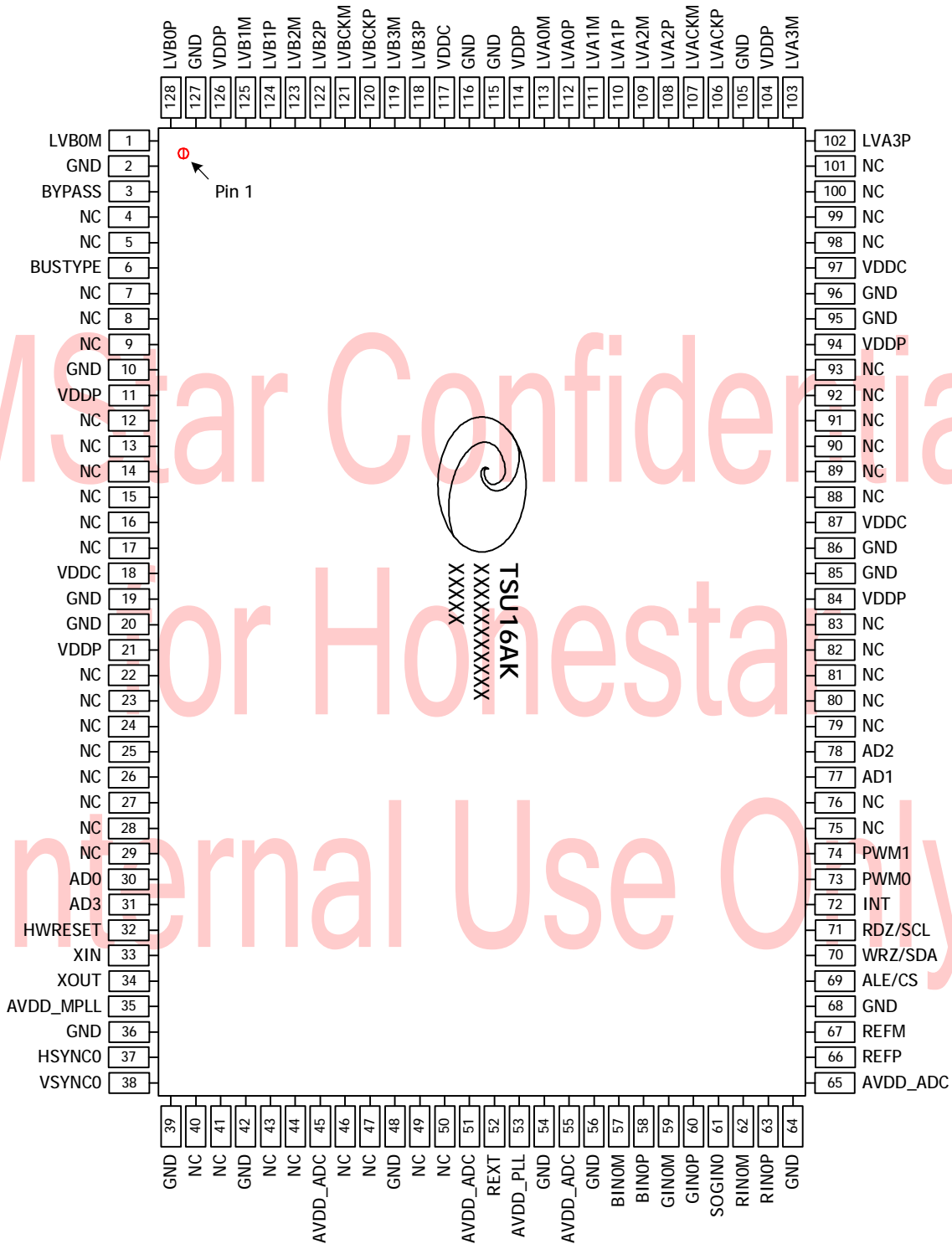
The TSU16AK incorporates the world's first coherent oversampled RGB graphics ADC in a monitor controller system<sup>1</sup>. The oversampling ADC samples the input RGB signals at a frequency that is much higher than the signal source pixel rate. This can preserve details in the video signal that ordinarily would be lost due to input signal jitter or bandwidth limitations in non-oversampled systems.

The TSU16AK also incorporates a new Dynamic Frame Rate (DFR) generator<sup>2</sup> for the digital output video to the display panel that preserves the advantages of a fixed output clock rate, while eliminating the output end of frame short-line.

<sup>1,2</sup> Patent Pending

Internal Use Only

**PIN DIAGRAM (TSU16AK)**



## PIN DESCRIPTION

### CPU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware reset; active high	32
CS	Input w/ 5V-tolerant	3 Wire Serial Bus Chip Select; active high	69
SDA	I/O w/ 5V-tolerant	3 Wire Serial Bus Data; 4mA driving strength	70
SCL	Input w/ 5V-tolerant	3 Wire Serial Bus Clock	71
INT	Output	CPU interrupt; 4mA driving strength	72
AD3	I/O w/ 5V-tolerant	DDR direct bus AD3; 4mA driving strength	31
AD2	I/O w/ 5V-tolerant	DDR direct bus AD2; 8mA driving strength	78
AD1	I/O w/ 5V-tolerant	DDR direct bus AD1; 8mA driving strength	77
AD0	I/O w/ 5V-tolerant	DDR direct bus AD0; 4mA driving strength	30
ALE	I w/ 5V-tolerant	DDR direct bus ALE; active high	69
RDZ	I w/ 5V-tolerant	DDR direct bus RDZ; active low	71
WRZ	I w/ 5V-tolerant	DDR direct bus WRZ; active low	70
BUSTYPE	Input (not 5V-tolerant)	Bus type Y Low : Serial bus Y High : DDR Direct bus	6

### Analog Interface

Pin Name	Pin Type	Function	Pin
HSYNCO	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC input	37
VSYNCO	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC input	38
REFP		Internal ADC top de-coupling pin	66
REFM		Internal ADC bottom de-coupling pin	67
RINOP	Analog Input	Analog red input	63
RINOM	Analog Input	Reference ground for analog red input	62
SOGINO	Analog Input	Sync-on-green input	61
GINOP	Analog Input	Analog green input	60
GINOM	Analog Input	Reference ground for analog green input	59
BINOP	Analog Input	Analog blue input	58
BINOM	Analog Input	Reference ground for analog blue input	57
REXT		External resistor 390 ohm to AVDD_ADC	52

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	A-Link Negative LVDS Differential Data Output	113
LVA0P	Output	A-Link Positive LVDS Differential Data Output	112
LVA1M	Output	A-Link Negative LVDS Differential Data Output	111
LVA1P	Output	A-Link Positive LVDS Differential Data Output	110
LVA2M	Output	A-Link Negative LVDS Differential Data Output	109
LVA2P	Output	A-Link Positive LVDS Differential Data Output	108
LVA3M	Output	A-Link Negative LVDS Differential Data Output	103
LVA3P	Output	A-Link Positive LVDS Differential Data Output	102
LVACKM	Output	A-Link Negative LVDS Differential Clock Output	107
LVACKP	Output	A-Link Positive LVDS Differential Clock Output	106
LVB0M	Output	B-Link Negative LVDS Differential Data Output	1
LVB0P	Output	B-Link Positive LVDS Differential Data Output	128
LVB1M	Output	B-Link Negative LVDS Differential Data Output	125
LVB1P	Output	B-Link Positive LVDS Differential Data Output	124
LVB2M	Output	B-Link Negative LVDS Differential Data Output	123
LVB2P	Output	B-Link Positive LVDS Differential Data Output	122
LVB3M	Output	B-Link Negative LVDS Differential Data Output	119
LVB3P	Output	B-Link Positive LVDS Differential Data Output	118
LVBCKM	Output	B-Link Negative LVDS Differential Clock Output	121
LVBCKP	Output	B-Link Positive LVDS Differential Clock Output	120

GPO Interface

Pin Name	Pin Type	Function	Pin
PWM1	Output	PWM1; 4mA driving strength	74
PWM0	Output	PWM0; 4mA driving strength	73

Misc. Interface

Pin Name	Pin Type	Function	Pin
BYPASS		For External Bypass Capacitor	3
XIN	Crystal Oscillator Input	Xin	33
XOUT	Crystal Oscillator Output	Xout	34

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_ADC	3.3V Power	ADC Power	45, 51, 55, 65
AVDD_PLL	3.3V Power	PLL Power	53
AVDD_MPLL	3.3V Power	MPLL Power	35
VDDP	3.3V Power	Digital Output Power	11, 21, 84, 94, 104, 114, 126
VDDC	1.8V Power	Digital Core Power	18, 87, 97, 117
GND	Ground	Ground	2, 10, 19, 20, 36, 39, 42, 48, 54, 56, 64, 68, 85, 86, 95, 96, 105, 115, 116, 127

No Connects

Pin Name	Pin Type	Function	Pin
NC		No Connect. Leave These Pins Floating.	4, 5, 7-9, 12-17, 22-29, 40, 41, 43, 44, 46, 47, 49, 50, 75, 76, 79-83, 88-93, 98-101

for Honestar  
Internal Use Only

## ELECTRICAL SPECIFICATIONS

### Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
Resolution		8		Bits
DC ACCURACY				
Differential Nonlinearity		±0.5	+1.50/-1.0	LSB
Integral Nonlinearity		±1		LSB
No Missing Codes		Guaranteed		
ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	220			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		220	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V <sub>IH</sub> )	2.5			V
Input Voltage, Low (V <sub>IL</sub> )			0.8	V
Input Current, High (I <sub>IH</sub> )			-1.0	uA
Input Current, Low (I <sub>IL</sub> )			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V <sub>OH</sub> )	VDDP-0.1			V
Output Voltage, Low (V <sub>OL</sub> )			0.1	V
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
Channel to Channel Matching		0.5%		Full-Scale

Specifications are subjected to change without notice.

### Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V <sub>VDD_33</sub>	-0.3		3.6	V
1.8V Supply Voltages	V <sub>VDD_18</sub>	-0.3		1.98	V
Input Voltage (5V tolerant inputs)	V <sub>IN5Vtol</sub>	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V <sub>IN</sub>	-0.3		V <sub>VDD_33</sub>	V
Ambient Operating Temperature	T <sub>A</sub>	0		70	°C
Storage Temperature	T <sub>STG</sub>	-40		150	°C
Junction Temperature	T <sub>J</sub>			150	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ <sub>JA</sub>		34		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ <sub>JC</sub>		6.0		°C/W

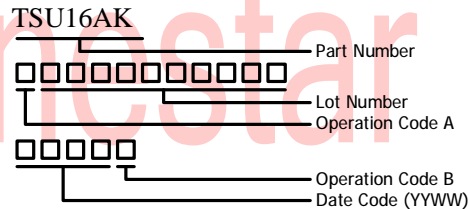
Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
TSU16AK	0°C to +70°C	PQFP	128
TSU16AWK	0°C to +70°C	PQFP	128
TSU16AK-LF	0°C to +70°C	PQFP	128
TSU16AWK-LF	0°C to +70°C	PQFP	128

Note: Product suffix "LF" represents lead-free version, and "W" represents MWE function.

### MARKING INFORMATION



### DISCLAIMER

MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.



Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. TSU16AK comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

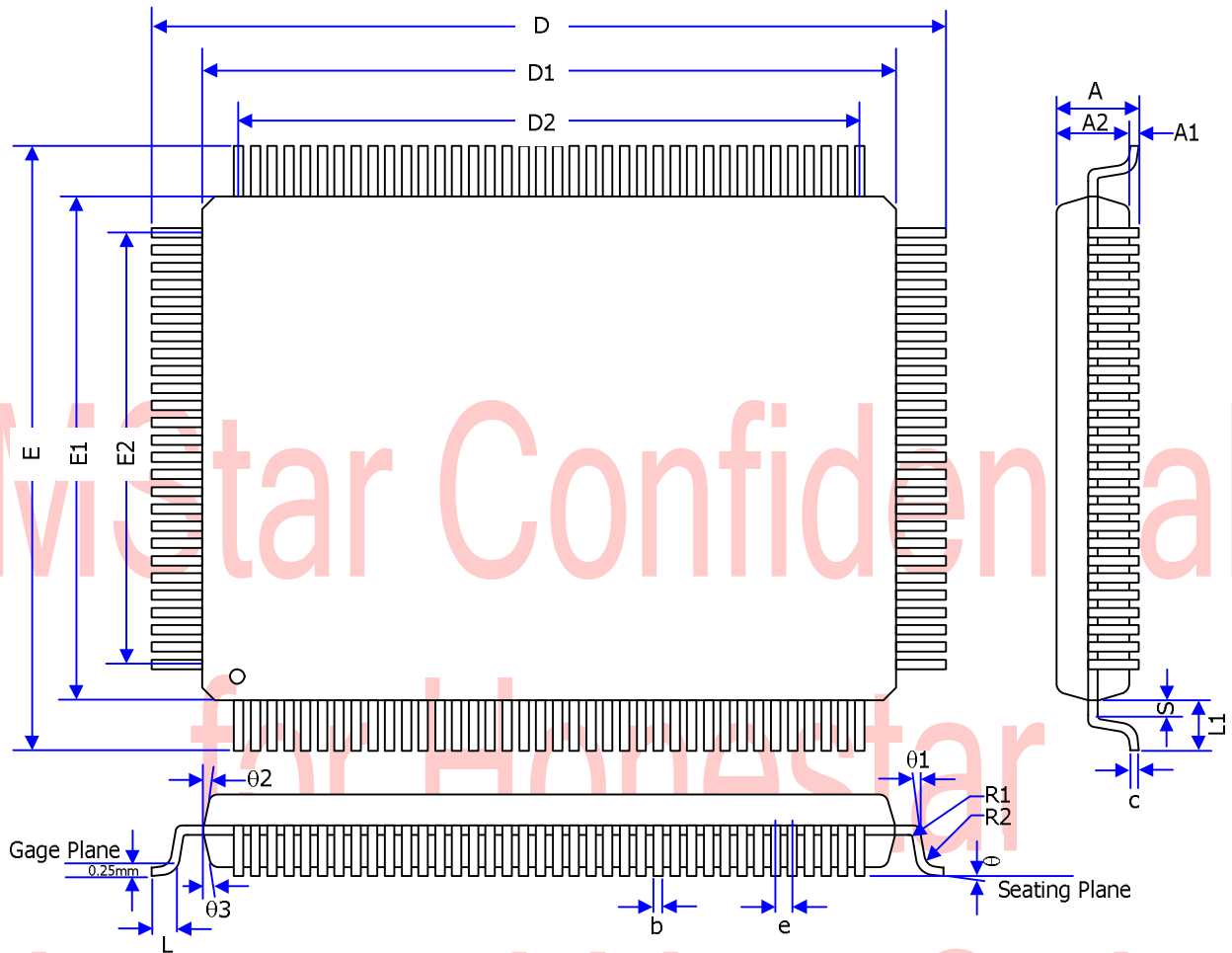


**REVISION HISTORY**

Document	Description	Date
TSU16AK_ds_v01	ÿ Initial release	Aug 2004
TSU16AK_ds_v02	ÿ Updated Register Table	Sep 2004
TSU16AK_ds_v03	ÿ Updated MWE related information ÿ Added lead-free information to Ordering Guide ÿ Updated Register Table	Oct 2004

MStar Confidential  
for Honestar  
Internal Use Only

**MECHANICAL DIMENSIONS**



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.40	-	-	0.134
A1	0.25	-	-	0.010	-	-
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20			0.913		
D1	20.00			0.787		
D2	18.50			0.728		
E	17.20			0.677		
E1	14.00			0.551		
E2	12.50			0.492		
R1	0.13	-	-	0.005	-	-
R2	0.13	-	0.30	0.005	-	0.012

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
$\theta$	0°	-	7°	0°	-	7°
$\theta_1$	0°	-	-	0°	-	-
$\theta_2, \theta_2$ (Alloy)	7° Ref			7° Ref		
$\theta_2, \theta_2$ (Copper)	15° Ref			15° Ref		
b	0.170	0.200	0.270	0.007	0.008	0.011
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.50 BSC.			0.020 BSC.		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 Ref			0.063 Ref		
S	0.20	-	-	0.008	-	-

## REGISTER DESCRIPTION

General Control Register			
Index	Mnemonic	Bits	Description
00h	REGBK	7:0	Default : <span style="border: 1px solid black; padding: 2px;"> </span> Access : R/W
	PORR	7	Power On Reset Ready (read only). 0: Not ready. 1: Ready.
		6:4	Reserved.
	AINC	3	Serial bus address auto increase. 0: Enable. 1: Disable.
	BUST	2	BUS type (read only). 0: Direct bus. 1: Serial bus.
	REGBK[1:0]	1:0	Register Bank Select. 00: Register of digital image processor. 01: Register of internal ADC, DVI/HDCP receiver. 10: Register of timing controller. 11: Register of MWE function.

### ADC Register (Bank = 01)

ADC Register (Bank=01)			
Index	Mnemonic	Bits	Description
01h	DBFC	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	DBVB	0	Double Buffer load at Vertical Blanking. 0: Disable. 1: Enable.
02h	PLLDIVM	7:0	Default : 0x69 Access : R/W
	PLLDIV[11:4]	7:0	PLL Divider ratio. When bank 1 register 3Dh[4] = 0 ADC PLL will multiply the horizontal line frequency by PLLDIV[11:0] + 3 to generate the ADC sampling clock. When bank 1 register 3Dh[4] = 1 ADC PLL will multiply the horizontal line frequency by (PLLDIV[11:0] + 3)*2 to generate the ADC sampling clock.
03h	PLLDIVL	7:0	Default : 0x50 Access : R/W
	PLLDIV[3:0]	7:4	PLL Divider ratio. Please see the description of PLLDIV[11:4].
	-	3	Reserved.
	STAT[2:0]	2:0	Status select. Selects 1/8 internal PLL status values to read from register 16h.

ADC Register (Bank=01)				
04h	REDGAIN	7:0	Default : 0x80	Access : R/W
	REDGAIN	7:0	Red channel Gain adjust.	
05h	GRNGAIN	7:0	Default : 0x80	Access : R/W
	GRNGAIN	7:0	Green channel Gain adjust.	
06h	BLUGAIN	7:0	Default : 0x80	Access : R/W
	BLUGAIN	7:0	Blue channel Gain adjust.	
07h	REDOFST	7:0	Default : 0x80	Access : R/W
	REDOFST	7:0	Red channel Offset adjust.	
08h	GRNOFST	7:0	Default : 0x80	Access : R/W
	GRNOFST	7:0	Green channel Offset adjust.	
09h	BLUOFST	7:0	Default : 0x80	Access : R/W
	BLUOFST	7:0	Blue channel Offset adjust.	
0Ah	CLPACE	7:0	Default: 0x05	Access : R/W
	CLPACE	7:0	Clamp Placement based on ADC clock.	
0Bh	CLDUR	7:0	Default : 0x05	Access : R/W
	CLDUR	7:0	Clamp Duration based on ADC clock.	
0Ch	GCTRL	7:0	Default : 0x82	Access : R/W
	HSP	7	Input HSYNC Polarity. 0: Active low. 1: Active high.	
	ECLK	6	External Clock. 0: ADC clock from internal ADC PLL. 1: ADC clock from external clock.	
	HSLE	5	HS Lock Edge. Determines which edge of HSYNC the ADC PLL will lock to, assuming HSP is set correctly. 0: Leading edge of HSYNC. 1: Trailing edge of HSYNC.	
	CLPE	4	Clamp reference Edge. 0: Trailing edge of HSYNC. 1: Leading edge of HSYNC.	
	CCDIS	3	Disable PLL watchdog timer. 0: Always enable clamp. 1: Disable clamp during active coast.	
	WDIS	2	Disable watchdog timer. 0: Enable PLL watchdog timer. A watchdog timer is used to reset the ADC PLL when the PLL remains much higher than PLLDIV*HSYNC_FREQ for a predetermined period. See WDTOL (Register 30h).	

ADC Register (Bank=01)			
			1: Disable PLL watchdog timer (should only be used when DPL_S = 0).
	CSTP	1	Coast Polarity. 0: Active low. 1: Active high.
	DRBS	0	DVI input Red/Blue swap (DVI features only). 0: Normal. 1: Swap.
0Dh	BWCOEF	7:0	Default : 0x02      Access : R/W
	DMODE[1:0]	7:6	Damping coefficient mode control. 00: Default value – backward compatibility mode. 01: Reserved. 10: Automatic DCOEF control (recommended mode). 11: Reserved.
	BWCOEF[5:0]	5:0	PLL loop filter control.
0Eh	FCOEF	7:0	Default : 0x09      Access : R/W
		7:5	Reserved.
	FREQCOEF[4:0]	4:0	PLL loop filter control.
0Fh	DCOEF	7:0	Default : 0x05      Access : R/W
		7:4	Reserved.
	DAMPCOEF[3:0]	3:0	PLL loop filter control.
10h	CLKCTRL1	7:0	Default : 0x08      Access : R/W
	-	7	Reserved.
	PHASE[6:0]	6:0	Clock Phase adjust (should be always set to PHASECC + 8).
11h	CLKCTRL2	7:0	Default : 0x00      Access : R/W
	-	7	Reserved.
	PHASECC[6:0]	6:0	Clock phase adjust for ADC sampling time point. Phase is adjustable between 0 and 360° in 5.6° steps.
12h	VCOCTRL	7:0	Default : 0x15      Access : R/W
	PDGT	7	Phase digitizer frequency compensation disable.
	DPL_S[2:0]	6:4	VCO range. Sets ADC PLL frequency range.
	SETCNT[3:0]	3:0	Setting time for ADC PLL phase detector, in ADC clock periods.

ADC Register (Bank=01)				
13h	RT_CTL	7:0	Default : 0x10	Access : R/W
	SFTF	7	DVI error correction enable (DVI feature only). 0: Error correction disable. 1: Error correction enable.	
	DEFE	6	DVI R/G/B alignment edge on DE (DVI feature only). 0: DE leading edge. 1: DE trailing edge.	
	WDF	5	DVI word alignment edge on DE (DVI feature only). 0: Disable. 1: Enable.	
	RT_CTL[4:0]	4:0	Resistor termination control for DVI (DVI feature only).	
14h	SOG_LVL	7:0	Default : 0x10	Access : R/W
	RMID	7	Middle clamp of Red Channel. 0: Disable. 1: Enable (used when YPbPr input).	
	BMID	6	Middle clamp of Blue Channel. 0: Disable. 1: Enable (used when YPbPr input).	
	SOGFLT	5	SOG Filter (low-pass filter on SOG input). 0: Disable. 1: Enable.	
	SOG_LVL[4:0]	4:0	SOG trigger level. 5'b00000: 10mV; 5'b00001: 20mV; ... .. 5'b11110: 310mV; 5'b11111: 320mV.	
15h	HS_LVL	7:0	Default: 0x00	Access : R/W
	ADCBW[2:0]	7:5	ADC Bandwidth.	
	-	4	Reserved.	
	-	3	Reserved.	
	HL_LVL[2:0]	2:0	HSYNC trigger level.	
16h	STATUS1	7:0	Default: -	Access : RO
	Note: PLL status is read based on STAT[2:0] (Reg_03h).			
		7	When STAT[2:0] = 000: LOCK: PLL Lock status. If 1, PLL is in lock.	
		6	IQ: PLL Lock status. If 1, PLL is in stable lock, and now capable of filtering spurious HSYNC inputs.	
	5	SLOW.		

ADC Register (Bank=01)				
		4	FAST.	
		3:0	Reserved.	
17h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
18h	STATUS5	7:0	Default: -	Access : RO
	RCMP[7:0]	7:0	DVI termination resistor status in 2's complement (DVI feature only). Positive value represents resistor value on low side, and RT_CTL needs to adjust to higher values for compensation. Negative value represents resistor value on high side, and RT_CTL needs to adjust to lower values for compensation.	
19h	STATUS4	7:0	Default:	Access : RO
	PH_STAT[7:0]	7	DVI phase status indicator in 2's complement (DVI feature only).	
1Ah	STATUS5	7:0	Default : -	Access : RO
	PH_STAT[15:8]	7	DVI phase status indicator in 2's complement (DVI feature only).	
1Bh	DVI_PHR	7:0	Default : 0x80	Access : R/W
	OVPB	7	Freeze and override DVI red channel PLL phase selection with OVPB[6:0].	
	OVPHR	6:0		
1Ch	DVI_PHG	7:0	Default : 0x80	Access : R/W
	OVPB	7	Freeze and override DVI red channel PLL phase selection with OVPB[6:0].	
	OVPHG	6:0		
1Dh	DVI_PHB	7:0	Default : 0x80	Access : R/W
	OVPB	7	Freeze and override DVI red channel PLL phase selection with OVPB[6:0].	
	OVPHB	6:0		
1Eh	DVI_ERST	7:0	Default : 0x00	Access : R/W
	DRR_ST[7:0]	7:0	DVI bit error status indicator.	
1Fh	DVI_ERTH	7:0	Default : 0x00	Access : R/W
	ERR_TH[7:0] / CLPSKIP[7:0]	7:0	DVI bit error tolerance threshold. / Clamp skipping on/select in ADC mode.	
	CLPSKIP[7]	7	Clamp skipping on.	
	CLPSKIP[3:0]	3:0	Clamping skipping select.	
20h	TESTEN	7:0	Default : 0x00	Access : R/W
	TESTEN	7	Enable Test Mode. 0: Disable. 1: Enable.	

ADC Register (Bank=01)				
	-	6	Reserved.	
	ERRCHSEL[1:0]	5:4	Channel select for DVI error status indicator (DVI feature only). 00: Red channel. 01: Green channel. 10: Blue channel. 11: Reserved.	
	ERRD	3	DVI bit error status indicator (ERR_ST) enable (DVI feature only). 0: Normal. 1: Read status.	
	RDST	2	Terminator resistance status (RCMP) and DVI phase status enable (DVI feature only). 0: Normal. 1: Read status.	
	PHSEL[1:0]	1:0	Channel Select for DVI phase status (DVI feature only). 00: Red channel. 01: Green channel. 10: Blue channel. 11: Reserved.	
21h	~ -	7:0	Default : -	Access : -
2Ch	-	7:0	Reserved.	
2Dh	TESTMOD	7:0	Default : 0x06	Access : R/W
	-	7	Reserved.	
	-	6:5	Reserved.	
	TESTMOD[4:0]	4:0	LVDS/RSDS differential output swing control. 5'b01000: 5.0mA for LVDS/ 2.5mA for RSDS 5'b00111: 4.6mA for LVDS/ 2.3mA for RSDS 5'b00110: 4.2mA for LVDS/ 2.1mA for RSDS	
2Eh	~ -	7:0	Default : -	Access : -
2Fh	-	7:0	Reserved.	
30h	PLLCTRLV	7:0	Default : 0xC6	Access : R/W
	WDTOL[1:0]	7:6	PLL Watchdog threshold.	
	IQCLR_TH[2:0]	5:3	PLL unstable lock threshold.	
	IQSET_TH[2:0]	2:0	PLL stable lock threshold.	
31h	~ -	7:0	Default : -	Access : -
3Ch	-	7:0	Reserved.	
3Dh	DAC_CTRL	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved	



ADC Register (Bank=01)			
	CMPATEN	4	Compatible bit.
	-	3:0	Reserved.
31h ~ FFh	-	7:0	Default : - Access : -
	-	7:0	Reserved.

Digital Image Processor Register (Bank = 00)

Digital Image Processor Register (Bank=00)			
Index	Mnemonic	Bits	Description
01h	DBFC	7:0	Default : 0x80 Access : R/W
		7:3	Reserved.
	DBL[1:0]	2:1	Double buffer load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.
	DBC	0	Double buffer control. 0: Double buffer disable. 1: Double buffer enable.
02h	ISELECT	7:0	Default : 0x00 Access : R/W
	NIS	7	Output lock mode. 0: Lock input (input signal exits). 1: Free-run (no input signal).
	STYPE[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).
	COMP	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.
	CSC	3	CSC function. 0: Disable (RGB -> RGB). 1: Enable (YCbCr -> RGB).
	IHSU	2	Input Sync Usage. When ISEL=00 or 01: 0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel. 1: Use HSYNC only. When ISEL=10:

Digital Image Processor Register (Bank=00)			
			0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL=11: 0: Normal. 1: Output Black at blanking.
	ISEL[1:0]	1:0	00: Analog 1. 01: Analog 2. 10: DVI. 11: Video.
03h	-	7:0	Default : -      Access : -
	-	7:0	Reserved.
04h	IPCTRL2	7:0	Default : 0x18      Access : R/W
	DHSR	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.
	DEON	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.
	IVSD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC (recommended). 1: No delay.
	HSE	4	Input HSYNC reference edge select. 0: From HSYNC leading edge, default value. 1: From HSYNC tailing edge.
	VSE	3	Input VSYNC reference edge select. 0: From VSYNC leading edge, default value. 1: From VSYNC tailing edge.
	ESLS	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.
	VWRP	1	Input image Vertical wrap. 0: Disable. 1: Enable.
	HWRP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.
05h	SPRVST-L	7:0	Default : 0x10      Access : R/W, DB
	SPRVST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.

Digital Image Processor Register (Bank=00)				
06h	SPRVST-H	7:0	Default : 0x00	Access : R/W, DB
		7:3	Reserved.	
	SPRVST[10:8]	2:0	Image vertical sample start point, count by input HSYNC. When Reg. 52, 51, 50 < 90 00 00, SPRHST is multiplied by 2 internally.	
07h	SPRHST-L	7:0	Default : 0x01	Access : R/W, DB
	SPRHST[7:0]	7:0	Image horizontal sample start point, count by input dot clock.	
08h	SPRHST-H	7:0	Default : 0x00	Access : R/W, DB
	SPRHSTLSB	7	Back 1 LSB, sample range will move 1 pixel left.	
	-	6	Reserved.	
	-	5	Reserved.	
	-	4	Reserved.	
	SPRGST[11:8]	3:0	Image horizontal sample start point, count by input dot clock.	
	09h	SPRVDC-L	7:0	Default : 0x10
SPRVDC[7:0]		7:0	Image vertical resolution (vertical display enable area count by line).	
0Ah	SPRVDC-H	7:0	Default: 0x00	Access : R/W
		7:3	Reserved.	
	SPRVDC[10:8]	2:0	Image vertical resolution (vertical display enable area count by line). When Reg. 52, 51, 50 < 90 00 00, SPRVST is multiplied by 2 internally.	
0Bh	SPRHDC-L	7:0	Default : 0x10	Access : R/W
	SPRHDC[7:0]	7:0	Image horizontal resolution (horizontal display enable area count by pixel).	
0Ch	SPRHDC-L	7:0	Default : 0x00	Access : R/W
		7:4	Reserved.	
	SPRHDC[11:8]	3:0	Image horizontal resolution (horizontal display enable area count by pixel).	
0Dh ~	-	7:0	Default : -	Access : -
0Eh	-	7:0	Reserved.	
0Fh	LYL	7:0	Default : 0x00	Access : R/W
		7:5	Reserved.	
	3LVRCEN	4	3 Line Vertical Resolution Conversion Enable.	
	LYL[3:0]	3:0	Lock Y Line.	
10h	DEVST-L	7:0	Default : 0x00	Access : R/W

Digital Image Processor Register (Bank=00)			
	DEVST[7:0]	7:0	Output DE Vertical Start.
11h	DEVST-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	DEVST[10:8]	2:0	See description for DEVST[7:0].
12h	DEHST-L	7:0	Default : 0x03 Access : R/W
	DEHST[7:0]	7:0	Output DE Horizontal Start.
13h	DEHST-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	DEHST[10:8]	2:0	See description for DEHST[7:0].
14h	DEVEND-L	7:0	Default : 0x06 Access : R/W
	DEVEND[7:0]	7:0	Output DE Vertical END.
15h	DEVEND-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	DEVEND[10:8]	2:0	See description for DEVEND[7:0].
16h	DEHEND-L	7:0	Default : 0x00 Access : R/W
	DEVEND[7:0]	7:0	Output DE Horizontal END.
17h	DEHEND-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	DEVEND[10:8]	2:0	See description for DEVEND[7:0].
18h	OIHST-L	7:0	Default : 0x00 Access : R/W
	OIHST[7:0]	7:0	Output Image window Horizontal Start.
19h	OIHST-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	OIHST[10:8]	2:0	See description for OIHST[7:0].
1Ah	OIVEND-L	7:0	Default : 0x06 Access : R/W
	OIVEND[7:0]	7:0	Output Image window Vertical END.
1Bh	OIVEND-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	OIVEND[10:8]	2:0	See description for OIVEND[7:0].
1Ch	OIHEND-L	7:0	Default : 0x00 Access : R/W
	OIHEND[7:0]	7:0	Output Image window Horizontal END.
1Dh	OIHEND-H	7:0	Default : 0x00 Access : R/W
		7:3	Reserved.
	OIHEND[10:8]	2:0	See description for OIHEND[7:0].
1Eh	VDTOT-L	7:0	Default : 0x03 Access : R/W

Digital Image Processor Register (Bank=00)			
	VDTOT[7:0]	7:0	Output Vertical Total.
1Fh	VDTOT-H	7:0	Default : 0x00      Access : R/W
		7:3	Reserved.
	VDTOT[10:8]	2:0	See description for VDTOT[7:0].
20h	VSST-L	7:0	Default : 0x03      Access : R/W
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS=1).
21h	VSST-H	7:0	Default : 0x00      Access : R/W
		7:4	Reserved.
	VSRU	3	VSYNC Register Usage. 0: Registers 20h – 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No signal VSYNC. Registers 22h and 23h are used to define minimum H total.
	VSST[10:8]	2:0	See description for VSST[7:0].
22h	VSEND-L	7:0	Default : 0x06      Access : R/W
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1).
23h	VSEND-H	7:0	Default : 0x00      Access : R/W DB
		7:3	Reserved.
	VSEND[10:8]	2:0	See description for VSEND[7:0].
24h	HDTOT-L	7:0	Default : 0x03      Access : R/W DB
	HDTOT[7:0]	7:0	Output Horizontal Total.
25h	HDTOT-H	7:0	Default : 0x00      Access : R/W
		7:4	Reserved.
	HDTOT[11:8]	3:0	See description for HDTOT[7:0].
26h	HSEND	7:0	Default : 0x00      Access : R/W
	HSEND[7:0]	7:6	Output HSYNC Pulse width.
27h	OSCTRL1	7:0	Default : 0x4C      Access : R/W
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 – 0x23).
	-	6	Reserved.
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC when GPOA (Bank 2 register 0x62 – 0x6A) is low.
	VSGP	4	VSYNC use GPO9. 0: Disable. 1: Enable (using Bank 2 register 0x59 – 0x61 to define

Digital Image Processor Register (Bank=00)				
			OVSYNC).	
	EHTT	3	Even H Total. 0: Enable, Output H Total always be even pixels. 1: Disable, Output H Total always be odd pixels.	
	-	2	Reserved.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	0: Disable. 1: Enable.	
28h	OSCTRL2	7:0	Default : 0x00	Access : R/W
	-	7:0	Reserved.	
29h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
2Ah	BRC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	BRC	0	Brightness function, reference to register 2Bh, 2Ch, and 2Eh. 0: Off. 1: On.	
2Bh	BCR	7:0	Default : 0x80	Access : R/W
	BCR[7:0]	7:0	Brightness Coefficient – Red color. 00h: -128. 80h: 0, default value. FFh: +127.	
2Ch	BCG	7:0	Default : 0x80	Access : R/W
	BCG[7:0]	7:0	Brightness Coefficient – Green color. 00h: -128. 80h: 0, default value. FFh: +127.	
2Dh	BCB	7:0	Default : 0x80	Access : R/W
	BCB[7:0]	7:0	Brightness Coefficient – Blue color. 00h: -128. 80h: 0, default value. FFh: +127.	
2Eh	CNTR	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CNREN[6:5]	6:5	Contrast Noise Rounding Enable. 11: Enable.	

Digital Image Processor Register (Bank=00)			
	CCLR	4	Contrast Coefficient LSB – Red color.
	CCLG	3	Contrast Coefficient LSB – Green color.
	CCLB	2	Contrast Coefficient LSB – Blue color.
	CNTT	1	Contrast Type select. 0: Use 0 as center point. 1: Use 128 as center point.
	CNTR	0	Contrast function. 0: Off. 1: On.
2Fh	CCR	7:0	Default : 0x80
	CCR[7:0]	7:0	Access : R/W Contrast Coefficient – Red color. 00h: 0.0000000. 80h: 1.0000000. Default value. FFh: 1.1111111.
30h	CCG	7:0	Default : 0x80
	CCG[7:0]	7:0	Access : R/W Contrast Coefficient – Green color. 00h: 0.0000000. 80h: 1.0000000. Default value. FFh: 1.1111111.
31h	CCB	7:0	Default : 0x80
	CCB[7:0]	7:0	Access : R/W Contrast Coefficient – Blue color. 00h: 0.0000000. 80h: 1.0000000. Default value. FFh: 1.1111111.
32h	FWC	7:0	Default : 0x00
	-	7:1	Access : R/W Reserved.
	FWC	0	Border Color (will be used when output is in free-run mode). 0: Off. 1: On.
33h	FCR	7:0	Default : 0x00
	FCR[7:0]	7:0	Access : R/W Border Color – Red channel.
34h	FCG	7:0	Default : 0x00
	FCG[7:0]	7:0	Access : R/W Border Color – Green channel.
35h	FCB	7:0	Default : 0x00
	FCB[7:0]	7:0	Access : R/W Border Color – Blue channel.
36h	DITHCTRL	7:0	Default : 0x02
	DITHG[1:0]	7:6	Access : R/W Dither coefficient for G channel.
	DITHB[1:0]	5:4	Dither coefficient for B channel.

Digital Image Processor Register (Bank=00)			
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.
	OBN	1	Output Bits Number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).
	DITH	0	Dither function. 0: Off. 1: On.
37h	DITHCOEF	7:0	Default : 0x20      Access : R/W
	TL[1:0]	7:6	Top – Left dither coefficient.
	TR[1:0]	5:4	Top – Right dither coefficient.
	BL[1:0]	3:2	Bottom – Left dither coefficient.
	BR[1:0]	1:0	Bottom – Right dither coefficient.
38h	TRFN	7:0	Default : 0x00      Access : R/W
	PSRD	7	Pseudo Random, resets every 4 frames. 0: Enable. 1: Disable.
	NDMD	6	Noise Dithering Method.
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame.



Digital Image Processor Register (Bank=00)				
			1: Tempo-dither every 2 frames.	
39h	DITHCTRL2	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	GAMMAPR	4	Gamma Protection	
	-	3:1	Reserved.	
	GATECLK	0	Gated clock.	
3Ah	BFRACDIV_L	7:0	Default : 0x00	Access : R/W
	BFRACDIV[7:0]	0	Blanking fraction divider.	
3Bh	BFRACDIV_H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	BFRACDIV[15:8]	7:0	See description for BFRACDIV[7:0].	
3Ch	BFRACV_L	7:0	Default : 0x00	Access : RO
	BFRACV[7:0]	0	Blanking fraction value.	
3Dh	BFRACV_H	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	BFRACV[10:8]	2:0	See description for BFRACV[7:0].	
3Eh ~	-	7:0	Default : -	Access : -
3Fh	-	7:0	Reserved.	
40h	GAMMAC	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DITHMTYPE	5	Dither function Minus Type	
	GNREN	4	Gamma Noise Round Enable.	
	BTCS[1:0]	3:2	Gamma Table Channel Select. 00: Write red channel. 01: Write green channel. 10: Write blue channel. 11: Write red/green/blue channel.	
	GTIO	1	Gamma Table I/O access. 0: Disable. 1: Enable.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
41h	GAMMAP	7:0	Default : 0x00	Access : R/W
	GAMMAP[7:0]	7:0	Gamma data Port.	
42h	OCTRL1	7:0	Default : 0x00	Access : R/W

Digital Image Processor Register (Bank=00)			
	LCPS	7	LVDS Channel Polarity Swap (P/N swap). 0: Disable. 1: Enable.
	LCS	6	LVDS Channel Swap. 0: Disable. 1: Enable. When enabled in dual LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap, LVB0M/LVB3M swap, LVB0P/LVB3P swap, LVB1M/LVBCKM swap, LVB1P/LVBCKP swap. When enabled in single LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap.
	MLXT	5	MSB/LSB Exchange Type. 0: Always reverse bit[7:0]. 1: Reverse bit[7:2] when 6-bit panel.
	LTIM	4	LVDS TI Mode. 0: Normal. 1: TI Mode.
	OMLX	3	Odd channel MSB/LSB Exchange. 0: Normal. 1: Exchange.
	EMLX	2	Even channel MSB/LSB Exchange. 0: Normal. 1: Exchange.
	ORBX	1	Odd channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.
	ERBX	0	Even channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.
43h	OCTRL2	7:0	Default : 0x00      Access : R/W
	TCOP	7	TCON Control Pin port select (only used when )BN=1, 6-bit output). 0: Use output data port. 1: Use video in port.
	DOT	6	Differential Output Type. 0: LVDS/RSDS. 1: Reduced-swing LVDS/increased-swing RSDS.
	WHTS	5	White Screen (screen off).

Digital Image Processor Register (Bank=00)				
			0: Disable. 1: Enable.	
	BLSK	4	Black Screen (screen off). 0: Disable. 1: Enable.	
	REV	3	Reverse luminosity. 0: Off. 1: On.	
	STO	2	Stagger Output (only used when DPO=1). 0: Disable. 1: Enable.	
	DPX	1	A/B Port Swap (only used when DPO=1). 0: Disable. 1: Enable.	
	DPO	0	Dual Pixel Output. 0: Single pixel. 1: Dual pixel.	
44h	OCTRL3	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CKSEL[4:0]	4:0	Enable clock of internal control. Supposed input interface (ADC/DVI) as the left-side.	
	CKSEL[4]	4	Enable clock of down-side GPO.	
	CKSEL[3]	3	Enable clock of up-side channel.	
	CKSEL[2]	2	Enable clock of down-side channel.	
	CKSEL[1]	1	Enable clock of right-side GPO.	
	CKSEL[0]	0	Enable clock and output current of right-side channel. Please use ADC bank register 0x2D bit 7 to control LVDS internal clock. 01h: LVDS output. 1Dh: Dual-Link RSDS output with down-side GPO. 0Fh: Dual-Link RSDS output with right-side GPO. 15h: Single-Link RSDS output with down-side GPO. 07h: Single-Link RSDS output with right-side GPO. 00h: TTL output.	
45h ~	-	7:0	Default : -	Access : -
4Ah	-	7:0	Reserved.	
4Bh	BLENDC	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CKIND[3:0]	6:3	Color Index of Color Key. 0000: Color index 0.	

Digital Image Processor Register (Bank=00)				
			0001: Color index 1. ... .. 1111: Color index 15. When OSD register 0x10[7]=1, OSD is not backward compatible. When OSD register 0x10[7]=0, OSD is backward compatible. When 8-color palette is selected, only CKIND[2:0] are used. When 16-color palette is selected, OSD0xE0 bit[6] is color key bit[3] instead of using CKIND[3].	
	ABM[2:0]	2:0	Alpha Blending Mode. 000: No alpha blending. 001: Background alpha blending. 010: Foreground alpha blending. 011: Color key alpha blending. 100: Not color key alpha blending. 101: Entire OSD alpha blending. 11x: Reserved.	
4Ch	BLENDL	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4:3	Reserved.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
4Dh ~ 4Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
50h	RDCRH-L	7:0	Default : 0x00	Access : R/W
	RDCRH[7:0]	7:0	Horizontal resolution down-conversion ratio (4 bits integer, 19 bits fraction), support to 1/15.9999. (don't support horizontal resolution up-conversion) XXXX.XXXXXXXXXXXXXXXXXXX	

Digital Image Processor Register (Bank=00)																																							
51h	RDCRH-M	7:0	Default : 0x00	Access : R/W																																			
	RDCRH[15:8]	7:0	See description for RDCRH[7:0].																																				
52h	RDCRH-H	7:0	Default : 0x00	Access : R/W																																			
	RDCENH	7	Horizontal Resolution Down-conversion Enable. (don't support horizontal resolution up-conversion) 0: Disable. 1: Enable.																																				
	RDCRH[22:16]	6:0	See description for RDCRH[7:0].																																				
53h	RRCRV-L	7:0	Default : 0x00	Access : R/W																																			
	RRCRV[7:0]	7:0	Vertical Resolution conversion ratio (2 bits integer, 20 bits fraction), support to 1/2.9999. xx.xxxxxxxxxxxxxxxxxxxx																																				
54h	RRCRV-M	7:0	Default : 0x00	Access : R/W																																			
	RRCRV[15:8]	7:0	See description for RRCRV[7:0].																																				
55h	RRCRV-H	7:0	Default : 0x00	Access : R/W																																			
	RCENV	7	Vertical Resolution Conversion Enable. 0: Disable. 1: Enable.																																				
	VFMD	6	Vertical Resolution conversion Factor Mode. 0: N-1/M-1 for vertical resolution conversion factor. 1: N/M for vertical resolution conversion factor.																																				
	RRCRV[21:16]	5:0	See description for RRCRV[7:0].																																				
56h	RDCFH	7:0	Default : 00x0	Access : -																																			
	RDCFH1[3:0]	7:4	Horizontal resolution down-conversion Filter for Edge.																																				
	RDCFH2[3:0]	3:0	Horizontal resolution down-conversion Filter for No Edge.																																				
57h	RCFV	7:0	Default : 0x00	Access : -																																			
	RCFV[7:0]	7:0	<table border="0"> <tr> <td>Vertical</td> <td>resolution</td> <td>conversion</td> <td>Filter.</td> </tr> <tr> <td>57h</td> <td>59h</td> <td>Description</td> <td></td> </tr> <tr> <td>00</td> <td>X</td> <td>BI</td> <td></td> </tr> <tr> <td>11</td> <td>00</td> <td>BI</td> <td></td> </tr> <tr> <td>11</td> <td>22</td> <td>BG (2)</td> <td></td> </tr> <tr> <td>11</td> <td>33</td> <td>BG (1.5)</td> <td></td> </tr> <tr> <td>22</td> <td>33</td> <td>BM (1.5)</td> <td></td> </tr> <tr> <td>33</td> <td>11</td> <td>BS (0.75)</td> <td></td> </tr> <tr> <td>55</td> <td>00</td> <td>CB (0)</td> <td></td> </tr> </table>		Vertical	resolution	conversion	Filter.	57h	59h	Description		00	X	BI		11	00	BI		11	22	BG (2)		11	33	BG (1.5)		22	33	BM (1.5)		33	11	BS (0.75)		55	00	CB (0)
Vertical	resolution	conversion	Filter.																																				
57h	59h	Description																																					
00	X	BI																																					
11	00	BI																																					
11	22	BG (2)																																					
11	33	BG (1.5)																																					
22	33	BM (1.5)																																					
33	11	BS (0.75)																																					
55	00	CB (0)																																					
58h	HDSUSG	7:0	Default : 0x00	Access : -																																			
	HDSUSG[7:0]	7:0	Horizontal DSUS resolution down-conversion Parameter.																																				
59h	HDSUSL	7:0	Default : 0x00	Access : -																																			

Digital Image Processor Register (Bank=00)			
	-	7	Reserved.
	HFMD	6	Horizontal resolution down-conversion Factor Mode. 0: N-1/M-1 for horizontal resolution down-conversion factor. 1: N/M for horizontal resolution down-conversion factor.
	GSR	5	Gray scale Sensitive Register IO. 0: Disable. 1: Enable.
	TSR	4	Text Sensitive Register IO. 0: Disable. 1: Enable.
	TXTJL[3:0]	3:0	Text Judge Level.
5Ah	VDSUSG	7:0	Default: 0x00      Access : -
	M_CSC_EN	7	Main window CSC enable (RGB-> YUV)
	S_CSC_EN	6	MWE window CSC enable (RGB-> YUV)
	VDSUSG[5:0]	5:0	Vertical DSUS resolution conversion Parameter.
5Bh	VDSUSL	7:0	Default: 0x01      Access : -
	MCKS	7	Manual Clock Select. 0: Auto select. 1: Manual select.
	IOCK	6	Input / FIX Clock Select (when MCKS=1). 0: FIXCLK faster, FIXCLK defined by Reg_D1h, bit[7]. 1: IDCLK faster.
	GSE	5	Gray scale Sensitive Function Enable. 0: Disable. 1: Enable.
	TSE	4	Text Sensitive function Enable. 0: Disable. 1: Enable.
	DSUSL[3:0]	3:0	DSUS resolution conversion Parameter Level.
5Ch	PFEN	7:0	Default: 0x00      Access : R/W
	-	7:6	Reserved.
	PFCOEF-H[4]	5	1: Add 2 to coefficient values of PFCOEF-H[3:0] (see below).
	PFCOEF-L[4]	4	1: Add 2 to coefficient values of PFCOEF-L[3:0] (see below).
	MWE_EN	3	MWE function Enable 0: Disable 1: Enable
	-	2:1	Reserved.
	PFEN	0	Post Filter Enable.

Digital Image Processor Register (Bank=00)			
			0: Disable. 1: Enable.
5Dh	PFCOEF	7:0	Default: 0x00
			Access : R/W
	PFCOEF-H[3:0]	7:4	Post Filter H Coefficient for edge part. 0000: Blur – 0.0; 0001: 0.125; 0010: 0.25; 0011: 0.375; 0100: 0.5; 0101: 0.625; 0110: 0.75; 0111: 8.875; 1000: No action – 1.0; 1001: 1.125; 1010: 1.25; 1011: 1.375; 1100: 1.5; 1101: 1.625; 1110: 1.75; 1111: Sharp – 1.875.
	PFCOEF-L[3:0]	3:0	Post Filter L Coefficient for edge part. 0000: Blur – 0.0; 0001: 0.125; 0010: 0.25; 0011: 0.375; 0100: 0.5; 0101: 0.625; 0110: 0.75; 0111: 0.875; 1000: No action – 1.0; 1001: 1.125; 1010: 1.25; 1011: 1.375; 1100: 1.5; 1101: 1.625; 1110: 1.75; 1111: Sharp – 1.875.
5Eh	-	7:0	Default: 0x00
			Access : R/W
	CTHRD[7:4]	7:4	Coring threshold.
	-	3	Reserved.
	STP[2:1]	2:1	Step.

Digital Image Processor Register (Bank=00)			
	VDEN	0	Video Enable.
5Fh ~ 64h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
65h	FTAPEN	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	sRGBNE	5	sRGB Noise round Enable. 0: Disable. 1: Enable.
	sRBGP	4	sRGB Precision. 0: Normal. 1: Shift 2 bits.
	sRGBG	3	sRGB go through Gamma. 0: Bypass gamma. 1: Go to gamma.
	TPP	2	Test Pattern Position. 0: After sRGB. 1: Before sRGB.
	FFSEL[1:0]	1:0	Filter Function Select. 00: Disable. 01: Enable 3 tap function. 1x: Enable sRGB function.
66h	sRGB12	7:0	Default : 0x00 Access : R/W
	sRGB12[7:0]	7:0	Coefficient 12, 1 sign bit, 7 bits.
67h	sRGB13	7:0	Default : 0x00 Access : R/W
	sRGB13[7:0]	7:0	Coefficient 13, 1 sign bit, 7 bits.
68h	sRGB21	7:0	Default : 0x00 Access : R/W
	sRGB21[7:0]	7:0	Coefficient 21, 1 sign bit, 7 bits.
69h	sRGB23	7:0	Default : 0x00 Access : R/W
	sRGB23[7:0]	7:0	Coefficient 23, 1 sign bit, 7 bits.
6Ah	sRGB31	7:0	Default : 0x00 Access : R/W
	sRGB31[7:0]	7:0	Coefficient 31, 1 sign bit, 7 bits.
6Bh	sRGB32	7:0	Default : 0x00 Access : R/W
	sRGB32[7:0]	7:0	Coefficient 32, 1 sign bit, 7 bits.
6Ch ~ 6Eh	-	7:0	Default : - Access : -
	-	7:0	Reserved.
6Fh	INTMDS	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.



Digital Image Processor Register (Bank=00)			
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.
	ODDF	3	Shift Odd Field. 0: Shift even field. 1: Shift odd field.
	SLN[2:0]	2:0	Shift Line Numbers. 000: Shift 0 line between odd and even fields. 001: Shift 1 line between odd and even fields. 010: Shift 2 line between odd and even fields. 011: Shift 3 line between odd and even fields. 1xx: Shift 4 line between odd and even fields.
71h ~	-	7:0	Default : -      Access : R/W
77h	-	7:0	Reserved.
78h	ATGCTRL	7:0	Default : 0x00      Access : R/W
	MAXR	7	Max value flag for red channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	MAXG	6	Max value flag for green channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	MAXB	5	Max value flag for blue channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.
	ACE	4	ADC Calibration Enable. 0: Disable. 1: Enable.
	AGR	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.
	ATGM	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATGE = 0).
	ATGR	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.
	ATGE	0	Auto Gain Function Enable.

Digital Image Processor Register (Bank=00)			
			0: Disable. 1: Enable.
79h	ATGST	7:0	Default : -      Access : RO
	VCLP	7	Video auto gain mode. 0: RGB mode. 1: YPbPr Mode.
	-	6	Reserved.
	CALR	5	Calibration value flag for Red channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE = 1.
	CALG	4	Calibration value flag for Green channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE = 1.
	CALB	3	Calibration value flag for Blue channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE = 1.
	MINR	2	Min value flag for Red channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.
	MING	1	Min value flag for Green channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.
	MINB	0	Min value flag for Blue channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.
7Ah	ATFCHSEL	7:0	Default: 0x00      Access : R/W
	-	7:6	Reserved.
	ATPCHSEL[1:0]	5:4	Auto Phase R/G/B channel select 00: R/G/B 3 channels 01: only R channel 10: only G channel 11: only B channel
	-	3	Reserved.
	ATGCHSEL[2:0]	2:0	Auto Gain R/G/B channel min/max value select.

Digital Image Processor Register (Bank=00)				
			000: R min value 001: G min value 010: B min value 011: R max value 100: G max value 101: B max value 11x: Reserved	
7Bh	ATOCTRL	7:0	Default : 0x00	Access : R/W
	JITLR	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: right result.	
	JITS	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITM	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITR	3	Jitter function Result. 0: No jitter. 1: Jitter present.	
	ATOM	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATOR	1	Auto position result Ready. 0: Result ready. 1: Result not ready.	
	ATOE	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
7Ch	AOVDV	7:0	Default : 0x00	Access : R/W
	AOVDV[3:0]	7:5	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. ... .. 1111: Valid if data >= 1111 0000.	
	-	4:0	Reserved.	

Digital Image Processor Register (Bank=00)				
7Dh	ATGVALUE	7:0	Default: -	Access : RO
	ATGVALUE[7:0]	7:0	Auto Gain result based on 7Ah[2:0].	
7Eh	AOVST-L	7:0	Default : -	Access : RO
	AOVST [7:0]	7:0	Auto position detected result Vertical Starting point.	
7Fh	AOVST-H	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	AOVST[10:8]	2:0	See description for AOVST [7:0].	
80h	AOHST-L	7:0	Default : -	Access : RO
	AOHST[7:0]	7:0	Auto position detected result Horizontal Starting point.	
81h	AOHST-H	7:0	Default : -	Access : R/W DB
	-	7:3	Reserved.	
	SPRGST[10:8]	2:0	Image horizontal sample start point, count by input dot clock.	
82h	AOVEND-L	7:0	Default : -	Access : RO
	AOVEND[7:0]	7:0	Auto position detected result Vertical End point.	
83h	AOVEND-H	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	AOVEND[10:8]	2:0	See description for AOVEND[7:0].	
84h	AOHEND-L	7:0	Default : -	Access : RO
	AOHEND[7:0]	7:0	Auto position detected result Horizontal End point.	
85h	AOHEND-H	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	AOHEND[11:8]	2:0	See description for AOHEND[7:0].	
86h	JLR-L	7:0	Default : -	Access : RO
	JLR[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_7Bh[7].	
87h	JLR-H	7:0	Default : -	Access : RO
	-	7:3	Reserved.	
	JLR[10:8]	2:0	See description for JLR[7:0].	
88h	ANRF	7:0	Default : -	Access : RO
	-	7:6	Reserved.	
	HNEN	5	High level Noise reduction Enable. 0: Disable. 1: Enable.	
	BGEN	4	Background Noise reduction Enable. 0: Disable. 1: Enable.	

Digital Image Processor Register (Bank=00)			
	-	3	Reserved.
	ANLV[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.
89h	ATPGTH	7:0	Default : 0x01      Access : R/W
	ATPGTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATPV3 when ATPN4 = 0.
8Ah	ATPTTH	7:0	Default : 0x10      Access : R/W
	ATPTTH[7:0]	7:0	Auto Phase Text Threshold for ATPV4.
8Bh	ATPCTRL	7:0	Default : 0x00      Access : R/W
	-	7	Reserved.
	GRY	6	Gray scale detect (read only).
	TXT	5	Text detect (read only).
	APMASK[2:0]	4:2	Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.
	ATPR	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.
	ATPE	0	Auto Phase function Enable. 0: Disable. 1: Enable.
8Ch	ATPV1	7:0	Default : -      Access : RO
	ATPVALUE[7:0]	7:0	Auto Phase Value.
8Dh	ATPV2	7:0	Default : -      Access : RO
	ATPVALUE[15:8]	7:0	See description for ATPVALUE[7:0].
8Eh	ATPV3	7:0	Default : -      Access : RO
	ATPVALUE[23:16]	7:0	See description for ATPVALUE[7:0].
8Fh	ATPV4	7:0	Default : -      Access : RO
	ATPVALUE[31:24]	7:0	See description for ATPVALUE[7:0].
90h	ASCTRL	7:0	Default : 0x90      Access : R/W
	IVB	7	Input VSYNC Blanking Status. 0: In display. 1: In blanking.

Digital Image Processor Register (Bank=00)			
	-	6	Reserved.
	DLINE[1:0]	5:4	Delay Line.
	-	3:2	Reserved.
	UNDER	1	Under run status.
	OVER	0	Over run status.
91h	LPVP-L	7:0	Default : - Access : RO
	LPVP[7:0]	7:0	Locking Point Vertical Position.
92h	LPVP-H	7:0	Default : - Access : RO
	-	7:3	Reserved.
	LPVP[10:8]	2:0	See description for LPVP[7:0].
93h	IFRACW-L	7:0	Default : - Access : RO
	IFRACW[7:0]	7:0	Insert Fraction Width.
94h	IFRACW-H	7:0	Default : - Access : R/W
	-	7	Reserved.
	-	6	Reserved.
	FIELD	5	Field select..
	SFRACU	4	Stop Fraction Update.
	-	3	Reserved.
	IFRACW[10:8]	2:0	See description for IFRACW[7:0]. (read only)
95h	LVSST-L	7:0	Default : - Access : RO
	LVSSTAT[7:0]	7:0	Locking Vertical Total line number.
96h	LVSST-H	7:0	Default : - Access : RO
	-	7	Reserved.
	-	6:3	Reserved.
	LVSSTAT[10:8]	2:0	See description for LVSSTAT[7:0].
97h	LHTST-L	7:0	Default : - Access : RO
	LHTSTAT[7:0]	7:0	Locking HTotal Status.
98h	LHTST-H	7:0	Default : - Access : RO
	-	7:3	Reserved.
	LHTSTAT[10:8]	2:0	See description for LHTSTAT[7:0].
99h	LFRST-L	7:0	Default : 0x00 Access : R/W
	LFTSTAT[7:0]	7:0	Locking Fraction Status.
9Ah	LFRST-H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	LFTSTAT[10:8]	2:0	See description for LFTSTAT[7:0].

Digital Image Processor Register (Bank=00)				
9Bh	LMARGIN	7:0	Default : 0x00	Access : R/W
	LHTTMGN[7:0]	7:0	Locking H Total Margin.	
9Ch	LRSV-L	7:0	Default : 0x00	Access : R/W
	LRSVALUE[7:0]	7:0	Locking Read Start Value.	
9Dh	LRSV-H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	LRSVALUE[10:8]	2:0	See description for LRSVALUE[7:0].	
9Eh	LMARGIN	7:0	Default : 0x00	Access : R/W
	LSSCMGN[7:0]	7:0	Locking SSC Margin.	
9Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
A0h	OSDIOA	7:0	Default : 0x10	Access : R/W
	OSBM	7	OSD SRAM I/O Access Burst Mode. 0: Disable. 1: Enable.	
	CLR	6	OSD Clear Bit (write only). 0: Normal. 1: Clear code with 00h, attribute with 00h.	
	CP	5	OSD 256 Color Palette I/O access. 0: Disable. 1: Enable.	
	RF	4	OSD RAM Font I/O access. 0: Disable. 1: Enable.	
	DC	3	OSD Display Code I/O access. 0: Disable. 1: Enable.	
	DA	2	OSD Display Attribute I/O access. 0: Disable. 1: Enable.	
	ORBW	1	OSD Register Burst Write mode. 0: Disable. 1: Enable.	
	-	0	Reserved.	
	A1h	OSDRA	7:0	Default : 0x00
-		7	Reserved.	
OSDRA[6:0]		6:0	OSD Register Address port.	
A2h	OSDRD	7:0	Default : 0x00	Access : R/W

**Digital Image Processor Register (Bank=00)**

	OSDRD[7:0]	7:0	OSD Register Data port.	
A3h	RAMFA	7:0	Default:	Access : R/W
	RAMFA[7:0]	7:0	OSD RAM Font Address port.	
A4h	RAMFD	7:0	Default : 0x00	Access : R/W
	RAMFD[7:0]	7:0	OSD RAM Font Data port.	
A5h	DISPCA-L	7:0	Default : 0x00	Access : R/W
	DISPCA[7:0]	7:0	OSD Display Code Address code.	
A6h	DISPCA-H	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	DISPCA[9:8]	1:0	See description for DISPCA[7:0].	
A7h	DISPCD	7:0	Default : 0x00	Access : R/W
	DISPCD[7:0]	7:0	OSD Display Code Data port.	
A8h	DISPAA-L	7:0	Default : 0x00	Access : R/W
	DISPAA[7:0]	7:0	OSD Display Attribute Address port.	
A9h	DISPAA-H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DISPAA[10:8]	2:0	See description for DISPAA[7:0].	
AAh	DISPAD	7:0	Default : 0x00	Access : R/W
	DISPAD	7:0	OSD Display Attribute Data Port.	
ABh	Bank 0 register 0xD0[0] = 0			
	FSM	7:0	Default : 0x00	Access : R/W
	FSMEN	7	Frame rate control Enable. 0: Disable. 1: Enable.	
	FSMRATIO[3:0]	6:3	Output frame rate / input frame rate. Bit[3]: 1/2; Bit[2]: 1/4; Bit[1]: 1/8; Bit[0]: 1/16.	
	-	2:0	Reserved.	
	Bank 0 register 0xD0[0] = 1			
	TSTDATA	7:0	Default : 0x00	Access : R/W
	TSTDATA[7:0]	7:0	LVDS/RSFS Test mode Data. When LVDS output, use TSTDATA[7:1]. When RSFS output, use TSTDATA[7:0].	
ACh	256CPA	7:0	Default : -	Access : WO



Digital Image Processor Register (Bank=00)			
	256CPA[7:0]	7:0	OSD 256 Color Palette Address port.
ADh	256CPD	7:0	Default : - Access : WO
	256CPD[7:0]	7:0	OSD 256 Color Palette Data port.
AEh	OSDDF	7:0	Default : 0x00 Access : R/W
	RAMFA[8]	7	See description for RAMFA[7:0].
	-	6:4	Reserved.
	DISPCD[8]	3	See description for DISPCD[7:0].
	-	2:0	Reserved.
AFh		7:0	Default : Access : WO
	DDC2BI_EN	7	0: Disable. 1: Enable.
	DDC2BI_ID	6:0	DDC2BI ID.
B0h	WDTEN	7:0	Default : 0x01 Access : R/W
	-	7:2	Reserved.
	WDTC	1	Watchdog Timer Clear (protected by WDTKEY). 0: Normal. 1: Clear.
	WDTE	0	Watchdog Timer Enable (protected by WDTDEY). 0: Disable. 1: Enable.
B1h	WDTKEY	7:0	Default : 0x00 Access : R/W
	WDTKEY	7:0	Watchdog Timer Enable Key. To disable/clear watchdog timer, you must first write the WDTKEY with 55h, AAh to unlock.
B2h	WDTCNT	7:0	Default : 0x03 Access : R/W
	WDTCNT	7:0	Watchdog Timer Counter. The clock of Watchdog timer is frequency of XTAL/(256*1024).
B3h	DDCEN	7:0	Default : 0x1E Access : R/W
	GPOU[1:0]	7:6	GPO Usage. 00: GPO. 01: MPU bypass. 10: DDC bypass. 11: ISP bypass (use I2C protocol).
	DMEN	5	DDC Master function Enable. 0: Disable. 1: Enable.
	CSOK	4	DDC Check sum (read only). 0: Check sum not okay.

Digital Image Processor Register (Bank=00)			
			1: Check sum okay.
	DMST	3	DDC Master function Status (read only). 0: Busy. 1: Not busy.
	DMF	2	DDC Master Finish. Already access 128 or 256 byte data (read only). 0: Not finish. 1: Finish.
	GPO[1:0]	1:0	GPO.
B4h	DDCEN	7:0	Default : 0x8A      Access : R/W
	D_EN1	7	DDC function Enable. 0: Disable. 1: Enable.
	DFLT	6	DDC Filter. 0: Enable. 1: Disable.
	DIWP	5	DDC I2C bus Write Protect. 0: Enable. 1: Disable.
	ISPT	4	ISP using RS-232 type. 0: Disable. 1: Enable.
	CSOK1	3	DDC Check Sum for input 1 (read only). 0: Check sum not okay. 1: Check sum okay.
	D_BSY1	2	DDC Busy (read only). 0: Not busy. 1: Busy.
	D_RW1	1	DDC last Read/Write status (read only). 0: Write. 1: Read.
	D_DTY1	0	DDC SRAM Dirty status (read/clear). 0: Not dirty. 1: Dirty.
B5h	DDC_LAST	7:0	Default : -      Access : RO
	DDCTS	7	DDC Type Select. 0: DDC. 1: DDC2BI.
	DDC_LAST1[6:0]	6:0	DDC Last R/W address.

Digital Image Processor Register (Bank=00)				
B6h	DDCADDR	7:0	Default : 0x8A	Access : R/W
	S_RW1	7	DDC SRAM Read/Write. 0: Write. 1: Read.	
	DDC_ADDRP1[6:0]	6:0	DDC Address Port.	
B7h	DDCDATA	7:0	Default : 0x00	Access : R/W
	DDCDATAP1[7:0]	7:0	DDC Data Port.	
B8h	DDCEN	7:0	Default : 0x82	Access : R/W
	D_EN2	7	See description for D_EN1. 1: Enable.	
	D_1A_INT	6	Enable 1 <sup>st</sup> DDC2BI Interrupt.	
	D_1D_INT	5	Enable 2 <sup>nd</sup> DDC2BI Interrupt.	
	1A_STA	4	1 <sup>st</sup> Status.	
	1D_STA	3	2 <sup>nd</sup> Status.	
	D_BSY2	2	See description for D_BSY1.	
	D_RW2	1	See description for D_RW1.	
D_DTY2	0	See description for D_DTY1.		
B9h	DDC_LAST	7:0	Default : -	Access : RO
	DDCTS	7	DDC Type Select. 0: DDC. 1: DDC2BI.	
	DDC_LAST2[6:0]	6:0	See description for DDC_LAST1[6:0].	
BAh	DDCADDR	7:0	Default : 0x86	Access : R/W
	S_RW2	7	See description for S_RW1.	
	DDC_ADDRP2[6:0]	6:0	See description for DDC_ADDRP1[6:0].	
BBh	DDCDATA	7:0	Default : 0x00	Access : R/W
	DDCDATAP2[7:0]	7:0	See description for DDCDATAP1[7:0].	
BCh	MISCFC	7:0	Default : 0x00	Access : R/W
	AFT	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	
	IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	VSGR	5	VSYNC glitch removal with line less than 2 (DE only). 0: Disable. 1: Enable.	

Digital Image Processor Register (Bank=00)			
	VSP	4	VSYNC Protect with V total (DE only). 0: Disable. 1: Enable.
	LBGC	3	LB Clock no gating mode. 0: Disable. 1: Enable.
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.
	-	1:0	Reserved.
BDh	HDCPCTRL	7:0	Default : 0x00 Access : R/W
	OVER2PIN	7:6	0: Not toggling (default). 1: Toggling.
	-	5:4	Reserved.
	-	3	Reserved.
	-	2	Reserved.
	HDCPADR[9:8]	1:0	HDCP address port (default=0), bit 9 is reserved.
BEh	HDCPADR	7:0	Default : 0x16 Access : R/W
	HDCPADR[7:0]	7:0	HDCP address port (default=0), bit 9 is reserved.
BFh	HDCPDAT	7:0	Default : 0x00 Access : R/W
	HDCPDAT[7:0]	7:0	HDCP Data port.
COh	DPMSTATUS	7:0	Default : 0x08 Access : R/W
	VS	7	VSYNC toggling Status. 0: Not toggling. 1: Toggling.
	HS	6	HSYNC toggling Status. 0: Not toggling. 1: Toggling.
	SCDT	5	SCDT Status. 0: No SCDT. 1: SCDT valid.
	DEV	4	DE with Valid blanking. 0: Not valid. 1: Valid.
	AutoOn	3	Hardware power on upon detecting valid DVI input. 0: Disable. 1: Enable.
	Auto	2	Hardware Auto detection on DVI input.

Digital Image Processor Register (Bank=00)			
			0: Disable. 1: Enable.
	Manual	1	Manual detection on DVI input. 0: Off. 1: On.
	ManualGo	0	Manual detection trigger, auto clear to 0 if finish. 0: Off. 1: On.
Note: This register is only valid when F0h[1:0] = 2'b10.			
C1h	DPMCTL	7:0	Default : 0x00 Access : R/W
	DPMPrd	7:6	Hardware auto detection cycle time. 00: Default. 01: Short. 10: Shortest.
	DMPPulse	5:3	Hardware auto Detection Pulse Width Manual detection pm DVI input. 000: Shortest. ... 111: Longest.
	DEMon	2	DVI DE Monitor enable. 0: Disable. 1: Enable.
	HVMon	1	DVI HSYNC and VSYNC Monitor enable. 0: Disable. 1: Enable.
	HMon	0	DVI HSYNC Monitor enable. 0: Disable. 1: Enable.
Note: This register is only valid when F0h[1:0] = 2'b10.			
C2h	PWMCLK	7:0	Default : 0x00 Access : R/W
	DB_EN	7	Double Buffer Enable. 0: Disable. 1: Enable.
	P1REN	6	PWM1 Reset every frame Enable. 0: Disable. 1: Enable.
	POREN	5	PWM1 Reset every frame Enable. 0: Disable. 1: Enable.

Digital Image Processor Register (Bank=00)			
	P1POL	4	PWM 1 Polarity when enhance PWM1 enable.
	EP1EN	3	Enhance PWM1 Enable. 0: Disable. 1: Enable.
	POPOL	2	PWM0 Polarity when enhance PWM0 enable.
	EPOEN	1	Enhance PWM0 Enable. 0: Disable. 1: Enable.
	PCLK	0	PWM base Clock select. 0: 14.318MHz. 1: 14.318MHz / 4.
C3h	PWMOC	7:0	Default : 0x00      Access : R/W
	PWMOC[7:0]	7:0	PWM0 Coarse adjustment.
C4h	PWM1C	7:0	Default : 0x00      Access : R/W
	PWM1C[7:0]	7:0	PWM1 Coarse adjustment.
C5h	PWM0EP	7:0	Default : 0x00      Access : R/W
	EPWM0P[7:0]	7:0	Enhance PWM0 Period.
C6h	PWM0EP	7:0	Default : 0x00      Access : R/W
	EPWM0P[7:0]	7:0	Enhance PWM0 Period.
C7h	PWM1EP	7:0	Default : 0x00      Access : R/W
	EPWM1P[7:0]	7:0	Enhance PWM1 Period.
C8h	PWM1EP	7:0	Default : 0x00      Access : R/W
	EPWM1P[7:0]	7:0	Enhance PWM1 Period.
C9h	-	7:0	Default : 0x00      Access : -
	-	7:0	Reserved.
CAh	INTCTROL	7:0	Default : 0x00      Access : R/W
	HCHGM	7	HSYNC Changing detect Method. 0: Interrupt only occurred at start and end of transition. 1: interrupt occurred at every line.
	DCMD	6	DVI Clock Missing Detected (read only; DVI feature only, independent of bank 0 register 0x02h, ISEL[1:0]). 0: DVI clock is OK, $Freq(dvi) > Freq(xtal) * EBh / 128$ . 1: DVI clock is missing, $Freq(dvi) < Freq(xtal) * EBh / 128$ . Where EBh default to 0x1E(30).
	HSPM	5	ADC Mode: HSYNC Pin Monitor (read only); DVI mode: SCDT value. When input is analog: 0: HSYNC pin is low.

Digital Image Processor Register (Bank=00)				
			1: HSYNC pin is high. When input is DVI: 0: SCDT is missing. 1: SCDT is OK.	
	HSST	4	HS Status (read only). 0: Stable. 1: Not stable.	
	IVSI	3	Input VSYNC Interrupt generated by: 0: Leading edge. 1: Tailing edge.	
	OVSI	2	Output VSYNC interrupt generated by: 0: Leading edge. 1: Tailing edge.	
	TRGC	1	Trigger Condition. 0: Active low for level trigger / tailing edge trigger. 1: Active high for level trigger / leading edge trigger.	
	INTT	0	Interrupt Trigger. 0: Generate an edge trigger interrupt. 1: Generate a level trigger interrupt.	
CBh	INTPULSE	7:0	Default : 0x0F	Access : R/W
	INTPULSE[7:0]	7:0	Interrupt Pulse Width by reference clock.	
CCh	INTSTA	7:0	Default : 0x00	Access : R/W
	INTSTA[7:0]	7:0	Interrupt Status byte A. Bit 7: Input VSYNC changed (co-work with register E7h). Bit 6: Input HSYNC changed (co-work with register E6h). Bit 5: Input VSYNC disappear. Bit 4: Input HSYNC disappear. Bit 3: Input VSYNC edge. Bit 2: Input HSYNC edge. Bit 1: ADC0 HSYNC0 pin toggling (independent with Reg_02h, ISEL[1:0]). Bit 0: Composite sync / SOG status change.	
CDh	INTSTB	7:0	Default : 0x06	Access : R/C
	INTSTB[7:0]	7:0	Interrupt Status control byte B. Bit 7: Auto phase ready. Bit 6: Auto position ready. Bit 5: Auto gain ready. Bit 4: Jitter detected. Bit 3: ADC1 HSYNC1 pin toggling. Bit 2: DVI clock status change; no clock <-> with clock.	

Digital Image Processor Register (Bank=00)			
			Bit 1: Watchdog timer. Bit 0: Under-run / Over-run occurred.
CEh	INTENA	7:0	Default : 0x00      Access : R/C
	INTENA[7:0]	7:0	Interrupt Enable control byte A. 0: Disable interrupt. 1: Enable interrupt.
CFh	INTENB	7:0	Default : 0x00      Access : R/W
	INTENB[7:0]	7:0	Interrupt Enable control byte A. 0: Disable interrupt. 1: Enable interrupt.
D0h	PLLCTRL1	7:0	Default : 0x00      Access : R/W
	XOUT	7	Enable PWM1 as XTAL clock output. 0: Disable. 1: Enable.
	EOCK	6	Use External Clock (pin #) as Output Dot Clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock).
	XDIV	5:4	XTAL clock Divided by: 00: 16; 01: 08; 10: 04; 11: 01.
	BPM	3	Bypass clock Mode (IDCLK as ODCLK). 0: Disable. 1: Enable.
	TSTM	2	Test Mode. 0: Disable. 1: Enable.
	PTEN	1	PLL Test register protect bit. 0: Disable. 1: Enable.
	LRTM	0	LVDS/RSDS Test Mode enable. 0: Disable. 1: Enable.
D1h	PLLCTRL2	7:0	Default : 0x00      Access : R/W
	MPPDIV	7	Master PLL Post Divider. 0: div 3 (143 MHz). 1: div 2.5 (172 MHz), for output dot clock higher than 143 MHz (vertical = 85 MHz).



Digital Image Processor Register (Bank=00)			
	LP_POR	6	Output PLL Power On Reset.
	LP_RST	5	Output PLL Reset.
	LP_PD	4	Output PLL Power Down.
	MP_K	3	Master PLL output frequency divided by 2.
	MP_PORT	2	Master PLL Power On Reset.
	MP_RST	1	Master PLL Reset.
	MP_PD	0	Master PLL Power Down.
D2h	MPLL_M	7:0	Default : 0x6F Access : R/W
	MP_ICTRL[2:0]	7:5	Master PLL Current Control.
	MPLL_M[4:0]	4:0	Master PLL divider.
D3h	LPLL_M	7:0	Default : 0x02 Access : R/W
	-	7:6	Reserved.
	SDMD	5	Output PLL spread spectrum Mode. 0: Normal. 1: Reverse for mode 1.
	LPLL_M[4:0]	4:0	Output PLL divider 1.
D4h	LPLL_CTL2	7:0	Default : 0x0B Access : R/W
	-	7:6	Reserved.
	LP_TP	5	Output PLL Type. 0: LVDS. 1: RSDS/TTL.
	LP_K[1:0]	4:3	Output PLL divider 2. 00: 8; 01: 4; 10: 2; 11: 1.
	LP_ICTROL[2:0]	2:0	Output PLL Current Control.
D5h	LPLL_SET	7:0	Default : 0x44 Access : R/W, DB
	LP_SET[7:0]	7:0	Output PLL Set.
D6h	LPLL_SET	7:0	Default : 0x55 Access : R/W, DB
	LP_SET[15:8]	7:0	See description for LP_SET[7:0].
D7h	LPLL_SET	7:0	Default : 0x24 Access : R/W, DB
	LP_SET[23:16]	7:0	See description for LP_SET[7:0].
D8h	LPLL_STEP	7:0	Default : 0x20 Access : R/W, DB
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum Step.
D9h	LPLL_STEP	7:0	Default : 0x00 Access : R/W, DB

Digital Image Processor Register (Bank=00)			
	-	7:3	Reserved.
	LPLL_STEP[10:8]	2:0	See description for LPLL_STEP[7:0].
DAh	LPLL_SPAN	7:0	Default : 0x00      Access : R/W, DB
	LP_SPAN[7:0]	7:0	Output PLL spread spectrum Span.
DBh	LPLL_SPAN	7:0	Default : 0x00      Access : R/W, DB
	-	7:3	Reserved.
	LP_SPAN[10:8]	2:0	See description for LP_SPAN[7:0].
DCh	MPLL_TST	7:0	Default : 0x00      Access : R/W
	MP_TEST[7:0]	7:0	
DDh	LPLL_TSTA	7:0	Default : 0x00      Access : R/W
	LP_TESTA[7:0]	7:0	
DEh	LPLL_TSTD	7:0	Default : 0x00      Access : R/W
	LP_LSTA	7	LPLL Lock Status.
	LP_TESTD[7:0]	6:0	
DFh	-	7:0	Default :      Access : -
	-	7:0	Reserved.
E0h	STATUS1	7:0	Default : -      Access : RO
	-	7:4	Reserved.
	IHSM	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly.
	IVSM	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly.
	OHSM	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly.
	OVSM	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly.
E1h	STATUS2	7:0	Default : -      Access : RO
	VSACT	7	Input VSYNC Active. 0: Not detected. 1: Detected.
	HSACT	6	Input HSYNC Active. 0: Not detected. 1: Detected.
	CSD	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.
	SOGD	4	Sync-On-Green Detected status.

Digital Image Processor Register (Bank=00)			
			0: Input is not SOG. 1: Input is detected as SOG.
	INTM	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.
	INTF	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.
	IHSP	1	Incoming input HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
	IVSP	0	Incoming input VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
E2h	VTOTAL-L	7:0	Default : -      Access : RO
	VTOTAL[7:0]	7:0	Input Vertical Total, count by HSYNC.
E3h	VTOTAL-H	7:0	Default : -      Access : RO
	-	7:3	Reserved.
	VTOTAL[10:8]	2:0	See description for VTOTAL[7:0].
E4h	HSPRD-L	7:0	Default : -      Access : RO
	HSPRD[7:0]	7:0	Input Horizontal Period, count by reference clock.
E5h	HSPRD-H	7:0	Default : -      Access : RO
	IHDM	7	Input HSYNC period Detect Mode. 0: One line. 1: 16 lines.
	-	6:5	Reserved.
	HSPRD[12:8]	4:0	See description for HSPRD[7:0].
E6h	HSTOL	7:0	Default : 0x05      Access : R/W
	VS2HS	7	Input VSYNC too close to input HSYNC.
	DEF	6	DE Follow mode (for DE to DE period is not fixed).
	HSTOL[5:0]	5:0	HSYNC Tolerance. 5: Default value.
E7h	VSTOL	7:0	Default : 0x01      Access : R/W
	-	7:6	Reserved.
	ANGF	5	Auto No signal Filter mode.
	ANG	4	Auto No signal.
	VSTOL[3:0]	3:0	VSYNC Tolerance.

Digital Image Processor Register (Bank=00)			
			1: Default value.
E8h	ISOVRD	7:0	Default : 0x00      Access : R/W
	SL	7	Shift Line. 0: Shift line method 0. 1: Shift line method 1 for interlace mode.
	CSHS	6	HSYNC in coast. 0: HSOUT (recommended). 1: Re-shaped HSYNC.
	UVSP	5	User defined input VSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.
	IVSJ	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UVSP).
	UHSP	3	User defined input HSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.
	IHSJ	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UHSP).
	UINT	1	User defined non-interlace/interlace, active when INTJ = 1. 0: Non-interlace. 1: Interlace.
	INTJ	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (UINT).
E9h	MDCTRL	7:0	Default : 0x00      Access : R/W
	RCFCPB	7	Resolution conversion filter Compatible select. 0: Compatible with old filter. 1: Use new filter.
	VERR	6	Video CCIR656 Error correct. 0: Disable. 1: Enable.
	SCSEL[1:0]	5:4	Software Compatibility Select.
	VFIV	3	Video Field Inversion. 0: Normal. 1: Invert.
	VEXF	2	Video External Field. 0: Use result of internal circuit detection.

Digital Image Processor Register (Bank=00)			
			1: Use external field.
	INTF	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.
	IFI	0	Interlace Field Invert. 0: Normal. 1: Invert.
EAh	DVICKD	7:0	Default : -      Access : RO
Note: When bank 0 reg 02h[1:0] = 2'b10 (DVI feature only)			
	OF	7	DVI clock detection overflow (DVI feature only). 0: Not overflow. 1: Overflow.
	DVICKD[6:0]	6:0	DVI clock detection report, based on oscillator clock (DVI feature only). $\text{Freq(DVI)} = \text{Freq(xtal)} * \text{DVICKD}[6:0] * 2/128$ , if OF = 0. $\text{Freq(DVI)} > \text{Freq(xtal)} * 2$ , if OF = 1.
EBh	DVICKTH	7:0	Default : 0x1E      Access : R/W
Note: When bank 0 reg 02h[1:0] = 2'b10 (DVI feature only)			
	DVICKTH[7:0]	7:0	DVI clock detection threshold, see CAh for usage (default 0x1E). CAh[6] = 0: DVI clock is OK, $\text{Freq(DVI)} > \text{Freq(xtal)} * \text{EBh}/128$ . CAh[6] = 1: DVI clock is missing, $\text{Freq(DVI)} < \text{Freq(xtal)} * \text{EBh}/128$ . Where EBh default to 0x1E(30).
ECh	MINVTT	7:0	Default : 0x00      Access : R/W
	VFRM	7	Video in free run mode (read only)
	MINVTT[6:0]	6:0	Min Vtt, when detected $\text{vtt} < \text{min vtt}$ , set video free run.
EDh	COCTRL1	7:0	Default : 0x00      Access : R/W
	-	7:6	Reserved.
	AVIS	5	Analog Video Input Select. 0: PC. 1: Component analog video.
	DLYV	4	Analog Delay Line for component analog Video input. 0: Delay 1 line. 1: Do not delay.
	CSCM	3	Composite SYNC cut mode. 0: Disable. 1: Enable.
	EXVS	2	External VSYNC polarity (only used when COVS is 1).

Digital Image Processor Register (Bank=00)			
			0: Normal. 1: Invert.
	COVS	1	Coast VSYNC Select. 0: Internal VSEP. 1: External VSYNC.
	CTA	0	Coast to ADC. 0: Disable. 1: Enable.
EEh	COCTRL2	7:0	Default : 0x00      Access : R/W
	COST[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. ... 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.
EFh	COCTRL3	7:0	Default : 0x00      Access : R/W
	COEND[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. ... 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.
FOh	PDMD	7:0	Default : 0x13      Access : R/W
	APDLD	7	Automatically Power Down when Low power using Digital pin. 0: Disable. 1: Enable.
	APDLA	6	Automatically Power Down when Low power using Analog pin. 0: Disable. 1: Enable.
	PHSRM	5	PD HDCP SRAM.
	PDDS	4	Power Down DDC SRAM. 0: Normal. 1: Power down while not used.
	GCLK[1:0]	3:2	Gated Clock for SRAM (excluding DDC SRAM). 00: Normal. 01: V Blank. 10: H Blank and V Blank. 11: Reserved.
	PDMD	0	Power Down Mode. 00: Normal.

Digital Image Processor Register (Bank=00)			
			01: Output (OSD) only (used when no input signal). 10: BIU, mode detection, GOUT are functional. 11: All chip power down.
F1h	SWRST	7:0	Default : 0x00      Access : R/W
	-	7:6	Reserved.
	ADCR	5	ADC Reset. 0: Normal operation. 1: Reset ADC.
	GPR	4	Graphic Port Reset. 0: Normal operation. 1: Reset.
	DPR	3	Display Port Reset. 0: Normal operation. 1: Reset.
	BIUR	2	BIU Reset. 0: Normal operation. 1: Reset BIU.
	OSDR	1	Internal OSD Reset. 0: Normal operation. 1: Reset internal OSD.
	SWR	0	Software Reset (reset GP, DP, BIU, OSD and ADC). 0: Normal operation. 1: Reset.
F2h	OSCTRL	7:0	Default : 0x00      Access : R/W
	OCLKDLY[3:0] /	7:4	OCLKDLY[3:0]: OCLK Delay adjustment (TCON feature only). 0: 16 step to adjust. 1: Typical 0.8ns delay/step.
	RSCK_SKE[3]	7	RSDS clock inverted. 0: Normal clock out. 1: RSDS clock output inverted.
	RSCK_SKE[2:0]	6:4	RSDS clock skew adjust. 000: Max setup time / min hold time to RSDS data output. 001: ... 011: ... 111: Min setup time / max hold time to RSDS data output.
	OCLK	3	Output CLK control. 0: Normal. 1: Invert.
ODE	2	Output DE control. 0: Active high.	

Digital Image Processor Register (Bank=00)			
			1: Active low.
	OVS	1	Output VSYNC control. 0: Active high. 1: Active low.
	OHS	0	Output HSYNC control. 0: Active high. 1: Active low.
F3h	ISCTRL	7:0	Default : 0x10      Access : R/W
	DEGE	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.
	DEGR[2:0]	6:4	DE or HSYNC post Glitch removal Range.
	HSFL	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.
	ISSM	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.
	-	1	Reserved.
	SCKI	0	Input Sample CLK Invert. 0: Normal. 1: Invert.
F4h	TRISTATE	7:0	Default : 0x7F      Access : R/W
	-	7	Reserved.
	TCS	6	HSYNC/VSYNC Control Signal pin tri-state control (TCON feature only). 0: Normal. 1: Tri-state.
	OEDB	5	Output Even Data Bus pin control. 0: Normal. 1: Tri-state.
	OODB	4	Output Odd Data Bus pin control. 0: Normal. 1: Tri-state.
	OVS	3	OVSYNC pin control.



Digital Image Processor Register (Bank=00)			
			0: Normal. 1: Tri-state.
	OHS	2	OHSYNC pin control. 0: Normal. 1: Tri-state.
	ODE	1	ODE pin control. 0: Normal. 1: Tri-state.
	OCLK	0	OCLK pin control. 0: Normal. 1: Tri-state.
F5h	ODRV	7:0	Default : 0x55 Access : R/W
	DEDRV[1:0]	7:6	Output DE Driving current select. 00: 4mA; 01: 6mA; 10: 8mA; 11: 12mA.
	CLKDRV[1:0]	5:4	Output Clock Driving current select. 00: 4mA; 01: 6mA; 10: 8mA; 11: 12mA.
	ODDDR[1:0]	3:2	Output data Odd channel Driving current select. 00: 4mA; 01: 6mA; 10: 8mA; 11: 12mA.
	EVENDRV[1:0]	1:0	Output data Even channel Driving current select. 00: 4mA; 01: 6mA; 10: 8mA; 11: 12mA.
F6h	ECLKDLY	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SKEW[1:0]	5:4	Output data Skew.
	ECLKDLY[3:0] /	3:0	ECLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: typical 0.8ns delay/step.
F7h	-	7:0	Default : - Access : -
	-	7:0	Reserved.

Digital Image Processor Register (Bank=00)				
F8h	TEST	7:0	Default : 0x05	Access : R/W
	-	7	Reserved.	
	-	6	Reserved.	
	-	5:4	Reserved.	
	TESTMD[3:0]	3:0	Test Mode. 0110: VS/HS/DE output while LVDS output Other: Reserved.	
F9h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
FAh	-	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	VDOE	4	Video reference Edge.(for non-standard signal)	
	IPAVG	3	Interlace Period Average	
	ACLKSW	2	Auto clock switch 0: auto clock switch when detected clock great than expect value 1: Disable auto clock switch	
	-	1:0	Reserved.	
FBh ~ FFh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)				
Index	Mnemonic	Bits	Description	
01h	OSDDBC	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DBL[1:0]	2:1	Double Buffer load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.	
	DBE	0	Double Buffer Enable. 0: Disable. 1: Enable.	
02h	OHSTA-L	7:0	Default : 0x00	Access : R/W DB
	OHSTA[7:0]	7:0	OSD window Horizontal Start position.	
03h	OHSTA-H	7:0	Default : 0x00	Access : R/W DB

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	-	7:1	Reserved.
	OHSTA[8]	0	See description for OHSTA[7:0].
04h	OVSTA-L	7:0	Default : 0x00 Access : R/W DB
	OVSTA[7:0]	7:0	OSD window Vertical Start position.
05h	OVSTA-H	7:0	Default : 0x00 Access : R/W DB
	-	7:1	Reserved.
	OVSTA[8]	0	See description for OVSTA[7:0].
06h	OSDW	7:0	Default : 0x00 Access : R/W DB
	-	7:6	Reserved.
	OSDW[5:0]	5:0	OSD window Width = OSDW + 1 (column), maximum 64 columns.
07h	OSDH	7:0	Default : 0x00 Access : R/W DB
	-	7:5	Reserved.
	OSDH[4:0]	4:0	OSD window Vertical Height = OSDH + 1 (row), maximum 32 rows.
08h	OHSPA	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	OHSPA[5:0]	5:0	OSD window Horizontal Space Start position = OHSPA + 1 (row).
09h	OVSPA	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	OVSPA[4:0]	4:0	OSD window Vertical Space Start position = OVSPA + 1 (column).
0Ah	OSPW	7:0	Default : 0x00 Access : R/W
	OSPW[7:0]	7:0	OSD Space Width = 8 * OSPW (pixel).
0Bh	OSPH	7:0	Default : 0x00 Access : R/W
	OSPH[7:0]	7:0	OSD Space Height = 8 * OSPH (pixel).
0Ch	IOSDC1	7:0	Default : 0x00 Access : R/W, DB
	OV[1:0]	7:6	OSD Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged by x4 by repeated pixels.
	OHS[1:0]	5:4	OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged by x4 by repeated pixels.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	C1C	3	Character 1 line Color. 0: Disable. 1: Enable.
	ROT[1:0]	2:1	Rotate. 00: Not rotate. 01: Rotate 90°. 10: Rotate 270°. 11: Reserved.
	MWIN	0	OSD Main Window display. 0: Main window off. 1: Main window on.
0Dh	IOSDC2	7:0	Default : 0x00      Access : R/W
	CF8E	7	8 Color Font Enable. 0: Disable. 1: Enable.
	BCLR[2:0]	6:4	OSD Border Color index; BCLR[3] is located at REG 0E[5]. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index 15.
	BDC	3	OSD Character Border Type Select. 0: All direction font boundary (border). 1: Bottom-right direction font boundary (shadow).
	BDW	2	OSD Character Border Width control. 0: One pixel width for all scale. 1: Scale with OVS[1:0] and OHS[1:0].
	C16_PAL	1	Color Palette Select. 0: 8 color palette. 1: 16 color palette.
	CF4E	0	4 Color Font Enable. 0: Disable. 1: Enable.
	0Eh	IOSDC3	7:0
C4TE		7	OSD 4-color Transparency Enable. 0: Disable. 1: Enable.
CKIND[3]		6	Color Index Bit 3 of Color Key. Note: When OSD register 0x10[7]=0, OSD is backward compatible. Reserved. Note: When OSD register 0x10[7]=1, OSD is not backward compatible.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	BCLR[3]	5	Border Color Bit 3. This bit should work with OSD 0Dh[6:4].
	SDC	4	OSD window Shadow Control. 0: Off. 1: On.
	SCLR[3:0]	3:0	OSD window Shadow Color index. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index 15.
0Fh	OSHC	7:0	Default : 0x00      Access : R/W
	OSDSH[3:0]	7:4	OSD Shadow Height.
	OSDSW[3:0]	3:0	OSD Shadow Width.
10h	OCFF	7:0	Default : 0x00      Access : R/W
	OCFF	7	OSD backward compatibility. 0: Backward compatible. 1: Not backward compatible.
	MFCS	6	OSD 256 color palette Mono Font Color Select. 0: Use 256 color palette select method. 1: Use 16 color palette select method.
	-	5	Reserved.
	-	4	Reserved.
	CFCTOSD	3	Color Font Code Address Type. 0: RAM base. 1: Code base.
	C256P_SEL	2	OSD 256 Palette Select. 0: Select 8 or 16 color palette. 1: Select 256 color palette.
	PAL_EXT	1	OSD 16/256 Palette Extended method. 0: Extended LSB. 1: Extended 0.
	-	0	Reserved.
11h	OSDCFA	7:0	Default : 0x00      Access : R/W
	OSDCFA[7:0]	7:0	OSD 4 Color RAM Font Starting Address.
12h	OCBUFO	7:0	Default : 0x00      Access : R/W
	COS	7	OSD Code buffer Offset Select. 0: Use OSDW[5:0] as offset. 1: Use OOFFSET[5:0] as offset.
	-	6	Reserved.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	OOFFSET	5:0	OSD code buffer Offset value.
13h	OSDBA-L	7:0	Default : 0x00      Access : R/W, DB
	OSDBA[7:0]	7:0	OSD code Base Address.
14h	OSDBA-H	7:0	Default : 0x00      Access : R/W, DB
	-	7:2	Reserved.
	OSDBA[9:8]	1:0	See description for OSDBA[7:0].
15h	GCCTRL	7:0	Default : 0x00      Access : R/W
	GVS[1:0]	7:6	Gradually color Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.
	GHS[1:0]	5:4	Gradually color Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.
	-	6	Reserved.
	OOFFSET	5:0	OSD code buffer Offset value.
16h	GRADCLR	7:0	Default : 0x00      Access : R/W
	NCLREN	7	New ini Color Enable. 0: Original function. 1: Frame color at bank 0 reg 0x33, 0x34 and 0x35.
	F/B	6	Gradually applied color. 0: Background color. 1: Foreground color.
	RCLR[1:0]	5:4	Red starting gradually Color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is AAh. 11: Red color is FFh.
	GCLR[1:0]	5:4	Green starting gradually Color. 00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh. 11: Green color is FFh.
	BCLR[1:0]	5:4	Blue starting gradually Color. 00: Blue color is 00h. 01: Blue color is 55h.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)				
			10: Blue color is AAh. 11: Blue color is FFh.	
17h	HGRADCR	7:0	Default : 0x00	Access : R/W
	SR	7	Sign bit of Red color. 0: Increase. 1: Decrease.	
	IRH	6	Inverse bit of Red color. 0: Normal. 1: Invert.	
	R_GRADH[5:0]	5:0	Increase/Decrease value of Red color.	
18h	HGRADCG	7:0	Default : 0x00	Access : R/W
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.	
	IGH	6	Inverse bit of Green color. 0: Normal. 1: Invert.	
	G_GRADH[5:0]	5:0	Increase/Decrease value of Green color.	
19h	HGRADCB	7:0	Default : 0x00	Access : R/W
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.	
	IBH	6	Inverse bit of Blue color. 0: Normal. 1: Invert.	
	B_GRADH[5:0]	5:0	Increase/Decrease value of Blue color.	
1Ah	HGRADSR	7:0	Default : 0x00	Access : R/W
	HGRADSR[7:0]	7:0	Horizontal Gradually Step of Red color.	
1Bh	HGRADSG	7:0	Default : 0x00	Access : R/W
	HGRADSG[7:0]	7:0	Horizontal Gradually Step of Green color.	
1Ch	HGRADSB	7:0	Default : 0x00	Access : R/W
	HGRADSB[7:0]	7:0	Horizontal Gradually Step of Blue color.	
	For example, of RCLR=0, R_GRADH=16h, and HGRADSR=20h, then Pixel 0 ~ 19 = 0; Pixel 20 ~ 39 = 16; Pixel 40 ~ 59 = 32; ... etc.			
1Dh	VGRADCR	7:0	Default : 0x00	Access : R/W
	SR	7	Sign bit of Red color.	

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
			0: Increase. 1: Decrease.
	IRV	6	Inverse bit of Red color. 0: Normal. 1: Invert.
	R_GRADV[5:0]	5:0	Increase/Decrease value of Red color.
1Eh	VGRADCG	7:0	Default : 0x00 Access : R/W
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.
	IGV	6	Inverse bit of Green color. 0: Normal. 1: Invert.
	G_GRADV[5:0]	5:0	Increase/Decrease value of Green color.
1Fh	VGRADCB	7:0	Default : 0x00 Access : R/W
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.
	IBV	6	Inverse bit of Blue color. 0: Normal. 1: Invert.
	B_GRADV[5:0]	5:0	Increase/Decrease value of Blue color.
20h	VGRADSR	7:0	Default : 0x00 Access : R/W
	VGRADSR[7:0]	7:0	Vertical Gradually Step of Red color.
21h	VGRADSG	7:0	Default : 0x00 Access : R/W
	VGRADSG[7:0]	7:0	Vertical Gradually Step of Green color.
22h	VGRADSB	7:0	Default : 0x00 Access : R/W
	VGRADSB[7:0]	7:0	Vertical Gradually Step of Blue color.
23h	SUBWOC	7:0	Default : 0x00 Access : R/W, DB
	-	7:4	Reserved.
	BTN0	3	Enable Button function for sub window 0. 0: Off. 1: On.
	BD0	2	Enable OSD sub window 0 Border. 0: Disable. 1: Enable.
	SOC	1	Sub window 0 Color select. If button function is disabled:



OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
			0: From sub window 0 attribute. 1: From attribute RAM. If button function is enable: 0: Set this bit with 0. Use sub window 0 attribute to select FG/BG color and use attribute RAM to select button type.
	SOE	0	Enable OSD sub window 0. 0: Disable. 1: Enable.
24h	SWOHST	7:0	Default : 0x00
	-	7:6	Reserved.
	SWOHST[5:0]	5:0	Sub Window 0 Horizontal Start Position.
25h	SWOHEND	7:0	Default : 0x00
	-	7:6	Reserved.
	SWOHEND[5:0]	5:0	Sub Window 0 Horizontal End Position.
26h	SWOVST	7:0	Default : 0x00
	-	7:5	Reserved.
	SWOVST[4:0]	4:0	Sub Window 0 Vertical Start Position.
27h	SWOVEND	7:0	Default : 0x00
	-	7:5	Reserved.
	SWOVEND[4:0]	4:0	Sub Window 0 Vertical End Position.
28h	SUBWOA2	7:0	Default : 0x00
	Note: When button function is enabled, the FG/BG color is defined by window attribute, character attribute is used to define button function border type and SOC (sub window color select) is disabled.		
	BLNK	7	OSD sub window 0 Blink control. 0: Disable. 1: Enable. When 16 color palette is selected, BLNK will be FGCLR[3].
	FGCLR[2:0]	6:4	OSD sub window 0 Foreground Color select. 000: Color index 0. 001: Color index 1. ... 111: Color index 7.
	TRAN	5	OSD sub window 0 Transparency control. 0: Disable. 1: Enable. When 16 color palette is selected, TRAN will be BGCLR[3].
BGCLR[2:0]	2:0	OSD sub window 0 Background Color select. 000: Color index 0. 001: Color index 1.	

**OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)**

			...
			111: Color index 7.
28h	SUBW0A2	7:0	Default : 0x00
			Access : R/W, DB
	BTNCSEL[2:0]	7:5	When OSD register 0x10[7]=0, OSD is backward compatible. Reserved.
	BTNCSEL[2]	7	When OSD register 0x10[7]=1, OSD is not backward compatible. Button red color is selected.
	BTNCSEL[1]	6	Button green color is selected.
	BTNCSEL[0]	5	Button blue color is selected.
	BTNU	4	Button up Control. 0: Button up. 1: Button down.
	BTNTYPE[3:0]	3:0	Button border Type. 0: No button. 1:

1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
											-	-		-

Note: The register of sub window 1, 2, and 3 are very similar with sub window 0

29h	SUBW1C	7:0	Default : 0x00
			Access : R/W, DB
	-	7:4	Reserved.
	BTN1	3	Enable Button function for sub window 1.
	BD1	2	Enable OSD sub window 1 Border.
	S1C	1	Sub window 1 Color select.
	S1E	0	Enable OSD sub window 1.
2Ah	SW1HST	7:0	Default : 0x00
			Access : R/W, DB
	-	7:6	Reserved.
	SW1HST[5:0]	5:0	Sub Window 1 Horizontal Start Position.
2Bh	SW1HEND	7:0	Default : 0x00
			Access : R/W, DB
	-	7:6	Reserved.
	SW1HEND[5:0]	5:0	Sub Window 1 Horizontal End Position.
2Ch	SW1VST	7:0	Default : 0x00
			Access : R/W, DB
	-	7:5	Reserved.
	SW1VST[4:0]	4:0	Sub Window 1 Vertical Start Position.
2Dh	SW1VEND	7:0	Default : 0x00
			Access : R/W, DB
	-	7:5	Reserved.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	SW1VEND[4:0]	4:0	Sub Window 1 Vertical End Position.
2Eh	SUBW1A	7:0	Default : 0x00 Access : R/W
	BLNK	7	OSD sub window 1 Blink control.
	FGCLR[2:0]	6:4	OSD sub window 1 Foreground Color select.
	TRAN	5	OSD sub window 1 Transparency control.
	BGCLR[2:0]	2:0	OSD sub window 1 Background Color select.
2Fh	SUBW2C	7:0	Default : 0x00 Access : R/W, DB
	-	7:4	Reserved.
	BTN2	3	Enable Button function for sub window 2.
	BD2	2	Enable OSD sub window 2 Border.
	S2C	1	Sub window 2 Color select.
	S2E	0	Enable OSD sub window 2.
	30h	SW2HST	7:0
-		7:6	Reserved.
SW2HST[5:0]		5:0	Sub Window 2 Horizontal Start Position.
31h	SW2HEND	7:0	Default : 0x00 Access : R/W, DB
	-	7:6	Reserved.
	SW2HEND[5:0]	5:0	Sub Window 2 Horizontal End Position.
32h	SW2VST	7:0	Default : 0x00 Access : R/W, DB
	-	7:5	Reserved.
	SW2VST[4:0]	4:0	Sub Window 2 Vertical Start Position.
33h	SW2VEND	7:0	Default : 0x00 Access : R/W, DB
	-	7:5	Reserved.
	SW2VEND[4:0]	4:0	Sub Window 2 Vertical End Position.
34h	SUBW2A	7:0	Default : 0x00 Access : R/W
	BLNK	7	OSD sub window 2 Blink control.
	FGCLR[2:0]	6:4	OSD sub window 2 Foreground Color select.
	TRAN	5	OSD sub window 2 Transparency control.
	BGCLR[2:0]	2:0	OSD sub window 2 Background Color select.
35h	SUBW3C	7:0	Default : 0x00 Access : R/W, DB
	-	7:4	Reserved.
	BTN3	3	Enable Button function for sub window 3.
	BD3	2	Enable OSD sub window 3 Border.
	S3C	1	Sub window 3 Color select.
	S3E	0	Enable OSD sub window 3.

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)				
36h	SW3HST	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SW3HST[5:0]	5:0	Sub Window 3 Horizontal Start Position.	
37h	SW3HEND	7:0	Default : 0x00	Access : R/W, DB
	-	7:6	Reserved.	
	SW3HEND[5:0]	5:0	Sub Window 3 Horizontal End Position.	
38h	SW2VST	7:0	Default : 0x00	Access : R/W, DB
	-	7:5	Reserved.	
	SW3VST[4:0]	4:0	Sub Window 3 Vertical Start Position.	
39h	SW2VEND	7:0	Default : 0x00	Access : R/W, DB
	-	7:5	Reserved.	
	SW3VEND[4:0]	4:0	Sub Window 3 Vertical End Position.	
3Ah	SUBW3A	7:0	Default : 0x00	Access : R/W
	BLNK	7	OSD sub window 3 Blink control.	
	FGCLR[2:0]	6:4	OSD sub window 3 Foreground Color select.	
	TRAN	5	OSD sub window 3 Transparency control.	
	BGCLR[2:0]	2:0	OSD sub window 3 Background Color select.	
3Bh	OSD8CFFA	7:0	Default : 0x00	Access : R/W
	OSD8CFFA[7:0]	7:0	OSD 8 Color Font RAM start Address.	
3Ch	OSD8CFCA	7:0	Default : 0x00	Access : R/W
	OSD8CFCA[7:0]	7:0	OSD 8 Color Font Code start Address.	
3Dh	256CPKEY0	7:0	Default : 0x00	Access : R/W
	256CPKEY0[7:0]	7:0	256 Color Palette Key 0.	
3Eh	256CPKEY1	7:0	Default : 0x00	Access : R/W
	256CPKEY1[7:0]	7:0	256 Color Palette Key 1.	
3Fh	256CPKEY2	7:0	Default : 0x00	Access : R/W
	256CPKEY2[7:0]	7:0	256 Color Palette Key 2.	
40h	256CPCLCI	7:0	Default : 0x00	Access : R/W
	256CPCLCI[7:0]	7:0	256 Color Palette Character 1 Line Color Index.	
41h	OSDCFHA	7:0	Default : 0x00	Access : R/W
	OSD8CFFA[8]	7	See description for OSD8CFFA[7:0].	
	OSD8CFCA[8]		See description for OSD8CFCA[7:0].	
	-	5:4	Reserved.	
	OSD4CFA[8]	3	See description for OSD4CFA[7:0].	
-	2:0	Reserved.		

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)					
42h	~	-	7:0	Default : -	Access : -
57h		-	7:0	Reserved.	
OSD 8-Color Palette (when C16_PAL=0), 8-bit resolution					
58h	CLR0R		7:0	Default : 0x00	Access : R/W
	CLR0R[7:0]		7:0	R component of index 0.	
59h	CLR0G		7:0	Default : 0x00	Access : R/W
	CLR0G[7:0]		7:0	G component of index 0.	
5Ah	CLR0B		7:0	Default : 0x00	Access : R/W
	CLR0B[7:0]		7:0	B component of index 0.	
5Bh	CLR1R		7:0	Default : 0x00	Access : R/W
	CLR1R[7:0]		7:0	R component of index 1.	
5Ch	CLR1G		7:0	Default : 0x00	Access : R/W
	CLR1G[7:0]		7:0	G component of index 1.	
5Dh	CLR1B		7:0	Default : 0x00	Access : R/W
	CLR1B[7:0]		7:0	B component of index 1.	
5Eh	CLR2R		7:0	Default : 0x00	Access : R/W
	CLR2R[7:0]		7:0	R component of index 2.	
5Fh	CLR2G		7:0	Default : 0x00	Access : R/W
	CLR2G[7:0]		7:0	G component of index 2.	
60h	CLR2B		7:0	Default : 0x00	Access : R/W
	CLR2B[7:0]		7:0	B component of index 2.	
61h	CLR3R		7:0	Default : 0x00	Access : R/W
	CLR3R[7:0]		7:0	R component of index 3.	
62h	CLR3G		7:0	Default : 0x00	Access : R/W
	CLR3G[7:0]		7:0	G component of index 3.	
63h	CLR3B		7:0	Default : 0x00	Access : R/W
	CLR3B[7:0]		7:0	B component of index 3.	
64h	CLR4R		7:0	Default : 0x00	Access : R/W
	CLR4R[7:0]		7:0	R component of index 4.	
65h	CLR4G		7:0	Default : 0x00	Access : R/W
	CLR4G[7:0]		7:0	G component of index 4.	
66h	CLR4B		7:0	Default : 0x00	Access : R/W
	CLR4B[7:0]		7:0	B component of index 4.	
67h	CLR5R		7:0	Default : 0x00	Access : R/W
	CLR5R[7:0]		7:0	R component of index 5.	

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)				
68h	CLR5G	7:0	Default : 0x00	Access : R/W
	CLR5G[7:0]	7:0	G component of index 5.	
69h	CLR5B	7:0	Default : 0x00	Access : R/W
	CLR5B[7:0]	7:0	B component of index 5.	
6Ah	CLR6R	7:0	Default : 0x00	Access : R/W
	CLR6R[7:0]	7:0	R component of index 6.	
6Bh	CLR6G	7:0	Default : 0x00	Access : R/W
	CLR6G[7:0]	7:0	G component of index 6.	
6Ch	CLR6B	7:0	Default : 0x00	Access : R/W
	CLR6B[7:0]	7:0	B component of index 6.	
6Dh	CLR7R	7:0	Default : 0x00	Access : R/W
	CLR7R[7:0]	7:0	R component of index 7.	
6Eh	CLR7G	7:0	Default : 0x00	Access : R/W
	CLR7G[7:0]	7:0	G component of index 7.	
6Fh	CLR7B	7:0	Default : 0x00	Access : R/W
	CLR7B[7:0]	7:0	B component of index 7.	
OSD 16-Color Palette (when C16_PAL=1), 4-bit resolution 16 color format: col[7:4], 4'h0				
58h	CLR0R	7:0	Default : 0x00	Access : R/W
	CLR0R[7:4]	7:4	R component of index 0.	
	CLR8R[7:4]	3:0	R component of index 8.	
59h	CLR0G	7:0	Default : 0x00	Access : R/W
	CLR0G[7:4]	7:4	G component of index 0.	
	CLR8G[7:4]	3:0	G component of index 8.	
5Ah	CLR0B	7:0	Default : 0x00	Access : R/W
	CLR0B[7:4]	7:4	B component of index 0.	
	CLR8B[7:4]	3:0	B component of index 8.	
5Bh	CLR1R	7:0	Default : 0x00	Access : R/W
	CLR1R[7:4]	7:4	R component of index 1.	
	CLR9R[7:4]	3:0	R component of index 9.	
5Ch	CLR1G	7:0	Default : 0x00	Access : R/W
	CLR1G[7:4]	7:4	G component of index 1.	
	CLR9G[7:4]	3:0	G component of index 9.	
5Dh	CLR1B	7:0	Default : 0x00	Access : R/W
	CLR1B[7:4]	7:4	B component of index 1.	

OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	CLR9B[7:4]	3:0	B component of index 9.
5Eh	CLR2R	7:0	Default : 0x00 Access : R/W
	CLR2R[7:4]	7:4	R component of index 2.
	CLR10R[7:4]	3:0	R component of index 10.
5Fh	CLR2G	7:0	Default : 0x00 Access : R/W
	CLR2G[7:4]	7:4	G component of index 2.
	CLR10G[7:4]	3:0	G component of index 10.
60h	CLR2B	7:0	Default : 0x00 Access : R/W
	CLR2B[7:4]	7:4	B component of index 2.
	CLR10B[7:4]	3:0	B component of index 10.
61h	CLR3R	7:0	Default : 0x00 Access : R/W
	CLR3R[7:4]	7:4	R component of index 3.
	CLR11R[7:4]	3:0	R component of index 11.
62h	CLR3G	7:0	Default : 0x00 Access : R/W
	CLR3G[7:4]	7:4	G component of index 3.
	CLR11G[7:4]	3:0	G component of index 11.
63h	CLR4B	7:0	Default : 0x00 Access : R/W
	CLR4B[7:4]	7:4	B component of index 3.
	CLR11B[7:4]	3:0	B component of index 11.
64h	CLR4R	7:0	Default : 0x00 Access : R/W
	CLR4R[7:4]	7:4	R component of index 4.
	CLR12R[7:4]	3:0	R component of index 12.
65h	CLR4G	7:0	Default : 0x00 Access : R/W
	CLR4G[7:4]	7:4	G component of index 4.
	CLR12G[7:4]	3:0	G component of index 12.
66h	CLR4B	7:0	Default : 0x00 Access : R/W
	CLR4B[7:4]	7:4	B component of index 4.
	CLR12B[7:4]	3:0	B component of index 12.
67h	CLR5R	7:0	Default : 0x00 Access : R/W
	CLR5R[7:4]	7:4	R component of index 5.
	CLR13R[7:4]	3:0	R component of index 13.
68h	CLR5G	7:0	Default : 0x00 Access : R/W
	CLR5G[7:4]	7:4	G component of index 5.
	CLR13G[7:4]	3:0	G component of index 13.
69h	CLR5B	7:0	Default : 0x00 Access : R/W



OSD Register (Indirect mapping, using Bank 0 register A1h/A2h)			
	CLR5B[7:4]	7:4	B component of index 5.
	CLR13B[7:4]	3:0	B component of index 13.
6Ah	CLR6R	7:0	Default : 0x00      Access : R/W
	CLR6R[7:4]	7:4	R component of index 6.
	CLR14R[7:4]	3:0	R component of index 14.
6Bh	CLR6G	7:0	Default : 0x00      Access : R/W
	CLR6G[7:4]	7:4	G component of index 6.
	CLR14G[7:4]	3:0	G component of index 14.
6Ch	CLR6B	7:0	Default : 0x00      Access : R/W
	CLR6B[7:4]	7:4	B component of index 6.
	CLR14B[7:4]	3:0	B component of index 14.
6Dh	CLR7R	7:0	Default : 0x00      Access : R/W
	CLR7R[7:4]	7:4	R component of index 7.
	CLR15R[7:4]	3:0	R component of index 15.
6Eh	CLR7G	7:0	Default : 0x00      Access : R/W
	CLR7G[7:4]	7:4	G component of index 7.
	CLR15G[7:4]	3:0	G component of index 15.
6Fh	CLR7B	7:0	Default : 0x00      Access : R/W
	CLR7B[7:4]	7:4	B component of index 7.
	CLR15B[7:4]	3:0	B component of index 15.
70h	-	7:0	Default : 0x00      Access : -
	-	7:0	Reserved.
71h	OSDRTP	7:0	Default : 0x00      Access : R/W
	-	7:3	Reserved.
	RTPT	2	OSD Random Test Pattern Type. 0: RGB is same. 1: RGB is different.
	OSDRTP	1:0	OSD Random Test Pattern. 00: Disable. 01: 1 random bit. 10: 2 random bit. 11: Reserved.
72h	ATRODATA	7:0	Default : 0x00      Access : R/W
	ATROkDATA[7:0]	7:0	ATR SRAM Address0 Data read back.
72h ~ FFh	-	7:0	Default : 0x00      Access : -
	-	7:0	Reserved.



TCON Register (Bank = 02)

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
01h	-	7:0	Default : -	Access : -
	-	7:-	Reserved.	
02h	OFC1	7:0	Default : 0x02	Access : R/W
	IFC	7	Inversion Function Combined. 0: Odd data inversion determined by OINV, even data inversion determined by EINV. 1: Odd/Even data inversion both determined by OINV.	
	IFS	6	Inversion Function Swap. 0: OINV/EINV = 0 when data is inverted. 1: OINV/EINV = 1 when data is inverted.	
	IFE	5	Inversion Function Enable. 0: Disable. 1: Enable. When enabled, an indication is output for each data bus. If the number of transitions from pixel to pixel exceed 24 bits from 48 bits (or 18 bits from 36 bits for 6-bit panels), the data is inverted and an indication corresponding to that bus is set active.	
	DPFS	4	Data Polarity Function Swap (useful when DPFE = 1). 0: Odd data inversion determined by OPOL, even data inversion determined by EPOL. 1: Odd data inversion determined by OPOL, even data opposite of odd data.	
	DPFC	3	Data Polarity Function Control. 0: Data inversion when OPOL/EPOL is 0. 1: Data inversion when OPOL/EPOL is 1.	
	DPFE	2	Data Polarity Function Enable. 0: Disable. 1: Enable (line inversion, use OPOL/EPOL to determine that polarity of the output data).	
	EEF	1	Early End Function. 0: Disable. 1: Enable.	
03h	TCEN	0	Timing Controller Enable. 0: Disable. 1: Enable.	
	OFC2	7:0	Default : 0x00	Access : R/W
	ESPP	7	Even Start Pulse Position.	

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
			0: Start pulse before data. 1: Start pulse after data.	
	ESPO[2:0]	6:4	Even Start Pulse Offset. 000: Start pulse 0 clocks before/after data. 001: Start pulse 1 clocks before/after data. 010: Start pulse 2 clocks before/after data. ... 111: Start pulse 7 clocks before/after data.	
	OSPP	3	Odd Start Pulse Position. 0: Start pulse before data. 1: Start pulse after data.	
	OSPO[2:0]	2:0	Odd Start Pulse Offset. 000: Start pulse 0 clocks before/after data. 001: Start pulse 1 clocks before/after data. 010: Start pulse 2 clocks before/after data. ... 111: Start pulse 7 clocks before/after data.	
04h	ODPC	7:0	Default : 0x00	Access : R/W
	OESPDC[1:0]	7:6	OSP/ESP Drive Control. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	GODC[1:0]	5:4	OPOL/EPOL/GPO Drive Control. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	ECP	3	ECLK Polarity. 0: Normal. 1: Inverted.	
	-	2	Reserved.	
	OCP	1	OCLK Polarity. 0: Normal. 1: Inverted.	
	-	0	Reserved.	
05h	ODC	7:0	Default : 0x00	Access : R/W
	EDDC[1:0]	7:6	EINV Driver Control.	

TCON Register (Bank = 02)			
Index	Mnemonic	Bits	Description
			00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.
	OIDC	5:4	OINV Drive Control.
	-	3	Reserved.
	OFTG	2	One Frame Toggle mode.
	RSBMLSW	1	RSDS B-port MSB/LSB Swap. Bank 0 reg 0x42[5] = 0 and 0x42[2] = 1: 0: Default. 1: B-port MSB/LSB swap for 8-bit RSDS output. Bank 0 reg 0x42[5] = 0 and 0x42[2] = 1: 0: Default. 1: B-port MSB/LSB swap for 6-bit RSDS output.
	RSAMLSW	0	RSDS A-port MSB/LSB Swap. Bank 0 reg 0x42[5] = 0 and 0x42[3] = 1: 0: Default. 1: A-port MSB/LSB swap for 8-bit RSDS output. Bank 0 reg 0x42[5] = 0 and 0x42[3] = 1: 0: Default. 1: A-port MSB/LSB swap for 6-bit RSDS output.
06h	GPO4ADF	7:0	Default : 0x00
	-	7:3	Reserved.
	GPO4ADF[2:0]	2:0	GPO4 (OE) Active Delay time. 000: No delay. 001: Delay 1 frame. ... 111: Delay 7 frames.
07h	IFCTRL	7:0	Default : 0x00
	WDG	7	White Data Generation (TCON feature only). 0: Black data generation during vertical blanking (GPOA). 1: Enable white data generation during vertical blanking (GPOA).
	PUA	6	Power-up Active (TCON feature only). 0: Outputs inactive. 1: Outputs active.
	GOAT	5	GPO0 Auto Toggle (TCON feature only). 0: Disable. 1: Enable.
	GDEEN	4	Gate DE Enable.

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
	DATI	3	Data Invert (TCON feature only). 0: Off. 1: On.	
	POLB	2	Polarity Blanked Enable (TCON feature only). 0: Disable. 1: Enable (EPOL/OPOL will be forced to blanked when GPOA is low).	
	SPB	1	Start Pulse Blanked enable (TCON feature only). 0: Disable. 1: Enable (EPOL/OPOL will be forced to blanked when GPOA is low).	
	CLKB	0	Clock Blanked Enable. 0: Disable. 1: Enable (ECLK/OCLK will be forced to blanked when GPOA is low).	
08h	GOVST-L	7:0	Default : 0x00	Access : R/W
	GOVST[7:0]	7:0	Line number that GPO0 start.	
09h	GOVST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GOVST[10:8]	2:0	See description for GOVST[7:0].	
0Ah	GOVEND-L	7:0	Default : 0x00	Access : R/W
	GOVEND[7:0]	7:0	Line number that GPO0 ends.	
0Bh	GOVEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GOVEND[10:8]	2:0	See description for GOVEND[7:0].	
0Ch	GOHST-L	7:0	Default : 0x00	Access : R/W
	GOHST[7:0]	7:0	Pixel number that GPO0 start.	
0Dh	GOHST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GOVHT[10:8]	2:0	Pixel description for GOHST[7:0].	
0Eh	GOHEND-L	7:0	Default : 0x00	Access : R/W
	GOHEND[7:0]	7:0	Pixel number that GPO0 ends.	
0Fh	GOHEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GOHEND[10:8]	2:0	See description for GOHEND[7:0].	
10h	COCTRL	7:0	Default : 0x00	Access : R/W

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
	COCS[2:0]	7:5	GPO0 Combination select. 000: No combination. 001: And. 010: Or. 011: Select GPO# and GPO#-1 on alternating frames. 1xx: Auto select 1 or 2 line toggle according to ATP value.	
	GOTS[1:0]	4:3	GPO0 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time. 10: Every two lines have one GPO0 pulse. 11: Every three lines have one GPO0 pulse. When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	GOES	2	GPO0 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (GOVST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	GOTC	1	GPO0 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	GOOP	0	GPO0 Output Polarity. 0: Active high. 1: Active low.	
11h	G1VST-L	7:0	Default : 0x00	Access : R/W
	G1VST[7:0]	7:0	Line number that GPO1 start.	
12h	G1VST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G1VST[10:8]	2:0	See description for G1VST[7:0].	
13h	G1VEND-L	7:0	Default : 0x00	Access : R/W

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
	G1VEND[7:0]	7:0	Line number that GPO1 ends.	
14h	G1VEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G1VEND[10:8]	2:0	See description for G1VEND[7:0].	
15h	G1HST-L	7:0	Default : 0x00	Access : R/W
	G1HST[7:0]	7:0	Pixel number that GPO1 start.	
16h	G1HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G1VHT[10:8]	2:0	Pixel description for G1HST[7:0].	
17h	G1HEND-L	7:0	Default : 0x00	Access : R/W
	G1HEND[7:0]	7:0	Pixel number that GPO1 ends.	
18h	G1HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G1HEND[10:8]	2:0	See description for G1HEND[7:0].	
19h	C1CTRL	7:0	Default : 0x00	Access : R/W
	C1CS[2:0]	7:5	GPO1 Combination select.	
	G1TS[1:0]	4:3	GPO1 Type Select.	
	G1ES	2	GPO1 Early Start function.	
	G1TC	1	GPO1 Toggle Circuit enable.	
	G1OP	0	GPO1 Output Polarity.	
1Ah	G2VST-L	7:0	Default : 0x00	Access : R/W
	G2VST[7:0]	7:0	Line number that GPO2 start.	
1Bh	G2VST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G2VST[10:8]	2:0	See description for G2VST[7:0].	
1Ch	G2VEND-L	7:0	Default : 0x00	Access : R/W
	G2VEND[7:0]	7:0	Line number that GPO2 ends.	
1Dh	G2VEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G2VEND[10:8]	2:0	See description for G2VEND[7:0].	
1Eh	G2HST-L	7:0	Default : 0x00	Access : R/W
	G2HST[7:0]	7:0	Pixel number that GPO2 start.	
1Fh	G2HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
	G2VHT[10:8]	2:0	Pixel description for G2HST[7:0].	
20h	G2HEND-L	7:0	Default : 0x00	Access : R/W
	G2HEND[7:0]	7:0	Pixel number that GPO2 ends.	
21h	G2HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G2HEND[10:8]	2:0	See description for G2HEND[7:0].	
22h	C2CTRL	7:0	Default : 0x00	Access : R/W
	C2CS[2:0]	7:5	GPO2 Combination select.	
	G2TS[1:0]	4:3	GPO2 Type Select.	
	G2ES	2	GPO2 Early Start function.	
	G2TC	1	GPO2 Toggle Circuit enable.	
	G2OP	0	GPO2 Output Polarity.	
23h	G3VST-L	7:0	Default : 0x00	Access : R/W
	G3VST[7:0]	7:0	Line number that GPO3 start.	
24h	G3VST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G3VST[10:8]	2:0	See description for G3VST[7:0].	
25h	G3VEND-L	7:0	Default : 0x00	Access : R/W
	G3VEND[7:0]	7:0	Line number that GPO3 ends.	
26h	G3VEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G3VEND[10:8]	2:0	See description for G3VEND[7:0].	
27h	G3HST-L	7:0	Default : 0x00	Access : R/W
	G3HST[7:0]	7:0	Pixel number that GPO3 start.	
28h	G3HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G3VHT[10:8]	2:0	Pixel description for 3HST[7:0].	
29h	G3HEND-L	7:0	Default : 0x00	Access : R/W
	G3HEND[7:0]	7:0	Pixel number that GPO3 ends.	
2Ah	G3HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G3HEND[10:8]	2:0	See description for G3HEND[7:0].	
2Bh	C3CTRL	7:0	Default : 0x00	Access : R/W
	C3CS[2:0]	7:5	GPO3 Combination select.	

TCON Register (Bank = 02)			
Index	Mnemonic	Bits	Description
	G3TS[1:0]	4:3	GPO3 Type Select.
	G3ES	2	GPO3 Early Start function.
	G3TC	1	GPO3 Toggle Circuit enable.
	G3OP	0	GPO3 Output Polarity.
2Ch	G4VST-L	7:0	Default : 0x00 Access : R/W
	G4VST[7:0]	7:0	Line number that GPO4 start.
2Dh	G4VST -H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	G4VST[10:8]	2:0	See description for G4VST[7:0].
2Eh	G4VEND-L	7:0	Default : 0x00 Access : R/W
	G4VEND[7:0]	7:0	Line number that GPO4 ends.
2Fh	G4VEND -H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	G4VEND[10:8]	2:0	See description for G4VEND[7:0].
30h	G4HST-L	7:0	Default : 0x00 Access : R/W
	G4HST[7:0]	7:0	Pixel number that GPO4 start.
31h	G4HST -H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	G4VHT[10:8]	2:0	Pixel description for G4HST[7:0].
32h	G4HEND-L	7:0	Default : 0x00 Access : R/W
	G4HEND[7:0]	7:0	Pixel number that GPO4 ends.
33h	G4HEND -H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	G4HEND[10:8]	2:0	See description for G4HEND[7:0].
34h	C4CTRL	7:0	Default : 0x00 Access : R/W
	C4CS[2:0]	7:5	GPO4 Combination select.
	G4TS[1:0]	4:3	GPO4 Type Select.
	G4ES	2	GPO4 Early Start function.
	G4TC	1	GPO4 Toggle Circuit enable.
	G4OP	0	GPO4 Output Polarity.
35h	G5VST-L	7:0	Default : 0x00 Access : R/W
	G5VST[7:0]	7:0	Line number that GPO5 start.
36h	G5VST -H	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.



TCON Register (Bank = 02)			
Index	Mnemonic	Bits	Description
	G5VST[10:8]	2:0	See description for G5VST[7:0].
37h	G5VEND-L	7:0	Default : 0x00
	G5VEND[7:0]	7:0	Line number that GPO5 ends.
38h	G5VEND -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G5VEND[10:8]	2:0	See description for G5VEND[7:0].
39h	G5HST-L	7:0	Default : 0x00
	G5HST[7:0]	7:0	Pixel number that GPO5 start.
3Ah	G5HST -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G5VHT[10:8]	2:0	Pixel description for G5HST[7:0].
3Bh	G5HEND-L	7:0	Default : 0x00
	G5HEND[7:0]	7:0	Pixel number that GPO5 ends.
3Ch	G5HEND -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G5HEND[10:8]	2:0	See description for G5HEND[7:0].
3Dh	C5CTRL	7:0	Default : 0x00
	C5CS[2:0]	7:5	GPO5 Combination select.
	G5TS[1:0]	4:3	GPO5 Type Select.
	G5ES	2	GPO5 Early Start function.
	G5TC	1	GPO5 Toggle Circuit enable.
	G5OP	0	GPO5 Output Polarity.
3Eh	G6VST-L	7:0	Default : 0x00
	G6VST[7:0]	7:0	Line number that GPO6 start.
3Fh	G6VST -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G6VST[10:8]	2:0	See description for G6VST[7:0].
40h	G6VEND-L	7:0	Default : 0x00
	G6VEND[7:0]	7:0	Line number that GPO6 ends.
41h	G6VEND -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G6VEND[10:8]	2:0	See description for G6VEND[7:0].
42h	G6HST-L	7:0	Default : 0x00
	G6HST[7:0]	7:0	Pixel number that GPO6 start.

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
43h	G6HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G6VHT[10:8]	2:0	Pixel description for G6HST[7:0].	
44h	G6HEND-L	7:0	Default : 0x00	Access : R/W
	G6HEND[7:0]	7:0	Pixel number that GPO6 ends.	
45h	G6HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G6HEND[10:8]	2:0	See description for G6HEND[7:0].	
46h	C6CTRL	7:0	Default : 0x00	Access : R/W
	C6CS[2:0]	7:5	GPO6 Combination select.	
	G6TS[1:0]	4:3	GPO6 Type Select.	
	G6ES	2	GPO6 Early Start function.	
	G6TC	1	GPO6 Toggle Circuit enable.	
	G6OP	0	GPO6 Output Polarity.	
47h	G7VST-L	7:0	Default : 0x00	Access : R/W
	G7VST[7:0]	7:0	Line number that GPO7 start.	
48h	G7VST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G7VST[10:8]	2:0	See description for G7VST[7:0].	
49h	G7VEND-L	7:0	Default : 0x00	Access : R/W
	G7VEND[7:0]	7:0	Line number that GPO7 ends.	
4Ah	G7VEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G7VEND[10:8]	2:0	See description for G7VEND[7:0].	
4Bh	G7HST-L	7:0	Default : 0x00	Access : R/W
	G7HST[7:0]	7:0	Pixel number that GPO7 start.	
4Ch	G7HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G7VHT[10:8]	2:0	Pixel description for G7HST[7:0].	
4Dh	G7HEND-L	7:0	Default : 0x00	Access : R/W
	G7HEND[7:0]	7:0	Pixel number that GPO7 ends.	
4Eh	G7HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G7HEND[10:8]	2:0	See description for G7HEND[7:0].	

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
4Fh	C7CTRL	7:0	Default :	Access : R/W
	C7CS[2:0]	7:5	GPO7 Combination select.	
	G7TS[1:0]	4:3	GPO7 Type Select.	
	G7ES	2	GPO7 Early Start function.	
	G7TC	1	GPO7 Toggle Circuit enable.	
	G7OP	0	GPO7 Output Polarity.	
50h	G8VST-L	7:0	Default : 0x00	Access : R/W
	G8VST[7:0]	7:0	When Bank 0 register ABh[7] = 0: G8VST[10:0]: Line number that GPO8 start. When Bank 0 register ABh[7] = 1: G8VST-L[7:0]: GPO[7:0] gating control. G8VST-H[1:0]: O(E)SP / O(E)INV gating control.	
51h	G8VST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G8VST[10:8]	2:0	See description for G8VST[7:0].	
52h	G8VEND-L	7:0	Default : 0x00	Access : R/W
	G8VEND[7:0]	7:0	Line number that GPO8 ends.	
53h	G8VEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G8VEND[10:8]	2:0	See description for G8VEND[7:0].	
54h	G8HST-L	7:0	Default : 0x00	Access : R/W
	G8HST[7:0]	7:0	Pixel number that GPO8 start.	
55h	G8HST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G8VHT[10:8]	2:0	Pixel description for G8HST[7:0].	
56h	G8HEND-L	7:0	Default : 0x00	Access : R/W
	G8HEND[7:0]	7:0	Pixel number that GPO8 ends.	
57h	G8HEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	G8HEND[10:8]	2:0	See description for G8HEND[7:0].	
58h	C6CTRL	7:0	Default : 0x00	Access : R/W
	C8CS[2:0]	7:5	GPO8 Combination select.	
	G8TS[1:0]	4:3	GPO8 Type Select.	
	G8ES	2	GPO8 Early Start function.	
	G8TC	1	GPO8 Toggle Circuit enable.	

TCON Register (Bank = 02)			
Index	Mnemonic	Bits	Description
	G8OP	0	GPO8 Output Polarity.
59h	G9VST-L	7:0	Default : 0x07
	G9VST[7:0]	7:0	Line number that GPO9 start.
5Ah	G9VST -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G9VST[10:8]	2:0	See description for G9VST[7:0].
5Bh	G9VEND-L	7:0	Default : 0x05
	G9VEND[7:0]	7:0	Line number that GPO9 ends.
5Ch	G9VEND -H	7:0	Default : 0x07
	-	7:3	Reserved.
	G9VEND[10:8]	2:0	See description for G9VEND[7:0].
5Dh	G9HST-L	7:0	Default : 0x00
	G9HST[7:0]	7:0	Pixel number that GPO9 start.
5Eh	G9HST -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G9VHT[10:8]	2:0	Pixel description for G9HST[7:0].
5Fh	G9HEND-L	7:0	Default : 0x00
	G9HEND[7:0]	7:0	Pixel number that GPO9 ends.
60h	G9HEND -H	7:0	Default : 0x00
	-	7:3	Reserved.
	G9HEND[10:8]	2:0	See description for G9HEND[7:0].
61h	C9CTRL	7:0	Default : 0x04
	C9CS[2:0]	7:5	GPO9 Combination select.
	G9TS[1:0]	4:3	GPO9 Type Select.
	G9ES	2	GPO9 Early Start function.
	G9TC	1	GPO9 Toggle Circuit enable.
	G9OP	0	GPO9 Output Polarity.
62h	GAVST-L	7:0	Default : 0x00
	G7VST[7:0]	7:0	Line number that GPOA start.
63h	GAVST -H	7:0	Default : 0x00
	-	7:3	Reserved.
	GAVST[10:8]	2:0	See description for GAVST[7:0].
64h	GAVEND-Lhjh	7:0	Default : 0x00
	GAVEND[7:0]	7:0	Line number that GPOA ends.

TCON Register (Bank = 02)				
Index	Mnemonic	Bits	Description	
65h	GAVEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GAVEND[10:8]	2:0	See description for GAVEND[7:0].	
66h	GAHST-L	7:0	Default : 0x00	Access : R/W
	GAHST[7:0]	7:0	Pixel number that GPOA start.	
67h	GAHST -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GAVHT[10:8]	2:0	Pixel description for GAHST[7:0].	
68h	GAHEND-L	7:0	Default : 0x00	Access : R/W
	GAHEND[7:0]	7:0	Pixel number that GPOA ends.	
69h	GAHEND -H	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GAHEND[10:8]	2:0	See description for GAHEND[7:0].	
6Ah	CACTRL	7:0	Default : 0x00	Access : R/W
	CACS[2:0]	7:5	GPOA Combination select.	
	GATS[1:0]	4:3	GPOA Type Select.	
	GAES	2	GPOA Early Start function.	
	GATC	1	GPOA Toggle Circuit enable.	
	GAOP	0	GPOA Output Polarity.	
6Bhh ~	-	7:0	Default : -	Access : -
FFh	-	7:0	Reserved.	

MWE Register (Bank = 03)

MWE Register (Bank = 03)				
Index	Mnemonic	Bits	Description	
01h ~	-	7:0	Default : -	Access : -
16h	-	7:0	Reserved.	
17h	SW2CTL	7:0	Default : 0x00	Access : R/W, DB
	-	7	Reserved.	
	MWEW3EN	6	MWE window 3 Enable	
	MWEW2EN	5	MWE window 2 Enable	
	MWEW1EN	4	MWE Window 1 Enable.	
	-	3:2	Reserved.	
	MWE_WSEL[1:0]	1:0	MWE window Select.	

MWE Register (Bank = 03)				
			00: MWE window 0. 01: MWE window 1. 10: MWE window 2. 11: MWE window 3.	
18h	MWEHST-L	7:0	Default : 0x00	Access : R/W, DB
	MWEHST[7:0]	7:0	MWE window Horizontal Start.	
19h	MWEHST-H	7:0	Default : 0x00	Access : R/W, DB
	-	7:3	Reserved.	
	MWEHST[10:8]	2:0	See description for MWEHST[7:0].	
1Ah	MWEVEND-L	7:0	Default : 0x06	Access : R/W, DB
	MWEVEND[7:0]	7:0	MWE window Vertical END.	
1Bh	MWEVEND-H	7:0	Default : 0x00	Access : R/W, DB
	-	7:3	Reserved.	
	MWEVEND[10:8]	2:0	See description for MWEVEND[7:0].	
1Ch	MWEHEND-L	7:0	Default : 0x00	Access : R/W, DB
	MWEHEND[7:0]	7:0	MWE window Horizontal END.	
1Dh	MWEHEND-H	7:0	Default : 0x00	Access : R/W, DB
	-	7:3	Reserved.	
	MWEHEND[10:8]	2:0	See description for MWEHEND[7:0].	
1Eh	MWEVST-L	7:0	Default : 0x00	Access : R/W, DB
	MWEVST[7:0]	7:0	MWE of Sub window Vertical Start.	
1Fh	MWEVST-H	7:0	Default : 0x00	Access : R/W, DB
	-	7:3	Reserved.	
	MWEVST [10:8]	2:0	See description for MWEVST [7:0].	
20h	-	7:0	Default : -	Access : -
3Ah	-	7:0	Reserved.	
3Bh	SPPCTRL	7:0	Default : 0x01	Access : R/W
	-	7:3	Reserved.	
	MWECEN	2	MWE window C Peaking Enable.	
	MWEYEN	1	MWE window Y Peaking Enable.	
	MWEPEN	0	MWE window Peaking Function Enable.	
3Ch	SCORING	7:0	Default : 0x00	Access : R/W
	SCTH_2[3:0]	7:4	MWE window Coring Threshold.	
	SCTH_1[3:0]	3:0	MWE window Coring Threshold.	
3Dh	MWECPK	7:0	Default : 0x08	Access : R/W

MWE Register (Bank = 03)			
	CPK_STP[1:0]	7:6	MWE window C Peaking Step.
	-	5	Reserved.
	CPK_COEF[4:0]	4:0	MWE window C Peaking Coefficient.
3Eh	-	7:0	Default : -      Access : -
	-	7:0	Reserved.
3Fh	MWEYPK	7:0	Default : 0x08      Access : R/W
	YPK_STP[1:0]	7:6	MWE window Y Peaking Step.
	-	5	Reserved.
	YPK_COEF[4:0]	4:0	MWE window Y Peaking Coefficient.
40h	SGAMMAC	7:0	Default : 0x00      Access : R/W
	-	7:5	Reserved.
	SGCR	4	MWE window Gamma Correction Rounding function. 0: Disable. 1: Enable.
	-	3:1	Reserved.
	SGCB	0	MWE window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.
42h ~ FFh	-	7:0	Default : -      Access : -
	-	7:0	Reserved.

### REGISTER TABLE REVISION HISTORY

Date	Bank	Register
07/12/04		Y Created first version.
07/30/04	01	Y 0x0A, 0x0B, 0x17
08/04/04	00	Y 0xF8
09/01/04	01	Y 0x15
09/29/04	01	Y 0x15
10/01/04	00	Y 0x32
	03	Y 0x10-0x13, 0x47

This page is intended to leave blank.

MStar Confidential  
for Honestar  
Internal Use Only