

TSD65R600WT/TSU65R600WT

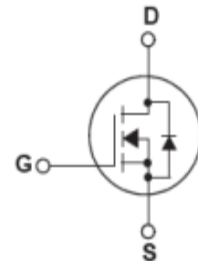
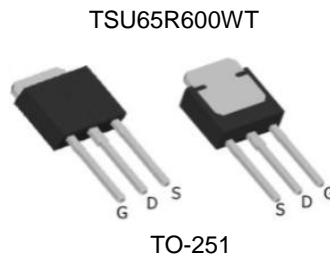
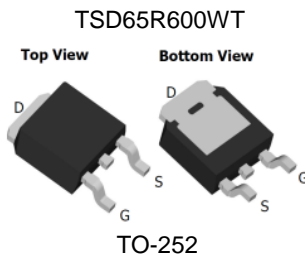
650V 7.5A N-Channel SJ-MOSFET

General Description

Truesemi SJ-FET is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance. This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. SJ-FET is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

Features

- 700V @T_J = 150 °C
- Max. RDS(on) = 0.6Ω
- Ultra Low gate charge (typ. Q_g = 14nC)
- 100% avalanche tested



Absolute Maximum Ratings

T_C=25°C unless otherwise specified

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-Source Voltage	650	V
I _D	Drain Current -Continuous (T _C = 25 °C) -Continuous (T _C = 100 °C)	7.5 4.7	A
I _{DM}	Drain Current – Pulsed (Note 1)	22	A
V _{GSS}	Gate-Source voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	160	mJ
P _D	Power Dissipation (T _A = 25 °C) * Power Dissipation (T _C = 25 °C)	2.5 57	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	--	2.2	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient*	--	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

*When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A,$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V$ $T_J = 25^\circ\text{C}$	--	--	10	μA
		$V_{DS} = 520V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current,	$V_{GS} = \pm 30V, V_{DS} = 0V$	--	--	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 2.5A$	--	0.54	0.6	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	--	590	770	pF
C_{OSS}	Output Capacitance		--	41	54	pF
C_{RSS}	Reverse Transfer Capacitance		--	6.5	8.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 325V, I_D = 7.5A$ $R_G = 25\Omega$	--	18	46	ns
t_r	Turn-On Rise Time		--	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	60	130	ns
t_f	Turn-Off Fall Time		--	22	54	ns
Q_g	Total Gate Charge	$V_{DS} = 520V, I_D = 7.5A$ $V_{GS} = 10V$	--	14.0	18.5	nC
Q_{gs}	Gate-Source Charge		--	3.2	--	nC
Q_{gd}	Gate-Drain Charge		--	4.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	22	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_F = 7.5A$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_F = 7.5A$ $di_F/dt = 100A/\mu s$	--	300	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS}=3.0A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

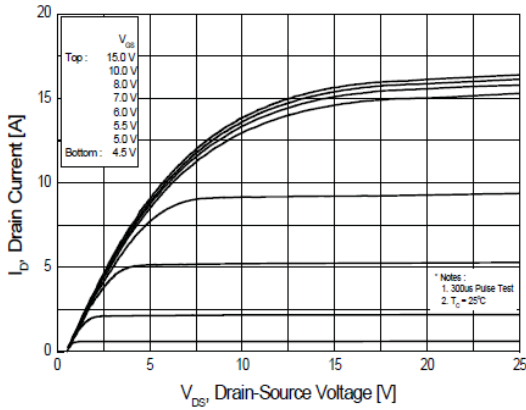


Figure 1. On Region Characteristics

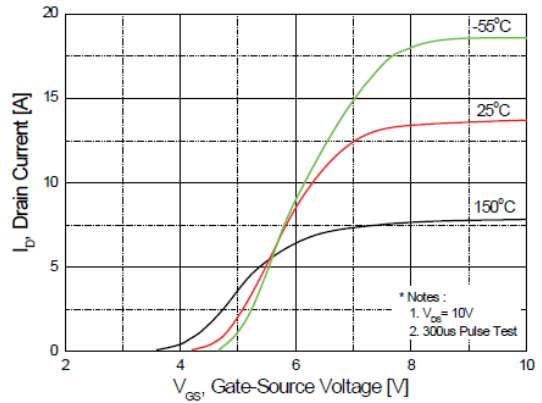


Figure 2. Transfer Characteristics

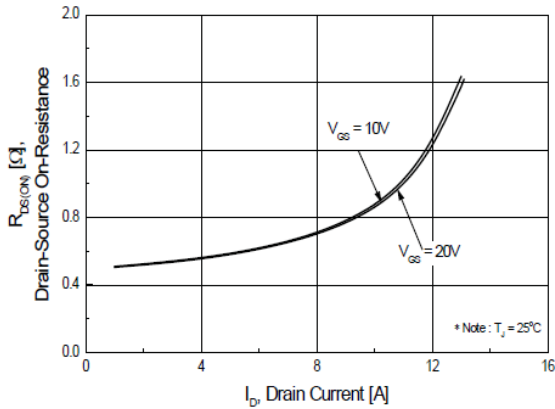


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

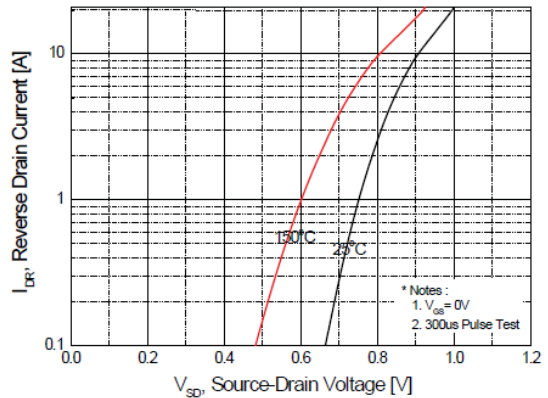


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

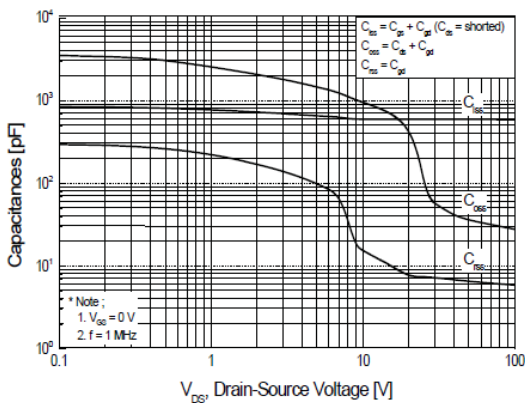


Figure 5. Capacitance Characteristics

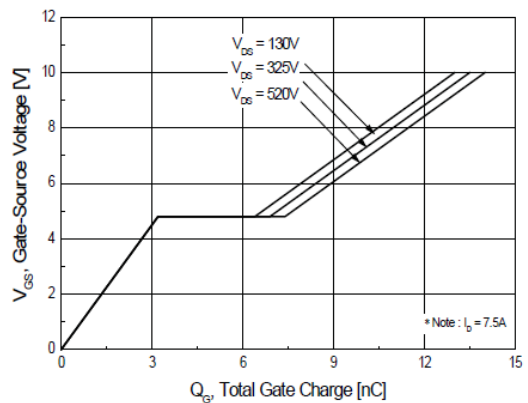


Figure 6. Gate Charge Characteristics

Typical Performance Characteristics

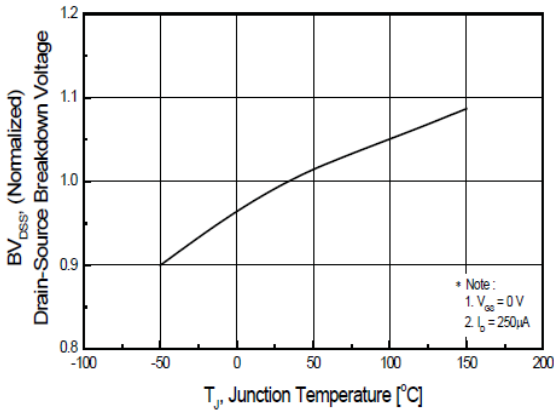


Figure 7. Breakdown Voltage Variation vs Temperature

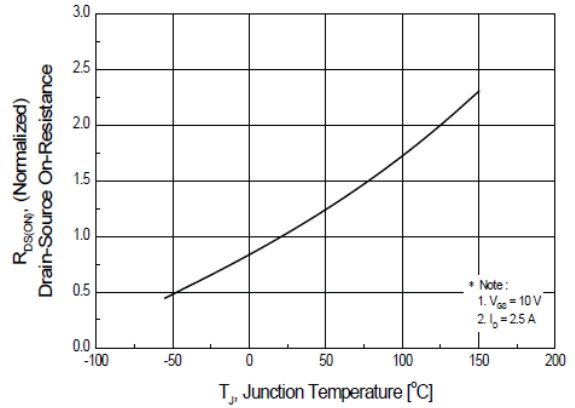


Figure 8. On-Resistance Variation vs Temperature

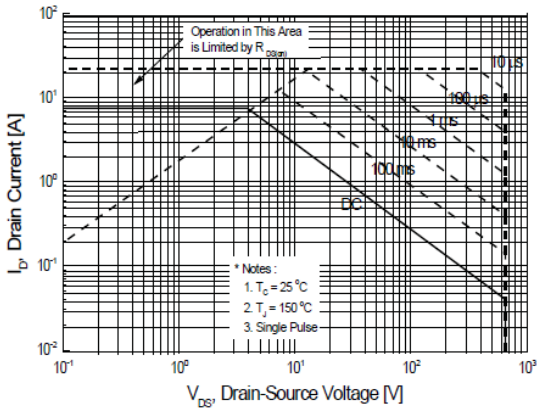


Figure 9. Maximum Safe Operating Area

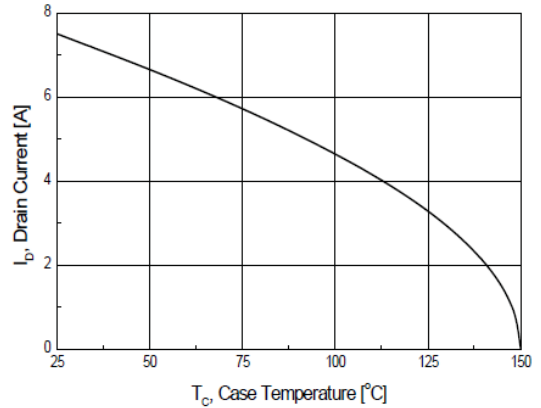


Figure 10. Maximum Drain Current vs Case Temperature

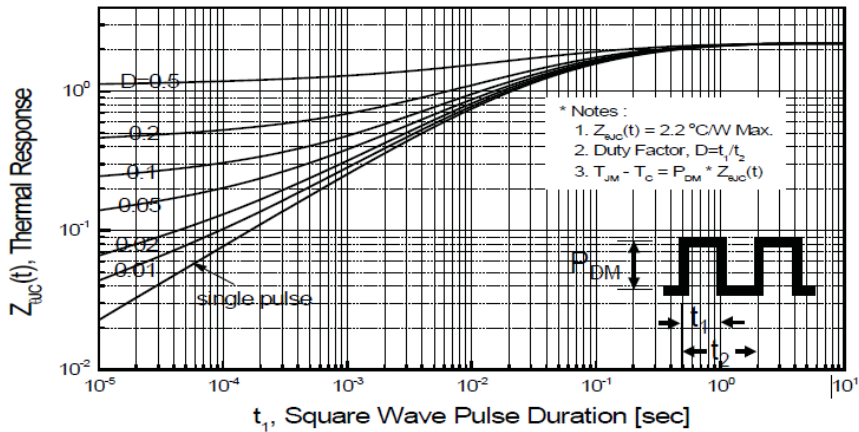
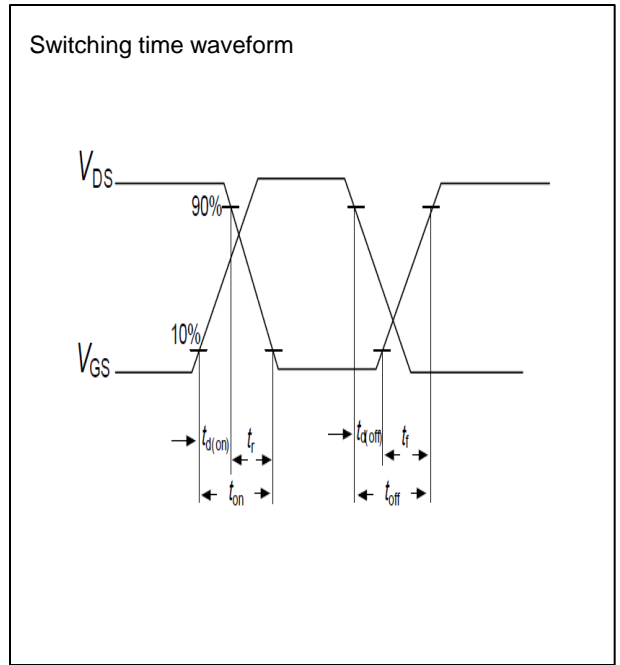
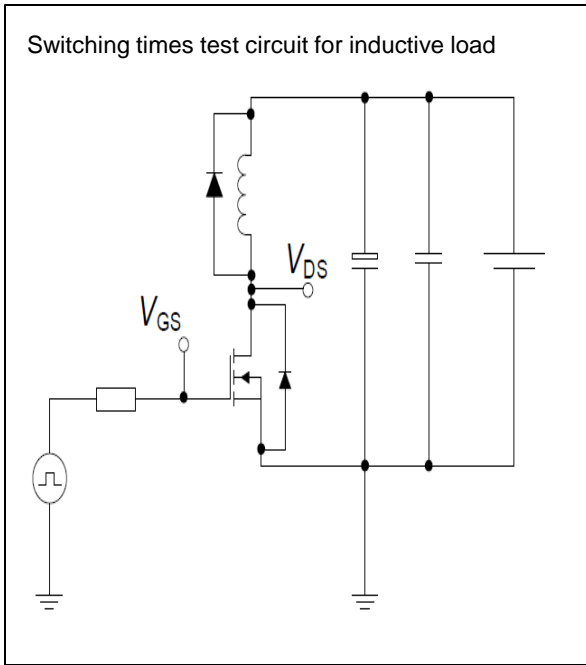


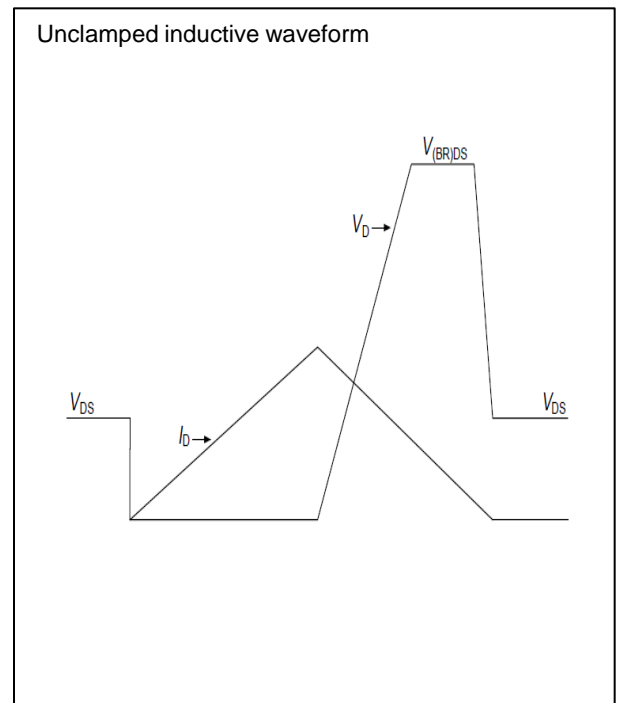
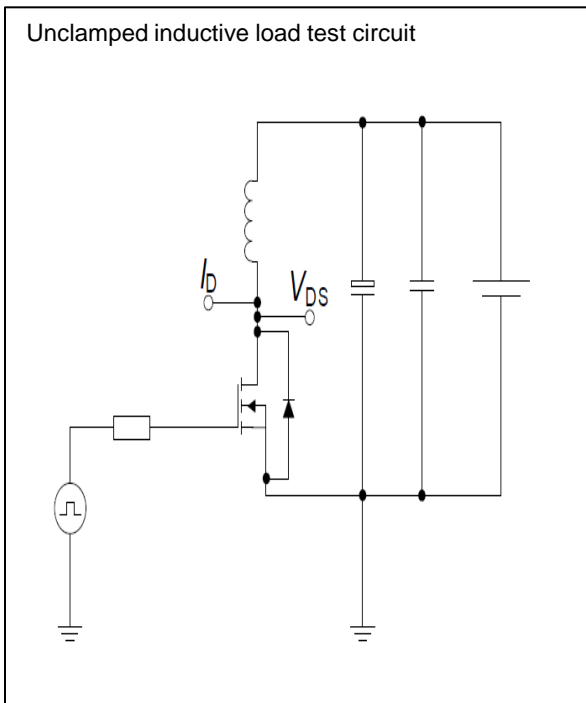
Figure 11. Transient Thermal Response Curve

Test circuits

Switching times test circuit and waveform for inductive load

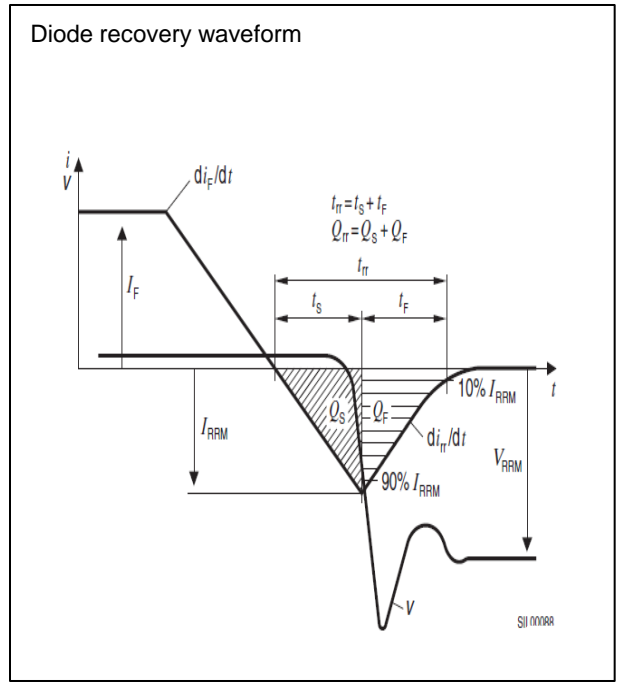
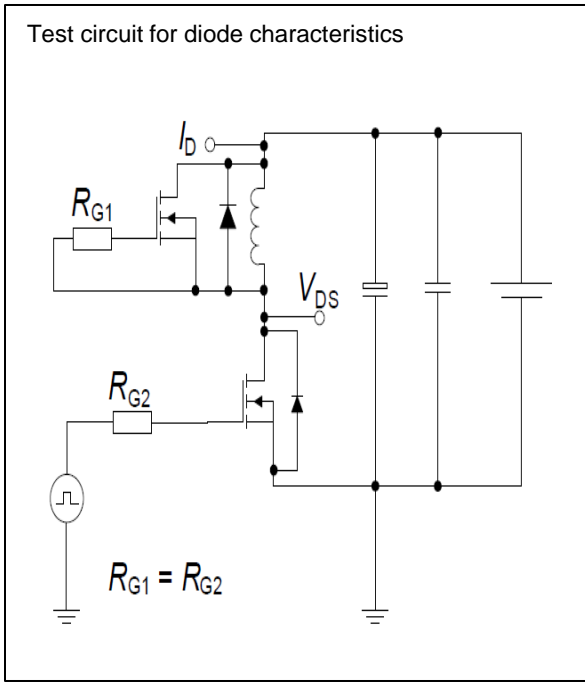


Unclamped inductive load test circuit and waveform



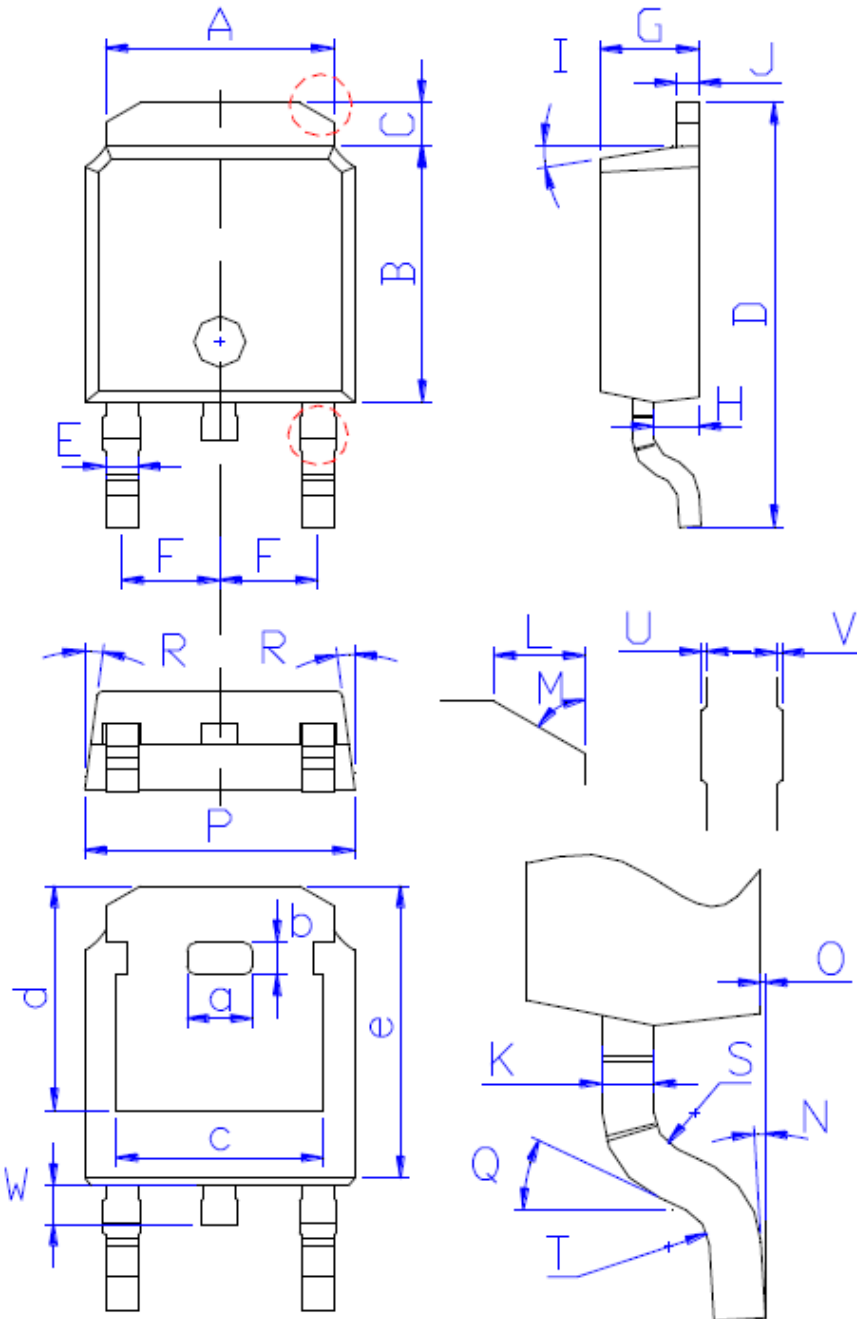
Test circuits

Test circuit and waveform for diode characteristics



Package Outline TO-252

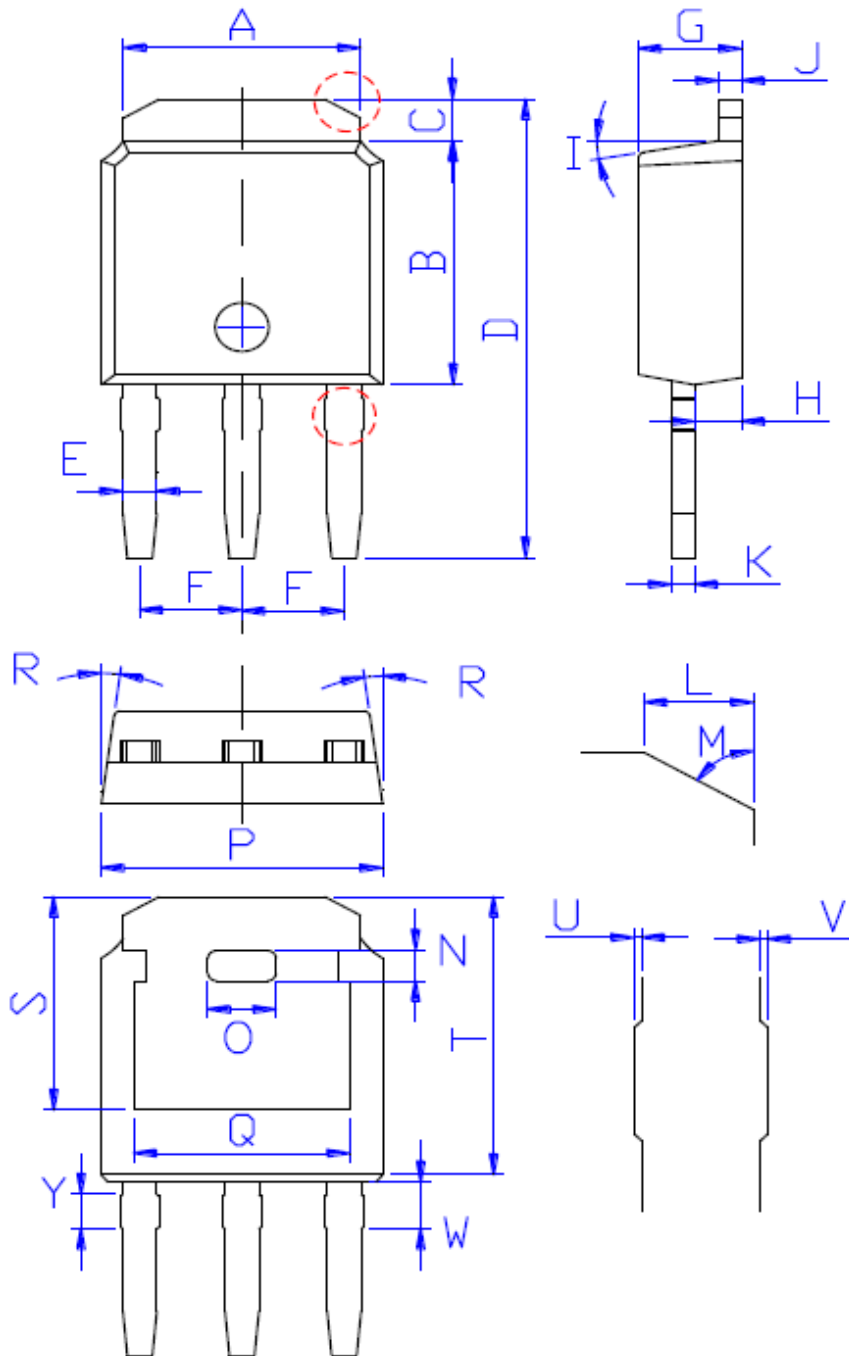
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DIM	MILLIMETERS
A	5.34 ± 0.30
B	6.00 ± 0.30
C	1.05 ± 0.30
D	9.95 ± 0.30
E	0.76 ± 0.15
F	2.28 ± 0.15
G	2.30 ± 0.30
H	1.06 ± 0.30
I	$(4-10)^\circ$
J	0.51 ± 0.15
K	0.52 ± 0.15
L	0.80 ± 0.30
M	60°
N	$(0-10)^\circ$
O	0.05 ± 0.05
P	6.60 ± 0.30
Q	25°
R	$(4-8.5)^\circ$
S	R0.40
T	R0.40
U	0.05 ± 0.05
V	0.05 ± 0.05
W	0.90 ± 0.30
a	1.80 ± 0.30
b	0.75 ± 0.30
c	4.85 ± 0.30
d	5.30 ± 0.30
e	6.90 ± 0.30

Package Outline TO-251

TSD65R600WT/TSU65R600WT 650V 7.5A N-Channel SJ-MOSFET



DIM	MILLIMETERS
A	5.34±0.30
B	6.00±0.30
C	1.05±0.30
D	11.31±0.30
E	0.76±0.15
F	2.28±0.15
G	2.30±0.30
H	1.06±0.30
I	(4-10)°
J	0.51±0.15
K	0.52±0.15
L	0.80±0.30
M	60°
N	0.75±0.30
O	1.80±0.30
P	6.60±0.30
Q	4.85±0.30
R	(4-8.5)°
S	5.30±0.30
T	6.90±0.30
U	0.05±0.05
V	0.05±0.05
W	1.15±0.25
Y	0.85±0.25