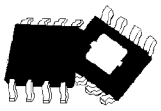
TSX582

Datasheet

200 mA, output current with thermal shutdown and output current limiter, 3 MHz, 16 V, dual operational amplifier



SO8 Exposed Pad

Maturity status link
TSX582

Features

- Supply voltage: 5 V to 16 V
- High output current 200 mA
- Rail-to-rail output, low rail input
- Gain bandwidth product: 3 MHz
- High slew rate: 2 V/µs
- Internal thermal shutdown & output current limiter
- Enhanced RF noise immunity
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to +125 °C
- Automotive-grade
- Low noise 45 nV/√Hz @ 1 kHz
- I_{CC} (typ.) = 2.3 mA
- Unity gain stable
- Low offset 2.4 mV max. (25 °C)/3 mV max. (full temperature range)
- Low input bias current

Applications

- Servo driver
- Valve driver
- DC power supply, AC source
- Portable instrumentation
- Line drivers
- Motor control
- Angle resolver
- LED driver
- Industrial process control

Description

The TSX582 is a unity gain stable, dual operational amplifier with high voltage and high current capability, featuring internal protections against overtemperature and current overload conditions. In addition, the TSX582 has enhanced ESD and RF noise immunity.

It typically outputs up to 200 mA per channel to drive low resistance inductive loads such as angle resolvers, line out cables, and piezo actuators.

The two high current output amplifiers of the TSX582 feature the advantage of driving loads directly in bridge tied mode or connected in parallel, which doubles the output sink/source current. Additionally, the TSX582 is available in a PowerSO-8 package with exposed pad and is qualified for automotive applications in a temperature range of -40 °C to +125 °C.

1 Pin configuration

Figure 1. Pin connections (top view)

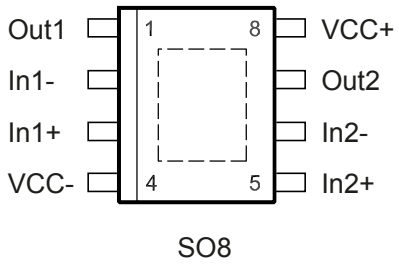


Table 1. Pin description

Pin	Pin name	Description
1	Out1	Output channel 1
2	In1-	Inverting input channel 1
3	In1+	Non-inverting input channel 1
4	V_{CC-}	Negative supply voltage
5	In2+	Non-inverting input channel 2
6	In2-	Inverting input channel 2
7	Out2	Output channel 2
8	V_{CC+}	Positive supply voltage
	ep	Exposed pad (1)

1. *The exposed pad can be left floating or connected to V_{CC-}.*

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbols	Parameters	Value	Unit
V_{CC}	Supply voltage (1)	18	V
V_{id}	Differential input voltage (2)	±18	
V_{in}	Input voltage (3)	V_{CC-} -0.2 V to V_{CC+} +0.2 V	
I_{in}	Input current (4)	±27	mA
V_o	Output voltage (5)	V_{CC-} -0.5 V to V_{CC+} +0.5 V	V
I_o	Output current	See Section 5.7	
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	
R_{th-JA}	Thermal resistance junction-to-ambient (6) (7) SO-8 EP	45	°C/W
ESD	HBM (8)	4	kV
	CDM (9)	1.5	

1. *All voltage values, except the differential voltage, are with respect to the network ground terminal.*
2. *Differential input voltage is the voltage difference between the non-inverting input and inverting input. This voltage may be exceeded by using external resistors, see Section 5.2.*
3. *The input voltage is the voltage that is allowed to be applied to the input terminal independently from the V_{CC} value.*
4. *If the input voltage exceeds the supply voltage or the differential input voltage V_{ID}, the input current must be limited to 27 mA by using a series resistor on the inputs. See Section 5.2.*
5. *The output voltage is the voltage that is allowed to be applied independently from the V_{CC} value.*
6. *R_{th} are typical values for exposed pads soldered onto the circuit board. (JEDEC JESD51).*
7. *Short circuits can cause excessive heating and destructive dissipation.*
8. *According to AECQ101-001.*
9. *According to AECQ101-005.*

Table 3. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	5		16	V
V_{icm}	Common-mode input voltage range	0		V_{CC} -1.5 V	V
T_{oper}	Operating temperature range	-40		+125	°C
Ψ_{JT} (1)	Junction-to-top characterization parameter		5.3		°C/W

1. *Ψ are typical values for exposed pads soldered onto the circuit board. (JEDEC JESD51).*

3 Electrical characteristics

Table 4. Electrical characteristics for V_{CC+} = 12 V, V_{CC-} = 0 V, V_{icm} = V_{out} = V_{CC}/2, and T_{amb} = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-2.4		+2.4	mV
		Tmin < T < Tmax	-3		+3	
		V_{icm} = V_{CC-}	-2.4		+2.4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	Tmin< T < Tmax	-8	-2	+4	µV/°C
I_{ib}	Input bias current				2	nA
		Tmin < T < Tmax			5	
I_{io}	Input offset current				2	
		Tmin < T < Tmax			5	
CMR	Common-mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	$V_{CC-} \le V_{ICM} \le V_{CC+}$ - 1.5 V, V_{out} = V_{CC}/2	75	100		dB
		Tmin < T < Tmax	70			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	5 V < V_{CC+} -V_{CC-} < 16 V, -40 °C < T < +125 °C	116	130		
Avd	Open loop gain	R_L = 10 kΩ, V_{out} = 0.3 to 11.7 V	110	125		
		Tmin < T < Tmax	101			
		R_L = 600 Ω, V_{out} = 1 to 11 V	110	125		
		Tmin < T < Tmax	101			
V_{oh}	High level output voltage Voltage drop from V_{CC+}	I_{source} = 150 mA		1.2	1.8	V
		Tmin < T < Tmax			2	
V_{ol}	Low level output voltage	I_{sink} = 150 mA		1.2	1.8	
		Tmin < T < Tmax			2.2	
I_{cc}	Supply current (per channel)	No load, V_{out} = V_{CC}/2		2.3	3	mA
		Tmin < T < Tmax			3.4	
I_{OUT} (1)	Isink	V_{out} = V_{CC}	160			
		Tmin < T < Tmax	150			
	Isource	V_{out} = 0 V	160			
		Tmin < T < Tmax	150			
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		3		MHz
ϕ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		17		dB
SR	Negative slew rate	Comparator mode, 10% to 90% R_L = 10 kΩ, C_L = 100 pF		1.9		V/µs
	Positive slew rate	Comparator mode, 10% to 90% R_L = 10 kΩ, C_L = 100 pF		1.9		
e_n	Equivalent input noise voltage	f = 1 kHz		45		nV/√Hz
		f = 0.1 Hz to 10 Hz		300		µVpp

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	f = 1 kHz, V_{in} = 2 Vpp, R_L = 10 kΩ, C_L = 100 pF		0.005		%
	Overload recovery time	100 mV from rail in comparator mode V_{id} = ±1 V		10		µs
Shutdown						
	Junction temperature	Shutdown		168	180	°C
		Reset from shutdown	130	146		

1. *While respecting the maximum junction temperature.*

Table 5. Electrical characteristics for V_{CC+} = 5 V, V_{CC-} = 0 V, V_{icm} = V_{out} = V_{CC}/2, and T_{amb} = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-2.4		+2.4	mV
		Tmin < T < Tmax	-3		+3	
		V_{icm} = V_{CC-}	-2.4		+2.4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	Tmin< T < Tmax	-8	-2	4	µV/°C
I_{ib}	Input bias current				2	nA
		Tmin < T < Tmax			5	
I_{io}	Input offset current				2	
		Tmin < T < Tmax			5	
CMR	Common-mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	$V_{CC-} \le V_{ICM} \le V_{CC+}$ - 1.5 V, V_{out} = V_{CC}/2	65	90		dB
		Tmin < T < Tmax	60			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	5 V < V_{CC+} - V_{CC-} < 16 V, -40 °C < T < +125 °C	116	130		
A_{VD}	Open loop gain	R_L = 10 kΩ, V_{out} = 0.3 to 4.7 V	100	120		
		Tmin < T < Tmax	98			
		R_L = 600 Ω, V_{out} = 1 to 4 V	100	115		
		Tmin < T < Tmax	98			
V_{oh}	High level output voltage. Voltage drop from V_{CC+}	I_{source} = 150 mA		1.2	1.8	V
		Tmin < T < Tmax			2	
V_{ol}	Low level output voltage	I_{sink} = 150 mA		1.2	1.8	
		Tmin < T < Tmax			2.2	
I_{CC}	Supply current (per channel)	No load, V_{out} = V_{CC}/2		2.3	3	mA
		Tmin < T < Tmax			3.4	
I_{OUT} (1)	Isink	V_{out} = V_{CC}	160			
		Tmin < T < Tmax	150			
	Isource	V_{out} = 0 V	160			
		Tmin < T < Tmax	150			
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		2.7		MHz
ϕ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		17		dB
SR	Negative slew rate	Comparator mode, 10% to 90% R_L = 10 kΩ, C_L = 100 pF		1.7		V/µs
	Positive slew rate	Comparator mode, 10% to 90% R_L = 10 kΩ, C_L = 100 pF		1.7		
e_n	Equivalent input noise voltage	f = 1 kHz		45		nV/√Hz
		f = 0.1 Hz to 10 Hz		300		µVpp
THD+N	Total harmonic distortion + noise	f = 1 kHz, V_{in} = 2 Vpp, R_L = 10 kΩ, C_L = 100 pF		0.007		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Overload recovery time	100 mV from rail in comparator mode V_{id} = ±1 V		10		µs
Shutdown						
	Junction temperature	Shutdown		168	180	°C
		Reset from shutdown	130	146		

1. *While respecting the maximum junction temperature.*

4 Typical performance characteristics

R_L connected to $V_{CC}/2$ (unless otherwise specified).

Figure 2. Supply current vs. supply voltage (per channel)

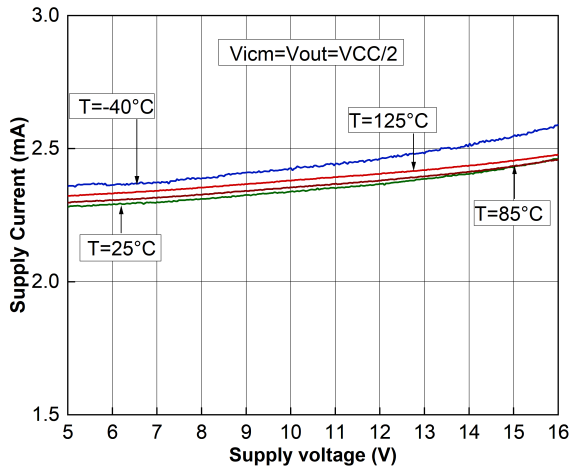


Figure 3. Supply current vs. input common-mode voltage per channel (V_{CC} = 16 V)

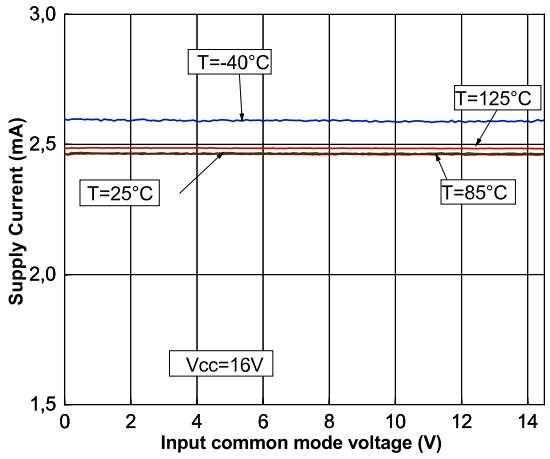


Figure 4. Input offset voltage distribution, T = 25 °C, V_{CC} = 12 V

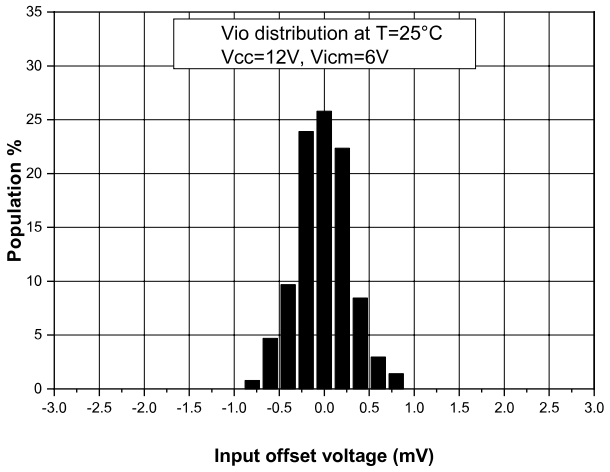


Figure 5. Input offset voltage temperature coefficient distribution from -40 °C to +25 °C (µV/°C), V_{CC} = 12 V

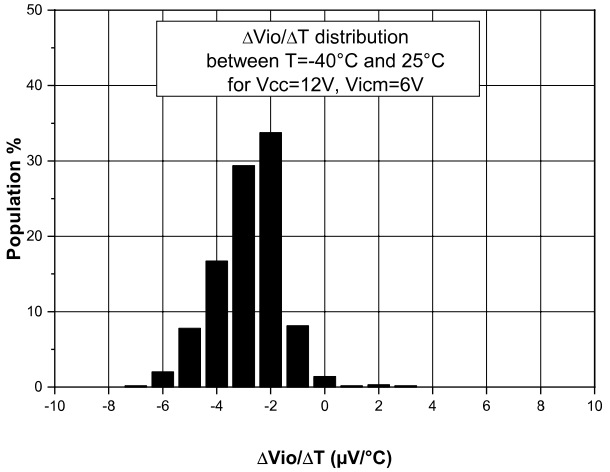


Figure 6. Input offset voltage temperature coefficient distribution from 25 °C to 125 °C (µV/°C), V_{CC} = 12 V

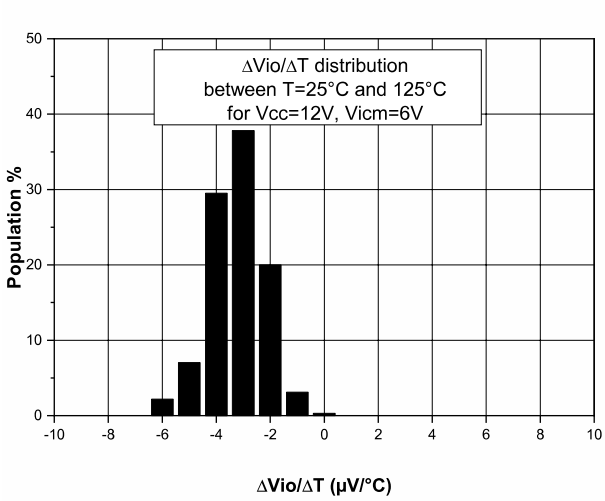


Figure 7. Input offset voltage vs. supply voltage

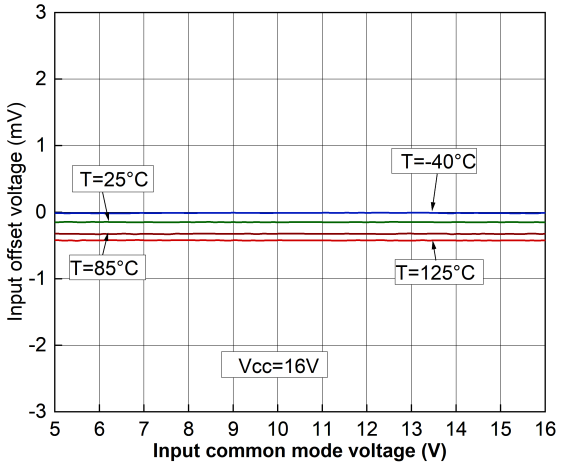


Figure 8. Input offset voltage vs. input common-mode voltage V_{CC} = 16 V

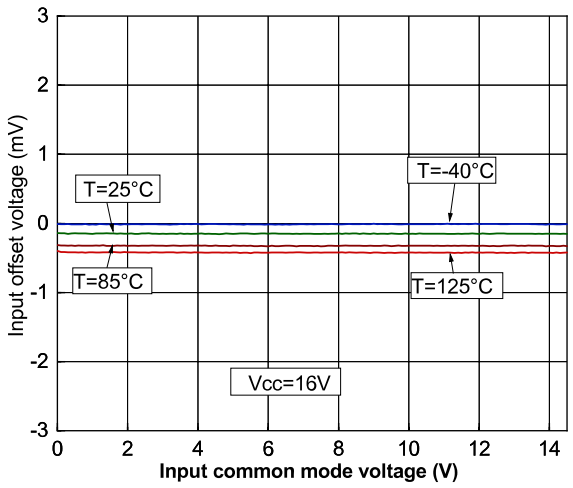


Figure 9. Input bias current vs. temperature at mid V_{ICM}

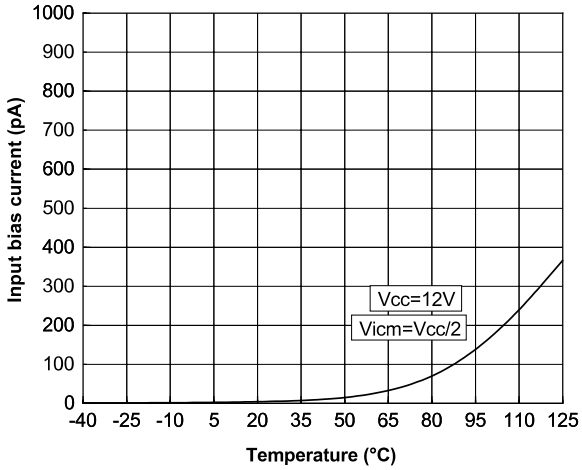


Figure 10. Output voltage drop vs. output current load, V_{CC} = 12 V, V_{icm} = V_{CC}/2, V_{id} = -1 V for sink, +1 V for source

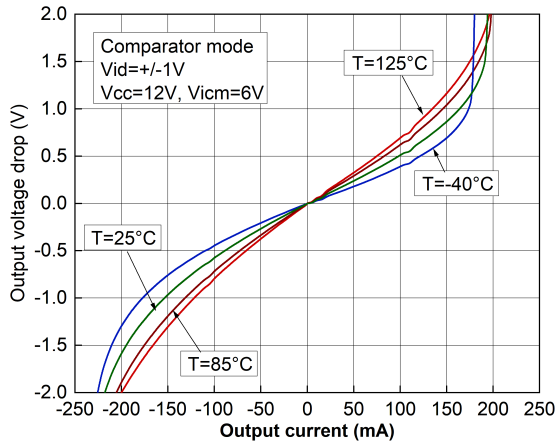


Figure 11. High-level output voltage (drop from V_{CC+}) vs. V_{CC}, I_{load} = 160 mA

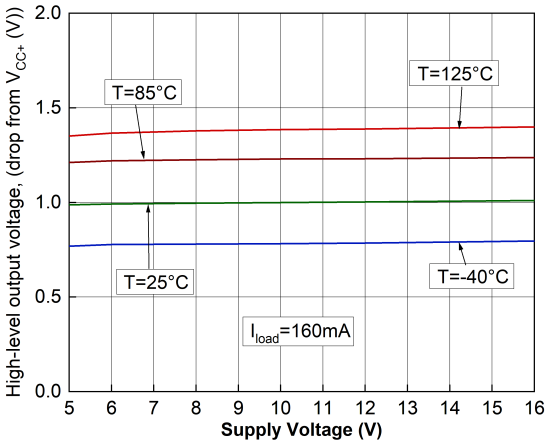


Figure 12. High-level output voltage, (drop from V_{CC+}) vs. temperature, I_{load} = 160 mA

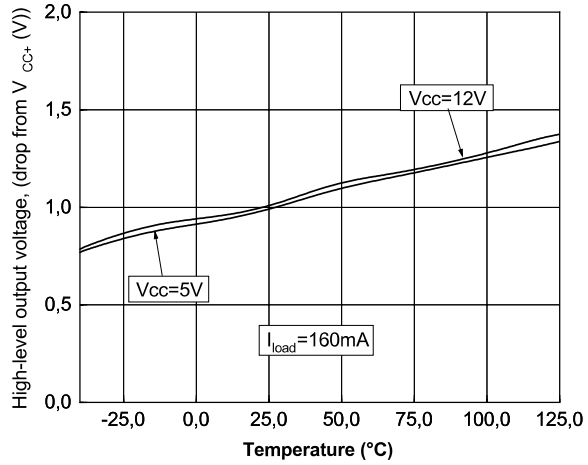


Figure 13. Low-level output voltage vs. V_{CC}, I_{load} = 160 mA

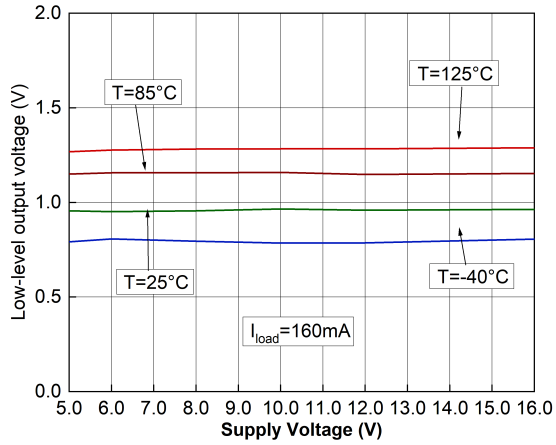


Figure 14. Low-level output voltage vs. temperature, I_{load} = 160 mA

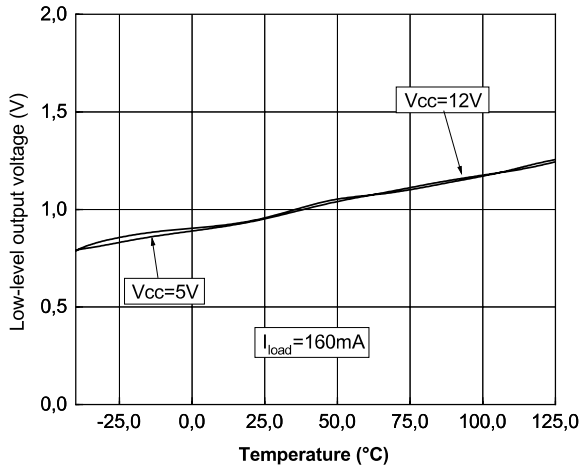


Figure 15. Slew rate vs. V_{CC}, R_{load} = 10 kΩ, C_{load} = 100 pF, comparator mode, V_{diff} = 5 V

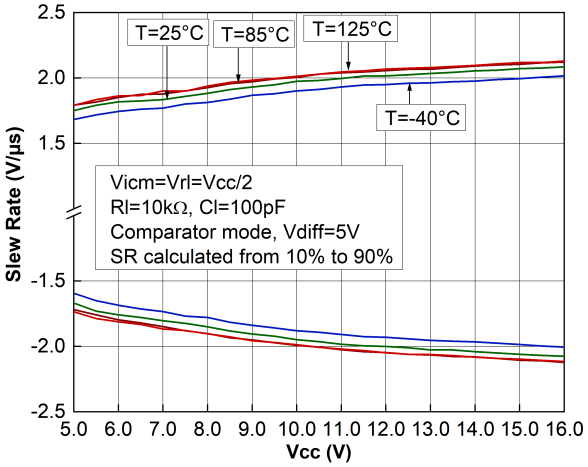


Figure 16. Small signal response at 16 V supply voltage

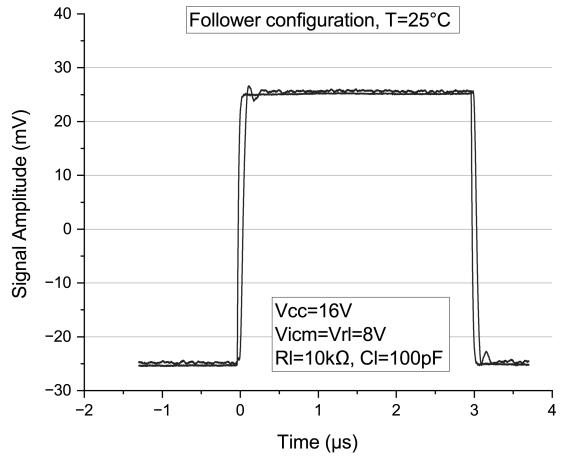


Figure 17. Bode diagram, V_{CC} = 16 V, R_l = 10 kΩ, C_{load} = 100 pF, common-mode voltage = 8 V

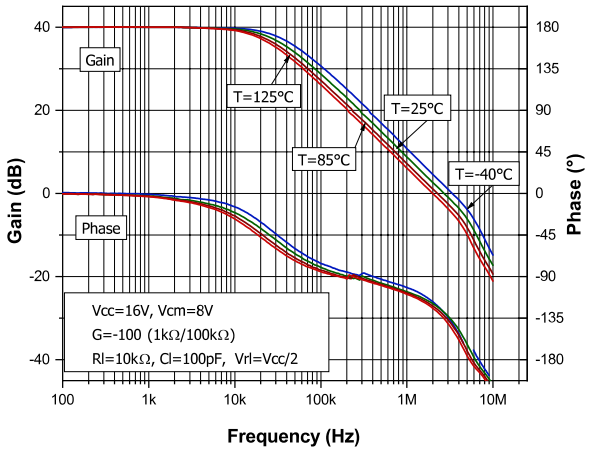


Figure 18. Unity gain frequency vs. temperature, V_{CC} = 16 V, R_l = 10 kΩ

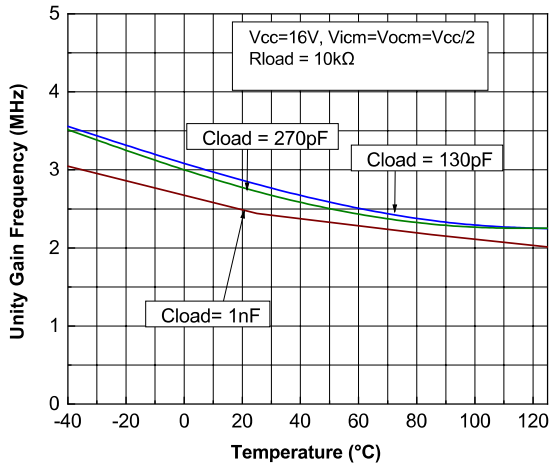


Figure 19. Phase margin vs. capacitive load V_{CC} = 16 V, R_l = 10 kΩ

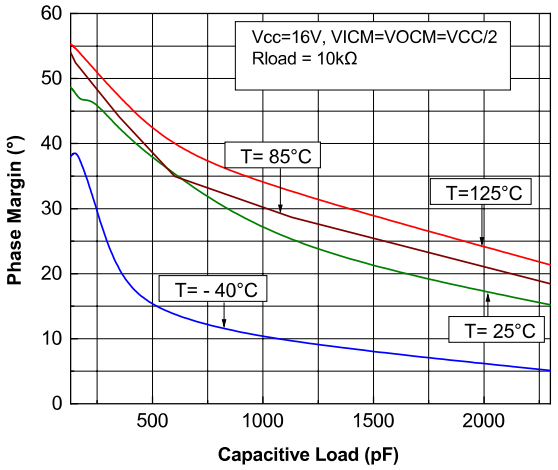


Figure 20. Gain margin vs. capacitive load V_{CC} = 16 V, R_l = 10 kΩ

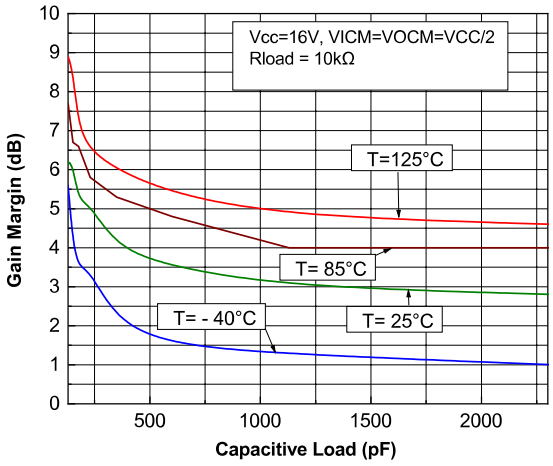


Figure 21. Overshoot vs. capacitive load

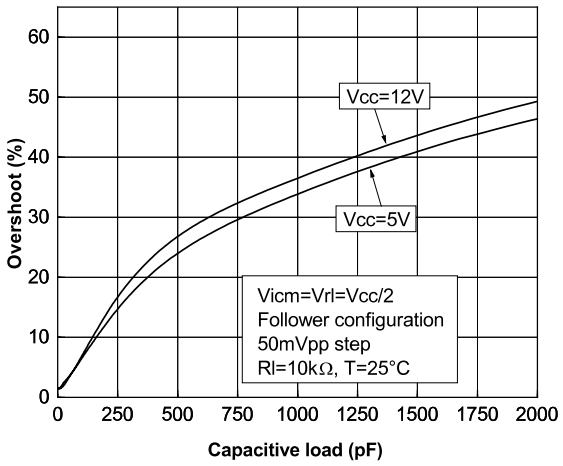


Figure 22. Noise vs. frequency for different supply voltages

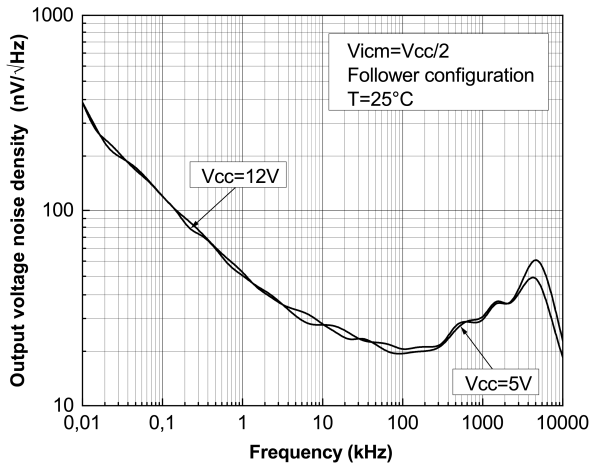


Figure 23. THD vs. output voltage swing for different frequencies, V_{CC} = 16 V, R_l = 10 kΩ, C_l = 100 pF

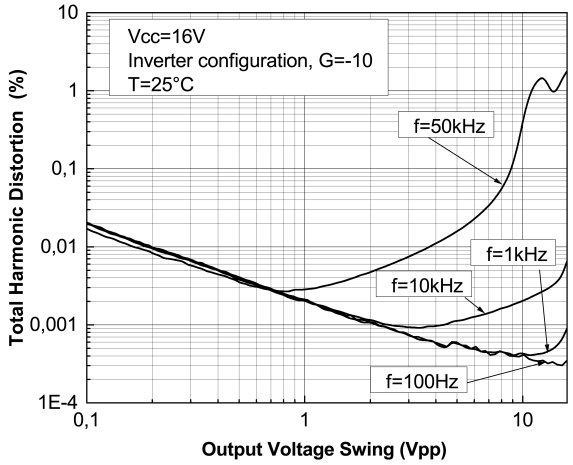


Figure 24. THD vs. frequency for different V_{cm}, V_{CC} = 16 V, V_{icm} = V_{ocm} = V_{cm}, R_l = 10 kΩ, C_l = 100 pF

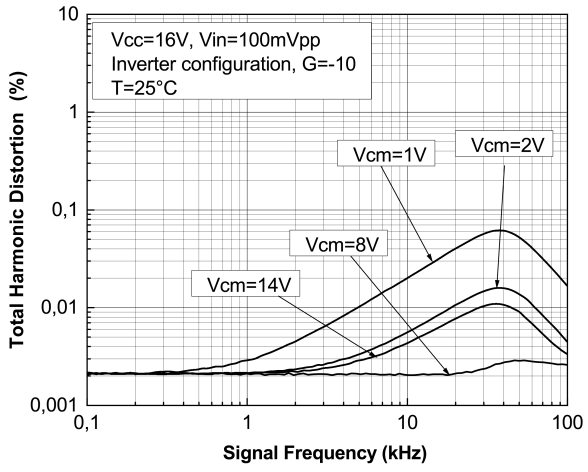


Figure 25. PSRR vs. frequency

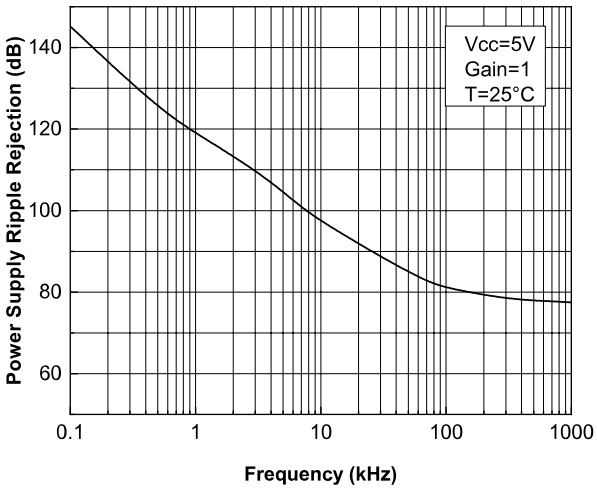
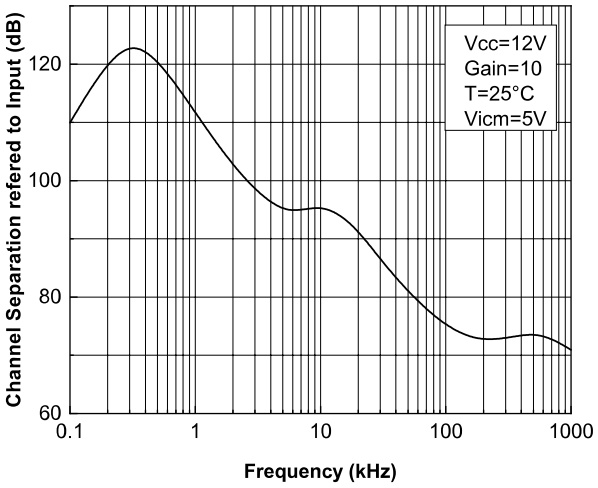


Figure 26. **Channel separation vs. frequency**



5 Application information

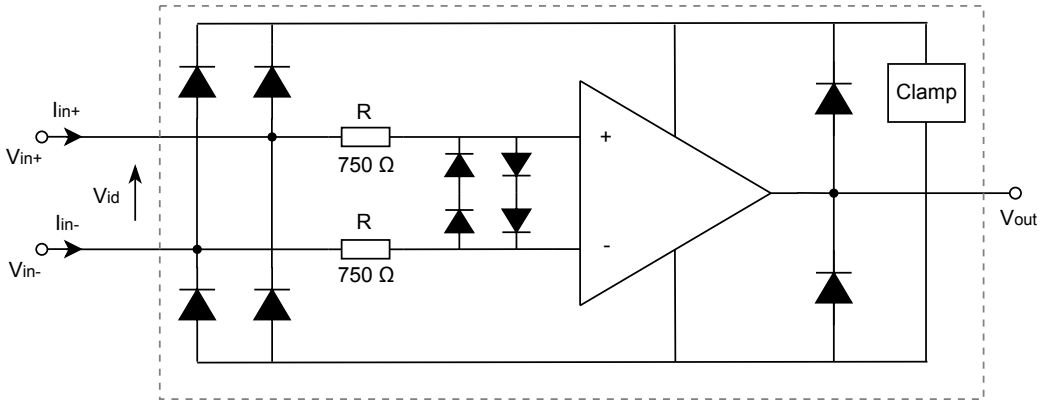
5.1 Operating voltages

The TSX582 can operate from 5 to 16 V. The parameters are fully specified at 5 V and 12 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSX582 device characteristics over the full operating range. Additionally, the main specifications are guaranteed in an extended temperature range from -40 to +125 °C.

5.2 ESD and input protection

Figure 27 illustrates an equivalent circuit of the TSX582's protection against ESD events and high differential input voltages. The TSX582 is designed for input common mode voltages ranging from the low rail up to V_{CC} – 1.5 V with input currents Iin that must not exceed 27 mA. Input resistors in combination with a voltage limitation prevent excessive differential voltages from damaging the differential input stage of the operational amplifier. However, note that differential input voltages of more than V_{id} = 1.3 V (typical) cause a non-negligible current flow through the input protection stage that might be considered when calculating the thermal budget of the amplifier. A high input current in comparator mode might also impact the input signal at application level. In case the differential input voltage of the application should exceed the absolute maximum rating of V_{id} = ± 18 V, it is recommended to add external resistors to the design to keep the maximum current below I_{in} = 27 mA.

Figure 27. Equivalent internal ESD and input protection circuit



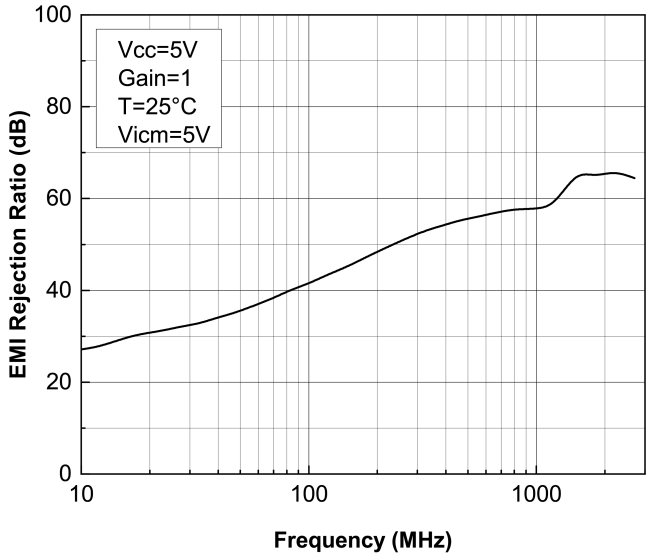
5.3 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined as follows:

$$EMIRR = 20.\log\left(\frac{V_{inpp}}{\Delta V_{io}}\right) \quad (1)$$

The TSX582 has been specially designed to minimize susceptibility to the EMIRR and shows a low sensitivity. As visible in the figure below, the EMI rejection ratio has been measured on both inputs and outputs, from 10 MHz to 2.4 GHz.

Figure 28. **EMI rejection ratio vs. frequency**



EMIRR performance might be improved by adding small capacitances (in the pF range) on the inputs, power supply, and output pins. These capacitances help in minimizing the impedance of these nodes at high frequencies.

5.4 Input offset voltage drift over the temperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{io}) is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using the equation:

$$\frac{\Delta V_{IO}}{\Delta T} = \max \left| \frac{V_{IO}(T) - V_{IO}(25°C)}{T - 25°C} \right|_{T = \ -40°C \ and \ T = \ 125°C} \quad (2)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.5 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSX582 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times Rth_{JA} + T_A \quad (3)$$

T_J is the die junction temperature.

P_D is the power dissipated in the package.

$R_{th\text{-}JA}$ is the junction to ambient thermal resistance of the package.

T_A is the ambient temperature.

The power dissipated in the package P_D is the sum of three main sources of both amplifier channels. The quiescent power, the power dissipated by the output stage transistor, and the input protection circuit in the case that the differential input voltage is forced to $|V_{id}| > 1.3$ V (see Section 5.2 ESD and input protection). It is calculated as follows.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_d = P_{d\_amp1} + P_{d\_amp2} \quad (4)$$

$$P_{d\_amp} = V_{CC} \times I_{CC} + (V_{CC+} - V_{out}) \times I_{load} + \left[\frac{(|V_{id}| - 1.3V) \times |V_{id}|}{1.5\ k\Omega}\right]_{if |V_{id}| > 1.3\ V} \quad (5)$$

when the op amp sources the current.

$$P_{d\_amp} = V_{CC} \times I_{CC} + (V_{out} - V_{CC-}) \times I_{load} + \left[\frac{(|V_{id}| - 1.3V) \times |V_{id}|}{1.5\ k\Omega}\right]_{if |V_{id}| > 1.3\ V} \quad (6)$$

when the op amp sinks the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.6 Thermal shutdown considerations

To guarantee proper operation, precautions must be taken to keep the device die temperature below the maximum junction temperature. This is achieved by computing the dissipated power in the device and using a large enough copper area or heatsink on the PCB to reduce the thermal resistance between the device and the ambient temperature.

To protect the device, a thermal shutdown mechanism is implemented:

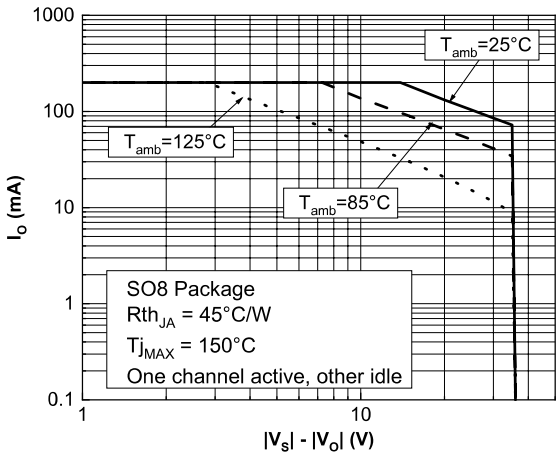
- A thermal sensor continuously measures the average die temperature.
- If the temperature goes above a high threshold, the output power stage is turned OFF to allow the device to cool down.
- When the temperature goes back below a low threshold, the output power stage is turned ON again.

This safety behavior prevents the die from reaching a destructive temperature. Nevertheless, the device is not intended to continuously operate in such a condition. The user should consider the maximum dissipated power and maximum temperature when designing the application. The maximum die temperature should be kept below the thermal shutdown temperature threshold. When safe operating conditions cannot be guaranteed, external protection such as PTC or fuses should be used.

5.7 Safe operating area

Figure 29 shows the typical safe operating area (SOA) of the TSX582, where one amplifier is in load condition whereas the second one stays in idle mode without the load. Depending on the intended application, the total power dissipation might be split over the two amplifiers. In the case that both amplifiers are used simultaneously, or the differential input voltage is forced to continuously exceed $|V_{id}|$ = 1.3 V, a calculation of the junction temperature based on the total power dissipation is recommended, as demonstrated in Section 5.5: Maximum power dissipation.

Figure 29. SO-8 safe operating area, one channel active



5.8 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 100 pF. Increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response. Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity gain configuration, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 30 Ω) in series with the output. This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error on the output, and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO}/R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point of view as described in the following figure.

Figure 30. Stability criteria with a serial resistor at different capacitive loads

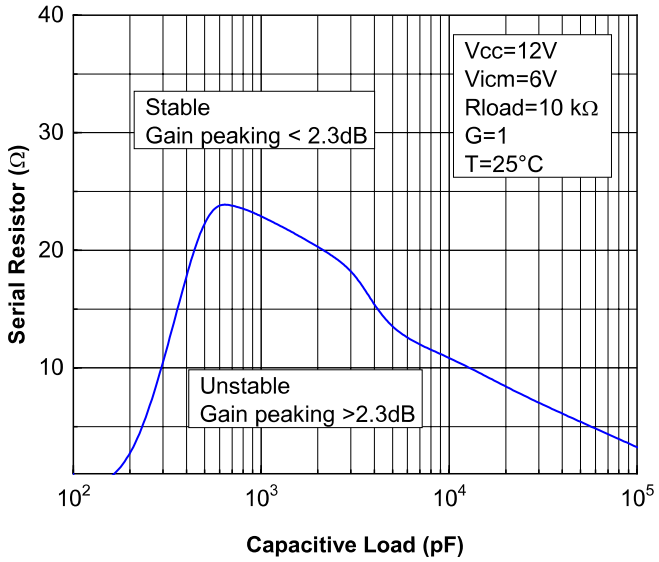
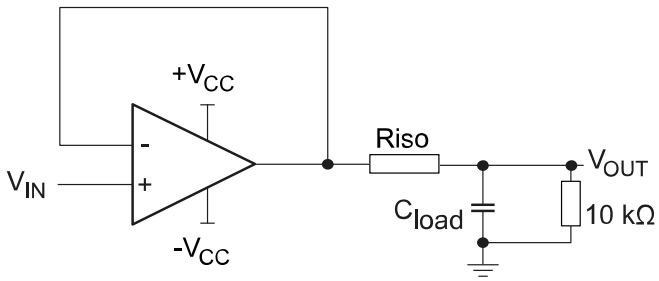


Figure 31. Test configuration for R_{ISO}



Note that R_{ISO} = 30 Ω is sufficient to make the TSX582 stable whatever the capacitive load. However, for high output currents, voltage drops across R_{ISO} should be considered.

5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces connecting the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

6 Typical applications

6.1 Rotary resolver

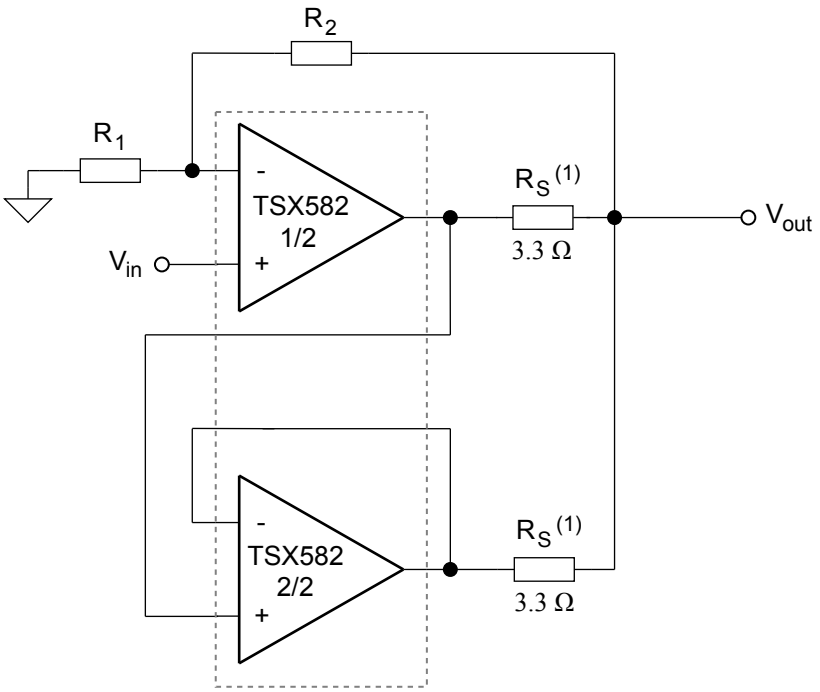
In closed-loop motor control systems, the preferred way to read out the shaft's angular position is the rotary resolver. It essentially consists of one primary reference winding plus two secondary windings, the sin- and cos winding in the stator. Since the primary winding is typically powered through a rotary transformer, no brushes or rings are needed. This increases the overall reliability and robustness of the resolver and makes it perfectly suitable for harsh environments with varying temperatures and in oily, dusty, or humid surroundings.

Closed-loop motor control systems help to navigate factory robots and to maneuver vehicles in autonomous parking mode. The TSX582 manages the power amplification to pilot the primary winding of a resolver device.

6.2 Increasing output current

To increase the output currents up to 400 mA, the two operational amplifiers can be tied in parallel, as shown in Figure 32. The output resistors R_S prevent differential current flow between the output stages of the two operational amplifiers due to deviations in V_{io}. Care must be taken when selecting R_S, since they introduce a non-negligible voltage drop to the design at high currents.

Figure 32. Increasing output current



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO-8 exposed pad package information

Figure 33. **SO-8 exposed pad package outline**

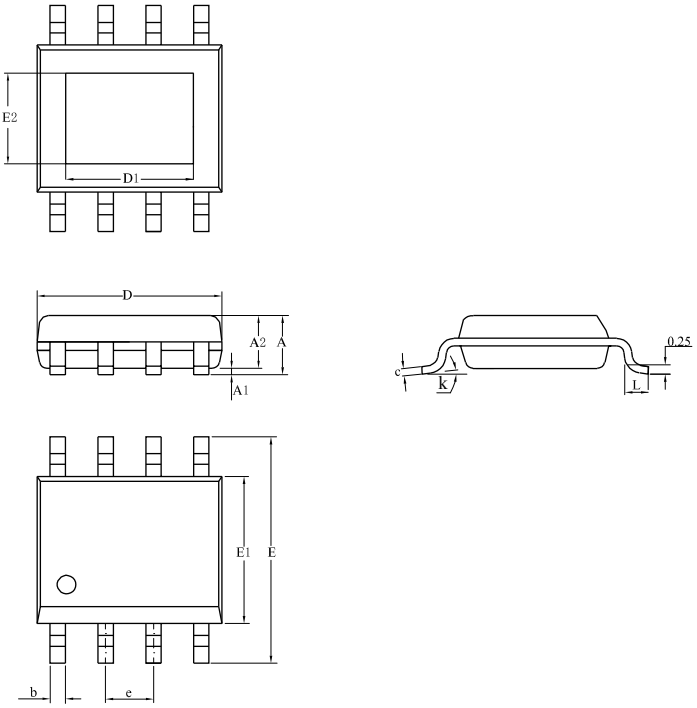
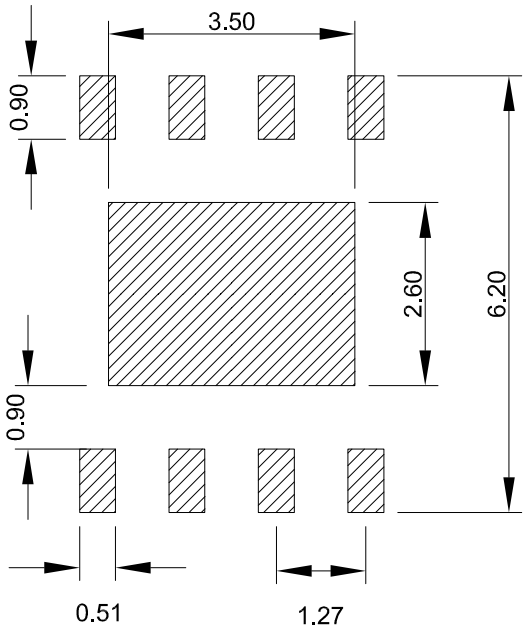


Table 6. **SO-8 exposed pad mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.70
A1	0.00		0.15
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D (1)	4.80	4.90	5.00
D1		2.09	
E	5.80	6.00	6.20
E1 (2)	3.80	3.90	4.00
E2		2.09	
e		1.27	
L	0.40		1.27
k	0°		8°

1. *Dimension “D” does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm in total (both sides).*
2. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Figure 34. **SO-8 exposed pad footprint data**



7.2 SO-8 packing information

Figure 35. **SO-8 drawing of carrier tape**

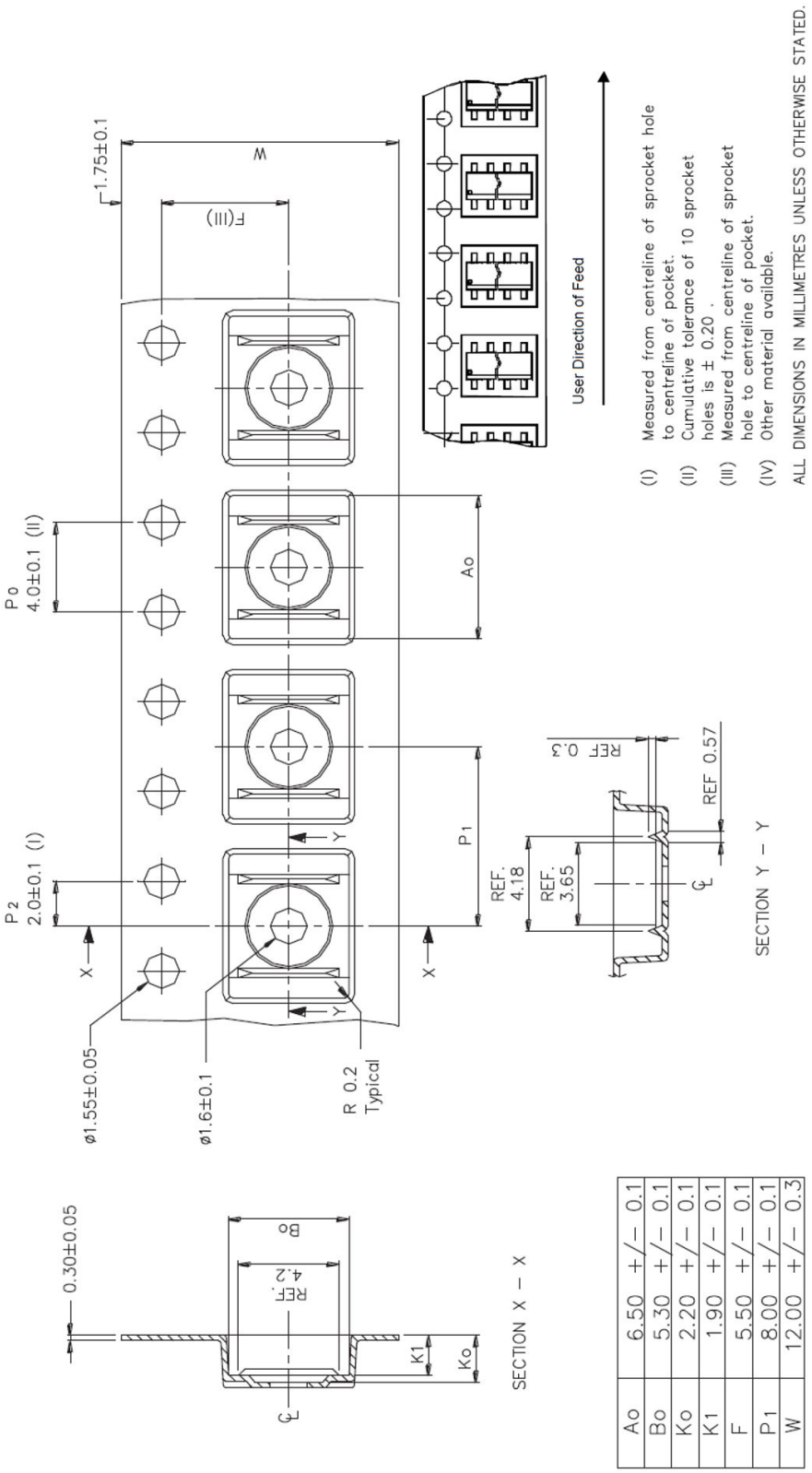


Figure 36. **SO-8 overall reel dimension**

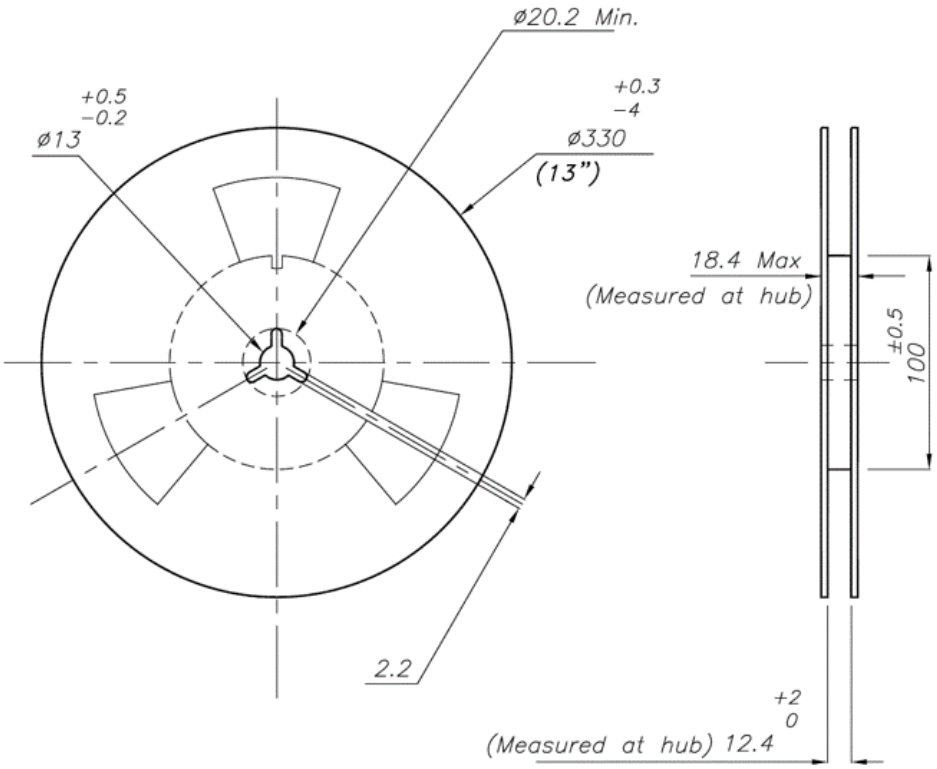
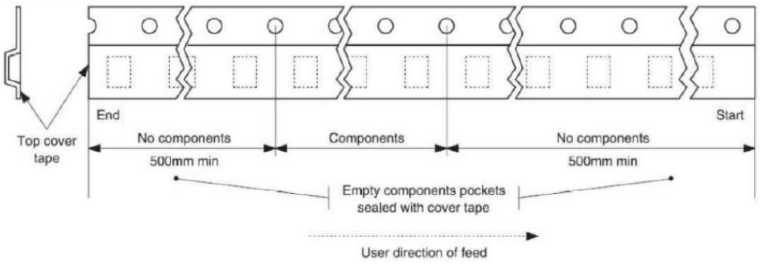


Figure 37. **SO-8 carrier tape leader and trailer**



8 Ordering information

Table 7. Order code

Order code	Temperature range	Package	Packing	Marking
TSX582IYDT (1)	-40 °C to +125 °C	SO-8 exposed pad	Tape and reel	K2D

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or the equivalent.*

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
01-Mar-2024	1	Initial release.

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