Very high accuracy (7 µV) high bandwidth (1.6 MHz) zero-drift 5 V op amp

TSZ151
SOT23-5

TSZ151
SC70-5

TSZ152
DFN8

TSZ152
MiniSO8

TSZ152
SO8

Features

- Very high accuracy and stability: offset voltage
  - 7 µV max. at 25 °C
  - 10 µV over full temperature range (-40 °C to 125 °C)
- Rail-to-rail input and output
- Low supply voltage: from 1.8 to 5.5 V
- Low power consumption: 210 µA at 5 V
- Gain bandwidth product: 1.6 MHz
- Extended temperature range: -40 to 125 °C
- AEC-Q100 qualified
- Benefits:
  - Higher accuracy without calibration
  - Accuracy is virtually unaffected by temperature change

Applications

- High accuracy signal conditioning
- Automotive current measurement and sensors signal conditioning

Description

The TSZ151 and TSZ152 are single and dual operational amplifier featuring very low offset voltages with virtually zero-drift versus temperature changes.

The TSZ151 and TSZ152 are single and dual offers rail-to-rail input and output, an excellent speed/power consumption ratio, and 1.6 MHz gain bandwidth product, while consuming just 210 µA at 5 V.

The device also features an ultra-low input bias current. These features make the TSZ151 and TSZ152 are ideal for high-accuracy sensor interfaces.

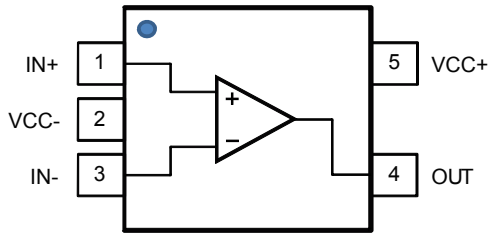
Product status link	Channel	Automotive	Package
TSZ151ICT	1		SC70-5
TSZ151IYCT	1	•	SC70-5
TSZ151ILT	1		SOT23-5
TSZ151IYLT	1	•	SOT23-5
TSZ152IDT	2		SO8
TSZ152IYDT	2	•	SO8
TSZ152IST	2		MiniSO8
TSZ152IYST	2	•	MiniSO8
TSZ152IQT	2		DFN8
TSZ152IYQT	2	•	DFN8

Related products	
TSZ121 TSZ122	Zero drift amplifier for more power savings (400 kHz, 31 µA)
TSZ181 TSZ182	Zero drift amplifier for higher bandwidth (3 MHz, 800 µA)

1 Pin description

1.1 TSZ151 single operational amplifier (SC70-5)

Figure 1. Pin connection (top view)



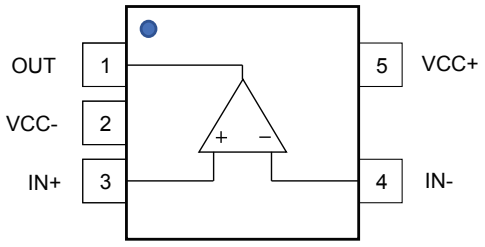
SC70-5

Table 1. Pin description

Pin n°	Pin name	Description
1	IN+	Non-inverting input channel
2	VCC-	Negative supply voltage
3	IN-	Inverting input channel
4	OUT	Output channel
5	VCC+	Positive supply voltage

1.2 TSZ151 single operational amplifier (SOT23-5)

Figure 2. Pin connection (top view)



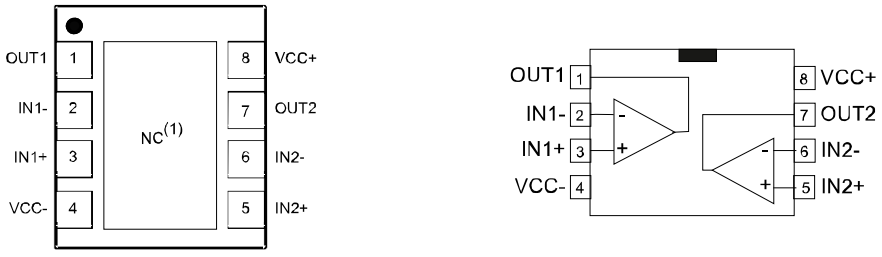
SOT23-5

Table 2. Pin description

Pin n°	Pin name	Description
1	OUT	Output channel
2	VCC-	Negative supply voltage
3	IN+	Non-inverting input channel
4	IN-	Inverting input channel
5	VCC+	Positive supply voltage

1.3 TSZ152 dual operational amplifier

Figure 3. Pin connections (top view)



DFN8 2x2 (TSZ152)

MiniSO8 and SO8 (TSZ152)

1. The exposed pad of the DFN8 2x2 can be connected to V_{CC-} or left floating.

Table 3. Pin description

Pin n°	Pin name	Description
1	OUT1	Output channel
2	IN1-	Inverting input channel
3	IN1+	Non-inverting input channel
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel
6	IN2-	Inverting input channel
7	OUT2	Output channel
8	VCC+	Positive supply voltage

2 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter [1]		Value	Unit
V_{CC}	Supply voltage		6	V
V_{id}	Differential input voltage (V_{IN+} - V_{IN-})		$\pm V_{CC}$	
V_{in}	Input voltage [2]		(V_{CC-}) -0.2 to (V_{CC+}) +0.2	
I_{in}	Input current		±10	mA
T_{stg}	Storage temperature		-65 to +150	°C
T_j	Maximum junction temperature		150	
R_{th-ja}	Thermal resistance junction-to-ambient [3]	SC70-5	205	°C/W
		SOT23-5	250	
		SO8	113	
		MiniSO8	127	
		DFN8 2x2	76	
ESD	HBM: human body model (industrial grade) [4]		4000	V
	HBM: human body model (automotive grade) [5]		4000	
	CDM: charged device model		1000	

1. *All voltage values are with respect to the VCC- pin, unless otherwise specified.*
2. *The maximum input voltage value may be extended on the condition that the input current is limited to ±10 mA.*
3. *R_{th-ja} is a typical value, obtained with PCB according to JEDEC 2s2p without vias.*
4. *Human body model: HBM test according to the standard ESDA-JS-001-2017.*
5. *Human body model: HBM test according to the standard AEC-Q100-002.*

Table 5. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 5.5	V
V_{icm}	Common-mode input voltage range	(V_{CC-}) -0.1 V to (V_{CC+}) +0.1	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 6. Electrical characteristics at V_{CC} = 5 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C (unless otherwise specified), R_L and C_L (if any specified) connected to V_{CC} / 2.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	±7	µV
		-40 °C ≤ T ≤ 125 °C			±10	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C	-15		35	nV/°C
I_{ib}	Input bias current	T = 25 °C		50	200	pA
		-40 °C ≤ T ≤ 125 °C			300	
I_{io}	Input offset current	T = 25 °C		100	400	pA
		-40 °C ≤ T ≤ 125 °C			600	
A_{VD}	Open loop gain	V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, T = 25 °C	120	135		dB
		V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C	115			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	120	132		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	115			
SVR	Supply-voltage rejection ratio 20.log ($\Delta V_{io}/\Delta V_{CC}$)	1.8 V ≤ V_{CC} ≤ 5.5 V, V_{icm} = 0 V, T = 25 °C	120	140		dB
		1.8 V ≤ V_{CC} ≤ 5.5 V, V_{icm} = 0 V, -40 °C ≤ T ≤ 125 °C	120			
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	R_L = 10 kΩ, T = 25 °C			30	mV
		R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C			70	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	R_L = 10 kΩ, T = 25 °C			30	mV
		R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C			70	
I_{OUT}	I_{SINK}, OUT connected to V_{CC+}	V_{ID} = -0.1 V, T = 25 °C	20	30		mA
		V_{ID} = -0.1 V, -40 °C ≤ T ≤ 125 °C	15			
	I_{SOURCE}, OUT connected to V_{CC-}	V_{ID} = +0.1 V, T = 25 °C	20	30		
		V_{ID} = +0.1 V, -40 °C ≤ T ≤ 125 °C	15			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		210	300	µA
		-40 °C ≤ T ≤ 125 °C			300	
AC performance						
GBP	Gain bandwidth product	C_L = 100 pF		1.6		MHz
SR	Slew rate (2) measured from 10% to 90%	A_V = 1 V/V, V_{in} = 0.3 V to V_{CC+} -0.3 V, R_L = 10 kΩ, C_L = 100 pF		0.8		V/µs
Φm	Phase margin	C_L = 100 pF		60		degrees
en	Input voltage noise density	f = 1 kHz		27		nV/√Hz
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.5		μV_{pp}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	V_{in} from (V_{CC+} +100 mV) to (V_{CC+} -1 V) , V_{OUT} measured at (V_{CC+} -100 mV), A_V = +1		5		µs
t_{init}	Initialization time, V_{OUT} at 100 mV from final value	T = 25 °C		80		µs
EMIRR	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mVpp, f = 400 MHz		84		dB
		V_{RF} = 100 mVpp, f = 900 MHz		87		
		V_{RF} = 100 mVpp, f = 1800 MHz		90		
		V_{RF} = 100 mVpp, f = 2400 MHz		91		

Table 7. Electrical characteristics at V_{CC} = 3.3 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C (unless otherwise specified), R_L and C_L (if any specified) connected to V_{CC} / 2.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	±7	µV
		-40 °C ≤ T ≤ 125 °C			±10	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C	-18		38	nV/°C
I_{ib}	Input bias current	T = 25 °C		50	200	pA
		-40 °C ≤ T ≤ 125 °C			300	
I_{io}	Input offset current	T = 25 °C		100	400	pA
		-40 °C ≤ T ≤ 125 °C			600	
A_{VD}	Open loop gain	V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, T = 25 °C	116	131		dB
		V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C	111			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	116	128		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	111			
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	R_L = 10 kΩ, T = 25 °C			25	mV
		R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C			60	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			25	mV
		-40 °C ≤ T ≤ 125 °C			60	
I_{OUT}	I_{SINK}, OUT connected to V_{CC+}	V_{ID} = -0.1 V, T = 25 °C	14	21		mA
		V_{ID} = -0.1 V, -40 °C ≤ T ≤ 125 °C	10			
	I_{SOURCE}, OUT connected to V_{CC-}	V_{ID} = +0.1 V, T = 25 °C	14	21		
		V_{ID} = +0.1 V, -40 °C ≤ T ≤ 125 °C	10			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		210	300	µA
		-40 °C ≤ T ≤ 125 °C			300	
AC performance						
GBP	Gain bandwidth product	C_L = 100 pF		1.6		MHz
SR	Slew rate (2) measured from 10% to 90%	A_V = 1 V/V, V_{in} = 0.3 V to V_{CC+} -0.3 V, R_L = 10 kΩ, C_L = 100 pF		0.8		V/µs
Φm	Phase margin	C_L = 100 pF		60		degrees
en	Input voltage noise density	f = 1 kHz		28		nV/√Hz
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.5		μV_{pp}
t_{rec}	Overload recovery time	V_{in} from (V_{CC+} +100 mV) to (V_{CC+} -1 V) , V_{OUT} measured at (V_{CC+} -100 mV), A_V = +1		3		µs
t_{init}	Initialization time, V_{OUT} at 100 mV from final value	T = 25 °C		70		µs
EMIRR	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mVpp, f = 400 MHz		84		dB
		V_{RF} = 100 mVpp, f = 900 MHz		87		
		V_{RF} = 100 mVpp, f = 1800 MHz		90		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EMIRR	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mVpp, f = 2400 MHz		91		dB

Table 8. Electrical characteristics at V_{CC} = 1.8 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C (unless otherwise specified), R_L and C_L (if any specified) connected to V_{CC} / 2.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	±7	µV
		-40 °C ≤ T ≤ 125 °C			±10	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C	-38		43	nV/°C
I_{ib}	Input bias current	T = 25 °C		50	200	pA
		-40 °C ≤ T ≤ 125 °C			300	
I_{io}	Input offset current	T = 25 °C		100	400	pA
		-40 °C ≤ T ≤ 125 °C			600	
A_{VD}	Open loop gain	V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, T = 25 °C	110	125		dB
		V_{CC-}+200 mV ≤ V_{OUT} ≤ V_{CC+}-200 mV, R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C	105			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	110	122		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	105			
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	R_L = 10 kΩ, T = 25 °C			20	mV
		R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C			50	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	R_L = 10 kΩ, T = 25 °C			20	mV
		R_L = 10 kΩ, -40 °C ≤ T ≤ 125 °C			50	
I_{OUT}	I_{SINK}, OUT connected to V_{CC+}	V_{ID} = -0.1 V, T = 25 °C	7	11		mA
		V_{ID} = -0.1 V, -40 °C ≤ T ≤ 125 °C	5			
	I_{SOURCE}, OUT connected to V_{CC-}	V_{ID} = +0.1 V, T = 25 °C	7	11		
		V_{ID} = +0.1 V, -40 °C ≤ T ≤ 125 °C	5			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		210	300	µA
		-40 °C ≤ T ≤ 125 °C			300	
AC performance						
GBP	Gain bandwidth product	C_L = 100 pF		1.6		MHz
SR	Slew rate (2) measured from 10% to 90%	A_V = 1 V/V, V_{in} = 0.3 V to V_{CC+} -0.3 V, R_L = 10 kΩ, C_L = 100 pF		0.8		V/µs
Φm	Phase margin	C_L = 100 pF		60		degrees
en	Input voltage noise density	f = 1 kHz		33		nV/√Hz
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.57		μV_{pp}
t_{rec}	Overload recovery time	V_{in} from (V_{CC+} +100 mV) to (V_{CC+} -1 V) , V_{OUT} measured at (V_{CC+} -100 mV), A_V = +1		2		µs
t_{init}	Initialization time, V_{OUT} at 100 mV from final value	T = 25 °C		60		µs
EMIRR	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mVpp, f = 400 MHz		84		dB
		V_{RF} = 100 mVpp, f = 900 MHz		87		
		V_{RF} = 100 mVpp, f = 1800 MHz		90		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EMIRR	EMI rejection rate = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mVpp, f = 2400 MHz		91		dB

1. *See section 4.2 Input offset voltage drift vs. temperature.*
2. *The slew rate value is the average of rising and falling values.*

4 Typical performance characteristics

Figure 4. Input offset voltage distribution at V_{CC} = 1.8 V

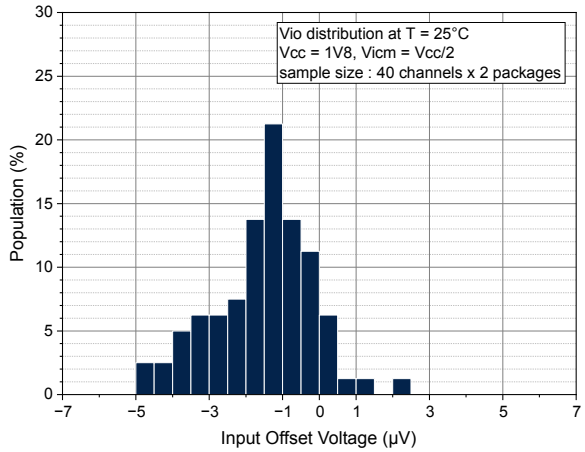


Figure 5. Input offset voltage distribution at V_{CC} = 3.3 V

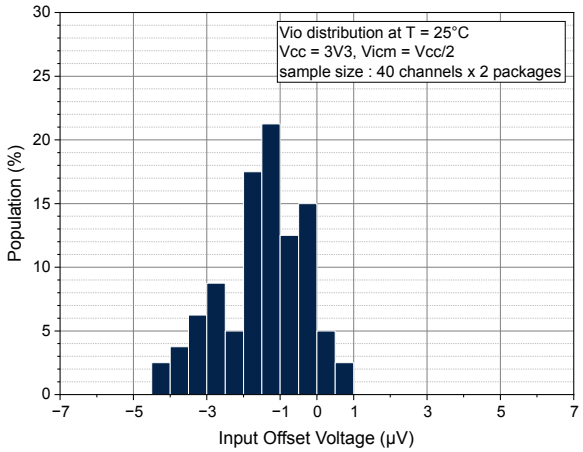


Figure 6. Input offset voltage distribution at V_{CC} = 5 V

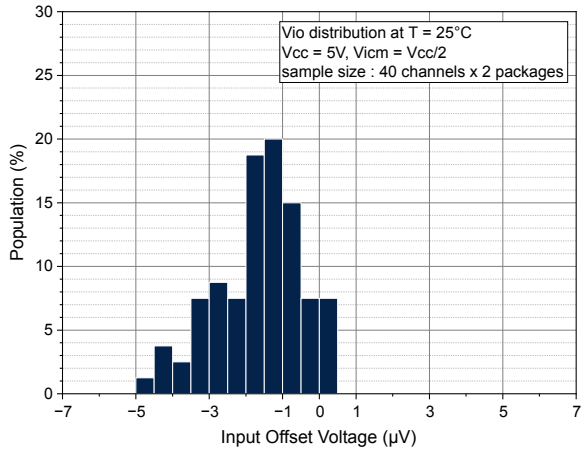


Figure 7. Input offset voltage vs. supply voltage

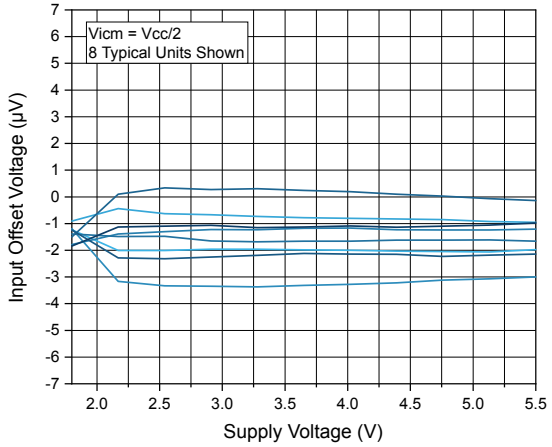


Figure 8. Input offset voltage temperature drift distribution at V_{CC} = 1.8 V (-40 °C to 25 °C)

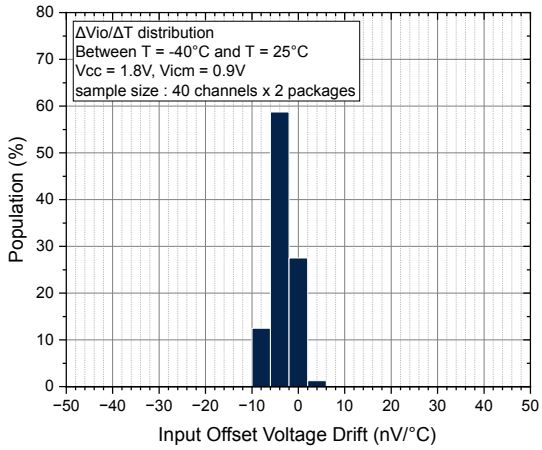


Figure 9. Input offset voltage temperature drift distribution at V_{CC} = 1.8 V (25 °C to 125 °C)

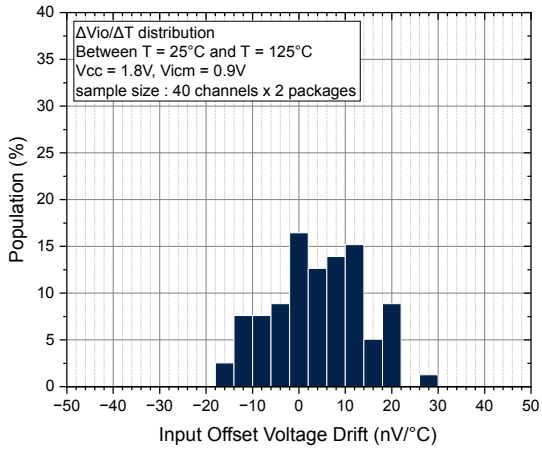


Figure 10. Input offset voltage temperature drift distribution at V_{CC} = 5 V (-40 °C to 25 °C)

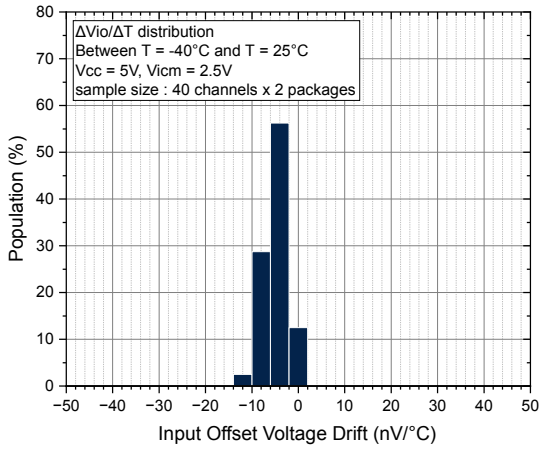


Figure 11. Input offset voltage temperature drift distribution at V_{CC} = 5 V (25 °C to 125 °C)

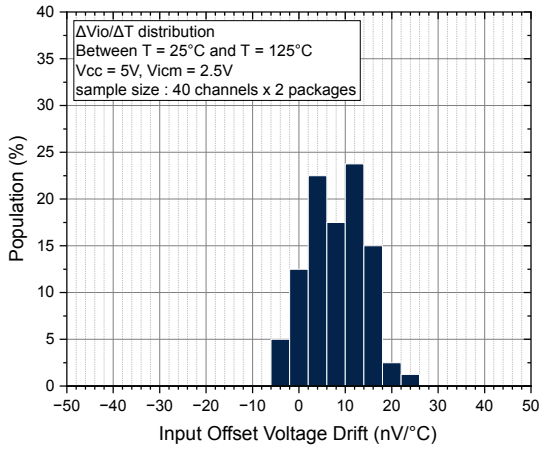


Figure 12. Input offset voltage vs. temperature

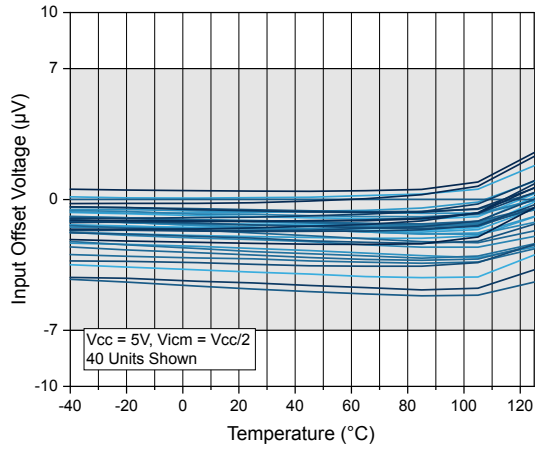


Figure 13. Input offset voltage vs. input common-mode voltage at V_{CC} = 1.8 V

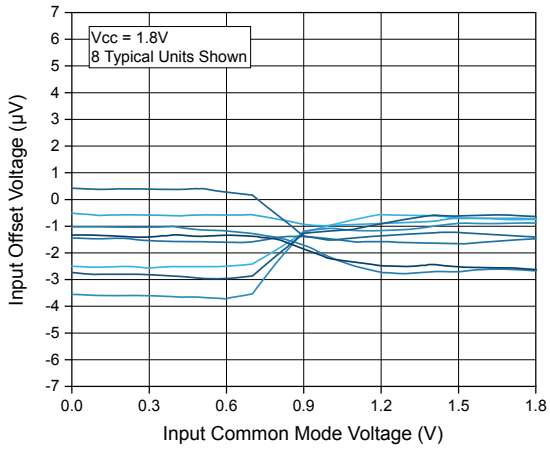


Figure 14. Input offset voltage vs. input common-mode voltage at V_{CC} = 3.3 V

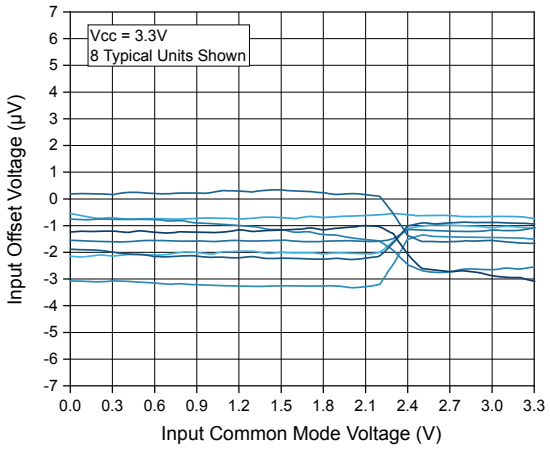


Figure 15. Input offset voltage vs. input common-mode voltage at V_{CC} = 5 V

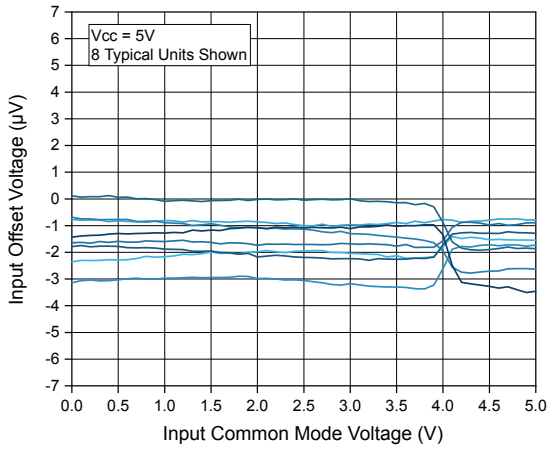


Figure 16. Supply current vs. input common-mode voltage at V_{CC} = 5 V

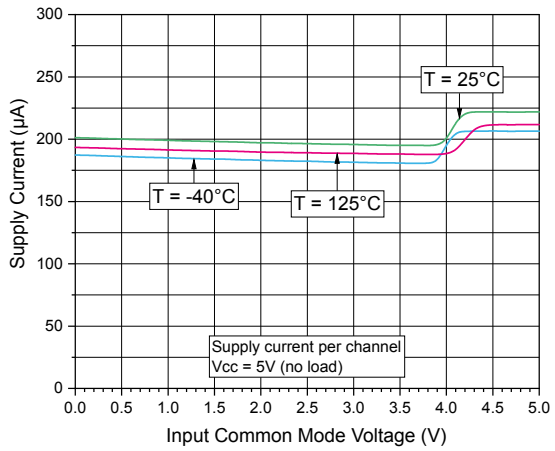


Figure 17. Supply current vs. supply voltage

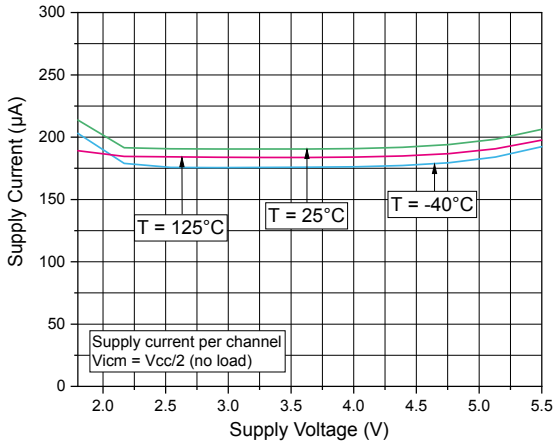


Figure 18. Output drop voltage V_{OH} vs. supply voltage

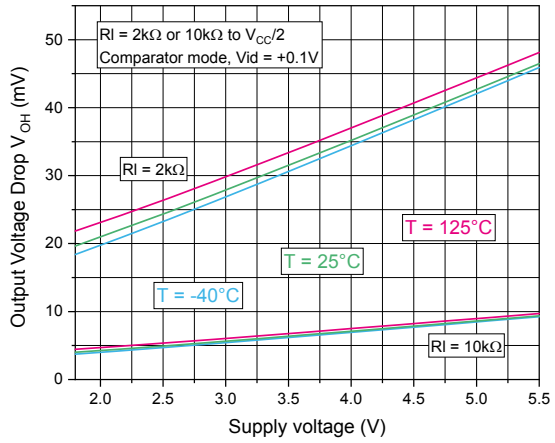


Figure 19. Output drop voltage V_{OL} vs. supply voltage

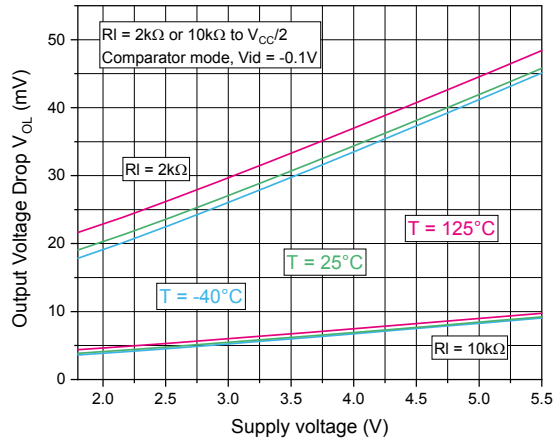


Figure 20. Output current vs. output voltage at V_{CC} = 1.8 V

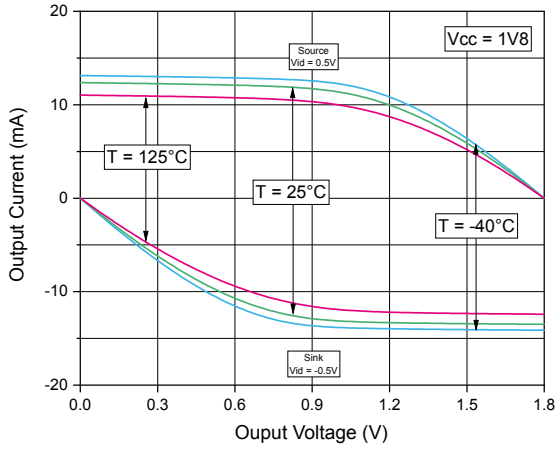


Figure 21. Output current vs. output voltage at V_{CC} = 3.3 V

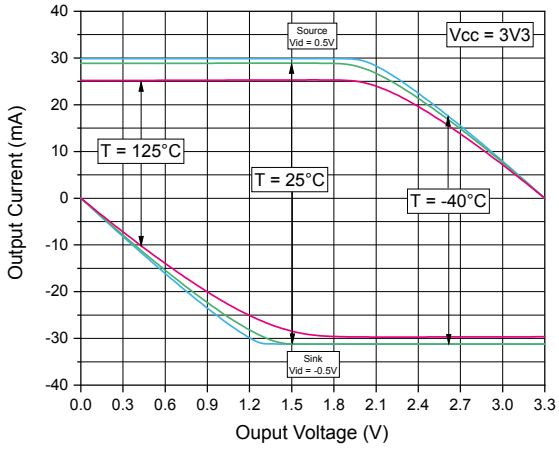


Figure 22. Output current vs. output voltage at V_{CC} = 5 V

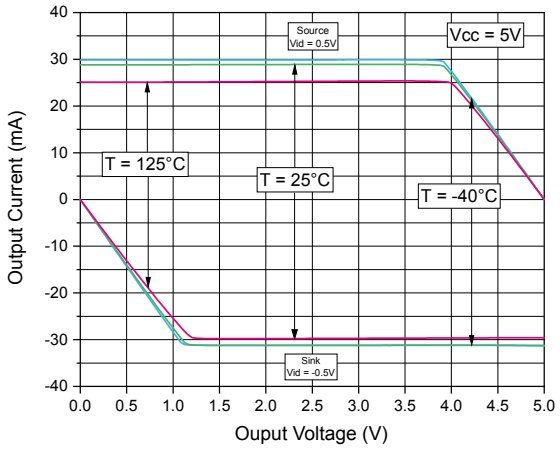


Figure 23. Input bias current vs. input common-mode voltage at V_{CC} = 1.8 V

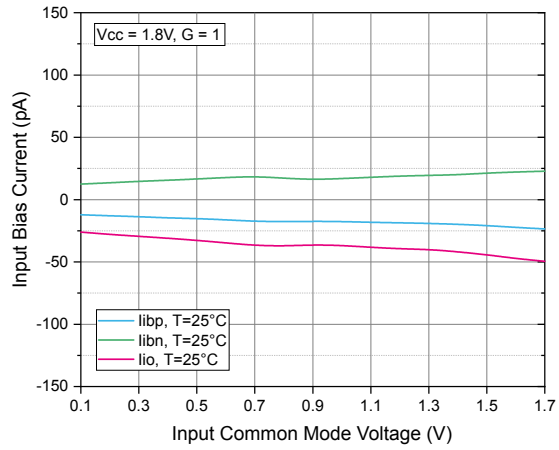


Figure 24. Input bias current vs. input common-mode voltage at V_{CC} = 5 V

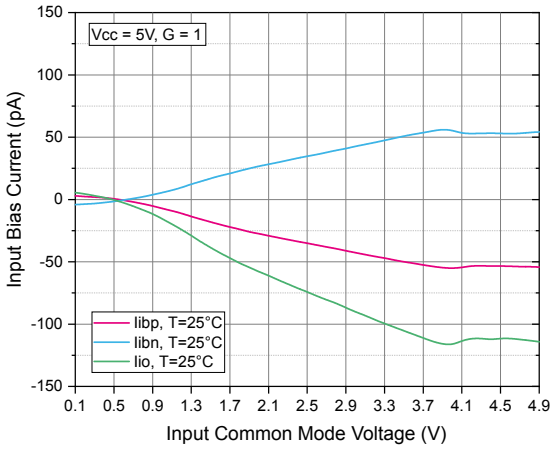


Figure 25. Input bias current vs. input common-mode voltage at T = 125 °C

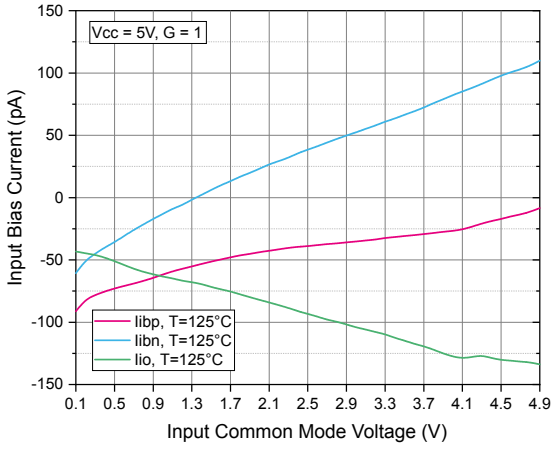


Figure 26. Bode diagram vs. temperature at V_{CC} = 1.8 V

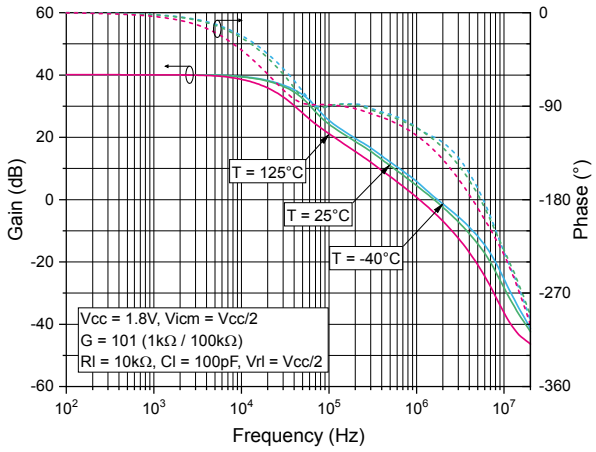


Figure 27. Bode diagram vs. temperature at V_{CC} = 3.3 V

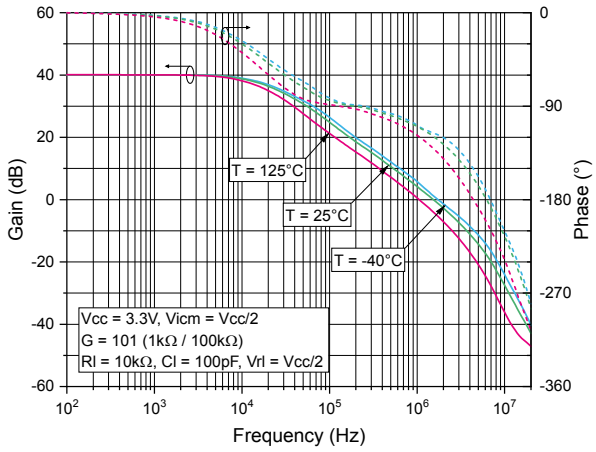


Figure 28. Bode diagram vs. temperature at V_{CC} = 5 V

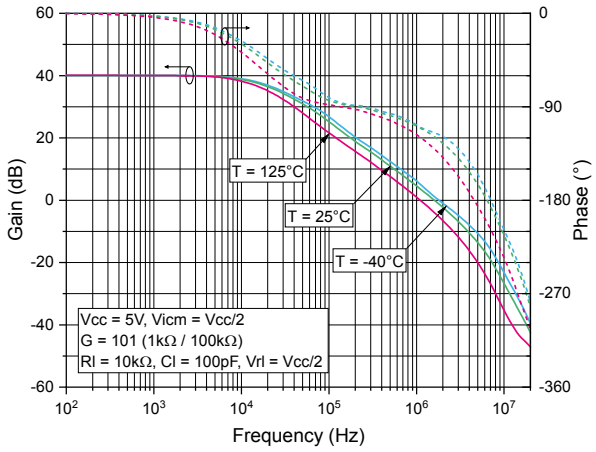


Figure 29. Bode diagram vs. output current at V_{CC} = 1.8 V

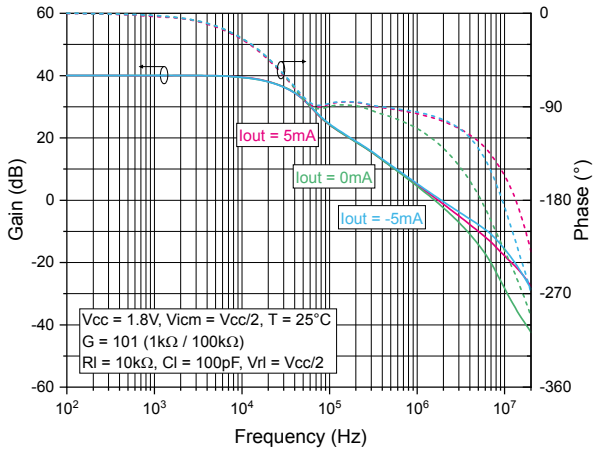


Figure 30. Bode diagram vs. output current at V_{CC} = 3.3 V

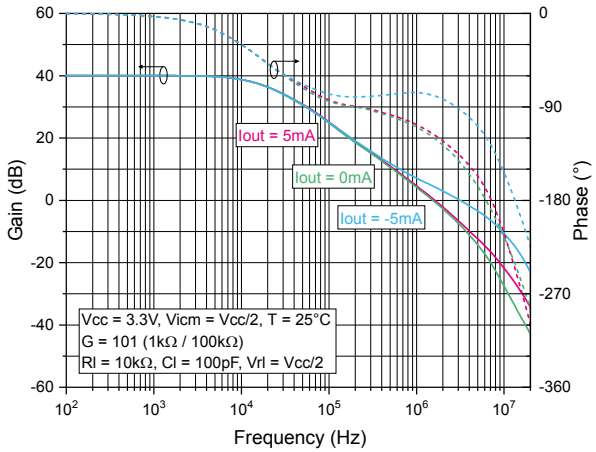


Figure 31. Bode diagram vs. output current at V_{CC} = 5 V

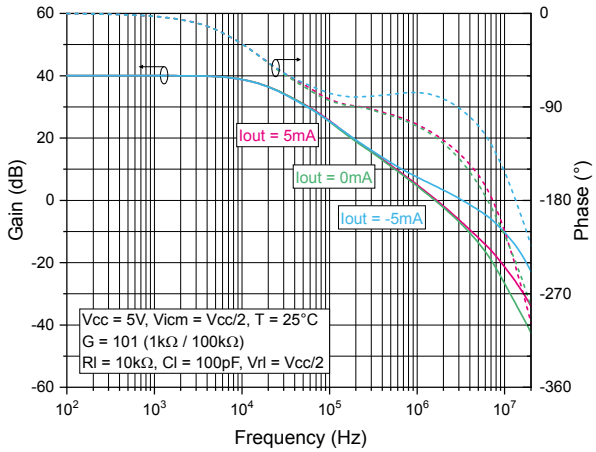


Figure 32. Step overshoot vs. load capacitance

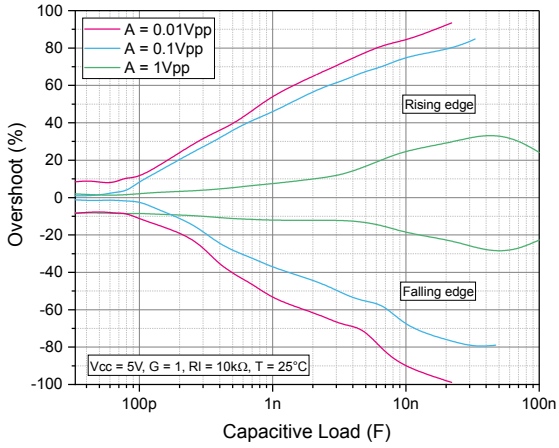


Figure 33. Small step overshoot vs. load capacitance and Riso

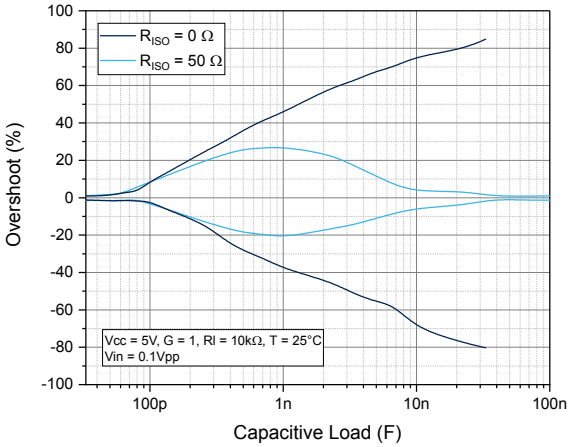


Figure 34. Small step overshoot vs. Riso

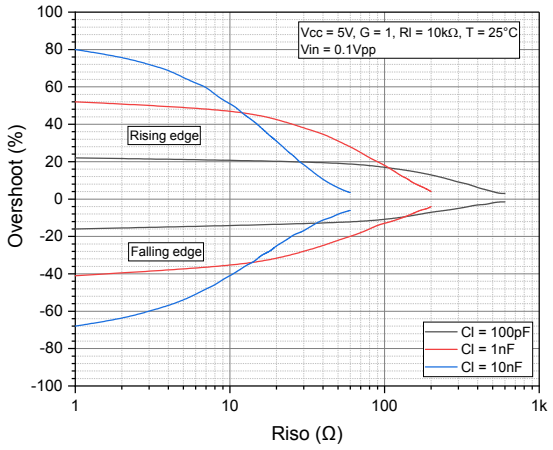


Figure 35. Small step settling time vs. Riso

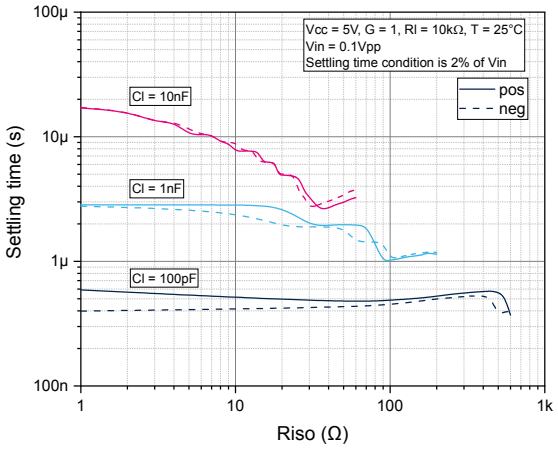


Figure 36. Overshoot vs. input common-mode voltage and output current at V_{CC} = 1.8 V

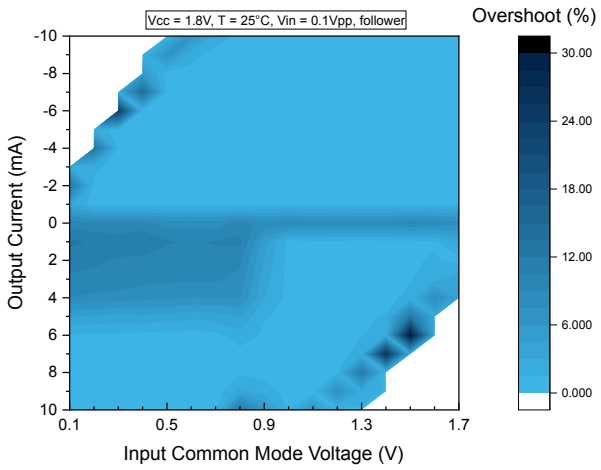


Figure 37. Overshoot vs. input common-mode voltage and output current at V_{CC} = 5 V

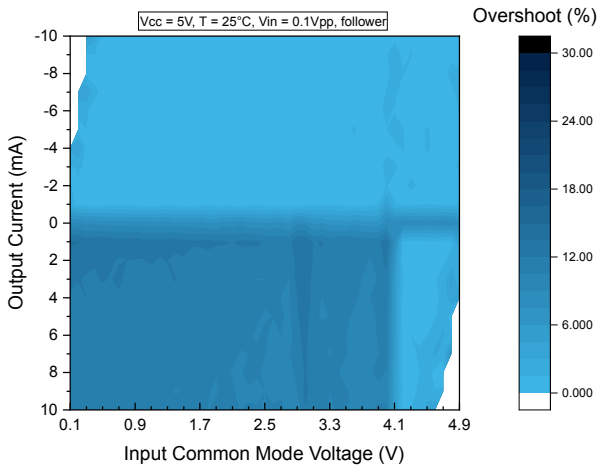


Figure 38. Overshoot vs. input common-mode voltage and output current at T = -40 °C

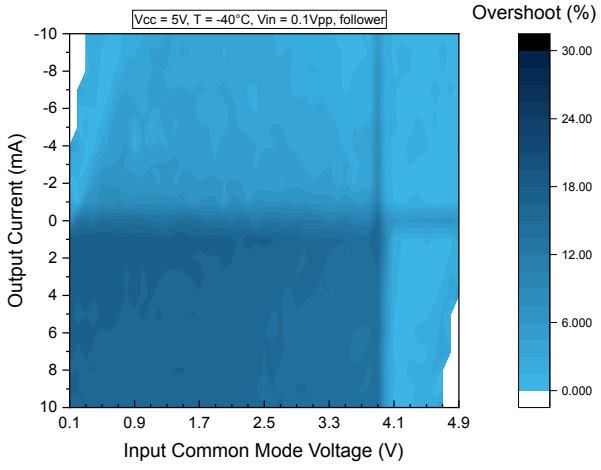


Figure 39. Overshoot vs. input common-mode voltage and output current at T = 125 °C

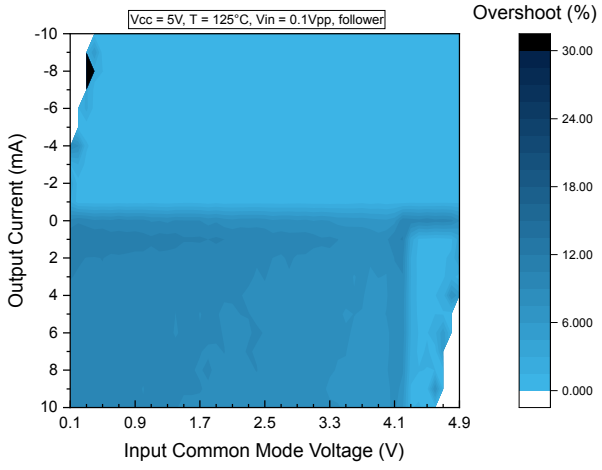


Figure 40. Slew rate vs. temperature

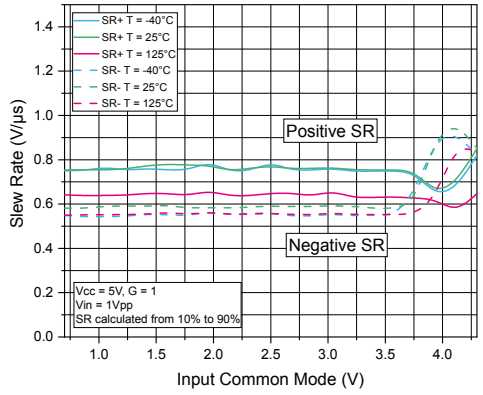


Figure 41. Noise vs. time at V_{CC} = 5 V

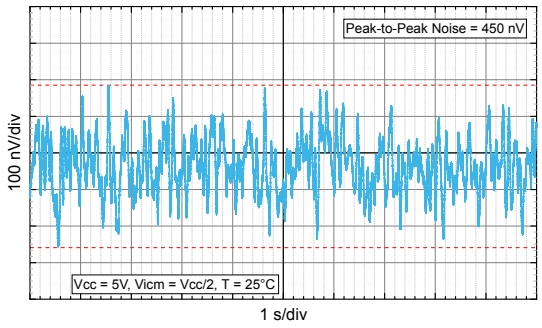


Figure 42. Voltage noise density vs. frequency at V_{CC} = 1.8 V

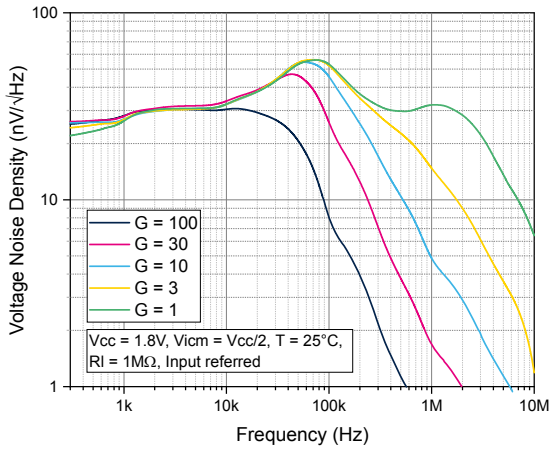


Figure 43. Voltage noise density vs. frequency at V_{CC} = 5 V

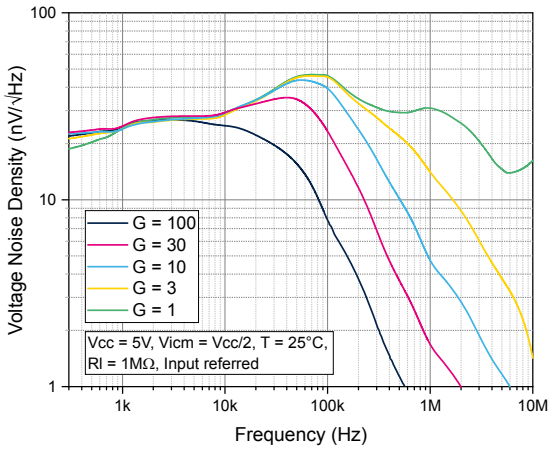


Figure 44. Small signal step response at V_{CC} = 1.8 V

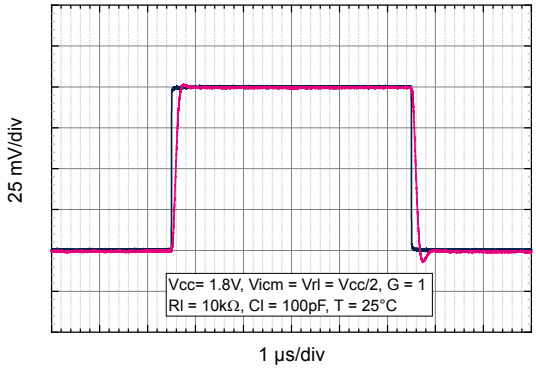


Figure 45. Large signal step response at V_{CC} = 1.8 V

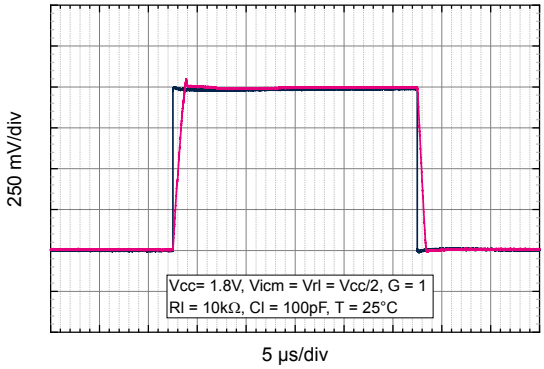


Figure 46. Small signal step response at V_{CC} = 5 V

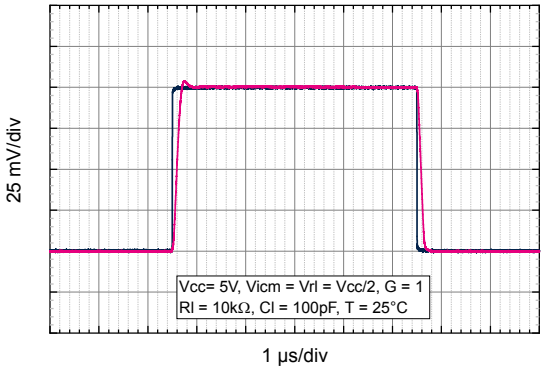


Figure 47. Large signal step response at V_{CC} = 5 V

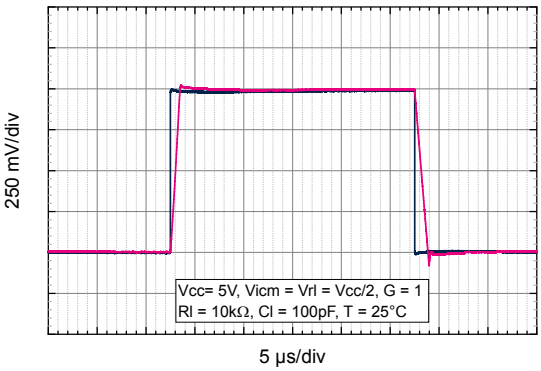


Figure 48. Very large signal step response at V_{CC} = 5 V

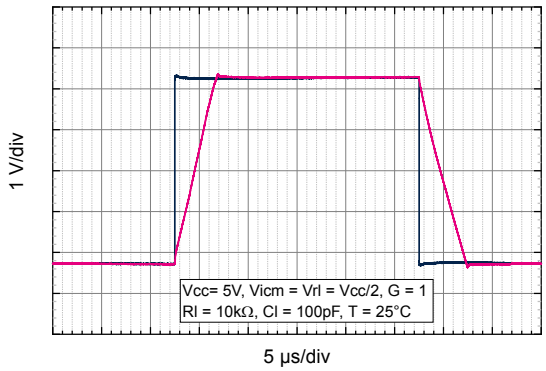


Figure 49. Output voltage saturation response at V_{CC} = 5 V

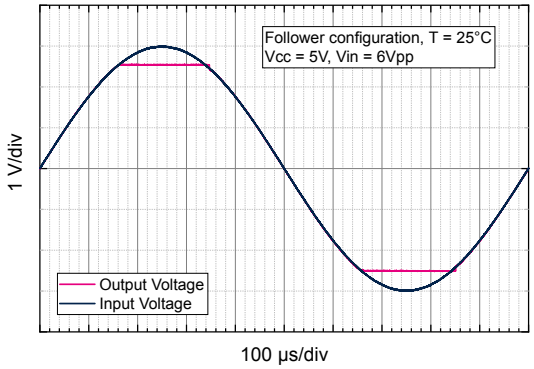


Figure 50. Positive overvoltage recovery at V_{CC} = 1.8 V

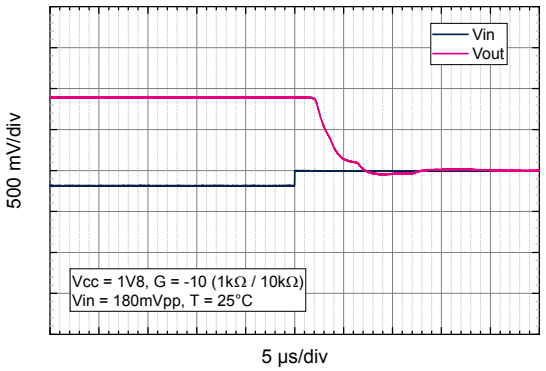


Figure 51. Positive overvoltage recovery at V_{CC} = 5 V

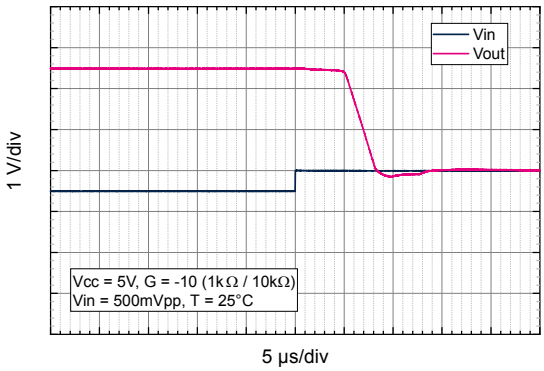


Figure 52. Negative overvoltage recovery at V_{CC} = 1.8 V

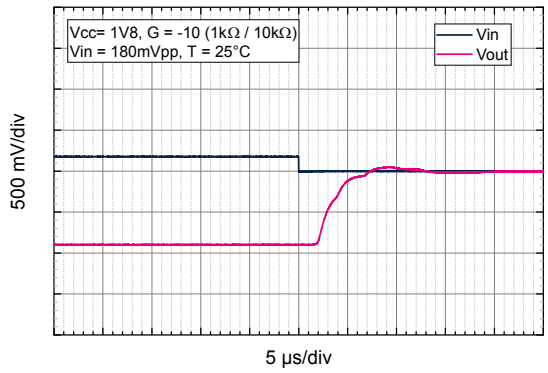


Figure 53. Negative overvoltage recovery at V_{CC} = 5 V

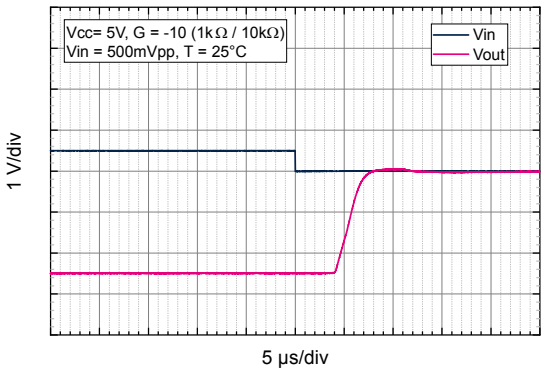


Figure 54. Settling time on negative input step

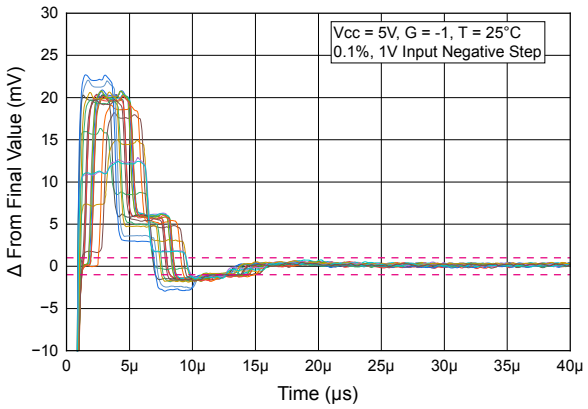


Figure 55. Settling time on positive input step

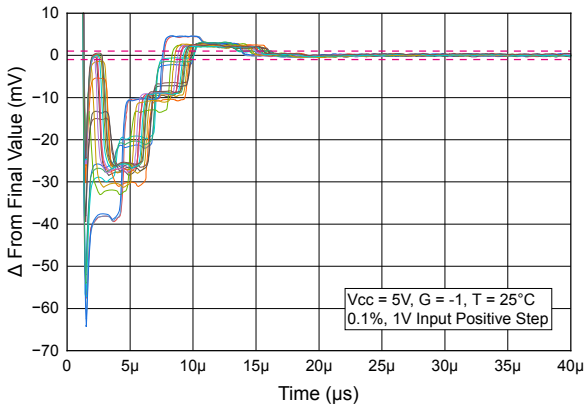


Figure 56. Output voltage vs. input voltage at V_{CC} = 5 V

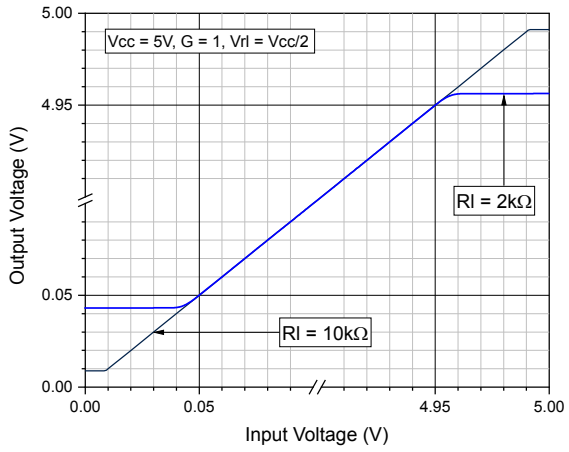


Figure 57. Startup behavior at V_{CC} = 5 V

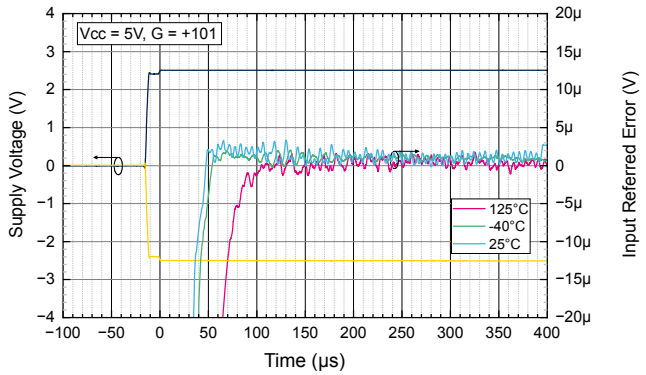


Figure 58. CMRR and PSRR vs. frequency at V_{CC} = 1.8 V

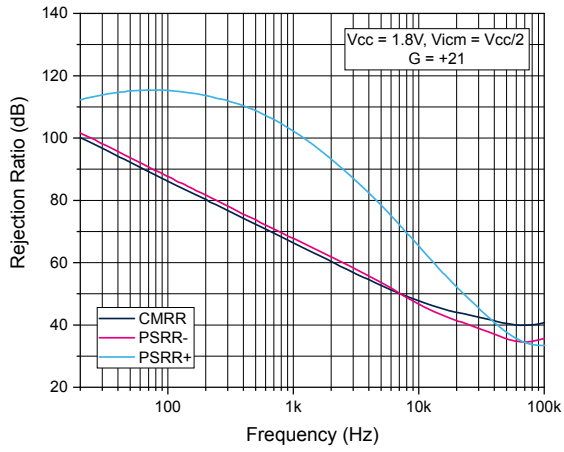


Figure 59. CMRR and PSRR vs. frequency at V_{CC} = 5 V

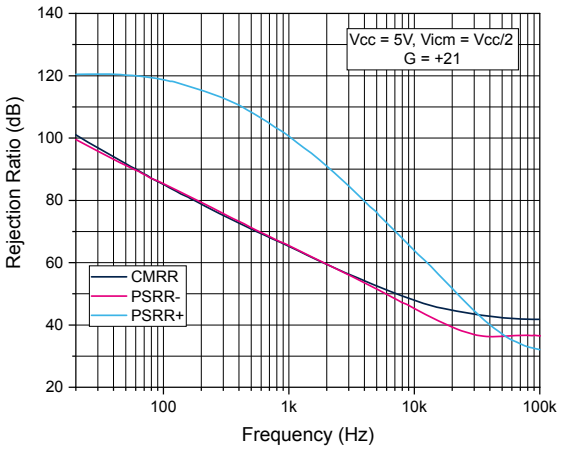


Figure 60. **THD vs. frequency**

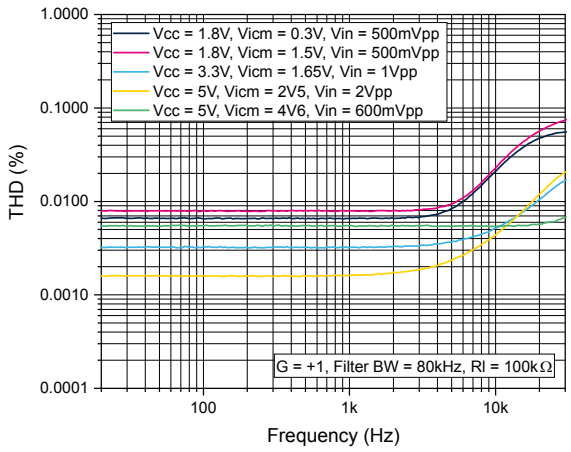
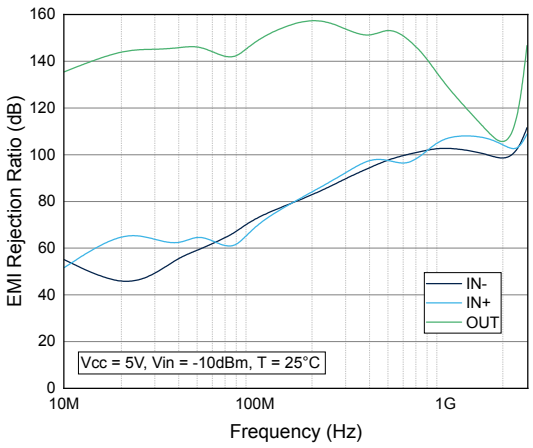


Figure 61. **EMI rejection vs. frequency**



5 Application information

5.1 Operating voltages

The TSZ151 and TSZ152 devices can operate from 1.8 to 5.5 V. The parameters are fully specified at 1.8 V, 3.3 V, and 5 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSZ151 and TSZ152 devices characteristics over the full operating range. Additionally, the main specifications are guaranteed in an extended temperature range from -40 to 125 °C.

5.2 Input offset voltage drift vs. temperature

The maximum input voltage drift variation vs. temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{io}) is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift vs. temperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift vs. temperature is computed using equation 1.

$$\frac{\Delta V_{io}}{\Delta T} = \left(\frac{V_{io\_T} - V_{io\_25°C}}{T - 25°C}\right)_{T = -40\,°C \text{ and } T = 125\,°C} \quad (1)$$

The datasheet minimum and maximum values are guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.3 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSZ151 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

T_J is the die junction temperature.

P_D is the power dissipated in the package.

θ_{JA} is the junction to thermal resistance of the package.

T_A is the ambient temperature.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times I_{OUT}$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times I_{OUT}$ when the op amp is sinking the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.4 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, use a multi-via technique that connects the bottom and top layer ground planes together in many locations. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.5 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pin. A good decoupling helps to reduce an electromagnetic interference impact.

5.6 Macromodel

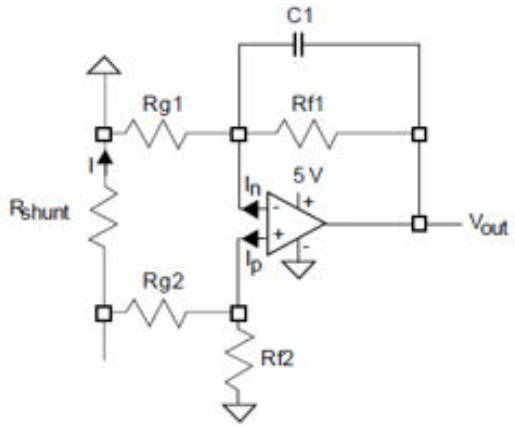
Accurate macromodels of the TSZ151 device are available on the STMicroelectronics website at: www.st.com. These models are a trade-off between the accuracy and complexity (that is, time simulation) of the TSZ151 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSZ151 and TSZ152.

Figure 62. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{out} = R_{shunt} \cdot I\left(1 - \frac{Rg2}{Rg2 + rf2}\right) \cdot \left(1 + \frac{Rf1}{Rf2}\right) + I_p \cdot \frac{Rg2 \cdot Rf2}{Rg2 + Rf2} \cdot \left(1 + \frac{Rf1}{Rg1}\right) - I_n \cdot Rf1 - V_{io} \cdot \left(1 + \frac{Rf1}{rg1}\right) \quad (3)$$

Assuming that Rf2 = Rf1 = Rf and Rg2 = Rg1 = Rg, equation 4 can be simplified as follows:

$$V_{out} = R_{shunt} \cdot I \cdot \frac{Rf}{Rg} - V_{io} \cdot \left(1 + \frac{Rf}{Rg}\right) + Rf \cdot I_{io} \quad (4)$$

The main advantage of using the TSZ151 and TSZ152 for a low-side current sensing relies on its low V_{io}, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the precision of Rg1 and Rf1, to maximize the accuracy of the measurement.

Note that the open loop gain of TSZ151 and TSZ152 are defined close to the rail. It enables measurements over a wide range of currents.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SC70-5 (or SOT323-5) package information

Figure 63. **SC70-5 (or SOT323-5) package outline**

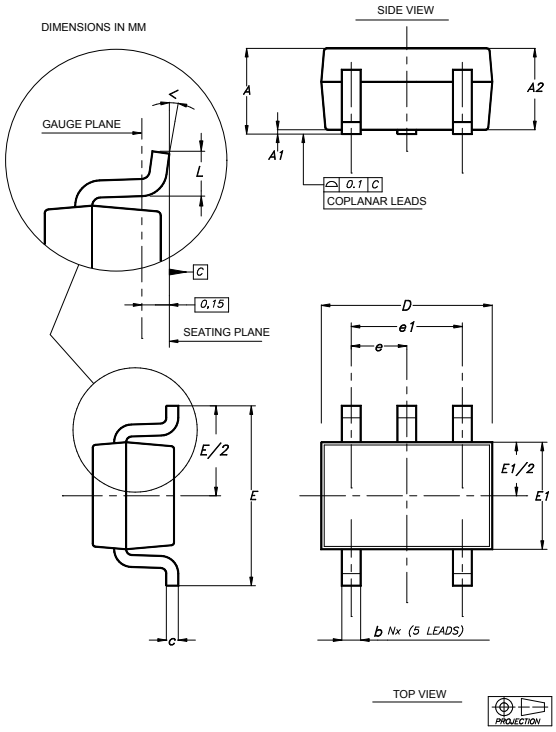


Table 9. **SC70-5 (or SOT323-5) package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

7.2 SOT23-5 package information

Figure 64. **SOT23-5 package outline**

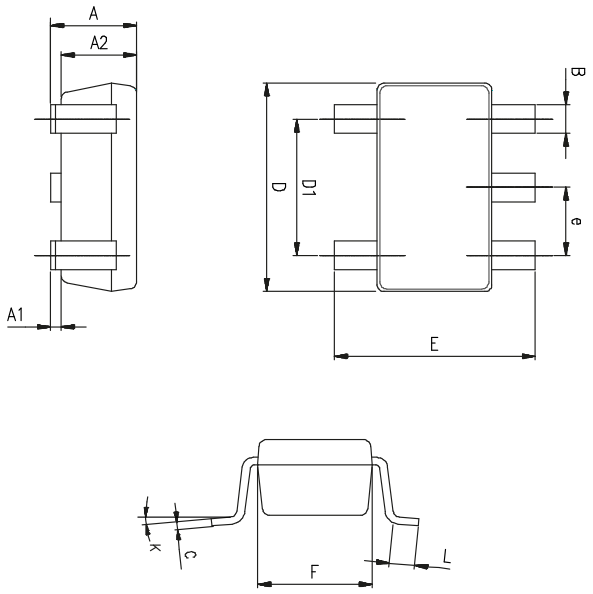


Table 10. **SOT23-5 mechanical data**

Dimensions						
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

7.3 SO8 package information

Figure 65. **SO8 package outline**

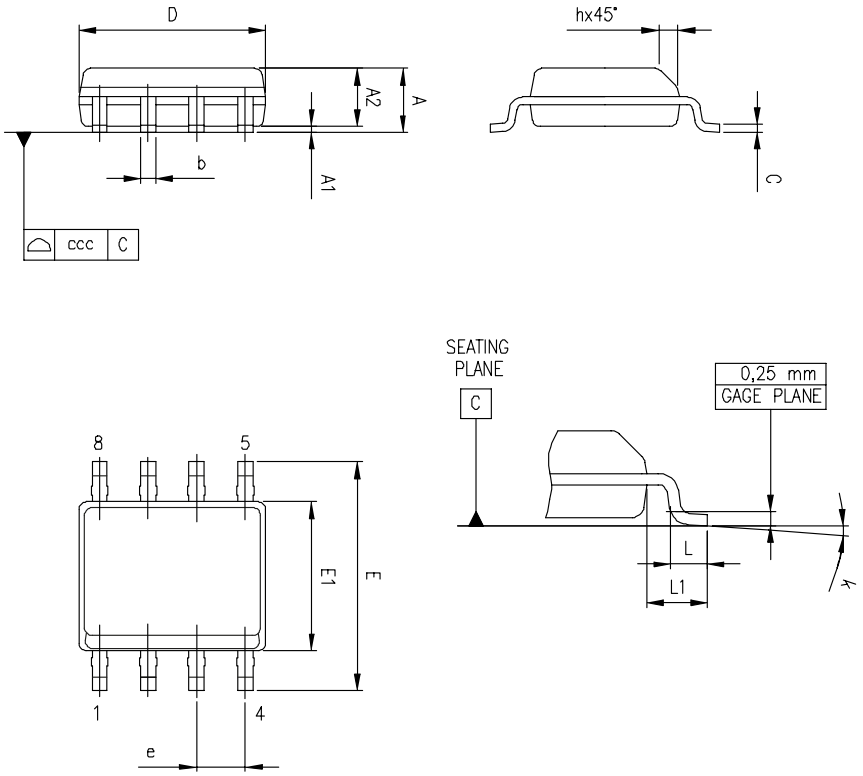


Table 11. **SO-8 mechanical data**

Symbol	Milimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

7.4 MiniSO8 package information

Figure 66. **MiniSO8 package outline**

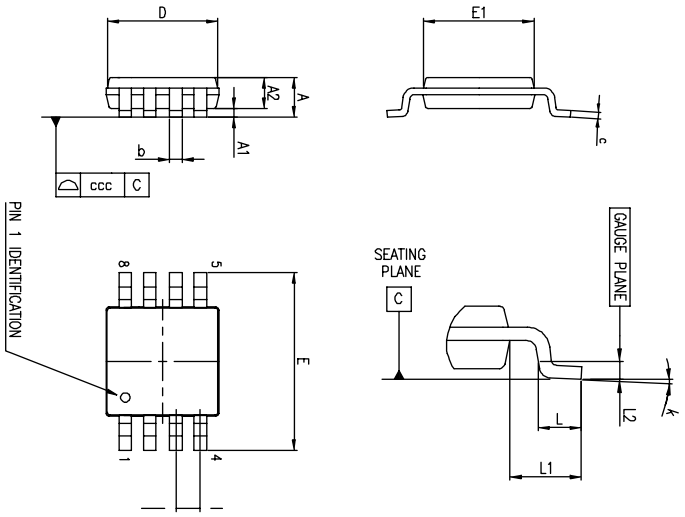


Table 12. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.5 DFN8 2 x 2 wettable flank package information

Figure 67. **DFN8 2 x 2 wettable flank package outline**

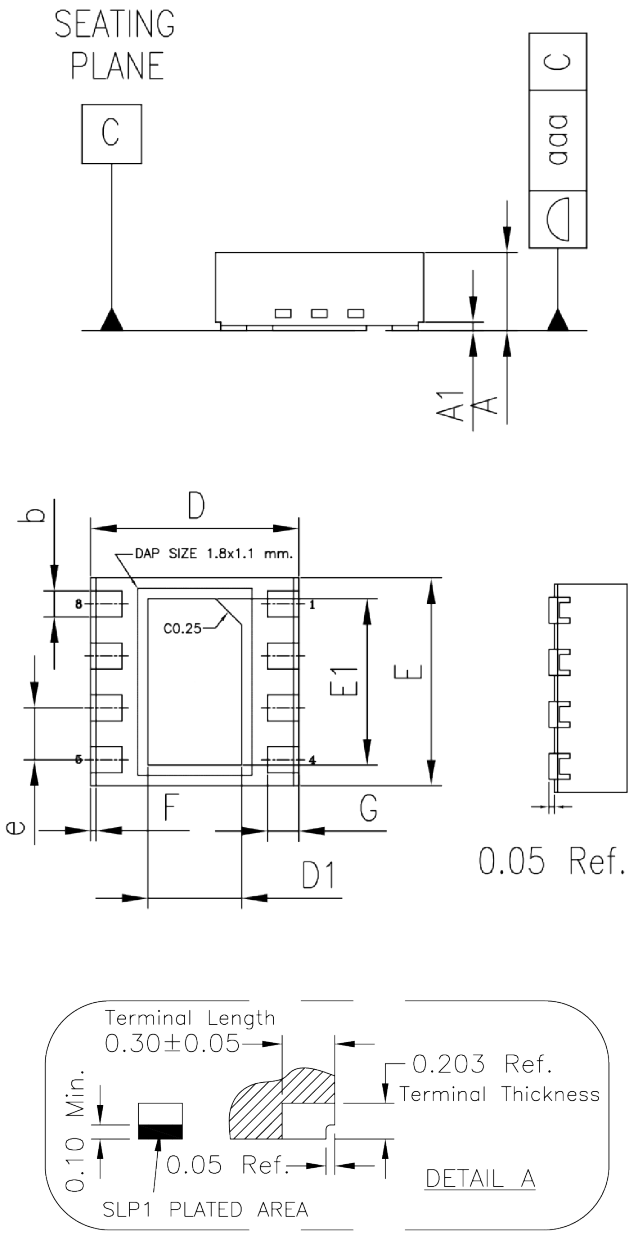
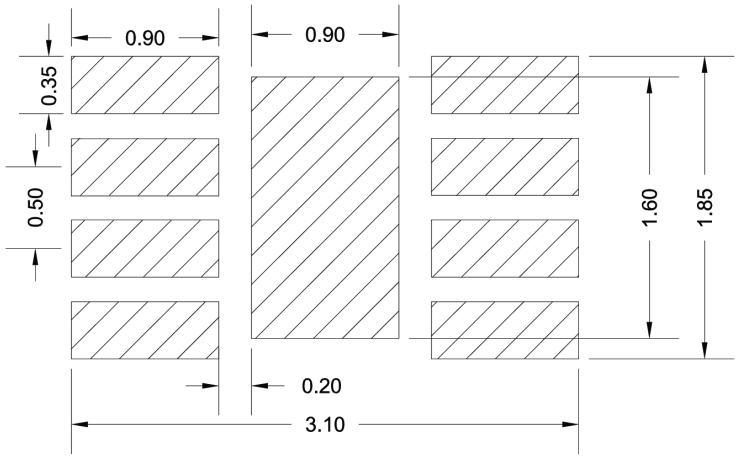


Table 13. **DFN8 2 x 2 wettable flank package mechanical data**

Ref.	Dimensions					
	Millimiters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.10			0.004		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	0.80	0.90	1.00	0.031	0.035	0.039
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.50	1.60	1.70	0.059	0.063	0.067
e		0.50			0.020	
F		0.05			0.002	
G	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.10			0.004	

Figure 68. **DFN8 2 x 2 wettable flank recommended footprint**



8 Ordering information

Table 14. **Order codes**

Order code	Temperature range	Package	Marking
TSZ151ICT	-40 °C to 125 °C	SC70-5	K4K
TSZ151ILT		SOT23-5	K234
TSZ151IYCT	-40 °C to 125 °C automotive grade (1)	SC70-5	K4L
TSZ151IYLT		SOT23-5	K235
TSZ152IDT	-40 °C to 125 °C	SO8	TSZ152I
TSZ152IYDT	-40 °C to 125 °C automotive grade (1)		TSZ152IY
TSZ152IST	-40 °C to 125 °C	MiniSO8	K4M
TSZ152IYST	-40 °C to 125 °C automotive grade (1)		K4O
TSZ152IQ2T	-40 °C to 125 °C	DFN8	K4M
TSZ152IYQ2T	-40 °C to 125 °C automotive grade (1)		K4O

1. *Qualification and characterization according to AEC Q100 and Q003 or the equivalent, advanced screening according to AEC Q001 & Q002 or the equivalent. For qualification status details, check the "Maturity Status" link on the first page ("Quality & Reliability" tab on www.st.com).*

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
13-Oct-2023	1	Initial release.
20-Nov-2023	2	Added new Section 4.
22-Jan-2024	3	Updated figure and description on the cover page, Section 8. Added new TSZ152 root part number, new Section 1.3, Section 7.3, Section 7.4 and Section 7.5.

Contents

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved