8 KEYS TOUCH PAD DETECTOR IC

GENERAL DESCRIPTION

The TTP225 TonTouch™ is a touch pad detector IC with open drain output which offers 8 touch keys. The touching detection IC is designed for replacing traditional direct button key with fixed pad size. Low power consumption and wide operating voltage are the contact key features for DC or AC application.

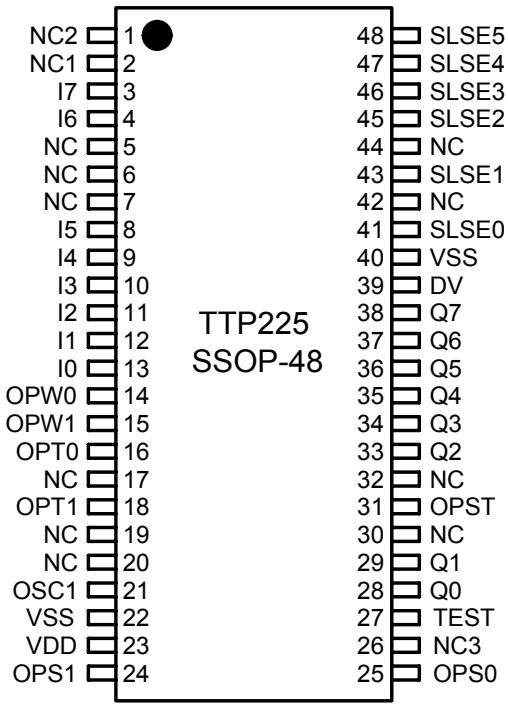
FEATURES

- Operating voltage 2.0V~5.5V
- Operating current typical 120uA, max 160uA at VDD=3V
- The output refresh rate about 85Hz at VDD=3V
- 64 steps sensitivity selectable (SLSE0~5 pin option)
  Another have offer 2 kinds of base-step (OPST pin option)
- Stable touching detection of human body for replacing traditional direct switch key
- Provides direct mode、matrix mode and serial mode selected by pad option
- Maximum 8 input pads and 8 outputs for direct mode;
  Maximum 8 input pads for serial interface mode;
  Maximum 8 input pads provide fixed 2*4 and 3*3 matrix types
- Outputs(Q0~Q7) are open drain(active low)
- After power-on have 0.5~0.7sec stable-time, during the time do not touch the key-pad, And the function is disabled.
- Auto calibration for life. And the re-calibration period is 0.5~0.7sec.
  When all keys do not touched.

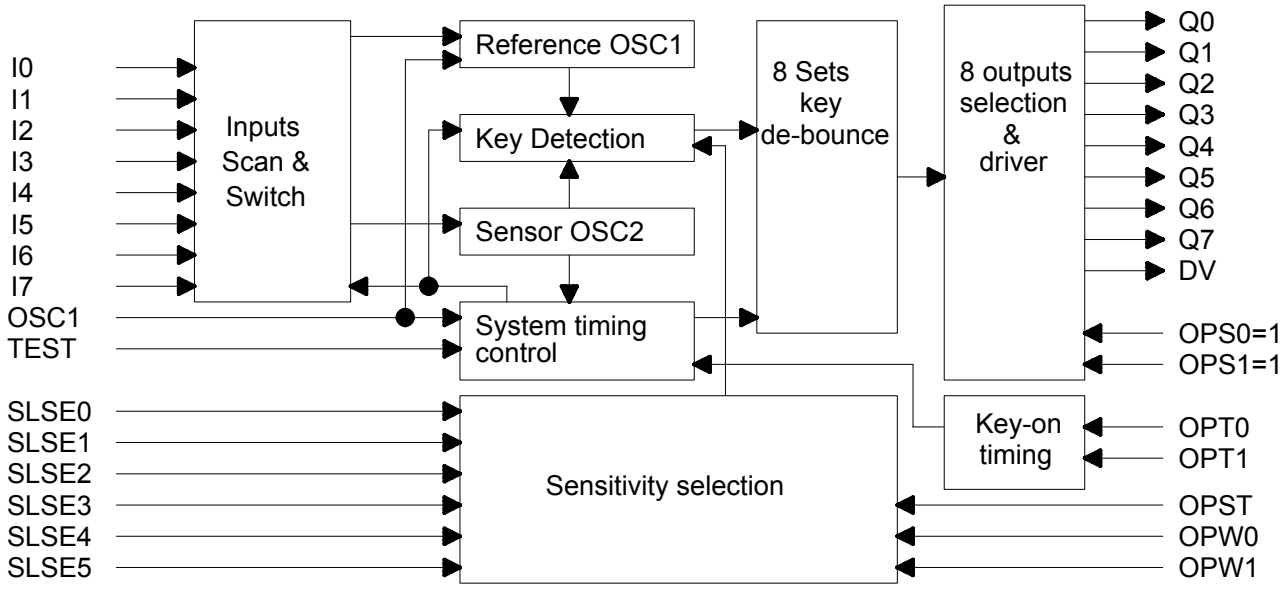
APPLICATION

- Wide consumer products
- Button key replacement

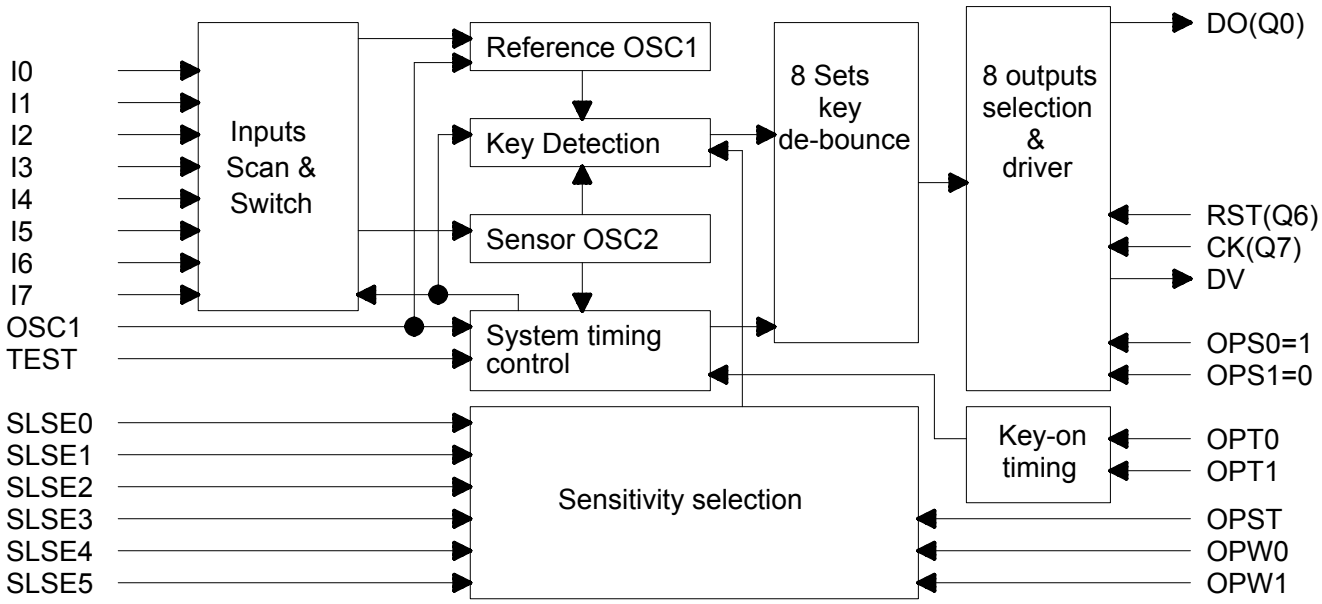
PACKAGE CONFIGURATION



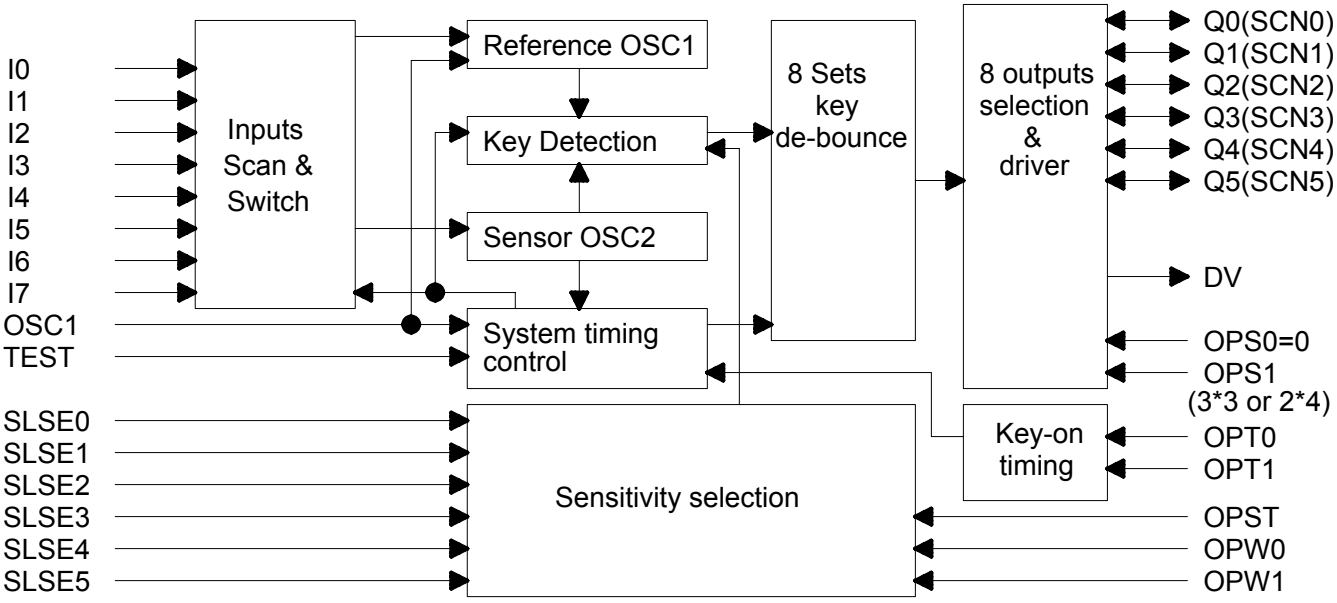
BLOCK DIAGRAM FOR DIRECT MODE :



BLOCK DIAGRAM FOR SERIAL INTERFACE MODE :



BLOCK DIAGRAM FOR KEY-MATRIX MODE :



PIN DESCRIPTION

Pin No.	Pin Name	Share Pin	I/O Type	Pin Description
1	NC2			
2	NC1			
3	I7		I	Input port
4	I6		I	Input port
5	NC			
6	NC			
7	NC			
8	I5		I	Input port
9	I4		I	Input port
10	I3		I	Input port
11	I2		I	Input port
12	I1		I	Input port
13	I0		I	Input port
14	OPW0		I-PH	OPW0~1 are option pins to select the windows of key-detected
15	OPW1		I-PH	OPW0~1 are option pins to select the windows of key-detected
16	OPT0		I-PH	OPT0~1 are option pins to select the time of key-on
17	NC			
18	OPT1		I-PH	OPT0~1 are option pins to select the time of key-on
19	NC			
20	NC			
21	OSC1		I/O	System oscillator pin
22	VSS		P	Negative power supply，ground
23	VDD		P	Positive power supply
24	OPS1		I-PH	Output type option pin
25	OPS0		I-PH	Output type option pin
26	NC3			
27	TEST		I-PH	Only for test，when normal function must be connected to VSS
28	Q0	(DO/SCN0)	I/O/OD	Q0 is open drain output pin on direct mode (active low) DO is the shifted data output pin on serial mode (open drain) SCN0 is the first scanning pin on matrix mode
29	Q1	(SCN1)	I/O/OD	Q1 is open drain output pin on direct mode (active low) SCN1 is the second scanning pin on matrix mode
30	NC			
31	OPST		I-PH	Selecting the base step of sensitivity
32	NC			
33	Q2	(SCN2)	I/O/OD	Q2 is open drain output pin on direct mode (active low) SCN2 is the third scanning pin on matrix mode
34	Q3	(SCN3)	I/O/OD	Q3 is open drain output pin on direct mode (active low) SCN3 is the fourth scanning pin on matrix mode
35	Q4	(SCN4)	I/O/OD	Q4 is open drain output pin on direct mode (active low) SCN4 is the fifth scanning pin on matrix mode
36	Q5	(SCN5)	I/O/OD	Q5 is open drain output pin on direct mode (active low) SCN5 is the sixth scanning pin on matrix mode
37	Q6	(RST)	I/OD	Q6 is open drain output pin on direct mode (active low) RST is the reset input pin on serial mode
38	Q7	(CK)	I/OD	Q7 is open drain output pin on direct mode (active low) CK is the clock input pin on serial mode
39	DV		O	Data valid output signal
40	VSS		P	Negative power supply，ground
41	SLSE0		I-PH	SLSE0~5 are option pins to selected the sensitivity
42	NC			
43	SLSE1		I-PH	SLSE0~5 are option pins to selected the sensitivity
44	NC			
45	SLSE2		I-PH	SLSE0~5 are option pins to selected the sensitivity
46	SLSE3		I-PH	SLSE0~5 are option pins to selected the sensitivity
47	SLSE4		I-PH	SLSE0~5 are option pins to selected the sensitivity
48	SLSE5		I-PH	SLSE0~5 are option pins to selected the sensitivity
Note: > CK and RST input with protection resistor for output collision.				

Pin Type

I	CMOS input only	I-PH	CMOS input and pull-high resister
O	CMOS push-pull output	P	Power / Ground
I/O	CMOS I/O		
I/O/OD	CMOS I/O or open-drain output		
I/OD	CMOS input or open-drain output		

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Value	Unit
Operating Temperature	T_{OP}	—	-20 ~ +70	℃
Storage Temperature	T_{STG}	—	-50 ~ +125	℃
Power Supply Voltage	VDD	Ta=25°C	VSS-0.3 ~ VSS+5.5	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3 ~ VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note：VSS symbolizes for system ground				

- **DC/AC Characteristics**：(Test condition at room temperature=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.0	3	5.5	V
Reference oscillator	OSC1	VDD=3V	-	710K	-	Hz
Sensor oscillator	OSC2	VDD=3V no load	-	710K	-	Hz
Operating Current	I_{OP}	VDD=3V output no load	-	120	160	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
Output port Sink Current	I_{OL}	VDD=3V, Vol=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=3V, Voh=2.4V	-	-4	-	mA

FUNCTION DESCRIPTION

1. System timing control

- Input detection sensitivity reserved 6 pin option 64 steps

Features	Characteristic	Example
System clock	OSC1	710KHz at 3V
Output refresh rate	<= OSC1/1024/8	~85Hz
DV active pulse width	<= OSC1/8	~88KHz

2. System initial signal

System initial or mode initial	
State	Function
Power on reset	System reset to initial state
RST=1	*Serial mode shift counter reset*

3. Interrupt

For MCU system, the interrupt request is useful for software programming. The DV signal offer the considerate output control. The DV is active low. Any active input can pass the de-bounce procedure will active the DV signal.

4. Output mode

Most output modes will operate at direct or serial mode. Only when OPS0=0, the output mode will work as matrix type.

Output type option			
OPS1	OPS0	Output type	Remark
1	1	*Direct type*	Qi ← de-bounce Ii
0	1	*Serial type*	Use CK & RST & DO serial out the de-bounce key
1	0	*Matrix type*	Matrix 3*3 fixed type
0	0	*Matrix type*	Matrix 2*4 fixed type

a. Direct mode: OPS1=1 & OPS0=1

Direct mode	Output state
Input trigger	De-bounce Ii trigger the Qi

b. Key matrix mode: OPS1=X & OPS0=0

b-1: 2*4 key map (By OPS1=0)

Matrix	*SCN2*	*SCN3*	*SCN4*	*SCN5*
SCN0	**I0**	**I2**	**I4**	**I6**
SCN1	**I1**	**I3**	**I5**	**I7**

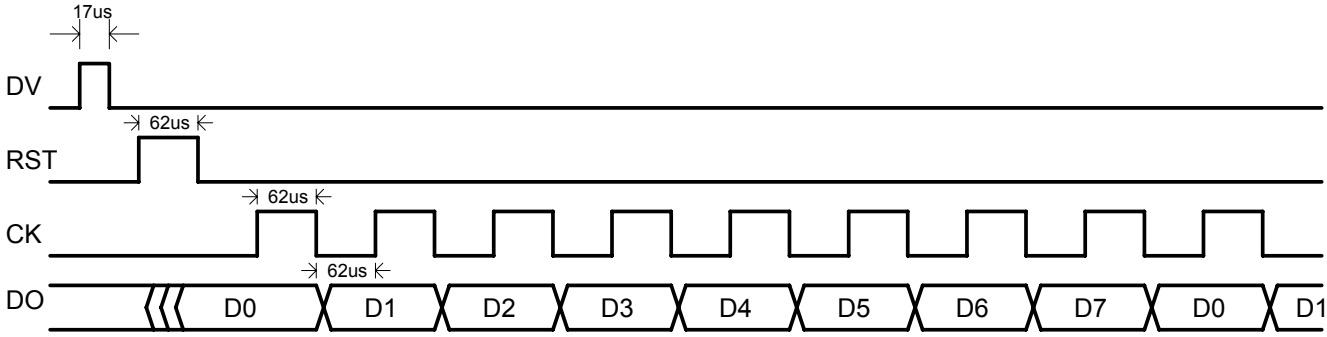
b-2: 3*3 key map (By OPS1=1)

Matrix	*SCN3*	*SCN4*	*SCN5*
SCN0	**I0**	**I3**	**I6**
SCN1	**I1**	**I4**	**I7**
SCN2	**I2**	**I5**	**-**

c. Serial mode: OPS1=0 & OPS0=1

Serial mode procedure (OPS1=0)		
RESET & CLOCK	Shifter counter	DO
RST =1	0	De-bounce I0
1st CK	1	De-bounce I1
2nd CK	2	De-bounce I2
3rd CK	3	De-bounce I3
4th CK	4	De-bounce I4
5th CK	5	De-bounce I5
6th CK	6	De-bounce I6
7th CK	7	De-bounce I7
8th CK	0	De-bounce I0
9th CK	1	De-bounce I1

Serial mode RST and CK and DO timing (the value is minimum)



5. Key on duration time

OPT1	OPT0	On duration time
1	1	Infinite(disable Key-on-time)
1	0	7 seconds to reset system
0	1	22 seconds to reset system
0	0	44 seconds to reset system

When enable key-on-time, any key of the I0~I7 keys has been detected, it will start the key-on-time counter until releasing key-touch. And for the duration has another key to be detected, the key-on-time counter will be re-counting.

6. Sensitivity select and Base-step select and Windows of sensitivity select

a. The windows of sensitivity select by OPW0 & OPW1 pins. When the windows of sensitivity is selected, and the key has detected, the condition for detecting different number will change from primitive setting numbers to smaller. So the doing will make the key touch detecting stably.

OPW1	OPW0	Windows selecting
1	1	No-windows
1	0	1/2-windows
0	1	1/4-windows
0	0	1/8-windows

b. The selecting base-step of sensitivity

OPST	Base-step
1	1-step(1 sensor-clock)
0	2-step(2 sensor-clock)

c. Sensitivity selecting
The key detecting condition is the value (different clock numbers) of No-windows for detecting from no-touching to touching. When the key has been detected, the condition of key detecting and releasing will change to the value of selecting windows for the windows enabling.

Sensitivity table

Pin SLSE[5~0]						The different clock numbers(△_CLK)							
						1-base-step				2-base-step			
5	4	3	2	1	0	No-W	1/2-W	1/4-W	1/8-W	No-W	1/2-W	1/4-W	1/8-W
1	1	1	1	1	1	1	-	-	-	2	-	-	-
1	1	1	1	1	0	2	1	1	1	4	2	2	2
1	1	1	1	0	1	3	1	2	2	6	2	4	4
1	1	1	1	0	0	4	2	3	3	8	4	6	6
1	1	1	0	1	1	5	2	3	4	10	4	6	8
1	1	1	0	1	0	6	3	4	5	12	6	8	10
1	1	1	0	0	1	7	3	5	6	14	6	10	12
1	1	1	0	0	0	8	4	6	7	16	8	12	14
1	1	0	1	1	1	9	4	6	7	18	8	12	14
1	1	0	1	1	0	10	5	7	8	20	10	14	16
1	1	0	1	0	1	11	5	8	9	22	10	16	18
1	1	0	1	0	0	12	6	9	10	24	12	18	20
1	1	0	0	1	1	13	6	9	11	26	12	18	22
1	1	0	0	1	0	14	7	10	12	28	14	20	24
1	1	0	0	0	1	15	7	11	13	30	14	22	26
1	1	0	0	0	0	16	8	12	14	32	16	24	28
1	0	1	1	1	1	17	8	12	14	34	16	24	28
1	0	1	1	1	0	18	9	13	15	36	18	26	30
1	0	1	1	0	1	19	9	14	16	38	18	28	32
1	0	1	1	0	0	20	10	15	17	40	20	30	34
1	0	1	0	1	1	21	10	15	18	42	20	30	36
1	0	1	0	1	0	22	11	16	19	44	22	32	38
1	0	1	0	0	1	23	11	17	20	46	22	34	40
1	0	1	0	0	0	24	12	18	21	48	24	36	42
1	0	0	1	1	1	25	12	18	21	50	24	36	42
1	0	0	1	1	0	26	13	19	22	52	26	38	44
1	0	0	1	0	1	27	13	20	23	54	26	40	46
1	0	0	1	0	0	28	14	21	24	56	28	42	48
1	0	0	0	1	1	29	14	21	25	58	28	42	50
1	0	0	0	1	0	30	15	22	26	60	30	44	52
1	0	0	0	0	1	31	15	23	27	62	30	46	54
1	0	0	0	0	0	32	16	24	28	64	32	48	56
0	1	1	1	1	1	33	16	24	28	66	32	48	56
0	1	1	1	1	0	34	17	25	29	68	34	50	58
0	1	1	1	0	1	35	17	26	30	70	34	52	60
0	1	1	1	0	0	36	18	27	31	72	36	54	62
0	1	1	0	1	1	37	18	27	32	74	36	54	64
0	1	1	0	1	0	38	19	28	33	76	38	56	66
0	1	1	0	0	1	39	19	29	34	78	38	58	68
0	1	1	0	0	0	40	20	30	35	80	40	60	70
0	1	0	1	1	1	41	20	30	35	82	40	60	70
0	1	0	1	1	0	42	21	31	36	84	42	62	72
0	1	0	1	0	1	43	21	32	37	86	42	64	74
0	1	0	1	0	0	44	22	33	38	88	44	66	76
0	1	0	0	1	1	45	22	33	39	90	44	66	78
0	1	0	0	1	0	46	23	34	40	92	46	68	80
0	1	0	0	0	1	47	23	35	41	94	46	70	82
0	1	0	0	0	0	48	24	36	42	96	48	72	84
0	0	1	1	1	1	49	24	36	42	98	48	72	84
0	0	1	1	1	0	50	25	37	43	100	50	74	86
0	0	1	1	0	1	51	25	38	44	102	50	76	88
0	0	1	1	0	0	52	26	39	45	104	52	78	90
0	0	1	0	1	1	53	26	39	46	106	52	78	92
0	0	1	0	1	0	54	27	40	47	108	54	80	94
0	0	1	0	0	1	55	27	41	48	110	54	82	96
0	0	1	0	0	0	56	28	42	49	112	56	84	98
0	0	0	1	1	1	57	28	42	49	114	56	84	98
0	0	0	1	1	0	58	29	43	50	116	58	86	100
0	0	0	1	0	1	59	29	44	51	118	58	88	102
0	0	0	1	0	0	60	30	45	52	120	60	90	104
0	0	0	0	1	1	61	30	45	53	122	60	90	106
0	0	0	0	1	0	62	31	46	54	124	62	92	108
0	0	0	0	0	1	63	31	47	55	126	62	94	110
0	0	0	0	0	0	64	32	48	56	128	64	96	112

7. Option pin

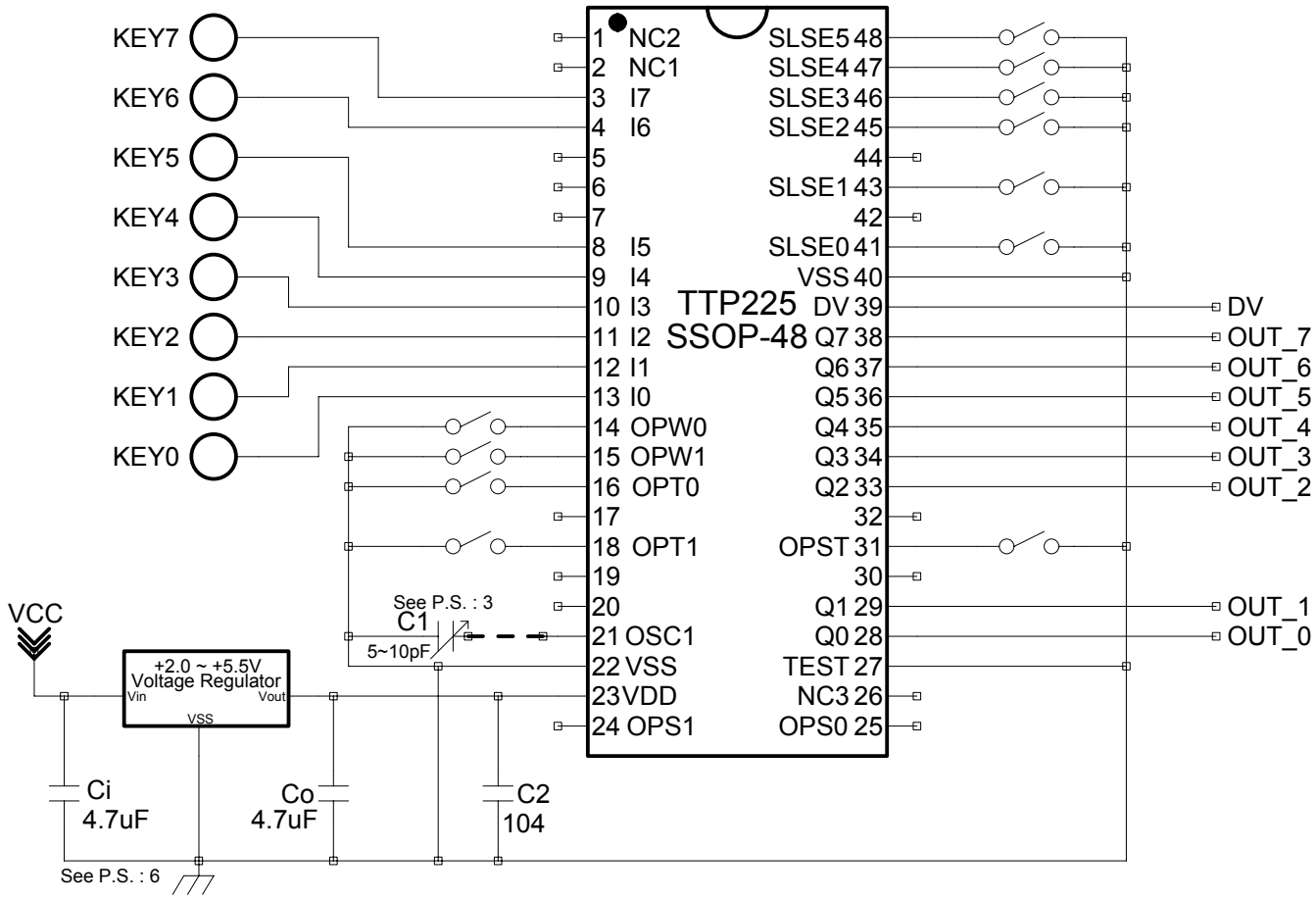
For power saving concern and package bonding option consideration, all the feature option pin with latch type design and initialized as 1 as power on. If those pins are forced to VSS, the states will be changed to 0 without any current leakage to conflict the power saving issue.

Feature option pins	Initial state by Power on
OPW0	1
OPW1	1
OPT0	1
OPT1	1
OPS1	1
OPS0	1
OPST	1
SLSE0~SLSE5 sensitivity	111111

APPLICATION CIRCUIT

a. For direct mode

APPLICATION FOR DIRECT KEY OUTPUT MODE

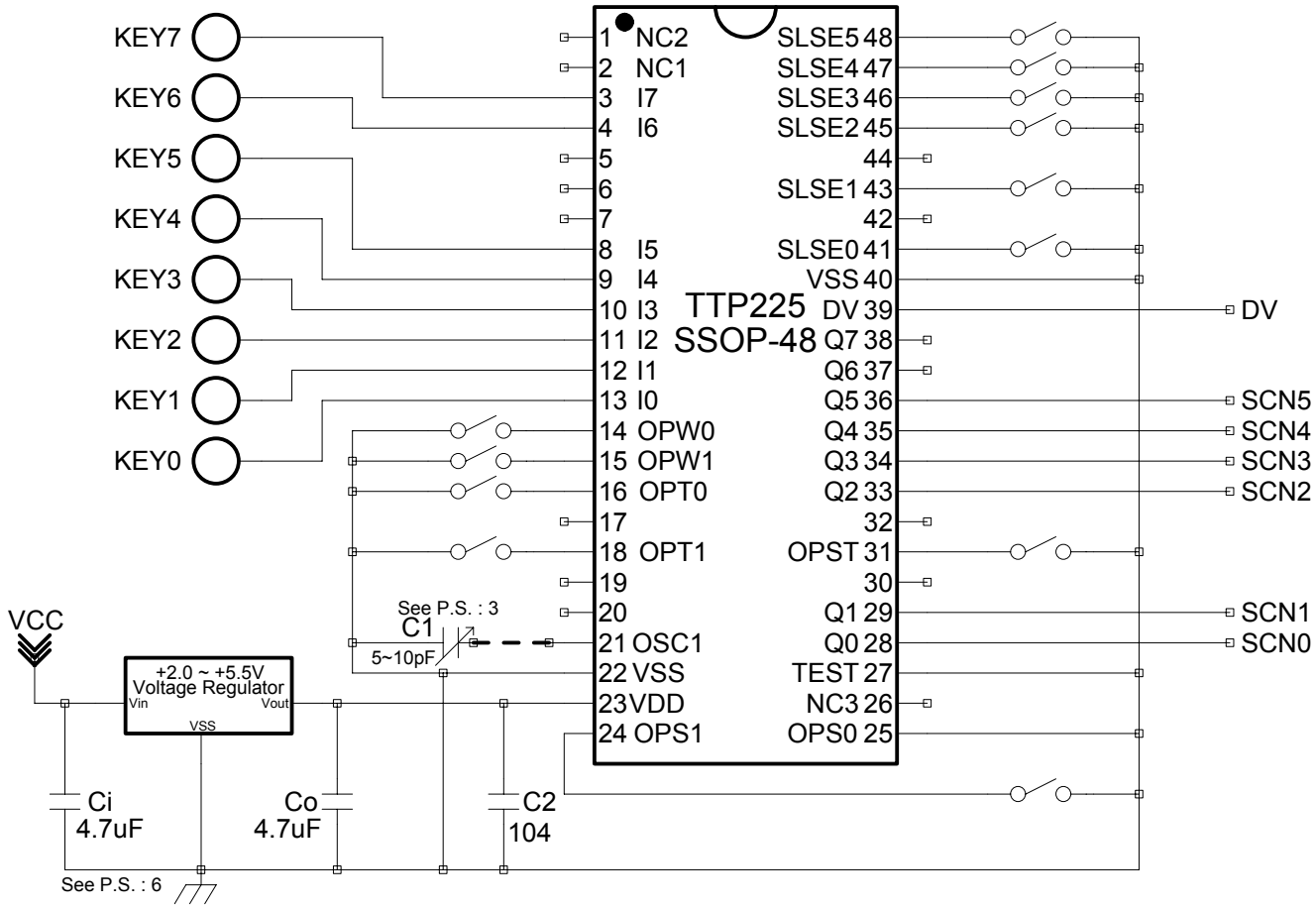


P.S.：1. On PCB, the length of lines from touch pad to IC pins are best the same with K0 to K7. And the lines do not parallel and cross with other lines.

2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. On OSC1 pin adding the C1 capacitor can adjust the system frequency, it will affect the output refresh rate, power-on stable-time, DV pulse width, and key-on duration time.
4. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
5. The C2 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP225).
6. The value of capacitors can be used by the real application for Ci and Co capacitors.

b. For matrix key mode

APPLICATION FOR MATRIX KEY OUTPUT MODE

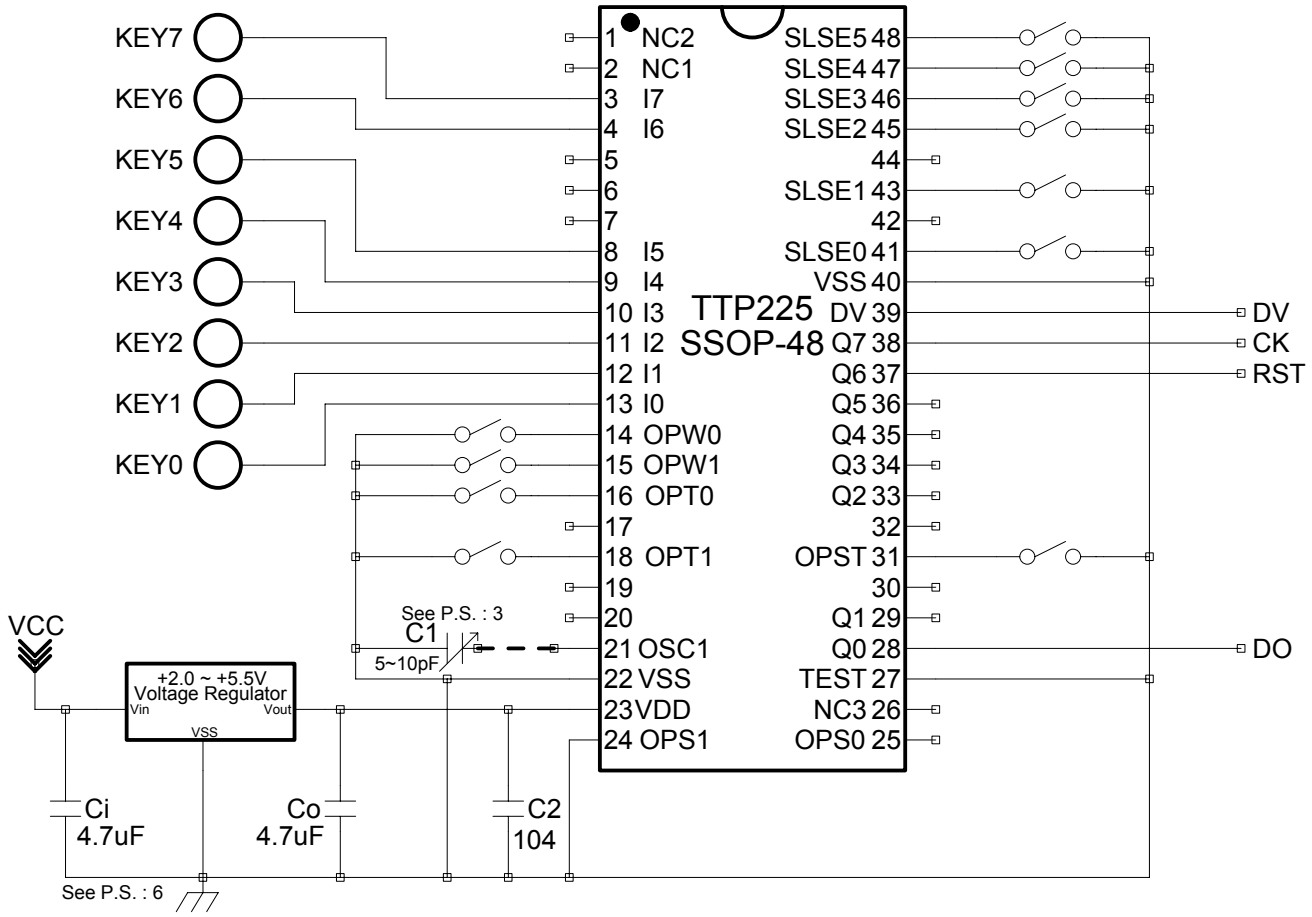


P.S.：1. On PCB, the length of lines from touch pad to IC pins are best the same with K0 to K7. And the lines do not parallel and cross with other lines.

2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. On OSC1 pin adding the C1 capacitor can adjust the system frequency, it will affect the output refresh rate, power-on stable-time, DV pulse width, and key-on duration time.
4. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
5. The C2 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP225).
6. The value of capacitors can be used by the real application for Ci and Co capacitors.

c. For serial output mode

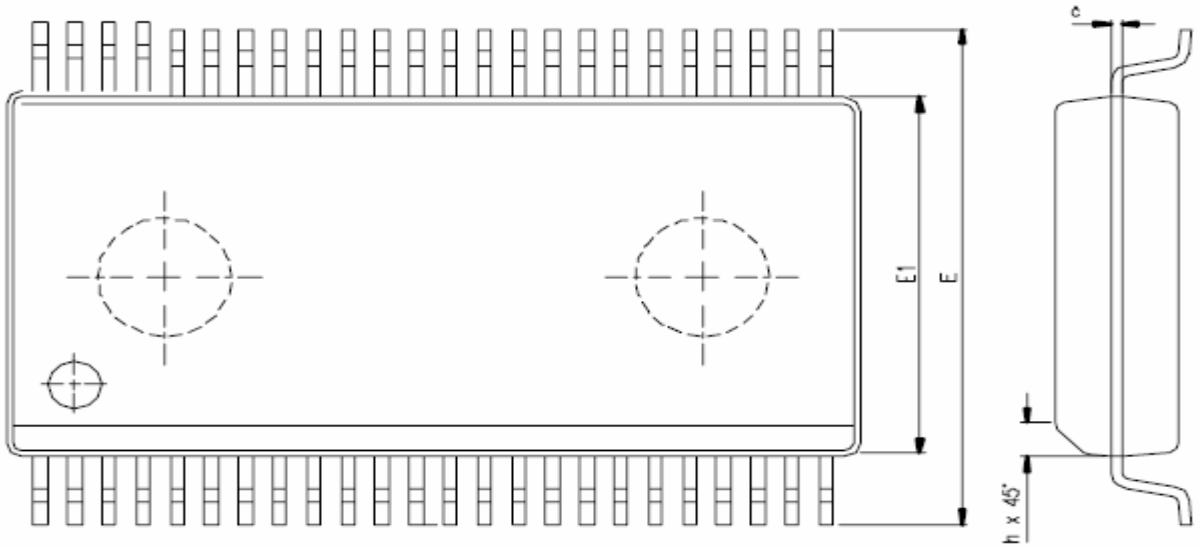
APPLICATION FOR SERIAL OUTPUT MODE

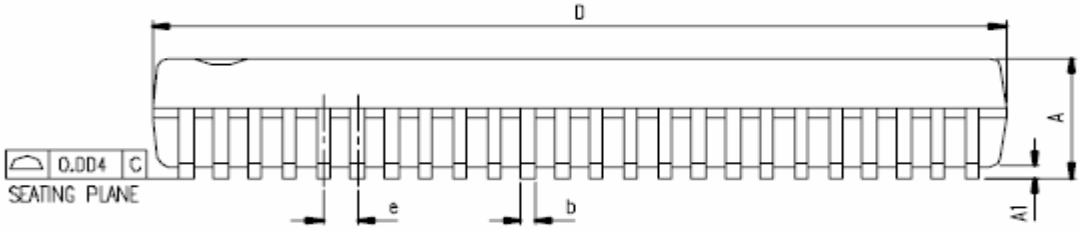


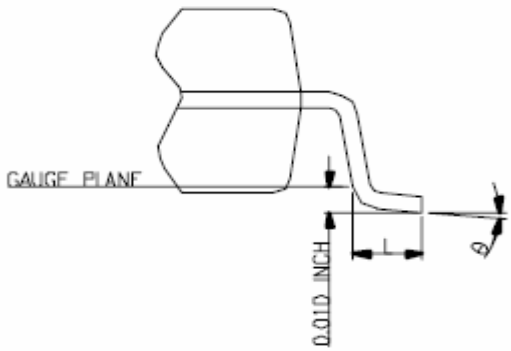
P.S.：1. On PCB, the length of lines from touch pad to IC pins are best the same with K0 to K7. And the lines do not parallel and cross with other lines.

2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. On OSC1 pin adding the C1 capacitor can adjust the system frequency, it will affect the output refresh rate, power-on stable-time, DV pulse width, and key-on duration time.
4. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
5. The C2 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP225).
6. The value of capacitors can be used by the real application for Ci and Co capacitors.

PACKAGE OUTLINE (48 PIN SSOP)







REV.	DESCRIPTION	BY	DATE
ORG.	DRAWING ISSUE	SANDY CHEN	97.11.04
A	MODIFY E-PIN	SANDY CHEN	97.12.05
B	ADD NOTES	SANDY CHEN	00.01.19

*NOTES : DIMENSION " D " DONE NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 INCH (0.1524 MM) PER SIDE.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.0135
c	0.127		0.254	0.005		0.010
e	0.635 BASIC			0.025 BASIC		
E	10.033		10.668	0.395		0.420
E1	7.391	7.493	7.595	0.291	0.295	0.299
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
θ	0		8	0		8

N	D DIMENSION (IN INCH)			JEDEC
48	0.620	0.625	0.630	MO-118 (AA)
56	0.720	0.725	0.730	MO-118 (AB)

TTP225 VS TTP222 Compare list:

Item	TTP225	TTP222
Output:Q0~Q7	Open drain(active low)	Digital output (active high or low by AHL pin option)
Power on stable-time	About 0.5~0.7sec	About 3.5~4sec
AHL pin	X	V
OSC2, TOPAD pin	X	V

ORDER INFORMATION

a. Package form: TTP225-XXX
b. Chip form: TCP225
c. Wafer base: TDP225

REVISE HISTORY

1. 2007/12/13
 -Original version： V_1.0
2. 2008/06/10 => V_1.1
 -Change the Page-1 APPLICATION.
 -Change the Page-2, 3 BLOCK DIAGRAM I/O mark.
 -Add the Page-4 the PIN TYPE description.
 -Change the Page-11, 12, 13 APPLICATION CIRCUIT.
 -Add the Page-15 the ORDER INFORMATION and REVISE HISTORY.
3. 2008/07/10 => V_1.2
 -Add the Page-1 Features.
 => · Auto calibration for life. ……
4.2009/08/25 => V1.3
 -於頁首加註 Ton Touch商標，於右邊加「Ton Touch ™」
 -於General Description 內容裡TTP225後加「Ton Touch ™」