§ PATENTEN

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP250 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1K-word ROM、64-nibble RAM、timer/Counter、interrupt service 、IO control hardware、LVR and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1K*16 program ROM and 64*4 SRAM
6. 2-level stacks
7. Operating voltage:3.5V~5.5V(LVR=ON); 2.2V~5.5V (LVR OFF)
8. System operating frequency: (at VDD=5V)
   . High-speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 4MHz(typical)

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Offer 8 IO+8 touch pad or 16 general programmable I/O
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs

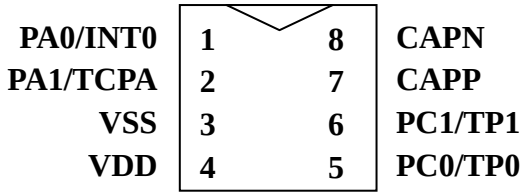
- ✧ Offering internal signal outputs, like buzzer(PFD)

10. One 8-bit TCP1 auto-reload timer/counter & one time base counter
    - ✧ 4 timer clock sources selected by software
    - ✧ Timer provides the PFD feature for Buzzer output driver
    - ✧ Time base offers 2 various period interrupt request
11. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep、stop mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
12. 8 pins with touch pad detection
13. Provides 5 interrupt sources
    - ✧ External: INT0 shared with IO pad
    - ✧ Internal: Timer/counter, Time base timer
    - ✧ Two touchpad's interrupt
14. Provide package types
    - ✧ TSSOP 20/SSOP 16/ SOP 8

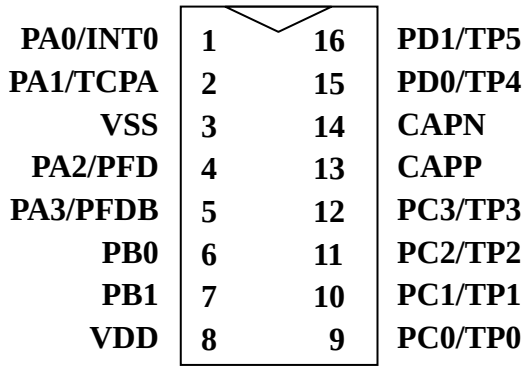
§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

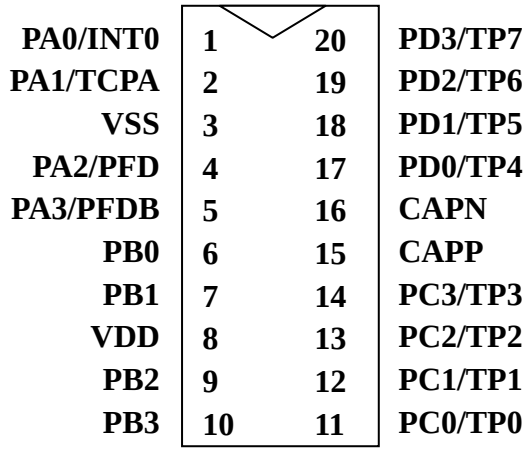
§ Package Description:



8-SOP-A(TTP250-NO8)

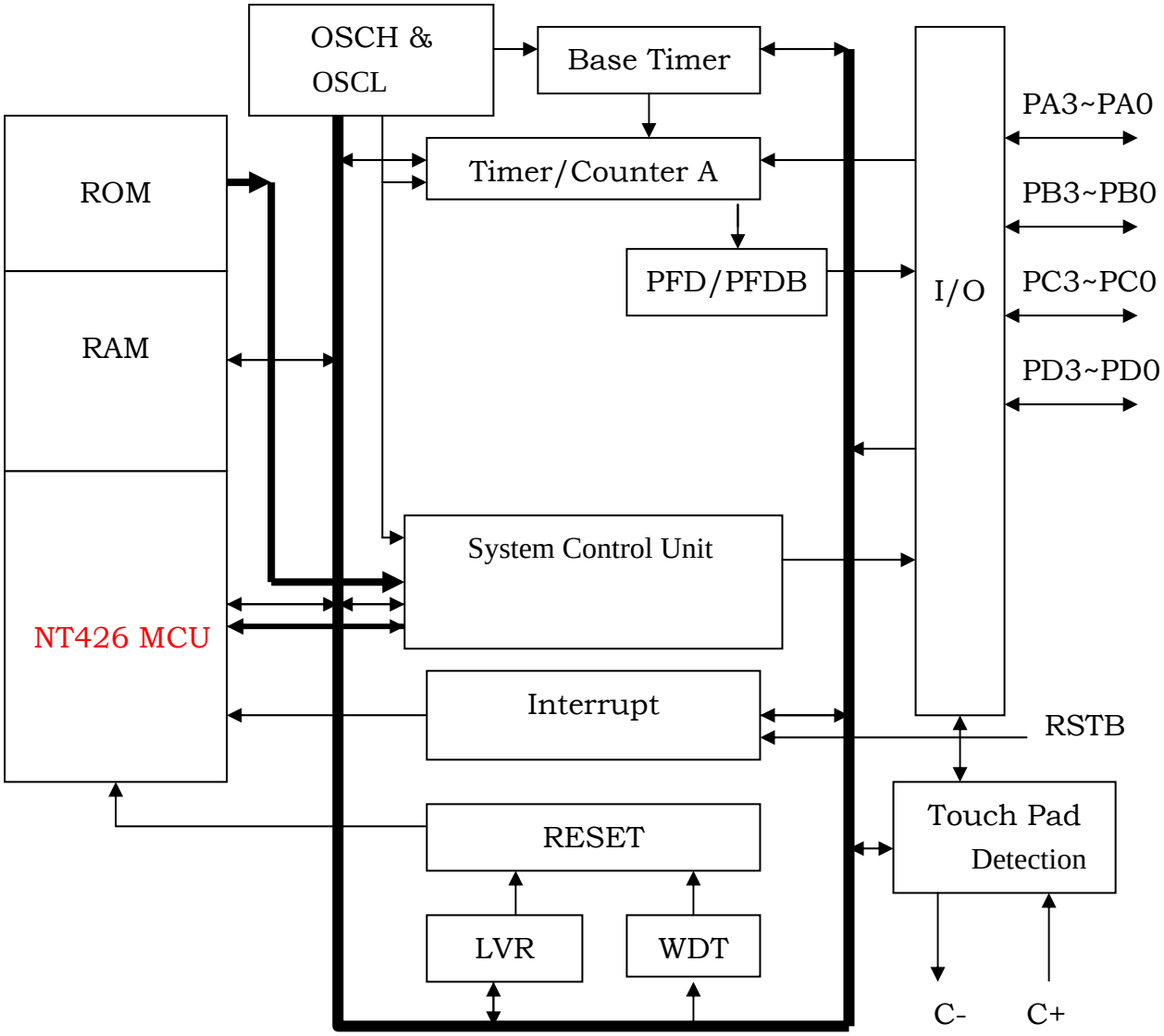


16-SSOP-A (TTP250-NSB)



20-TSSOP-A (TTP250-NTD)

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
V_{DD}	-	Power	+1	-	Positive power supply
V_{SS}	-	Power	+1	-	Negative power supply, ground
RSTB	-	I	+1	-	External reset input, active low, 50kΩ pull-up(V_{DD} =5v)
PA0(INT0) PA1(TCPA) PA2(PFD) PA3(PFDB)	Vpp	IO IO IO IO	+4	-	I/O port with external interrupt input (PA0). PA1 is used as clock inputs of timer/counter A .PA2&PA3 are shared with internal PFD output
PB0~PB3	-	IO	+4	-	I/O port with internal signal output
PC0 PC1 PC2 PC3	TP0 TP1 TP2 TP3	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
PD0 PD1 PD2 PD3	TP4 TP5 TP6 TP7	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
C+	-	I	+1	-	Touch sensor input
C-	-	O	+1	-	Touch signal output with pull up R
			21	-	

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA1	Figure IO-A	STD IO with external input
PA2~PA3	Figure IO-B	STD IO with internal output
PB0~PB3	Figure IO-C	STD IO
PC0~PC3	Figure IO-A	STD IO with external input
PD0~PD3	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃ ~ +70℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~ VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>3	KV
Note: VSS symbolizes for system ground			

DC & AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=4MHz LVR on	3.5	-	5.5	V
		LVR off	2.2	-	5.5	
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	2.5	3.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	0.7	1.0	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	5	10	uA
Standby Current	I_{STB}	I/O no load, FOSCH & FOSCL stop	-	-	1.0	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RSTB & INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RSTB & INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD
PA0 Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-1	-	mA
Output port Sink Current (exclude PA0)	I_{OL}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current (exclude PA0)	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-4	-	mA
I/O Port Pull-up Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RSTB Pull-up Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	LVREN ON	2.1	3.0	3.5	V

§ AC Characteristics:

Parameter	Test Condition		Min.	Typ.	Max.	Unit
External Reset	Low active pulse width tRES		2	-	-	CPU clock
Interrupt input	Low active pulse width tINT		2	-	-	
Wake up input	Low active pulse width $t_{wkup,}$ Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=2.2~5.0V	-	16K	-	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	F_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	F_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH & OSCH off	8	-	-	F_{OSCH}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL & OSCL on	8	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

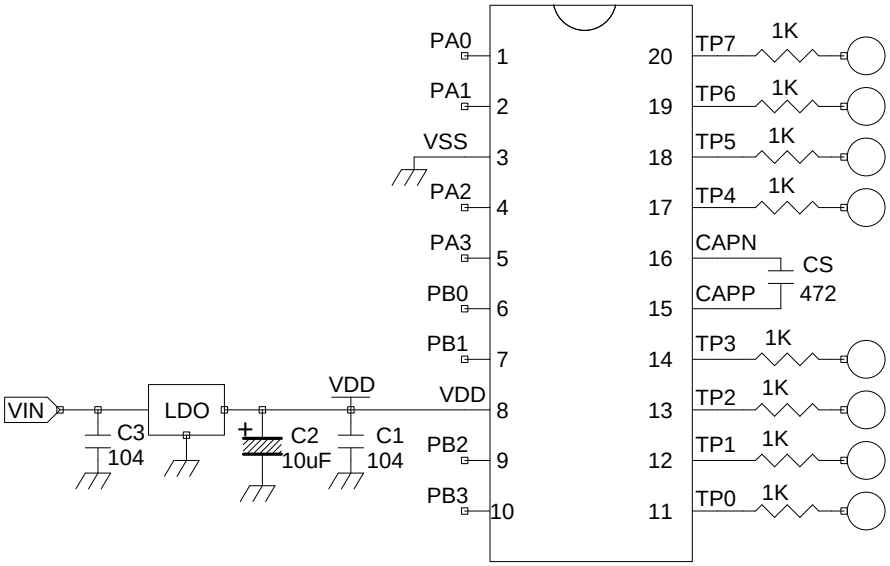
§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$3FF_H$	-	Program ROM [1K*16]
-	000_H ~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$05F_H$	Working RAM [64*4]
-	120_H~$12A_H$	Peripheral registers (II)

§ Interrupt Vectors:

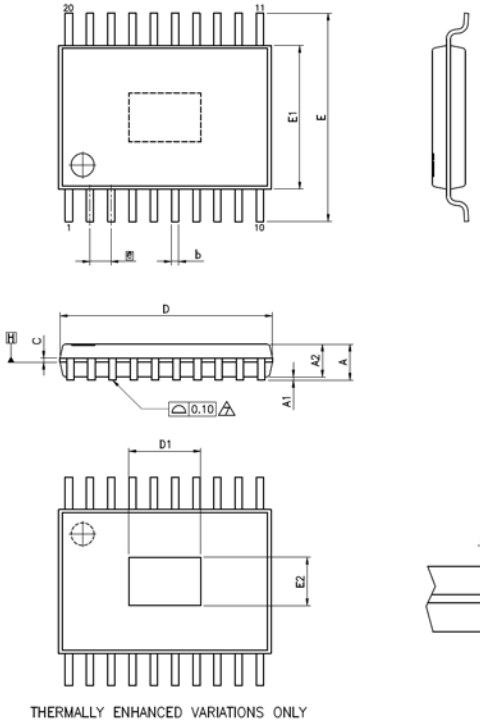
Interrupt Vectors	Function Description
$000	hardware RESET
$001	Hardware IRQ

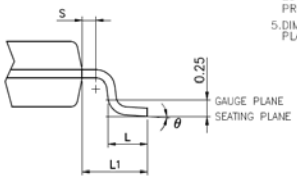
§ Application Circuit



§ Package Information:

- **TSSOP 20**





VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

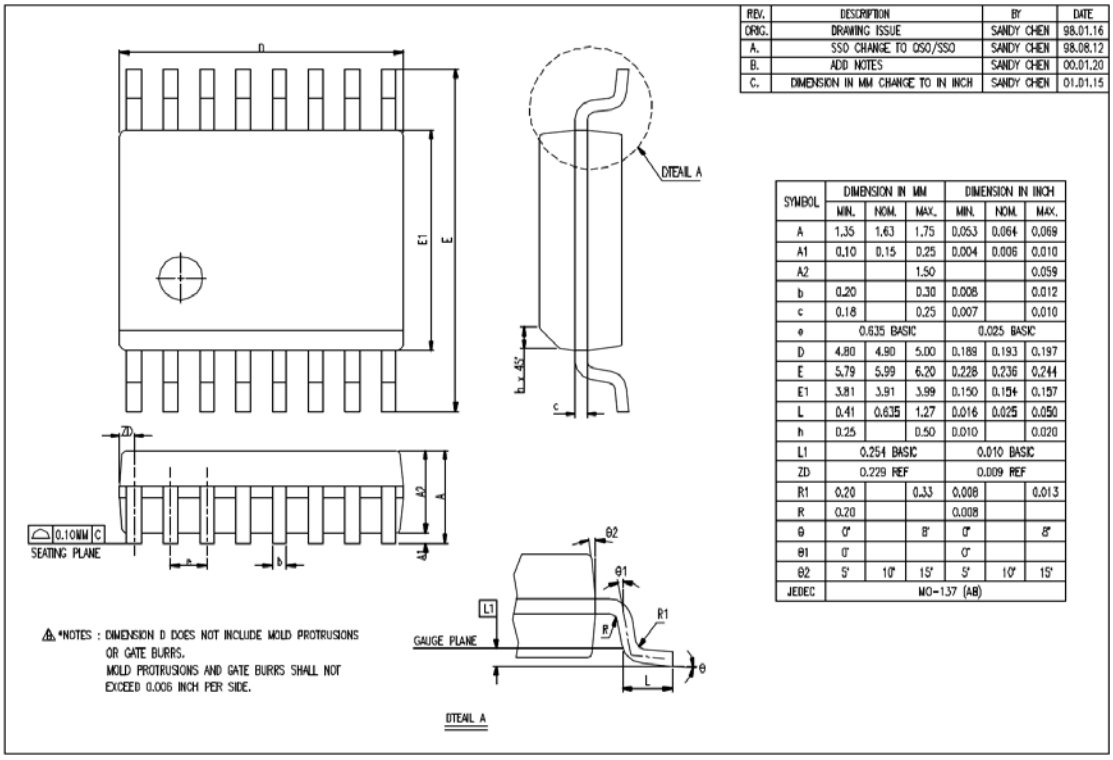
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2			D1		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
118X16E	2.60	2.80	3.00	3.79	3.99	4.19

NOTES:
1. JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

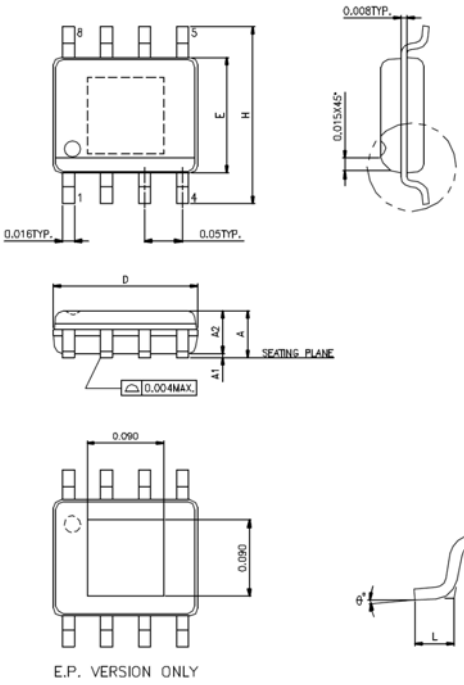
- **SSOP 16**



REV.	DESCRIPTION	BY	DATE
ORIG.	DRAWING ISSUE	SANDY CHEN	98.01.16
A.	SSO CHANGE TO OSO/SSO	SANDY CHEN	98.08.12
B.	ADD NOTES	SANDY CHEN	00.01.20
C.	DIMENSION IN MM CHANGE TO IN INCH	SANDY CHEN	01.01.15

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
b	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
L1	0.254 BASIC			0.010 BASIC		
ZD	0.229 REF			0.009 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AB)					

- **SOP 8**



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

§ Ordering Form:

	Package type
TTP250-NTD	**20-TSSOP-A**
TTP250-NSB	**16-SSOP-A**
TTP250-NO8	**8-SOP-A**

Modified Record:

Body:

2007/11/16:

- New build