TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

TENTATIVE

Pseudo SRAM and NOR Flash Memory Mixed Multi-Chip Package

DESCRIPTION

The TV00570002/003CDGB is a mixed multi-chip package containing a 33,554,432-bit pseudo static RAM and a 134,217,728-bit Nor Flash Memory. The TV00570002/003CDGB is available in a 81-pin BGA package making it suitable for a variety of applications.

MCP Features

- Power supply voltage of 2.7 to 3.3 V
- Operating temperature of –30° to 85°C
- Package
  P-TFBGA81-0710-0.80BZ (Weight: 0.15 g)

Pseudo SRAM Features

- Organization : 2M × 16 bits
- Power dissipation
  Operating : 40 mA maximum
  Standby : 150 μA maximum
  Deep power-down standby : 5 μA maximum
- Access time :
  Random / Page : 70 ns / 30 ns @CL=30pF
- Page read operation by 8 words
- Deep power-down mode : Memory cell data invalid

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Nor Flash Memory Features

- Organization: 8M × 16 bits
- Power dissipation
  Read operating : 55 mA maximum
  Address Increment Read operation: 24mA maximum
  Page Read operating : 5 mA maximum
  Program / Erase operating: 15 mA maximum
  Standby : 10 μA maximum
- Access time :
  Random : 70 ns @CL=30pF
  Page : 25 ns @CL=30pF
- Functions
  Simultaneous Read/Write
  Page read
  Auto-Program , Auto Page Program
  Auto Block Erase , Auto Chip Erase
  Program Suspend / Resume
  Erase Suspend/Resume
  Data polling / Toggle bit
  Password block protection
  Block Protection/Boot Block Protection
  Automatic Sleep, supports for hidden ROM Area
  Common Flash Memory Interface (CFI)
- Block erase architecture
  8 × 8 Kbytes / 127 × 64 Kbytes
- Bank architecture
  16 Mbits × 8 Banks
- Boot block architecture
  TV00570002CDGB : top boot block
  TV00570003CDGB : bottom boot block
- Mode control
  Compatible with JEDEC standard commands
- Erase/Program cycles
  100,000 cycles typ.

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PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8
A	NC							NC
B	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	A7	$\overline{LB}$	$\overline{WP}$/ACC	$\overline{WE}$	A8	A11	
D	A3	A6	$\overline{UB}$	$\overline{RESET}$	CE2ps	A19	A12	A15
E	A2	A5	A18	RY/ $\overline{BY}$ f	A20	A9	A13	A21
F	A1	A4	A17	NC	NC	A10	A14	A22
G	A0	V_{SS}	DQ1	NC	NC	DQ6	NC	A16
H	$\overline{CEf}$	$\overline{OE}$	DQ9	DQ3	DQ4	DQ13	DQ15	NC
J	$\overline{CE1ps}$	DQ0	DQ10	V_{CCf}	V_{CCps}	DQ12	DQ7	V_{SS}
K		DQ8	DQ2	DQ11	NC	DQ5	DQ14	
L	NC	NC	NC	NC	NC	NC	NC	NC
M	NC							NC

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PIN NAMES

A0 to A22	Address inputs
DQ0 to DQ15	Data inputs / outputs
$\overline{CE1ps}$, CE2ps	Chip enable inputs for Pseudo SRAM
$\overline{CEf}$	Chip enable inputs for Nor Flash Memory
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{LB}$, $\overline{UB}$	Data byte control inputs for Pseudo SRAM
$\overline{WP}$/ACC	Write protect /program acceleration input for Nor Flash Memory
$\overline{RESET}$	Hardware reset input for Nor Flash Memory
RY/ $\overline{BY}$ f	Ready/Busy output for Nor Flash Memory
V_{CCps}	Power supply for Pseudo SRAM
V_{CCf}	Power supply for Nor Flash Memory
V_{SS}	Ground
NC	Not connected

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PIN NAME CONVERSION TABLE

MCP Pin		32M	128M
Location	Name	PSRAM	Nor
A1	NC	–	–
A2	–	–	–
A3	–	–	–
A4	–	–	–
A5	–	–	–
A6	–	–	–
A7	–	–	–
A8	NC	–	–
B1	NC	–	–
B2	NC	–	–
B3	NC	–	–
B4	NC	–	–
B5	NC	–	–
B6	NC	–	–
B7	NC	–	–
B8	NC	–	–
C1	NC	–	–
C2	A7	A7	A7
C3	$\overline{LB}$	$\overline{LB}$	–
C4	$\overline{WP}$/ACC		$\overline{WP}$/ACC
C5	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
C6	A8	A8	A8
C7	A11	A11	A11
C8	–	–	–
D1	A3	A3	A3
D2	A6	A6	A6
D3	$\overline{UB}$	$\overline{UB}$	–
D4	$\overline{RESET}$	–	$\overline{RESET}$
D5	CE2ps	CE2	–
D6	A19	A19	A19
D7	A12	A12	A12
D8	A15	A15	A15
E1	A2	A2	A2
E2	A5	A5	A5
E3	A18	A18	A18
E4	$\overline{RY/BY}$ f	–	$\overline{RY/BY}$
E5	A20	A20	A20
E6	A9	A9	A9
E7	A13	A13	A13
E8	A21	–	A21
F1	A1	A1	A1
F2	A4	A4	A4
F3	A17	A17	A17
F4	NC	–	–
F5	NC	–	–
F6	A10	A10	A10
F7	A14	A14	A14
F8	A22	–	A22

MCP Pin		32M	128M
Location	Name	SRAM	Nor
G1	A0	A0	A0
G2	V_{SS}	GND	V_{SS}
G3	DQ1	I/O2	DQ1
G4	NC	–	–
G5	NC	–	–
G6	DQ6	I/O7	DQ6
G7	NC	–	–
G8	A16	A16	A16
H1	$\overline{CEf}$	–	$\overline{CE}$
H2	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
H3	DQ9	I/O10	DQ9
H4	DQ3	I/O4	DQ3
H5	DQ4	I/O5	DQ4
H6	DQ13	I/O14	DQ13
H7	DQ15	I/O16	DQ15
H8	NC	–	–
J1	$\overline{CE1ps}$	$\overline{CE1}$	
J2	DQ0	I/O1	DQ0
J3	DQ10	I/O11	DQ10
J4	V_{CCf}	–	V_{CC}
J5	V_{CCps}	V_{DD}	–
J6	DQ12	I/O13	DQ12
J7	DQ7	I/O8	DQ7
J8	V_{SS}	GND	V_{SS}
K1	–	–	–
K2	DQ8	I/O9	DQ8
K3	DQ2	I/O3	DQ2
K4	DQ11	I/O12	DQ11
K5	NC	NC	NC
K6	DQ5	I/O6	DQ5
K7	DQ14	I/O15	DQ14
K8	–	–	–
L1	NC	–	–
L2	NC	–	–
L3	NC	–	–
L4	NC	–	–
L5	NC	–	–
L6	NC	–	–
L7	NC	–	–
L8	NC	–	–
M1	NC	–	–
M2	–	–	–
M3	–	–	–
M4	–	–	–
M5	–	–	–
M6	–	–	–
M7	–	–	–
M8	NC	–	–

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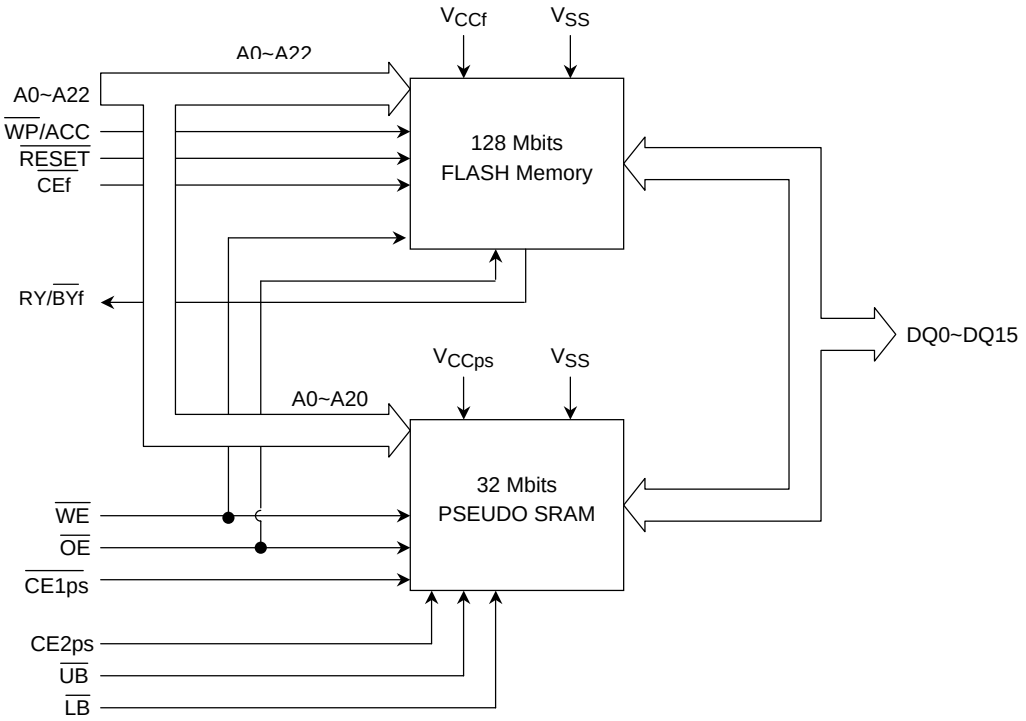
BLOCK DIAGRAM



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MODE SELECTION

Pseudo SRAM

MODE	$\overline{CE1ps}$	CE2ps	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Add	DQ0~DQ7	DQ8~DQ15
Read(Word)	L	H	L	H	L	L	X	D_{OUT}	D_{OUT}
Read(Lower Byte)					L	H		D_{OUT}	High-Z
Read(Upper Byte)					H	L		High-Z	D_{OUT}
Write(Word)			X	L	L	L		D_{IN}	D_{IN}
Write(Lower Byte)					L	H		D_{IN}	Invalid
Write(Upper Byte)					H	L		Invalid	D_{IN}
Outputs Disabled			H	H	X	X		High-Z	High-Z
Standby	H	H	X	X	X	X		High-Z	High-Z
Deep Power-down Standby	H	L	X	X	X	X		High-Z	High-Z

Nor Flash Memory

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MODE	$\overline{CEf}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$	DQ0~DQ15
Read / Page Read	L	L	H	H	X	D_{OUT}
Standby	H	X	X	H	X	High-Z
Output Disable	X	H	H	X	X	High-Z
Write	L	H	⎍(1)	H	X	D_{IN}
Hardware Reset / Standby	X	X	X	L	X	High-Z
Boot Block Protect	X	X	X	X	L	X

Notes: L = V_{IL}; H = V_{IH}; X = V_{IH} or V_{IL}

Does not apply when $\overline{CEf}$ = V_{IL} and $\overline{CE1ps}$ = V_{IL} and CE2ps = V_{IH} at the same time.

(1) Pulse input

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ID CODE TABLE

TYPE		A22~A12	A6	A1	A0	CODE (HEX)
Manufacturer Code		*	L	L	L	0098H
Device Code	TV00570002CDGB	*	L	L	H	0003H
	TV00570003CDGB	*	L	L	H	0014H
Verify Block Protect		BA(1)	L	H	L	Data(2)

Note: * = V_{IH} or V_{IL} , L = V_{IL} H = V_{IH}

(1) BA: Block address

(2) 0001H: Protected block , 0000H: Unprotected block

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{CC}	V_{CCps}/V_{CCf} Power Supply Voltage	−0.6~3.6(4)	V
V_{IN}	Input Voltage(1)	−0.6~3.6	V
V_{DQ}	Input/Output Voltage	−0.5~V_{CC} + 0.5 (≤ 3.6)	V
V_{ACC}	Maximum Input Voltage for $\overline{WP}$/ACC (2)	13.0	V
T_{opr}	Operating Temperature	−30~85	°C
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature	260	°C
I_{OSHORT}	Output Short Circuit Current(3)	100	mA
T_{stg}	Storage Temperature	−55~125	°C

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Note : (1) −1.0 V for pulse width ≤ 10 ns

(2) Do not apply VID/VACC when the supply voltage is not within the device's recommended operating voltage range

(3) Output shorted for no more than one second. No more than one output shorted at a time

(4) The potential difference of V_{CCps} and V_{CCf} is less than 0.5 V

RECOMMENDED DC OPERATING CONDITIONS (Ta = −30°~85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	V_{CCps}/V_{CCf} Power Supply Voltage	2.7(2)	—	3.3(2)	V
V_{IH}	Input High-Level Voltage	0.7 × V_{CC}	—	V_{CC} + 0.3	
V_{IL}	Input Low-Level Voltage	−0.3(1)	—	0.4	
V_{ACC}	High Voltage for $\overline{WP}$/ACC	8.5	—	12.6	

Note : (1) −1.0 V for pulse width ≤ 10 ns

(2) The potential difference of V_{CCps} and V_{CCf} is less than 0.5 V

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	—	—	17	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	—	—	22	pF

Note: These parameters are sampled periodically and are not tested for every device.

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DC CHARACTERISTICS (Ta = –30°~85°C, V_{CCps}/ V_{CCf} = 2.7 V~3.3 V)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{CCf} (V_{CCps})		—	±1	μA
I_{OHps}	Pseudo SRAM Output High Current	V_{OH} = V_{CCps} − 0.5 V		−0.5	—	mA
I_{OLps}	Pseudo SRAM Output Low Current	V_{OL} = 0.4 V		1.0	—	mA
I_{OHf1}	Flash Output High Current (TTL)	V_{OH} = 2.4 V		−0.4	—	mA
I_{OHf2}	Flash Output High Current (CMOS)	V_{OH} = V_{CCf} × 0.85		−2.5	—	mA
		V_{OH} = V_{CCf} − 0.4 V		−100	—	μA
I_{OLf}	Flash Output Low Current	V_{OL} = 0.4 V		4	—	mA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V~V_{CCf} (V_{CCps}), $\overline{OE}$ = V_{IH}		—	±1	μA
I_{CCO1f}	Flash Random Read Current	$\overline{CEf}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 100ns		—	55	mA
I_{CCO2f}	Flash Program Current	$\overline{CEf}$ = V_{IL}, I_{OUT} = 0 mA		—	15	mA
I_{CCO3f}	Flash Erase Current	$\overline{CEf}$ = V_{IL}, I_{OUT} = 0 mA		—	15	mA
I_{CCO4f}	Flash Read-While-Program Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 100 ns		—	70	mA
I_{CCO5f}	Flash Read-While- Erase Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 100 ns		—	70	mA
I_{CCO6f}	Flash Program-while- Erase-Suspend Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA		—	15	mA
I_{CCO7f}	Flash Page Read Current	$\overline{CEf}$ = V_{IL}, I_{OUT} = 0 mA , t_{RC} = 100 ns		—	5	mA
I_{CCO8f}	Flash Address Increment Read Current(4)	$\overline{CEf}$ = V_{IL}, I_{OUT} = 0 mA t_{RC} = 100 ns , t_{RPC} = 25 ns		—	24	mA
I_{CCO1ps}	Pseudo SRAM Operating Current(2,3)	$\overline{CE1ps}$ = V_{IL} , CE2ps = V_{IH}, I_{OUT} = 0 mA	t_{RC} = min	—	40	mA
I_{CCO2ps}	Pseudo SRAM Page Access Operating Current (2,3)	$\overline{CE1ps}$ = V_{IL}, CE2ps = V_{IH}, Page add. Cycling, I_{OUT} = 0 mA	t_{PC} = min	—	25	mA
I_{CCSps}	Pseudo SRAM Standby Current (MOS)	$\overline{CE1ps}$= V_{CCps} − 0.2 V, CE2ps = V_{CCps} − 0.2 V		—	150	μA
I_{CCSDps}	Pseudo SRAM Deep Power-down Standby Current	CE2ps = 0.2 V		—	5	μA
I_{CCS1f}	Flash Standby Current	$\overline{WP}$/ACC = V_{CCf} $\overline{CEf}$ = $\overline{RESET}$ = V_{CCf} or $\overline{RESET}$ = V_{SS}		—	10	μA
I_{CCS2f}	Flash Standby Current (Automatic Sleep Mode(1))	V_{IH} = V_{CCf} or V_{IL} = V_{SS}		—	10	μA
V_{LKO}	Low Voltage Lock-out Voltage	—		—	2.5	V

(1) The device is going to Automatic Sleep Mode, when address remain steady during 150 ns.

(2) I_{CCO} depends on the cycle time.

(3) I_{CCO} depends on output loading. Specified values are defined with the output open condition.

(4) (I_{CCO1f}+ I_{CCO7f} x 7)／8word

See page P-1 to page P-6 for the specification of Pseudo Static RAM.

See page F-1 to page F-47 for the specification of Nor Flash Memory.

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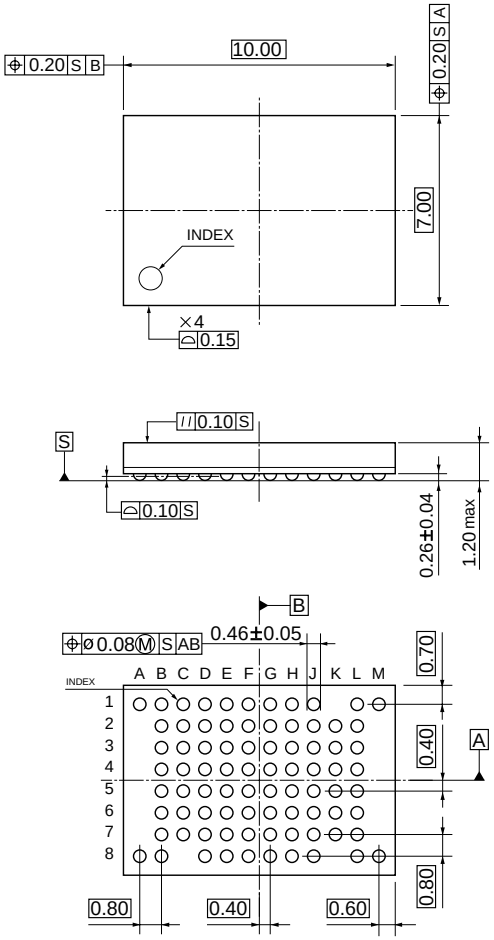
PACKAGE DIMENSIONS

P-TFBGA81-0710-0.80BZ Unit: mm



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32 Mbits PSEUDO STATIC RAM

TC51WHM516B

Organization : 2M × 16bits

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AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –30°C to 85°C, V_{DD} = 2.7 to 3.3 V) (See Note 1 to 7)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	70	10000	ns
t_{ACC}	Address Access Time	—	70	ns
t_{CO}	Chip Enable ($\overline{CE1}$) Access Time	—	70	ns
t_{OE}	Output Enable Access Time	—	25	ns
t_{BA}	Data Byte Control Access Time	—	25	ns
t_{COE}	Chip Enable Low to Output Active	10	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	Data Byte Control Low to Output Active	0	—	ns
t_{OD}	Chip Enable High to Output High-Z	—	20	ns
t_{ODO}	Output Enable High to Output High-Z	—	20	ns
t_{BD}	Data Byte Control High to Output High-Z	—	20	ns
t_{OH}	Output Data Hold Time	5	—	ns
t_{PM}	Page Mode Time	70	10000	ns
t_{PC}	Page Mode Cycle Time	30	—	ns
t_{AA}	Page Mode Address Access Time	—	30	ns
t_{AOH}	Page Mode Output Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	70	10000	ns
t_{WP}	Write Pulse Width	50	—	ns
t_{CW}	Chip Enable to End of Write	70	—	ns
t_{BW}	Data Byte Control to End of Write	60	—	ns
t_{AW}	Address Valid to End of Write	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{CEH}	Chip Enable High Pulse Width	10	—	ns
t_{WEH}	Write Enable High Pulse Width	6	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	20	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{CS}	CE2 Set-up Time	0	—	ns
t_{CH}	CE2 Hold Time	300	—	μs
t_{DPD}	CE2 Pulse Width	10	—	ms
t_{CHC}	CE2 Hold from $\overline{CE1}$	0	—	ns
t_{CHP}	CE2 Hold from Power On	30	—	μs

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AC TEST CONDITIONS

PARAMETER	CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V_{DD} – 0.2 V, 0.2 V
Timing measurements	V_{DD} × 0.5
Reference level	V_{DD}× 0.5
t_R, t_F	5 ns

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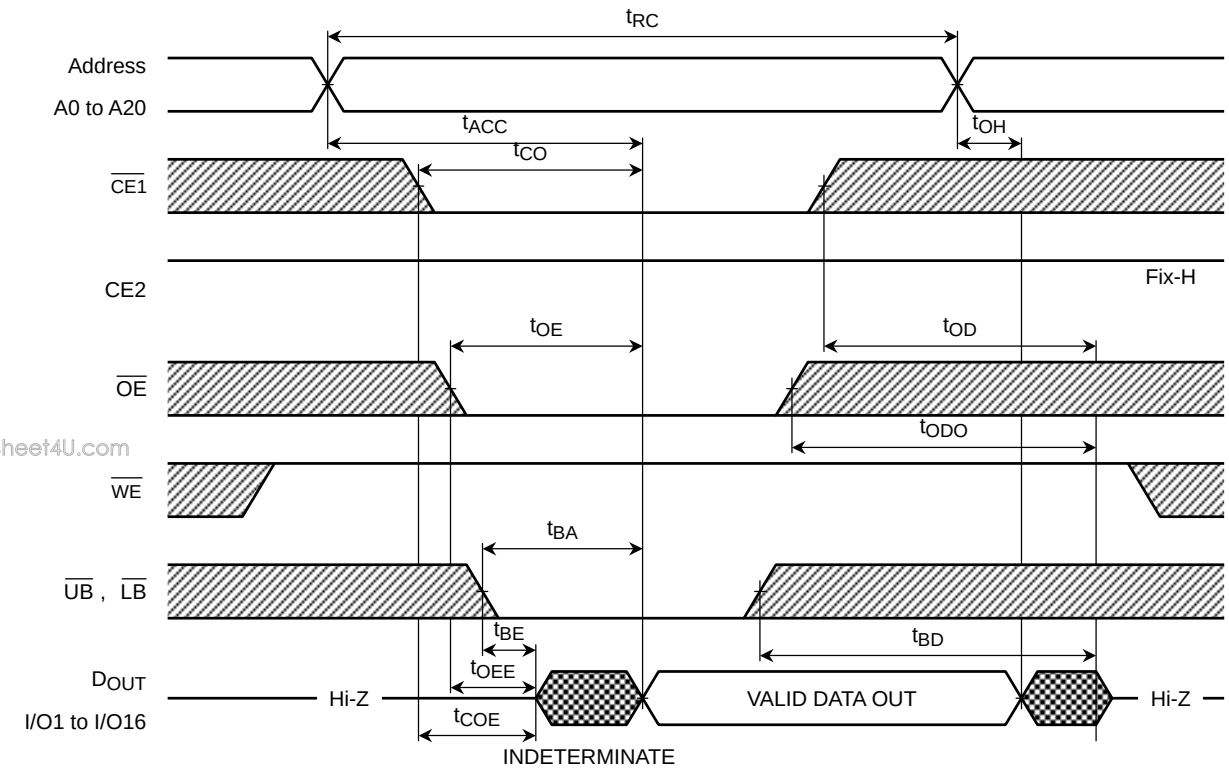
TIMING DIAGRAMS

READ CYCLE



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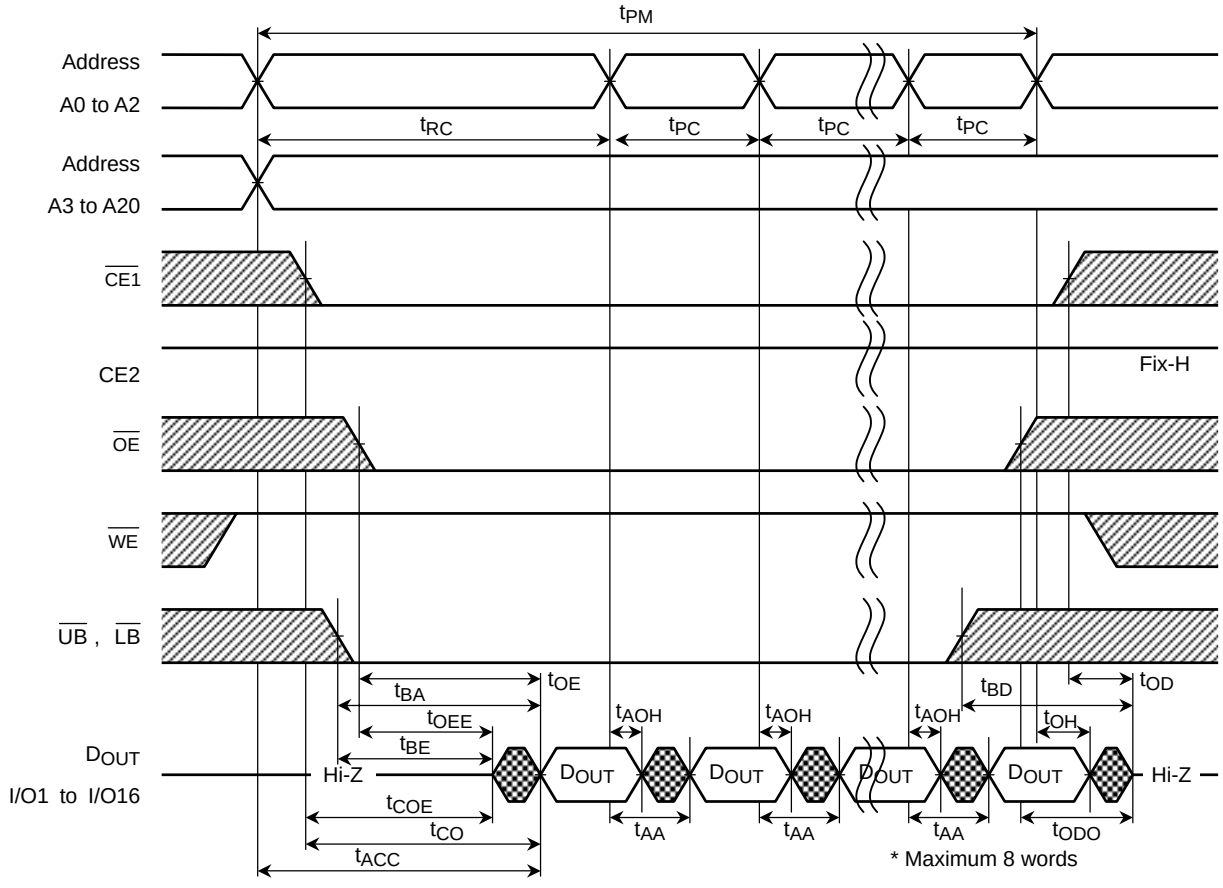
PAGE READ CYCLE (8 words access)



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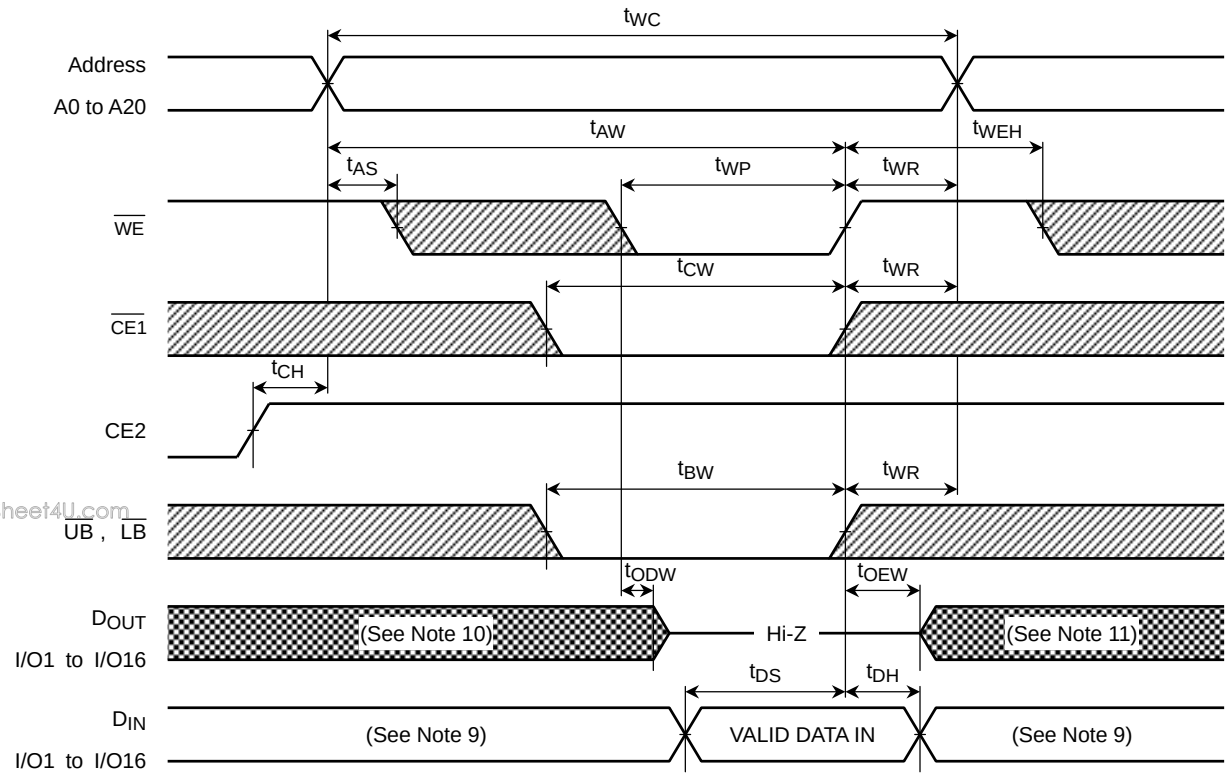
WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 8)



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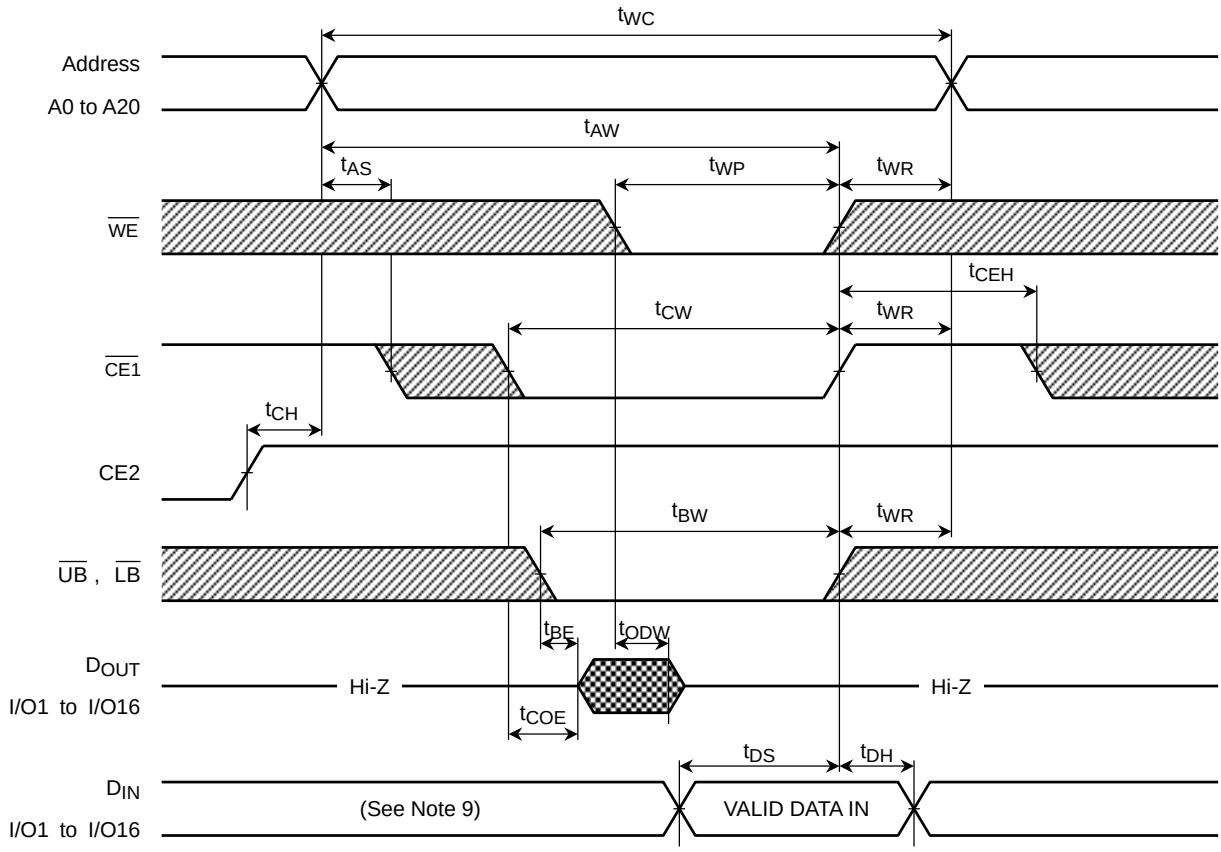
WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 8)



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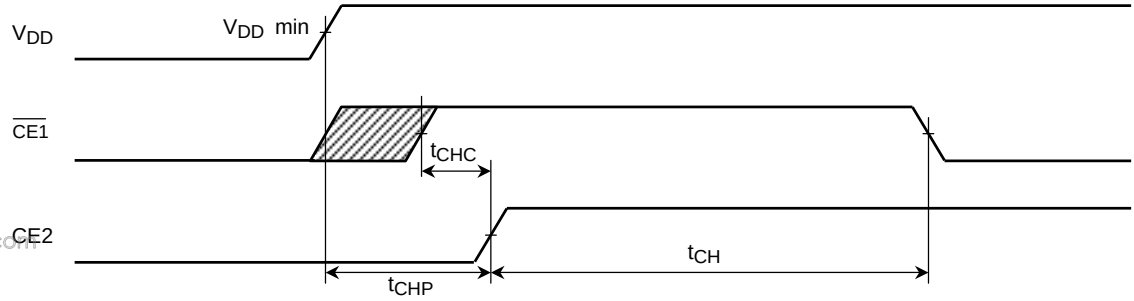
Deep Power-down Timing

Power-on Timing



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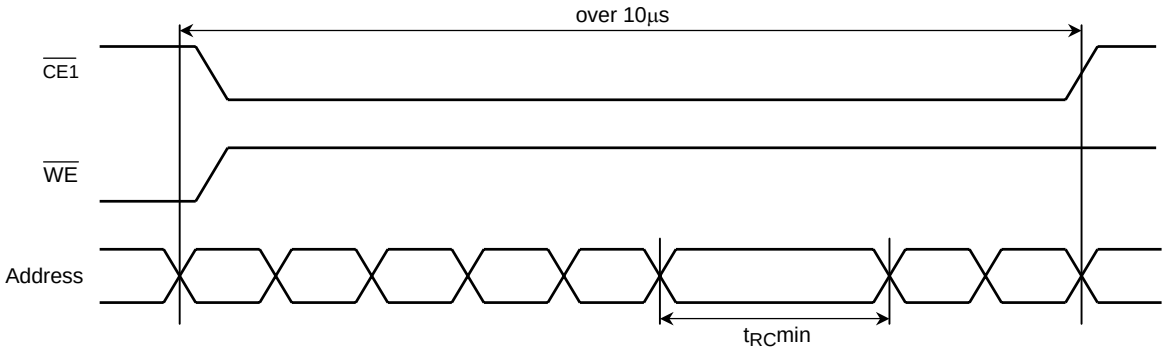
Provisions of Address Skew

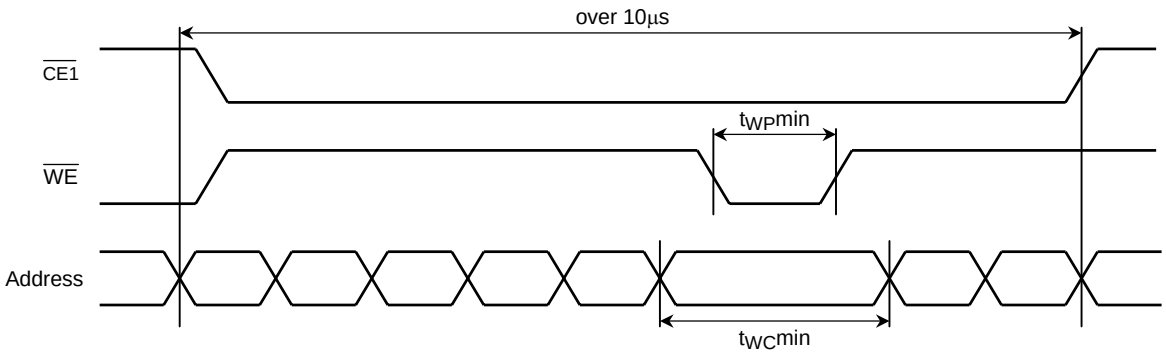
Read

In case, multiple invalid address cycles shorter than t_{RC}min sustain over 10μs in a active status, as least one valid address cycle over t_{RC}min must be needed during 10μs.



Write

In case, multiple invalid address cycles shorter than t_{WC}min sustain over 10μs in a active status, as least one valid address cycle over t_{WC}min with t_{WP}min must be needed during 10μs.



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Notes:

(1) AC measurements are assumed t_R, t_F = 5 ns.

(2) Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are not output voltage reference levels.

(3) Data cannot be retained at deep power-down stand-by mode.

(4) If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.

(5) During the output state of I/O signals, input signals of reverse polarity must not be applied.

(6) If $\overline{CE1}$ or $\overline{LB}$ / $\overline{UB}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

(7) If $\overline{CE1}$ or $\overline{LB}$ / $\overline{UB}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

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128 Mbits NOR FLASH MEMORY

TC58FVM7TDD : Top Boot Block

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TC58FVM7BDD : Bottom Boot Block

Organization : 8M × 16bits

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2. COMMAND SEQUENCES

COMMAND SEQUENCE	BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h										
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA(1)	RD(2)				
ID Read	3	555h	AAh	2AAh	55h	BK(3) + 555h	90h	IA(4)	ID(5)				
Auto Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(6)	PD(7)				
Auto Page Program	11	555h	AAh	2AAh	55h	555h	E6h	PA(6)	PD(7)	PA(6)	PD(7)	PA(6)	PD(7)
Program Suspend	1	BK(3)	B0h										
Program Resume	1	BK(3)	30h										
Auto Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Auto Block Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA(8)	30h
Block Erase Suspend	1	BK(3)	B0h										
Block Erase Resume	1	BK(3)	30h										
Hidden ROM Mode Entry	3	555h	AAh	2AAh	55h	555h	88h						
Hidden ROM Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(6)	PD(7)				
Hidden ROM Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA(8)	30h
Hidden ROM Protect	5	555h	AAh	2AAh	55h	555h	60h	XX1Ah	68h				
Hidden ROM Exit	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h				
CFI	1	BK(3) + 55h	98h	CA(10)	CD(11)								
PPB Set	5	555h	AAh	555h	55h	555h	60h	BA(5) + XX02h	68h				
ALL PPB Clear	5	555h	AAh	555h	55h	555h	60h	XX02h	60h				
Verify Block Protect	3	555h	AAh	555h	55h	BA(5) + 555h	90h	BA(5) + XX02h	PD(0)(4)				

Notes: The system should generate the following address patterns:
555h or 2AAh on address pins A10~A0. DQ8~DQ15 are ignored. X : V_{IH} or V_{IL} (0h-Fh)

(1) RA: Read Address
(2) RD: Read Data Output
(3) BK: Bank Address = A22~A20
(4) IA: Bank Address and ID Read Address (A6,A1,A0)
Bank Address = A22~A20
Manufacturer Code = (0,0,0)
Device Code = (0,0,1)
(5) ID: ID Code Output
(6) PA: Program Address Input
Input continuous 8 addresses from (A0, A1, A2) = (0, 0, 0)
to (A0, A1, A2) = (1, 1, 1) in Page program.
(7) PD: Program Data Input
Input continuous 8 addresses from (A0, A1, A2) = (0, 0, 0)
to (A0, A1, A2) = (1, 1, 1) in Page program.
(8) BA: Block Address = A22~A12
(9) F0h: 00h is valid too.
(10) CA: CFI Address
(11) CD: CFI Data Output

: Read Operations

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3. SIMULTANEOUS READ/WRITE OPERATION

The TC58FVM7(T/B)DD features a Simultaneous Read/Write operation. The Simultaneous Read/Write operation enables the device to simultaneously write data to or erase data from a bank while reading data from another bank.

The TC58FVM7(T/B)DD has a total of sixteen banks (16Mbits x 8 Banks). Banks can be switched by using the bank addresses (A22~A20). For a description of bank blocks and addresses, please refer to the Block Address Table and Block Size Table.

The Simultaneous Read/Write operation cannot perform multiple operations within a single bank. The table below shows the operation modes in which simultaneous operation can be performed.

Note that during Auto-Program execution or Auto Block Erase operation, the Simultaneous Read/Write operation cannot read data from addresses in the same bank which have not been selected for operation. Data from these addresses can be read using the Program Suspend or Erase Suspend function, however.

In order to perform simultaneous operation during automatic operation execution, when changing a bank, it is necessary to set $\overline{OE}$ to V_{IH}.

SIMULTANEOUS READ/WRITE OPERATION

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STATUS OF BANK ON WHICH OPERATION IS BEING PERFORMED	STATUS OF OTHER BANKS
Read Mode	Read Mode
ID Read Mode(1)	
Auto-Program Mode	
Auto-Page Program Mode	
Program Suspend Mode	
Auto Block Erase Mode	
Erase Suspend Mode	
Program during Erase Suspend	
Program Suspend during Erase Suspend	
CFI Mode	

(1) Only Command Mode is valid.

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4. OPERATION MODES

In addition to the Read, Write and Erase Modes, the TC58FVM7(T/B)DD features many functions including block protection and data polling. When incorporating the device into a design, please refer to the timing charts and flowcharts in combination with the descriptions below.

4.1. Read Mode

To read data from the memory cell array, set the device to Read Mode.

The device is automatically set to Read Mode immediately after power-on or on completion of an automatic operation. The Software Reset Command releases The ID Read Mode, releases the lock state when an automatic operation ends abnormally, and sets the device to Read Mode. Hardware Reset terminates operation of the device and resets it to Read Mode. When reading data without changing the address immediately after power-on, the host should input Hardware Reset or change $\overline{CE}$ from H to L.

4.2. ID Read Mode

ID Read Mode is used to read the device manufacturer code and device code. The mode is useful in that it allows EPROM programmers to identify the device type automatically.

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Inputting an ID Read command sets the specified bank to ID Read Mode. Banks are specified by inputting the bank address (BK) in the third Bus Write cycle of the Command cycle. To read an ID code, the bank address as well as the ID read address must be specified (with $\overline{WP}$ = V_{IH} or V_{IL}). The manufacturer code is output from address BK + 00; the device code is output from address BK + 01. From other banks, data is output from the memory cells. Access time in ID Read Mode is the same as that in Read Mode. However 1st access after command input need tWEHH+tACC. For a list of the codes, please refer to the ID Code Table. Inputting a Reset command releases ID Read Mode and returns the device to Read Mode.

4.3. Standby Mode

TC58FVM7(T/B)DD has two ways to put the device into Standby Mode. In Standby Mode, DQ is put into the High-Impedance state.

(1) Control using $\overline{CE}$ and $\overline{RESET}$

With the device in Read Mode, input V_{DD} ± 0.3 V to $\overline{CE}$ and $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow.

(2) Control using $\overline{RESET}$ only

With the device in Read Mode, input V_{SS} ± 0.3 V to $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). Even if the device is in the process of performing simultaneous operation, this method will terminate the current operation and set the device to Standby Mode. This is a hardware reset and is described later.

4.4. Auto-Sleep Mode

This function suppresses power dissipation during reading. If the address input does not change for 150 ns, the device will automatically enter Sleep Mode and the current will be reduced to the standby current (I_{DDS2}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow. Because the output data is latched, data is output in Sleep Mode. When the address is changed, Sleep Mode is automatically released, and data from the new address is output.

4.5. Output Disable Mode

Inputting V_{IH} to $\overline{OE}$ disables output from the device and sets DQ to High-Impedance.

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4.6. Command Write

The TC58FVM7(T/B)DD uses the standard JEDEC control commands for a single-power supply E²PROM. A Command of Write is executed by inputting the address and data into the Command Register. The command is written by inputting a pulse to $\overline{WE}$ with $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} ($\overline{WE}$ control). The command can also be written by inputting a pulse to $\overline{CE}$ with $\overline{WE}$ = V_{IL} ($\overline{CE}$ control). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$. DQ0~DQ7 are valid for data input and DQ8~DQ15 are ignored.

To abort input of the command sequence uses the Reset command. The device will reset the Command Register and enter Read Mode. If an undefined command is input, the Command Register will be reset and the device will enter Read Mode.

4.7. Software Reset: Read/Reset Command

Initiate the software reset by inputting a Read/Reset command. The software reset returns the device from ID Read Mode or CFI Mode to Read Mode, releases the lock state if automatic operation has ended abnormally, and clears the Command Register.

4.8. Hardware Reset

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A hardware reset initializes the device and sets it to Read Mode. When a pulse is input to $\overline{RESET}$ for t_{RP}, the device abandons the operation which is in progress and enters the Read Mode after t_{READY}. Note that if a hardware reset is applied during data overwriting, such as a Write or Erase operation, data at the address or block being written to at the time of the reset will become undefined.

After a hardware reset, the device enters Read Mode if $\overline{RESET}$ = V_{IH} or Standby Mode if $\overline{RESET}$ = V_{IL}. The DQ pins are High-Impedance when $\overline{RESET}$ = V_{IL}. After the device has entered Read Mode, Read operations and input of any command are allowed.

4.9. Comparison between Software Reset and Hardware Reset

ACTION	SOFTWARE RESET	HARDWARE RESET
Releases ID Read Mode or CFI Mode.	True	True
Clears the Command Register.	True	True
Releases the lock state if automatic operation has ended abnormally.	True	True
Stops any automatic operation which is in progress.	False	True
Stops any operation other than the above and returns the device to Read Mode.	False	True

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4.10. Auto-Program Mode

The TC58FVM7(T/B)DD can be programmed in word units. Auto-Program Mode is set using the Program command. The program address and program data is latched in the fourth Bus Write cycle. Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is indicated by the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which the Write is being performed.

During Auto Program execution, a command sequence for the bank on which execution is being performed cannot be accepted. To terminate execution, use a hardware reset. Note that if the Auto-Program operation is terminated in this manner, the data written so far is invalid.

Any attempt to program a protected block is ignored. In this case, the device enters Read Mode 5.5 μs after a latch of program data in the fourth Bus Write cycle.

If an Auto-Program operation fails, the device remains in the programming state and does not automatically return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure. If a programming operation fails, the device should not be used. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

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The device allows 0s to be programmed into memory cells which contain a 1. 1s cannot be programmed into cells which contain 0s. If this is attempted, execution of Auto Program will fail. This is a user error, not a device error. A cell containing 0 must be erased in order to set it to 1.

4.11. Auto-Page Program Mode

Auto-Page Program is a function which enables simultaneously Programming or 8words of data.

In this mode, the Programming time for 128M bit is less than 60% compared with the Auto program mode. In word mode, input the page program command during first bus write cycle to third bus writes cycle. Input program data and address of (A0, A1, A2) = (0, 0, 0) in the forth bus write cycle. Input increment address and program data during the fifth bus write cycle to the eleventh bus write cycle. After input of the eleventh bus write cycle, page program operation starts.

4.12. Program Suspend/Resume Mode

Program Suspend is used to enable Data Read by suspending the Write operation. The device accepts a Program Suspend command in Write Mode (including Write operations performed during Erase Suspend) but ignores the command in other modes. When the command is input, the address of the bank on which Write is being performed must be specified. After input of the command, the device will enter Program Suspend Read Mode after t_{SUSP}.

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend, input a Program Resume command to return to Write Mode. When inputting the command, specify the address of the bank on which Write is being performed. If the ID Read or CFI Data Read function is being used, abort the function before inputting the Resume command. On receiving the Resume command, the device returns to Write Mode and resumes outputting the Hardware Sequence flag for the bank to which data is being written.

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4.13. Auto Chip Erase Mode

The Auto Chip Erase Mode is set using the Chip Erase command. An Auto Chip Erase operation starts on the latch of the command in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the Hardware Sequence flag.

Command input is ignored during an Auto Chip Erase. A hardware reset can interrupt an Auto Chip Erase operation. If an Auto Chip Erase operation is interrupted, it cannot be completed correctly. Hence, an additional Erase operation must be performed.

Any attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 500 μs after the latch of command in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device will remain in the erasing state and will not return to the Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure.

In this case, it cannot be ascertained which block the failure occurred in. Either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed blocks, and stop using them. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

4.14. Auto Block Erase Mode

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The Auto Block Erase Mode is set using the Block Erase command. An Auto Block Erase operation starts on the latch of the command in the sixth bus cycle. All memory cells in the selected block are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the setting of the Hardware Sequence flag. When the Hardware Sequence flag is read, the addresses of the blocks on which the Auto Erase operation is being performed must be specified.

All commands (except Erase Suspend) are ignored during an Auto Block Erase operation. Either operation can be aborted using a Hardware Reset. If an auto-erase operation is interrupted, it cannot be completed correctly; therefore, a further erase operation is necessary to complete the erasing.

Any attempt to erase a protected block is ignored. If the selected block is protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 μs after the latch of command in the sixth bus cycle.

If an Auto Block Erase operation fails, the device remains in the Erasing state and does not return to Read Mode. The device status is indicated by the Hardware Sequence flag. After a failure, either a Reset command or a Hardware Reset is required to return the device to Read Mode. If an Auto Block Erase operation fails, the device should not be used. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed block.

4.15. Erase Suspend/Erase Resume Modes

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other oreration modes. When the command is input, the address of the bank on which Erase is being performed must be specified.

In Erase Suspend Mode only a Read, Program or Resume command can be accepted. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE}. The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and $RY/\overline{BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On input of the command, the address of the bank on which the Write was being performed must be specified. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on $RY/\overline{BY}$.

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4.16. Block Protection

TC58FVM7(T/B)DD has Block Protection that is a function for disabling writing and erasing specific blocks. Block Protection features several level of Block Protection.

(1) Write Protect ($\overline{WP}$ pin) [Hardware Protection]

The TC58FVM7(T/B)DD has Hardware Block protection feature by $\overline{WP}$=V_{IL}. The TC58FVM7TDD protects BA133 and BA134 with $\overline{WP}$=V_{IL}. TC58FVM7BDD protects BA0 and BA1 with $\overline{WP}$=V_{IL}. This mode is released with $\overline{WP}$=V_{IH}. When the device is programming operation or erasing operation, $\overline{WP}$ pin has to fix to V_{IH} or V_{IL}.

(2) Block Protection 1 Persistent Protection Bit(PPB) [Software Protection]

By using Persistent Protection Bit, protection can be set to each block. The PPBs retains the state across power cycle. Each PPB can be individually modifiable through the PPB Set command. All PPB can be cleared by the PPB Clear Command at a time. The Verify Block Protect command to the device can check the PPB status.

The PPB set and the PPB clear are an auto operation same as the Auto Program and the Auto Chip Erase. An auto operation start from the command latch in the 4th write bus cycle of the PPB Set and the PPB clear. The status of the PPB set and the PPB clear are indicated by the below haradware sequence flag. If an auto operation fails,either a Hidden ROM exit command or a Hardware Reset is required to return the device to Read Mode. The PPB set time is eqal to tPPAW (auto-page program time). The PPB clear time is equal to tPBEW (auto-block erase time).

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When PPB is locked by the PPB Lock Set command, PPB is disabled for PPB Set and PPB Clear Operation. The PPB Lock Verify command can check the PPB Lock status on the DQ1 ('1' is Set state and '0' is Clear state). Behaviors of PPB Lock differ between password protection mode and non-password protection mode.

At the time of the finishing PPB Set, PPB Clear, PPB Lock Set and PPB Lock Verify, the hosts have to inputting the Hidden ROM Exit command.

At the time of shipment, the PPBs and PPB Lock are settled to "0".

The Hardware Sequence Flags of the PPB Set

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/$\overline{BY}$
In Progress	0	Toggle	0	0	0	1	0	0	0
Set Complete	1	1	0	0	0	1	0	0	High-Z
Set Failed	0	Toggle	1	0	0	1	0	0	0

The Hardware Sequence Flags of the PPB Clear

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/$\overline{BY}$
In Progress	0	Toggle	0	0	1	Toggle	0	0	0
Clear Complete	1	1	0	0	1	1	0	0	High-Z
Clear Failed	0	Toggle	1	0	1	N/A	0	0	0

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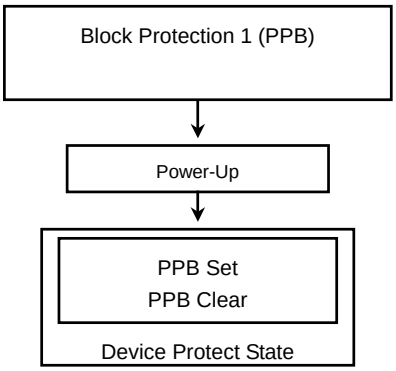
4.16.1 Relationship of the Each Block Protection



4.16.2. Block Protection Matrix

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Hardware Protection	Software Protection	Block Protect Status	
$\overline{WP}$	PPB	Two Boot Block	Other Block
L	Clear	Protected	Unprotected
	Set	Protected	Protected
H	Clear	Unprotected	Unprotected
	Set	Protected	Protected

4.16.3. Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. The Verify Block Protect command, which can be performed simultaneously with operations in another bank, is performed by setting the block address with A0 = A6 = V_{IL} and A1 = V_{IH}. If the block is protected, 01h is output. If the block is unprotected, 00h is output. The status depends on PPB, DPB, $\overline{WP}$ state. Inputting the verify block protect command sequence sets the specified bank to the Verify Block Protect mode. Inputting a Reset command releases this mode and returns the device to Read Mode. When verifying block protect across a bank boundary, a Reset command is needed at the time of the change of a bank.

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4.17. Hidden ROM Area

The TC58FVM7(T/B)DD features a 64-Kword hidden ROM area, which is separate from the memory cells. The area consists of one block. Data Read, Write and Protect can be performed on this block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The hidden ROM area is located in the address space indicated in the HIDDEN ROM AREA ADDRESS TABLE. To access the Hidden ROM area, input a Hidden ROM Mode Entry command. The device now enters Hidden ROM Mode, allowing Read, Write, Erase and Block Protect to be executed. Write and Erase operations are the same as auto operations except that the device is in Hidden ROM Mode.

To protect the hidden ROM area, use the Hidden ROM Protect Command. The status of Hidden ROM protect operation can be checked by hardware sequence flags. Hidden ROM protect time is eqal to tPPAW (auto-page program time). Note that in Hidden ROM Mode, simultaneous operation cannot be performed for BANK7 in top boot type and for BANK0 in bottom boot type. To exit Hidden ROM Mode, use the Hidden ROM Mode Exit command. This will return the device to Read Mode.

HIDDEN ROM AREA ADDRESS TABLE

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TYPE	BOOT BLOCK ARCHITECTURE	ADDRESS RANGE	SIZE
TC58FVM7TDD	TOP BOOT BLOCK	7F0000h~7FFFFFh	64 Kwords
TC58FVM7BDD	BOTTOM BOOT BLOCK	000000h~00FFFFh	64 Kwords

The Hardware Sequence Flags of the Hidden ROM Protect

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/$\overline{BY}$
In Progress	0	Toggle	0	0	0	1	0	0	0
Protect Complete	1	1	0	0	0	1	0	0	High-Z
Protect Failed	0	Toggle	1	0	0	1	0	0	0

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4.18. CFI (Common Flash memory Interface)

The TC58FVM7(T/B)DD conforms to the CFI specifications. To read information from the device, input the Query command followed by the address. To exit this mode, input the Reset command.

CFI CODE TABLE 1 (Continue)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
10h 11h 12h	0051h 0052h 0059h	ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM command set 2: AMD/FJ standard type
15h 16h	0040h 0000h	Address for primary extended table
17h 18h	0000h 0000h	Alternate OEM command set 0: none exists
19h 1Ah	0000h 0000h	Address for alternate OEM extended table
1Bh	0027h	V_{DD} (min) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Ch	0033h	V_{DD} (max) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Dh	0000h	V_{PP} (min) voltage
1Eh	0000h	V_{PP} (max) voltage
1Fh	0004h	Typical time-out per single word write (2^N μs)
20h	0000h	Typical time-out for minimum size buffer write (2^N μs)
21h	000Ah	Typical time-out per individual block erase (2^N ms)
22h	0000h	Typical time-out for full chip erase (2^N ms)
23h	0004h	Maximum time-out for word write (2^N times typical)
24h	0006h	Maximum time-out for buffer write (2^N times typical)
25h	0004h	Maximum time-out per individual block erase (2^N times typical)
26h	0004h	Maximum time-out for full chip erase (2^N times typical)
27h	0018h	Device Size (2^N byte) 18h:128Mbit
28h 29h	0001h 0000h	Flash device interface description 1: x 16
2Ah 2Bh	0004h 0000h	Maximum number of bytes in multi-byte write (2^N)

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CFI CODE TABLE 2(Sequel)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
2Ch	0002h	Number of erase block regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0040h 0000h	Erase Block Region 1 information Bits 0~15: y = block number Bits 16~31: z = block size (z × 256 bytes)
31h 32h 33h 34h	007Eh 0000h 0000h 0002h	Erase Block Region 2 information
40h 41h 42h	0050h 0052h 0049h	ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0031h	Minor version number, ASCII
45h	0000h	Address-Sensitive Unlock 0: Required 1: Not required
46h	0002h	Erase Suspend 0: Not supported 1: For Read-only 2: For Read & Write
47h	0001h	Block Protect 0: Not supported X: Number of blocks per group
48h	0000h	Block Temporary Unprotect 0: Not supported 1: Supported
49h	0007h	Block Protect/Unprotect scheme
4Ah	0001h	Simultaneous operation 0: Not supported 1: Supported
4Bh	0000h	Burst Mode 0: Not supported
4Ch	0001h	Page Mode 0: Not supported 1: Supported
4Dh	0085h	V_{ACC} (min) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Eh	00C6h	V_{ACC} (max) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Fh	000xh	Top/Bottom Boot Block Flag X = 2: Bottom Boot Block: TC58FVM7BDD X = 3: Top Boot Block: TC58FVM7TDD
50h	0001h	Program Suspend 0: Not supported 1: Supported

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CFI CODE TABLE 3(Sequel)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
57h	0008h	Bank Organization 00h: Data at 4Ah is zero X: Number of Banks
58h	00XXh	Bank0 Region information XX: Number of blocks Bank0 TOP : 10h BOTTOM:27h
59h	0010h	Bank1 Region information Number of blocks Bank1 n=16
5Ah	0010h	Bank2 Region information Number of blocks Bank2 n=16
5Bh	0010h	Bank3 Region information Number of blocks Bank3 n=16
5Ch	0010h	Bank4 Region information Number of blocks Bank4 n=16
5Dh	0010h	Bank5 Region information Number of blocks Bank5 n=16
5Eh	0010h	Bank6 Region information Number of blocks Bank6 n=16
5Fh	00XXh	Bank7 Region information XX: Number of blocks Bank7 TOP : 27h BOTTOM:10h

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4.19. HARDWARE SEQUENCE FLAGS

The TC58FVM7(T/B)DD has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE}$ = $\overline{OE}$ = V_{IL} in Read Mode. The RY/$\overline{BY}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

STATUS				DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	0	0	1	0
	Read in Program Suspend(1)			Data	Data	Data	Data	Data	High-Z
	In Auto Erase	Auto Erase	Selected(2)	0	Toggle	0	1	Toggle	0
			Not-selected(3)	0	Toggle	0	1	1	0
	In Erase Suspend	Read	Selected	1	1	0	0	Toggle	High-Z
			Not-selected	Data	Data	Data	Data	Data	High-Z
		Programming	Selected	$\overline{DQ7}$	Toggle	0	0	Toggle	0
			Not-selected	$\overline{DQ7}$	Toggle	0	0	1	0
Time Limit Exceeded	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	1	0	1	0
	Auto Erase			0	Toggle	1	1	N/A	0
	Programming in Erase Suspend			$\overline{DQ7}$	Toggle	1	0	N/A	0

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Notes:DQ outputs cell data and RY/$\overline{BY}$ goes High-Impedence when the operation has been completed.
DQ0 and DQ1 pins are reserved for future use. 0 is output on DQ0, DQ1 and DQ4.

(1) Data output from an address to which Write is being performed is undefined.
(2) Output when the block address selected for Auto Block Erase is specified and data is read from there.
(3) Output when a block address not selected for Auto Block Erase of same bank as selected block is specified and data is read from there. During Auto Chip Erase, all blocks are selected.
(4) In case of Page program operation is program data of (A0, A1, A2) = (1, 1, 1) in eleventh bus write cycle.

4.19.1. DQ7 ($\overline{DATA}$ polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto-Program or auto-erase operation fails, DQ7 simply outputs the data.

When the operation has finished, the address latch is reset. Data polling is asynchronous with the $\overline{OE}$ signal.

4.19.2. DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto-Program or auto-erase operation. The Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each $\overline{OE}$ access while $\overline{CE}$ = V_{IL} while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation fails, the DQ6 output toggles.

If an attempt is made to execute an Auto Program operation on a protected block, DQ6 will toggle for around 3 μs. It will then stop toggling. If an attempt is made to execute an auto chip erase operation on a protected all block, DQ6 will toggle for around 300 μs. It will then stop toggling. After toggling has stopped the device will return to Read Mode. If an attempt is made to execute an auto block erase operation on a protected block, DQ6 will toggle for around 3 μs. It will then stop toggling. After toggling has stopped the device will return to Read Mode.

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4.19.3. DQ5 (internal time-out)

If an Auto-Program or auto-erase operates normally, DQ5 outputs a 0. If the internal timer times out during a Program or Erase operation, DQ5 outputs a 1. This indicates that the operation has not been completed within the allotted time.

Any attempt to program a 1 into a cell containing a 0 will fail (see Auto-Program Mode). In this case, DQ5 outputs a 1. In this case, DQ5 doesn't indicate defective device but mistaken usage.

After an Auto-Program or auto-erase operation ends normally, the device outputs actual cell array data. Therefor only with the data of DQ5 can't specify whether cell array data or hardware sequence flag. The hosts shuold check the state of device whether progrress or not, using DQ7, DQ6, or RY/$\overline{BY}$.

In the case of internal time-out, either hardware reset or a software Reset command is required to return the device to Read Mode.

4.19.4. DQ3 (Block Erase)

DQ3 is used to indicate whether the device is in Auto Erase Mode or Erase Suspend Mode.

DQ3 outputs a 1 when the Auto Block Erase or the Auto Chip Erase operation starts. If data is read from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ3 output a 0. Moreever, DQ3 outputs a 0 regardless of the block at the Erase Suspend Programming mode. DQ3 outputs a 1 if the Erase operation fails, and outputs a 0 if the Program in Erase Suspend operation fails.

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4.19.5. DQ2 (Toggle bit 2)

DQ2 is used to indicate which blocks have been selected for Auto Block Erase or to indicate whether the device is in Erase Suspend Mode.

If data is read continuously from the selected block during an Auto Block Erase, the DQ2 output will toggle.

Now 1 will be output from non-selected blocks; thus, the selected block can be ascertained. If data is read continuously from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ2 output will toggle. Because the DQ6 output is not toggling, it can be determined that the device is in Erase Suspend Mode. If data is read from the address to which data is being written during Erase Suspend in Programming Mode, DQ2 will output a 1.

4.19.6. RY/$\overline{BY}$ (READY/ $\overline{BUSY}$)

The TC58FVM7(T/B)DD has a RY/$\overline{BY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto-Program or auto-erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can now accept a new command. RY/$\overline{BY}$ outputs a 0 when an operation has failed.

RY/$\overline{BY}$ outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. RY/$\overline{BY}$ outputs a 1 during an Erase Suspend operation. The output buffer for the RY/$\overline{BY}$ pin is an open-drain type circuit, allowing a wired-OR connection. A pull-up resistor must be inserted between V_{DD} and the RY/$\overline{BY}$ pin.

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5. DATA PROTECTION

The TC58FVM7(T/B)DD includes a function which guards against malfunction or data corruption.

5.1. Protection against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power-on or power-down, the device will not accept commands while V_{DD} is below V_{LKO}. In this state, command input is ignored.
If V_{DD} drops below V_{LKO} during an Auto Operation, the device will terminate Auto-Program execution. In this case, Auto operation is not executed again when V_{DD} returns to recommended V_{DD} voltage. Therefore, command need to be input to execute Auto operation again.
When $V_{DD} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

5.2. Protection against Malfunction Caused by Glitches

To prevent malfunction write during operation caused by noise from the system, the device will not accept pulses shorter than 3 ns (Typ.) input on $\overline{WE}$, $\overline{CE}$ or $\overline{OE}$. However, if a glitch exceeding 3 ns (Typ.) occurs and the glitch is input to the device malfunction write may occur.
The device uses standard JEDEC commands. It is conceivable that, in extreme cases, system noise may be misinterpreted as part of a command sequence input and that the device will acknowledge it. Then, even if a proper command is input, the device may not operate. To avoid this possibility, clear the Command Register before command input. In an environment prone to system noise, Toshiba recommends input of a software or hardware reset before command input.

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5.3. Protection against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power-on, when power is turned on with $\overline{WE} = \overline{CE} = V_{IL}$ the device does not latch the command on the first rising edge of $\overline{WE}$ or $\overline{CE}$. Instead, the device automatically Resets the Command Register and enters Read Mode.

6. AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	V_{DD}, 0.0 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	$V_{DD}/2$, $V_{DD}/2$
Timing Measurement Reference Level (output)	$V_{DD}/2$, $V_{DD}/2$
Output Load	C_L (30 pF) + 1 TTL Gate

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7. AC CHARACTERISTICS AND OPERATING CONDITIONS

7.1. Read Cycle

Symbol	Parameter	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	70	—	ns
t_{PRC}	Page Read Cycle Time	25	—	ns
t_{ACC}	Address Access Time	—	70	ns
t_{CE}	$\overline{CE}$ Access Time	—	70	ns
t_{OE}	$\overline{OE}$ Access Time	—	25	ns
t_{PACC}	Page Access Time	—	25	ns
t_{OEH}	$\overline{OE}$ High-Level Hold Time (read)	0	—	ns
t_{CEE}	$\overline{CE}$ to Output Low-Z	0	—	ns
t_{OEE}	$\overline{OE}$ to Output Low-Z	0	—	ns
t_{OH}	Output Data Hold Time	0	—	ns
t_{AOH}	Output Data Hold Time (Page Read)	0	—	ns
t_{DF1}	$\overline{CE}$ to Output High-Z	—	25	ns
t_{DF2}	$\overline{OE}$ to Output High-Z	—	25	ns

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7.2. Command Write cycle

Symbol	Parameter		MIN	MAX	UNIT
t_{CMD}	Command Write Cycle Time		70	—	ns
t_{AS}	Address Set-up Time		0	—	ns
t_{AH}	Address Hold Time		30	—	ns
t_{DS}	Data Set-up Time		30	—	ns
t_{DH}	Data Set-up Time		0	—	ns
t_{WELH}	$\overline{WE}$ Low-Level Hold Time	($\overline{WE}$ Control)	30	—	ns
t_{WEHH}	$\overline{WE}$ High-Level Hold Time	($\overline{WE}$ Control)	20	—	ns
t_{CES}	$\overline{CE}$ Set-up Time to $\overline{WE}$ Active	($\overline{WE}$ Control)	0	—	ns
t_{CEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level	($\overline{WE}$ Control)	0	—	ns
t_{CELH}	$\overline{CE}$ Low-Level Hold Time	($\overline{CE}$ Control)	30	—	ns
t_{CEHH}	$\overline{CE}$ High-Level Hold Time	($\overline{CE}$ Control)	20	—	ns
t_{WES}	$\overline{WE}$ Set-up time to $\overline{CE}$ Active	($\overline{CE}$ Control)	0	—	ns
t_{WEH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High Level	($\overline{CE}$ Control)	0	—	ns
t_{OES}	$\overline{OE}$ Set-up Time		0	—	ns
t_{VDS}	V_{DD} Set-up Time		500	—	μs

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7.3. Program and Erase cycle

Symbol	Parameter	MIN	MAX	UNIT
t_{OEHP}	$\overline{OE}$ High Level Hold Time (Polling)	10	—	ns
t_{OEHT}	$\overline{OE}$ High Level Hold Time (Toggle Read)	20	—	ns
t_{CEHT}	$\overline{CE}$ High Level Hold Time (Toggle Read)	20	—	ns
t_{AHT}	Address Hold Time (Toggle)	0	—	ns
t_{AST}	Address Set-up Time (Toggle)	0	—	ns
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	—	90	ns
	Program/Erase Valid to RY/$\overline{BY}$ Delay during Suspend Mode	—	500	ns
t_{RB}	RY/$\overline{BY}$ Recovery Time	0	—	ns
t_{SUSP}	Program Suspend Command to Suspend Mode	—	5.5	μs
t_{SUSPA}	Page Program Suspend Command to Suspend Mode	—	5.5	μs
t_{RESP}	Program Resume Command to Program Mode	—	1	μs
t_{SUSE}	Erase Suspend Command to Suspend Mode	—	25	μs
t_{RESE}	Erase Resume Command to Erase Mode	—	1	μs

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7.4. Hardware RESET

Symbol	Parameter	MIN	MAX	UNIT
t_{READY}	Read Mode Recovery Time from $\overline{RESET}$ (During Auto Operation)	—	25	μs
t_{READY}	Read Mode Recovery Time from $\overline{RESET}$ （During Non Auto Operation）	—	500	ns
t_{RP}	$\overline{RESET}$ Low Level Hold Time	500	—	ns
t_{RH}	Recovery Time from $\overline{RESET}$	50	—	ns
t_{RPD}	$\overline{RESET}$ goes Low to Standby Mode	20	—	μs

7.5. Program and Erase characteristics

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
t_{PPW}	Auto-Program Time (Word Mode)	—	12	300	μs
t_{PPAW}	Auto-Page program time	—	60	2400	μs
t_{PCEW}	Auto Chip Erase Time(1)	—	162	675	s
t_{PBEW}	Auto Block Erase Time(1)	—	1.2	5(2)	s
t_{EW}	Erase/Program Cycle	10^5	—	—	Cycle.

(1) Auto Chip Erase Time and Auto Block Erase Time include internal pre program time.

(2) Minimum interval between resume and the following suspend command is 150 μs. If it's shorter than 150 μs, auto block erase time is expand more than maximum(5 s).

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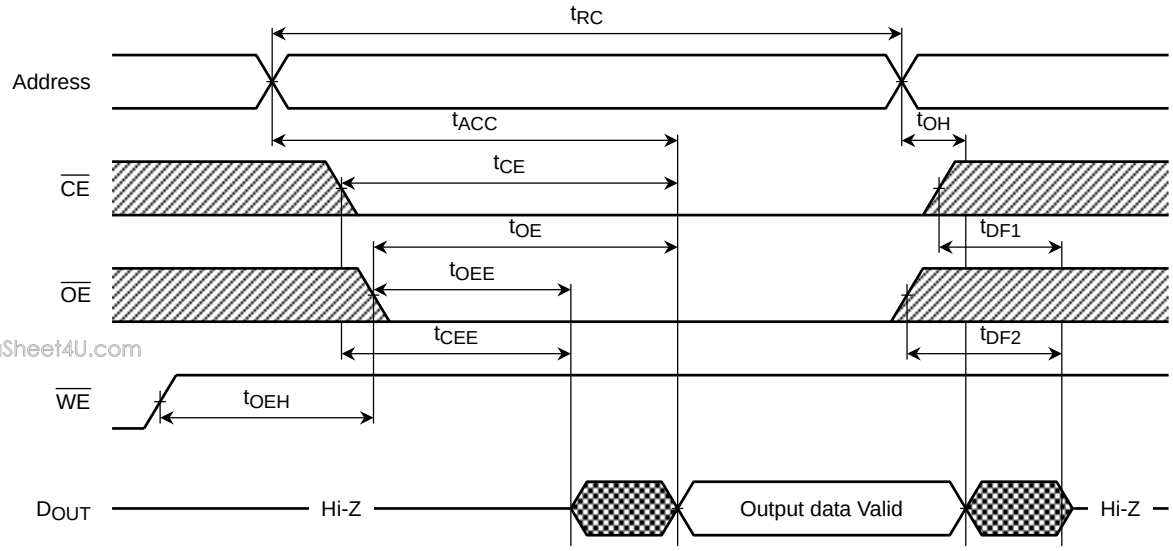
8. TIMING DIAGRAMS

V_{IH} or V_{IL} Data invalid

Read/ID Read Operation



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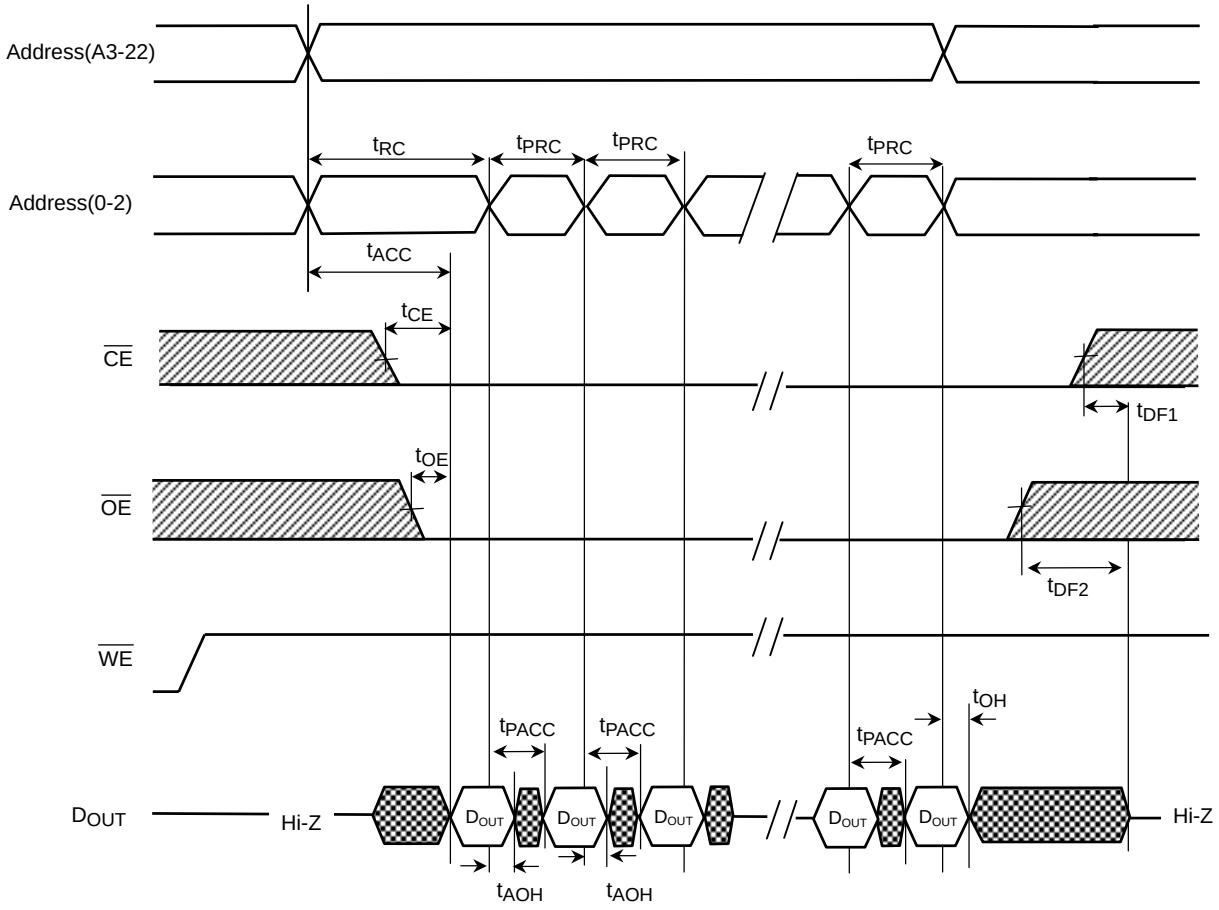
Page Read Operation



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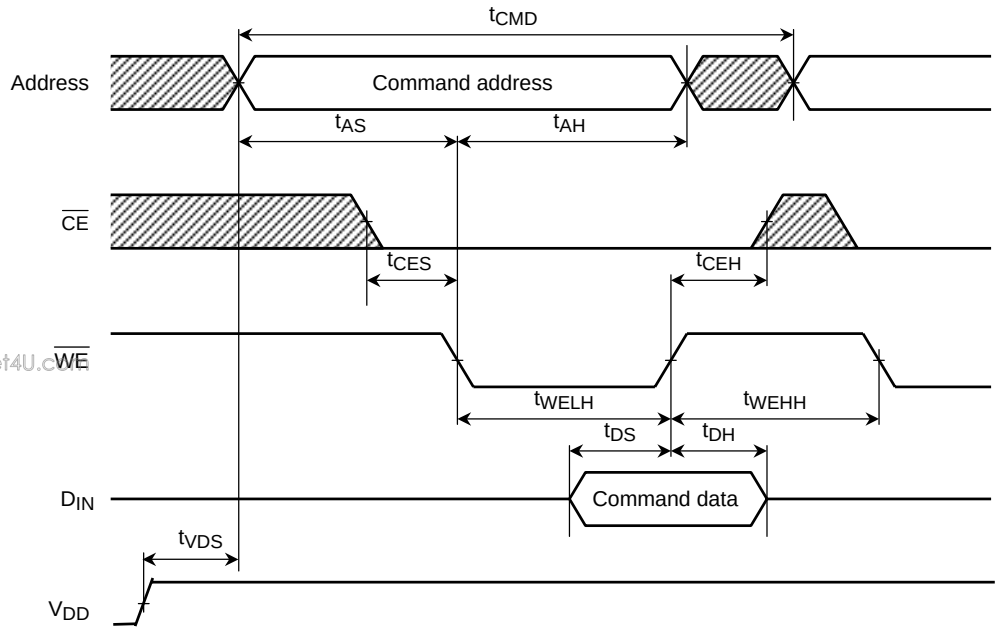
Command Write Operation

This is the timing of the Command Write Operation. The timing which is described in the following pages is essentially the same as the timing shown on this page.

- $\overline{WE}$ Control



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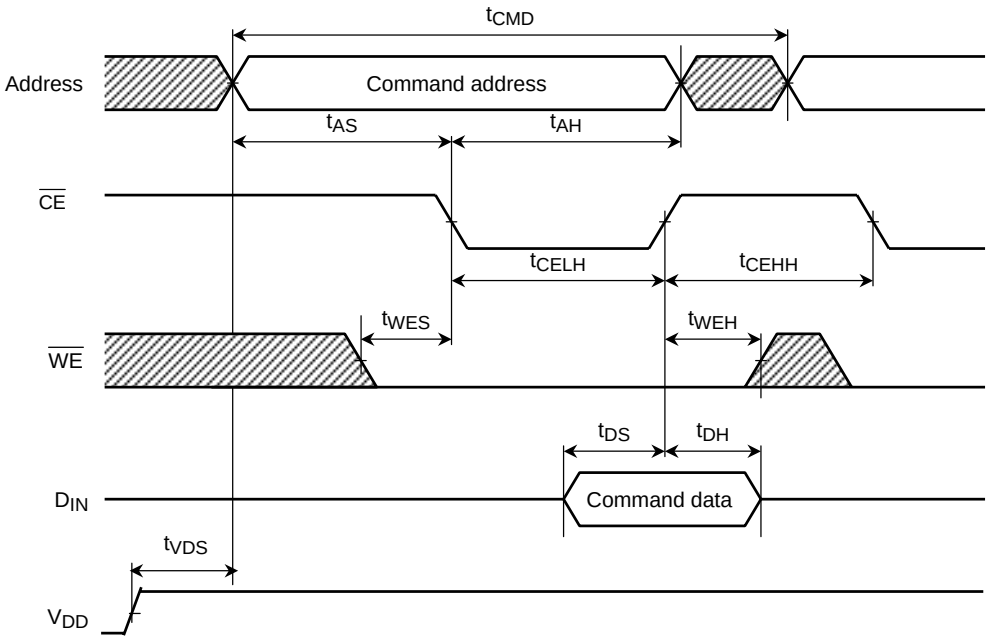
- $\overline{CE}$ Control



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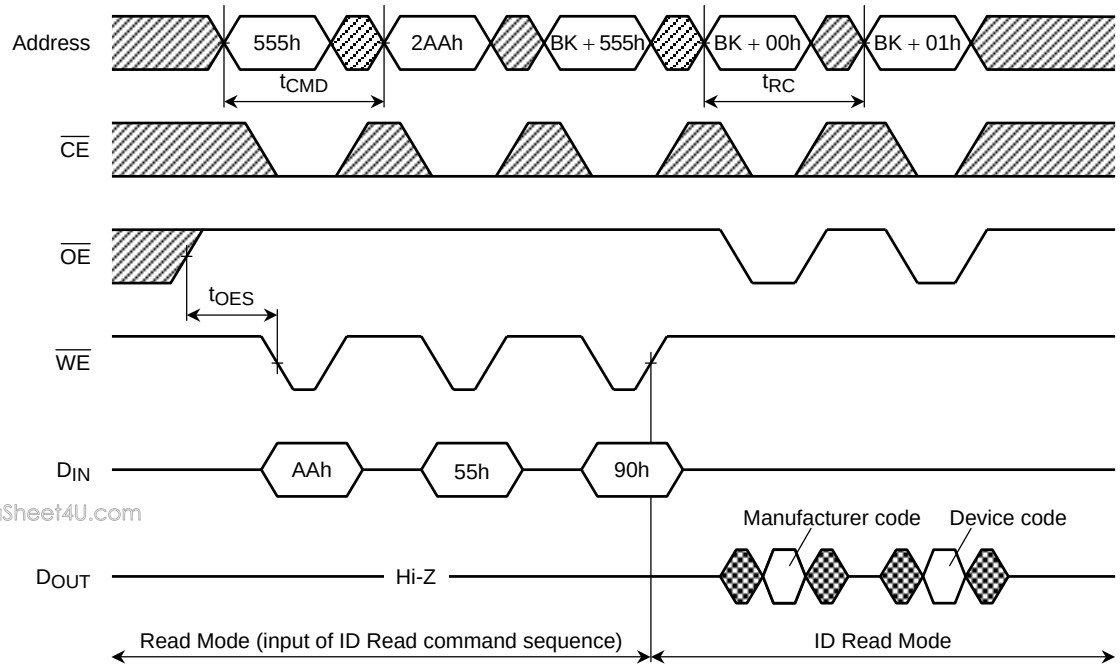
ID Read Operation (input command sequence)



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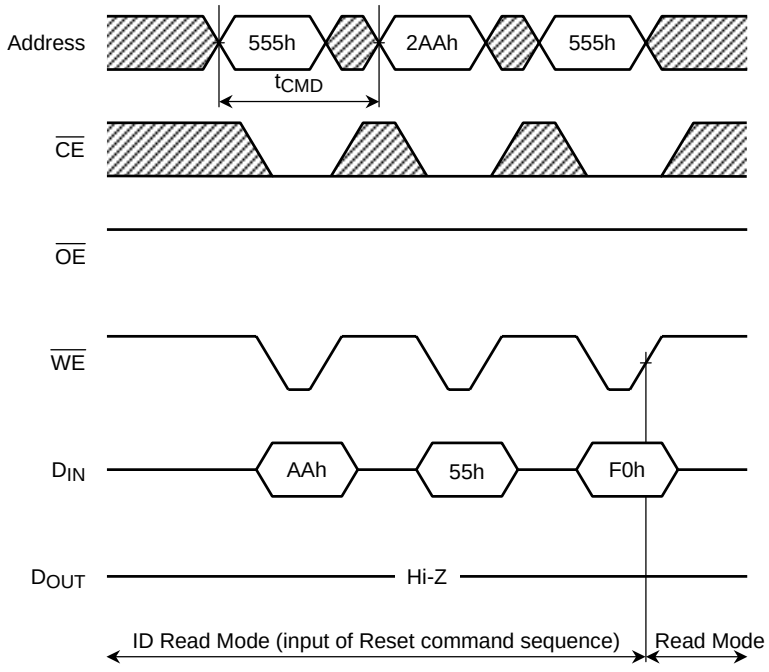
(Continued)



BK: Bank address

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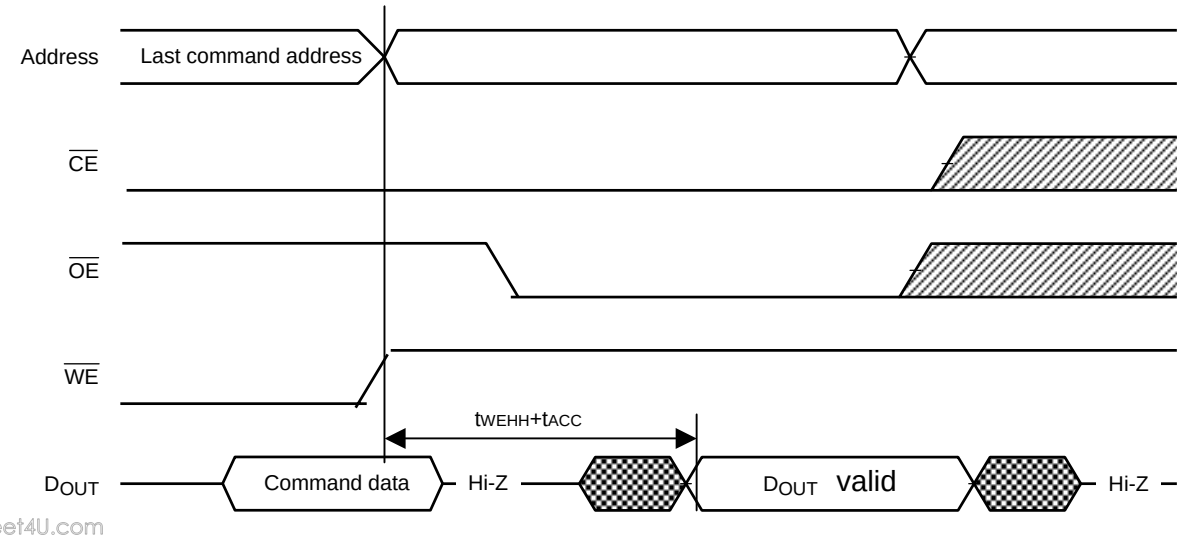
Read after command input (Only Hidden Rom/CFI Read)



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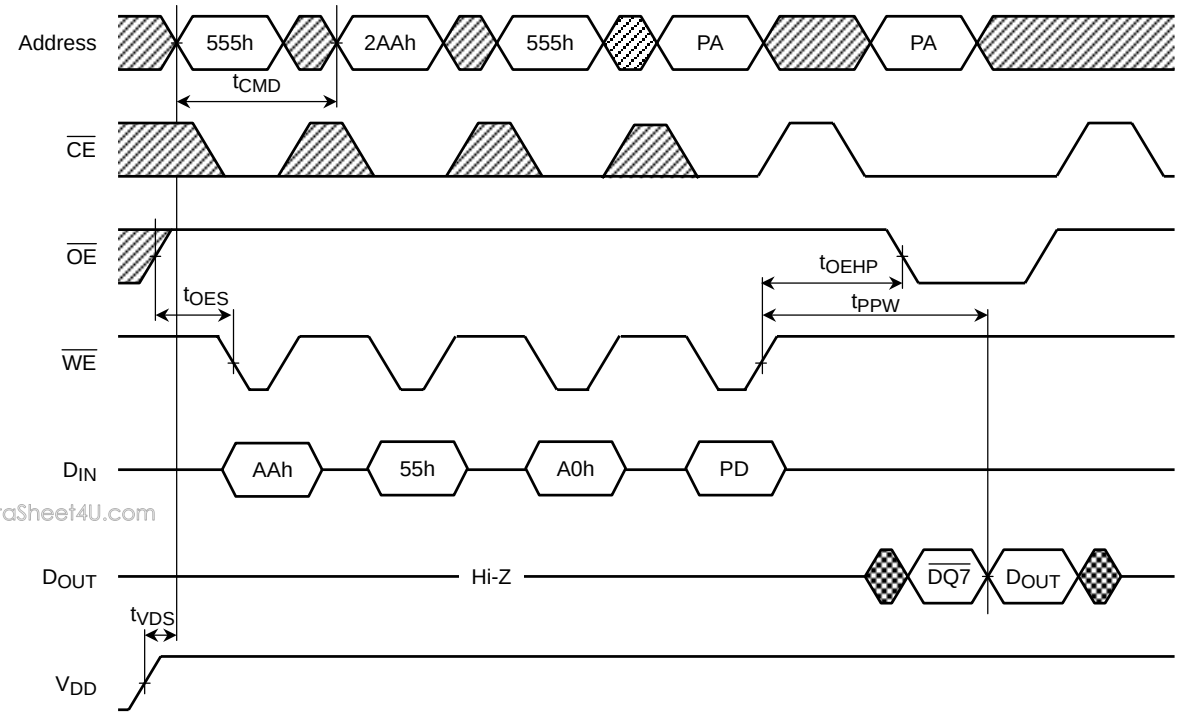
Auto-Program Operation ($\overline{WE}$ Control)



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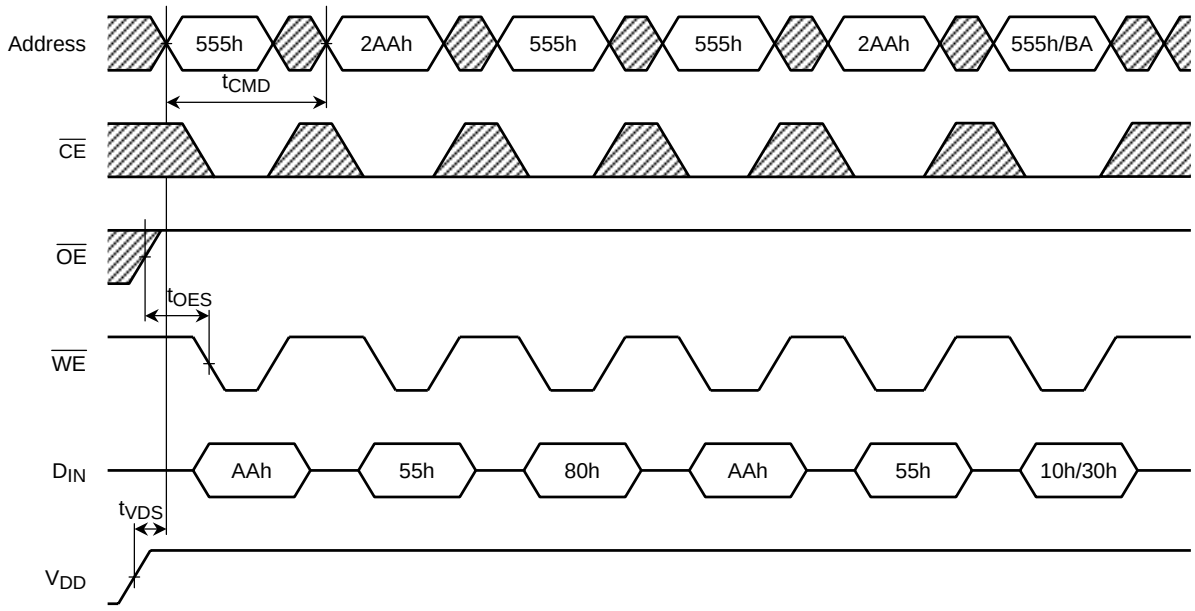
Notes: PA: Program address
PD: Program data

Auto Chip Erase/Auto Block Erase Operation ($\overline{WE}$ Control)



Notes: BA: Block Address

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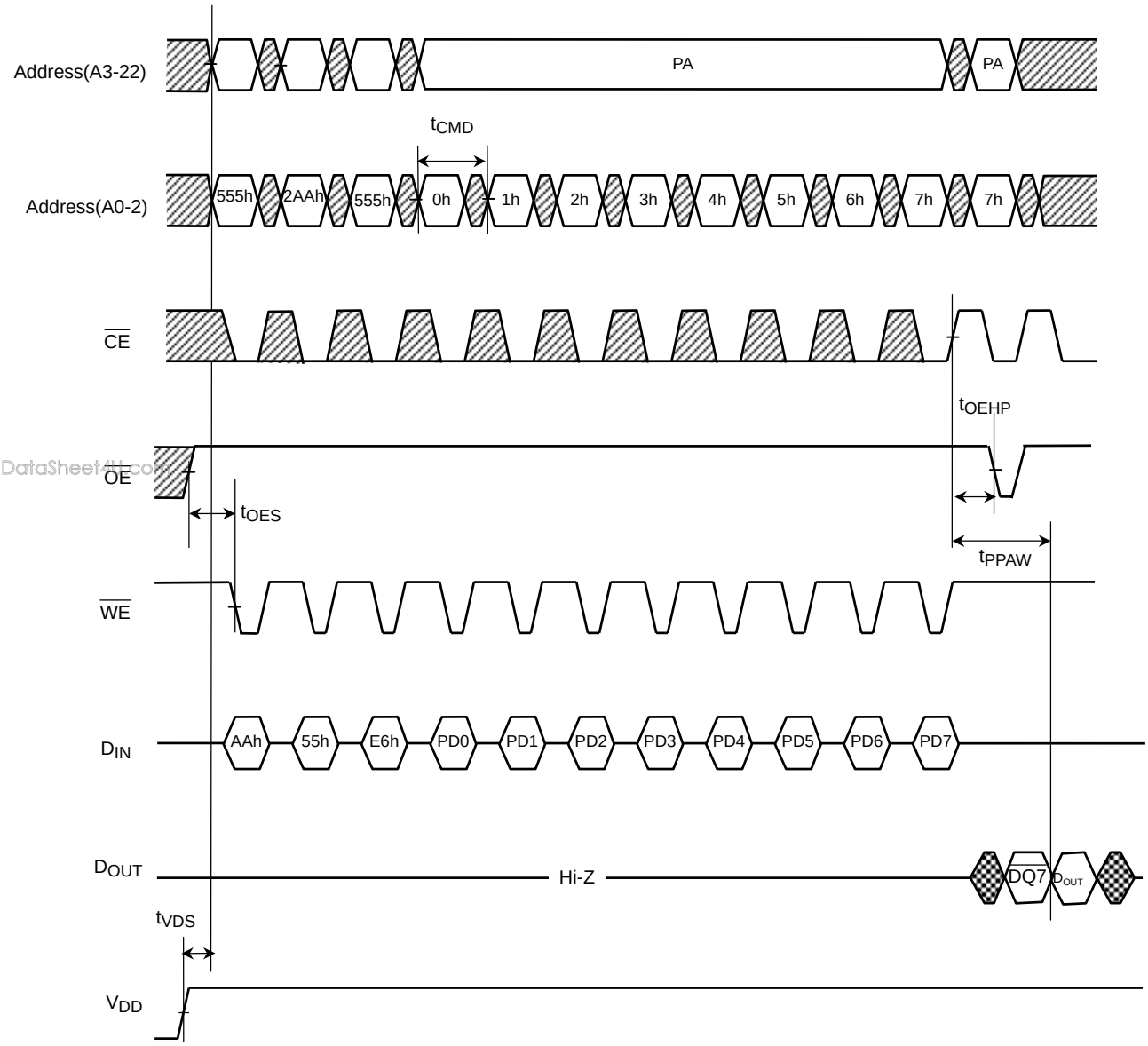
Auto Page Program Operation ($\overline{WE}$ Control)



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Notes: PA: Program address
PD: Program Data

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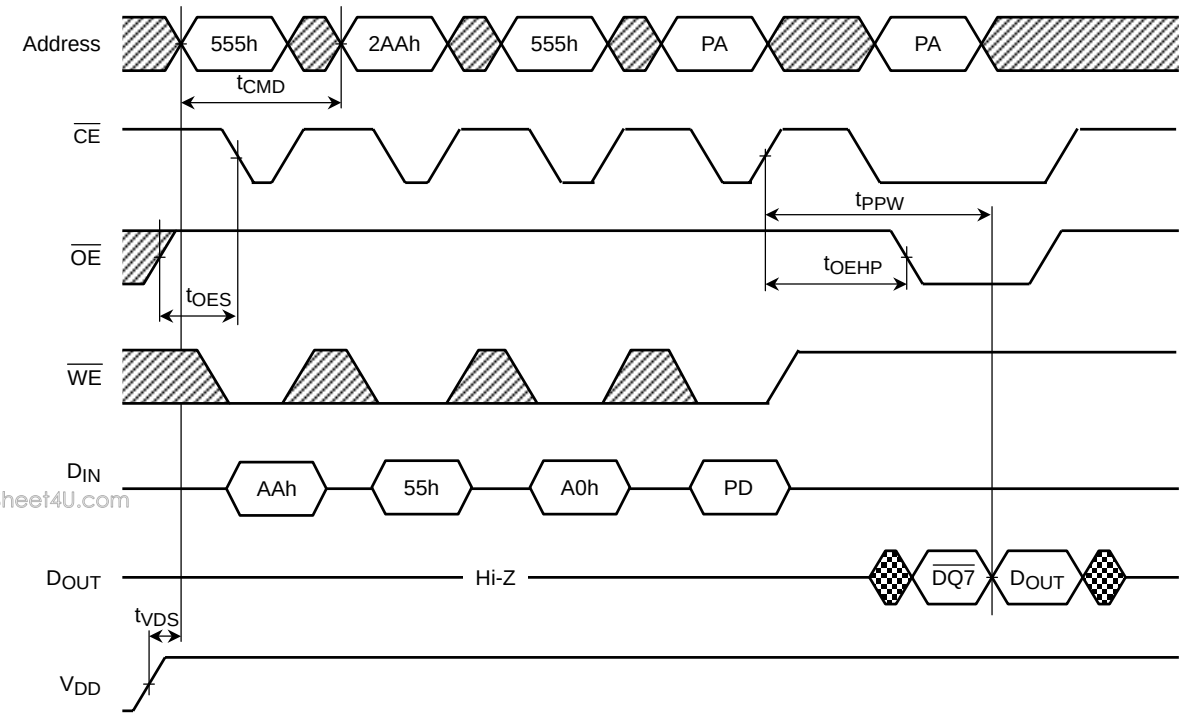
Auto-Program Operation ($\overline{CE}$ Control)



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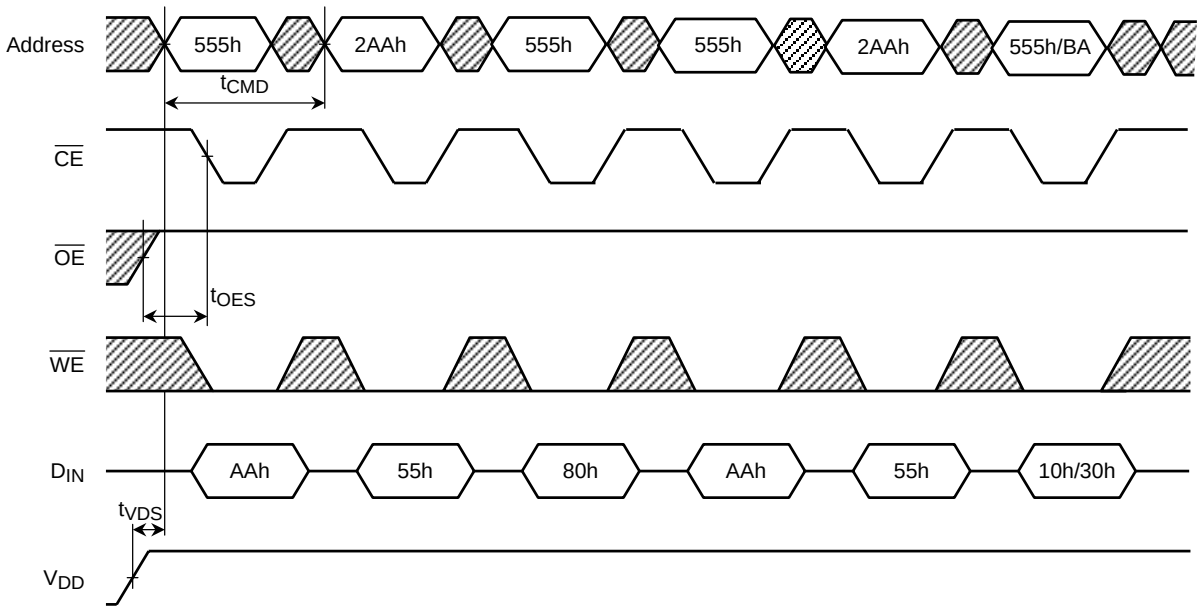
Note: PA: Program address
PD: Program data

Auto Chip Erase/Auto Block Erase Operation ($\overline{CE}$ Control)



Note: BA: Block address for Auto Block Erase operation

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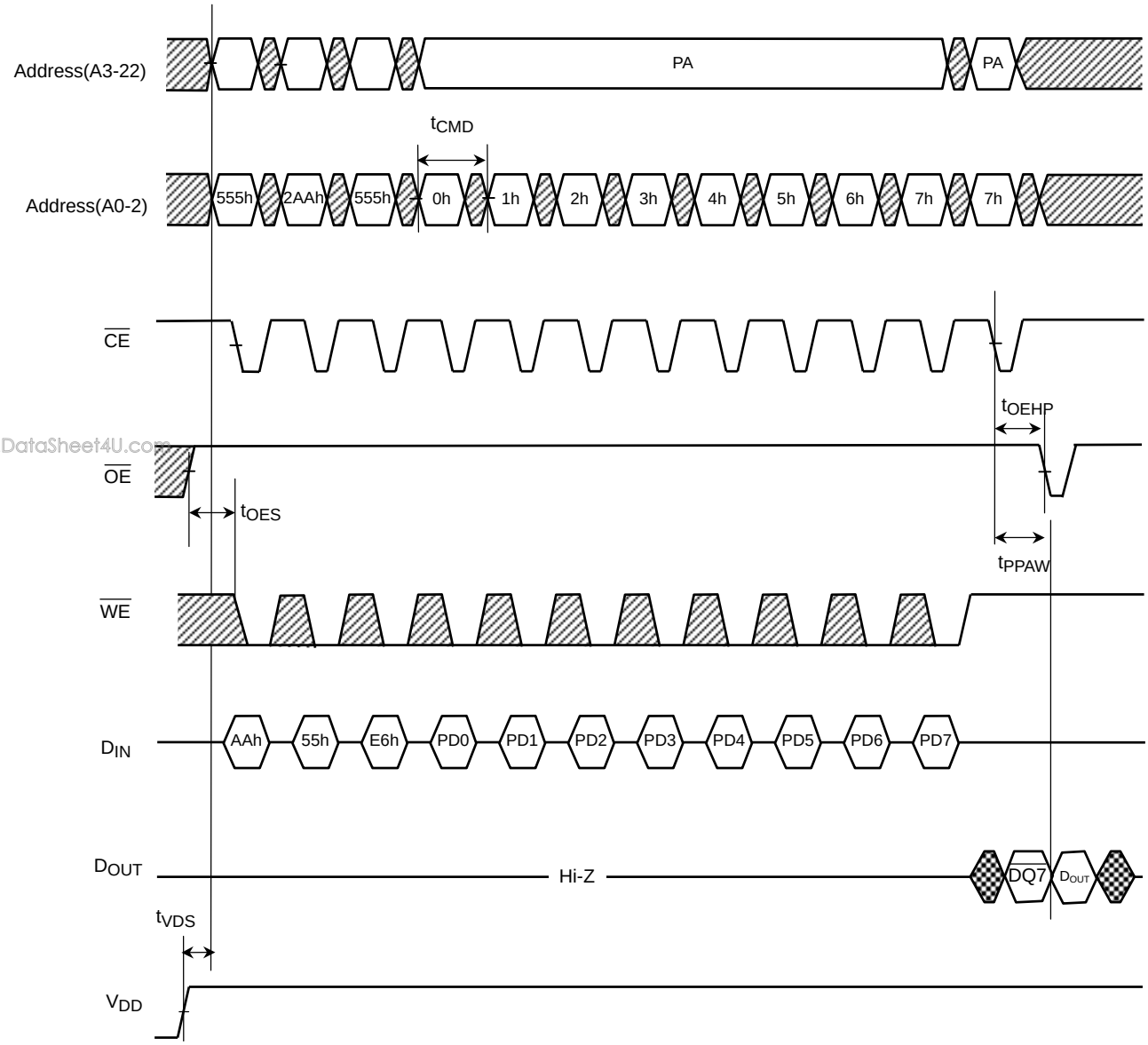
Auto Page Program Operation ($\overline{CE}$ Control)



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Notes: PA: Program address
PD: Program data

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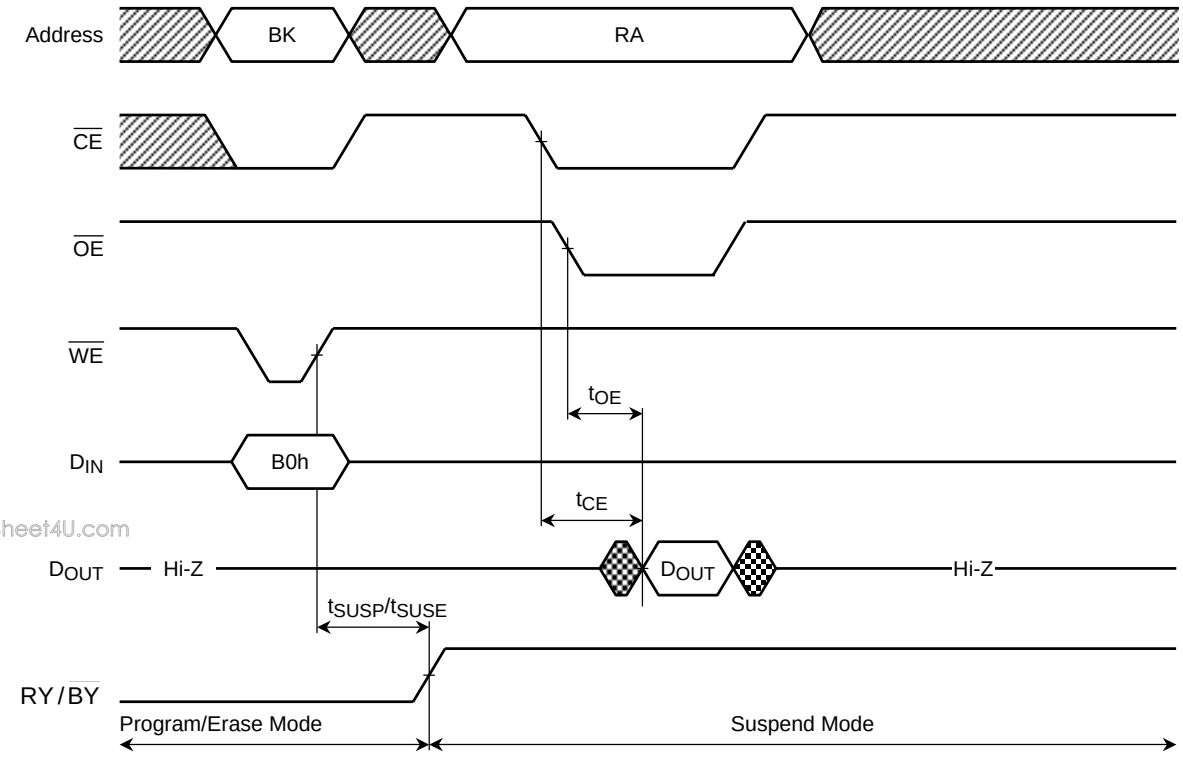
Program/Erase Suspend Operation



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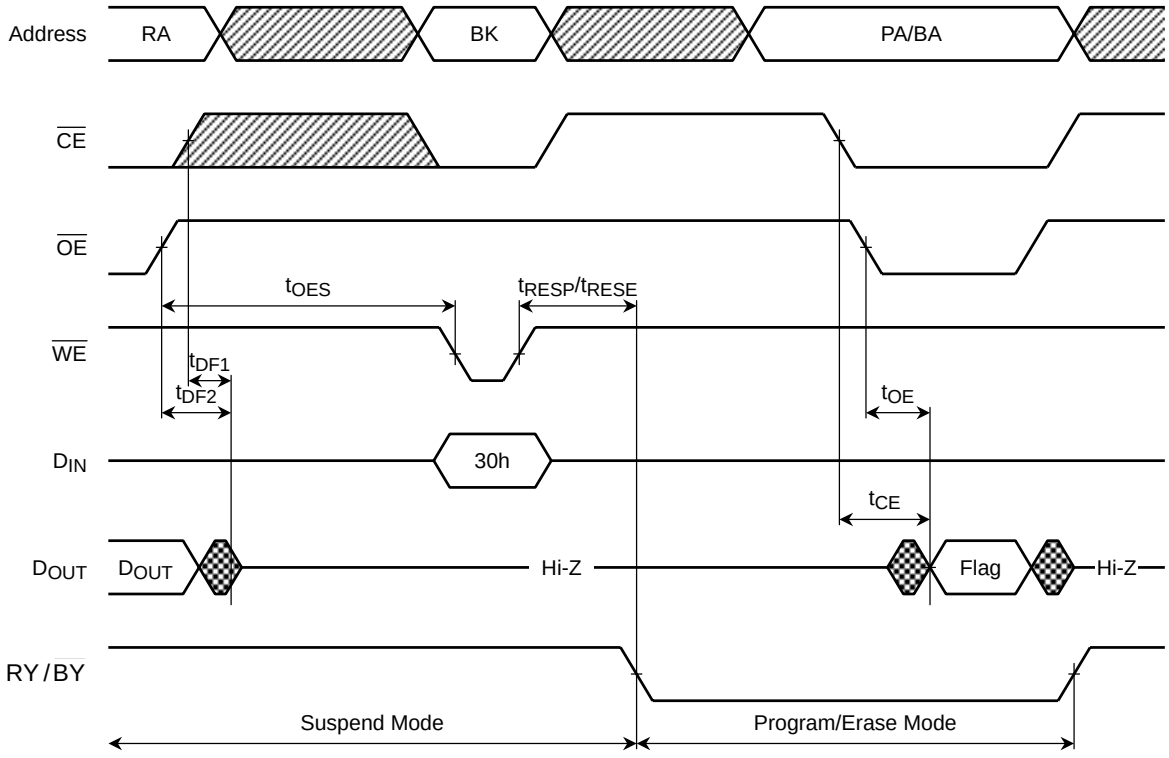
RA: Read address

Program/Erase Resume Operation



PA: Program address
BK: Bank address
BA: Block address
RA: Read address
Flag: Hardware Sequence flag

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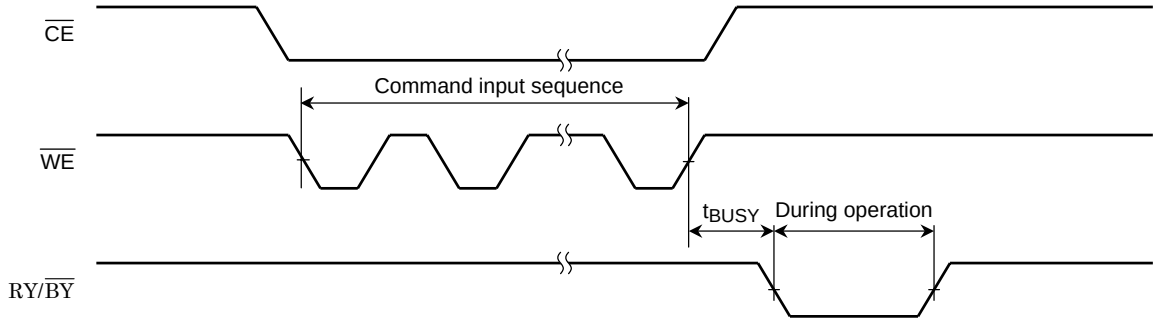
RY/$\overline{BY}$ during Auto Program/Erase Operation



Hardware Reset Operation (At the Auto Operation)

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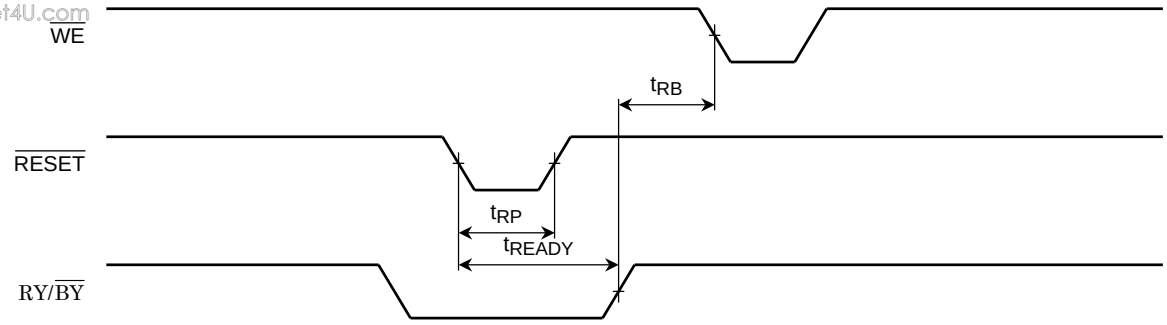
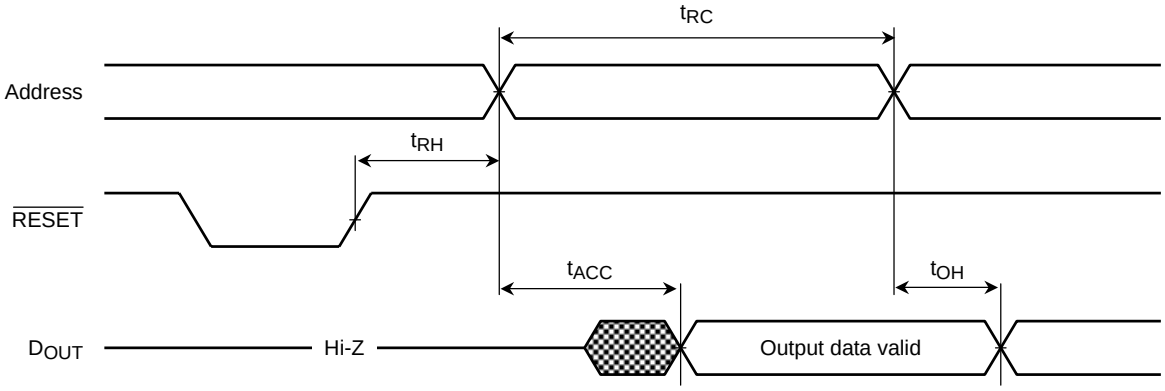


Read after $\overline{RESET}$



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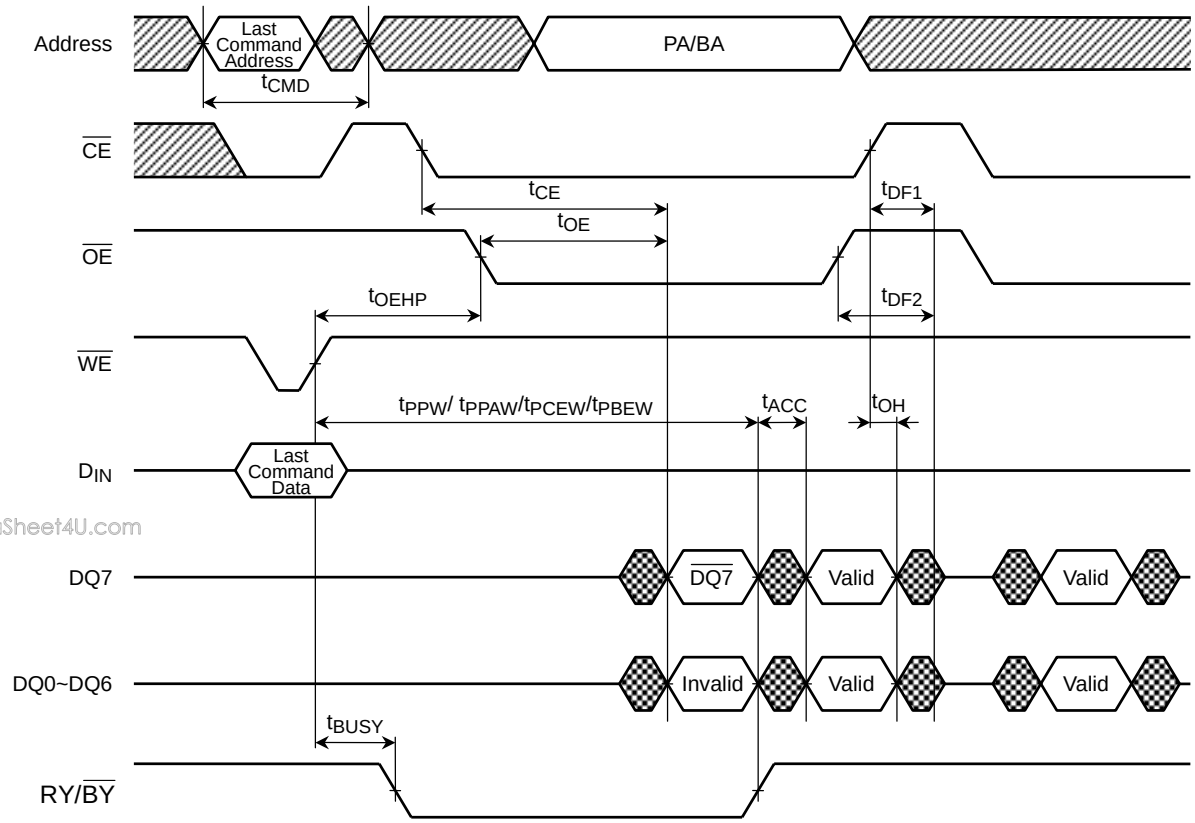
Hardware Sequence Flag ($\overline{\text{DATA}}$ Polling)



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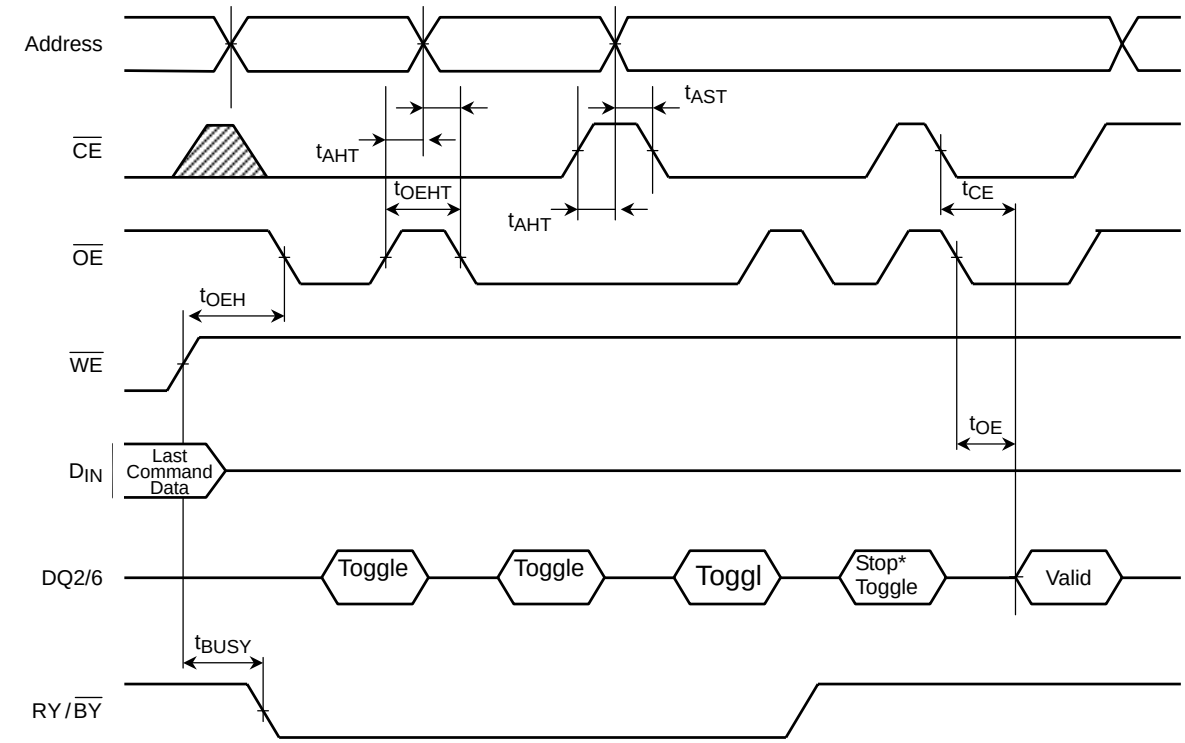
PA: Program address
BA: Block address

Hardware Sequence Flag (Toggle bit)



*DQ2/DQ6 stops toggling when auto operation has been completed.

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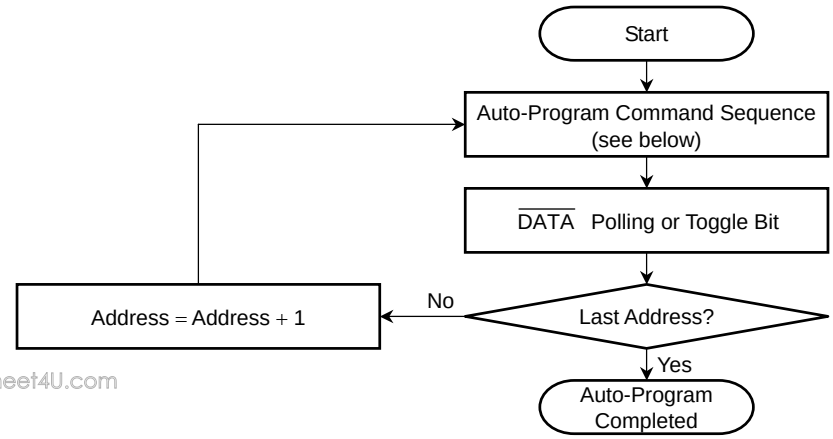
9. FLOWCHARTS

Auto-Program



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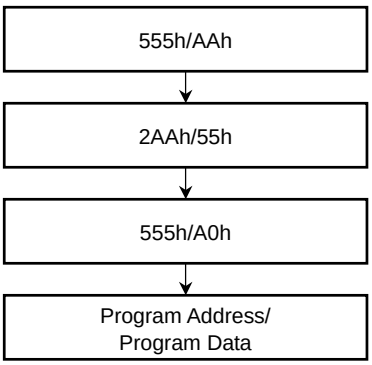
Auto-Program Command Sequence (address/data)



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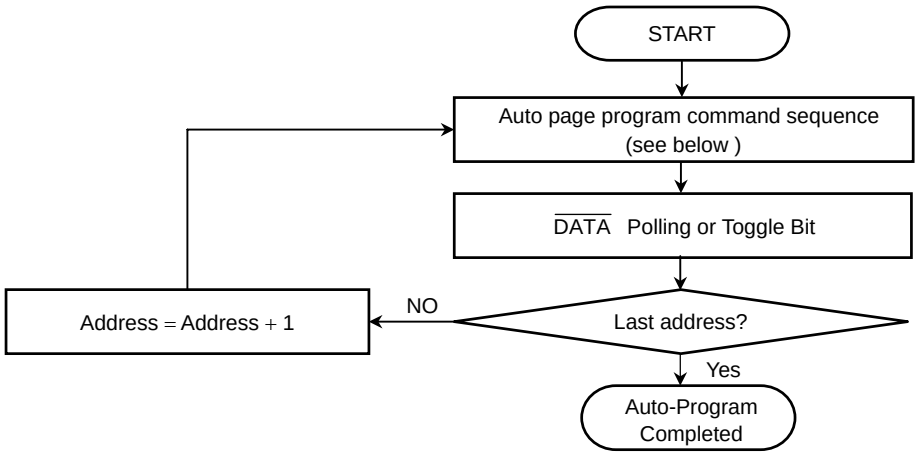
Auto-Page Program



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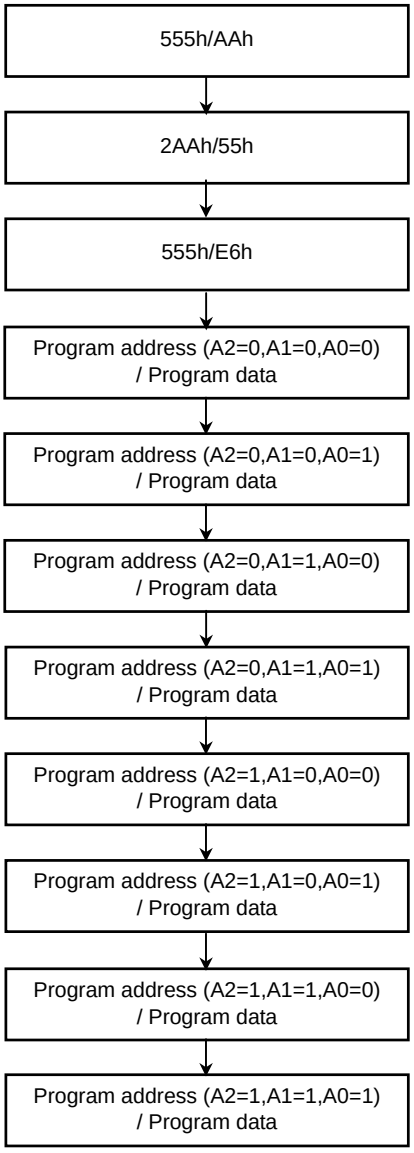

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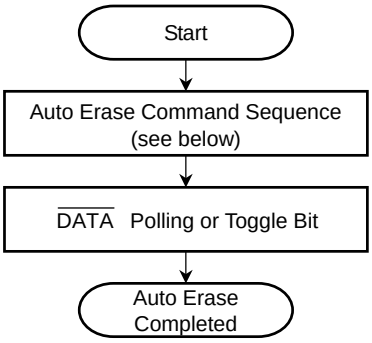
Auto Erase



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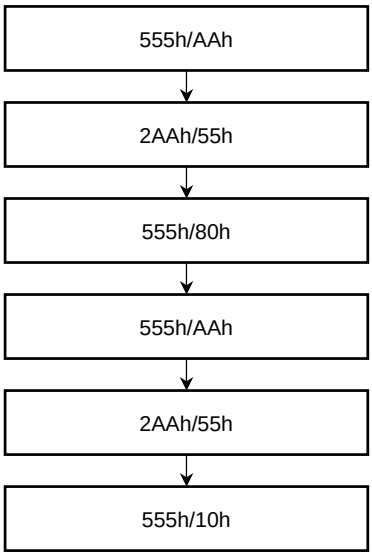
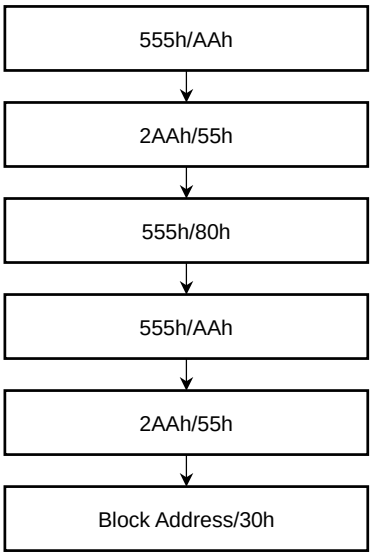
Auto Chip Erase Command Sequence
(address/data)



Auto Block Erase Command Sequence
(address/data)



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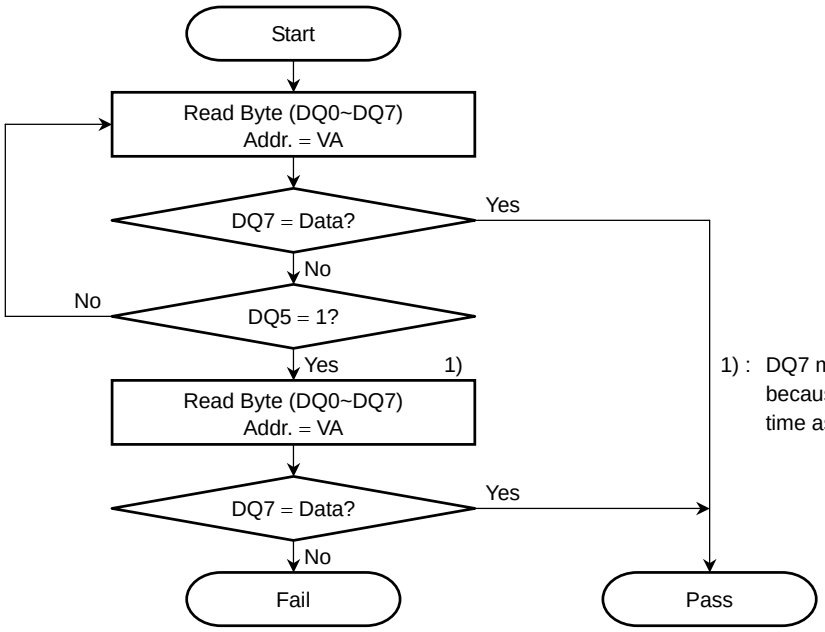
DQ7 $\overline{\text{DATA}}$ Polling



1) : DQ7 must be rechecked even if DQ5 = 1 because DQ7 may change at the same time as DQ5.

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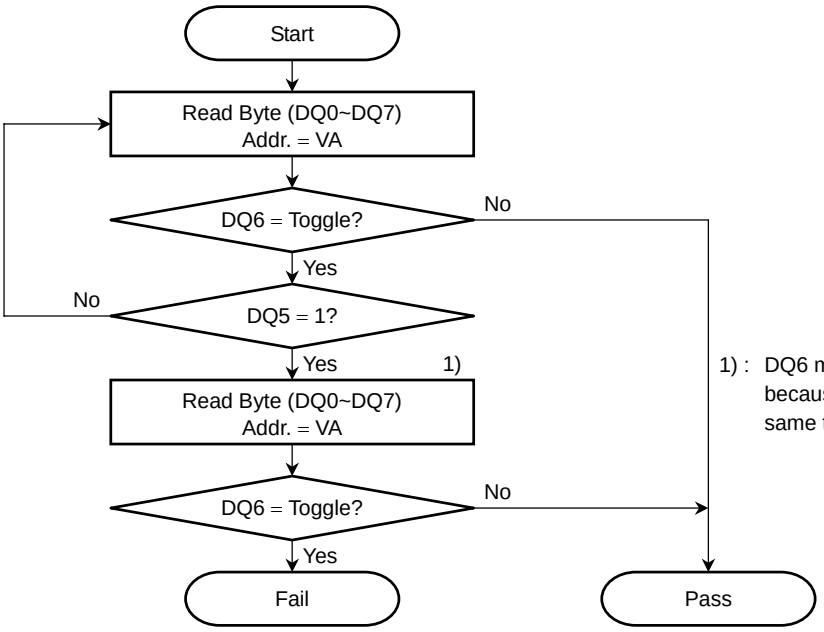
DQ6 Toggle Bit



1) : DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same times that DQ5 changes to 1.

VA: Valid address for programming
Any of the addresses within the block being erased during a Block Erase operation
"Don't care" during a Chip Erase operation

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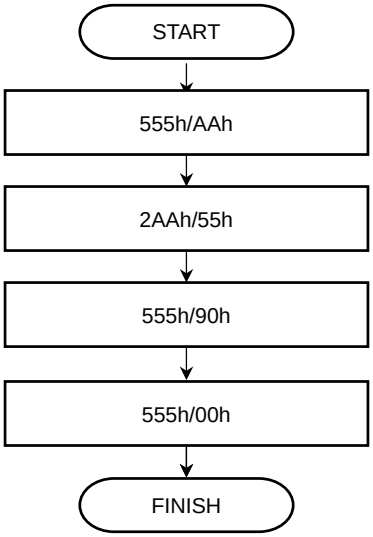
Hidden ROM Exit Command Input



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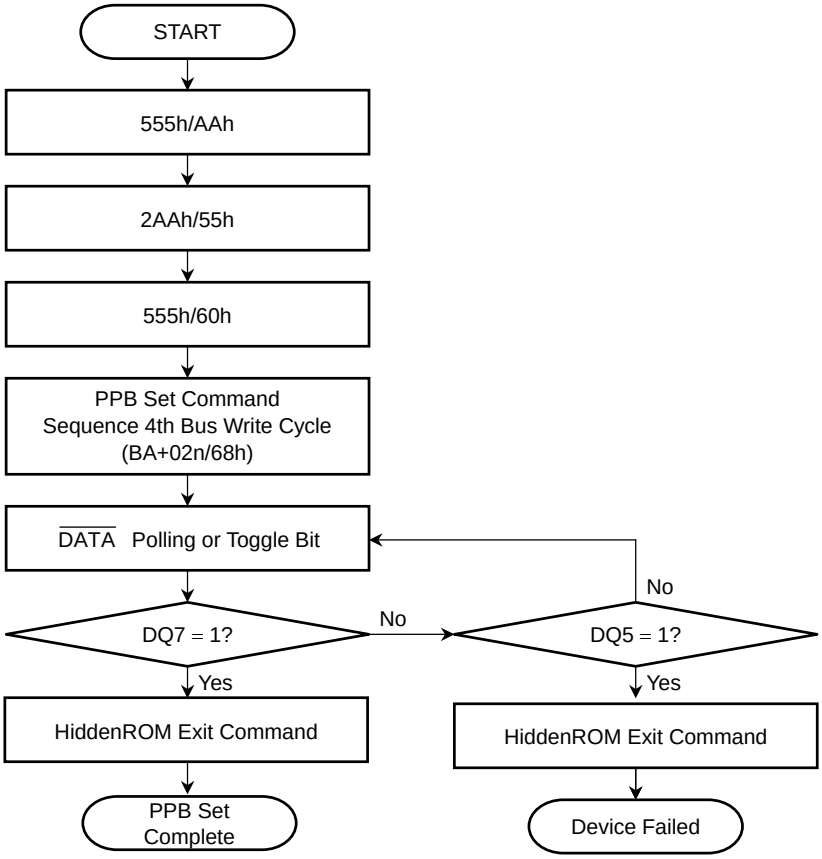
PPB Set Command Sequence



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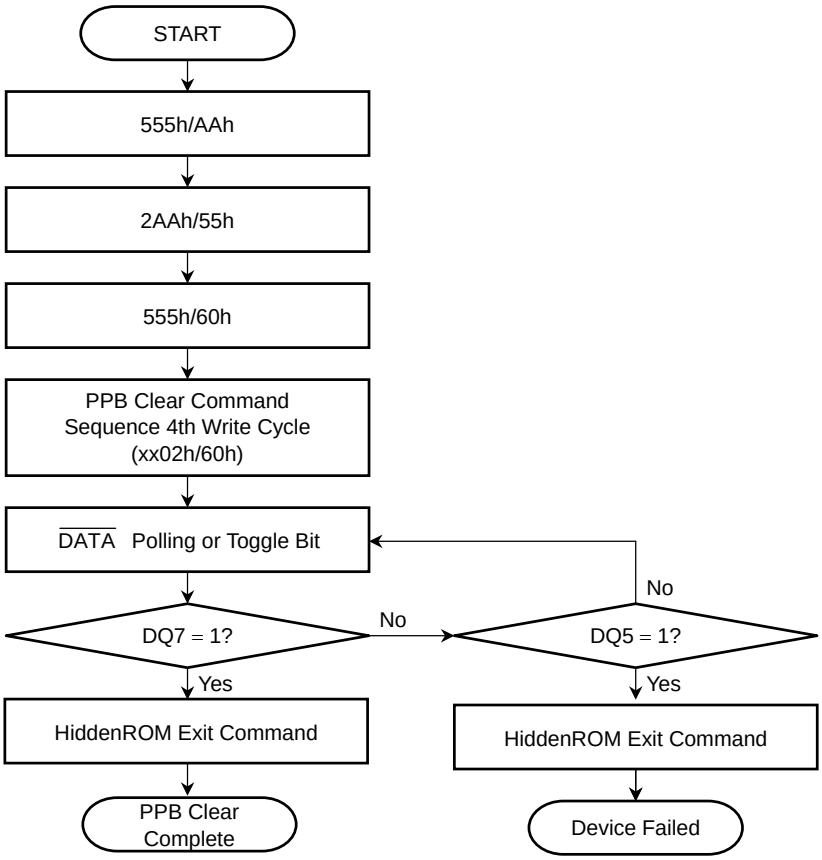
PPB Clear Command Sequence



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10. BLOCK ADDRESS TABLES

* : V_{IH} or V_{IL}

10.1. TC58FVM7TDD (Top Boot Block) 1/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK0	BA0	L	L	L	L	L	L	L	*	*	*	000000h~00FFFFh
	BA1	L	L	L	L	L	L	H	*	*	*	010000h~01FFFFh
	BA2	L	L	L	L	L	H	L	*	*	*	020000h~02FFFFh
	BA3	L	L	L	L	L	H	H	*	*	*	030000h~03FFFFh
	BA4	L	L	L	L	H	L	L	*	*	*	040000h~04FFFFh
	BA5	L	L	L	L	H	L	H	*	*	*	050000h~05FFFFh
	BA6	L	L	L	L	H	H	L	*	*	*	060000h~06FFFFh
	BA7	L	L	L	L	H	H	H	*	*	*	070000h~07FFFFh
	BA8	L	L	L	H	L	L	L	*	*	*	080000h~08FFFFh
	BA9	L	L	L	H	L	L	H	*	*	*	090000h~09FFFFh
	BA10	L	L	L	H	L	H	L	*	*	*	0A0000h~0AFFFFh
	BA11	L	L	L	H	L	H	H	*	*	*	0B0000h~0BFFFFh
	BA12	L	L	L	H	H	L	L	*	*	*	0C0000h~0CFFFFh
	BA13	L	L	L	H	H	L	H	*	*	*	0D0000h~0DFFFFh
	BA14	L	L	L	H	H	H	L	*	*	*	0E0000h~0EFFFFh
	BA15	L	L	L	H	H	H	H	*	*	*	0F0000h~0FFFFFh
BK1	BA16	L	L	H	L	L	L	L	*	*	*	100000h~10FFFFh
	BA17	L	L	H	L	L	L	H	*	*	*	110000h~11FFFFh
	BA18	L	L	H	L	L	H	L	*	*	*	120000h~12FFFFh
	BA19	L	L	H	L	L	H	H	*	*	*	130000h~13FFFFh
	BA20	L	L	H	L	H	L	L	*	*	*	140000h~14FFFFh
	BA21	L	L	H	L	H	L	H	*	*	*	150000h~15FFFFh
	BA22	L	L	H	L	H	H	L	*	*	*	160000h~16FFFFh
	BA23	L	L	H	L	H	H	H	*	*	*	170000h~17FFFFh
	BA24	L	L	H	H	L	L	L	*	*	*	180000h~18FFFFh
	BA25	L	L	H	H	L	L	H	*	*	*	190000h~19FFFFh
	BA26	L	L	H	H	L	H	L	*	*	*	1A0000h~1AFFFFh
	BA27	L	L	H	H	L	H	H	*	*	*	1B0000h~1BFFFFh
	BA28	L	L	H	H	H	L	L	*	*	*	1C0000h~1CFFFFh
	BA29	L	L	H	H	H	L	H	*	*	*	1D0000h~1DFFFFh
	BA30	L	L	H	H	H	H	L	*	*	*	1E0000h~1EFFFFh
	BA31	L	L	H	H	H	H	H	*	*	*	1F0000h~1FFFFFh

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10.1. TC58FVM7TDD (Top Boot Block) 2/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK2	BA32	L	H	L	L	L	L	L	*	*	*	200000h~20FFFFh
	BA33	L	H	L	L	L	L	H	*	*	*	210000h~21FFFFh
	BA34	L	H	L	L	L	H	L	*	*	*	220000h~22FFFFh
	BA35	L	H	L	L	L	H	H	*	*	*	230000h~23FFFFh
	BA36	L	H	L	L	H	L	L	*	*	*	240000h~24FFFFh
	BA37	L	H	L	L	H	L	H	*	*	*	250000h~25FFFFh
	BA38	L	H	L	L	H	H	L	*	*	*	260000h~26FFFFh
	BA39	L	H	L	L	H	H	H	*	*	*	270000h~27FFFFh
	BA40	L	H	L	H	L	L	L	*	*	*	280000h~28FFFFh
	BA41	L	H	L	H	L	L	H	*	*	*	290000h~29FFFFh
	BA42	L	H	L	H	L	H	L	*	*	*	2A0000h~2AFFFFh
	BA43	L	H	L	H	L	H	H	*	*	*	2B0000h~2BFFFFh
	BA44	L	H	L	H	H	L	L	*	*	*	2C0000h~2CFFFFh
	BA45	L	H	L	H	H	L	H	*	*	*	2D0000h~2DFFFFh
	BA46	L	H	L	H	H	H	L	*	*	*	2E0000h~2EFFFFh
	BA47	L	H	L	H	H	H	H	*	*	*	2F0000h~2FFFFFh
BK3	BA48	L	H	H	L	L	L	L	*	*	*	300000h~30FFFFh
	BA49	L	H	H	L	L	L	H	*	*	*	310000h~31FFFFh
	BA50	L	H	H	L	L	H	L	*	*	*	320000h~32FFFFh
	BA51	L	H	H	L	L	H	H	*	*	*	330000h~33FFFFh
	BA52	L	H	H	L	H	L	L	*	*	*	340000h~34FFFFh
	BA53	L	H	H	L	H	L	H	*	*	*	350000h~35FFFFh
	BA54	L	H	H	L	H	H	L	*	*	*	360000h~36FFFFh
	BA55	L	H	H	L	H	H	H	*	*	*	370000h~37FFFFh
	BA56	L	H	H	H	L	L	L	*	*	*	380000h~38FFFFh
	BA57	L	H	H	H	L	L	H	*	*	*	390000h~39FFFFh
	BA58	L	H	H	H	L	H	L	*	*	*	3A0000h~3AFFFFh
	BA59	L	H	H	H	L	H	H	*	*	*	3B0000h~3BFFFFh
	BA60	L	H	H	H	H	L	L	*	*	*	3C0000h~3CFFFFh
	BA61	L	H	H	H	H	L	H	*	*	*	3D0000h~3DFFFFh
	BA62	L	H	H	H	H	H	L	*	*	*	3E0000h~3EFFFFh
	BA63	L	H	H	H	H	H	H	*	*	*	3F0000h~3FFFFFh

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10.1. TC58FVM7TDD (Top Boot Block) 3/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK4	BA64	H	L	L	L	L	L	L	*	*	*	400000h~40FFFFh
	BA65	H	L	L	L	L	L	H	*	*	*	410000h~41FFFFh
	BA66	H	L	L	L	L	H	L	*	*	*	420000h~42FFFFh
	BA67	H	L	L	L	L	H	H	*	*	*	430000h~43FFFFh
	BA68	H	L	L	L	H	L	L	*	*	*	440000h~44FFFFh
	BA69	H	L	L	L	H	L	H	*	*	*	450000h~45FFFFh
	BA70	H	L	L	L	H	H	L	*	*	*	460000h~46FFFFh
	BA71	H	L	L	L	H	H	H	*	*	*	470000h~47FFFFh
	BA72	H	L	L	H	L	L	L	*	*	*	480000h~48FFFFh
	BA73	H	L	L	H	L	L	H	*	*	*	490000h~49FFFFh
	BA74	H	L	L	H	L	H	L	*	*	*	4A0000h~4AFFFFh
	BA75	H	L	L	H	L	H	H	*	*	*	4B0000h~4BFFFFh
	BA76	H	L	L	H	H	L	L	*	*	*	4C0000h~4CFFFFh
	BA77	H	L	L	H	H	L	H	*	*	*	4D0000h~4DFFFFh
	BA78	H	L	L	H	H	H	L	*	*	*	4E0000h~4EFFFFh
	BA79	H	L	L	H	H	H	H	*	*	*	4F0000h~4FFFFFh
BK5	BA80	H	L	H	L	L	L	L	*	*	*	500000h~50FFFFh
	BA81	H	L	H	L	L	L	H	*	*	*	510000h~51FFFFh
	BA82	H	L	H	L	L	H	L	*	*	*	520000h~52FFFFh
	BA83	H	L	H	L	L	H	H	*	*	*	530000h~53FFFFh
	BA84	H	L	H	L	H	L	L	*	*	*	540000h~54FFFFh
	BA85	H	L	H	L	H	L	H	*	*	*	550000h~55FFFFh
	BA86	H	L	H	L	H	H	L	*	*	*	560000h~56FFFFh
	BA87	H	L	H	L	H	H	H	*	*	*	570000h~57FFFFh
	BA88	H	L	H	H	L	L	L	*	*	*	580000h~58FFFFh
	BA89	H	L	H	H	L	L	H	*	*	*	590000h~59FFFFh
	BA90	H	L	H	H	L	H	L	*	*	*	5A0000h~5AFFFFh
	BA91	H	L	H	H	L	H	H	*	*	*	5B0000h~5BFFFFh
	BA92	H	L	H	H	H	L	L	*	*	*	5C0000h~5CFFFFh
	BA93	H	L	H	H	H	L	H	*	*	*	5D0000h~5DFFFFh
	BA94	H	L	H	H	H	H	L	*	*	*	5E0000h~5EFFFFh
	BA95	H	L	H	H	H	H	H	*	*	*	5F0000h~5FFFFFh

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10.1. TC58FVM7TDD (Top Boot Block) 4/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK6	BA96	H	H	L	L	L	L	L	*	*	*	600000h~60FFFFh
	BA97	H	H	L	L	L	L	H	*	*	*	610000h~61FFFFh
	BA98	H	H	L	L	L	H	L	*	*	*	620000h~62FFFFh
	BA99	H	H	L	L	L	H	H	*	*	*	630000h~63FFFFh
	BA100	H	H	L	L	H	L	L	*	*	*	640000h~64FFFFh
	BA101	H	H	L	L	H	L	H	*	*	*	650000h~65FFFFh
	BA102	H	H	L	L	H	H	L	*	*	*	660000h~66FFFFh
	BA103	H	H	L	L	H	H	H	*	*	*	670000h~67FFFFh
	BA104	H	H	L	H	L	L	L	*	*	*	680000h~68FFFFh
	BA105	H	H	L	H	L	L	H	*	*	*	690000h~69FFFFh
	BA106	H	H	L	H	L	H	L	*	*	*	6A0000h~6AFFFFh
	BA107	H	H	L	H	L	H	H	*	*	*	6B0000h~6BFFFFh
	BA108	H	H	L	H	H	L	L	*	*	*	6C0000h~6CFFFFh
	BA109	H	H	L	H	H	L	H	*	*	*	6D0000h~6DFFFFh
	BA110	H	H	L	H	H	H	L	*	*	*	6E0000h~6EFFFFh
	BA111	H	H	L	H	H	H	H	*	*	*	6F0000h~6FFFFFh
BK7	BA112	H	H	H	L	L	L	L	*	*	*	700000h~70FFFFh
	BA113	H	H	H	L	L	L	H	*	*	*	710000h~71FFFFh
	BA114	H	H	H	L	L	H	L	*	*	*	720000h~72FFFFh
	BA115	H	H	H	L	L	H	H	*	*	*	730000h~73FFFFh
	BA116	H	H	H	L	H	L	L	*	*	*	740000h~74FFFFh
	BA117	H	H	H	L	H	L	H	*	*	*	750000h~75FFFFh
	BA118	H	H	H	L	H	H	L	*	*	*	760000h~76FFFFh
	BA119	H	H	H	L	H	H	H	*	*	*	770000h~77FFFFh
	BA120	H	H	H	H	L	L	L	*	*	*	780000h~78FFFFh
	BA121	H	H	H	H	L	L	H	*	*	*	790000h~79FFFFh
	BA122	H	H	H	H	L	H	L	*	*	*	7A0000h~7AFFFFh
	BA123	H	H	H	H	L	H	H	*	*	*	7B0000h~7BFFFFh
	BA124	H	H	H	H	H	L	L	*	*	*	7C0000h~7CFFFFh
	BA125	H	H	H	H	H	L	H	*	*	*	7D0000h~7DFFFFh
	BA126	H	H	H	H	H	H	L	*	*	*	7E0000h~7EFFFFh

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10.1. TC58FVM7TDD (Top Boot Block) 5/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK7	BA127	H	H	H	H	H	H	H	L	L	L	7F0000h~7F1FFFh
	BA128	H	H	H	H	H	H	H	L	L	H	7F2000h~7F3FFFh
	BA129	H	H	H	H	H	H	H	L	H	L	7F4000h~7F5FFFh
	BA130	H	H	H	H	H	H	H	L	H	H	7F6000h~7F7FFFh
	BA131	H	H	H	H	H	H	H	H	L	L	7F8000h~7F9FFFh
	BA132	H	H	H	H	H	H	H	H	L	H	7FA000h~7FBFFFh
	BA133	H	H	H	H	H	H	H	H	H	L	7FC000h~7FDFFFh
	BA134	H	H	H	H	H	H	H	H	H	H	7FE000h~7FFFFFh

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10.2. TC58FVM7BDD (Bottom Boot Block) 1/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK0	BA0	L	L	L	L	L	L	L	L	L	L	000000h~001FFFh
	BA1	L	L	L	L	L	L	L	L	L	H	002000h~003FFFh
	BA2	L	L	L	L	L	L	L	L	H	L	004000h~005FFFh
	BA3	L	L	L	L	L	L	L	L	H	H	006000h~007FFFh
	BA4	L	L	L	L	L	L	L	H	L	L	008000h~009FFFh
	BA5	L	L	L	L	L	L	L	H	L	H	00A000h~00BFFFh
	BA6	L	L	L	L	L	L	L	H	H	L	00C000h~00DFFFh
	BA7	L	L	L	L	L	L	L	H	H	H	00E000h~00FFFFh

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10.2. TC58FVM7BDD (Bottom Boot Block) 2/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK0	BA8	L	L	L	L	L	L	H	*	*	*	010000h~01FFFFh
	BA9	L	L	L	L	L	H	L	*	*	*	020000h~02FFFFh
	BA10	L	L	L	L	L	H	H	*	*	*	030000h~03FFFFh
	BA11	L	L	L	L	H	L	L	*	*	*	040000h~04FFFFh
	BA12	L	L	L	L	H	L	H	*	*	*	050000h~05FFFFh
	BA13	L	L	L	L	H	H	L	*	*	*	060000h~06FFFFh
	BA14	L	L	L	L	H	H	H	*	*	*	070000h~07FFFFh
	BA15	L	L	L	H	L	L	L	*	*	*	080000h~08FFFFh
	BA16	L	L	L	H	L	L	H	*	*	*	090000h~09FFFFh
	BA17	L	L	L	H	L	H	L	*	*	*	0A0000h~0AFFFFh
	BA18	L	L	L	H	L	H	H	*	*	*	0B0000h~0BFFFFh
	BA19	L	L	L	H	H	L	L	*	*	*	0C0000h~0CFFFFh
	BA20	L	L	L	H	H	L	H	*	*	*	0D0000h~0DFFFFh
	BA21	L	L	L	H	H	H	L	*	*	*	0E0000h~0EFFFFh
	BA22	L	L	L	H	H	H	H	*	*	*	0F0000h~0FFFFFh
BK1	BA23	L	L	H	L	L	L	L	*	*	*	100000h~10FFFFh
	BA24	L	L	H	L	L	L	H	*	*	*	110000h~11FFFFh
	BA25	L	L	H	L	L	H	L	*	*	*	120000h~12FFFFh
	BA26	L	L	H	L	L	H	H	*	*	*	130000h~13FFFFh
	BA27	L	L	H	L	H	L	L	*	*	*	140000h~14FFFFh
	BA28	L	L	H	L	H	L	H	*	*	*	150000h~15FFFFh
	BA29	L	L	H	L	H	H	L	*	*	*	160000h~16FFFFh
	BA30	L	L	H	L	H	H	H	*	*	*	170000h~17FFFFh
	BA31	L	L	H	H	L	L	L	*	*	*	180000h~18FFFFh
	BA32	L	L	H	H	L	L	H	*	*	*	190000h~19FFFFh
	BA33	L	L	H	H	L	H	L	*	*	*	1A0000h~1AFFFFh
	BA34	L	L	H	H	L	H	H	*	*	*	1B0000h~1BFFFFh
	BA35	L	L	H	H	H	L	L	*	*	*	1C0000h~1CFFFFh
	BA36	L	L	H	H	H	L	H	*	*	*	1D0000h~1DFFFFh
	BA37	L	L	H	H	H	H	L	*	*	*	1E0000h~1EFFFFh
	BA38	L	L	H	H	H	H	H	*	*	*	1F0000h~1FFFFFh

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10.2. TC58FVM7BDD (Bottom Boot Block) 3/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK2	BA39	L	H	L	L	L	L	L	*	*	*	200000h~20FFFFh
	BA40	L	H	L	L	L	L	H	*	*	*	210000h~21FFFFh
	BA41	L	H	L	L	L	H	L	*	*	*	220000h~22FFFFh
	BA42	L	H	L	L	L	H	H	*	*	*	230000h~23FFFFh
	BA43	L	H	L	L	H	L	L	*	*	*	240000h~24FFFFh
	BA44	L	H	L	L	H	L	H	*	*	*	250000h~25FFFFh
	BA45	L	H	L	L	H	H	L	*	*	*	260000h~26FFFFh
	BA46	L	H	L	L	H	H	H	*	*	*	270000h~27FFFFh
	BA47	L	H	L	H	L	L	L	*	*	*	280000h~28FFFFh
	BA48	L	H	L	H	L	L	H	*	*	*	290000h~29FFFFh
	BA49	L	H	L	H	L	H	L	*	*	*	2A0000h~2AFFFFh
	BA50	L	H	L	H	L	H	H	*	*	*	2B0000h~2BFFFFh
	BA51	L	H	L	H	H	L	L	*	*	*	2C0000h~2CFFFFh
	BA52	L	H	L	H	H	L	H	*	*	*	2D0000h~2DFFFFh
	BA53	L	H	L	H	H	H	L	*	*	*	2E0000h~2EFFFFh
	BA54	L	H	L	H	H	H	H	*	*	*	2F0000h~2FFFFFh
BK3	BA55	L	H	H	L	L	L	L	*	*	*	300000h~30FFFFh
	BA56	L	H	H	L	L	L	H	*	*	*	310000h~31FFFFh
	BA57	L	H	H	L	L	H	L	*	*	*	320000h~32FFFFh
	BA58	L	H	H	L	L	H	H	*	*	*	330000h~33FFFFh
	BA59	L	H	H	L	H	L	L	*	*	*	340000h~34FFFFh
	BA60	L	H	H	L	H	L	H	*	*	*	350000h~35FFFFh
	BA61	L	H	H	L	H	H	L	*	*	*	360000h~36FFFFh
	BA62	L	H	H	L	H	H	H	*	*	*	370000h~37FFFFh
	BA63	L	H	H	H	L	L	L	*	*	*	380000h~38FFFFh
	BA64	L	H	H	H	L	L	H	*	*	*	390000h~39FFFFh
	BA65	L	H	H	H	L	H	L	*	*	*	3A0000h~3AFFFFh
	BA66	L	H	H	H	L	H	H	*	*	*	3B0000h~3BFFFFh
	BA67	L	H	H	H	H	L	L	*	*	*	3C0000h~3CFFFFh
	BA68	L	H	H	H	H	L	H	*	*	*	3D0000h~3DFFFFh
	BA69	L	H	H	H	H	H	L	*	*	*	3E0000h~3EFFFFh
	BA70	L	H	H	H	H	H	H	*	*	*	3F0000h~3FFFFFh

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10.2. TC58FVM7BDD (Bottom Boot Block) 4/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK4	BA71	H	L	L	L	L	L	L	*	*	*	400000h~40FFFFh
	BA72	H	L	L	L	L	L	H	*	*	*	410000h~41FFFFh
	BA73	H	L	L	L	L	H	L	*	*	*	420000h~42FFFFh
	BA74	H	L	L	L	L	H	H	*	*	*	430000h~43FFFFh
	BA75	H	L	L	L	H	L	L	*	*	*	440000h~44FFFFh
	BA76	H	L	L	L	H	L	H	*	*	*	450000h~45FFFFh
	BA77	H	L	L	L	H	H	L	*	*	*	460000h~46FFFFh
	BA78	H	L	L	L	H	H	H	*	*	*	470000h~47FFFFh
	BA79	H	L	L	H	L	L	L	*	*	*	480000h~48FFFFh
	BA80	H	L	L	H	L	L	H	*	*	*	490000h~49FFFFh
	BA81	H	L	L	H	L	H	L	*	*	*	4A0000h~4AFFFFh
	BA82	H	L	L	H	L	H	H	*	*	*	4B0000h~4BFFFFh
	BA83	H	L	L	H	H	L	L	*	*	*	4C0000h~4CFFFFh
	BA84	H	L	L	H	H	L	H	*	*	*	4D0000h~4DFFFFh
	BA85	H	L	L	H	H	H	L	*	*	*	4E0000h~4EFFFFh
	BA86	H	L	L	H	H	H	H	*	*	*	4F0000h~4FFFFFh
BK5	BA87	H	L	H	L	L	L	L	*	*	*	500000h~50FFFFh
	BA88	H	L	H	L	L	L	H	*	*	*	510000h~51FFFFh
	BA89	H	L	H	L	L	H	L	*	*	*	520000h~52FFFFh
	BA90	H	L	H	L	L	H	H	*	*	*	530000h~53FFFFh
	BA91	H	L	H	L	H	L	L	*	*	*	540000h~54FFFFh
	BA92	H	L	H	L	H	L	H	*	*	*	550000h~55FFFFh
	BA93	H	L	H	L	H	H	L	*	*	*	560000h~56FFFFh
	BA94	H	L	H	L	H	H	H	*	*	*	570000h~57FFFFh
	BA95	H	L	H	H	L	L	L	*	*	*	580000h~58FFFFh
	BA96	H	L	H	H	L	L	H	*	*	*	590000h~59FFFFh
	BA97	H	L	H	H	L	H	L	*	*	*	5A0000h~5AFFFFh
	BA98	H	L	H	H	L	H	H	*	*	*	5B0000h~5BFFFFh
	BA99	H	L	H	H	H	L	L	*	*	*	5C0000h~5CFFFFh
	BA100	H	L	H	H	H	L	H	*	*	*	5D0000h~5DFFFFh
	BA101	H	L	H	H	H	H	L	*	*	*	5E0000h~5EFFFFh
	BA102	H	L	H	H	H	H	H	*	*	*	5F0000h~5FFFFFh

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10.2. TC58FVM7BDD (Bottom Boot Block) 5/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	
BK6	BA103	H	H	L	L	L	L	L	*	*	*	600000h~60FFFFh
	BA104	H	H	L	L	L	L	H	*	*	*	610000h~61FFFFh
	BA105	H	H	L	L	L	H	L	*	*	*	620000h~62FFFFh
	BA106	H	H	L	L	L	H	H	*	*	*	630000h~63FFFFh
	BA107	H	H	L	L	H	L	L	*	*	*	640000h~64FFFFh
	BA108	H	H	L	L	H	L	H	*	*	*	650000h~65FFFFh
	BA109	H	H	L	L	H	H	L	*	*	*	660000h~66FFFFh
	BA110	H	H	L	L	H	H	H	*	*	*	670000h~67FFFFh
	BA111	H	H	L	H	L	L	L	*	*	*	680000h~68FFFFh
	BA112	H	H	L	H	L	L	H	*	*	*	690000h~69FFFFh
	BA113	H	H	L	H	L	H	L	*	*	*	6A0000h~6AFFFFh
	BA114	H	H	L	H	L	H	H	*	*	*	6B0000h~6BFFFFh
	BA115	H	H	L	H	H	L	L	*	*	*	6C0000h~6CFFFFh
	BA116	H	H	L	H	H	L	H	*	*	*	6D0000h~6DFFFFh
	BA117	H	H	L	H	H	H	L	*	*	*	6E0000h~6EFFFFh
	BA118	H	H	L	H	H	H	H	*	*	*	6F0000h~6FFFFFh
BK7	BA119	H	H	H	L	L	L	L	*	*	*	700000h~70FFFFh
	BA120	H	H	H	L	L	L	H	*	*	*	710000h~71FFFFh
	BA121	H	H	H	L	L	H	L	*	*	*	720000h~72FFFFh
	BA122	H	H	H	L	L	H	H	*	*	*	730000h~73FFFFh
	BA123	H	H	H	L	H	L	L	*	*	*	740000h~74FFFFh
	BA124	H	H	H	L	H	L	H	*	*	*	750000h~75FFFFh
	BA125	H	H	H	L	H	H	L	*	*	*	760000h~76FFFFh
	BA126	H	H	H	L	H	H	H	*	*	*	770000h~77FFFFh
	BA127	H	H	H	H	L	L	L	*	*	*	780000h~78FFFFh
	BA128	H	H	H	H	L	L	H	*	*	*	790000h~79FFFFh
	BA129	H	H	H	H	L	H	L	*	*	*	7A0000h~7AFFFFh
	BA130	H	H	H	H	L	H	H	*	*	*	7B0000h~7BFFFFh
	BA131	H	H	H	H	H	L	L	*	*	*	7C0000h~7CFFFFh
	BA132	H	H	H	H	H	L	H	*	*	*	7D0000h~7DFFFFh
	BA133	H	H	H	H	H	H	L	*	*	*	7E0000h~7EFFFFh
	BA134	H	H	H	H	H	H	H	*	*	*	7F0000h~7FFFFFh

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11. BLOCK SIZE TABLE

11.1. TC58FVM7TDD (Top Boot Block)

BLOCK #	BLOCK SIZE	BANK #	BANK SIZE	BLOCK COUNT
BA0~BA15	64 Kwords x 16	BK0	1024Kwords	16
BA16~BA31	64 Kwords x 16	BK1	1024Kwords	16
BA32~BA47	64 Kwords x 16	BK2	1024Kwords	16
BA48~BA63	64 Kwords x 16	BK3	1024Kwords	16
BA64~BA79	64 Kwords x 16	BK4	1024Kwords	16
BA80~BA95	64 Kwords x 16	BK5	1024Kwords	16
BA96~BA111	64 Kwords x 16	BK6	1024Kwords	16
BA112~BA126	64 Kwords x 15	BK7	1024Kwords	23
BA127~BA134	8 Kwords x 8			

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11.2. TC58FVM7BDD (Bottom Boot Block)

BLOCK #	BLOCK SIZE	BANK #	BANK SIZE	BLOCK COUNT
BA0~BA7	8 Kwords x 8	BK0	1024Kwords	23
BA8~BA38	64 Kwords x 15			
BA39~BA70	64 Kwords x 16	BK1	1024Kwords	16
BA71~BA102	64 Kwords x 16	BK2	1024Kwords	16
BA103~BA134	64 Kwords x 16	BK3	1024Kwords	16
BA135~BA166	64 Kwords x 16	BK4	1024Kwords	16
BA167~BA198	64 Kwords x 16	BK5	1024Kwords	16
BA199~BA230	64 Kwords x 16	BK6	1024Kwords	16
BA231~BA262	64 Kwords x 16	BK7	1024Kwords	16

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