INTRODUCTION

The TrueView™ 5715 is a low pin count and low cost member of the TrueView™ family of advanced and highly integrated Multimedia Display Processors providing the key features needed to design the next generation progressive scan CRT Televisions.

The TrueView 5715 offers a unique solution to support and process video streams up to 1080I. It has a built-in de-Interlacer, advanced scaler, and dithering which enables a video source to stream through and be displayed without compromising the video quality.

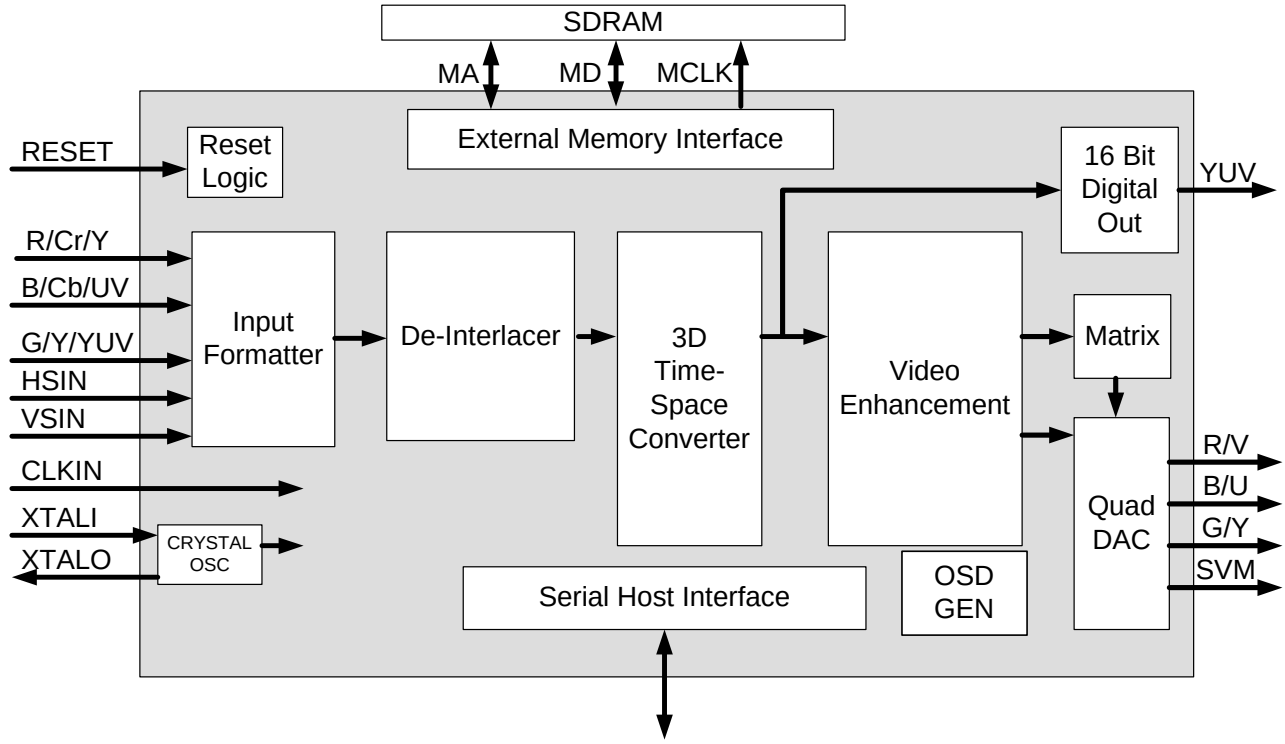
With the high quality video DACs, the video stream is displayed through its de-interlaced RGB/YPbPr outputs.

The I2C host interface enables OEMs to select from many different CPU's in order to meet their system and technical requirements.

OEMs can easily design a very low cost solution, while minimizing their software development time by leveraging on the TrueView 5715's level of integration and software support.

The TrueView 5715 provides 3D motion adaptive de-interlacing with diagonal detection. It performs high quality line doubling and high-accuracy motion estimation. It performs pixel- based motion estimation using two-field buffers. The Video Deinterlacing Processor automatically detects and can respond to noise thresholds (for improved mode detection) and still images (for reduced signal processing errors).

Additionally the TrueView 5715 includes an integrated OSD generator.



FEATURES

- **Input Formats**
  - 24-bit YCbCr/RGB
  - Single Video Port
  - 8 ITU-R BT.656
  - 8 or 16 bit ITU-R BT.601
  - Progressive/Interlaced
  - NTSC and PAL formats
  - 1080I, 1080P, 720P HD
  - Automatic format detection
  - 24 bit VGA, SVGA, XGA

- **Output Formats**
  - 480P, 540P, 576P, 720P, 1080I
  - 28-38K Hz Horizontal frequency
  - 50/60Hz to 100/120Hz double scan interlaced
  - 75Hz single scan interlaced
  - 50 - 75 Hz Scan Rate Conversion
  - YPbPr/RGB
  - Progressive 16 bit YCbCr with syncs

- **Video Enhancements**
  - Black and white level expansion
  - Color Transient Improvement (DCTI)
  - Dynamic Range expansion
  - Brightness, Saturation, Contrast
  - Dynamic Peaking
  - 2D coring
  - Scan Velocity Modulation (SVM)
  - Independent 2D up/down scaling
  - 3D Noise Reduction
  - Hue control
  - Vertical Peaking

- **De-Interlacer**
  - Direct Edge Correction De-interlace (DECD)
  - Motion Adaptive
  - Edge Adaptive
  - Mode Adaptive
  - Motion detection
  - Auto Noise detection
  - Still mode detection
  - 3:2/2:2 pull down mode detection

- **OSD**
  - OSD generator

- **Digital to Analog Conversion**
  - 10 bit quality
  - Quadruple DAC

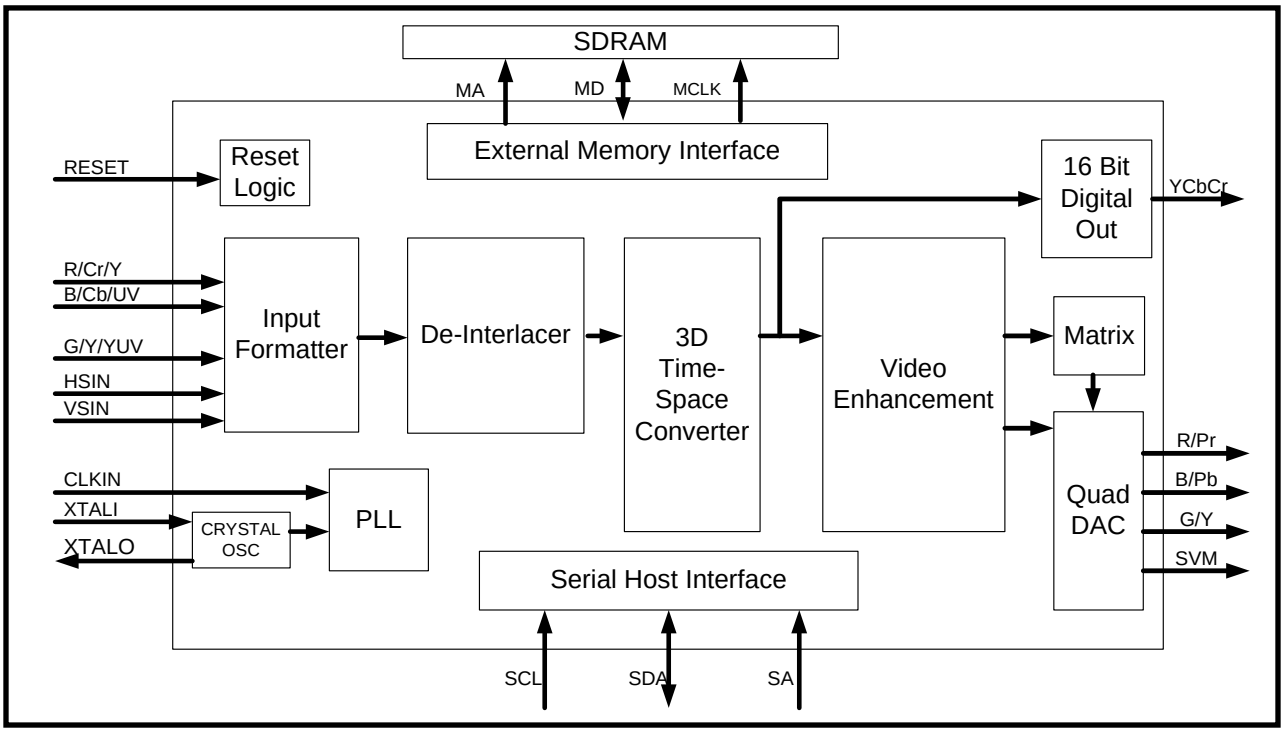
- **Memory**
  - SDRAM
  - 16 bits data access
  - 2/4/6/8 Mbytes

- **Host Interface and I/O**
  - 2 Wire serial bus
  - GPIO ports

- **100-Pin PQFP Package**
  - 0.35 Micron
  - 3.3V power supply

BLOCK DIAGRAM

Figure 1: Block Diagram



PIN DESCRIPTION

Table 1: Pin List

Pin #	Pin Name	Pin Description	I/O	Note
1	AGPb	Analog Blue/Pb output	O	
2	AGY	Analog Green/Y output	O	
3	AGPr	Analog Red/Pr output	O	
4	VG0	Video Green Input data0	I/O	Video Green
5	VG1	Video Green Input data1	I/O	Y data for YCbCr mode
6	VG2	Video Green Input data2	I/O	Y data for 8-bit 4:2:2 mode.
7	VG3	Video Green Input data3	I/O	
8	VG4	Video Green Input data4	I/O	
9	VG5	Video Green Input data5	I/O	
10	VG6	Video Green Input data6	I/O	
11	VG7	Video Green Input data7	I/O	
12	GPIO	GPIO	I/O	
13	SCLSA	Serial bus slave address selection	I/O	GPIO pin
14	VSS	Core Power GND	G	
15	VDD	3.3V Core Power	P	
16	SCLCK	Serial bus clock	I	
17	SCLDA	Serial bus data	I/O	(External pull up)
18	VB0	Video Blue Input data0	I/O	Video Blue
19	VB1	Video Blue Input data1	I/O	Cb data for YCbCr mode
20	VB2	Video Blue Input data2	I/O	CbCr data for 16-bit 4:2:2 mode.
21	CLKIN	Input Pixel Clock	I	Input clock
22	HSIN	Video Input HSYNC	I	Horizontal sync
23	VSIN	Video Input VSYNC	I	Vertical sync
24	RST	Asynchronous reset	I	Active low
25	PVDD	3.3V I/O Power	P	
26	XTALO	External crystal output	O	27 MHz crystal out (bypass open)
27	XTALI	External crystal input	I	27 MHz crystal out (bypass clock in)
28	PVSS	I/O GND	G	
29	PAVD	Analog power for PLL	P	
30	PAVS	Analog ground for PLL	G	
31	VB3	Video Blue Input data3	I/O	
32	VB4	Video Blue Input data4	I/O	
33	VB5	Video Blue Input data5	I/O	
34	VB6	Video Blue Input data6	I/O	
35	VB7	Video Blue Input data7	I/O	
36	VR0	Video Red Input data0	I/O	Video Red
37	VR1	Video Red Input data1	I/O	Cr data for YCbCr mode

Pin #	Pin Name	Pin Description	I/O	Note
38	VR2	Video Red Input data2	I/O	YCBCR data for 16-bit 4:2:2 mode.
39	VR3	Video Red Input data3	I/O	
40	VR4	Video Red Input data4	I/O	
41	VR5	Video Red Input data5	I/O	
42	VR6	Video Red Input data6	I/O	
43	VR7	Video Red Input data7	I/O	
44	PVDD	3.3V Digital Power	P	
45	PVSS	Digital GND	G	
46	MD0	Memory Data Bus 0	I/O	
47	MD15	Memory Data Bus 15	I/O	
48	MD1	Memory Data Bus 1	I/O	
49	MD14	Memory Data Bus 14	I/O	
50	MD2	Memory Data Bus 2	I/O	
51	MD13	Memory Data Bus 13	I/O	
52	MD3	Memory Data Bus 3	I/O	
53	MD12	Memory Data Bus 12	I/O	
54	MD4	Memory Data Bus 4	I/O	
55	PVDD	3.3V I/O Power	P	
56	PVSS	I/O GND	G	
57	MD11	Memory Data Bus 11	I/O	
58	MD5	Memory Data Bus 5	I/O	
59	MD10	Memory Data Bus 10	I/O	
60	MD6	Memory Data Bus 6	I/O	
61	MD9	Memory Data Bus 9	I/O	
62	MD7	Memory Data Bus 7	I/O	
63	MD8	Memory Data Bus 8	I/O	
64	DQM#	SDRAM data qualify signal	O	
65	PVDD	3.3V I/O Power	P	
66	SDCLK	SDRAM clock	O	
67	PVSS	I/O GND	G	
68	WE#	Write control for SDRAM	O	
69	RAS#	Row address strobe	O	
70	CAS#	Column address strobe	O	
71	FBCLK	Feed back clock for memory controller	I	
72	BA	SDRAM bank select	O	
73	CS1#	Chip Selection 1	O	
74	VSS	Core Power GND	G	
75	VDD	3.3V Core Power	P	
76	CS0#	Chip Selection 0	O	
77	MA9	Memory address bus 9	I/O	
78	MA10	Memory address bus 10	I/O	
79	PVDD	3.3V I/O Power	P	
80	PVSS	I/O GND	G	

Pin #	Pin Name	Pin Description	I/O	Note
81	MA8	Memory address bus 8	I/O	
82	MA0	Memory address bus 0	I/O	
83	MA7	Memory address bus 7	I/O	
84	MA1	Memory address bus 1	I/O	
85	MA6	Memory address bus 6	I/O	
86	MA2	Memory address bus 2	I/O	
87	MA5	Memory address bus 5	I/O	
88	MA3	Memory address bus 3	I/O	
89	MA4	Memory address bus 4	I/O	
90	HALF	Half contrast control input	I/O	GPIO pin
91	PVDD	3.3V I/O Power	P	
92	PVSS	I/O GND	G	
93	CLKOUT	Output Pixel Clock	O	Display clock output
94	HSOUT	Video Output HSYNC	O	Horizontal sync
95	VSOUT	Video Output VSYNC	O	Vertical sync
96	DVSS	DAC GND	G	
97	ASVM	Analog SVM output	O	
98	IREF	Full-scale adjust resistor	I	
99	DAVS	Analog ground for DAC	G	
100	DAVD	Analog power for DAC	P	

Note

- Pin Type Definition

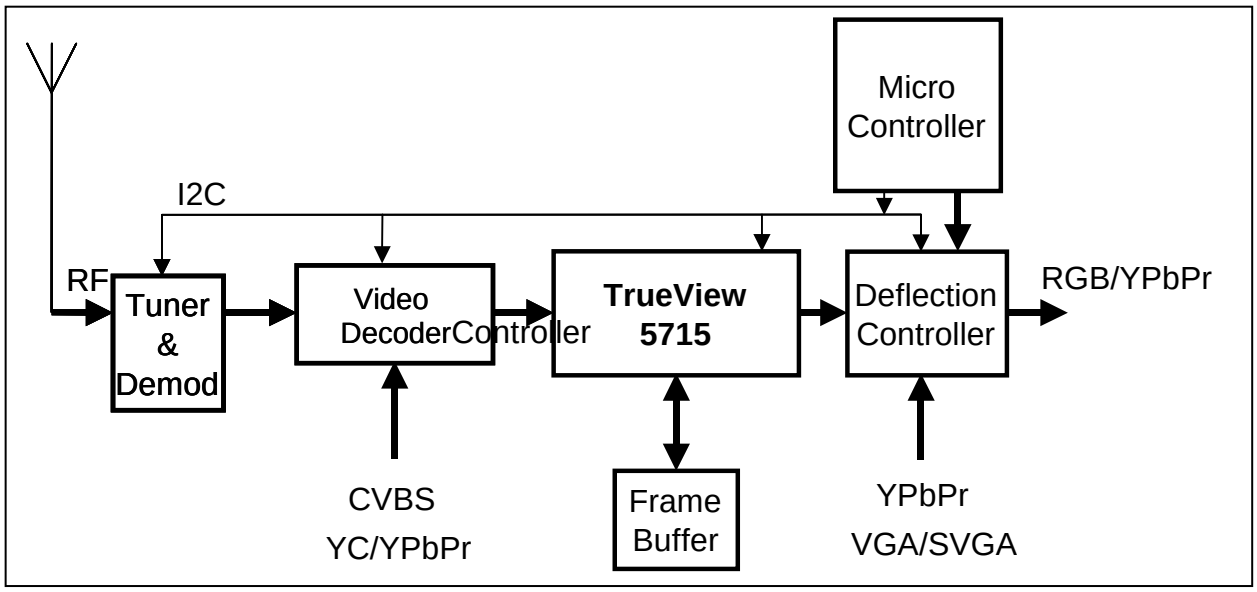
  I = Input
  O = Output
  G = Ground
  P = Power

APPLICATION: TV SYSTEMS

The following diagrams show three possible TV system configurations.

TV SYSTEM 1

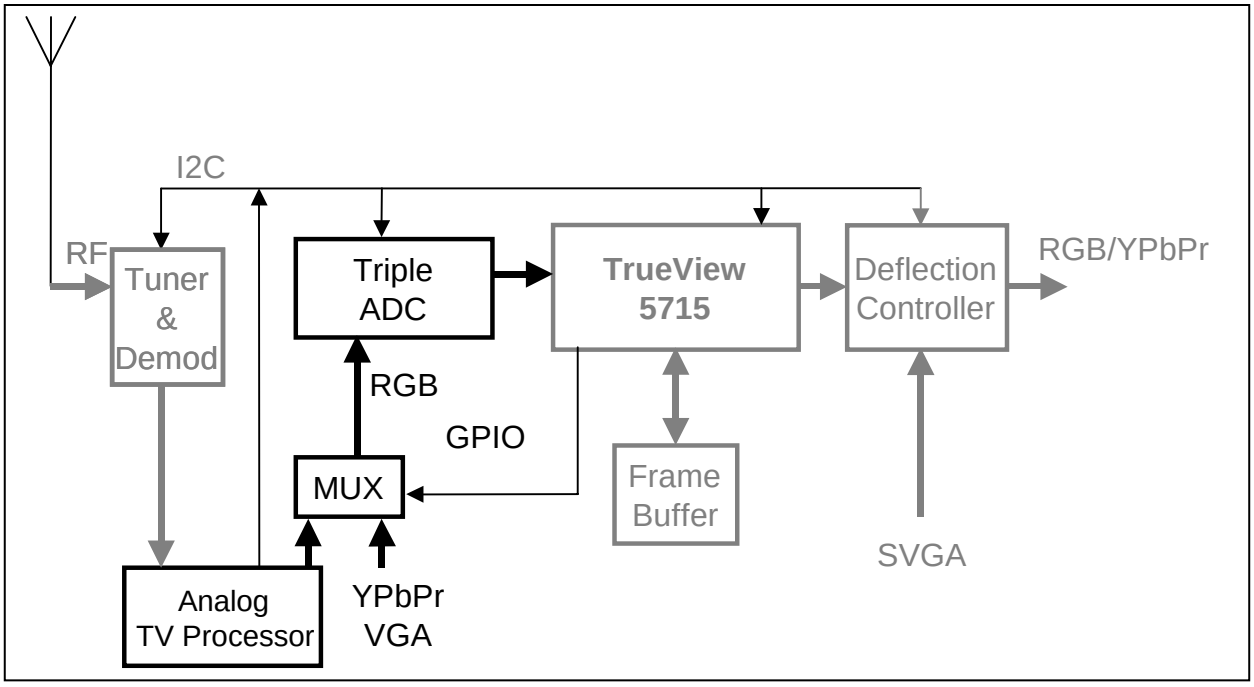
Figure 3: TV system 1



TV system 1 shows a basic TV system that uses a standard video decoder to provide the interlaced input to the TrueView 5715.

TV SYSTEM 3

Figure 5: TV system 3



TV System 3 shows the block diagram of a TV that uses a standard TV system processor that could contain a microcontroller and VBI decoder. The analog output of the TV processor is input to a triple analog to digital converter through an optional multiplexer that allows the input of external analog TV signals.

FUNCTIONAL DESCRIPTION

The TrueView 5715 TV Display Processor consists the following functional blocks:

- Input Formatter
- De-interlacer
- 3D Time-Space Converter
- Video Enhancer
- Output Formatter
- Analog and Digital Output
- Memory Controller
- PLL and Oscillator
- Serial Host Interface
- OSD Engine

INPUT FORMATTER

The Input Formatter accepts video data in several formats.

- 24-bit YCbCr or RGB
- 4:4:4 or 4:2:2
- 8 bit ITU-R BT.656
- 8 or 16 or 24 bit ITU-R BT.601
- NTSC or PAL
- 24 bit VGA (800*525@60Hz), SVGA, XGA
- 1080i, 720p, 1080p, HD

The incoming video format can be automatically detected and can be interlaced or progressive.

DE-INTERLACER

The TrueView 5715 deinterlacer uses motion-detection techniques to produce a progressive scan video output. Noise which otherwise would be seen as motion can be removed during motion processing. It also uses an edge detection algorithm that enables the smoothing of jagged edges that could occur in the de-interlacing process. Several different detection angles can be programmed.

FILM MODE

The De-interlace Processor can detect video that has originated from film and detects 3:2 or 2:2 pull down. If film originated video is detected the two fields from the original frame are combined into one progressive frame.

Thirty frames per second interlaced video can be output as 60 or 72Hz progressive frames.

Twenty-five frames per second interlaced video can be output as 50 or 75Hz progressive frames, or 100Hz-interlaced fields.

The de-interlacer continuously monitors the incoming video to detect any changes to the pull-down sequence. If a change is detected the deinterlacer quickly adapts its de-interlacing algorithm to compensate.

3D TIME – SPACE CONVERTER

The 3D Time – Space converter is used to alter the size of the picture depending on the output resolution. It contains an Up-Down scaler and Rate converter.

VIDEO ENHANCER

The Video Enhancer is a high-quality programmable processor that brings out details and color in the video.

Luminance Peaking Filter

The Luminance Peaking Filter can alter the frequency response of the luminance signal by selectively increasing the amplitude.

DCTI

Enhanced Chroma Transient improvement (ELCTI) improves video by replacing slower edges of the video with edges that have steeper rise and fall times. DCTI turns sloped or sinusoidal waveforms into rectangular or square waveforms with the same duty cycles and peak-to-peak amplitude. It improves the color transitions of vertical objects and reduces color smearing introduced by a video decoder.

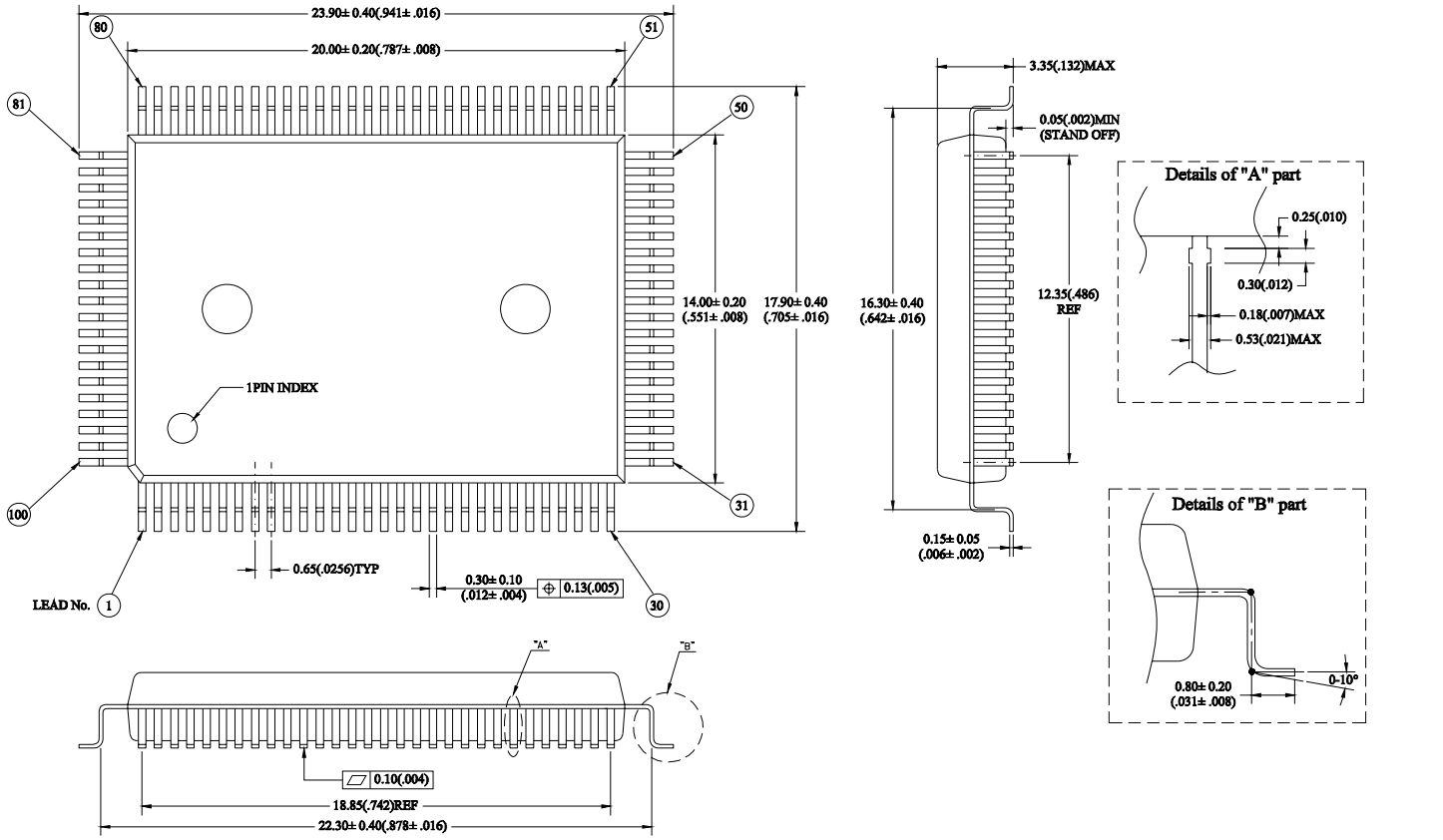



Figure 11: Package Dimensions