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4-CH 960H Video Decoders and Audio Codecs

TW2960

Features

Video Decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60) support with automatic format detection
- Software selectable analog inputs allows any of 2 CVBS per one video ADC
- Built-in analog anti-alias filter
- Four 10-bit ADCs and analog clamping circuit for CVBS input
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for CVBS channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, sharpness
- Automatic color control and color killer
- Chroma IF compensation
- ITU-R 656 like YCbCr(4:2:2) output or time multiplexed output with 72/144MHz

Audio Codecs

- Integrated five audio ADCs processing and one audio DAC
- Provides multi-channel audio mixed analog output
- Support I2S/DSP Master/Slave interface for record output and playback input
- PCM 8/16-bit and u-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz

Miscellaneous

- Two-wire MPU serial bus interface
- Integrated clock PLL for 144MHz clock output
- Power save and Power down mode
- Low power consumption
- Single 36MHz crystal for all standards
- 3.3V tolerant I/O
- 1.8V/3.3V power supply
- 100-pin LQFP package

Function Description

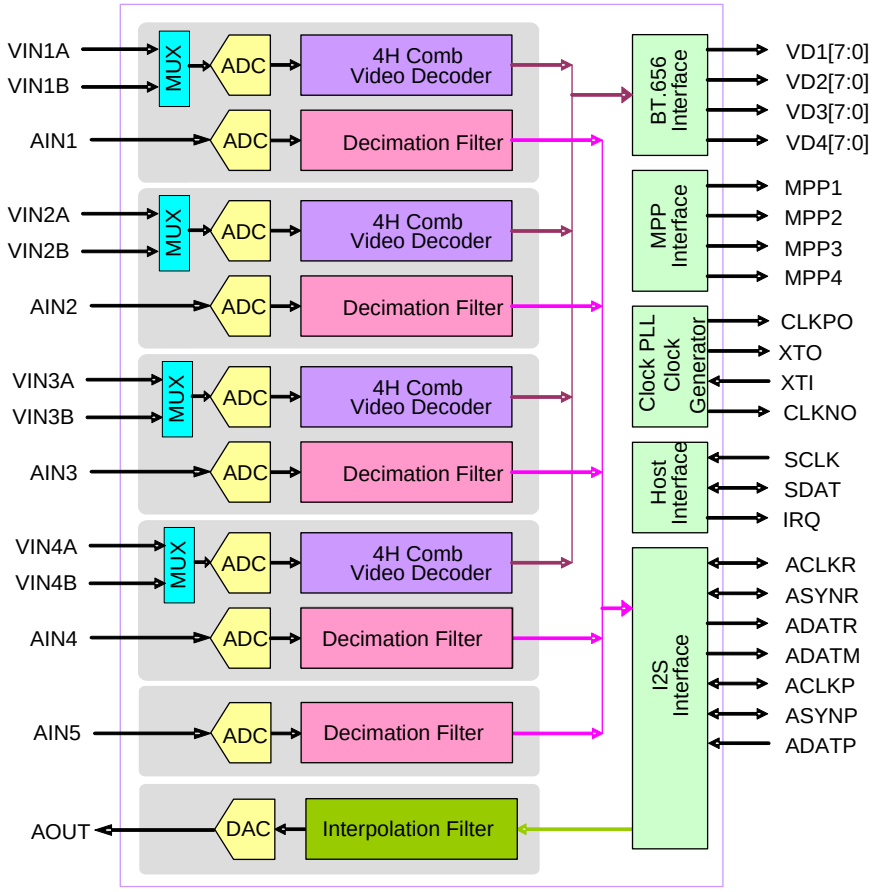


FIGURE 1. TW2960 BLOCK DIAGRAM

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2960-LA1-CR (Note 1)	TW2960 LA1-CR	100 Lead LQFP (12mmx12mm)	Q100.12X12

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Table of Contents

Video Decoder

VIDEO DECODER OVERVIEW

The TW2960 is a low power NTSC/PAL video decoder chip that is designed for video surveillance applications. It consumes very low power in a typical composite input application. The available power down mode further reduces the power consumption. It uses the 1.8V for both analog and digital supply voltage and 3.3V for I/O power. A single 36MHz crystal is all that needed to decode all analog video standards.

The video decoder decodes the base-band analog CVBS into digital 8-bit 4:2:2 YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43) and synchronization circuitry. The Y/C separation is done with high quality adaptive 4H (5-line) comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal.

Analog Front End

The analog front-end prepares and digitizes the AC coupled analog signal for further processing. Each channel has built-in anti-aliasing filter and 10-bit over-sampling ADCs. The characteristic of the filter is available in the filter curve section. The Y channel has additional 2-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). It can support a maximum input voltage range of 1.4V without attenuation. Software selectable analog inputs allow two selectable composite video inputs.

Sync Processor

The sync processor of TW2960 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward. It allows the sampling of the video signal in line-locked fashion.

Y/C Separation

For NTSC and PAL standard signals, the luma/chroma separation can be done either by adaptive comb filtering or notch/band-pass filter combination. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

TW2960 employs high quality 4-H (5-line) adaptive comb filter to reduce artifacts like hanging dots and crawling dots. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color Demodulation

The color demodulation of NTSC and PAL signal is done by first quadrature down mixing and then low-pass filtering. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

AUTOMATIC CHROMA GAIN CONTROL

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC control is –6db to +26db.

COLOR KILLER

For low color amplitude signals, black and white video or very noisy signals, the color will be suppressed or killed. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch-off the color.

AUTOMATIC STANDARD DETECTION

The TW2960 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC or PAL color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM. Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection. The SECAM standard can be recognized but not properly decoded.

TW2960 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW2960

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (Note 1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding
NTSC 50	625	50	3.579545 MHz	

NOTE:

1. NTSC-Japan has 0 IRE setup.

Component Processing

The TW2960 supports the brightness, contrast, color saturation and Hue adjustment for changing the video characteristic. The Cb and Cr gain can be adjusted independently for flexibility.

SHARPNESS

The TW2960 also provides a sharpness control function through control registers. It provides the control up to +9db. The center frequency of the enhancement curve is selectable. A coring function is provided to prevent noise enhancement.

COLOR TRANSIENT IMPROVEMENT

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Video Output Format

The TW2960 supports ITU-R BT.656 like format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data. In addition, the phase of CLKPO or CLKNO can be controlled by delay unit via the CLKPO_DEL or CLKNO_DEL registers and polarity inverse cell via the CLKPO_POL or CLKNO_POL registers independently.

CHANNEL ID

The channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Each ITU-R BT.656 like data stream in 4x960H output data, 2x960H output data can have this Sync Code and Blanking Code. Table 2 shows this Channel ID format. Nibble data value m shows Video Decoder number to be output in this video stream.

TABLE 2. THE CHANNEL ID FORMAT FOR 4X960H, 2X960H TIME-MULTIPLEXED FORMAT

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
Field	Vtime	Htime	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xFm
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEm
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDm
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xCm
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xBm
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAm
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9m
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x8m

(a) ITU-R BT.656 Sync Code with Channel ID

VIDEO	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
VINn	8'h1m	8'h8m	8'h8m

(b) Horizontal Blanking Code with Channel ID

As default, m = 0 Video1 656 data, m = 1 Video2 656 data, m = 2 Video3 656 data, m = 3 Video4 656 data. n = m+1.CH1NUM, CH2NUM, CH3NUM and CH4NUM registers can change this m value in each video channel output data if necessary.

VIDEO LOSS OUTPUT

When NOVID_656 register is set to 1, bit7 of Fourth byte of SAV/EAV code will be 0 when video signal is lost. This can be an optional set of 656 SAV/EAV code for no-video (video lost) specific application.

ITU-R BT.656 LIKE FORMAT

In ITU-R BT.656 like format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 2. The SAV and EAV sequences are shown in Table 3. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

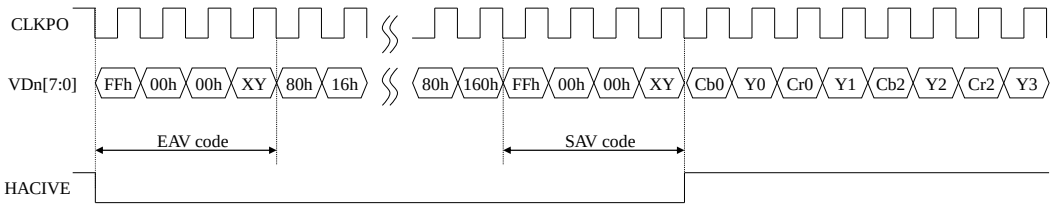


FIGURE 2. TIMING DIAGRAM OF ITU-R BT.656 LIKE FORMAT

TABLE 3. ITU-R BT.656 LIKE SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
									FOURTH	
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	NORMAL	OPTION (NOTE 1)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE:

1. Option includes video loss information in ITU-R BT.656 like format.

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 72MHZ

The TW2960 supports two channels ITU-R BT.656 like time-multiplexed format with 72MHz that is useful to security application requiring two channel outputs through one channel video port. The CHMDn register enables the dual ITU-R BT.656 like time-multiplexed format and the MAINCHn/SELCHn register selects channel output to be multiplexed with its own channel on each VD pins. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Figure 3 and Figure 4 illustrate VDn[7:0]/CLKPO/CLKNO pin timing with 72MHz/36MHz clock output mode.

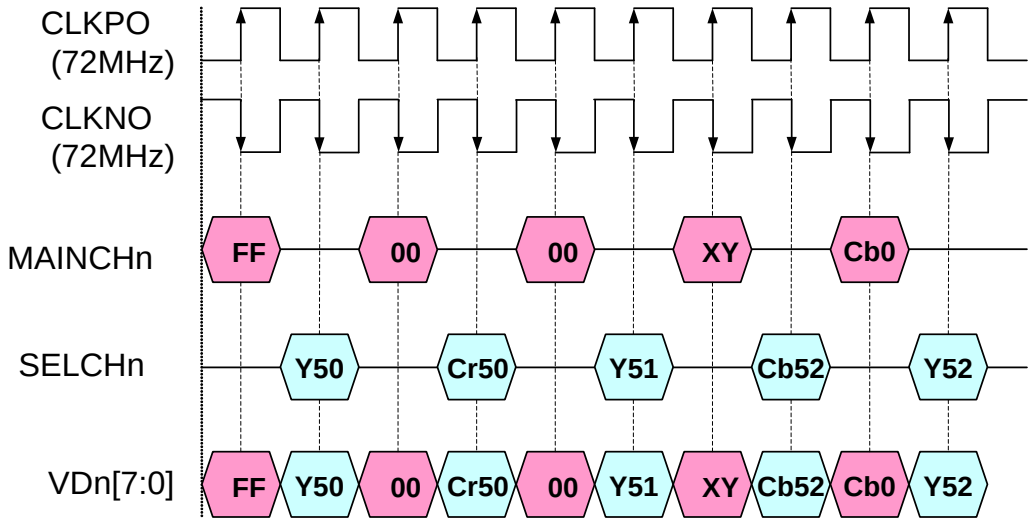


FIGURE 3. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 72MHZ CLOCK

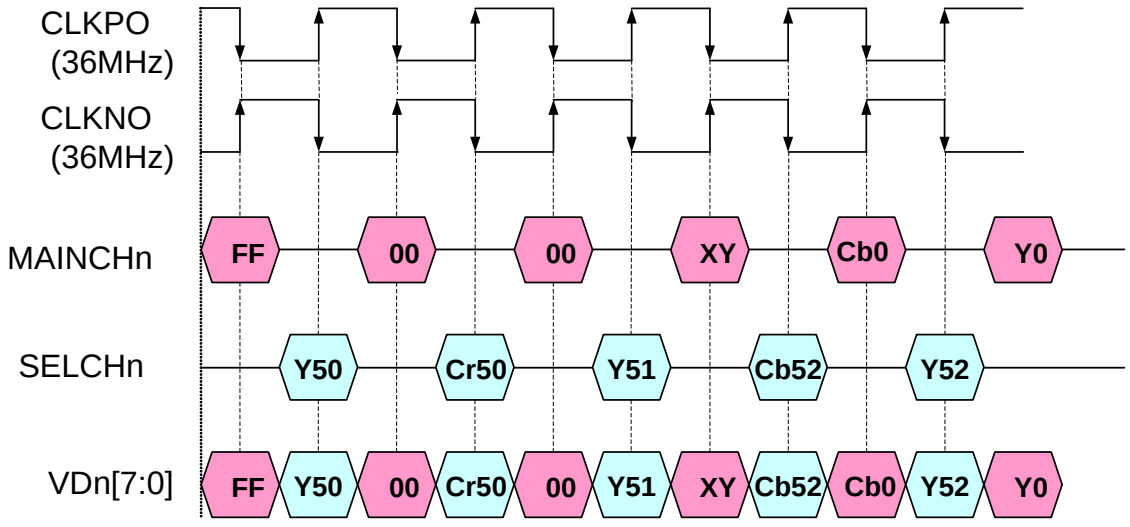


FIGURE 4. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 36MHZ CLOCK.

FOUR CHANNEL 960H TIME-DIVISION-MULTIPLEXED FORMAT WITH 144MHZ

Four channel of 960H (960x480 for NTSC,960x576 for PAL) at 36MHz video stream that are time-division-multiplexed at 144MHz data rate format is implemented in TW2960 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2960 implements single 8-bit bus at 4 times the base band pixel clock rate of 36MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 36MHz ITU-R BT.656 like specification. For interface that can accept the new 144MHz clock bus, only one single clock at 144MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

Figure 5 depicts the temporal arrangement of the video data in 144MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 144MHz clock

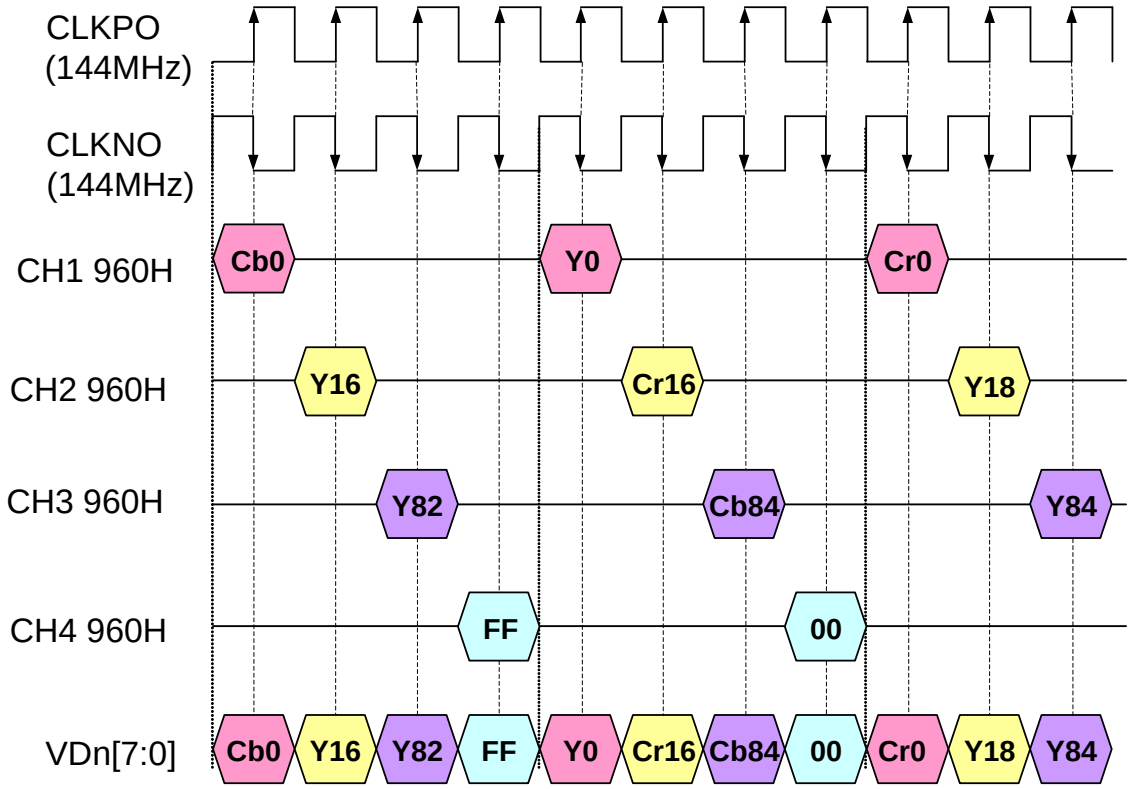


FIGURE 5. PIN OUTPUT TIMING OF 144MHZ 4 CH 960H TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 144MHZ CLOCK

TABLE 4. SHOWS THE SPECIAL FORMAT OF ITU-R BT. 656 LIKE EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

OUTPUT ENABLING ACT

After power-up, the TW2960 registers have the default values. After RSTB pin is asserted and released, all registers have the default values. After reset, the TW2960 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

VIDEO OUTPUT CHANNEL SELECTION

If CHMDn[1:0] in Reg0xCA is set to 0hex,MAINCHn[1:0] in Reg0xCD selects one number of Video Channels to be output on VDn[7:0] pin as Single Channel ITU-R BT.656 like 960H Format output. If CHMDn[1:0] in Reg0xCA is set to 1hex, MAINCHn[1:0] in Reg0xCD and SELCHn[1:0] in Reg0xCC select two numbers of Video Channels to be output on VDn[7:0] pin as Two Channel ITU-R BT.656 like 960H Time-multiplexed Format output. If CHMDn[1:0] in Reg0xCA is set to 2hex, Four Channel ITU-R BT.656 like 960H Time-multiplexed Format is output on VDn[7:0] pin.

EXTRA SYNC OUTPUT

The additional timing information such as syncs and field flag are also supported through the MPP pins. The video output timing is illustrated in Figure 6 and Figure 7. TW2960 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VSYNC/FIELD output function. Start of VS timing is controlled by VSHT register(V timing) and OVSDLY register(H timing).End of VS timing is controlled by OVSEND register(V Timing). Start of FLD timing is controlled by OFDLY register(V timing). Start of HS timing is controlled by HSBEGIN register and End of HS timing is controlled by HSEND register.

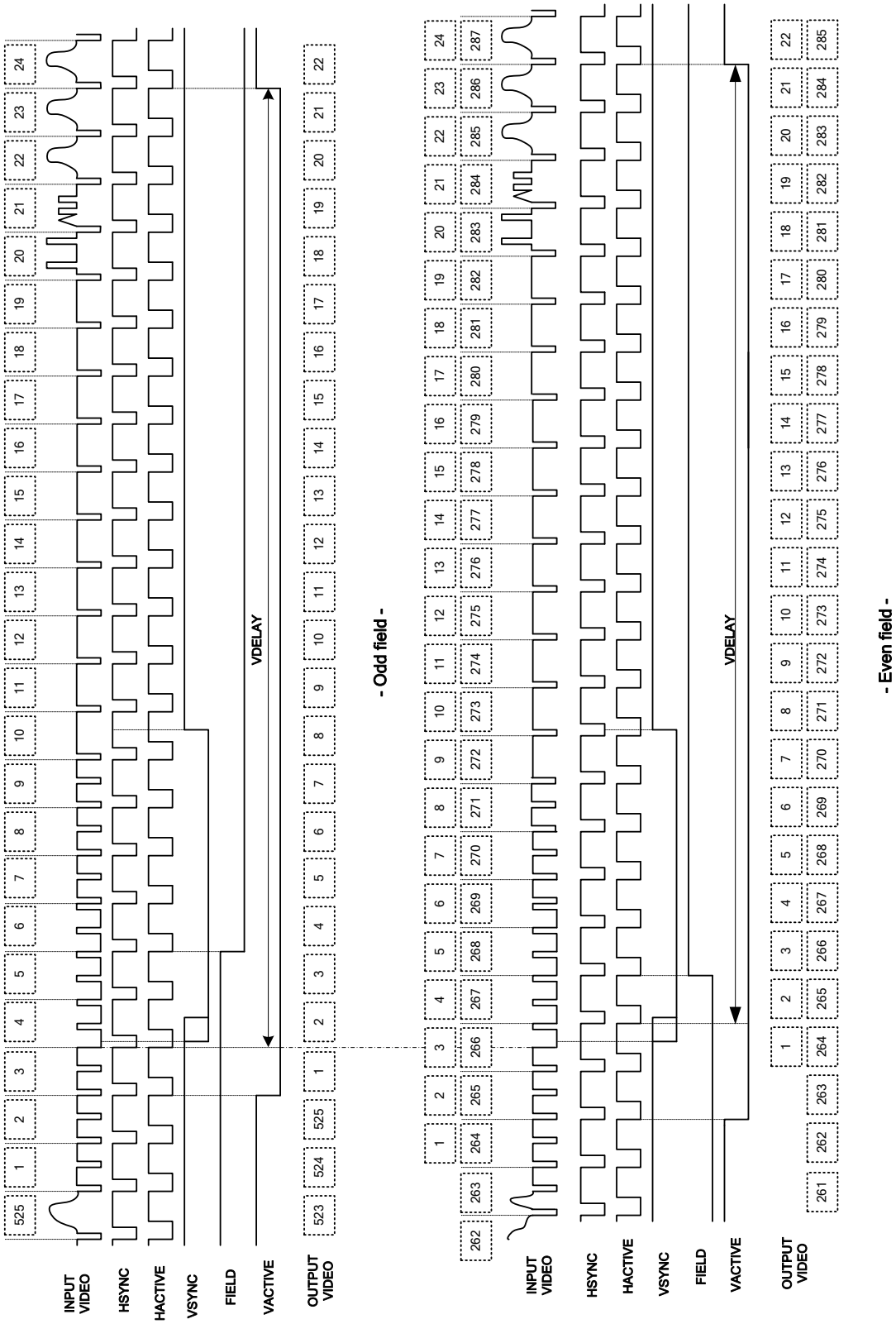


FIGURE 6. VERTICAL TIMING DIAGRAM FOR 60HZ/525 LINE SYSTEM

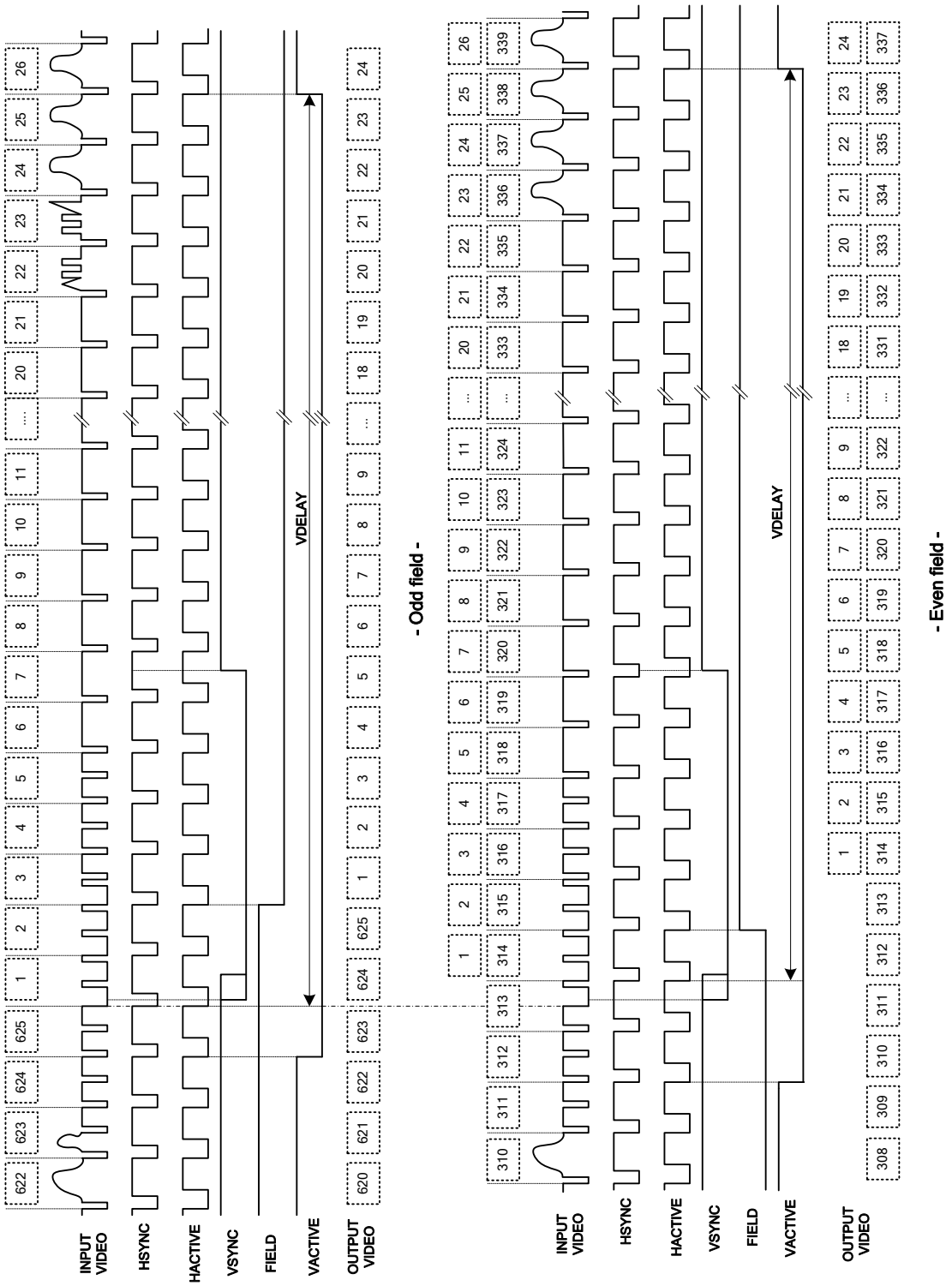


FIGURE 7. VERTICAL TIMING DIAGRAM FOR 50HZ/625 LINE SYSTEM

Audio Codec

The audio codec in the TW2960 is composed of five audio Analog-to-Digital converters processing, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as the Figure 8. The TW2960 can accept 5 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

The level of analog audio input signal AIN1 ~ AIN5 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1,AIGAIN2,AIGAIN3,AIGAIN4 and AIGAIN5 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pins are used for playback function. To record audio data, the TW2960 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pins.

The TW2960 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO5 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the AOGAIN register. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The main purpose of AIN5 is to make the standard I2S/DSP digital audio output on ADATM pin for special application. Usually, 4 AIN1/AIN2/AIN3/AIN4 audio data are only used on ADATR pin output.

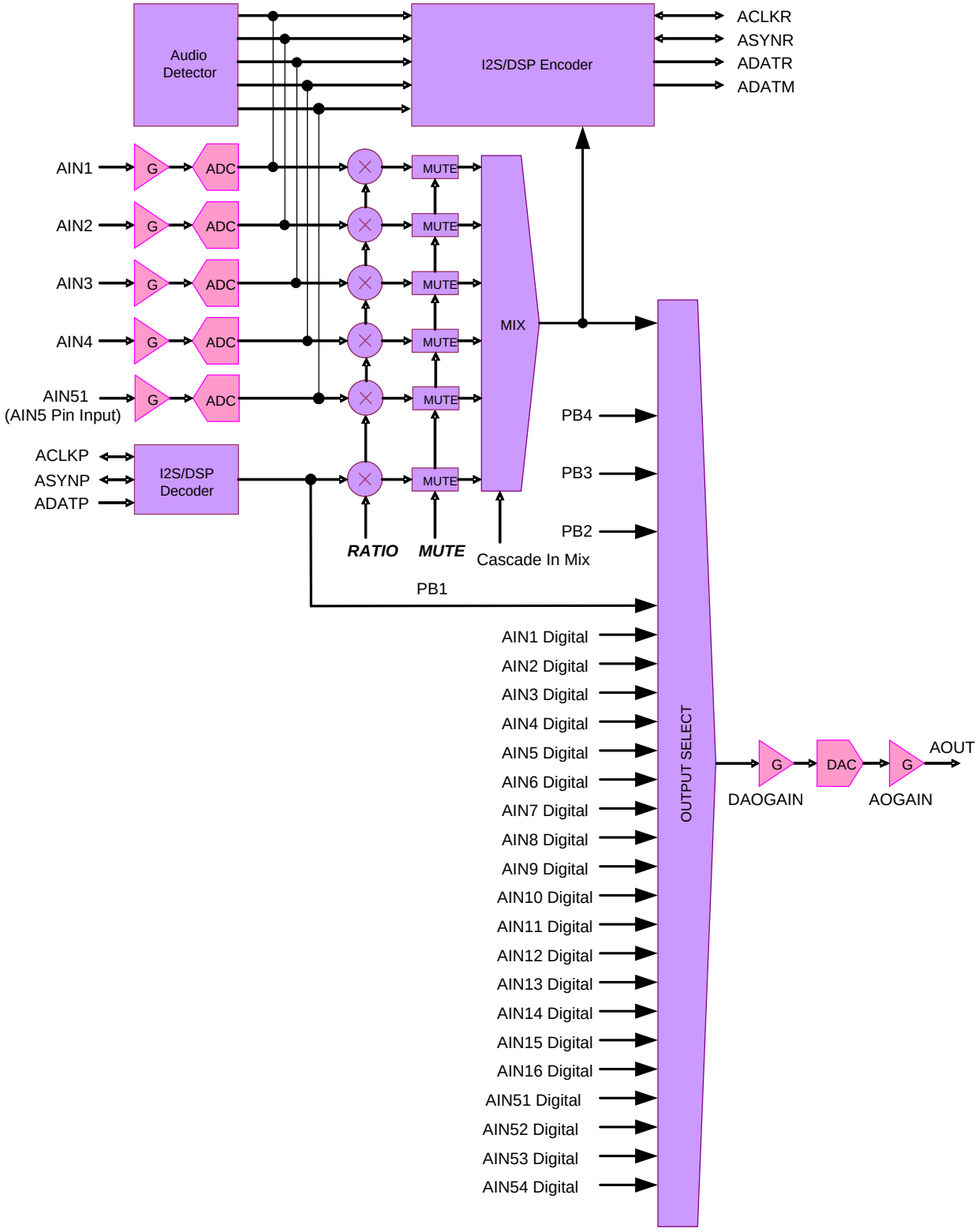


FIGURE 8. BLOCK DIAGRAM OF AUDIO CODEC

AUDIO CLOCK MASTER/SLAVE MODE

The TW2960 has two types of Audio Clock modes. If ACLKRMASTER register is set to 1, fs audio sample date is processed from audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0 (output enable mode). If ACLKRMASTER register is set to 0, fs audio sample rate is processed from audio clock on ACLKR pin input. 256xfs, 320xfs or 384xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode. AIN5MD and AFS384 register set up Audio fs mode by following table.

REGISTER		FS MODE
AIN5MD	AFS384	
0	0	256xfs
1	0	320xfs
0	1	384xfs

AUDIO DETECTION

The TW2960 has an audio detector for individual 5 channels. There are 2 kinds of audio detection method defined by the ADET_TH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1 ~ ADET_TH5 registers. The detection of differential amplitude is recommended for most use. The status for audio detection is read by the STATE_AVDET register and it also makes the interrupt request through the IRQ pin with the combination of the status for video loss detection.

MULTI-CHIP OPERATION

TW2960 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 4 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode.

Each stage chip can accept 5 analog audio signals so that four cascaded chips will be 16-channel audio controller as default {AFS384, AIN5MD} = 00. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2960 can generate 16 channel data simultaneously using multi-channel method. In addition, each stage chip can support 4 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channel mixing audio data by the digital serial audio data and analog audio signal. The first stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog converter in the first stage chip.

Several Master/Slave mode configurations are available. Figure 9 is the most recommended and demanded system with Clock Master mode (ACLKRMASTER = 1). Figure 10 is the most recommended system with Clock Slave Sync Slave mode (ACLKRMASTER=0, ASYNROEN=1) . Other system combinations are also available if application need different type specific system. Figure 9 and Figure 10 show the most typical system.

In the following FIGUREs, Mix1-16-51-54/Pb1 means Mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected Audio output in AIN1-16-51-54/Pb1.

If one of TW2960s uses {AFS384, AIN5MD} = 01 or {AFS384, AIN5MD} = 10, all other cascaded TW2960 chips must set up same {AFS384 AIN5MD} mode together.

In Multi-Chip Audio operation mode, one same Oscillator clock source 36MHz need to be connected to all TW2960 XTI pins.

If a special application needs 72MHz/144MHz XTI input, the RSTB pin input control needs to be considered. RSTB input controlled by MPP4 or MPP3 GPO output is one of the solutions. Another way needs XTI/RSTB timing control, as shown in Figure 9. RSTB/XTI timing control is not required in 36MHz XTI mode.

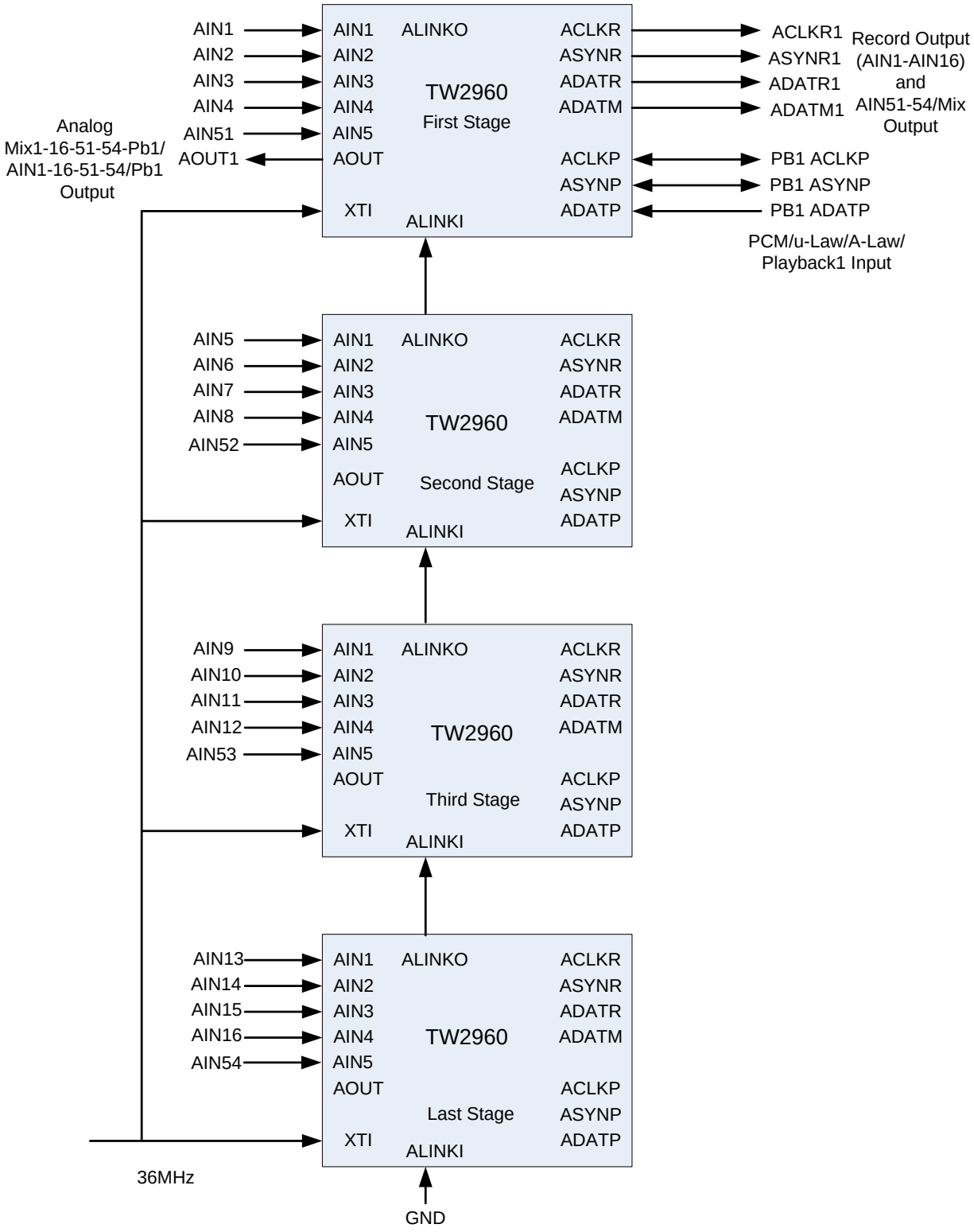


FIGURE 9. RECOMMENDED CLOCK MASTER CASCADE MODE SYSTEM

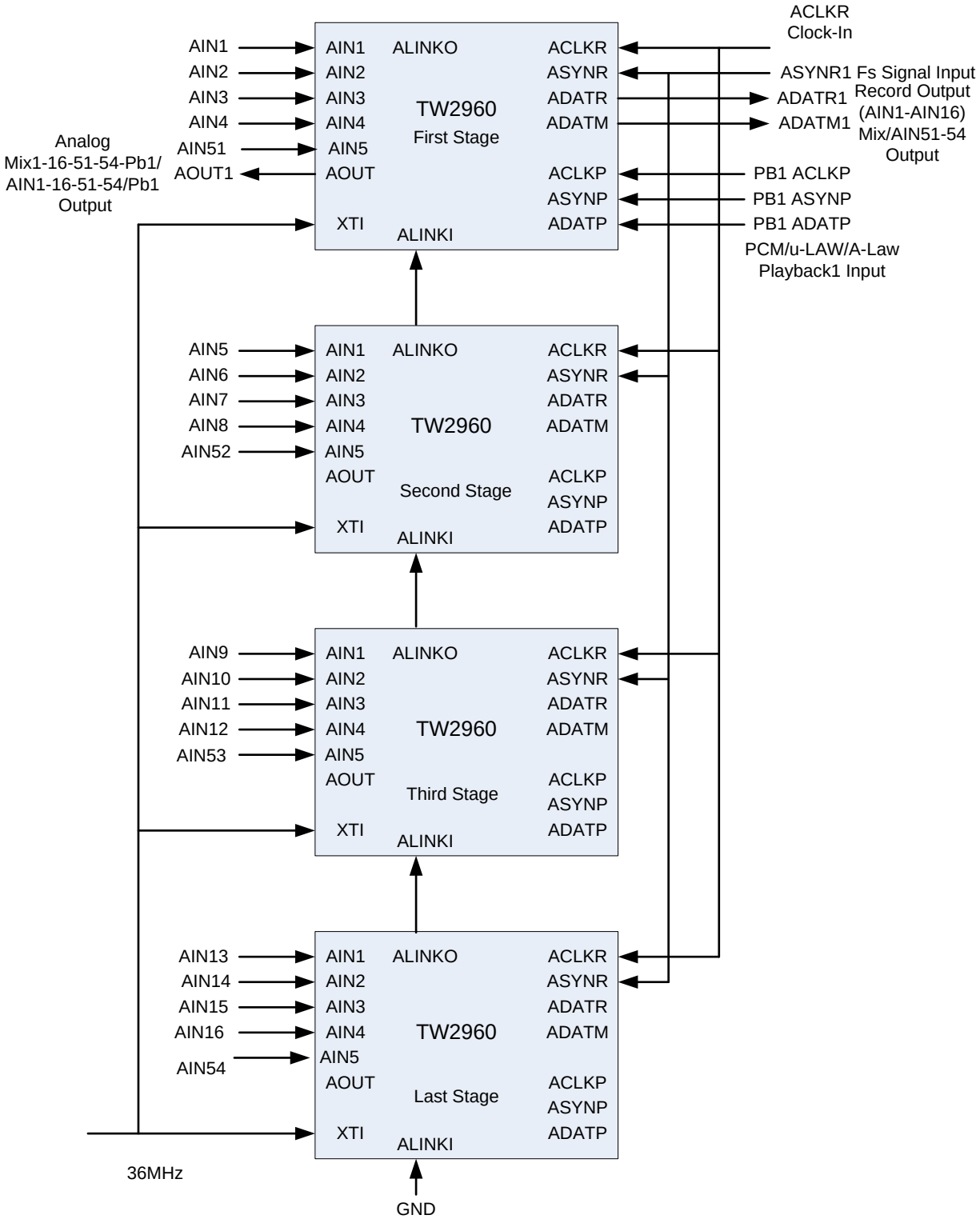


FIGURE 10. RECOMMENDED CLOCK SLAVE SYNC SLAVE CASCADE MODE SYSTEM

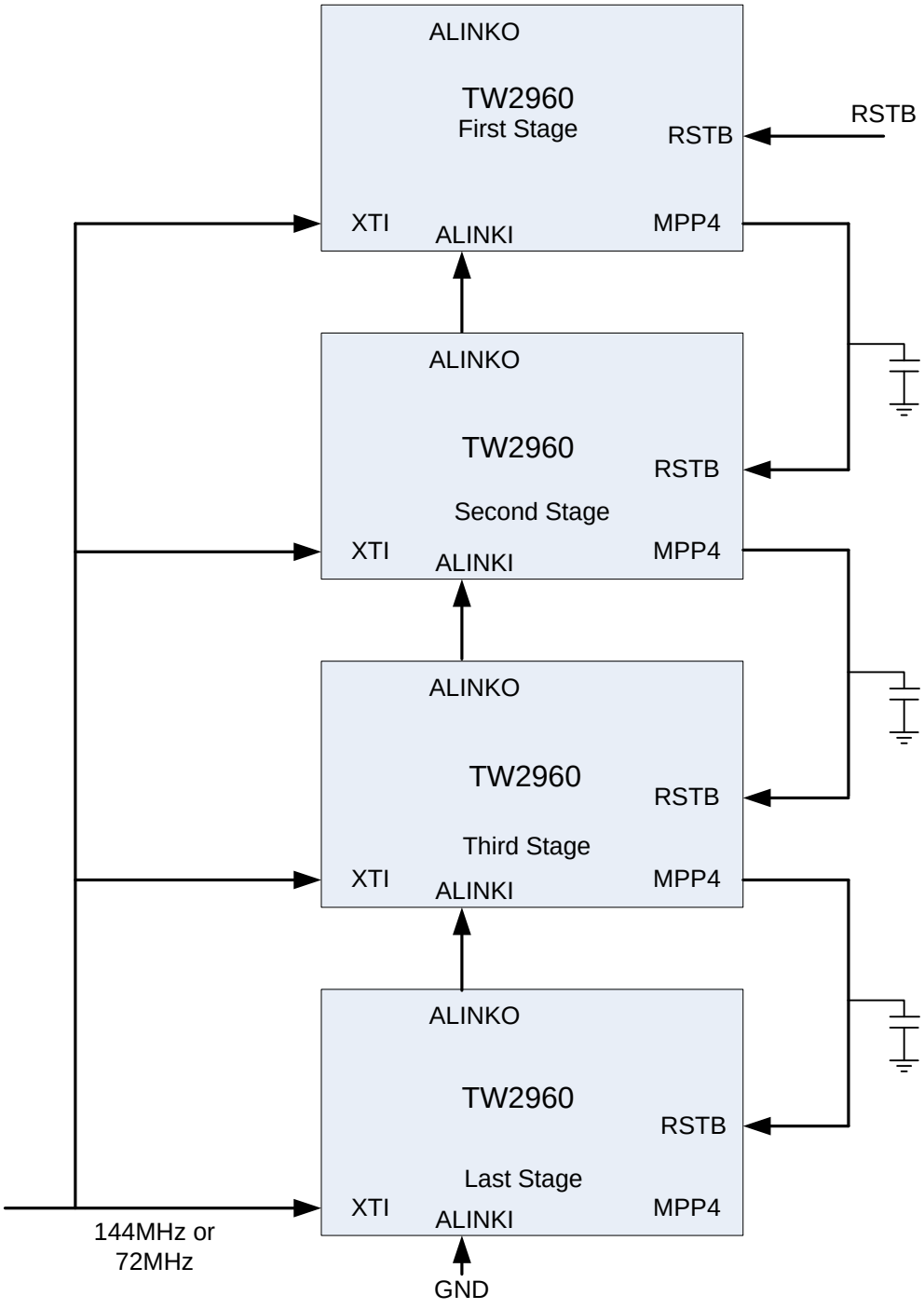


FIGURE 11. RSTB CONTROL BY MPP4GPO OUTPUT FOR 144MHZ/72MHZ XTI INPUT

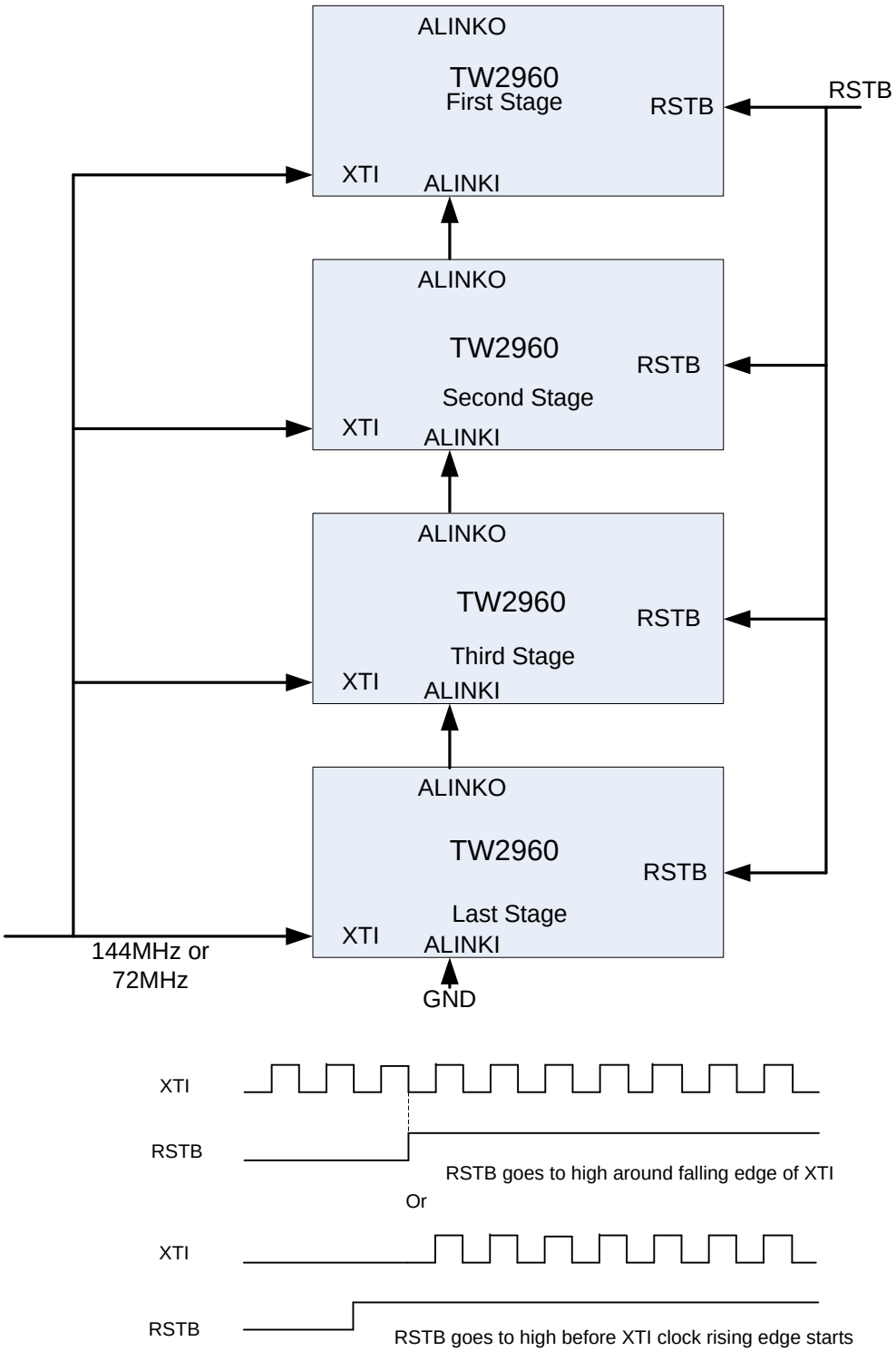
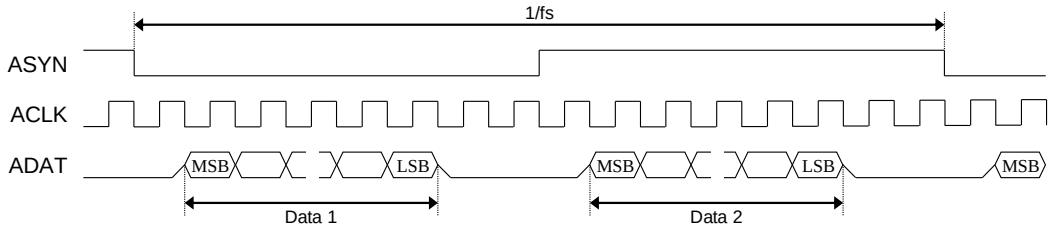


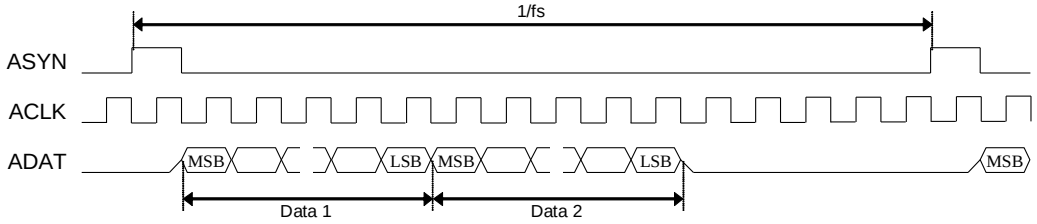
FIGURE 12. RSTB CONTROL FOR 144MHZ/72MHZ XTI INPUT

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW2960; the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in Figure 13.



(a) I2S Format



(b) DSP Format

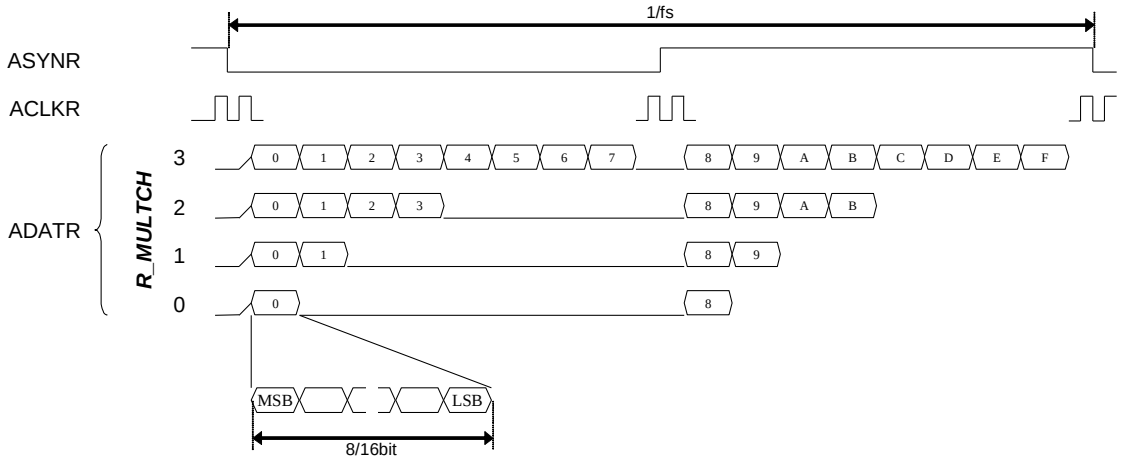
FIGURE 13. FIG13 TIMING CHART OF SERIAL AUDIO INTERFACE

Playback Input

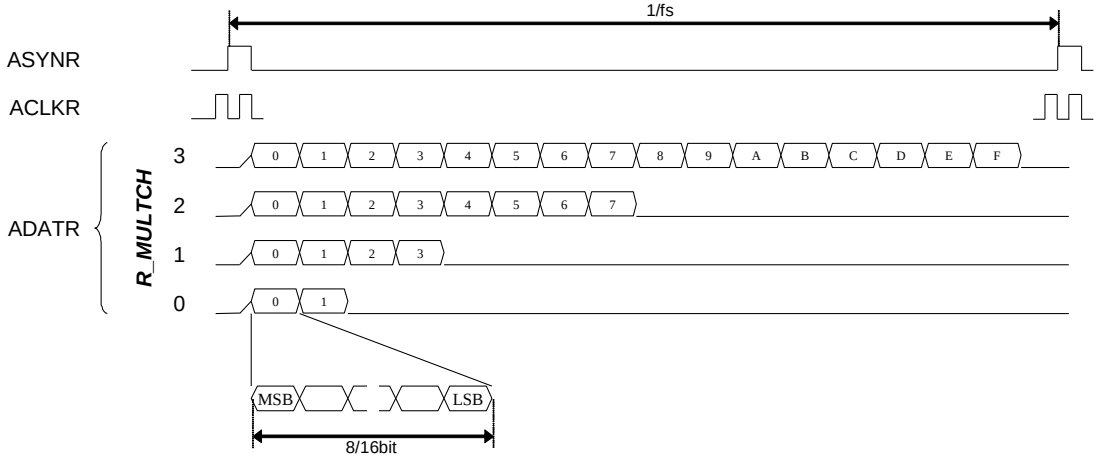
The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW2960 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs, 320xfs or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2960 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. Figure 14 shows the digital serial audio data organization for multi-channel audio.



(a) I2S Format



(b) DSP Format

FIGURE 14. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

Table 5 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is also shown in Table 5.

TABLE 5. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD

(a) I2S Format

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data, which are mixing audio, and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO CLOCK SLAVE MODE DATA OUTPUT TIMING

TW2960 always output ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing. ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM output are always fixed to one ACLKR falling edge timing. However, if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, TW2960 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following FIGUREs. ASYNR signal is changing during ACLKR = 0. TW2960 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

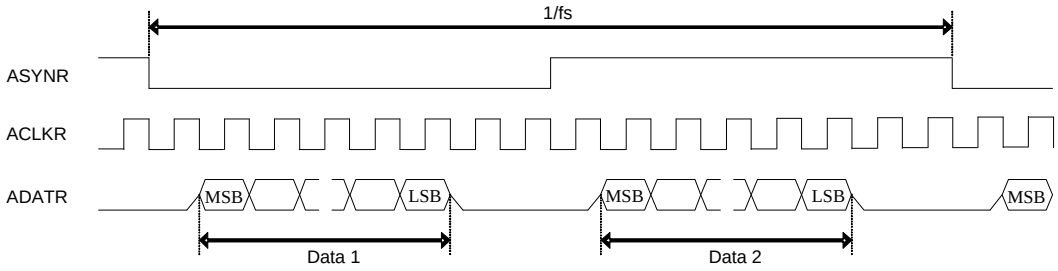


FIGURE 15. ACLKMASTER=0, RM_SYNC=0

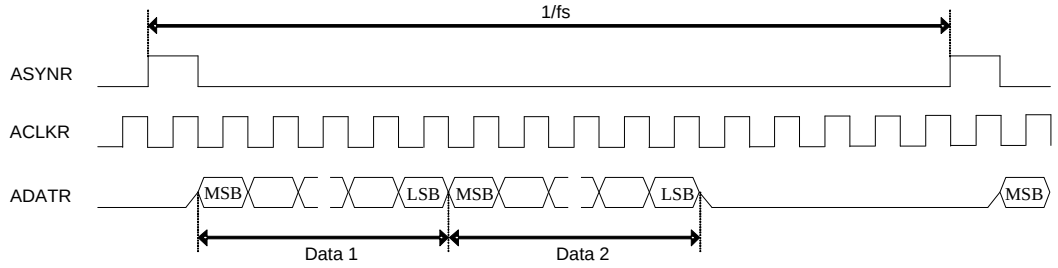


FIGURE 16. ACLKMASTER=0, RM_SYNC=1

ASYNR is ACLKR rising edge triggered input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2960 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following FIGUREs. ASYNR signal is changing during ACLKR = 1. TW2960 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

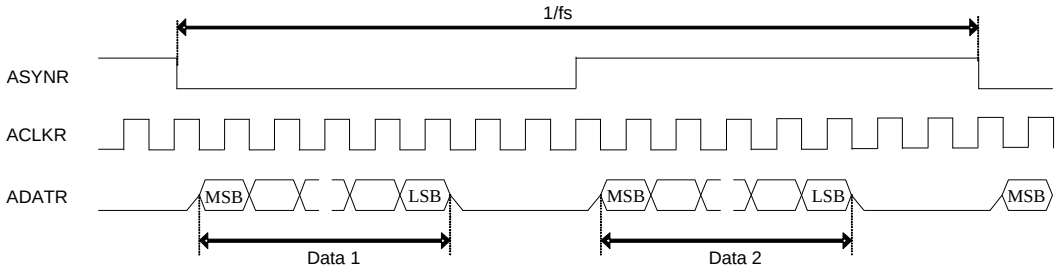


FIGURE 17. ACLKMASTER=0, RM_SYNC=0, ASYNROEN=1

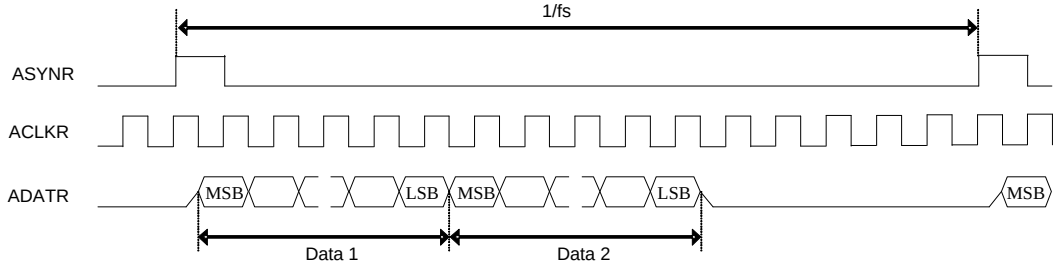


FIGURE 18. ACLKMASTER=0, RM_SYNC=1, ASYNROEN=1

ACLKP/ASYNP SLAVE MODE DATA INPUT TIMING

The following 8 data input timings are supported. ADATPDLY register needs to be set up according to the difference of ADATP data input timings. Data1 is only used as default. The MSB bit is the first input bit as default PBINSWAP = 0.If PBINSWAP = 1, LSB bit is the first input bit.

ASYNP is ACLKP falling edge triggered input.

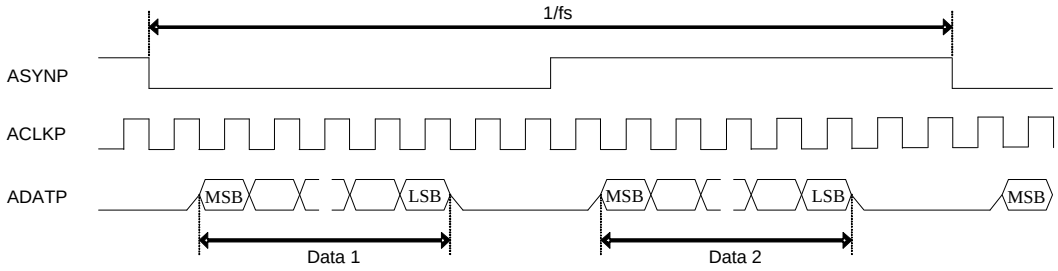


FIGURE 19. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

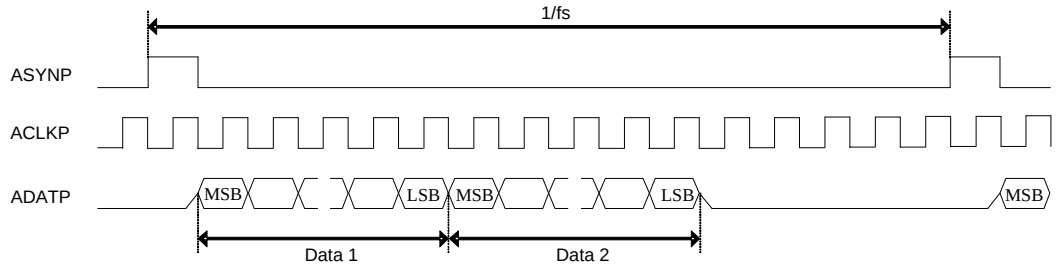


FIGURE 20. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

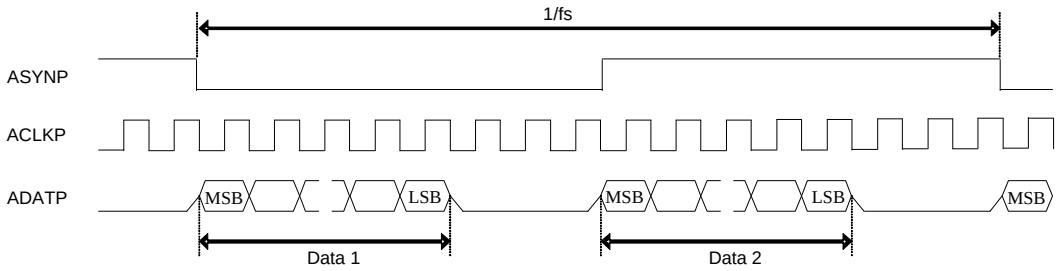


FIGURE 21. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

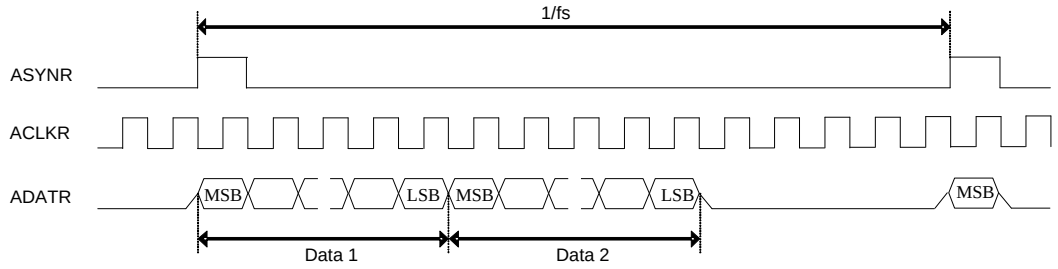


FIGURE 22. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

ASYNP is ACLKP rising edge triggered input.

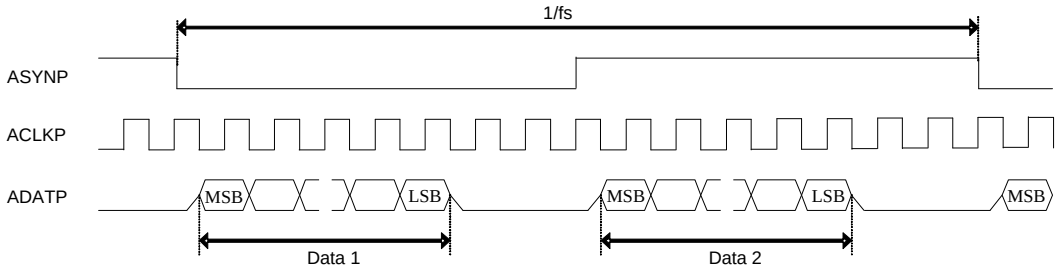


FIGURE 23. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

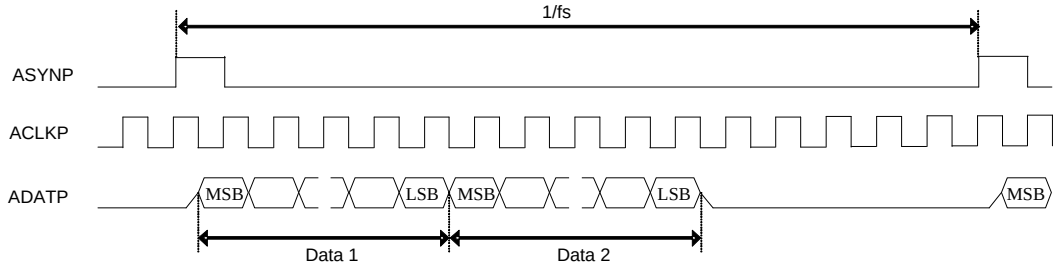


FIGURE 24. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

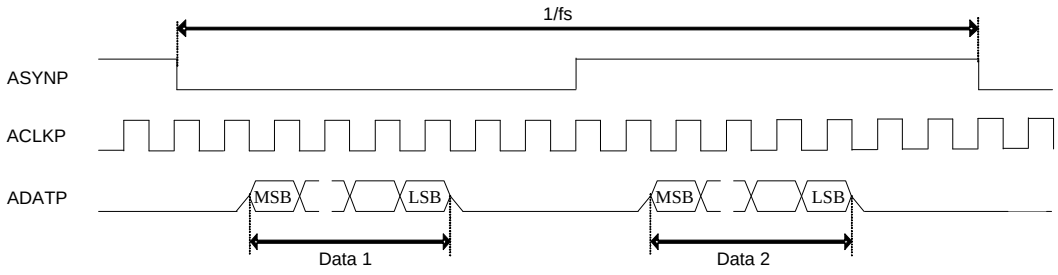


FIGURE 25. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

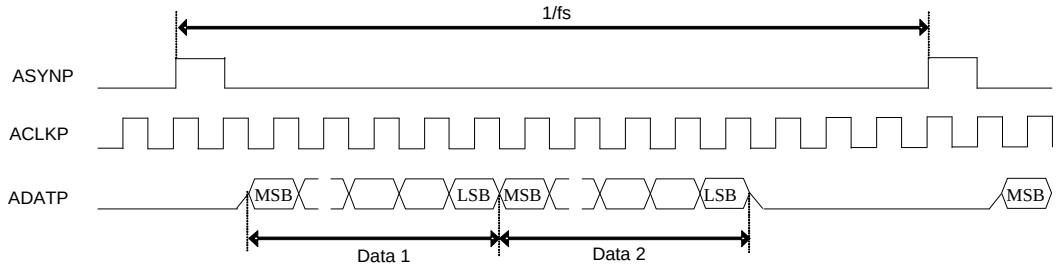


FIGURE 26. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

AUDIO CLOCK GENERATION

TW2960 has built-in audio clock generator. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKI register based following two equations.

ACKI = round (F AMCLK / F 36MHz * 2^23), it gives the Audio master Clock Nominal increment.

ACKI registers make audio_source _clock by 36MHz clock.
If MASCKMD=0, AMCLK=audio_source_clock.If MASCKMD=1, AMCLK=audio_source_clock/2.
AMCLK is used as audio system clock and audio ADC clock in Master clock mode.

The following table provides setting example of some common used audio frequency assuming XTI clock frequency of 36MHz.If ACLKRMASTER register bit is set to 1, following AMCLK is used as audio system clock with MASCKMD inside TW2960.

ACPL=1(Loop open) should be used in TW2960 system.

256xfs mode: AFS384 = 0, AIN5MD = 0,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 X 16 KHZ		
4.096	1908874	1D-20-8A
256 x 8 KHz		
2.048	954437	E-90-45

320xfs mode: AFS384 = 0, AIN5MD = 1,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 16 KHz		
5.12	2386093	24-68-AD
320 x 8 KHz		
2.56	1193046	12-34-56

384xfs mode: AFS384 = 1, AIN5MD=0,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 16 KHz		
6.144	2863312	2B-B0-D0
384 x 8 KHz		
3.072	1431656	15-D8-68

256xfs mode: AFS384=0,AIN5MD=0,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 x 48 KHz		
12.288	2863312	2B-B0-D0
256 x 44.1KHz		
11.2896	2630667	28-24-0B
256 x 32 KHz		
8.192	1908874	1D-20-8A
256 x 16 KHz		
4.096	954437	E-90-45
256 x 8 KHz		
2.048	477219	7-48-23

320xfs mode: AFS384=0,AIN5MD=1,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 32 KHz		
10.24	2386093	24-68-AD
320 x 16 KHz		
5.12	1193046	12-34-56
320 x 8 KHz		
2.56	596523	9-1A-2B

384xfs mode: AFS384=1,AIN5MD=0,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 32 KHz		
12.288	2863312	2B-B0-D0
384 x 16 KHz		
6.144	1431656	15-D8-68
384 x 8 KHz		
3.072	715828	A-EC-34

AUDIO CLOCK AUTO SETUP

If ACLKRMASTER = 1 audio clock master mode is selected, and AFAUTO register is set to “1”,TW2960 set up ACKI register by AFMD register value automatically.ACKI control input in ACKG module block is automatically set up to the required value by the condition of AFS384 and AFS384 register value.

AFAUTO	AFMD	ACKG MODULE ACKI CONTROL INPUT VALUE
1	0	8kHz mode value by each AFS384/AIN5MD case.
1	1	16kHz mode value by each AFS384/AIN5MD case.
1	2	32kHz mode value by each AFS384/AIN5MD case.
1	3	44.1kHz mode value by eachAFS384/AIN5MD case.
1	4	48kHz mode value by each AFS384/AIN5MD case.
0	X	ACKI register set up ACKI control input value.

Two-wire Serial Bus Interface

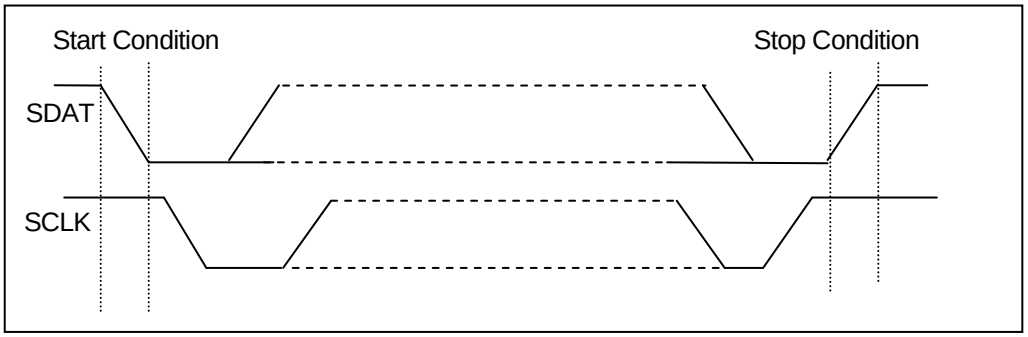


FIGURE 27. DEFINITION OF THE SERIAL BUS INTERFACE BUS START AND STOP

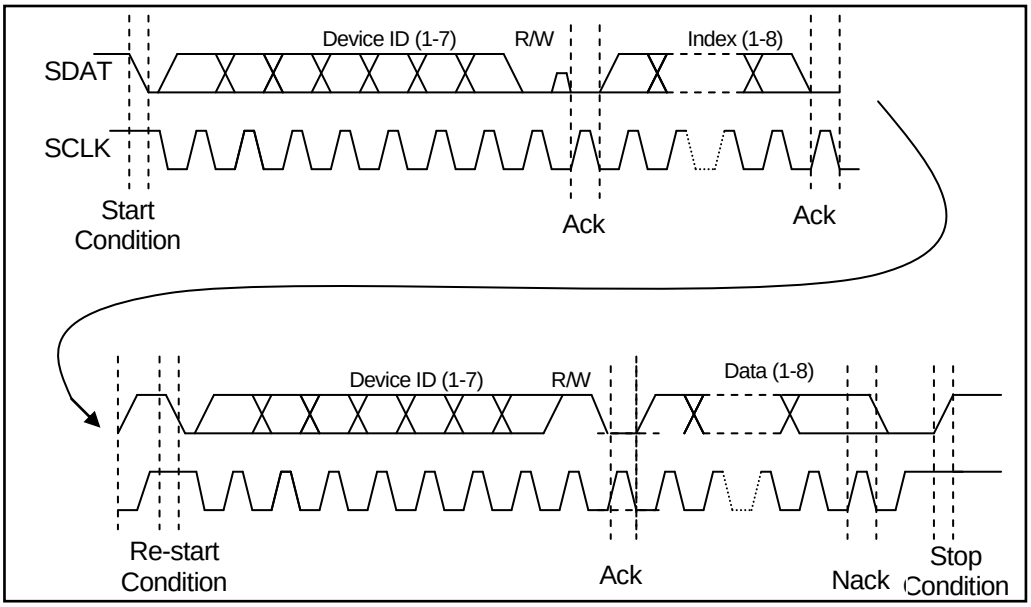


FIGURE 28. ONE COMPLETE REGISTER READ SEQUENCE VIA THE SERIAL BUS INTERFACE

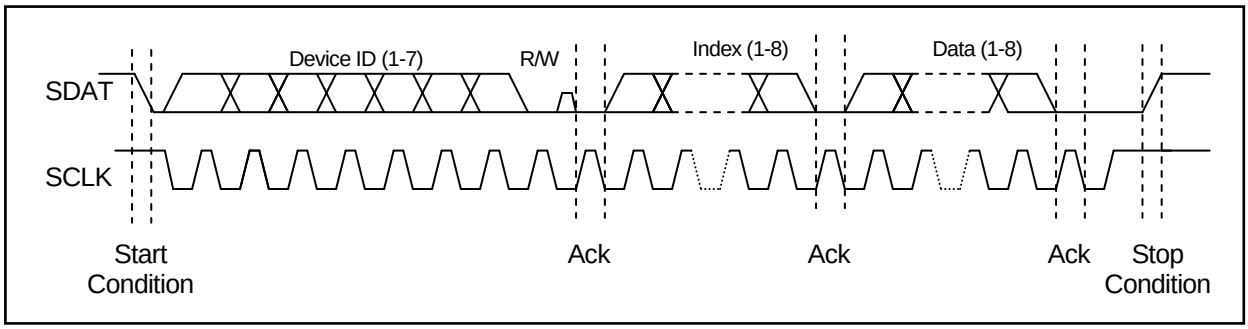


FIGURE 29. ONE COMPLETE REGISTER WRITE SEQUENCE VIA THE SERIAL BUS INTERFACE

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW2960 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDDO. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW2960 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD[1:0] (Serial Interface Address) pins to either VDDOO or VSS (See below Table) through a pull-up or pull-down resister. The SIAD[1:0] pins are multi-purpose pins and must not tied to supply voltage or ground directly. If the SIAD[1:0] pins are tied to VDDO, then the least significant 2-bit of the 7-bit address is a “11”. If the SIAD[1:0] pins are tied to VSS then the least significant 2-bit of the 7-bit address is a “00”. The most significant 5-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDAT from high to low, while SCLK is high, this is defined to be a start condition (See FIGURE 27.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in FIGURE 28. (For the TW2960, the next byte is normally the index to the TW2960 registers and is a write to the TW2960 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of the TW2960, the master sends another 8-bits of data, the TW2960 loads this to the register pointed by the internal index register. The TW2960 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW2960 if they are in ascending sequential

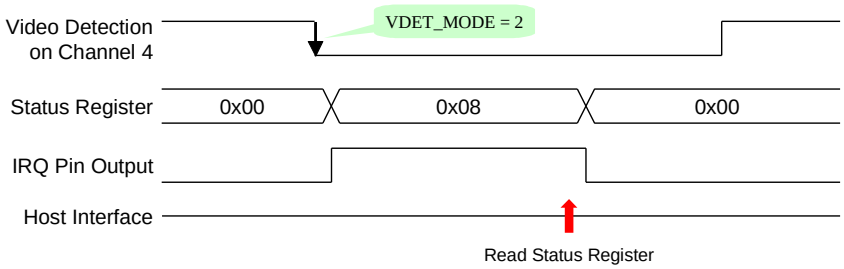
order. After each 8-bit transfer,the TW2960 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW2960 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
0	1	0	1	0	SIAD[1]	SIAD[0]	1=Read 0=Write

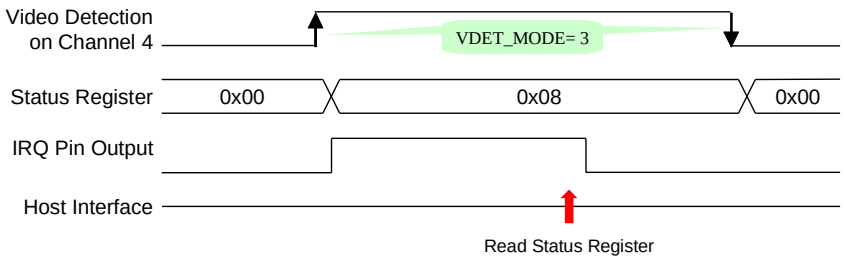
A TW2960 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See FIGURE 28). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Interrupt Interface

The TW2960 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2960. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. In addition, each channel of video and audio detection should be enabled by the AVDET_ENA. Then, the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET_STATE. Figure 30 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading the AVDET_STATE. When the VDET_MODE and/or ADET_MODE are 1 or 2, the status register AVDET_STATE will also be cleared automatically by reading AVDET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status register AVDET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video and Audio Detection Flag Mode

FIGURE 30. TIMING DIAGRAM OF INTERRUPT INTERFACE

Clock PLL

The TW2960 has built-in 2x/4x clock PLL to generate 2xXTI clock or 4xXTI clock. If 36MHz is connected to XTI pin, SEL_X24 register need to be 1(4x).XTIMD register selects which clock source is used in the system. If clock PLL is not used, XTIMD register selects XTI input clock frequency mode.

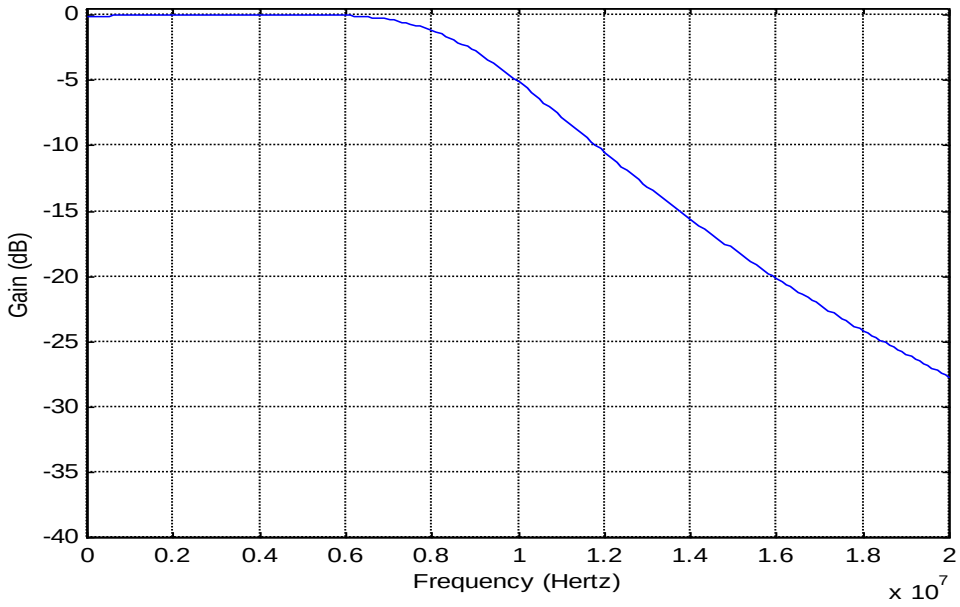
XTI Clock Input

If XTI input needs special 72MHz/144MHz frequency, {MPP2,MPP1} pin pull-down setting during RSTB = 0 period support up to 400kbps two wire serial bus speed at all 36MHz/72MHz/144MHz XTI input mode.

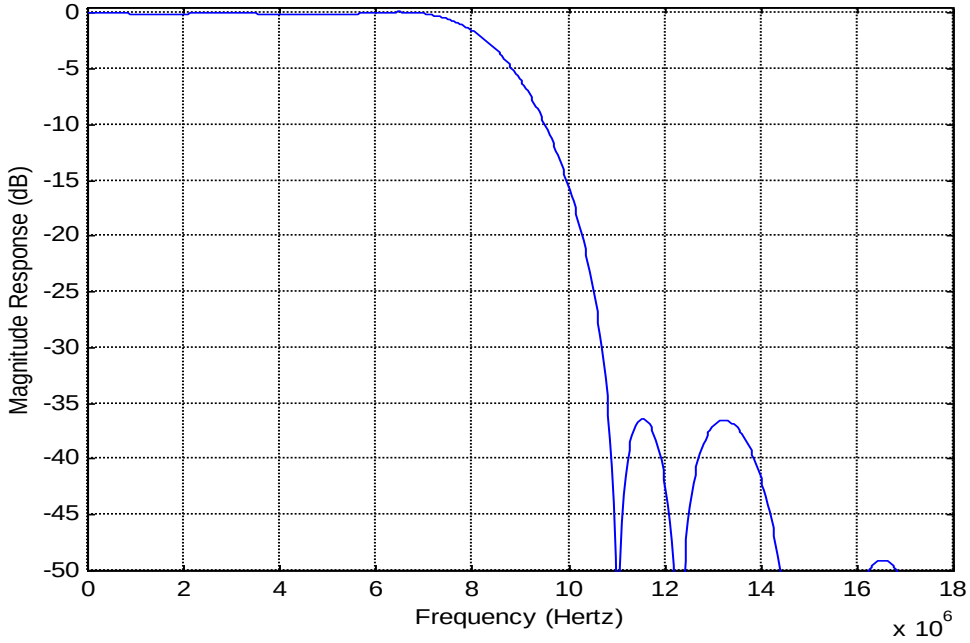
MPP2	MPP1	SYSTEM CLOCK OF TWO WIRE SERIAL BUS INTERFACE	REQUIRED XTI INPUT FREQUENCY
NC	NC	XTI	36MHz
NC	Pull-down	XTI/2	72MHz
Pull-down	NC	XTI/4	144MHz

Video Decoder Filter Curves

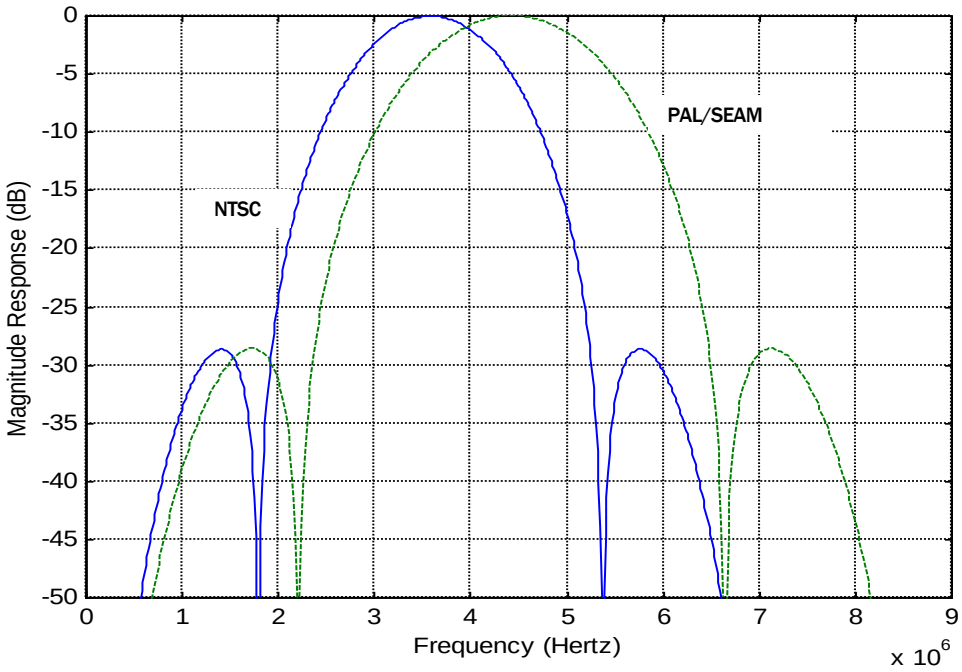
ANTI-ALIAS FILTER



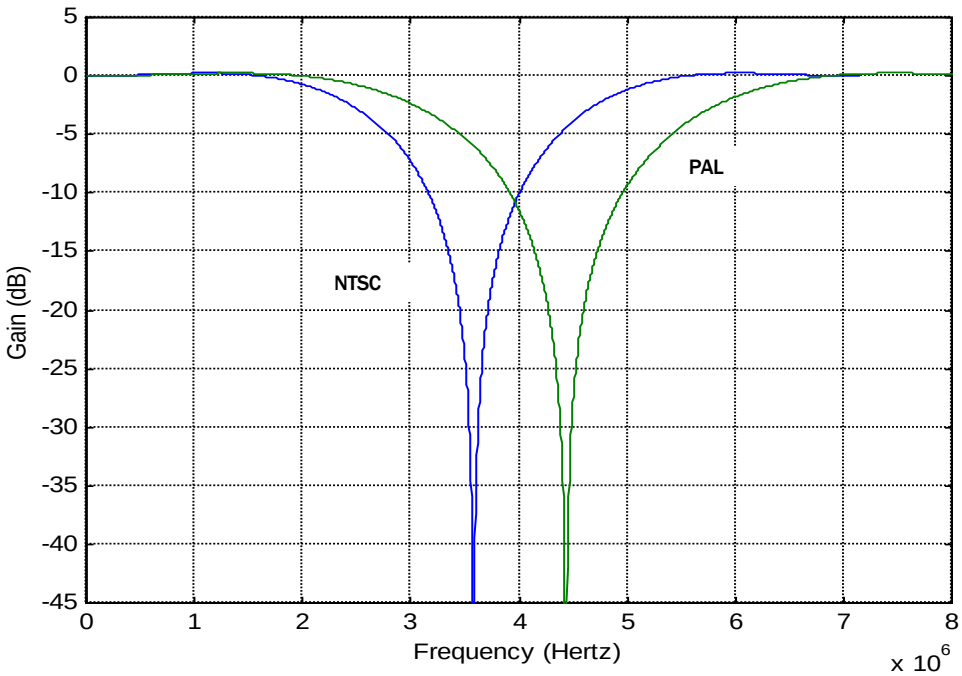
DECIMATION FILTER



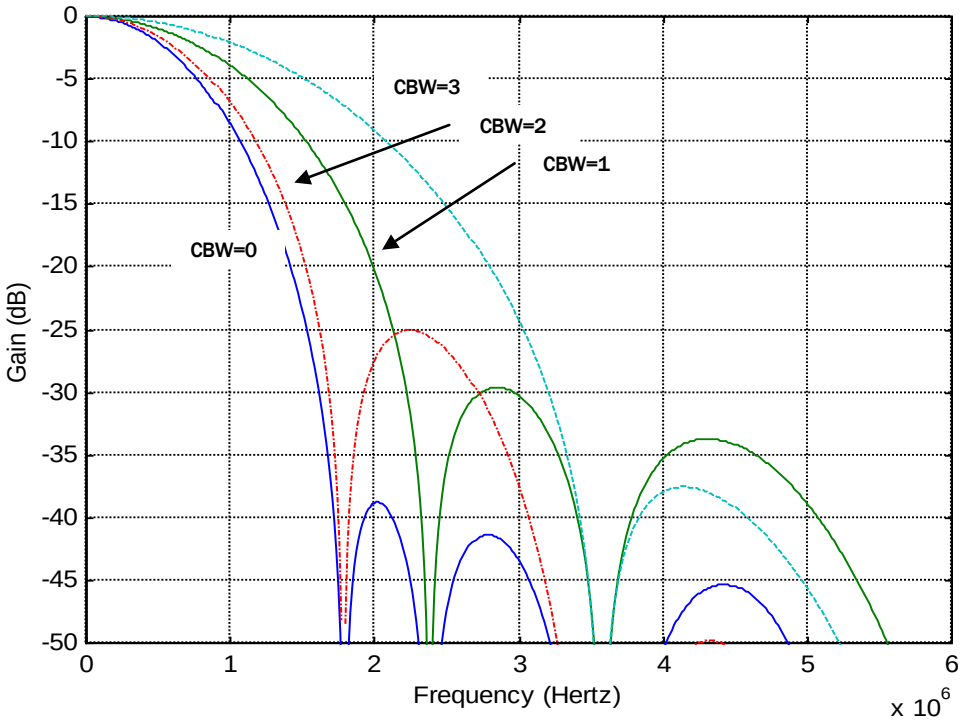
CHROMA BAND PASS FILTER CURVES



LUMA NOTCH FILTER CURVE FOR NTSC AND PAL

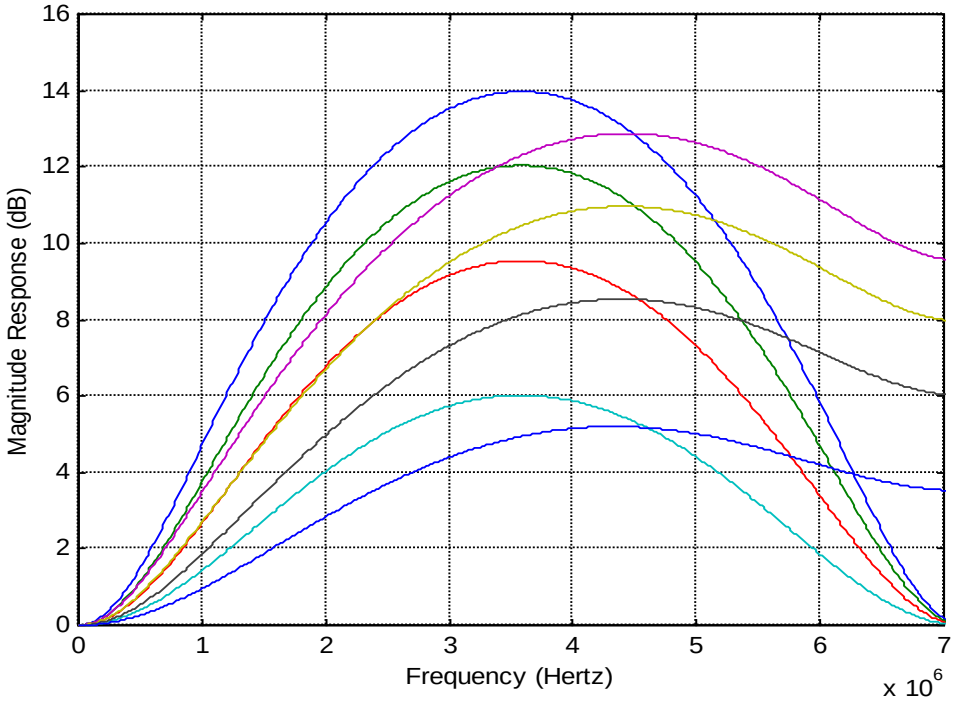


CHROMINANCE LOW-PASS FILTER CURVE

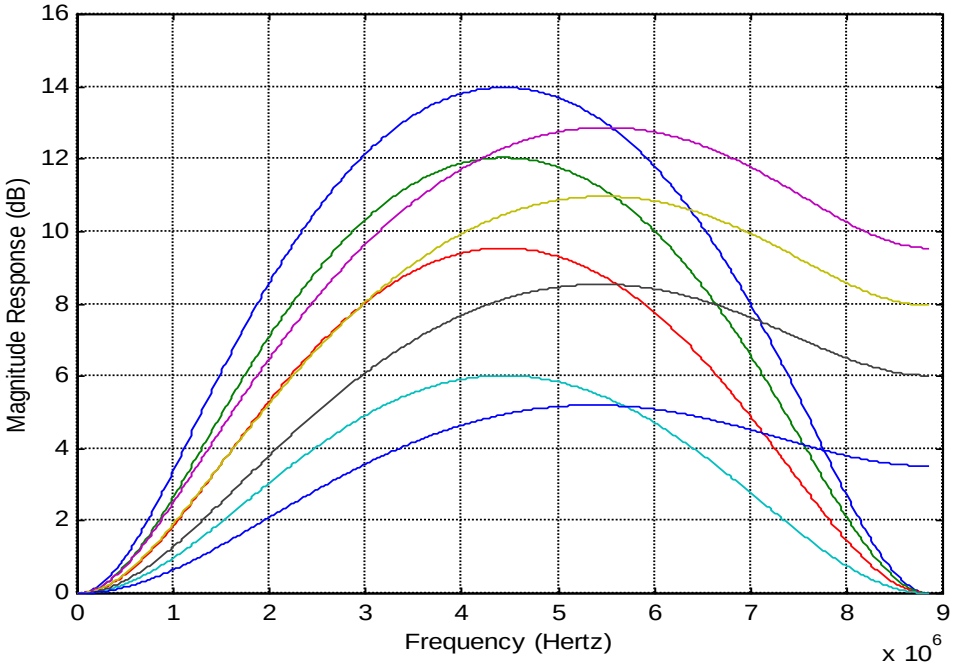


PEAKING FILTER CURVES

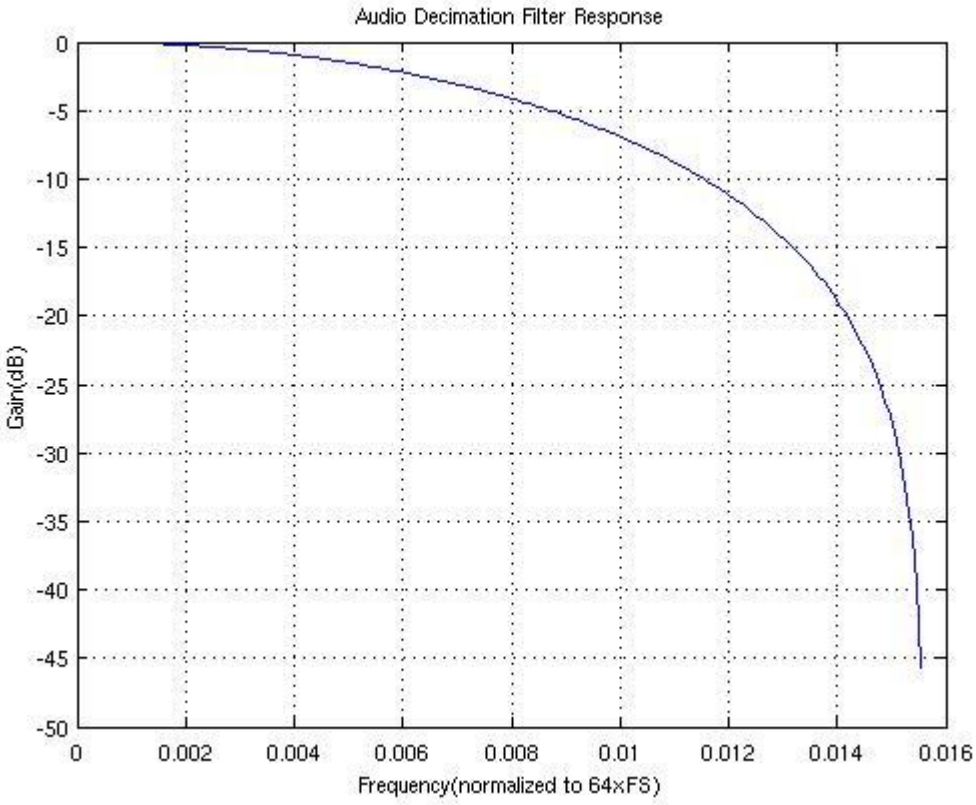
NTSC



PAL



Audio Decimation Filter Response



(*) 0.016 line = 0.016x64xFs

Control Register

REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xA0	0xA1	0xA2	0xA3	NT50	NT50	CVSTD*			CVFMT			
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF*							

Note: * Read only registers

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x53				ANADACTEST	0	TAADCO			ADAC_CNTL			
0x54				ASAVE	0	0	DOUT_RST	DIV_RST	ACALEN	1	1	1
0x55				VADCCTL	IBINBUF_SEL		IB_ADC		ICLAMP_SEL		VCMIN_SEL	
0x56				AADCCTL	AFE_CNTL							
0x5C				BGCTL	TVADCO		BGCTL	VSWEN	VSWNUM			
0x5D				CH2MISC2	NKILL_2	PKILL_2	SKILL_2	CBAL_2	FCS_2	LCS_2	CCS_2	BST_2
0x5E				CH3MISC2	NKILL_3	PKILL_3	SKILL_3	CBAL_3	FCS_3	LCS_3	CCS_3	BST_3
0x5F				CH4MISC2	NKILL_4	PKILL_4	SKILL_4	CBAL_4	FCS_4	LCS_4	ICCS_4	BST_4
0x60				PLL1	PLLCKOUIT	PLL_PD	PLLIREF	SEL_X24	LP_X4		CP_X4	
0x61				PLL2	0	0	0	DECOSC	CKOUTSEL		XTIMD	
0x62				MPPOE	Reserved				MPP4OE	MPP3OE	MPP2OE	MPP1OE
0x63				CH21NUM	CH2NUM				CH1NUM			
0x64				CH43NUM	CH4NUM				CH3NUM			
0x65				VDOEB			VD_36C	VD4ORD	VD4OEB	VD3OEB	VD2OEB	VD1OEB
0x70				ACLKPOL	0	S2I_8BIT	ACLKRPOL	ACLKPPOL	AFAUTO	AFMD		
0x71				AINCTL	I2S8MODE	MASCKMD	PBINSWAP	ASYNRDLY	ASYNPDLY	ADATPDLY	INLAWMD	
0x72				MRATIOMD	MRATIOMD	ADACTEST	AOFFCORE	DAORATIO	DAOGAIN			
0x73				A5NUM	Reserved					AIN5FORM	AINTPOFF	A5DET_ENA
0x74				A5DETST	0	0	0	0	0	0	0	A5DET_STATE*
0x75				AADC5OFS_H	0	0	0	0	0	0	AADC5OFS[9:8]	
0x76				AADC5OFS_L	AADC0FS[7:0]							
0x77				AUD5ADC_H	0	0	0	0	0	0	AUD5ADC[9:8]	
0x78				AUD5ADC_L	AUD5ADC[7:0]							
0x79				ADJAADC5_H	0	0	0	0	0	0	ADJAADC5[9:8]	
0x7A				ADJAADC5_L	ADJAADC5[7:0]							

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x7B				I2SO_RSEL	0	0	0	I2SO_RSEL				
0x7C				I2SO_LSEL	0	0	0	I2SO_LSEL				
0x7D				RECSEL5	RECSEL54		RECSEL53		RECSEL52		RECSEL51	
0x7E				ADATMI2S	A5OUTOFF	ADATMI2SOEN	MUTEA5	ADET_TH5[4:0]				
0x7F				AIGAIN5	AIGAIN5				MIX_RATIO5			
0x80				SRST	0	0	AUDIORST	VOUTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x81				ACNTL	0	I0	0	0	CLKPDN	0	YFLEN	0
0x82				ACNTL2	CTEST	YCLEN	CKIPOL	0	GTEST	VLPF	CKLY	CKLC
0x83				CNTRL1	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY
0x84				CKHY	GMEN	CKHY		HSDLY				
0x85				SHCOR	SHCOR				VIN4	VIN3	VIN2	VIN1
0x86				CORING	CTCOR		CCOR		VCOR		CIF	
0x87				CLMPG	CLPEND				CLPST			
0x88				IAGC	NMGAIN				WPGAIN			0
0x89				AIN5MD	ATHROUGH	ASYNSERIAL	ACLKR128	ACLKR64	AFS384	AIN5MD	0	0
0x8A				PEAKWT	PEAKWT							
0x8B				CLMPL	CLMPLD	CLMPL						
0x8C				SYNCT	SYNCTD	SYNCT						
0x8D				MISSCNT	MISSCNT				HSWIN			
0x8E				PCLAMP	PCLAMP							
0x8F				VCNTL1	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT
0x90				VCNTL2	BSHT			VSHT				
0x91				CKILL	CKILMAX		CKILMIN					
0x92				COMB	COMBMD	HTL			VTL			
0x93				LDLY	CKLM	YDLY			0	0	AAFLPF	
0x94				MISC1	HPLC	ENCNT	PALC	SDET	0	BYPASS	SYOUT	0
0x95				LOOP	HPM		ACCT		SPM		CBW	
0x96				MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST
0x97				CLMD	FRM		YNR		CLMD		PSP	
0x98				HSLOWCTL	HSBEGIN[3:0]				HSEND[3:0]			
0x99				HSBEGIN	HSBEGIN[11:4]							
0x9A				HSEND	HSEND[11:4]							

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x9B				OVSDLY	OVSDLY							
0x9C				OVSEND	HASYNC	OFDLY			VSMODE	OVSEND		
0x9D				HBLEN	HBLEN							
0x9E				NOVID	VDELAYMD	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656
0x9F				CLK1MD	CLKNO_DEL				CLKPO_DEL			
0xA8				HFLT21	HFLT2				HFLT1			
0xA9				HFLT43	HFLT4				HFLT3			
0xAA				AGCEN	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB				AGCGAIN1	AGCGAIN1[7:0]							
0xAC				AGCGAIN2	AGCGAIN2[7:0]							
0xAD				AGCGAIN3	AGCGAIN3[7:0]							
0xAE				AGCGAIN4	AGCGAIN4[7:0]							
0xAF				VSHP21	0	VSHP2			0	VSHP1		
0xB0				VSHP43	0	VSHP4			0	VSHP3		
0xB1				NOVIDMODE	CH8IDEN	0	0	0	0	0	0	0
0xB2				VDLOSSOE	0	0	0	0	VDLOSSOE4	VDLOSSOE3	VDLOSSOE2	VDLOSSOE1
0xB3				AADC0FS_H	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0xB4				AADC1OFS_L	AADC1OFS[7:0]							
0xB5				AADC2OFS_L	AADC2OFS[7:0]							
0xB6				AADC3OFS_L	AADC3OFS[7:0]							
0xB7				AADC4OFS_L	AADC4OFS[7:0]							
0xB8				AUDADC_H*	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9				AUD1ADC_L*	AUD1ADC[7:0]							
0xBA				AUD2ADC_L*	AUD2ADC[7:0]							
0xBB				AUD3ADC_L*	AUD3ADC[7:0]							
0xBC				AUD4ADC_L*	AUD4ADC[7:0]							
0xBD				ADJAADC_H*	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE				ADJAADC1_L*	ADJAADC1[7:0]							
0xBF				ADJAADC2_L*	ADJAADC2[7:0]							
0xC0				ADJAADC3_L*	ADJAADC3[7:0]							
0xC1				ADJAADC4_L*	ADJAADC4[7:0]							

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0xC8				MPP21	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0xC9				MPP43	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		
0xCA				CHMD	CHMD4		CHMD3		CHMD2		CHMD1	
0xCB				POLMPP	POLMPP4	POLMPP3	POLMPP2	POLMPP1	Reserved			
0xCC				SELCH	SELCH4		SELCH3		SELCH2		SELCH1	
0xCD				MAINCH	MAINCH4		MAINCH3		MAINCH2		MAINCH1	
0xCE				ANAPWDN	AAUTOMUTE	Reserved	A_DAC_PWDN	A_ADC_PWDN	V4_ADC_PWDN	V3_ADC_PWDN	V2_ADC_PWDN	V1_ADC_PWDN
0xCF				SMD	SMD		VRSTSEL		FIRSTCNUM			
0xD0				AIGAIN21	AIGAIN2				AIGAIN1			
0xD1				AIGAIN43	AIGAIN4				AIGAIN3			
0xD2				R_MULTCH	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH	
0xD3				R_SEQ10	R_SEQ_1				R_SEQ_0			
0xD4				R_SEQ32	R_SEQ_3				R_SEQ_2			
0xD5				R_SEQ54	R_SEQ_5				R_SEQ_4			
0xD6				R_SEQ76	R_SEQ_7				R_SEQ_6			
0xD7				R_SEQ98	R_SEQ_9				R_SEQ_8			
0xD8				R_SEQBA	R_SEQ_B				R_SEQ_A			
0xD9				R_SEQDC	R_SEQ_D				R_SEQ_C			
0xDA				R_SEQFE	R_SEQ_F				R_SEQ_E			

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0xDB				AMASTER	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER
0xDC				MIX_MUTE	LAWMD		MIX_DERATIO	MIX_MUTE				
0xDD				MIX_RATIO21	MIX_RATIO2				MIX_RATIO1			
0xDE				MIX_RATIO43	MIX_RATIO4				MIX_RATIO3			
0xDF				MIX_RATIOP	1	0	0	0	MIX_RATIOP			
0xE0				MIX_OUTSEL	VADCCKPOL	AADCCKPOL	ADACCKPOL	MIX_OUTSEL				
0xE1				ADET	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0xE2				ADET_TH21	ADET_TH2[3:0]				ADET_TH1[3:0]			
0xE3				ADET_TH43	ADET_TH4[3:0]				ADET_TH3[3:0]			
0xF0				ACKI_L	ACKI[7:0]							
0xF1				ACKI_M	ACKI[15:8]							
0xF2				ACKI_H	0	0	ACKI[21:16]					
0xF3				ACKN_L	ACKN[7:0]							
0xF4				ACKN_M	ACKN[15:8]							
0xF5				ACKN_H	0	0	0	0	0	0	ACKN[17:16]	
0xF6				SDIV	0	0	SDIV					
0xF7				LRDIV	0	0	LRDIV					
0xF8				ACCNTL	APZ	APG			Reserved	ACPL	SRPH	LRPH
0xF9				VMISC	LIM16	PBREFEN	YCBCR422	Reserved	VBI_FRAM	CNTL656	Reserved	
0xFA				CLKOCTL	VSCL_ENA	OE	CLKNO1_OEB	CLKPO1_OEB	CLKNO_MD		CLKPO_MD	
0xFB				AVDET_MODE	CLKNO_POL	CLKPO_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE	
0xFC				AVDET_ENA	AVDET_ENA							
0xFD				AVDET_STATE*	AVDET_STATE							
0xFE				TEST	DEV_ID[6:5]*		0	0	0	TEST		
0xFF				DEV_ID*	DEV_ID[4:0]*					REV_ID		

Note: * Read only registers

Register Descriptions

0X00(CH1)/0X10(CH2)/0X20(CH3)/0X30(CH4) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(CH1)/0X11(CH2)/0X21(CH3)/0X31(CH4) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(CH1)/0X12(CH2)/0X22(CH3)/0X32(CH4) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(CH1)/0X13(CH2)/0X23(CH3)/0X33(CH4) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X04(CH1)/0X14(CH2)/0X24(CH3)/0X34(CH4) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(CH1)/0X15(CH2)/0X25(CH3)/0X35(CH4) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(CH1)/0X16(CH2)/0X26(CH3)/0X36(CH4) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(CH1)/0X17(CH2)/0X27(CH3)/0X37(CH4) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	3

0X08(CH1)/0X18(CH2)/0X28(CH3)/0X38(CH4) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(CH1)/0X19(CH2)/0X29(CH3)/0X39(CH4) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(CH1)/0X1A(CH2)/0X2A(CH3)/0X3A(CH4) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0C

0X0B(CH1)/0X1B(CH2)/0X2B(CH3)/0X3B(CH4) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	C0

0X0C(CH1)/0X1C(CH2)/0X2C(CH3)/0X3C(CH4) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(CH1)/0X1D(CH2)/0X2D(CH3)/0X3D(CH4) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(CH1)/0X1E(CH2)/0X2E(CH3)/0X3E(CH4) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM(not supported) 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(CH1)/0X1F(CH2)/0X2F(CH3)/0X3F(CH4) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0XA0(CH1)/0XA1(CH2)/0XA2(CH3)/0XA3(CH4) – NT50

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register Standard Selection.	0
6-4	VSTD	R/W	Reserved	0h
3-0	CVFMT	R/W	Reserved	8h

0XA4(CH1)/0XA5(CH2)/0XA6(CH3)/0XA7(CH4) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0XC4(CH1)/0XC5(CH2)/0XC6(CH3)/0XC7(CH4) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator (Test purpose only)	X

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R	Reserved	00b
5	AUDIORST	W	A 1 written to this bit resets the Audio portion to its default state but all register content remains unchanged. This bit is self-resetting.When {AFS384,AIN5MD} state changes,AUDIOTST=1 is needed once.	0
4	VOUTRST	W	A 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting.	0
3	VDEC4RST	W	A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC3RST	W	A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC2RST	W	A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC1RST	W	A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X81 – ANALOG CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R/W		0h
3	CLKPDN	R/W	0 = Normal clock operation. 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active.	0
2	Reserved	R/W		0
1	YFLEN	R/W	Analog Video CH1/CH2/CH3/CH4 anti-alias filter control 1 = enable 0 = disable	1
0	Reserved	R/W		0

0X82 – ANALOG CONTROL REGISTER2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control for debugging use.(Test purpose only)	0
6	YCLEN	R/W	1 = Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
5	CKIPOL	R/W	36MHz clock output signal rise/fall timing. 0: change by 72MHz clock output falling edge. 1: change by 72MHz clock output rising edge.	0
4	Reserved	R		0
3	GTEST	R/W	1 = Test.(Test purpose only) 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0X83 – CONTROL REGISTER I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GMEN	R/W	Reserved.	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	00b
4-0	HSDLY	RW	Reserved for test.	00h

0X85 – VERTICAL SHARPNESS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3	VIN4	R/W	Ch4 Video ADC input signal select. 0:VIN4A, 1:VIN4B	0
2	VIN3	R/W	Ch3 Video ADC input signal select. 0:VIN3A, 1:VIN3B	0
1	VIN2	R/W	Ch2 Video ADC input signal select. 0:VIN2A, 1:VIN2B	0
0	VIN1	R/W	Ch1 Video ADC input signal select. 0:VIN1A, 1:VIN1B	0

0X86 – CORING CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X87 – CLAMPING GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0X88 – INDIVIDUAL AGC GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	Reserved	R	Reserved	0

0X8A – WHITE PEAK THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0X8B– CLAMP LEVEL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0X8C– SYNC AMPLITUDE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X8D – SYNC MISS COUNT REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR mode detection threshold.	4

0X8E – CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

0X8F – VERTICAL CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = short 0 = normal	0

0X90 – VERTICAL CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0X91 – COLOR KILLER LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0X92 – COMB FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HTL	R/W	0 = adaptive mode 1 = fixed comb	0
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X93 – LUMA DELAY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-2	Reserved	R/W		0
1-0	AAFLPF	RW	Anti-aliasing filter selection 00->9Mhz, 0dB gain 01->10MHz, -3.4dB gain 10->7MHz, 0dB gain 11->8MHz, -3.4dB gain	0

0X94 – MISCELLANEOUS CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	Reserved	R/W		0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	Reserved	R/W		0

0X95 – LOOP CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X96 – MISCELLANEOUS CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X97 – CLAMP MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto, 2 = default to 60Hz, 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None, 1 = smallest, 2 = small, 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top, 1 = Auto, 2 = Pedestal, 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0X98 – HSLOWCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HSBEGIN[3:0]	R/W	HSYNC Start position Control Bit3-0.	00
3-0	HSEND[3:0]	R/W	HSYNC End position Control Bit3-0.	00

0X99 – HSBEGIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSBEGIN[11:3]	R/W	HSYNC Start position Control Bit11-3.	13h

0X9A – HSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSEND[11:3]	R/W	HSYNC End position Control Bit11-3.	1Fh

0X9B – OVSDLY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	OVSDLY	R/W	VSYNC Start position. Control H position on VSYNC start.	44

0X9C – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC	R/W	1: the length of EAV to SAV is set up and fixed by HBLEN registers. 0: the length of SAV to EAV is set up and fixed by HACTIVE registers.	0
6-4	OFDLY	R/W	FIELD output delay. 0h:0H line delay FIELD output.(601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h:Reserved.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0X9D – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLEN	R/W	These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value. NTSC/PAL-M(60Hz): B8h(184dec)=1144-960 PAL/SECAM(50Hz): C0h(192dec)=1152-960 If Reg0x0E[3](ATRIG for CH1) is set to 0, this value changes into B8h or C0h at auto video format detection initial time automatically according to CH1 video detection status.	C0h

0X9E – NOVID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDELAYMD	R/W	0:normal VDELAY mode. 1: Optional VDELAY mode.	0
6	FC27	R/W	1:normal ITU-R656 operation 0:Reserved	1
5-4	CHID_MD	R/W	Select the Channel ID format for time-multiplexed output 0 No channel ID (default) 1 CHID with the specific ITU-R BT.656 sync Code 2 CHID with the specific horizontal blanking code 3 CHID with the specific ITU-R BT.656 sync & horizontal blanking code	0
3	NOVID_656	R/W	0:Normal ITU-R BT.656 SA/EAV(default) 1:AN optional set of ITU-R BT.656 SAV/EAV code for No-video status	0
2	EAVSWAP	R/W	1:EAV-SAV code is swapped. 0:EAV-SAV code is not swapped(standard 656 output mode)	0
1	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code. 1:Standard ITU-R656 code format.(It's also VIP task-A code format.) 0:Old VIP task-B code format.	1
0	NTSC656	R/W	1:Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0

0X9F – CLOCK OUTPUT DELAY CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLKNO_DEL	R/W	Control the clock delay of CLKNO pin. 0h/1h/3h/7h/Fh values are effective. 1h: about 3ns more delay, 3h: about 7ns more delay, 7h: about 10ns more delay, Fh: about 14ns more delay	0h
3-0	CLKPO_DEL	R/W	Control the clock delay of CLKPO pin. 0h/1h/3h/7h/Fh values are effective. 1h: about 3ns more delay, 3h: about 7ns more delay, 7h: about 10ns more delay, Fh: about 14ns more delay	0h

0XA8 – HFLT21

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT2	R/W	Reserved	0h
3-0	HFLT1	R/W	Reserved	0h

0XA9 – HFLT43

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT4	R/W	Reserved	0h
3-0	HFLT3	R/W	Reserved	0h

0XAA – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AGCEN4	R/W	Select Video AGC loop function on VIN4 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4	0
6	AGCEN3	R/W	Select Video AGC loop function on VIN3 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3	0
5	AGCEN2	R/W	Select Video AGC loop function on VIN2 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2	0
4	AGCEN1	R/W	Select Video AGC loop function on VIN1 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN1	0
3	AGCGAIN4[8]	R/W	AGCGAIN4 MSB bit	0
2	AGCGAIN3[8]	R/W	AGCGAIN3 MSB bit	0
1	AGCGAIN2[8]	R/W	AGCGAIN2 MSB bit	0
0	AGCGAIN1[8]	R/W	AGCGAIN1 MSB bit	0

0XAB – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN1[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN1 bit7-0.	F0h

0XAC – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN2[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN2 bit7-0.	F0h

0XAD – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN3[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN3 bit7-0.	F0h

0XAE – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN4[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGC GAIN4 bit7-0.	F0h

0XAF – VERTICAL PEAKING LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP2	R/W	Select CH2 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP1	R/W	Select CH1 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.				

0XB0 – VERTICAL PEAKING LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP4	R/W	Select CH4 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP3	R/W	Select CH3 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.				

0XB1 – NOVIDMODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CH8IDEN	R/W	Video Channel ID number has following value in Sync Code and Horizontal Blanking Code with CHNUM1, CHNUM2, CHNUM3 and CHNUM4. 0: 4 channel ID Only output VIN1A/VIN1B : {1'b0,CHNUM1[2:0]} VIN2A/VIN2B : {1'b0,CHNUM2[2:0]} VIN3A/VIN3B : {1'b0,CHNUM3[2:0]} VIN4A/VIN4B: {1'b0,CHNUM4[2:0]} 1: 8 channel ID output VIN1A : {1'b0,CHNUM1[2:0]} VIN2A : {1'b0,CHNUM2[2:0]} VIN3A : {1'b0,CHNUM3[2:0]} VIN4A : {1'b0,CHNUM4[2:0]} VIN1B : {1'b1,CHNUM1[2:0]} VIN2B : {1'b1,CHNUM2[2:0]} VIN3B : {1'b1,CHNUM3[2:0]} VIN4B : {1'b1,CHNUM4[2:0]}	0
6-0	Reserved	R/W		4Ah

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AADC4OFS[9:8]	R/W	Ch4 Digital ADC input data offset control bit9-8.	0h
5-4	AADC3OFS[9:8]	R/W	Ch3 Digital ADC input data offset control bit9-8.	0h
3-2	AADC2OFS[9:8]	R/W	Ch2 Digital ADC input data offset control bit9-8.	0h
1-0	AADC1OFS[9:8]	R/W	Ch1 Digital ADC input data offset control bit9-8.	0h
Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.				

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC1OFS[7:0]	R/W	Ch1 Digital ADC input data offset control bit7-0.	0h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC2OFS[7:0]	R/W	Ch2 Digital ADC input data offset control bit7-0.	0h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC3OFS[7:0]	R/W	Ch3 Digital ADC input data offset control bit7-0.	0h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC4OFS[7:0]	R/W	Ch4 Digital ADC input data offset control bit7-0.	0h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		0h
1-0	AADC5OFS[9:8]	R/W	Ch5 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC5OFS[7:0]	R/W	Ch5 Digital ADC input data offset control bit7-0.	0h

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AUD4ADC[9:8]	R	Bit9-8 of Ch4 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD3ADC[9:8]	R	Bit9-8 of Ch3 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD2ADC[9:8]	R	Bit9-8 of Ch2 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD1ADC[9:8]	R	Bit9-8 of Ch1 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD1ADC[7:0]	R	Bit7-0 of Ch1 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD2ADC[7:0]	R	Bit7-0 of Ch2 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD3ADC[7:0]	R	Bit7-0 of Ch3 Analog Audio ADC Digital Output Value by 2's format..	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD4ADC[7:0]	R	Bit7-0 of Ch4 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	AUD5ADC[9:8]	R	Bit9-8 of Ch5 Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD5ADC[7:0]	R	Bit7-0 of Ch5 Analog Audio ADC Digital Output Value by 2's format.	X

0XBD – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	ADJAADC4[9:8]	R	Bit9-8 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC3[9:8]	R	Bit9-8 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC2[9:8]	R	Bit9-8 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC1[9:8]	R	Bit9-8 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format.	X
The value shows the first input data in front of Digital Audio Decimation Filtering process.				

0XBE – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC1[7:0]	R	Bit7-0 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBF – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC2[7:0]	R	Bit7-0 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC3[7:0]	R	Bit7-0 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC4[7:0]	R	Bit7-0 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ADJAADC5[9:8]	R	Bit9-8 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC5[7:0]	R	Bit7-0 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC8 – MPP PIN OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL2	R/W	Write value select the general purpose value through the MPP2 pin output. Read value shows MPP2 pin input status. 0 : “0” value, 1: “1” value	0
6-4	MPP_MODE2	R/W	Select the output mode for MPP2 pin. Followings show the status when POLMPP2 register is set to 0. If POLMPP2 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active. 1:Vertical sync output. Low is V-sync active. 2:Field flag output. Low is field1 (Odd), High is field2 (Even). 3:Horizontal active signal output. High is H-active. 4:Vertical active & horizontal active signal output. High is VH-active. 5:No video flag. High is No-video, Low is Video. 6:Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL2 register value. If VDLOSSOE2 register is set to “1”, vdloss2 signal is output to MPP2 pin and these MPP_MODE2 function is not effective.	0h
3	GPP_VAL1	R/W	Write value select the general purpose value through the MPP1 pin output. Read value shows MPP1 pin input status. 0 : “0” value, 1: “1” value	0
2-0	MPP_MODE1	R/W	Select the output mode for MPP1 pin. Followings show the status when POLMPP1 register is set to 0. If each POLMPP1 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active.	0h

BIT	FUNCTION	R/W	DESCRIPTION	RESET
			1:Vertical sync output. Low is V-sync active. 2:Field flag output. Low is field1 (Odd), High is field2 (Even). 3:Horizontal active signal output. High is H-active. 4:Vertical active & horizontal active signal output. High is VH-active. 5:No video flag. High is No-video, Low is Video. 6: Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL1 register value. If VDLOSSOE1 register is set to “1”, vdloss1 signal is output to MPP1 pin and these MPP_MODE1 function is not effective.	

0XC9 – MPP PIN OUTPUT MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GPP_VAL4	R/W	Write value select the general purpose value through the MPP4 pin output. Read value shows MPP4 pin input status. 0 : “0” value, 1: “1” value	0
6-4	MPP_MODE4	R/W	Select the output mode for MPP4 pin. Followings show the status when POLMPP4 register is set to 0. If POLMPP4 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active. 1:Vertical sync output. Low is V-sync active. 2:Field flag output. Low is field1 (Odd), High is field2 (Even). 3:Horizontal active signal output. High is H-active. 4:Vertical active & horizontal active signal output. High is VH-active. 5:No video flag. High is No-video, Low is Video. 6: Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL4 register value. If VDLOSSOE4 register is set to “1”, vdloss4 signal is output to MPP4 pin and these MPP_MODE4 function is not effective.	0h
3	GPP_VAL3	R/W	Write value select the general purpose value through the MPP3 pin output. Read value shows MPP3 pin input status. 0 : “0” value, 1: “1” value	0
2-0	MPP_MODE3	R/W	Select the output mode for MPP3 pin. Followings show the status when POLMPP3 register is set to 0. If each POLMPP3 register is set to 1, following values have inversed status. 0:Horizontal sync output. Low is H-sync active.	0h

BIT	FUNCTION	R/W	DESCRIPTION	RESET
			1:Vertical sync output. Low is V-sync active. 2:Field flag output. Low is field1 (Odd), High is field2 (Even). 3:Horizontal active signal output. High is H-active. 4:Vertical active & horizontal active signal output. High is VH-active. 5:No video flag. High is No-video, Low is Video. 6: Vertical sync & horizontal sync signal output. Low is sync active. 7:GPP_VAL.Same as GPP_VAL3 register value. If VDLOSSOE3 register is set to “1”, vdloss3 signal is output to MPP3 pin and these MPP_MODE3 function is not effective.	

0XCA – VIDEO CHANNEL OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CHMD4	R/W	Select video bus output mode on 8bit VD4[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	0h
5-4	CHMD3	R/W	Select video bus output mode on 8bit VD3[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	0h
3-2	CHMD2	R/W	Select video bus output mode on 8bit VD2[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	0h
1-0	CHMD1	R/W	Select video bus output mode on 8bit VD1[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	0h

0XCB –POLMPP

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	POLMPP4	R/W	Select MPP4 pin output polarity. 0: normal, 1: inverse polarity.	0
6	POLMPP3	R/W	Select MPP3 pin output polarity. 0: normal, 1: inverse polarity.	0
5	POLMPP2	R/W	Select MPP2 pin output polarity. 0: normal, 1: inverse polarity.	0
4	POLMPP1	R/W	Select MPP1 pin output polarity. 0: normal, 1: inverse polarity.	0
3-0	Reserved	R/W		0h

0XCC – 2ND CHANNEL SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	SELCH4	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	0h
5-4	SELCH3	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	3h
3-2	SELCH2	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: Ch4 video output	2h
1-0	SELCH1	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	1h

0XCD – 1ST CHANNEL SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	MAINCH4	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	3h
5-4	MAINCH3	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	2h
3-2	MAINCH2	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	1h
1-0	MAINCH1	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	0h

0XCE – ANALOG POWER DOWN CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAUTOMUTE	R/W	1: When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200. 0: No effect	0
6	Reserved	R/W		0
5	A_DAC_PWDN	R/W	Power down the audio DAC. 0: Normal operation 1: Power down	0
4	A_ADC_PWDN	R/W	Power down the audio ADC. 0: Normal operation 1: Power down	0
3-0	V_ADC_PWDN	R/W	Power down the video ADC. V_ADC_PWDN[3:0] stands for CH4 to CH1. 0: Normal operation 1: Power down	0h

0XCF – SERIAL MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	SMD	R/W	Set up cascade Audio Serial mode. When SMD=2hex or 3hex, ALINKO pin output cascaded audio serial data. When SMD=0hex, ALINKO pin output is tri-state. 00:No Serial mode. ALINKO pin is tri-state output. 10: ALINKO pin is Serial out pin. ALINKI pin is Serial input pin.	0h
5-4	VRSTSEL	R/W	Select VRST (V reset) signal on ACKG (Audio Clock Generator) refin input. 0 Ch1 VRST 1 Ch2 VRST 2 Ch3 VRST 3 Ch4 VRST	0h
3-0	Reserved	R/W		0h

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD0	7-4	AIGAIN2	R/W	Code -> gain (full scale voltage in peak to peak)	8h
0xD1		AIGAIN4	R/W	0000 -> -9.0dB (2.8V p2p)	
0x7F		AIGAIN5	R/W	0001 -> -7.5dB (2.4V p2p)	
0xD0	3-0	AIGAIN1	R/W	0010 -> -6.0dB (2.0V p2p)	8h
0xD1		AIGAIN3	R/W	0011 -> -4.5dB (1.67V p2p) 0100 -> -3.0dB (1.41V p2p) 0101 -> -1.5dB (1.18V p2p) 0110 -> -0dB (1.00V p2p) (use as design default) 0111 -> +1.5dB (0.84V p2p) 1000 -> +3.0dB (0.71V p2p)(default) 1001 -> +4.5dB (0.59V p2p) 1010 -> +6.0dB (0.50V p2p) 1011 -> +7.5dB (0.42V p2p) 1100 -> +9.0dB (0.35V p2p) 1101 -> +10.5dB (0.30V p2p) 1110 -> +12.0dB (0.25V p2p) 1111 -> +13.5dB (0.21V p2p)	
0x7F		MIXRATIO5	R/W	Audio input AIN5 ratio value for audio mixing	0h

0XD2 – NUMBER OF AUDIO TO BE RECORDED

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	M_RLSWAP	R/W	Define the sequence of mixing and playback audio data on the ADATM pin. If RM_SYNC=0 : I2S format, 0:Mixing audio on position 0 and playback audio on position 8 1:Playback audio on position 0 and mixing audio on position 8 If RM_SYNC=1 : DSP format, 0:Mixing audio on position 0 and playback audio on position 1 1:Playback audio on position 0 and mixing audio on position 1	0
6	RM_SYNC	R/W	Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin. 0: I2S format 1: DSP format	0
5-4	RM_PBSEL	R/W	Select the output PlayBackIn data for the ADATM pin. 0 First Stage PalyBackIn audio 1 Second Stage PalyBackIn audio 2 Third Stage PalyBackIn audio 3 Last Stage PalyBackIn audio	0h
3-2	R_ADATM	R/W	Select the output mode for the ADATM pin. 0:Digital serial data of mixing audio 1:Digital serial data of ADATR format record audio 2:Digital serial data of ADATM format record audio	0h
1-0	R_MULTCH	R/W	Define the number of audio for record on the ADATR pin. 0 2 audios 1 4 audios 2 8 audios 3 16 audios Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. In addition, each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers.	0h

0XD3, 0XD4, 0XD5, 0XD6, 0XD7, 0XD8, 0XD9, 0XDA – SEQUENCE OF AUDIO TO BE RECORDED

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD3	7-4	R_SEQ1	R/W	Define the sequence of record audio on the ADATR pin. Refer to Figure 14 and Table 5 for the detail of the R_SEQ_0 ~ R_SEQ_F. The default value of R_SEQ_0 is “0”, R_SEQ_1 is “1”, and R_SEQ_F is “F”. 0 AIN1 1 AIN2 2 AIN3 : : : : 14 AIN15 15 AIN16	1h
	3-0	R_SEQ0	R/W		0h
0xD4	7-4	R_SEQ3	R/W		3h
	3-0	R_SEQ2	R/W		2h
0xD5	7-4	R_SEQ5	R/W		5h
	3-0	R_SEQ4	R/W		4h
0xD6	7-4	R_SEQ7	R/W		7h
	3-0	R_SEQ6	R/W		6h
0xD7	7-4	R_SEQ9	R/W		9h
	3-0	R_SEQ8	R/W		8h
0xD8	7-4	R_SEQB	R/W		Bh
	3-0	R_SEQA	R/W		Ah
0xD9	7-4	R_SEQD	R/W		Dh
	3-0	R_SEQC	R/W		Ch
0xDA	7-4	R_SEQF	R/W		Fh
	3-0	R_SEQE	R/W		Eh

0XDB –MASTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ADACEN	R/W	Audio DAC Function mode 0:Audio DAC function disable(test purpose only) 1:Audio DAC function enable	1
6	AADCEN	R/W	Audio ADC Function mode 0:Audio ADC function disable(test purpose only) 1:Audio ADC function enable	1
5	PB_MASTER	R/W	Define the operation mode of the ACLKP and ASYNP pin for playback. 0:All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1:TW2960 type I2S/DSP Master mode (ACLKP and ASYNP is output)	0
4	PB_LRSEL	R/W	Select audio data to be used for playback input. If PB_SYNC=0 I2S format, 0: 1st Left channel audio data(default), 1: 1st Right channel audio data. If PB_SYNC=1 DSP format, 0: 1st input audio data. 1: 2nd input audio data	0
3	PB_SYNC	R/W	Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin. 0:I2S format 1:DSP format	0
2	RM_8BIT	R/W	Define output data format per one word unit on ADATR pin. 0:16bit one word unit output 1:8bit one word unit packed output	0
1	ASYNROEN	R/W	Define input/output mode on the ASYNR pin. 1:ASYNR pin is input 0:ASYNR pin is output	1
0	ACLKRMASTER	R/W	Define input/output mode on the ACLKR pin and set up audio system processing. 0:ACLKR pin is input. External 256xfs or 320fs or 384xfs clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1:ACLKR pin is output. Internal ACKG generates audio system clock.	0

0XDC –U-LAW/A-LAW OUTPUT AND MIX MUTE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	LAWMD	R/W	Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin. 0:PCM output 1:SB(Signed MSB bit in PCM data is inverted) output 2:u-Law output 3:A-Law output	0
5	MIX_DERATIO	R/W	Disable the mixing ratio value for all audio. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly	0
4-0	MIX_MUTE	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0] : Audio input AIN1. MIX_MUTE[1] : Audio input AIN2. MIX_MUTE[2] : Audio input AIN3. MIX_MUTE[3] : Audio input AIN4. MIX_MUTE[4] : Playback audio input. 0:Normal 1:Muted.	10h

0X7E – MIX_MUTE_A5

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	A5OUTOFF	R/W	AIN5 data output control on ADATR record signal. 0: output AIN51/AIN52/AIN53/AIN54 record data on ADATR. 1: not output AIN51/AIN52/AIN53/AIN54 record data on ADATR.	1
6	ADATM_I2SOEN	R/W	Define ADATM pin output 2 word data to make standard I2S output. 0:Mixing Data or Playback Input data are only output on ADATM pin by M_RLSWAP register.(default) 1:L/R data on ADATM pin is selected by I2SO_RSEL / I2SO_LSEL registers.	0
5	MIX_MUTE_A5	R/W	MIX_MUTE_A5: Audio input AIN5 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH5[4:0]	R/W	AIN5 threshold value for audio detection	03h

0X72 – MIX RATIO VALUE 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	MRATIOMD	R/W	Audio Mixing ratio value divider control 0: MIX_RATIOn 0 0.25 (default) 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: MIX_RATIO / 64	0
6	ADACTEST	R/W	0: must be set up 0 in normal mode. 1: test purpose only	0
5	AOFFCORE	R/W	0: Audio No-input Noise reduction on(Test purpose only) 1: Audio No-input Noise reduction off	0

0X72 – MIX RATIO VALUE 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4	DAORATIO	R/W	Digital Audio Output Gain is controlled by following. 0: DAOGAIN 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00(default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: DAOGAIN / 64	0
3-0	DAOGAIN	R/W	Digital Audio Output Gain. Gain is controlled with DAORATIO mode.	8h

0XDD – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO2	R/W	Audio input AIN2 ratio value for audio mixing	0
3-0	MIX_RATIO1	R/W	Audio input AIN1 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO4	R/W	Audio input AIN4 ratio value for audio mixing	0
3-0	MIX_RATIO3	R/W	Audio input AIN3 ratio value for audio mixing	0

0XDF – ANALOG AUDIO OUTPUT GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	AOGAIN	R/W	Output voltage swing control Code -> Output gain (peak to peak voltage) 0000 -> -22.5dB (0.11V p2p) 0001 -> -21.0dB (0.13V p2p) 0010 -> -19.5dB (0.15V p2p) 0011 -> -18.0dB (0.18V p2p) 0100 -> -16.5dB (.21V p2p) 0101 -> -15.0dB (0.25V p2p) 0110 -> -13.5dB (0.29V p2p) 0111 -> -12.0dB ((0.35V p2p) 1000 -> -10.5dB (0.42V p2p) 1001 -> -9.0dB (0.50V p2p) 1010 -> -7.5dB (0.59V p2p) 1011 -> -6.-dB (0.70V p2p) 1100 -> -4.5dB (0.83V p2p) 1101 -> -3.0dB (0.98V p2p) *default value 1110 -> -1.5dB (1.17V p2p) 1111 -> 0dB (1.4V p2p)	Dh
3-0	MIX_RATIOP	R/W	Playback audio input ratio value for audio mixing.	0h

0XE0 – MIX OUTPUT SELECTION 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VADCCKPOL	R/W	Test purpose only.	0
6	AADCCKPOL	R/W	1:Analog Audio ADC input clock polarity inverse 0:not inverse.	0
5	ADACCKPOL	R/W	Test purpose only.	0

0XE0 – MIX OUTPUT SELECTION 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4-0	MIX_OUTSEL	R/W	Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10(Ah) Select record audio of channel 11 11(Bh) Select record audio of channel 12 12(Ch) Select record audio of channel 13 13(Dh) Select record audio of channel 14 14(Eh) Select record audio of channel 15 15(Fh) Select record audio of channel 16 16(10h) Select playback audio of the first stage chip PB1 17(11h) Select playback audio of the first stage chip PB2 18(12h) Select playback audio of the last stage chip PB3 19(13h) Select playback audio of the first stage chip PB4 20(14h) Select mixed audio 21(15h) Select record audio of channel AIN51 22(16h) Select record audio of channel AIN52 23(17h) Select record audio of channel AIN53 24(18h) Select record audio of channel AIN54 Others no sound. Default 1Fh.	1Fh

0XE1 – AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAMPMD	R/W	Define the audio detection method. 0: Detect audio if absolute amplitude is greater than threshold 1: Detect audio if differential amplitude is greater than threshold(recommended)	1
6-4	ADET_FILT	R/W	Select the filter for audio detection 0: Wide LPF. . . . 7: Narrow LPF	7
3	ADET_TH4[4]*	R/W	MSB bit of AIN4 threshold value for audio detection.	0
2	ADET_TH3[4]*	R/W	MSB bit of AIN3 threshold value for audio detection.	0
1	ADET_TH2[4]*	R/W	MSB bit of AIN2 threshold value for audio detection.	0
0	ADET_TH1[4]*	R/W	MSB bit of AIN1 threshold value for audio detection.	0

* Note:

ADET_TH :Define the threshold value for audio detection.

ADET_TH1: Audio input AIN1.

ADET_TH2: Audio input AIN2.

ADET_TH3: Audio input AIN3.

ADET_TH4: Audio input AIN4.
ADET_TH5: Audio input AIN5.

0:Low value (default)

. .

. .

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH2[3:0]	R/W	Bit3-0 of AIN2 threshold value for audio detection.	3h
3-0	ADET_TH1[3:0]	R/W	Bit3-0 of AIN1 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH4[3:0]	R/W	Bit3-0 of AIN4 threshold value for audio detection.	3h
3-0	ADET_TH3[3:0]	R/W	Bit3-0 of AIN3 threshold value for audio detection.	3h

AUDIO CLOCK INCREMENT

0XF0 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[7:0]	R/W	ACKI[7:0], these bits control ACKI Clock Increment in ACKG block. ACKI[21:0]: 074823h for fs = 8kHz is default.	23h

0XF1 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[15:8]	R/W	ACKI[15:8], these bits control ACKI Clock Increment in ACKG block.	48h

0XF2 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0h
5-0	ACKI[21:16]	R/W	ACKI[21:16], these bits control ACKI Clock Increment in ACKG block.	07h

0XF3 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[7:0]	R/W	Reserved.	00h

0XF4 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[15:8]	R/W	Reserved.	01h

0XF5 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ACKN[17:16]	R/W	Reserved.	0h

0XF6 – SERIAL CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	SDIV	R/W	These bits control SDIV Serial Clock Divider in ACKG block.	00h

0XF7 – LEFT/RIGHT CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	LRDIV	R/W	Reserved.	20h

0XF8 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	APZ	R/W	These bits control Loop in ACKG block.	1
6-4	APG	R/W	These bits control Loop in ACKG block.	4h
3	Reserved	R		0
2	ACPL	R/W	These bits control Loop closed/open in ACKG block. 0: Loop closed(special purpose only) 1 :Loop open(normal function mode)	1
1	SRPH	R/W	Reserved.	0
0	LRPH	R/W	Reserved.	0

0XF9 – VIDEO MISCELLANEOUS FUNCTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LIM16	R/W	0: Output ranges are limited to 2~254 1: Output ranges are limited to 16~235 for Y and 16~239 for CbCr	0
6	PBREFEN	R/W	Audio ACKG Reference (refin) input select for test purpose. When ACPL=1, this function is no effect. 0: ACKG has video VRST refin input selected by VRSTSEL register 1: ACKG has audio ASYNP refin input	1
5	YCBCR422	R/W	Control YCbCr 4:2:2 output mode 0: Normal 4:2:2 output mode 1: Averaging 4:2:2 output mode	0
4	Reserved	R/W		0
3	VBI_FRAM	R/W	Test purpose only.	0
2	CNTL656	R/W	Select invalid data value. 0: 0x80 and 0x10 code will be output as invalid data during active video line. 1: 0x00 code will be output as invalid data during active video line.	0
1-0	Reserved	R/W		0

0XFA – OUTPUT ENABLE CONTROL AND CLOCK OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6	OE	R/W	Control the tri-state of output pin 0: Outputs are Tri-state except clock output (CLKPO, CLKNO) pin 1: Outputs are enabled	0
5	CLKNO_OEB	R/W	Control the tri-state of CLKNO pin 0: Output is enabled (default) 1: Output is Tri-state	0
4	CLKPO_OEB	R/W	Control the tri-state of CLKPO pin 0: Output is enabled 1: Output is Tri-state	0
3-2	CLKNO_MD	R/W	Control the clock frequency of CLKNO pin 0: 36MHz clock output 1: 72MHz clock output 2: 144MHz clock output 3: always 0 value	0h
1-0	CLKPO_MD	R/W	Control the clock frequency of CLKPO pin 0: 36MHz clock output 1: 72MHz clock output 2: 144MHz clock output 3: always 0 value	0h

0XFB – CLOCK POLARITY CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLKNO_POL	R/W	Polarity inverse control on output CLKNO signal just before CLKNO pin. 0: Not inversed. 1: Polarity inverse. Good for 36MHz/72MHz clock output.	0
6	CLKPO_POL	R/W	Polarity inverse control on output CLKPO signal just before CLKPO pin. 0: Not inversed. Good for 36MHz/72MHz clock output. 1: Polarity inverse.	0
5	IRQENA	R/W	Enable/Disable the interrupt request through the IRQ pin. 0: Disable 1: Enable	0
4	IRQPOL	R/W	Select the polarity of interrupt request through the IRQ pin. 0: Falling edge requests the interrupt and keeps its state until cleared 1: Rising edge requests the interrupt and keeps its state until cleared	0
3-2	ADET_MODE	R/W	Define the polarity of state register and interrupt request for audio detection. 0: No interrupt request by the audio detection 1: Make the interrupt request rising only when the audio signal comes in 2: Make the interrupt request falling only when the audio signal goes out 3: Make the interrupt request rising and falling when the audio comes in and goes out	3
1-0	VDET_MODE	R/W	Define the polarity of state register and interrupt request for video detection. 0: No interrupt request by the video detection 1: Make the interrupt request rising only when the video signal comes in 2: Make the interrupt request falling only when the video signal goes out 3: Make the interrupt request rising and falling when the video comes in and goes out	3

0XFC – ENABLE VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET_ENA	R/W	Enable state register updating and interrupt request of video and audio detection for each input. [0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	FFh

0X73 – ENABLE VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	Reserved	R	Reserved	00h
2	AIN51FORM	R/W	AIN51/52/53/54 record output format selection. This bit is only effective when A51OUTOFF register is set to 0. When AIN1/2/3/4/51 and AIN6/7/8/9/52 are required to be continuous order in record output, 1 is necessary. 0: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat4><dat5> <dat6><dat7><dat51>< dat52> R dat : <dat8><dat9><datA><datB><datC><datD> <datE><datF><dat53><dat54> If DSP mode(RM_SYNC=1) all data are continuous. <dat0><dat1><dat2><dat3><dat4><dat5><dat6> <dat7><dat8><dat9><datA><datB><datC><datD> <datE><datF><dat51><dat52><dat53><dat54> 1: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat51><dat4> <dat5><dat6><dat7><dat52> R dat : <dat8><dat9><datA><datB><dat53><datC> <datD>< datE>< datF><dat54> If DSP mode(RM_SYNC=1) all data continuous. <dat0><dat1><dat2><dat3>< dat51><dat4><dat5> <dat6><dat7><dat52><dat8><dat9><datA><datB> <dat53><datC><datD><datE><datF><dat54>	0
1	AINTPOFF	R/W	0:must be set up 1:test purpose only	0
0	A51DET_ENA	R/W	Enable state register updating and interrupt request of audio AIN51 (AIN5 input in this chip) detection for each input. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	0

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET_STATE	R/W	State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE. [0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4. 0 Inactivated 1 Activated	00h

0X74 – STATUS OF VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R		00h
0	A5DET_STATE	R/W	State of Audio AIN51(AIN5 input in this chip) detection. This bit is activated according ADET_MODE. 0 Inactivated 1 Activated	0

0XFE – DEVICE ID AND REVISION ID FLAG

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	DEV_ID[6:5]	R	Bit6-5 of Device ID. Together with 0xFF[7:3] indicate TW2960 product ID code. DEV_ID=7'h1C	0
5-3	Reserved	R		0
2-0	TEST	R/W	Test purpose only. This must be 0 in normal mode.	0

0XFF – DEVICE ID AND REVISION ID FLAG

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	DEV_ID[4:0]	R	Bit4-0 of Device ID.	1Ch
2:0	REV_ID	R	The revision number. REV_ID=3'h0 1st TW2960chip.	0h

0X60 – CLOCK PLL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PLLCKOUT	R/W	0: must be set up in normal mode. 1: MPP1 pin output 144MHz Clock - in phase in Clock PLL MPP2 pin output 144MHz Clock - 90 degree phase shift in Clock PLL MPP3 pin output 144MHz Clock - 180 degree phase shift in Clock PLL MPP4 pin output 144MHz Clock – 270 degree phase shift in Clock PLL	0
6	PLL_PD	R/W	Clock PLL Power down control. 0: Clock PLL normal mode. 1: Clock PLL power down mode.	0
5	PLL_IREF	R/W	Clock PLL Current bias reference. 0: reference 0. 1: reference 1.	0
4	SEL_X24	R/W	Clock PLL output mode 0: 2x XTI input frequency.72MHz clock input mode. 1: 4x XTI input frequency.36MHz clock input mode.	1
3-2	LP_X4	R/W	Loop resistor for PLL. 0: 80.5kΩ. 1: 35.5kΩ. 2: 25.5kΩ. 3: 20.5kΩ.	1h
1-0	CP_X4	R/W	Charge-pump current for PLL. 0: 1μA. 1: 5μA. 2: 10μA. 3: 15μA.	1h

0X61 – 144MHZ CLOCK SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R	Reserved	0h
4	DECOSC	R/W	Video Decoder system clock select. 0: Clock PLL output 144MHz/4 clock is selected. 1: system clock generated by XTI input crystal clock. If 144MHz is connected, system clock is XTI / 4 If 72MHz is connected, system clock is XTI / 2. If 36MHz is connected, system clock is XTI.	1
3-2	CKOUTSEL	R/W	Clock PLL output 144MHz select. 0: 144MHz Clock output - in phase. 1: 144MHz Clock output - 90 degree phase shift. 2: 144MHz Clock output - 180 degree phase shift. 3: 144MHz Clock output – 270 degree phase shift.	0h
1-0	XTIMD	R/W	XTI pin input clock process control. If XTIMD=0/1/2, Clock PLL Output clock is not used for internal logic process. 0: 36MHz XTI input clock is used for all clock source. 1: 72MHz XTI input clock is used for all clock source. 2: 144MHz XTI input clock is used for all clock source. 3: Clock PLL 144MHz output is used for all system clock source.	3h

0X62 – MPP0E

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	MPP4OE	R/W	0 : MPP4 pin is input 1 : MPP4 pin is output	1
2	MPP3OE	R/W	0 : MPP4 pin is input 1 : MPP3 pin is output	1
1	MPP2OE	R/W	0 : MPP2 pin is input 1 : MPP2 pin is output	0
0	MPP1OE	R/W	0 : MPP1 pin is input 1 : MPP1 pin is output	0

0X63 – CHANNEL ID 21

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6-4	CH2NUM	R/W	Set up Channel ID number in VIN2A/VIN2B video decoder data output.	1h
3	Reserved	R/W		0
2-0	CH1NUM	R/W	Set up Channel ID number in VIN1A/VIN1B video decoder data output.	0h

0X64 – CHANNEL ID 43

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6-4	CH4NUM	R/W	Set up Channel ID number in VIN4A/VIN4B video decoder data output.	3h
3	Reserved	R/W		0
2-0	CH3NUM	R/W	Set up Channel ID number in VIN3A/VIN3B video decoder data output.	2h

0X65 – VIDEO BUS TRI-STATE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0h
5	VD_36C	R/W	0:36MHz clock output type1 is selected. 1:36MHz clock output type2 is selected.	0
4	VD4ORD	R/W	Select the video channel output order on 4xD1 output mode. 0:Ch1->Ch2->Ch3->Ch4->Ch1->Ch2->Ch3->....(increase). 1:Ch4->Ch3->Ch2->Ch1->Ch4->Ch3->Ch2->....(decrease)	0
3	VD4OEB	R/W	VD4[7:0] output tri-state control. 1: tri-state output VD4[7:0]. 0: normal output VD4[7:0].	0
2	VD3OEB	R/W	VD3[7:0] output tri-state control. 1: tri-state output VD3[7:0]. 0: normal output VD3[7:0].	0
1	VD2OEB	R/W	VD2[7:0] output tri-state control. 1: tri-state output VD2[7:0]. 0: normal output VD2[7:0].	0
0	VD1OEB	R/W	VD1[7:0] output tri-state control. 1: tri-state output VD1[7:0]. 0: normal output VD1[7:0].	0

0X70 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6	S2I_8BIT	R/W	0: ACLKP/ASYNP/ADATP pin input is 16-bit control. 1: ACLKP/ASYNP/ADATP pin input is 8-bit control.	0
5	ACLKRPOL	R/W	ACLKR input signal polarity inverse. 0: not inverse. 1: inverse.	0
4	ACLKPPOL	R/W	ACLKP input signal polarity inverse. 0: not inverse. 1: inverse.	0
3	AFAUTO	R/W	ACKI[21:0] control automatic set up with AFMD registers. This mode is only effective when ACLKRMASTER=1. 0: ACKI[21:0] registers set up ACKI control. 1: ACKI control is automatically set up by AFMD register values.	1
2-0	AFMD	R/W	AFAUTO control mode. 0: 8kHz setting (default). 1: 16kHz setting. 2: 32kHz setting. 3: 44.1kHz setting. 4: 48kHz setting.	0h

0X71 – DIGITAL AUDIO INPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	I2S8MODE	R/W	8-bit I2S Record output mode. 0: L/R half length separated output. 1: One continuous packed output equal to DSP output format.	0
6	MASCKMD	R/W	Audio Clock Master ACLKR output wave format. 0: High period is one 36MHz clock period. 1: Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up ACKI registers. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1. SDIV=00h is used with this function normally.	1
5	PBINSWAP	R/W	Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping. 0: Not swapping. 1: Swapping.	0
4	ASYNRDLY	R/W	ASYNR input signal delay. 0: No delay. 1: Add one 27MHz period delay in ASYNR signal input.	0
3	ASYNPDLY	R/W	ASYNP input signal delay. 0: No delay. 1: Add one 36MHz period delay in ASYNP signal input.	0
2	ADATPDLY	R/W	ADATP input data delay by one ACLKP clock. 0: No delay. This is for I2S type 1T delay input interface. 1: Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.	0
1-0	INLAWMD	R/W	Select u-Law/A-Law/PCM/SB data input format on ADATP pin. 0:PCM input 1:SB(Signed MSB bit in PCM data is inverted) input 2:u-Law input 3:A-Law input	0h

0X7B – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_RSEL	R/W	Select R-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

*Note :
Both I2SO_RSEL and I2SO_LSEL select output data by following order.

0	Select record audio of channel 1(AIN1)
1	Select record audio of channel 2(AIN2)
2	Select record audio of channel 3(AIN3)
3	Select record audio of channel 4(AIN4)
4	Select record audio of channel 5(AIN5)
5	Select record audio of channel 6(AIN6)
6	Select record audio of channel 7(AIN7)
7	Select record audio of channel 8(AIN8)
8	Select record audio of channel 9(AIN9)
9	Select record audio of channel 10(AIN10)
10(Ah)	Select record audio of channel 11(AIN11)
11(Bh)	Select record audio of channel 12(AIN12)
12(Ch)	Select record audio of channel 13(AIN13)
13(Dh)	Select record audio of channel 14(AIN14)
14(Eh)	Select record audio of channel 15(AIN15)
15(Fh)	Select record audio of channel 16(AIN16)
16(10h)	Select playback audio of the first stage chip(PB1)
17(11h)	Select playback audio of the second stage chip(PB2)
18(12h)	Select playback audio of the third stage chip(PB3)
19(13h)	Select playback audio of the last stage chip(PB4)
20(14h)	Select mixed audio.
21(15h)	Select record audio of channel 51(AIN51)(default)
22(16h)	Select record audio of channel 52(AIN52)
23(17h)	Select record audio of channel 53(AIN53)
24(18h)	Select record audio of channel 54(AIN54)
Others	no audio output.

0X7C – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_LSEL	R/W	Select L-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h
* Note : Please read 0x7B Note for detail description.				

0X7D – AIN51/52/53/54 RECORD OUTPUT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	I2SRECSEL54	R/W	Select output data in bellow dat54 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	3h
5-4	I2SRECSEL53	R/W	Select output data in bellow dat53 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	2h
3-2	I2SRECSEL52	R/W	Select output data in bellow dat52 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	1h
1-0	I2SRECSEL51	R/W	Select output data in bellow dat51 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	0

These registers are only effective when A51OUTOFF=0.These registers function change under AIN51FORM control at that time as follows.

When AIN51FORM=0:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat51><dat52>

R data : <dat8><dat9><datA><datB><datC><datD><datE><datF><dat53><dat54>

If DSP mode(RM_SYNC=1), all data are continuous.

<dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat8><dat9><datA><datB><datC>

<datD><datE><datF><dat51><dat52><dat53><dat54>

When AIN51FORM=1:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52>

R data : <dat8><dat9><datA><datB><dat53><datC><datD><datE><datF><dat54>

If DSP mode(RM_SYNC=1),all data are continuous.

<dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52><dat8><dat9>
<datA><datB><dat53><datC><datD><datE><datF><dat54>

All other datN(N=0,1,2,,,,F) are selected by R_SEQ_N registers

0X89 – AUDIO FS MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATHROUGH	R/W	0: must be set up in normal mode. 1: test purpose only.	0
6	ASYNSERIAL	R/W	ALINKO/ALINKI bit rate. 0: 36MHz.Effective for all Fs clock mode. 1: 18MHz.Effective for Fs 8kHz/16kHz mode.	1
5	ACLKR128	R/W	ACLKR clock output mode for special 16x8bit(total 128bit) data interface. 0: ACLKR output is normal. 1: the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8-bit mode (special purpose).	0
4	ACLKR64	R/W	ACLKR clock output mode for special 4 word output interface.ACLKRMASTER=1 mode only. 0: ACLKR output is normal 1: the number of ACLKR clock per fs is 64.	0
3	AFS384	R/W	Special Audio fs Sampling mode. 0: Audio fs Sampling mode is normal 256xfs if AIN5=0. 1: Audio fs Sampling mode is 384xfs mode.	0
2	AIN5MD	R/W	Audio Input process mode. 0: AIN1/AIN2/AIN3/AIN4 4 Audio input only process. This mode is 256xfs if AFS384=0.In this mode, AIN5 input is not processed. 1: AIN1/AIN2/AIN3/AIN4/AIN5 5 Audio input process. This mode is 320xfs Mode if AFS384=0.	0
1-0	Reserved	R		0h

0XB2 – VDLOSS OUTPUT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0h
3	VDLOSSOE4	R/W	VIN4A/VIN4B Video Decoder VDLOSS4 output MPP4 pin. 0: not output VDLOSS4 on MPP4 pin (default). 1:VIN4A/VIN4B Video Decoder VDLOSS4 output on MPP4 pin.	
2	VDLOSSOE3	R/W	VIN3A/VIN3B Video Decoder VDLOSS3 output MPP3 pin. 0: not output VDLOSS3 on MPP3 pin (default). 1:VIN3A/VIN3B Video Decoder VDLOSS3 output on MPP3 pin.	
1	VDLOSSOE2	R/W	VIN2A/VIN2B Video Decoder VDLOSS2 output MPP2 pin. 0: not output VDLOSS2 on MPP2 pin (default). 1:VIN2A/VIN2B Video Decoder VDLOSS2 output on MPP2 pin.	
0	VDLOSSOE1	R/W	VIN1A/VIN1B Video Decoder VDLOSS1 output MPP1 pin. 0: not output VDLOSS1 on MPP1 pin (default). 1:VIN1A/VIN1B Video Decoder VDLOSS1 output on MPP1 pin.	0

0X53 – AUDIO DAC TEST CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	TAADCO	R/W	Audio ADC Test Purpose only. When TEST(regFE[2:0]) register is set to 6h, MPP4,MPP3,VD4[7:0]} pins have audio ADC data output by following selection. 0 : AIN1 Audio ADC data output 1 : AIN2 Audio ADC data output 2 : AIN3 Audio ADC data output 3 : AIN4 Audio ADC data output 4 : AIN5 Audio ADC data output	0
3	ADAC_CNTL[3]	R/W	DAC reference voltage source 0-> use VDD/R as the voltage reference 1-> use VDD/R and LPF as the voltage reference (when this is selected, it rejects more power supply noise)	0
2	ADAC_CNTL[2]	R/W	Clk_inv 0-> normal operation. The incoming DAC data is latched by an inverted clock (referenced to the incoming clock) 1-> clock inverted operation. The incoming DAC data is latched by a buffered clock (referenced to the incoming clock)	0
1	ADAC_CNTL[1]	R/W	DAC common mode voltage reference source 0-> use VDD/R as the voltage reference 1-> use VDD/R and LPF as the voltage reference (when this is selected, it rejects more power supply noise)	0
0	ADAC_CNTL[0]	R/W	Test_en. This is not used for the test 0-> Output driver is enabled 1-> output driver is disabled	0

0X54 – AUDIO ADC CONTROL 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5	DOUT_RST	R/W	Audio ADC digital output reset for all channel. This bit must be set up to 0 again after 1 value is set up.	0
4	DIV_RST	R/W	Audio ADC divider reset. This bit must be set up to 0 again after 1 value is set up.	0
3	ACALEN	RW	Audio ADC Calibration control. This bit must be set up to 0 again after 1 value is set up.	0
2-0	Reserved	R/W		7

0X55 –VIDEO ADC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IBINBUF_SEL	R/W	Bias current control for AFE input buffers 000->20µA (default) 001->30µA 010->40µA 011->50µA	0
5-4	IB_ADC	R/W	ADC bias current selection 00->10µA 01->15µA 10->20µA (default) 11->25µA	0
3-2	ICLAMP_SEL	R/W	Digital clamp current selection 00->10µA 01->20µA (default) 10->30µA 11->40µA	1
1-0	VCMIN_SEL	R/W	Input common mode selection 00->700mV 01->800mV 10->900mV (default) 11->100mV	2

0X56 – AUDIO ADC CONTROL 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R/W		0
3-2	AFE_CNTL[3:2]	R/W	Bias current control for channel 4, and channel 3. Note: channel 0, 1, and 2 are designed with fixed bias current 00-> normal operation. Bias current is 20µA 01-> 20µA (for testing only) 10->40µA (for testing only) 11->50µA (for testing only)	0
7-0	AFE_CNTL[1:0]	R/W	Bias control for the ADC 00-> 10µA (default) 01->15µA 10->20µA 11->25µA	0

0X5C– BGCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	TVADCO	R/W	Video ADC Test Purpose only. When TEST(regFE[2:0]) register is set to 4h, MPP4,MPP3,VD4[7:0]} pins have video ADC data output by following selection. 0 : VIN1A/VIN1B video ADC data output 1 : VIN2A/VIN2B video ADC data output 2 : VIN3A/VIN3B video ADC data output 3 : VIN4A/VIN4B video ADC data output	0
5	BGCTL	R/W	0: Reg96[7:0] control all CH1/CH2/CH3/CH4 video. 1: Reg96[7:0] control only CH1 video. Reg5D[7:0] control only CH2 video. Reg5E[7:0] control only CH3 video. Reg5F[7:0] control only CH4 video.	0
4	VSWEN	R/W	0: Video Input VIN1A/VIN1B,VIN2A/VIN2B, VIN3A/VIN3B,VIN4A/VIN4B are selected by register VIN1/VIN2/VIN3/VIN4. 1: One Video input time of either VINnA or VINnB changes automatically by VSWNUM setting.	0
3-0	VSWNUM	R/W	One Video input time is (VSWNUM+1) frame time in VIN1A/VIN1B video when VSWEN=1. 0: 1 frame time in VIN1A/VIN1B video. 1: 2 frame time in VIN1A/VIN1B video. 2: 3 frame time in VIN1A/VIN1B video. . . F: 16 frame time in VIN1A/VIN1B video.	1

0X5D – CH2 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_2	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_2	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_2	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_2	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_2	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_2	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_2	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_2	R/W	1 = Enable blue stretch. 0 = Disabled.	0

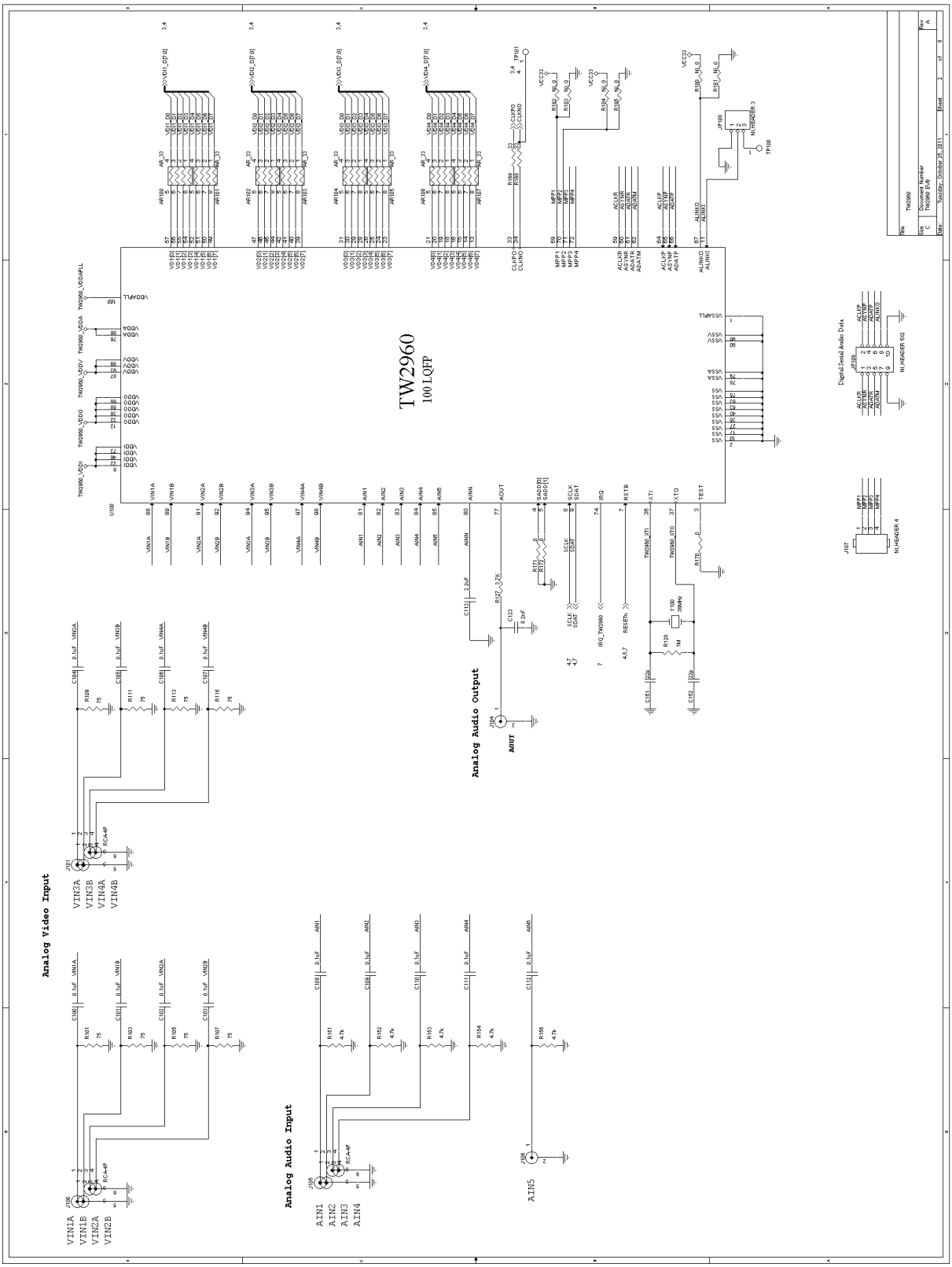
0X5E – CH3 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_3	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_3	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_3	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_3	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_3	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_3	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_3	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_3	R/W	1 = Enable blue stretch. 0 = Disabled.	0

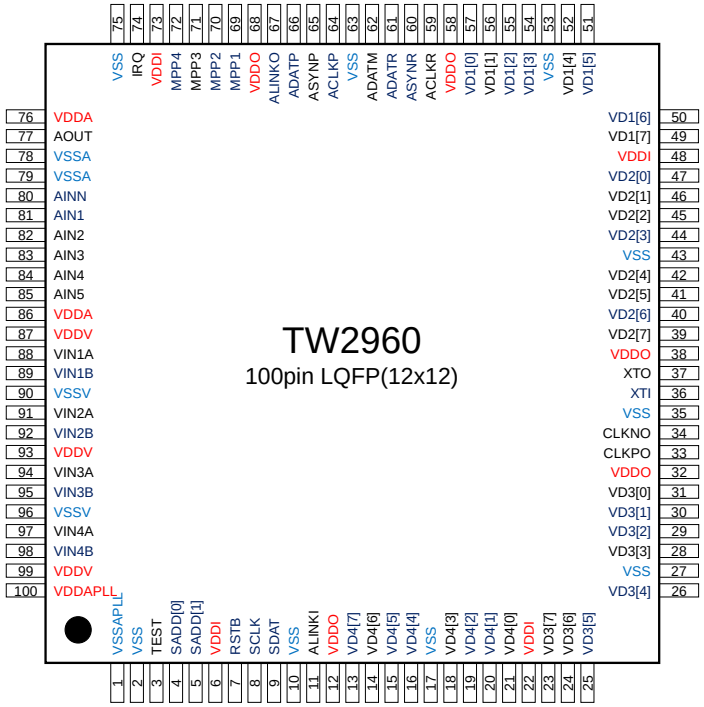
0X5F – CH4 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_4	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_4	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_4	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_4	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_4	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_4	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_4	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_4	R/W	1 = Enable blue stretch. 0 = Disabled.	0

Application Schematic



Pin Diagram


TW2960
100pin LQFP(12x12)
1 VSSAPLL
2 VSS
3 TEST
4 SADD[0]
5 SADD[1]
6 VDDI
7 RSTB
8 SCLK
9 SDAT
10 VSS
11 ALINKI
12 VDDO
13 VD4[7]
14 VD4[6]
15 VD4[5]
16 VD4[4]
17 VSS
18 VD4[3]
19 VD4[2]
20 VD4[1]
21 VD4[0]
22 VDDI
23 VD3[7]
24 VD3[6]
25 VD3[5]
26 VD3[4]
27 VSS
28 VD3[3]
29 VD3[2]
30 VD3[1]
31 VD3[0]
32 VDDO
33 CLKPO
34 CLKNO
35 VSS
36 XTI
37 XTO
38 VDDO
39 VD2[7]
40 VD2[6]
41 VD2[5]
42 VD2[4]
43 VSS
44 VD2[3]
45 VD2[2]
46 VD2[1]
47 VD2[0]
48 VDDI
49 VD1[7]
50 VD1[6]
51 VD1[5]
52 VD1[4]
53 VSS
54 VD1[3]
55 VD1[2]
56 VD1[1]
57 VD1[0]
58 VDDO
59 ACLKR
60 ASYNR
61 ADATR
62 ADATM
63 VSS
64 ACLKP
65 ASYNP
66 ADATP
67 ALINKO
68 VDDO
69 MPP1
70 MPP2
71 MPP3
72 MPP4
73 VDDI
74 IRQ
75 VSS
76 VDDA
77 AOUT
78 VSSA
79 VSSA
80 AINN
81 AIN1
82 AIN2
83 AIN3
84 AIN4
85 AIN5
86 VDDA
87 VDDV
88 VIN1A
89 VIN1B
90 VSSV
91 VIN2A
92 VIN2B
93 VDDV
94 VIN3A
95 VIN3B
96 VSSV
97 VIN4A
98 VIN4B
99 VDDV
100 VDDAPLL

Pin Descriptions

Analog Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VIN1A	88	A	Composite video input A of channel 1.
VIN1B	89	A	Composite video input B of channel 1.
VIN2A	91	A	Composite video input A of channel 2.
VIN2B	92	A	Composite video input B of channel 2.
VIN3A	94	A	Composite video input A of channel 3.
VIN3B	95	A	Composite video input B of channel 3.
VIN4A	97	A	Composite video input A of channel 4.
VIN4B	98	A	Composite video input B of channel 4.
AIN1	81	A	Audio input of channel 1.
AIN2	82	A	Audio input of channel 2.
AIN3	83	A	Audio input of channel 3.
AIN4	84	A	Audio input of channel 4.
AIN5	85	A	Audio input of channel 5.
AINN	80	A	Audio input negative control.
AOUT	77	A	Audio output.

Digital Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VD1[7:0]	49, 50, 51, 52, 54, 55, 56, 57	O	Video data output of channel 1.
VD2[7:0]	39,40,41,42, 44, 45, 46, 47	O	Video data output of channel 2.
VD3[7:0]	23, 24, 25, 26, 28, 29, 30, 31	O	Video data output of channel 3.
VD4[7:0]	13, 14, 15, 16, 18, 19, 20, 21	O	Video data output of channel 4.
MPP1	69	IO	HS/VS/FLD/ACTIVE/NOVID of channel 1.
MPP2	70	IO	HS/VS/FLD/ACTIVE/NOVID of channel 2.
MPP3	71	IO	HS/VS/FLD/ACTIVE/NOVID of channel 3.
MPP4	72	IO	HS/VS/FLD/ACTIVE/NOVID of channel 4.
ACLKR	59	IO	Audio serial clock input/output of record.
ASYNR	60	IO	Audio serial sync input/output of record.
ADATR	61	O	Audio serial data output of record.
ADATM	62	O	Audio serial data output of mixing.
ACLKP	64	IO	Audio serial clock input/output of playback.
ASYNP	65	IO	Audio serial sync input/output of playback.
ADATP	66	I	Audio serial data input of playback.
ALINKI	11	I	Audio Multi-chip operation serial input.
ALINKO	67	O	Audio Multi-chip operation serial output.

System Control Pins

NAME	NUMBER	TYPE	DESCRIPTION
RSTB	7	I	System reset.
XTI	36	I	Crystal 36MHz connection or Oscillator clock input.
XTO	37	O	For crystal 36MHz connection.
CLKPO	33	O	36/72/144MHz clock output.
CLKNO	34	O	36/72/144MHz clock output.
TEST	3	I	Test pin. Connect to ground.
SCLK	8	I	Serial control clock line.
SDAT	9	IO	Serial control data line.
SADD[1:0]	5,4	I	Serial control address.
IRQ	74	O	Interrupt request output.

Power and Ground Pins

NAME	NUMBER	TYPE	DESCRIPTION
VDDI	6, 22, 48, 73	P	1.8V Power for internal logic.
VDDO	12, 32, 38, 58, 68	P	3.3V Power for output driver.
VSS	2, 10, 17, 27, 35, 43, 53, 63, 75	G	Ground for internal logic and output driver.
VDDV	87, 93, 99	P	1.8V Power for analog video ADC.
VSSV	90,96	G	Ground for analog video ADC.
VDDA	76,86	P	1.8V Power for analog audio.
VSSA	78,79	G	Ground for analog audio.
VDDAPLL	100	P	1.8V Power for clock PLL.
VSSAPLL	1	G	Ground for clock PLL.

Parametric Information

AC/DC Electrical Parameters

TABLE 6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDDVM	-	-	1.92	V
VDDA (Measured to VSSA)	VDDAM	-	-	1.92	V
VDDAPLL (Measured to VSSAPLL)	VDDAPLLM	-	-	1.92	V
V DDI (Measured to VSS)	VDDIM	-	-	1.98	V
VDDO (Measured to VSS)	VDDOM	-	-	3.6	V
Voltage on any Digital Signal Pin (See the note below)	-	VSS –0.5	-	5.5	V
Analog Video Input Voltage	-	VSSV – 0.5	-	1.92	V
Analog Audio Input Voltage	-	VSSA– 0.5	-	2.4	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	0	-	+125	°C
Reflow Soldering	T_{PEAK}	255 +5/-0 (10-30 seconds)			°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges listed in Table 6 can induce destructive latch-up.

TABLE 7. CHARACTERISTICS

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
SUPPLY					
Power Supply — IO	VDDO	3.15	3.3	3.6	V
Power Supply — Analog Video	VDDV	1.62	1.8	1.92	V
Power Supply — Analog Audio	VDDA	1.62	1.8	1.92	V
Power Supply — Clock PLL	VDDAPLL	1.62	1.8	1.92	V
Power Supply — Digital	VDDI	1.62	1.8	1.98	V
Maximum|VDDI – VDDV|		-	-	0.3	V
Maximum|VDDI – VDDA|		-	-	0.3	V
Maximum|VDDI – VDDAPLL|		-	-	0.3	V
VIN1A, VIN1B, VIN2A, VIN2B, VIN3A, VIN3B, VIN4A, VIN4B Input Range		0.5	1.0	1.4	V

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
(AC Coupling Required)					
AIN1, AIN2, AIN3, AIN4, AIN5 Input Range (AC Coupling Required)		0.21	1.4	2.4	V
Ambient Operating Temperature	T_A	-40		+85	°C
Analog Video Supply Current	Ivddv	-	42	-	mA
Analog Audio Supply Current	Ivdda	-	12	-	mA
Clock PLL Supply Current	Ivddapll	-	2	-	mA
Digital I/O Supply Current	Iddi	-	26	-	mA
Digital Core Supply Current	Iddo	-	86	-	mA
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDO} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} = V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4V)	C_{IN}	-	5	-	pF
DIGITAL OUTPUTS					
Output High Voltage (I_{OH} = –2mA)	V_{OH}	2.4	-	V_{DDO}	V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF
ANALOG VIDEO INPUT					
Analog Pin Input Voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
VIDEO ADCS					
ADC Resolution	ADCR	-	10	-	bits
ADC Integral Non-Linearity	AINL	-	±1	-	LSB
ADC Differential Non-Linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f_{ADC}	-	36	-	MHz
Video Bandwidth (-3db)	BW	-	10	-	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}	-	15.625	-	kHz
Line Frequency (60Hz)	f_{LN}	-	15.734	-	KHz

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Static Deviation	Δf_H	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
Lock In Range	Δf_H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal Frequency (Fundamental)		-	36	-	MHz
Deviation (Note 1)		-	-	±50	ppm
Load Capacitance	CL	-	18	-	pF
Series Resistor (ESR)	RS	-	50	-	Ω
OSCILLATOR INPUT					
Nominal Frequency		-	36	-	MHz
Deviation		-	-	±50	ppm
Duty Cycle		-	-	55	%

NOTE:

1. Crystal deviation is base on normal operation condition.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

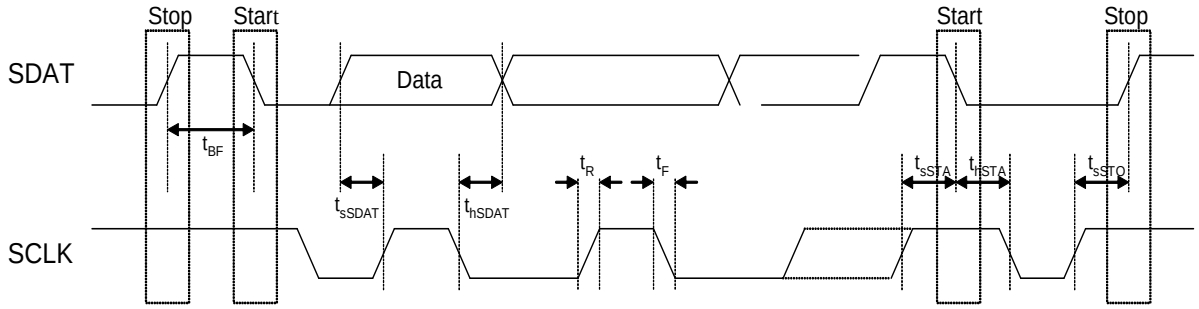
Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	74			ns
SDAT Hold Time	t_{hSDAT}	50		900	ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for each Bus Line	C_{BUS}			400	pF
SCLK Clock Frequency	f_{SCLK}			400	KHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Serial Host Interface Timing Diagram

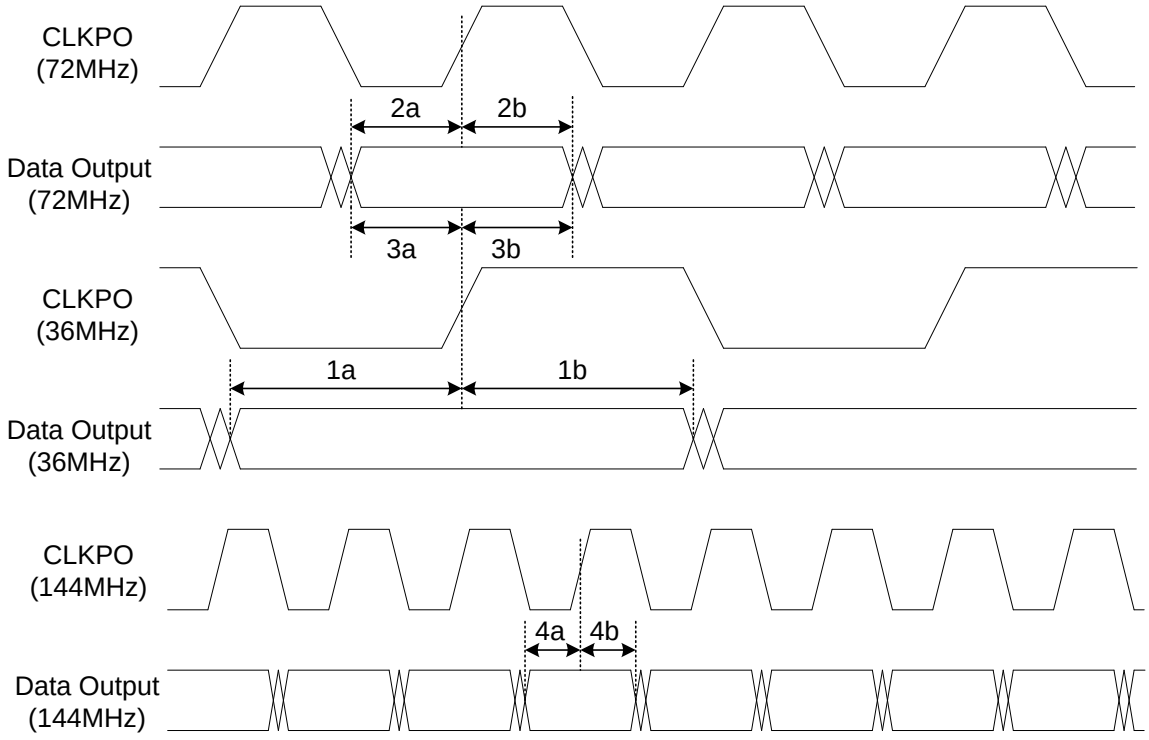


CLKPO and Video Data Timing

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Setup from CLKPO(36MHz) to Video Data(36MHz)	1a	8		10	ns
Hold from CLKPO(36MHz) to Video Data(36MHz)	1b	15		17	ns
Setup from CLKPO(72MHz) to Video Data(72MHz)	2a	6		8	ns
Hold from CLKPO(72MHz) to Video Data(72MHz)	2b	3		6	ns
Setup from CLKPO(36MHz) to Video Data(72MHz)	3a	8		10	ns
Hold from CLKPO(36MHz) to Video Data(72MHz)	3b	2		4	ns
Setup from CLKPO(144MHz) to Video Data(144MHz)	4a	2		3.5	ns
Hold from CLKPO(144MHz) to Video Data(144MHz)	4b	3		4	ns

NOTE:

1. CLKPO timing is related with CLKPO_DEL register value. The following timing diagram is illustrated in the case that the CLKPO_DEL is set to 0hex and CLKPO_POL is set to 0.CLKNO timing is inversed CLKPO timing as default setting. CLKPO_DEL/CLKNO_DEL can make more timings.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

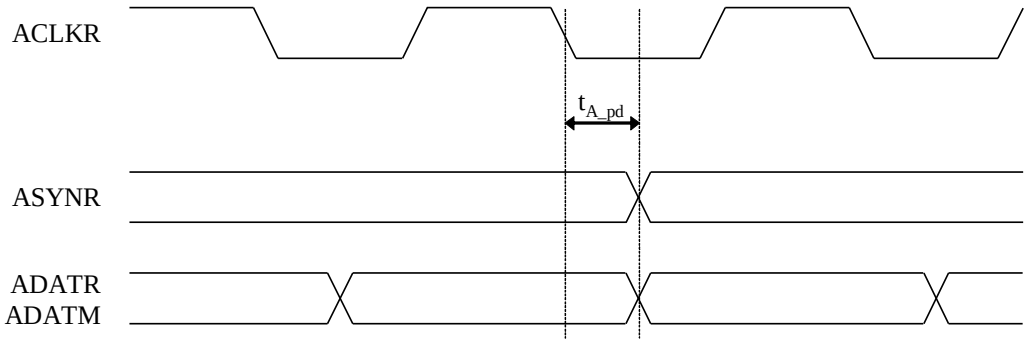


Digital Serial Audio Interface Timing

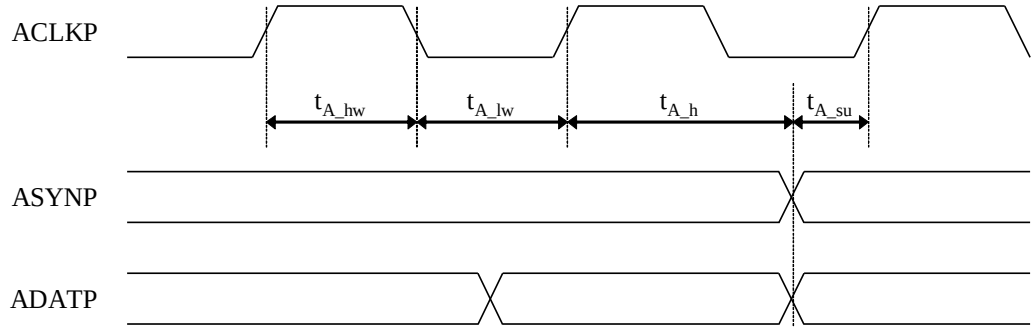
PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
ASYNR, ADATR, ADATM Propagation Delay	T_{A_pd}	1.0		4	ns
ACLKP High Pulse Duration	T_{A_hw}	27			ns
ACLKP Low Pulse Duration	T_{A_lw}	54			ns
ASYNP, ADATP Setup Time	T_{A_su}	26			ns
ASYNP, ADATP Hold Time	T_{A_h}	25			ns

NOTE:

1. T_{A_lw} Min value and T_{A_su} Min value are Fs=48KHz mode only.If Fs < 48KHz, these Min values are more bigger. High period of ACLKR/ACLKP is 36MHz one clock period.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



(A) RECORD AND MIX AUDIO(MASTER MODE)



(B) PLAYBACK AUDIO(MASTER MODE)

Analog Audio Parameters

PARAMETER	SYMBOL	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG AUDIO INPUT CHARACTERISTICS					
AIN1-5 Input Impedance	RINX	10			kΩ
Interchannel gain mismatch			0.2		dB
Input voltage range		0	1.4	2.4	Vpp
Full scale input voltage (peak to peak) (Note 1)	ViFULL	0.21	1.4	2.4	Vpp
Interchannel Isolation (Note 2)			90		dB
ANALOG AUDIO OUTPUT CHARACTERISTICS					
AOUT Output Load Resistance	RLAO	300			ohm
AOUT Load Capacitance	CLAO			1	nF
AOUT Offset Voltage	VOSAO			100	mV
Full Scale Output Voltage (Note 3)	V_{OFULL}		1.0	1.4	Vpp

NOTE:

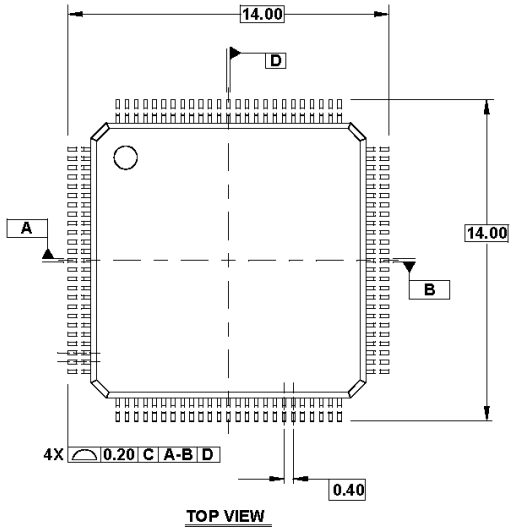
1. Tested at input gain of 0 dB, Fin = 1kHz.
2. Tested at input gain of 0 dB, Fs=8kHz and 16kHz.
3. Tested at output gain of 0 dB, Fout = 1kHz.
4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Package Outline Drawing

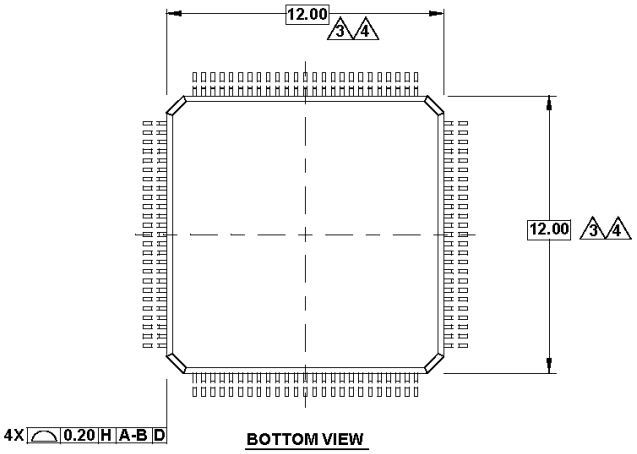
Q100.12X12

100 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE (LQFP)

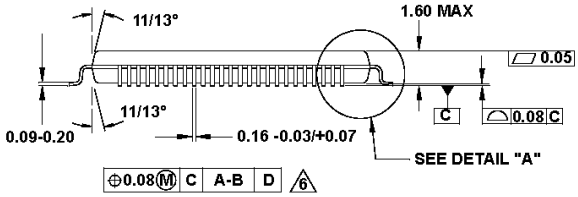
Rev 1, 6/11



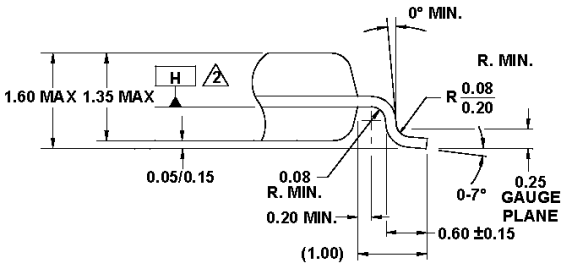
TOP VIEW



BOTTOM VIEW

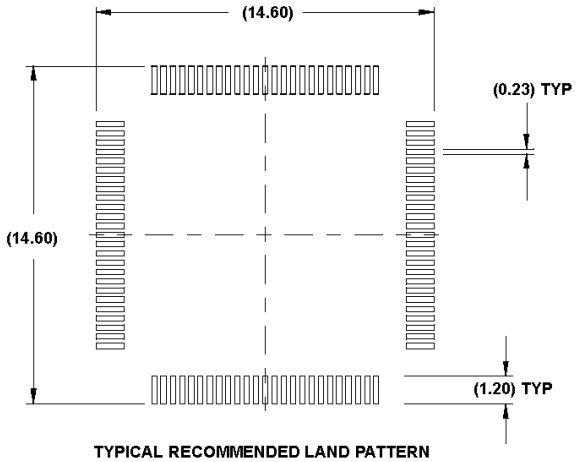


SIDE VIEW



DETAIL "A"

SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.25mm per side.
4. These dimensions to be determined at datum plane H.
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
6. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Controlling dimension: millimeter.
8. This outline conforms to JEDEC publication 95 registration MS-026, variation ADE.
9. Dimensions in ( ) are for reference only.

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

DATE	REVISION	CHANGE
January 18, 2012	FN7942.0	Initial release.
June 7, 2012	FN7942.1	Changed package outline drawing into correct version.