TW3801

SLOC™ Camera Modem PHY IC for Security Surveillance Applications

Preliminary Data Sheet

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Document Revision History

Version	Date	Description	By
Rev 0.1	2010.08.13	Initial	Vicky Huang
Rev 0.2	2010.08.18	Correct pin 51, 52, 58, 59 Power and Ground on Pin Diagram.	Vicky Huang
Rev 0.3	2010.08.26	Correct pin 36 (MII2RCLK) and pin 37 (MII2TCLK). Rename pin 67 from COAX_IO to COAX_O and pin 78 from RX_IN to COAX_I.	Vicky Huang
Rev 0.4	2010.10.01	Correct pin numbers for VDD_DAC, VSS_DAC, VDD_PLL and VSS_PLL	Vicky Huang
Rev 0.5	2010.12.10	Add Electrical information and package drawing	Vicky Huang
Rev 0.6	2011.01.21	Add Crystal characteristic and power on sequence	Vicky Huang
Rev 0.7	2011.03.07	Add Analog and Digital I/O timing characteristics	Vicky Huang
Rev 0.8	2011.03.24	Update register settings for B1 chip	Vicky Huang
Rev 0.9	2011.04.01	Add pin description for Pin 46,47,50	Vicky Huang
Rev 0.10	2011.05.03	Add pin description for Analog and Digital pins. Update MODE_S1, MODE_S0 transmission speed for B2 revision	SJ Kim Vicky Huang

Introduction

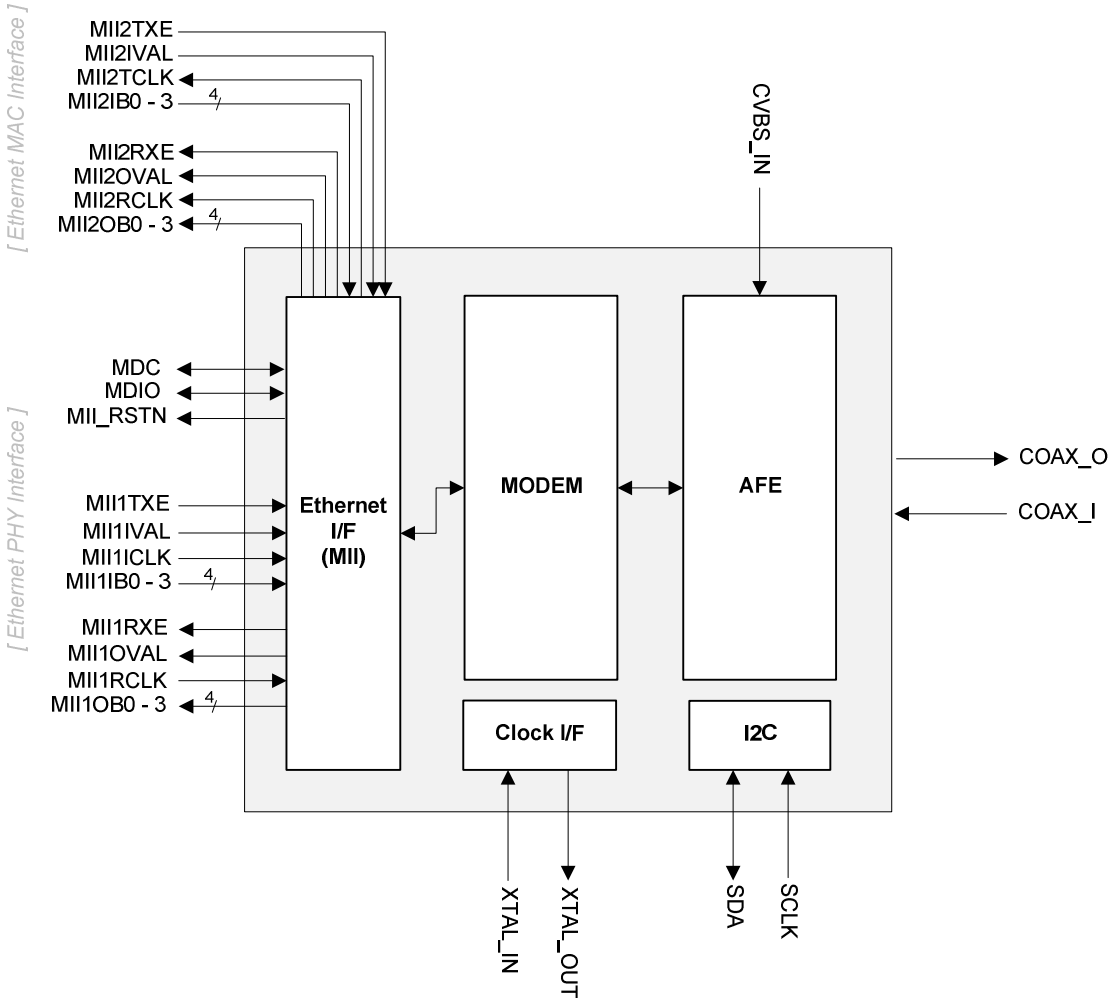
SLOC (a.k.a. Security Link Over Coax) is Intersil's advanced modem PHY technology that simultaneously transmits analog CVBS video and digital IP video over a single coaxial cable. This innovative modem PHY technology enables modern mega-pixel IP camera to operate in the existing CCTV coaxial cable infrastructure without the need for new wiring or modifications. Having both analog CVBS video and digital IP video in the same coaxial transmission enables system manufacturer to architect a cost-effective hybrid surveillance system supporting both traditional analog CCTV and modern networked IP surveillance applications.

The TW3801 is a SLOC-based camera modem PHY IC designed to operate with a SLOC-based receiver modem PHY IC like the Techwell TW3811. The combination of TW3801 and TW3811 enables high-performance and robust communications between the camera and the receiver and can operate over a very long coaxial cable. The TW3801 is a highly integrated modem PHY subsystem that includes an AFE, a digital modem, and two Ethernet MII interfaces. The device accepts an analog CVBS signal and an Ethernet MII signal and internally combines these signals into one proprietary output signal for transmission over a coaxial cable.

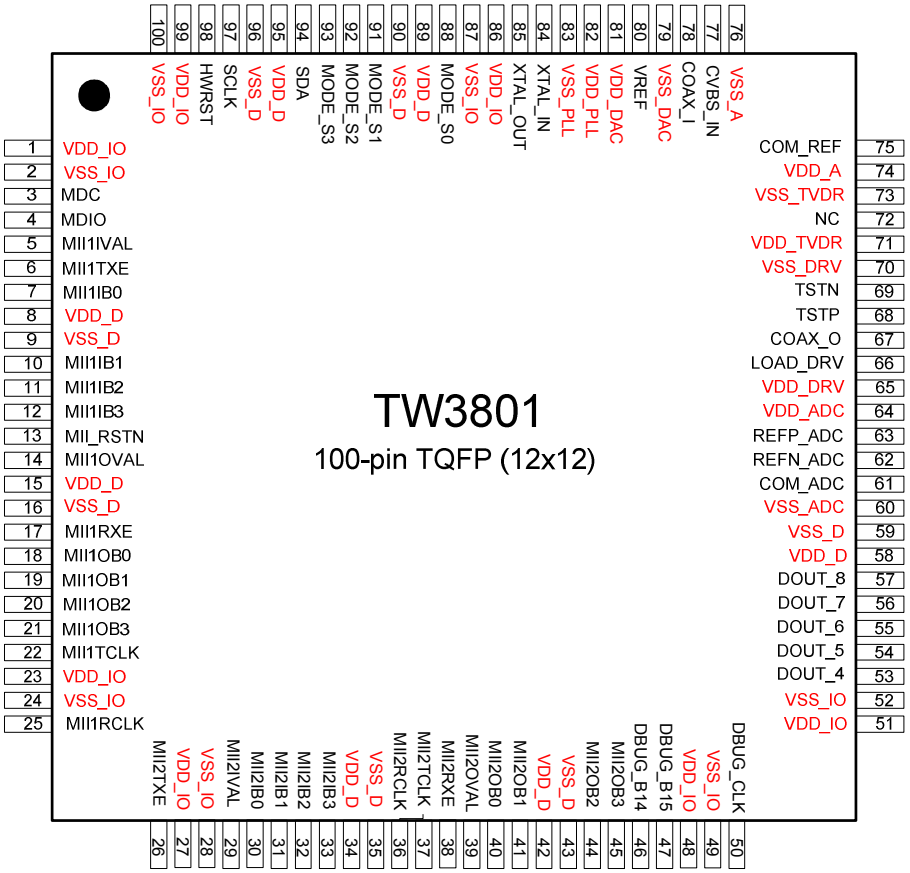
Key Features

- Simultaneous transmission of analog CVBS video & digital IP data over a long coaxial cable (up to 500m)
- Analog CVBS video preview support using same BNC output
  - CVBS-only output via proprietary smart detection technology
- Full-duplex digital communications
  - Downlink throughput up to 36Mbps (from camera to receiver)
  - Uplink throughput up to 11Mbps (from receiver to camera)
- Ethernet MAC MII interface for interfacing to camera processor DSP/SoC
- Optional Ethernet PHY MII interface for interfacing to external Ethernet PHY chip
- 2-wire control interface
- Integrated PLL with 25MHz XTAL
- 1.8V, 3.3V supply
- Low power consumption
- Package: 100-TQFP (12x12mm)

Block Diagram



Pin Diagram


TW3801
100-pin TQFP (12x12)
1 VDD_IO
2 VSS_IO
3 MDC
4 MDIO
5 MII1IVAL
6 MII1TXE
7 MII1IB0
8 VDD_D
9 VSS_D
10 MII1IB1
11 MII1IB2
12 MII1IB3
13 MII_RSTN
14 MII1OVAL
15 VDD_D
16 VSS_D
17 MII1RXE
18 MII1OB0
19 MII1OB1
20 MII1OB2
21 MII1OB3
22 MII1TCLK
23 VDD_IO
24 VSS_IO
25 MII1RCLK
26 MII2TXE
27 VDD_IO
28 VSS_IO
29 MII2IVAL
30 MII2IB0
31 MII2IB1
32 MII2IB2
33 MII2IB3
34 VDD_D
35 VSS_D
36 MII2RCLK
37 MII2TCLK
38 MII2RXE
39 MII2OVAL
40 MII2OB0
41 MII2OB1
42 VDD_D
43 VSS_D
44 MII2OB2
45 MII2OB3
46 DBUG_B14
47 DBUG_B15
48 VDD_IO
49 VSS_IO
50 DBUG_CLK
51 VDD_IO
52 VSS_IO
53 DOUT_4
54 DOUT_5
55 DOUT_6
56 DOUT_7
57 DOUT_8
58 VDD_D
59 VSS_D
60 VSS_ADC
61 COM_ADC
62 REFN_ADC
63 REFP_ADC
64 VDD_ADC
65 VDD_DRV
66 LOAD_DRV
67 COAX_O
68 TSTP
69 TSTN
70 VSS_DRV
71 VDD_TVDR
72 NC
73 VSS_TVDR
74 VDD_A
75 COM_REF
76 VSS_A
77 CVBS_IN
78 COAX_I
79 VSS_DAC
80 VREF
81 VDD_DAC
82 VDD_PLL
83 VSS_PLL
84 XTAL_IN
85 XTAL_OUT
86 VDD_IO
87 VSS_IO
88 MODE_S0
89 VDD_D
90 VSS_D
91 MODE_S1
92 MODE_S2
93 MODE_S3
94 SDA
95 VDD_D
96 VSS_D
97 SCLK
98 HWRST
99 VDD_IO
100 VSS_IO

Pin Description

Power & Ground Pins

Name	Number	Type	Description
VDD_IO	1, 23, 27, 48, 51,86, 99	P	Digital I/O Power 3.3V
VSS_IO	2, 24, 28, 49, 52, 87, 100	G	Digital I/O Ground
VDD_D	8, 15, 34, 42 58, 89, 95	P	Digital Core Power 1.8V
VSS_D	9, 16, 35, 43 59, 90, 96	G	Digital Core Ground
VDD_ADC	64	P	ADC Analog Power
VSS_ADC	60	G	ADC Analog Ground
VDD_DRV	65	P	Driver Analog Power
VSS_DRV	70	G	Driver Analog Ground
VDD_TVDR	71	P	TV Driver Analog Power
VSS_TVDR	73	G	TV Driver Analog Ground
VDD_A	74	P	Analog Power
VSS_A	76	G	Analog Ground
VDD_DAC	81	P	DAC Analog Power
VSS_DAC	79	G	DAC Analog Ground
VDD_PLL	82	P	PLL Analog Power
VSS_PLL	83	G	PLL Analog Ground

Analog Pins

Name	Number	Type	Description
COM_ADC	61	A	ADC Reference Voltage. This pin is for an internal ADC reference amplifier. A 0.1uF ceramic capacitor should be connected between the pin and ground
REFN_ADC	62	A	ADC Reference Voltage. This pin is for a differential reference (-) for ADC. A 0.1uF ceramic capacitor should be connected between the pin and ground
REFP_ADC	63	A	ADC Reference Voltage. This pin is for a differential reference (+) for ADC. A 0.1uF ceramic capacitor should be connected between the pin and ground
LOAD_DRV	66	A	Driver Load. Connect a 1.5Kohm 1% resistor to ground. To avoid interference, please ensure that the PCB trace from this pin is not parallel to the PCB trace from the COAX_O pin. This can be achieved by placing the resistor on the bottom side of PCB and routing the trace in the opposite direction from the COAX_O trace.
COAX_O	67	A	Coaxial TX Output. This pin is a high impedance current source output. Connect a75ohm 1% resistor to ground and AC coupling capacitor. Refer to a reference schematic for this pin application.
TSTP	68	A	No Connect

TSTN	69	A	No Connect
COM_REF	75	A	Analog Equalizer Reference Voltage Node. It should be bypassed through a capacitor to ground. Refer to a reference schematic.
CVBS_IN	77	I	Composite video input. The input signal must be AC-coupled by 10uF ceramic capacitor.
COAX_IN	78	A	Coaxial RX Input.
VREF	80	A	VREF Input. This pin is voltage reference input for DAC. The input voltage should be 1.2V. Refer to a reference schematic for the pin application.
XTAL_IN	84	A	Crystal Clock Input (25MHz)
XTAL_OUT	85	A	Crystal Clock Output (25MHz)

Digital Pins

Name	Number	Type	Description
MDC	3	I/O	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 3.125MHz
MDIO	4	I/O	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC.
MII1IVAL	5	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Valid: Indicates the valid input data is presented on MII1B[3:0] signals, for transmission. It is synchronous to MII1TCLK.
MII1TXE	6	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Error. It is synchronous to MII1TCLK.
MII1IB0	7	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Data Bit[0]. It is synchronous to MII1TCLK.
MII1IB1	10	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Data Bit[1]. It is synchronous to MII1TCLK.
MII1IB2	11	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Data Bit[2]. It is synchronous to MII1TCLK.
MII1IB3	12	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Input Data Bit[3]. It is synchronous to MII1TCLK.
MII_RSTN	13	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. Reset Ethernet PHY, active low.
MII1OVAL	14	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Data Output Valid. It is synchronous to MII1RCLK.
MII1RXE	17	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Output Error. It is synchronous to MII1RCLK.
MII1OB0	18	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Output Data Bit[0]. It is synchronous to MII1RCLK.
MII1OB1	19	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Output Data Bit[1]. It is synchronous to MII1RCLK.

MII1OB2	20	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Output Data Bit[2]. It is synchronous to MII1RCLK.
MII1OB3	21	O	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Output Data Bit[3]. It is synchronous to MII1RCLK.
MII1TCLK	22	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Transmit Clock Input, 25MHz.
MII1RCLK	25	I	When MODE_S3=0, Ethernet PHY connect with SLOC by MII1. MII Receive Clock Input, 25MHz.
MII2TXE	26	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Error. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2IVAL	29	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Valid: Indicates the valid input data is presented on MII2B[3:0] signals, for transmission. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2IB0	30	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Data Bit[0]. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2IB1	31	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Data Bit[1]. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2IB2	32	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Data Bit[2]. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2IB3	33	I	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Input Data Bit[3]. It is synchronous to MII2TCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2RCLK	36	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Clock Input, 25MHz. When MODE_S3=0, this pin is not in use, connect to GND.
MII2TCLK	37	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Transmit Clock Input, 25MHz. When MODE_S3=0, this pin is not in use, connect to GND.
MII2RXE	38	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Output Error. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2OVAL	39	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Data Output Valid. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2OB0	40	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Output Data Bit[0]. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2OB1	41	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Output Data Bit[1]. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2OB2	44	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Output Data Bit[2]. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.
MII2OB3	45	O	When MODE_S3=1, SOC connect to SLOC by MII2. MII2 Receive Output Data Bit[3]. It is synchronous to MII2RCLK. When MODE_S3=0, this pin is not in use, connect to GND.

System & Control Pins

Name	Number	Type	Description
MODE_S0	88	I	SLOC Transmission Speed Selection
MODE_S1	91	I	{MODE_S1,MODE_S0} / Speed 00 / 36 Mbps 01 / 28 Mbps 10 / 25 Mbps 11 / 21 Mbps
MODE_S2	92	I	Connect to GND
MODE_S3	93	I	MII Interface Selection 0: Ethernet PHY connect with SLOC by MII1 data bus 1: SOC connect with SLOC by MII2 data bus
SDA	94	I/O	I2C Serial Data
SCLK	97	I	I2C Clock
HWRST	98	I	System Reset

Test Pins

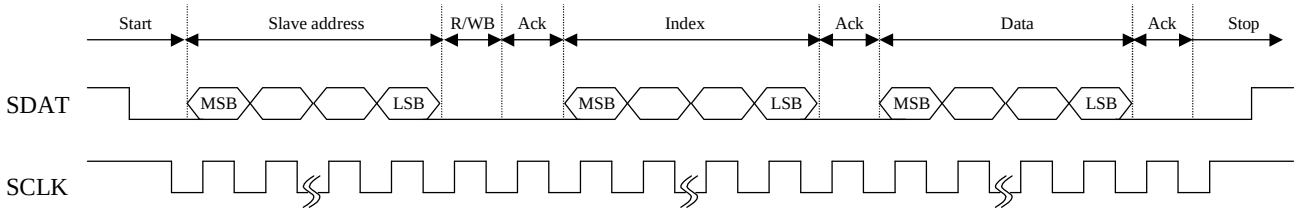
Name	Number	Type	Description
DEBUG_B14	46	I	Test Input, connect to GND for normal operation
DEBUG_B15	47	I	Test Input, connect to GND for normal operation
DEBUG_CLK	50	I/O	Test I/O, connect to GND for normal operation
DOUT_4	53	O	LED_0, indicates SLOC data link is connected
DOUT_5	54	O	LED_1, indicates MII Transmit Data is valid
DOUT_6	55	O	LED_2, indicates MII Receive Data is valid
DOUT_7	56	I/O	SLOC Chip ID Address 0
DOUT_8	57	I/O	SLOC Chip ID Address 1

Digital I/O Timing Characteristics

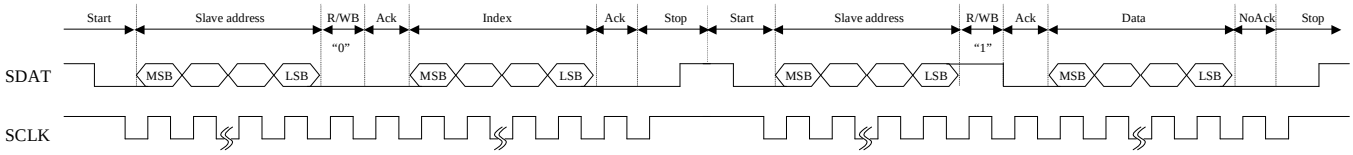
Serial Interface

The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW3801 register. The SCLK is the serial clock and SDA is the data line. Both lines are pulled high by the resistors connected to VDD. The DOUT_7 and DOUT_8 define the slave device address by tying the DOUT_7 and DOUT_8 pins either to VDD or GND.

{ DOUT_8,DOUT_7 } =	I2C Address =
2'b00	0x38
2'b01	0x3A
2'b10	0x3C
2'b11	0x3E

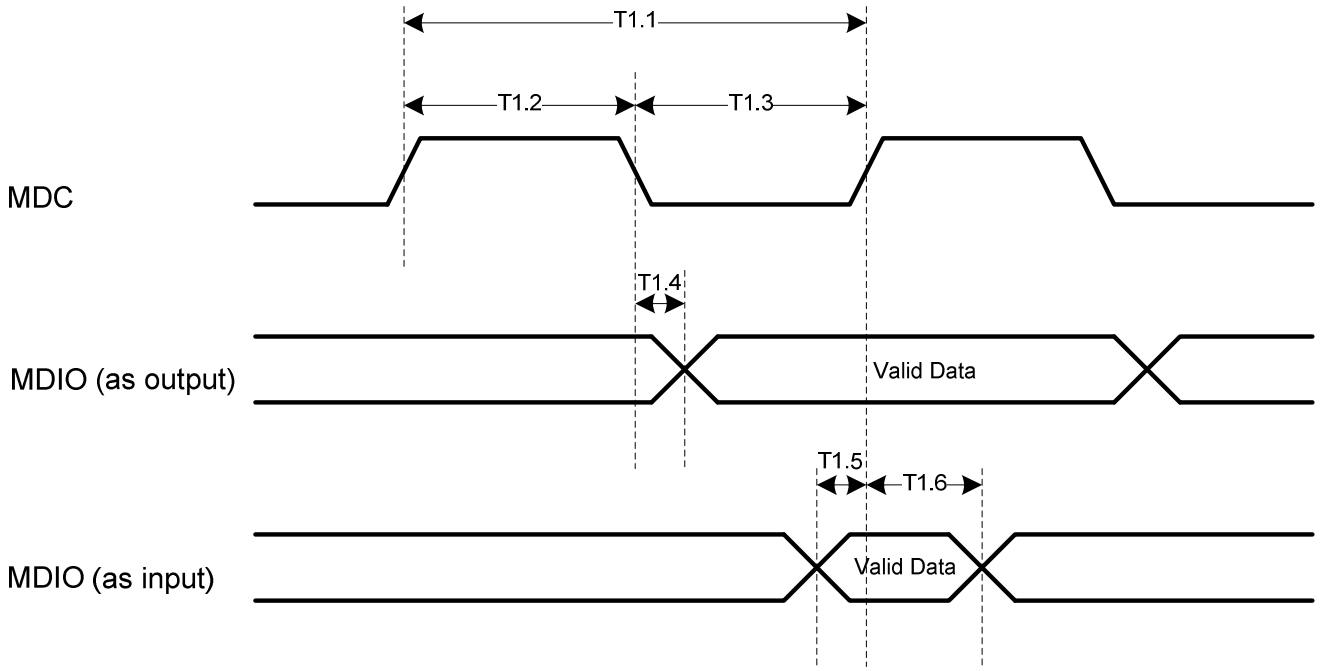


(a) Write Mode



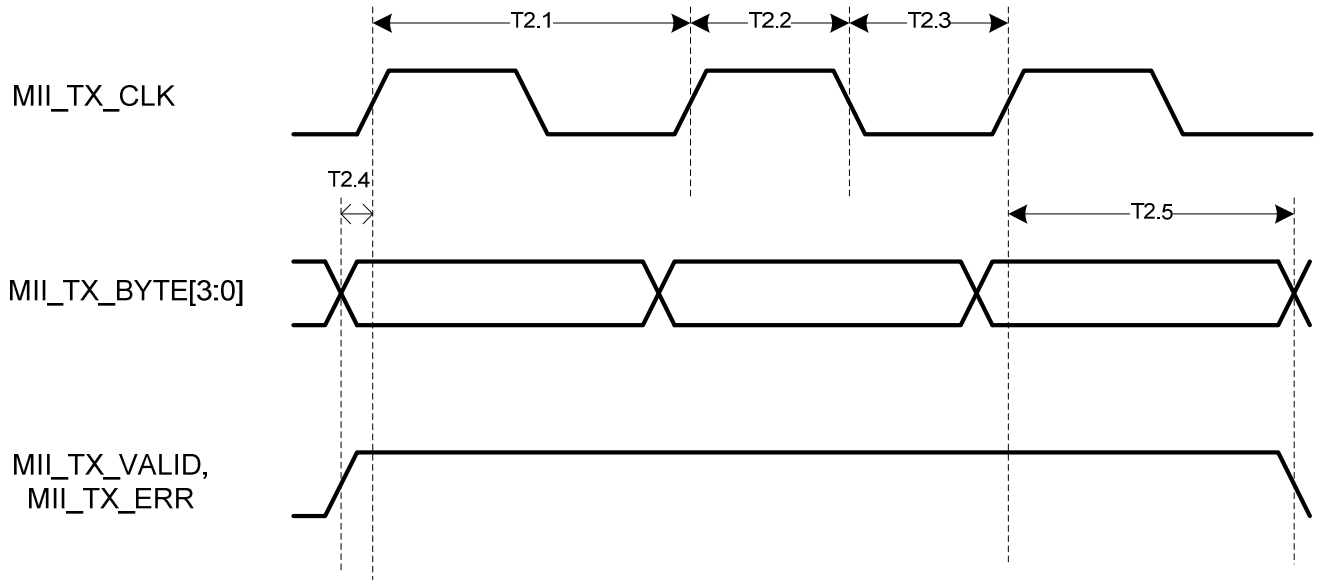
(b) Read Mode

Management Data I/O Timing

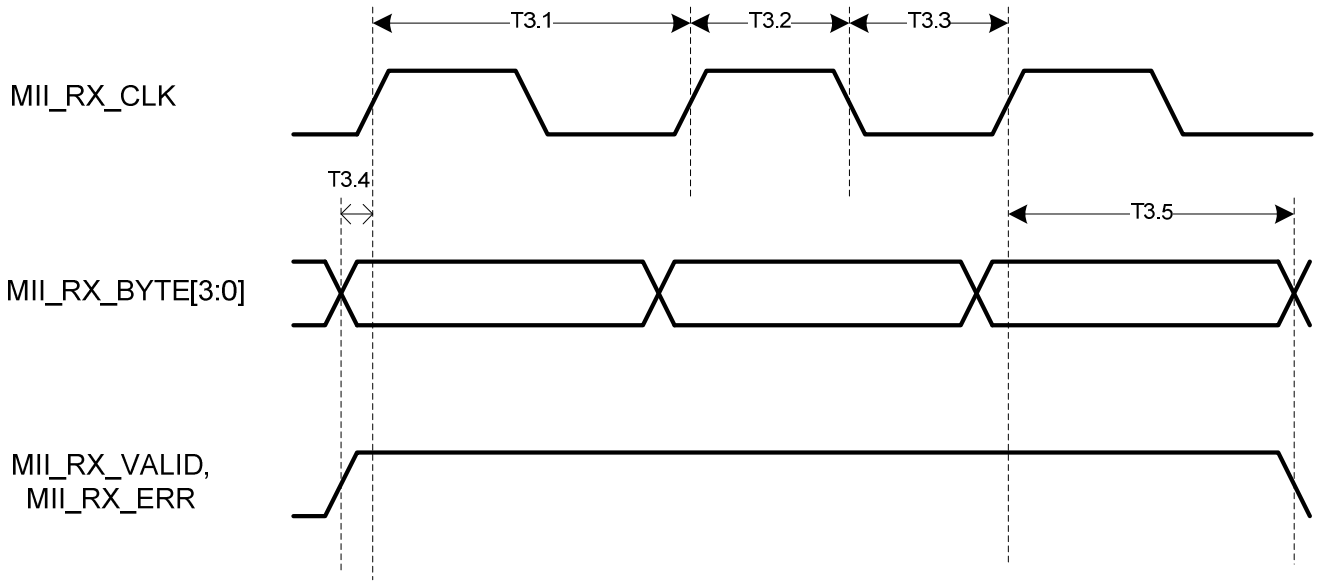


PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T1.1	MDC clock cycle time		320		ns
T1.2	MDC clock high time		160		ns
T1.3	MDC clock low time		160		ns
T1.4	MDC data output delay		-		ns
T1.5	MDC data input setup time		160		ns
T1.6	MDC data input hold time		160		ns

MII Timing



PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T2.1	TX_CLK clock cycle time	-	40	-	ns
T2.2	TX_CLK clock high time	-	20	-	ns
T2.3	TX_CLK clock low time	-	20	-	ns
T2.4	TX signals required setup to TX_CLK rising		25	-	ns
T2.5	TX signals required hold to TX_CLK rising		15	-	ns



PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T3.1	RX_CLK clock cycle time	-	40	-	ns
T3.2	RX_CLK clock high time	-	20	-	ns
T3.3	RX_CLK clock low time	-	20	-	ns
T3.4	RX signals required setup to RX_CLK rising		28	-	ns
T3.5	RX signals required hold to RX_CLK rising		10	-	ns

Device Control Registers

Control Register Table

<table>
<tr><th colspan="2">Address</th><th>Register Name</th><th>Description</th><th>Default</th></tr>
<tr><td>8’h00</td><td>Bit[0]</td><td>reg_chip_swrst</td><td>0: Normal operation
1: SLOC Reset, this bit will be self-clear by system</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[2:1]</td><td>Reserved</td><td>Reserved</td><td>2’b0</td></tr>
<tr><td></td><td>Bit[3]</td><td>reg_eqcr_filter_ctrl</td><td>CVBS Equalizer Filter Selection
0: Turn ON digital equalizer filter
1: Turn OFF digital equalizer filter</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[5:4]</td><td>Reserved</td><td>Reserved</td><td>2’b0</td></tr>
<tr><td></td><td>Bit[6]</td><td>reg_agc_ctrl</td><td>AGC Pre-gain control, need to set before turning on Receiver
0: Enable AGC pregain
1: Disable AGC pregain</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[7]</td><td>Reserved</td><td>Reserved</td><td>1’b0</td></tr>
<tr><td>8’h01</td><td>Bit[0]</td><td>reg_mode_overwrite</td><td>0: SLOC operates by system input pins
<table><tr><td>MODE_SEL[3]</td><td>= 1’b0</td><td>= 1’b1</td></tr><tr><td>MII Interface</td><td>EPHY-SLOC</td><td>SLOC-SOC</td></tr></table><table><tr><td>MODE_SEL[2]</td><td>=1’b0</td><td>=1’b1</td></tr><tr><td>Chip Function</td><td>TW3801</td><td>TW3811</td></tr></table>Transmission Speed<table><tr><td></td><td colspan="2">MODE_SEL[2]</td></tr><tr><td>MODE_SEL[1:0]</td><td>= 1’b0</td><td>= 1’b1</td></tr><tr><td>= 2’b00</td><td>36 Mbps</td><td>11 Mbps</td></tr><tr><td>= 2’b01</td><td>28 Mbps</td><td>9 Mbps</td></tr><tr><td>= 2’b10</td><td>25 Mbps</td><td>4 Mbps</td></tr><tr><td>= 2’b11</td><td>21 Mbps</td><td>3 Mbps</td></tr></table>1: Enable manual system control register. Need to program register:
0x01, bit[1]: reg_sloc_opmode
0x01, bit[4:3]: reg_mii_opmode
0x0A, bit[4:0]: reg_tx_speed</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[1]</td><td>reg_sloc_opmode</td><td>0: Chip operates as Camera(TW3801)
1: Chip operates as Monitor(TW3811)</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[2]</td><td>reg_loopback</td><td>Loopback DAC output data to ADC input
0: Disable
1: Enable</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[4:3]</td><td>reg_mii_opmode</td><td>Ethernet MAC MII interface selection
2’d0: EPHY-SLOC
2’d1: SOC-SLOC
2’d2: EPHY-SLOC-SOC</td><td>2’b0</td></tr>
<tr><td></td><td>Bit[7:5]</td><td>Reserved</td><td>Reserved</td><td>3’b0</td></tr>
<tr><td>8’h07</td><td>Bit[1:0]</td><td>Reserved</td><td>Reserved</td><td>2’b0</td></tr>
</table>

<table>
<tr><th colspan="2">Address</th><th>Register Name</th><th>Description</th><th>Default</th></tr>
<tr><td></td><td>Bit[2]</td><td>reg_revision_id</td><td>Chip Revision ID, the default value is different for A1 and B1/B2 Chip
0: SLOC B1/B2 Chip
1: SLOC A1 Chip</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[7:3]</td><td>Reserved</td><td>Reserved</td><td>5’b0</td></tr>
<tr><td>8’h0A</td><td>Bit[4:0]</td><td>reg_tx_speed</td><td>Programmable Transmission Throughput(Mbps) base on reg_sloc_opmode(0x01, bit[1])

reg_sloc_opmode = 1’b0 (TW3801)
<table>
<tr><td></td><td colspan="3">reg_tx_speed[4:3]=</td></tr>
<tr><td>reg_tx_speed[2:0]</td><td>2’b00</td><td>2’b01</td><td>2’10</td></tr>
<tr><td>= 3’b000</td><td>7</td><td>14</td><td>21</td></tr>
<tr><td>= 3’b001</td><td>9</td><td>19</td><td>28</td></tr>
<tr><td>= 3’b010</td><td>10</td><td>21</td><td>32</td></tr>
<tr><td>= 3’b011</td><td>11</td><td>23</td><td>36</td></tr>
<tr><td>= 3’b100</td><td>12</td><td>25</td><td>N/A</td></tr>
</table>
reg_sloc_opmode = 1’b1 (TW3811)
<table>
<tr><td></td><td colspan="3">reg_tx_speed[4:3]=</td></tr>
<tr><td>reg_tx_speed[2:0]</td><td>2’b00</td><td>2’b01</td><td>2’10</td></tr>
<tr><td>= 3’b000</td><td>2</td><td>4</td><td>6.5</td></tr>
<tr><td>= 3’b001</td><td>2.5</td><td>6</td><td>9</td></tr>
<tr><td>= 3’b010</td><td>3</td><td>6.5</td><td>10</td></tr>
<tr><td>= 3’b011</td><td>3.5</td><td>7</td><td>11</td></tr>
<tr><td>= 3’b100</td><td>4</td><td>7.5</td><td>N/A</td></tr>
</table></td><td>5’b0</td></tr>
<tr><td></td><td>Bit[7:5]</td><td>Reserved</td><td>Reserved</td><td>3’b0</td></tr>
<tr><td>8’h1E</td><td>Bit[0]</td><td>reg_mdio_rd</td><td>MDIO Register Read</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[1]</td><td>reg_mdio_wr</td><td>MDIO Register Write</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[6:2]</td><td>reg_mdio_phy_addr</td><td>MDIO PHY address</td><td>5’b0</td></tr>
<tr><td></td><td>Bit[7]</td><td>Reserved</td><td>Reserved</td><td>1’b0</td></tr>
<tr><td>8’h1F</td><td>Bit[4:0]</td><td>reg_mdio_reg_addr</td><td>MDIO Register R/W address</td><td>5’b0</td></tr>
<tr><td></td><td>Bit[7:5]</td><td>Reserved</td><td>Reserved</td><td>3’b0</td></tr>
<tr><td>8’h20</td><td>Bit[7:0]</td><td>reg_mdio_reg_wdata[7:0]</td><td>MDIO Register Write Data</td><td>8’h0</td></tr>
<tr><td>8’h21</td><td>Bit[7:0]</td><td>reg_mdio_reg_wdata[15:8]</td><td>MDIO Register Write Data</td><td>8’h0</td></tr>
<tr><td>8’h22</td><td>Bit[7:0]</td><td>reg_mdio_reg_rdata[7:0]</td><td>MDIO Register Read Data -Read Only</td><td>8’h0</td></tr>
<tr><td>8’h23</td><td>Bit[7:0]</td><td>reg_mdio_reg_rdata[15:8]</td><td>MDIO Register Read Data -Read Only</td><td>8’h0</td></tr>
<tr><td>8’h26</td><td>Bit[0]</td><td>reg_control_overwrite</td><td>0: Automatic system control
1: Manual system control by register setting. System idle waiting for bit[5:3] to be programmed</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[2:1]</td><td>Reserved</td><td>Reserved</td><td>2’b0</td></tr>
<tr><td></td><td>Bit[3]</td><td>reg_sloc_tx</td><td>0: Disable Transmitter
1:Turn on Transmitter</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[4]</td><td>reg_sloc_rx</td><td>0: Disable Receiver
1:Turn on Receiver</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[5]</td><td>reg_ephy_resetN</td><td>0: Disable Ethernet PHY
1: Turn on Ethernet PHY</td><td>1’b0</td></tr>
<tr><td></td><td>Bit[7:6]</td><td>Reserved</td><td>Reserved</td><td>2’b0</td></tr>
<tr><td>8’h27</td><td>Bit[7:0]</td><td>reg_rs_seg_num_ctrl</td><td>The number of segments to monitor error count at Reed-Solomon Decoder. Actual segment number is (reg_rs_seg_num_ctrl x 65536). After setting this register, check status register rs_err_cnt_rdy (0x43, bit[0]) for completion of error count.</td><td>8’h0</td></tr>
</table>

Address		Register Name	Description	Default
			0: Disable Reed-Solomon Error Count and will also reset rs_err_cnt_rdy(0x43 bit[0]) to 0	

Status Register Table – READ Only

Address		Register Name	Description	Default
8'h40	Bit[7:0]	rs_err_cnt_stat[7:0]	Reed-Solomon Decoder error segment count, value is valid when rs_err_cnt_rdy = 1'b1	8'hFF
8'h41	Bit[7:0]	rs_err_cnt_stat[15:8]	Reed-Solomon Decoder error segment count, value is valid when rs_err_cnt_rdy = 1'b1	8'hFF
8'h42	Bit[7:0]	rs_err_cnt_stat[23:16]	Reed-Solomon Decoder error segment count, value is valid when rs_err_cnt_rdy = 1'b1	8'hFF
8'h43	Bit[0]	rs_err_cnt_rdy	0: Reed-Solomon Error count is not ready 1: rs_err_cnt_stat[23:0] is updated. This signal can be reset by program reg_rs_seg_num_ctrl (0x27) to 8'b0	1'b0
	Bit[7:1]	*Reserved*	*Reserved*	*7'b0*
8'h44	*Bit[2:0]*	*Reserved*	*Reserved*	*3'b0*
	Bit[3]	ephy_linkup	0: Ethernet PHY connection is down 1: Ethernet PHY connection is up	1'b0
	Bit[4]	sloc_lock	0: The transmitted signal is not locked 1: The transmitted signal is detected and locked	1'b0
	Bit[5]	sloc_connect	0: SLOC connection is not established 1: SLOC connection is established	1'b0
	Bit[7:6]	*Reserved*	*Reserved*	*2'b0*

Electrical Information

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDD33	VDD_IO	-0.5	-	3.6	V
VDDA33	VDD_ADC,VDD_DRV,VDD_TVDR, VDD_A,VDD_DAC,VDD_PLL	-0.5	-	3.6	V
VDD18	VDD_D	-0.5	-	1.98	V
Digital Input/Output Voltage	-	-0.5	-	5.5	V
Analog Input Voltage	-	-0.5	-	3.6	V
Storage Temperature	T_S	-65	-	150	° C
Junction Temperature	T_J	0	-	125	° C
Reflow Soldering (10-30 Seconds)	T_{PEAK}	-	-	255-260	° C

Note1 : VSS_IO, VSS_D, VSS_ADC, VSS_DRV, VSS_TVDR, VSS_A, VSS_DAC, VSS_PLL all ground together

Note2: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VDD33 (measured to VSS_IO)	VDD_IO	3.15	3.3	3.6	V
VDDA33 (measured to VSS_ADC)	VDD_ADC,VDD_DRV,VDD_TVDR, VDD_A,VDD_DAC,VDD_PLL	3.15	3.3	3.6	V
VDD18 (measured to VSS_D)	VDD_D	1.62	1.8	1.98	V
Composite Video Input Range	CVBS_IN	0.5	1	1.4	V
Ambient Operating Temperature	T_A	-40		85	℃

AC/DC Electrical Parameters

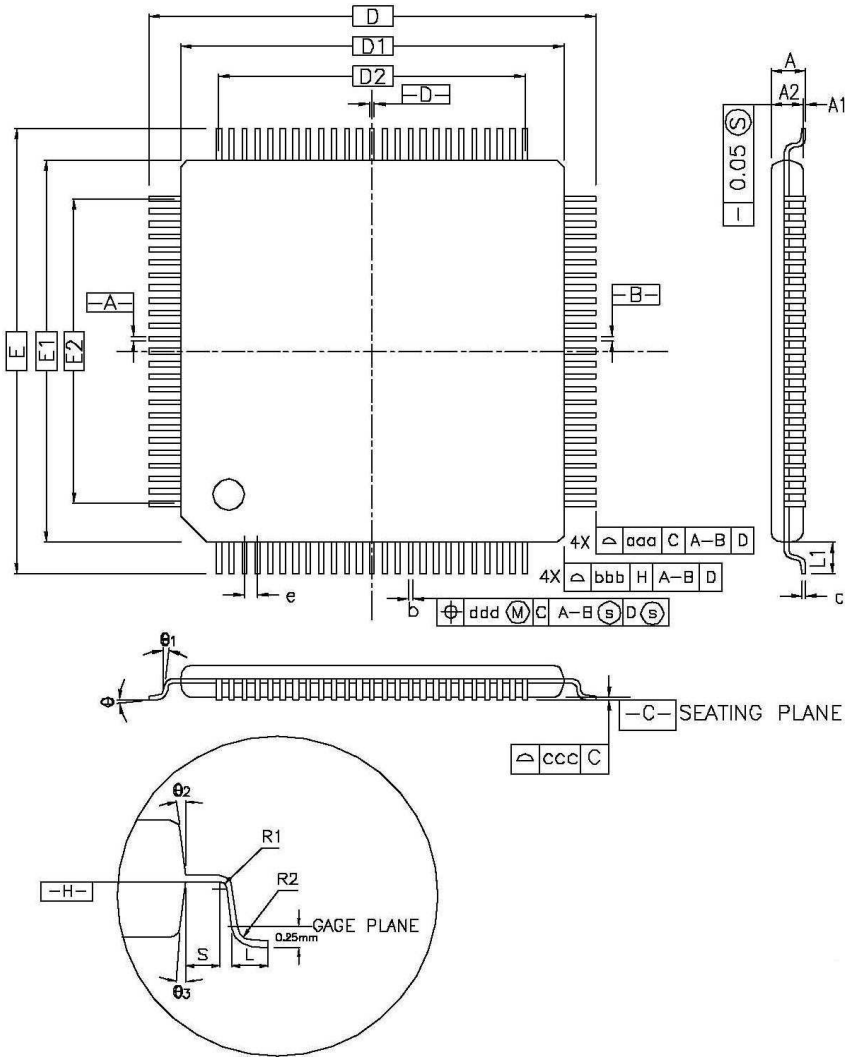
Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=3.3V or 0V)	I_L			±10	uA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
Output Capacitance	C_O		6		pF
Analog Pin input Voltage	Vi		1		Vpp
Analog Pin Input Capacitance	C_A		6		pF
Supply Current					
Analog Supply Current (VDDA33, 3.3V)	I_{DDA}		70		mA
Analog Drive Supply Current (VDD_DRV,3.3V)	I_{DDADR}		20		mA
Digital Internal Supply Current (VDD18, 1.8V)	I_{DDI}		198		mA
Digital I/O Supply Current (VDD33, 3.3V)	I_{DDO}		7.8		mA
Total Power Dissipation	P		679		mW

Crystal Characteristic

Parameter	Symbol	Min	Typ	Max	Units
Crystal spec					
nominal frequency (fundamental)		-	25	-	MHz
Deviation * * Crystal deviation is base on normal operation condition		-	-	±50	ppm
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
Oscillator Input					
nominal frequency		-	25	-	MHz
deviation		-	-	±50	ppm
duty cycle		-	-	55	%

Package Dimension

100-pin TQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
D	14.00 BSC.			0.551 BSC.		
D_1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E_1	12.00 BSC.			0.472 BSC.		
R_2	0.15	0.20	0.25	0.006	0.008	0.010
R_1	0.08	—	—	0.003	0.006	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

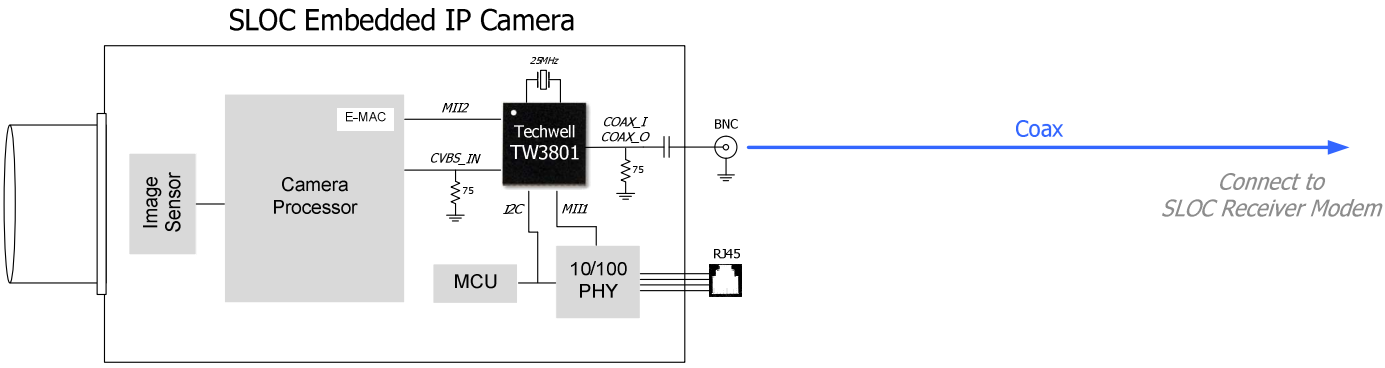
Package Dimension

100-pin TQFP Package Mechanical Drawing

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	9.60			0.378		
E2	9.60			0.378		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Typical Applications

1. Embedded Camera



2. Camera Adapter Module