

TW3801

Security Link Over Coax (SLOC) Transmitter

FN8283

Rev.1.00

November 29, 2012

SLOC™ (Security Link Over Coax) is a transmission protocol for simultaneously transmitting analog CVBS video and digital IP video over a single coaxial cable.

The TW3801 is the transmitting (“camera”) end of a SLOC link, combining Ethernet digital video data and analog CVBS video into a single SLOC signal that can be transmitted over 500m of coaxial cable. It can be embedded into a camera or configured as a stand-alone IP+CVBS-to-SLOC converter.

The TW3801 includes an AFE, digital modem, and two Ethernet MII/RMII interfaces. The device accepts an analog CVBS signal and an Ethernet (R)MII signal and encodes it into a SLOC signal.

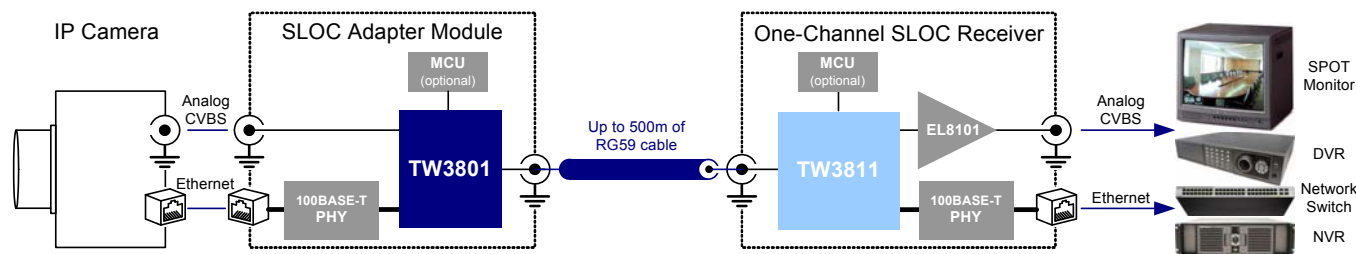
Applications

- Single-channel SLOC transmitter modem
- Embedded SLOC camera modem

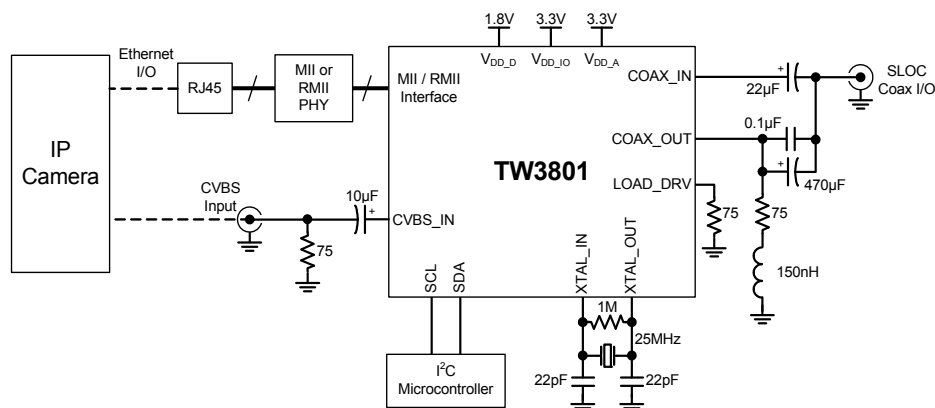
Features

- Simultaneous transmission of IP video data and analog CVBS video over up to 500m of RG59 coaxial cable
- Analog CVBS video preview support
- Proprietary adaptive analog equalizer for extending the reach of CVBS video
- Proprietary SLOC-based IP DVR detection
- Creates a full-duplex 100BASE-T digital link
- 36Mbps downlink speed from TW3801 to TW3811
- 4Mbps uplink for SLOC compliance
- Ethernet MAC MII/RMII interface for interfacing to Camera ISPs
- Ethernet PHY MII/RMII interface for interfacing to Ethernet PHY chip
- I²C 2-wire control interface
- Integrated PLL with 25MHz crystal interface
- 1.8V, 3.3V supplies
- 100-TQFP (12mmx12mm) Package

Application Block Diagram



Simplified Application Schematic



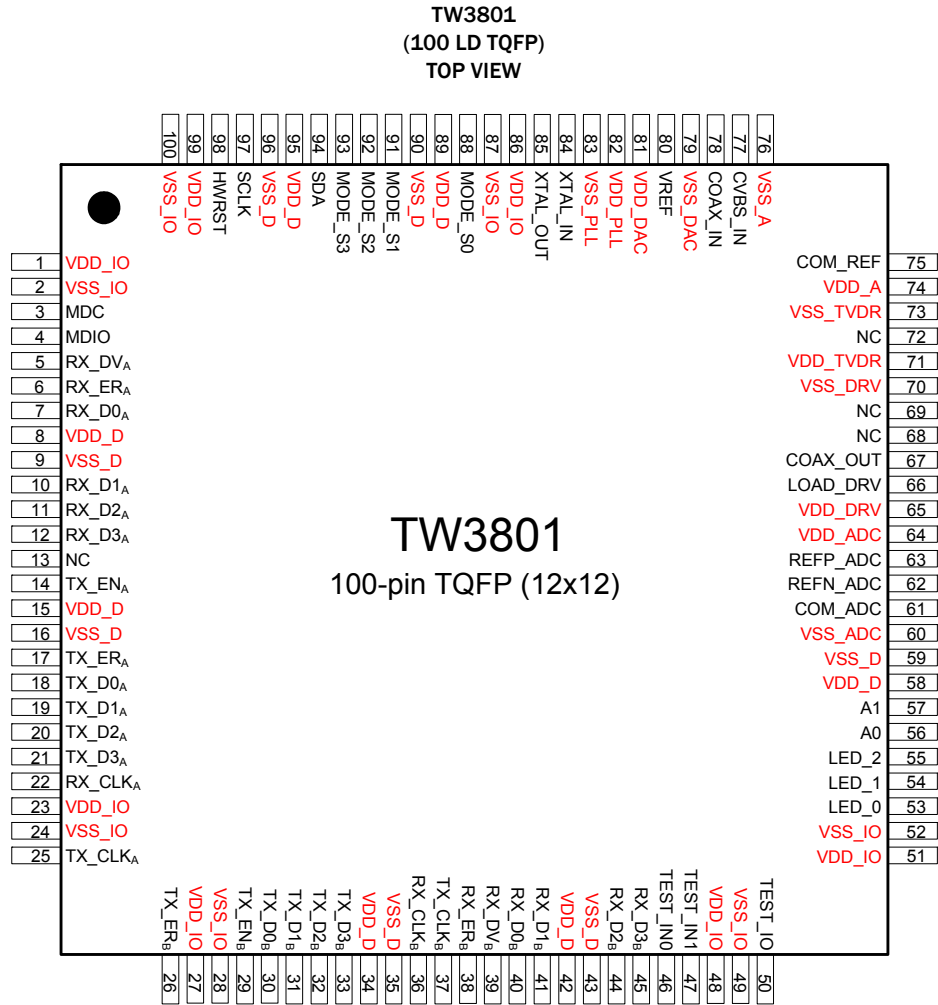
Ordering Information

| PART NUMBER | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|-------------------------------|------------------|-----------------|-------------------|-------------|
| TW3801-TC1-CR (Notes 1, 2, 3) | TW3801 TC1-CR | -40 to +85 | 100 Ld TQFP | Q100.12X12A |
| TW3801-TC1-CR-EVAL | Evaluation Board | | | |

NOTES:

1. Add "T" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL please see tech brief [TB363](#).

Pin Configuration



Pin Descriptions

| SYMBOL | NUMBER | DESCRIPTION |
|--------------------------------|----------------------------|--|
| POWER SUPPLY AND GROUND | | |
| VDD_IO | 1, 23, 27, 48, 51, 86, 99 | 3.3V Power supply for all digital I/Os. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass each supply pin to ground plane with a 0.1 μ F capacitor. |
| VSS_IO | 2, 24, 28, 49, 52, 87, 100 | Digital I/O Ground. Connect each pin to ground plane using the shortest/lowest inductance path possible. |
| VDD_D | 8, 15, 34, 42, 58, 89, 95 | 1.8V Power supply for core digital logic. Connect to the 1.8V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass each supply pin to ground plane with a 0.1 μ F capacitor. |
| VSS_D | 9, 16, 35, 43, 59, 90, 96 | Digital Core Ground. Connect each pin to ground plane using the shortest/lowest inductance path possible. |
| VDD_ADC | 64 | 3.3V Power supply for internal ADC. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass to ground plane with a 0.1 μ F capacitor. |
| VSS_ADC | 60 | ADC Analog Ground. Connect to ground plane using the shortest/lowest inductance path possible. |
| VDD_DRV | 65 | 3.3V Power supply for analog output stages. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass to ground plane with a 0.1 μ F capacitor. |
| VSS_DRV | 70 | Analog Output Driver Ground. Connect to ground plane using the shortest/lowest inductance path possible. |
| VDD_A | 71, 74 | 3.3V Power supply for internal analog. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass each pin to ground plane with a 0.1 μ F capacitor. |
| VSS_A | 73, 76 | Analog Ground. Connect each pin to ground plane using the shortest/lowest inductance path possible. |
| VDD_DAC | 81 | 3.3V Power supply for DAC. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass to ground plane with a 0.1 μ F capacitor. |
| VSS_DAC | 79 | DAC Analog Ground. Connect to ground plane using the shortest/lowest inductance path possible. |
| VDD_PLL | 82 | 3.3V Power supply for PLL. Connect to the 3.3V supply through a MI0805K601R-10 (or equivalent) ferrite bead and bypass to ground plane with a 0.1 μ F capacitor. |
| VSS_PLL | 83 | PLL Analog Ground. Connect to ground plane using the shortest/lowest inductance path possible. |
| ANALOG | | |
| ADC_COM | 61 | Analog Output. Internally Generated ADC Reference Voltage. Common mode reference voltage for ADC. Bypass to ground plane with a 0.1 μ F capacitor. |
| ADC_REFN | 62 | Analog Output. Internally Generated ADC Reference Voltage. Negative differential reference voltage for ADC. Bypass to ground plane with a 0.1 μ F capacitor. |
| ADC_REFP | 63 | Analog Output. Internally Generated ADC Reference Voltage. Positive differential reference voltage for ADC. Bypass to ground plane with a 0.1 μ F capacitor. |
| LOAD_DRV | 66 | Analog Output. Driver Reference Load. The signal on this pin generates the output current that is mirrored onto the COAX_OUT pin. Connect to a 75 Ω , 1% resistor to ground. To maximize stability, ensure that this signal is isolated from the COAX_OUT signal. This can be achieved by placing the resistor on the bottom side of PCB and routing the trace in the opposite direction from the COAX_OUT trace. |
| COAX_OUT | 67 | Analog Output. Coaxial TX Output. This pin is a high impedance current source output. Terminate to VSS_A with a 75 Ω 1% resistor in series with a 150nH inductor. AC-couple per Figure 1 to SLOC I/O connector. |
| COM_REF | 75 | Analog Output. Internally Generated Reference Voltage. Bypass to ground plane with a 0.1 μ F capacitor. |
| CVBS_IN | 77 | Analog Input. Standard 1V _{pp} CVBS video signal from camera or other source. |
| COAX_IN | 78 | Analog Input. Coaxial RX Input. |
| VREF | 80 | Analog Input. Externally Generated Reference Voltage. Voltage reference input for internal DAC. Connect to a 1.2VDC source. This voltage can be generated from AVD_DAC with a 6.34k/3.65k resistor divider and 0.1 μ F bypass capacitor. Refer to reference schematic for more details. |

Pin Descriptions (Continued)

| SYMBOL | NUMBER | DESCRIPTION |
|--|--------|---|
| XTAL_IN | 84 | Analog Input. Crystal Input. Connect to one end of a 25MHz crystal with 22pF capacitor and 1MΩ feedback resistor. Refer to reference schematic for more details. |
| XTAL_OUT | 85 | Analog Output. Crystal Output. Connect to other end of a 25MHz crystal with 22pF capacitor and 1MΩ feedback resistor. Refer to reference schematic for more details. |
| MII/RMII DIGITAL INTERFACE | | |
| MDC | 3 | Digital Output. MDC is the management data clock reference for the serial management interface. The maximum frequency supported is 3.125MHz. |
| MDIO | 4 | Digital I/O. MDIO is the management data. MDIO transfers data synchronously with MDC. |
| The following pins are used to connect TW3801 to an external Ethernet PHY using the A Interface pins, when MODE_S3 = 0. | | |
| RX_DV _A | 5 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Data Valid. 0: The incoming data on the RX_Dn _A is not ready to be latched. 1: The incoming data on the RX_Dn _A pins is valid and should be latched using RX_CLK _A . |
| RX_ER _A | 6 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Error. 0: The incoming data on the RX_Dn _A pins is valid. 1: The incoming data on the RX_Dn _A pins has an error. |
| RX_D0 _A | 7 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Data bit 0. |
| RX_D1 _A | 10 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Data bit 1. |
| RX_D2 _A | 11 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Data bit 2. (MII mode only) |
| RX_D3 _A | 12 | Digital Input with internal 57k pull-down resistor to VSS_IO. Receive Data bit 3. (MII mode only) |
| TX_EN _A | 14 | Digital Output. Transmit Enable. 0: Data on the TX_Dn _A pins is not ready. 1: Data on the TX_Dn _A pins is valid and should be latched using TX_CLK _A . |
| TX_ER _A | 17 | Digital Output. Transmit Error This pin is normally low. When in "Passthrough Mode", this pin duplicates the state of TX_ER _B . |
| TX_D0 _A | 18 | Digital Output. Transmit Data bit 0. |
| TX_D1 _A | 19 | Digital Output. Transmit Data bit 1. |
| TX_D2 _A | 20 | Digital Output. Transmit Data bit 2. (MII mode only) |
| TX_D3 _A | 21 | Digital Output. Transmit Data bit 3. (MII mode only) |
| RX_CLK _A | 22 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Receive Data Clock signal. |
| TX_CLK _A | 25 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Data Clock signal. MII: 25MHz. RMII: 50MHz. |
| The following pins are used to connect TW3801 to an external MAC/SoC using the B Interface pins, when MODE_S3 = 1. | | |
| TX_ER _B | 26 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Receive Error. This bit is synchronous to TX_CLK _B . 0: The incoming data on the TX_Dn _B pins is valid. 1: The incoming data on the TX_Dn _B pins has an error. |
| TX_EN _B | 29 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Enable. 0: Data on the TX_Dn _B pins is not ready. 1: Data on the TX_Dn _B pins is valid and should be latched using TX_CLK _B . |
| TX_D0 _B | 30 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Data bit 0. |
| TX_D1 _B | 31 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Data bit 1. |
| TX_D2 _B | 32 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Data bit 2. (MII mode only) |
| TX_D3 _B | 33 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Transmit Data bit 3. (MII mode only) |
| RX_CLK _B | 36 | Digital Output. Receive Data Clock signal. |
| TX_CLK _B | 37 | Digital Output. Transmit Data Clock signal. |
| RX_ER _B | 38 | Digital Output. Receiver Error. This pin is normally low. When in "Passthrough Mode", this pin duplicates the state of RX_ER _A . |

Pin Descriptions (Continued)

| SYMBOL | NUMBER | DESCRIPTION |
|--------------------------------|-----------------------|---|
| RX_DV _B | 39 | Digital Output. Receive Data Valid. 0: The data on the RX_Dn _B is not ready to be latched. 1: The data on the RX_Dn _B pins is valid and should be latched using RX_CLK _B . |
| RX_D0 _B | 40 | Digital Output. Receive Data bit 0. |
| RX_D1 _B | 41 | Digital Output. Receive Data bit 1. |
| RX_D2 _B | 44 | Digital Output. Receive Data bit 2. (MII mode only) |
| RX_D3 _B | 45 | Digital Output. Receive Data bit 3. (MII mode only) |
| MISCELLANEOUS | | |
| MODE_S0 | 88 | Digital Inputs. TW3801 Transmission Speed Selection. Status latched at power-on/reset. Only valid if register 0x01[0] = 0. If register 0x01[0] = 1, Transmission Speed is set by register 0x0A. |
| MODE_S1 | 91 | MODE_S1 = 0, MODE_S0 = 0: 36Mbps MODE_S1 = 0, MODE_S0 = 1: 28Mbps MODE_S1 = 1, MODE_S0 = 0: 25Mbps MODE_S1 = 1, MODE_S0 = 1: 21Mbps Note: This bitrate should always be set to 36Mbps for maximum compatibility with all cameras. A lower bitrate will increase the chances of a buffer overflow without significantly increasing cable connection distance |
| MODE_S2 | 92 | Digital Input. Tie to GND. |
| MODE_S3 | 93 | Digital Input. MII Interface Selection. Status latched on reset/power-on. Only valid if register 0x01[0] = 0. If register 0x01[0] = 1, Interface Mode is set by register 0x01. 0: Ethernet PHY connect with SLOC by MII _A data bus. 1: SOC connect with SLOC by MII _B data bus. |
| LED_0 / MII_Mode_ Select | 53 | Digital I/O with internal 57kΩ pull-up resistor to VDD_IO (active low). As an output during normal operation, a low output on LED_0 indicates the SLOC data link is connected. If register 0x01[0] = 0, the state of this pin is latched at power-on/reset to set MII or RMII operation. If register 0x01[0] = 1, MII or RMII operation is determined by register 0x01[5]. >2.0V: MII mode (default if pin is floating) <0.8V: RMII mode (10kΩ pull-down resistor or equivalent) |
| LED_1 | 54 | Digital I/O with internal 57kΩ pull-up resistor to VDD_IO (active low). A low output on LED_1 indicates MII Transmit Data is valid. For correct TW3801 operation, this pin must be left floating or be held to a voltage >2.0V during power on/reset. |
| LED_2 | 55 | Digital I/O with internal 57kΩ pull-up resistor to VDD_IO (active low). A low output on LED_2, indicates MII Receive Data is valid. For correct TW3801 operation, this pin must be left floating or be held to a voltage >2.0V during power on/reset. |
| SDA | 94 | Digital I/O with open-drain. I ² C Serial Data. |
| SCLK | 97 | Digital Input. I ² C Clock. |
| A0 | 56 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. TW3801 I ² C Address Bit 0. |
| A1 | 57 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. TW3801 I ² C Address Bit 1. |
| HWRST | 98 | Digital I/O with internal 57kΩ pull-up resistor to VDD_IO (active low). Active LOW system reset. To reset the TW3801, hold low (<0.8V) for at least 12 cycles of the 25MHz crystal clock after the oscillator has stabilized (crystal oscillator may take up to 1ms to start up and stabilize after power is applied). |
| TEST_IN0, TEST_IN1 | 46, 47 | Digital Input with internal 57kΩ pull-down resistor to VSS_IO. Do not connect anything to this pin. |
| TEST_IO | 50 | Digital I/O with internal 57kΩ pull-down resistor to VDD_IO. Do not connect anything to this pin. |
| NC | 13, 68, 69, 72, 77 | Do Not Connect. Do not connect anything to these pins. |

Absolute Maximum Ratings

| | |
|--|---------------|
| VDD_D Digital Core Supply Voltage Range | -0.5V to 2.4V |
| VDD_IO Digital I/O Supply Voltage Range | -0.5V to 4.3V |
| VDD_A=VDD_ADC=VDD_DRV=VDD_TVDR=VDD_DAC=VDD_PLL | |
| Analog Supply Voltage Range | -0.5V to 4.3V |
| Voltage on Digital I/O Pins | -0.5V to 5.5V |
| Voltage on Analog I/O Pins | -0.5V to 4.3V |
| ESD Rating | |
| Human Body Model (Tested per JESD22-A114E) | 2kV |
| Machine Model (Tested per JESD22-A115-A) | 200V |
| CDM Model (Tested per JESD22-C101) | 750V |
| Latch Up (Tested per JESD-78B; Class 2, Level A) | ±100mA |

Thermal Information

| | | |
|---|---------------------------|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 100 Ld TQFP Package (Notes 4, 5) | 41 | 7 |
| Maximum Junction Temperature (Plastic Package) | +125°C | |
| Storage Temperature Range | -65°C to +150°C | |
| Pb-Free Reflow Profile | see link below | |
| http://www.intersil.com/pbfree/Pb-FreeReflow.asp | | |
| Pb-Free Reflow Profile (*) | see TB487 | |
| *Peak temperature during solder reflow | +235°C max | |

Recommended Operating Conditions

| | |
|--|----------------|
| Temperature | -40°C to +85°C |
| VDD_D Digital Supply Voltage | 1.6V to 2.0V |
| VDD_IO Digital Supply Voltage | 3.0V to 3.6V |
| VDD_ADC=VDD_DRV=VDD_TVDR=VDD_A=VDD_DAC | |
| =VDD_PLL Analog Supply Voltage | 3.0V to 3.6V |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the “case temp” location is taken at the package top center.

Electrical Specifications VDD_D = 1.8V, VDD_I/O = 3.3V, VDD_ADC = VDD_DRV = VDD_TVDR = VDD_A = VDD_DAC = VDD_PLL = 3.3V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.** (Note 6)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|--|--|-----|------|-----|------------------|
| POWER SUPPLY | | | | | | |
| VDD_D | Digital Core Supply Voltage Range | | 1.6 | 1.8 | 2.0 | V |
| IDD_D | VDD_D Supply Current | | | 160 | | mA |
| VDD_IO | Digital I/O Supply Voltage Range | | 3.0 | 3.3 | 3.6 | V |
| IDD_IO | VDD_IO Supply Current | | | 7 | | mA |
| VDD_A | Analog Supply Voltage Range | | 3.0 | 3.3 | 3.6 | V |
| IDD_A | VDD_A Supply Current | | | 135 | | mA |
| PD | Total Power Dissipation | | | 760 | | mW |
| COAX I/O | | | | | | |
| | COAX_IN Input Capacitance | | | 9 | | pF |
| VCXO | COAX_OUT Output Level | RL = 37.5Ω, 15 - 24MHz, transmitting IP Data and CVBS | | 0.5 | | V _{P-P} |
| | Return Loss | RL = 75Ω, 6 - 42MHz | | -10 | | dB |
| CVBS OUTPUT | | | | | | |
| Vin | Video Input Range | 100IRE White Pattern; AC-coupled to CVBS_IN | | 1 | 1.2 | V _{pp} |
| | Luminance Non-Linearity | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, 5 step pattern, VOUT = TW3811 CVBS_OUT | | 5 | | % |
| | Chroma Non-Linear Gain Distortion (reference for 40IRE) | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, Modulated pedestal signal, VOUT = TW3811 CVBS_OUT | | -1.8 | | % |
| | Chroma Non-Linear Phase Distortion (Reference for 40IRE) | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, Modulated pedestal signal, VOUT = TW3811 CVBS_OUT | | -2 | | ° |

Electrical Specifications VDD_D = 1.8V, VDD_I/O = 3.3V, VDD_ADC = VDD_DRV = VDD_TVDR = VDD_A = VDD_DAC = VDD_PLL = 3.3V, T_A = +25 °C. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C.** (Note 6) (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|--|------|------|-----|-------|
| DG | Differential Gain | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, Modulated ramp, VOUT = TW3811 CVBS_OUT | | 4 | | % |
| DP | Differential Phase | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, Modulated ramp, VOUT = TW3811 CVBS_OUT | | -0.6 | | ° |
| BW | Video Bandwidth (-3dB) | 1M COAX, IP data on, VIN = TW3801 CVBS_IN, VOUT = TW3811 CVBS_OUT | | 5.4 | | MHz |
| SNR | Video Signal-To-Noise Ratio | 1M COAX, IP data on, Unweighted filter, VIN = TW3801, 100IRE White pattern, VOUT = TW3811 CVBS_OUT | | 52.5 | | dB |
| DIGITAL I/O | | | | | | |
| DIGITAL INPUTS | | | | | | |
| VIH | Input High Voltage (TTL) | | 2.0 | | 5.5 | V |
| VIL | Input Low Voltage (TTL) | | -0.3 | | 0.8 | V |
| IL | Input Leakage Current (Inputs Without Pull-up Or Pull-down Resistors) | VIN = 3.3V and 0V | | | ±10 | μA |
| CIN | Input Capacitance | | | 6 | | pF |
| DIGITAL OUTPUTS | | | | | | |
| VOH | Output High Voltage | | 2.4 | | | V |
| VOL | Output Low Voltage | | | | 0.4 | V |
| EXTERNAL CRYSTAL/REFERENCE CLOCK REQUIREMENTS (per MII/RMII standard) | | | | | | |
| f _{XTAL} | External Crystal/Clock Frequency | | | 25 | | MHz |
| XTALTOL | External Crystal/Clock Tolerance | | | | ±50 | ppm |

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Register Listing

| ADDRESS | REGISTER (DEFAULT VALUE) | BIT(S) | FUNCTION NAME | DESCRIPTION |
|---------|-----------------------------------|--------|---------------------|--|
| 0x00 | Reset and Device ID (0x80) | 0 | Soft Reset | Soft chip reset. Write a 1 to reset. Will set itself to 0 when reset is complete. Does not reset register settings. |
| | | 4:1 | Reserved | Set to 0 when writing this register. |
| | | 7:5 | Revision ID | 100: C1 Revision |
| 0x01 | SLOC Configuration (0x60) | 0 | Config Source | 0: Configuration determined by external pins (default). 1: Configuration determined by registers 0x01 and 0x0A. |
| | | 1 | Operational Mode | 0: Transmitter (TW3801) (default) 1: Receiver (TW3811) |
| | | 2 | Reserved | Set to 0 when writing this register. |
| | | 4:3 | I/O Configuration | 00: MII _A bus enabled. TW3801 acts like a MAC and is connected to a PHY (default). 01: MII _B bus enabled. TW3801 acts like a PHY and is connected to a MAC. 02: Both MII _A and MII _B buses are connected together (passthrough mode) (experimental). 03: Reserved |
| | | 5 | Interface Selection | 0: RMII 1: MII (default) |
| | | 6 | RMII Clock Source | 0: An internally-generated 50MHz RMII reference clock is available on the TEST_IO pin. 1: An externally-supplied 50MHz RMII reference clock must be supplied to TX_CLK _A pin for RMII operation (default). |
| | | 7 | Reserved | Set to 0 when writing this register. |
| 0x0A | Transmit Link Datarate (0x00) | 4:0 | Tx Link Datarate | When 0x01[0] = 0, the transmit datarate is determined by the MODE_S0 and MODE_S1 pins. When 0x01[0]=1, this register sets the bitrate of data transmitted from the TW3801 to the TW3811. This bitrate should always be set to 36Mbps for maximum compatibility with all cameras. A lower bitrate will increase the chances of a buffer overflow without significantly increasing cable connection distance. The speed selection choices below are shown for historical continuity. Use 0x13 for all new designs. 0x0C: 25Mbps 0x0A: 21Mbps 0x11: 28Mbps 0x13: 36Mbps 0x00 - 0x0B, 0x10, 0x12, 0x14-0x1F: Reserved |
| | | 7:5 | Reserved | Set to 0 when writing this register. |
| 0x14 | Receive Link Datarate (Read Only) | 4:0 | Rx Link Datarate | When a SLOC link is established, this register indicates the bit rate of the data from the TW3811 to the TW3801. 0x02: 3Mbps 0x04: 4Mbps 0x11: 9Mbps 0x13: 11Mbps |
| | | 7:5 | Reserved | |
| 0x19 | CVBS Channel Gain (0x00) | 6:0 | CVBS Gain | 0x00: Minimum CVBS Gain (default) 0x7F: Maximum CVBS Gain |
| | | 7 | Reserved | Set to 0 when writing this register. |

Register Listing (Continued)

| ADDRESS | REGISTER (DEFAULT VALUE) | BIT(S) | FUNCTION NAME | DESCRIPTION |
|---------|---|--------|---------------------------|--|
| 0x1E | MDIO 1 (0x00) | 0 | MDIO Register Read | MDIO register read command. Specify MDIO register address in 0x1F, apply read command (set this bit), clear read command (clear this bit), then read MDIO register value in registers 0x22 and 0x23. |
| | | 1 | MDIO Register Write | MDIO register write command. Specify MDIO register address in 0x1F, write MDIO register data into registers 0x20 and 0x21, apply write command (set this bit), then clear write command (clear this bit). |
| | | 3:2 | Reserved | Set to 0 when writing this register. |
| | | 6:4 | MDIO PHY Address | These are the 3 MSB bits of MDIO PHY address that SLOC needs to match with Ethernet-PHY chip's PHY address. The 2 lower LSB = {A1,A0}, where A1 and A0 are set by the logic levels of the external A1 and A0 pins. |
| | | 7 | Reserved | Set to 0 when writing this register. |
| 0x1F | MDIO 2 (0x00) | 4:0 | MDIO Register R/W Address | |
| | | 7:5 | Reserved | Set to 0 when writing this register. |
| 0x20 | MDIO OUT DATA LSB (0x00) | 7:0 | MDIO OUT (LSB) | Lower 8 bits of 16 bit word to be transmitted. |
| 0x21 | MDIO OUT DATA MSB (0x00) | 7:0 | MDIO OUT (MSB) | Upper 8 bits of 16 bit word to be transmitted. |
| 0x22 | MDIO IN DATA LSB (Read Only) | 7:0 | MDIO IN (LSB) | Lower 8 bits of 16 bit word received. |
| 0x23 | MDIO IN DATA MSB (Read Only) | 7:0 | MDIO IN (MSB) | Upper 8 bits of 16 bit word received. |
| 0x26 | SLOC Control (0x00) | 0 | Control Overwrite | 0: Automatic System Control. SLOC Tx and Rx automatically enabled if "Ethernet PHY Connected" bit is set (44[3] = 1). 1: Manual System Control. SLOC Tx and Rx enabled based on bits 3 and 4 of this register. |
| | | 2:1 | Reserved | Set to 11b when writing this register. |
| | | 3 | SLOC Transmitter Enable | 0: Disabled. 1: Enabled. |
| | | 4 | SLOC Receiver Enable | 0: Disabled. 1: Enabled. |
| | | 7:5 | Reserved | Set to 0 when writing this register. |
| 0x27 | Reed-Solomon Segment Monitor Count (0x00) | 7:0 | Reed-Solomon Segments | The number of segments to monitor error count at Reed-Solomon Decoder. Actual segment number is 65536 x [the value in this register]. After setting this register, check status bit Error Count Updated (0x43, bit[0]) for completion of error count. A value of 0 in this register will disable the Reed-Solomon Error Counter and reset Error Count Updated (0x43 bit[0]) to 0. |
| 0x40 | Reed-Solomon Error Count 7:0 (Read Only, default is 0xFF) | 7:0 | Error Count 7:0 | Bits 7:0 of the 24-bit Reed-Solomon Error Count. Registers 0x40 - 0x42 = 0FFFFFFF whenever 0x43[0] = 0. |
| 0x41 | Reed-Solomon Error Count 15:8 (Read Only, default is 0xFF) | 7:0 | Error Count 15:8 | Bits 15:8 of the 24-bit Reed-Solomon Error Count. Registers 0x40 - 0x42 = 0FFFFFFF whenever 0x43[0] = 0. |
| 0x42 | Reed-Solomon Error Count 23:16 (Read Only, default is 0xFF) | 7:0 | Error Count 23:16 | Bits 23:16 of the 24-bit Reed-Solomon Error Count. Registers 0x40 - 0x42 = 0FFFFFFF whenever 0x43[0] = 0. |
| 0x43 | Reed-Solomon Error Count Updated (Read Only, default is 0x00) | 0 | Error Count Updated | 0: Reed-Solomon Error Count is not valid. 1: Reed-Solomon Error Count value has been updated. To clear this bit, write a 0 to register 0x27. |
| | | 7:1 | Reserved | |

Register Listing (Continued)

| ADDRESS | REGISTER (DEFAULT VALUE) | BIT(S) | FUNCTION NAME | DESCRIPTION |
|---------|--------------------------|--------|------------------------|---|
| 0x44 | Status Bits (Read Only) | 2:0 | Reserved | |
| | | 3 | Ethernet PHY Connected | 0: Ethernet PHY reporting no link. 1: Ethernet PHY reporting link established. |
| | | 4 | SLOC Rx Locked | 0: SLOC carrier not detected. 1: SLOC carrier detected and locked. |
| | | 5 | SLOC Data Active | 0: SLOC data link not established. 1: SLOC data link established. |
| | | 7:6 | Reserved | |

Functional Description

Functional Overview

The TW3801 block diagram is shown in Figure 1.

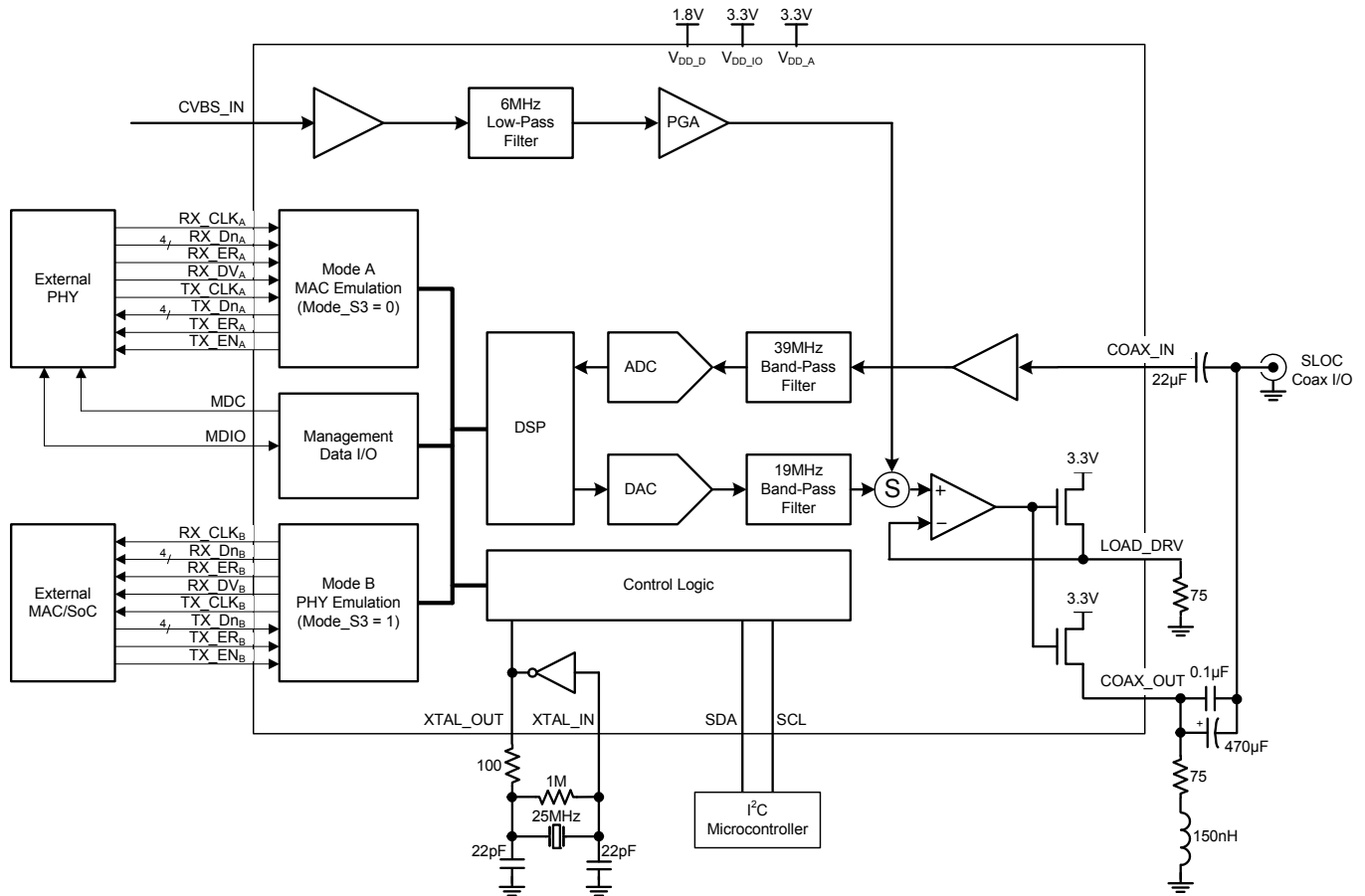


FIGURE 1. TW3801 INTERNAL BLOCK DIAGRAM

Applications Information

External Interfacing

The TW3801 uses the standard Ethernet MII or RMI interface to communicate with Ethernet PHYs (in Mode A, where the TW3801 emulates a MAC) or Ethernet MACs (in Mode B, where the TW3801 emulates a PHY).

The TW3801 supports the 100BASE-T communication mode. 10BASE-T communication is not supported, so both ends of a SLOC system must be connected to 100BASE-T devices.

Management Interface

The management interface is a serial bus used in Mode A to communicate between the TW3801 and the external PHY it is connected to.

SLOC as a MDIO master will check Ethernet PHY linkup status periodically by sending out MDC and MDIO signals. It requires SLOC to have MDIO PHY address to sync with the Ethernet-PHY chip's PHY address [4:0]. The SLOC MDIO PHY address can be programmed at {Reg0x1E[6:4], A1,A0}, where A1 and A0 are set by the logic levels of the external A1 and A0 pins.

Management Data I/O Timing

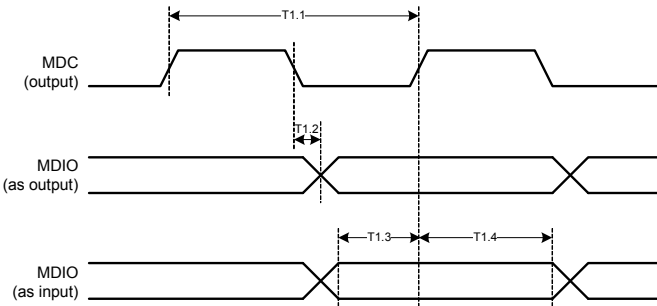


TABLE 1. MDIO INTERFACE TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------|----------------------------|-----|---------------------|-----|------|
| T1.1 | MDC Clock Cycle Time | | 8/f _{XTAL} | | ns |
| DC _{MDC} | MDC Clock Duty Cycle | 45 | | 55 | % |
| T1.2 | MDIO Data Output Delay | | | 5 | ns |
| T1.3 | MDIO Data Input Setup Time | 10 | | | ns |
| T1.4 | MDIO Data Input Hold Time | 10 | | | ns |

Setting the MDIO PHY Address

The TW3801's MDIO PHY address is abcde (in binary), where:

- a = register 0x1E bit 6
- b = register 0x1E bit 5
- c = register 0x1E bit 4
- d = state of A1 (pin 57)
- e = state of A0 (pin 56)

The TW3801's MDIO PHY address should be set to match the PHY address of the device it is connected to.

MII Interface

Ethernet data is transferred via the MII or RMI interface. The TW3801 is designed to work with any PHY with an MII interface, and has been tested with the following PHYs in MII mode:

- 88E1111 (Marvell)
- IP101A (IC+)
- LAN8710 (SMSC)
- RTL8201EL (Realtek)

MII Mode A (MAC Emulation) Input Timing

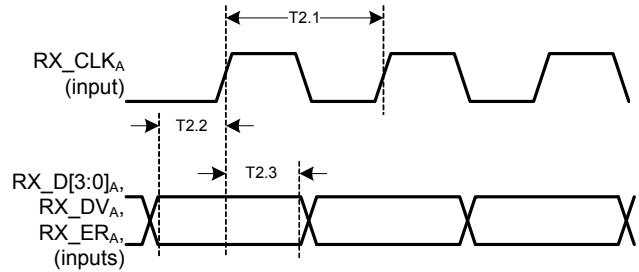


TABLE 2. MII MODE A (MAC EMULATION) INPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| T2.1 | RX_CLK _A Period | | 40 | | ns |
| DC _{RX_CLKA} | RX_CLK _A Duty Cycle | 20 | | 80 | % |
| T2.2 | Data Setup Time | 10 | | | ns |
| T2.3 | Data Hold Time | 10 | | | ns |

MII Mode A (MAC Emulation) Output Timing

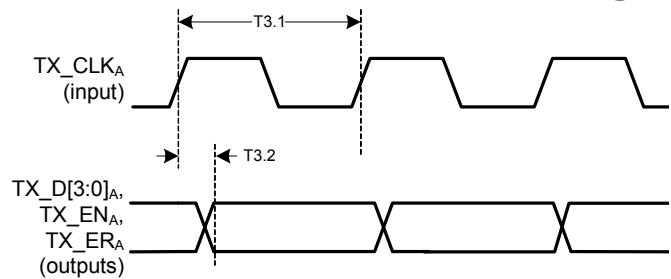


TABLE 3. MII MODE A (MAC EMULATION) OUTPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| T3.1 | TX_CLK _A Period | | 40 | | ns |
| DC _{TX_CLKA} | TX_CLK _A Duty Cycle | 20 | | 80 | % |
| T3.2 | Output Data Valid Delay | | | 14 | ns |

MII Mode B (PHY Emulation) Input Timing

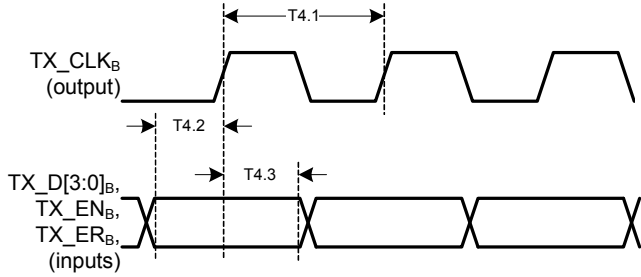


TABLE 4. MII MODE B (PHY EMULATION) INPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|--------------------------------|-----|------|
| T4.1 | TX_CLK _B Period | | 1/f _{X_{TAL}} | | ns |
| DC _{TX_CLKB} | TX_CLK _B Duty Cycle | 45 | | 55 | % |
| T4.2 | Data Setup Time | 10 | | | ns |
| T4.3 | Data Hold Time | 10 | | | ns |

MII Mode B (PHY Emulation) Output Timing

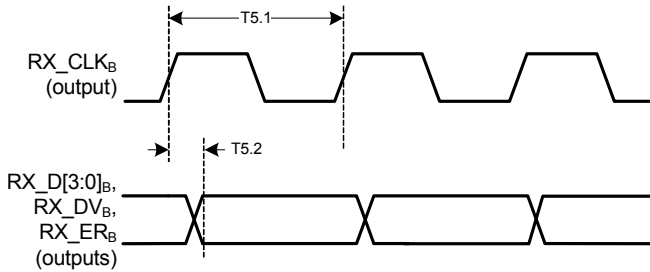


TABLE 5. MII MODE B (PHY EMULATION) OUTPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|--------------------------------|-----|------|
| T5.1 | RX_CLK _B Period | | 1/f _{X_{TAL}} | | ns |
| DC _{RX_CLKB} | RX_CLK _B Duty Cycle | 45 | | 55 | % |
| T5.2 | Output Data Valid Delay | | | 5 | ns |

RMII Interface

Ethernet data is transferred via the MII or RMII interface. The TW3801 is designed to work with any PHY with an RMII interface, and has been tested with the IP101A (IC+) PHY in RMII mode. The 50MHz RMII clock may be supplied by the external PHY or by the TEST_IO pin (when RMII Clock Source = 1).

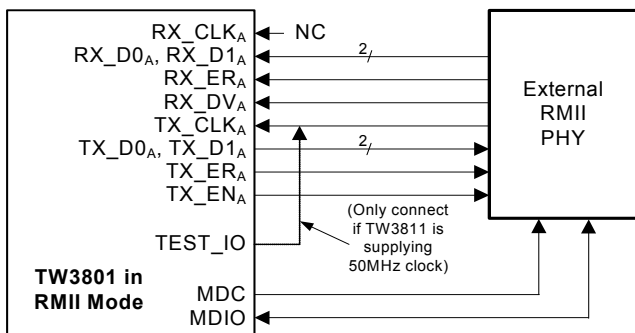


FIGURE 2. OPTIONAL USE OF TEST_IO AS RMII CLOCK SOURCE

RMII Mode A (MAC Emulation) Input Timing

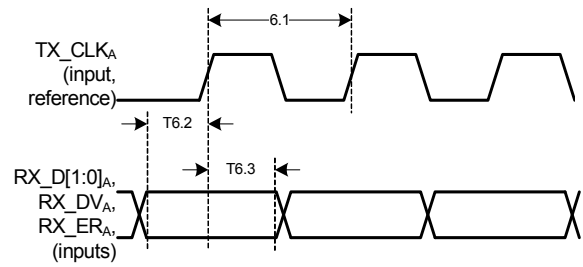


TABLE 6. RMII MODE A (MAC EMULATION) INPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| T6.1 | TX_CLK _A Period | | 20 | | ns |
| DC _{TX_CLKA} | TX_CLK _A Duty Cycle | 20 | | 80 | % |
| T6.2 | Data Setup Time | 4 | | | ns |
| T6.3 | Data Hold Time | 2 | | | ns |

RMII Mode A (MAC Emulation) Output Timing

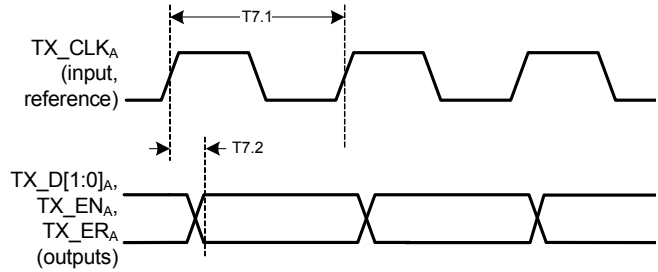


TABLE 7. RMII MODE A (MAC EMULATION) OUTPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| T7.1 | TX_CLK _A Period | | 20 | | ns |
| DC _{TX_CLKA} | TX_CLK _A Duty Cycle | 20 | | 80 | % |
| T7.2 | Output Data Valid Delay | | | 14 | ns |

RMII Mode B (PHY Emulation) Input Timing

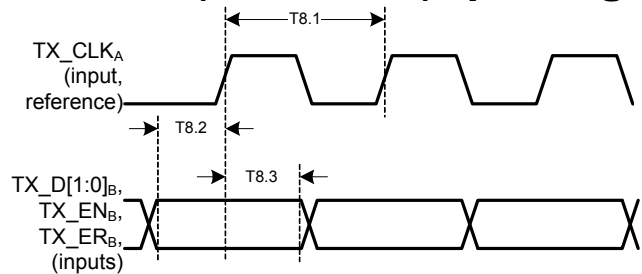


TABLE 8. RMII MODE B (PHY EMULATION) INPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| T8.1 | TX_CLK _A Period | | 20 | | ns |
| DC _{TX_CLKA} | TX_CLK _A Duty Cycle | 20 | | 80 | % |
| T8.2 | Data Setup Time | 4 | | | ns |
| T8.3 | Data Hold Time | 2 | | | ns |

RMII Mode B (PHY Emulation) Output Timing

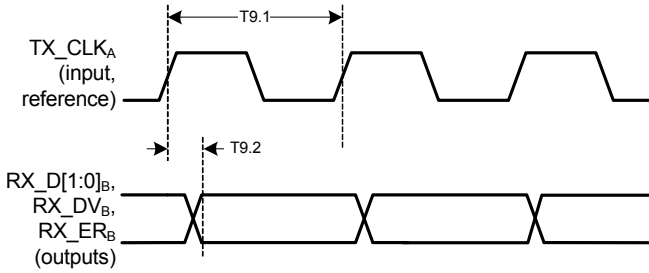


TABLE 9. RMII MODE B (PHY EMULATION) OUTPUT TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|---------------------|-----|------|
| T9.1 | TX_CLK _A Period | | 1/f _{XTAL} | | ns |
| DC _{TX_CLKA} | TX_CLK _A Duty Cycle | 45 | | 55 | % |
| T9.2 | Output Data Valid Delay | | | 14 | ns |

MII Passthrough Mode

Passthrough mode connects all the MII Inputs to all the MII outputs through the TW3801's internal drivers (Figure 3). Passthrough mode is enabled by setting Register 0x01[4:3] to 10b. Passthrough mode introduces a small delay between the input and output signals.

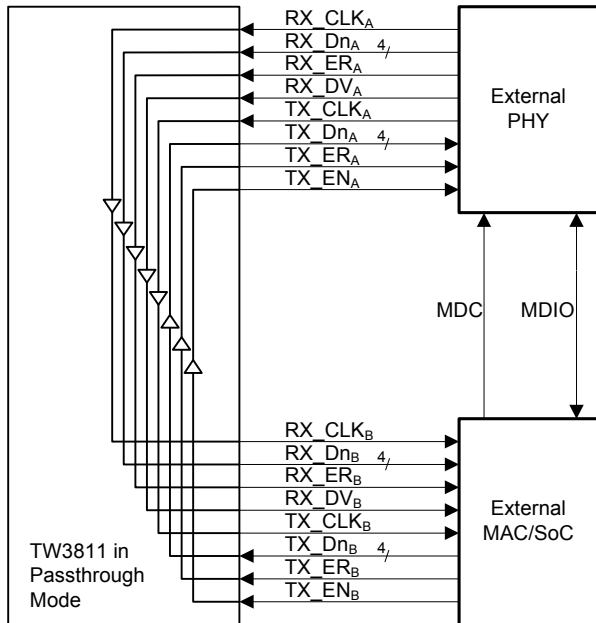


FIGURE 3. MII PASSTHROUGH MODE

TABLE 10. MII PASSTHROUGH MODE TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------|--|-----|-----|-----|------|
| Signal Delay | RX_CLK _A to RX_CLK _B RX_D[3:0] _A to RX_D[3:0] _B RX_ER _A to RX_ER _B RX_DV _A to RX_DV _B TX_CLK _A to TX_CLK _B TX_D[3:0] _B to TX_D[3:0] _A TX_ER _B to TX_ER _A TX_EN _B to TX_EN _A | 2.5 | | 10 | ns |

RMII Passthrough Mode

In RMII Passthrough mode, the signals are registered by the TX_CLK_A clock to minimize skew (Figure 4). Passthrough mode is enabled by setting Register 0x01[4:3] to 10b. Passthrough mode introduces a small delay between the input and output signals.

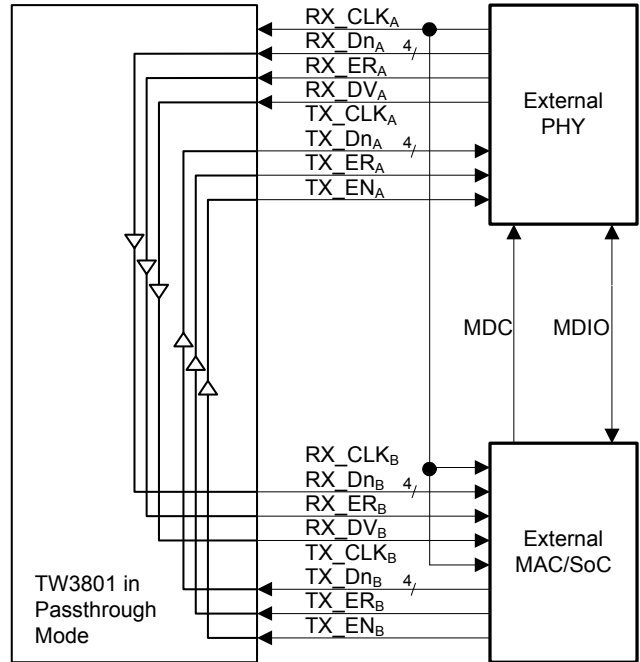


FIGURE 4. RMII PASSTHROUGH MODE

TABLE 11. RMII PASSTHROUGH MODE TIMING

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|-------------------|-----|-----|-----|------|
| T10.1 | D to Q Setup Time | 4 | | | ns |
| T10.2 | D to Q Hold Time | 2 | | | ns |

I²C Serial Interface

The TW3801 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the TW3801 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 5). On power-up of the TW3801, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The TW3801 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 5). A START condition is ignored during the power-up sequence and during non-volatile write cycles for the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 5). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode. A STOP condition at the end of a write operation to a non-volatile byte initiates an internal non-volatile write cycle. The device enters its standby state when the internal, non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 6).

The TW3801 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The TW3801 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0011 1 A1 A0 R/ \overline{W} as the seven MSBs, where A0 = the logic level of the A0 pin, A1 = the logic level of the A1 pin, and R/ \overline{W} is the bit that determines if the next operation is a read or a write. The Read/ \overline{Write} bit is "1" for a Read operation, and "0" for a Write operation (see Table 12).

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the TW3801 responds with an ACK.

STOP conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the TW3801 resets itself without performing the write.

TABLE 12. IDENTIFICATION BYTE FORMAT

| A1 | A0 | ADDRESS BYTE FOR A WRITE | ADDRESS BYTE FOR A READ |
|----|----|--------------------------|-------------------------|
| 0 | 0 | 0x38 | 0x39 |
| 0 | 1 | 0x3A | 0x3B |
| 1 | 0 | 0x3C | 0x3D |
| 1 | 1 | 0x3E | 0x3F |

Read Operation

A Current Address Read operation is shown in Figure 8. It consists of a minimum 2 bytes: a START followed by the ID byte from the master with the R/ \overline{W} bit set to 1, then an ACK followed by the data byte or bytes sent by the slave. The master terminates the Read operation by not responding with an ACK and then issuing a STOP condition. This operation is useful if the master knows the current address and desires to read one or more data bytes.

A Random Address Read operation consists of a three byte "dummy write" instruction followed by a Current Address Read operation (see Figure 6). The master initiates the operation issuing the following sequence: a START, the identification byte with the R/ \overline{W} bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/ \overline{W} bit set to "1". After each of the three bytes, the TW3801 responds with an ACK. The TW3801 then transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the Read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 9).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial's value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. Address 04h is the last valid data byte, higher addresses are not available. Data from addresses higher than memory location 04h will be invalid.

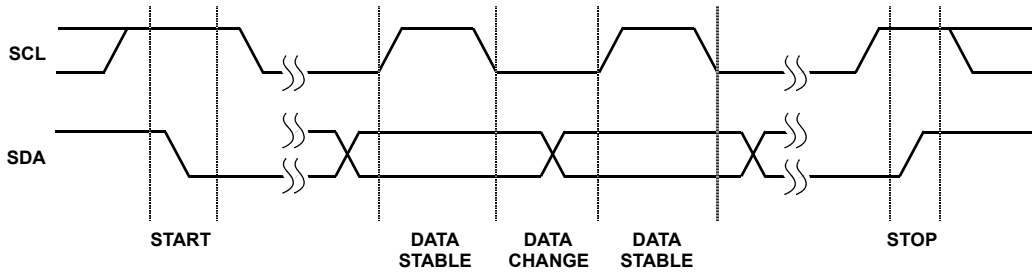


FIGURE 5. VALID DATA CHANGES, START AND STOP CONDITIONS

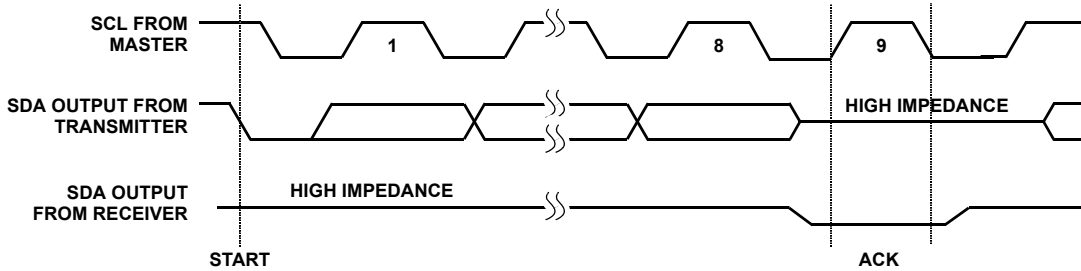


FIGURE 6. ACKNOWLEDGE RESPONSE FROM RECEIVER

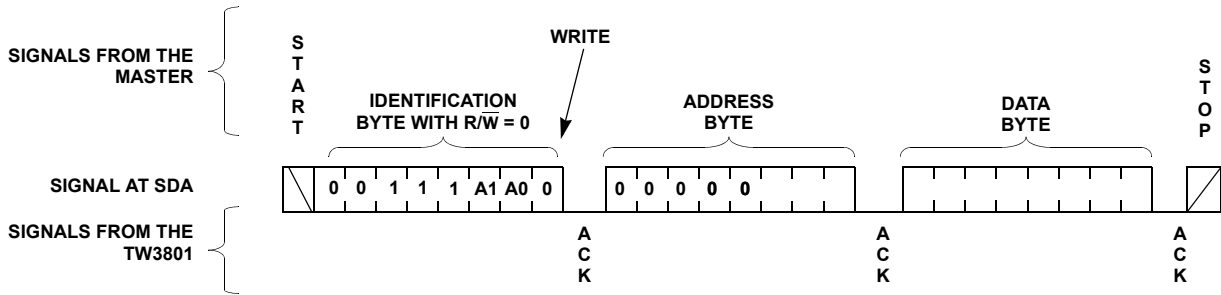


FIGURE 7. BYTE WRITE SEQUENCE

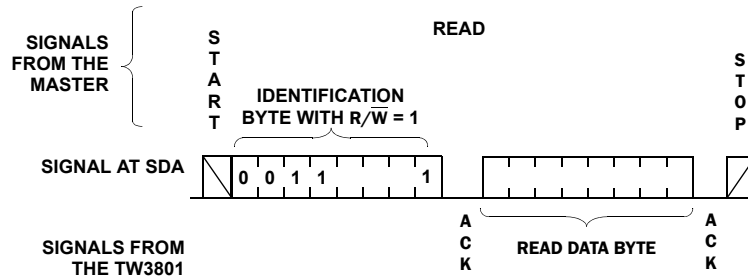


FIGURE 8. BYTE READ SEQUENCE

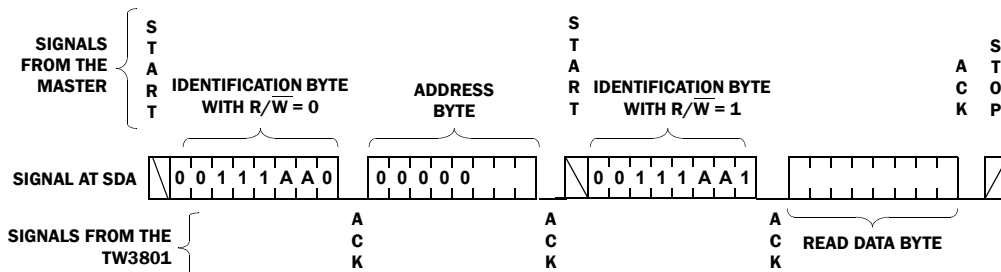


FIGURE 9. RANDOM ADDRESS READ SEQUENCE

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip lines are used.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Place power supply decoupling capacitors (0.1 μ F) as close to the device connections as possible. Avoid vias between the cap and the device because vias adds unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible. Do not connect anything to pins labelled "NC".

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|-------------------|----------|---|
| November 16, 2012 | FN8283.1 | <p>Changed "Application Block Diagram" on page 1 to only show 100BASE-T, and MCU as optional.</p> <p>Added 75Ω termination resistor to CVBS_IN in "Simplified Application Schematic" on page 1.</p> <p>Added 150nH inductor to COAX_OUT termination in "Simplified Application Schematic" on page 1.</p> <p>Horizontally flipped "Simplified Application Schematic" on page 1 so signal flow is from left to right.</p> <p>Eliminated unnecessary "Vdd Range" from Ordering Information table on page 2.</p> <p>For clarification, added "internal" in front of all pull-up/pull-down resistors in Pin Descriptions table.</p> <p>Added 150nH inductor to COAX_OUT pin description on page 3.</p> <p>Clarified Pin Description information for LED_0, LED_1, and LED_2 (all active low) on page 5. Previous version of datasheet incorrectly indicated LED_0 was active high.</p> <p>Changed CVBS Gain register on page 8 from 0x30 (correct for TW3811 but not TW3801) to 0x19.</p> <p>Corrected Register 0x30[6:0] on page 8 to show Maximum CVBS Gain as 0x7F.</p> <p>Changed Register 0x26 bit 7:5 on page 9 to "reserved" because the bit has no function.</p> <p>In "SLOC Control (0x00)" on page 9, changed "Set to 0 when writing this register." to "Set to 11b when writing this register."</p> <p>Clarified operation of registers 0x26, 0x27, and 0x43 on page 9.</p> <p>Added 150nH inductor to COAX_OUT termination in Figure 1 on page 11.</p> <p>Horizontally flipped Figure 1 on page 11 so signal flow is from left to right.</p> <p>Added "Setting the MDIO PHY Address" on page 12 to "Applications Information" section.</p> <p>Added "External Interfacing" paragraph to Applications Information section on page 12 clarifying that SLOC supports 100Mb/s 100BASE-T only (not 1-T).</p> <p>Added MII Interface and RMII Interface paragraphs to page 12 and page 13, including list of tested PHYs, and how to optionally use TEST_IO as the RMII clock source.</p> <p>Corrected drawings in Figures 1, 3, and 4 incorrectly showing the MDIO bus connecting the TW3811 to a MAC/SoC device.</p> <p>In "RMII Passthrough Mode" on page 14, changed "0x01[4:3] to 01b" to "0x01[4:3] to 10b"</p> <p>Emphasized 36Mbps and 4Mbps link speeds (the rates required for SLOC compliance) throughout document, including rewriting the Description section of registers 0x0A and 0x14 in the Register Listing section.</p> |
| June 8, 2012 | FN8283.0 | Initial Release |

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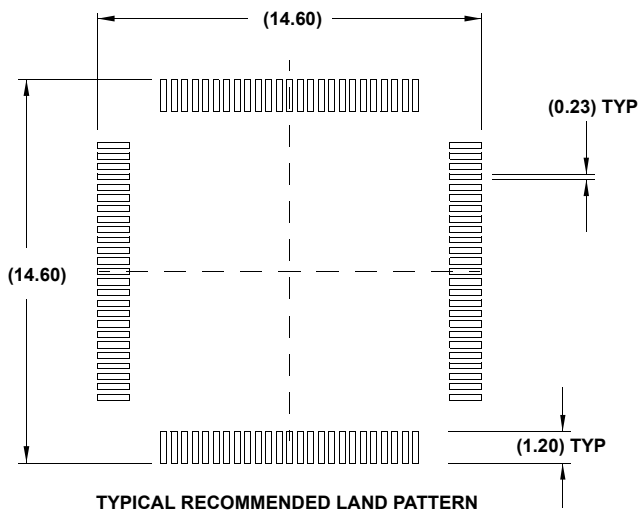
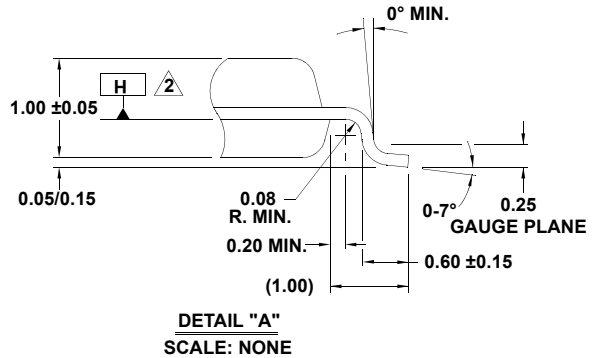
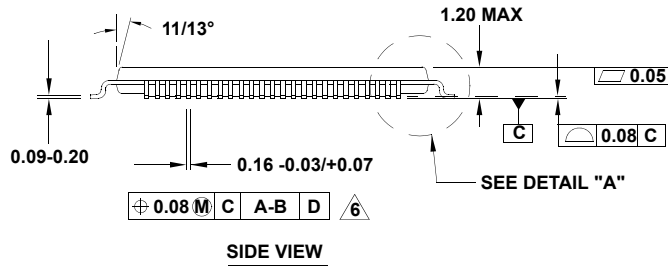
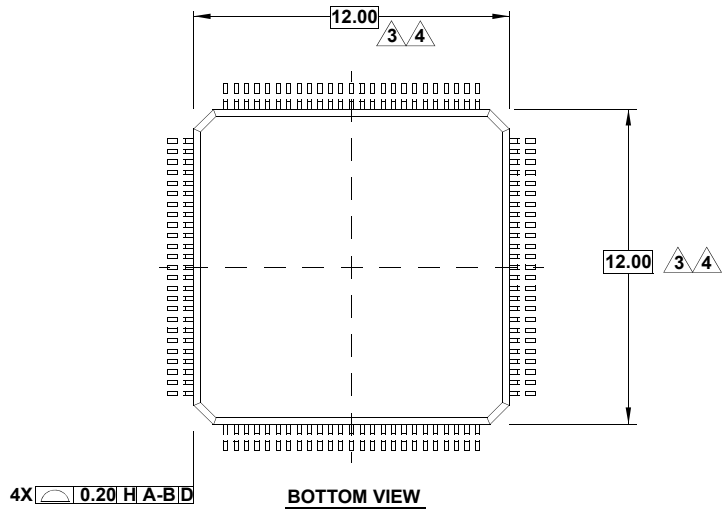
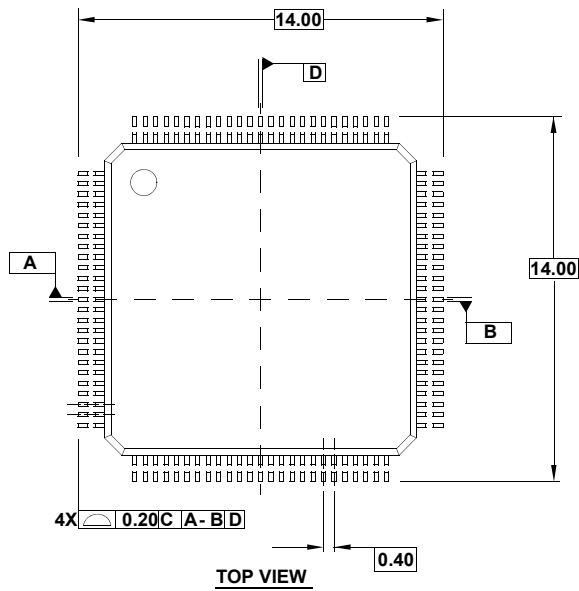
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Package Outline Drawing

Q100.12x12A

100 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE (TQFP)

Rev 0, 2/11



NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane **H** located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.25mm per side.
4. These dimensions to be determined at datum plane **H**.
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
6. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Controlling dimension: millimeter.
8. This outline conforms to JEDEC publication 95 registration MS-026, variation ADE.
9. Dimensions in () are for reference only.