



8-in-1 Video Decoders with PCI Express Media Bridge

TW6869

The [TW6869](#) is a highly integrated solution that supports multi-channel video and audio capture via PCIe x1 interface for PC DVR system and video analytic application. It contains high quality eight-channel NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data, and utilize adaptive 4H comb filter for separating luminance and chrominance to reduce cross noise artifacts.

TW6869 contains a high performance proprietary DMA controller that fully optimizes the utilization of PCIe x1 bandwidth and enables it to transfer video and audio data at a high throughput rate that closely approaches the theoretical limit of PCIe x1 interface. TW6869 is able to simultaneously decode and transfer 8 real time D1 video, or up to 32 channel non-real time D1, plus 8 channel audio.

TW6869 decreases the complexity and workload of client-side software development, and significantly reduces the strains on PC hardware and resources. TW6869 also includes a software development kit (SDK) with Windows and Linux compliant drivers and reference application software.

Features

Video Decoders

- Accepts all NTSC(M/N/4.43) / PAL(B/D/G/H/I/K/L/M/N/60) standards with auto detection
- Integrated eight video analog anti-alias filters and 10-bit CMOS ADCs
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- White peak AGC control
- Programmable hue, saturation, contrast, brightness and sharpness
- High quality proprietary fast video locking system for non-real-time application
- High performance adaptive 4H comb filters for all NTSC and PAL standards

Audio Codecs

- Integrated eight audio ADCs
- 8/16 bit audio word length
- Sample audio with 8/16/32/44.1/48kHz

DMA Controller

- Highly-efficient DMA design can support up to 8 real time D1 video and 8 real time audio channels, or up to 32 non-real-time video with optimization of full PCIe x1 bandwidth
- Multiple video format output support: UYVY/Y422, YUYV/YUY2, IYU1/Y411, Y41P, YUV420, RGB555 and RGB565
- Integrated internal video and audio generator simplifies system test and development
- Built-in motion detection engine for each video channel
- Hardware-friendly design enables smooth data transfer and virtually eliminates unwanted big-block data jamming among PC devices, resulting in optimized PC internal bandwidth consumption

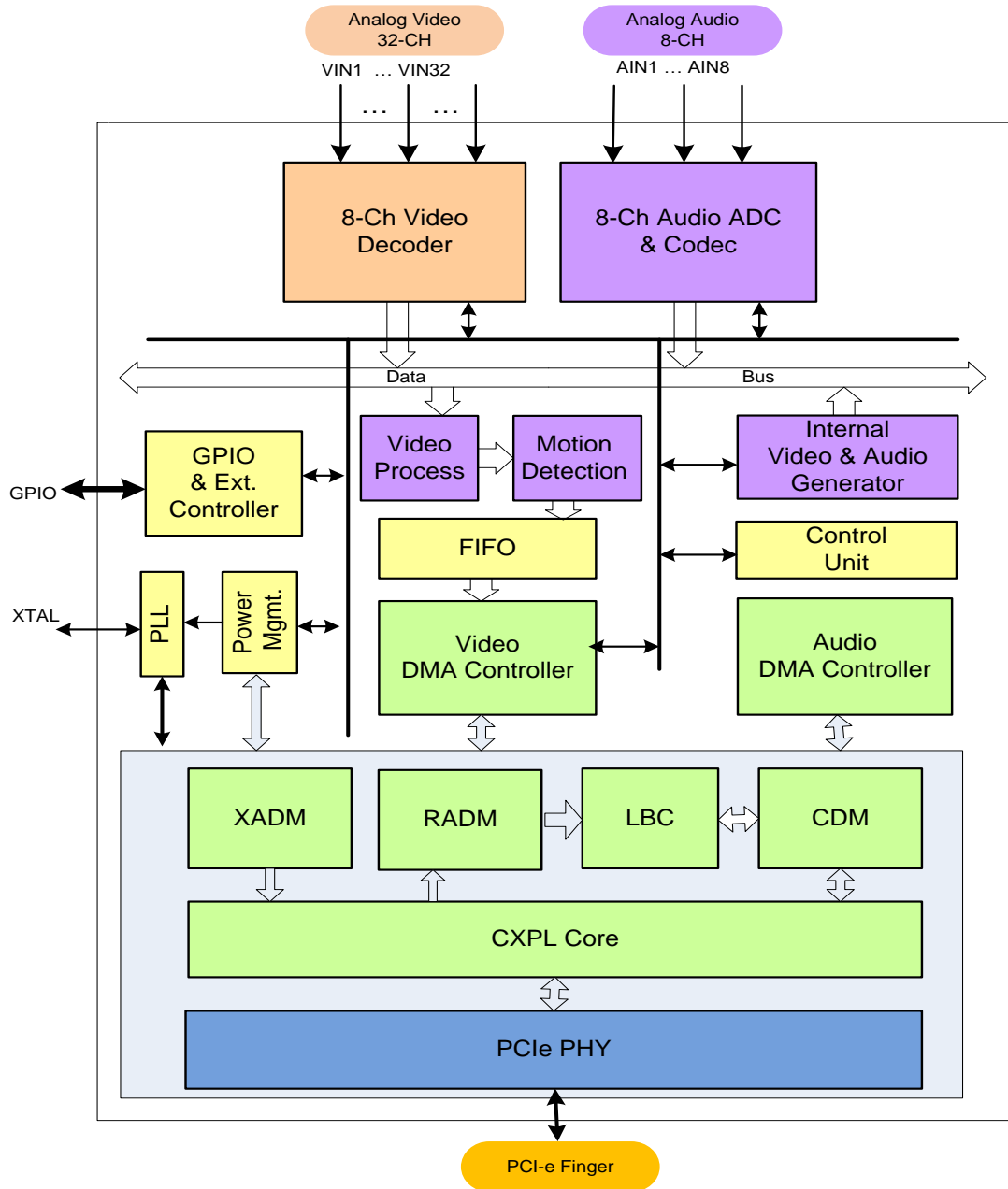
PCIe Configurations

- PCI Express Base Specification 1.1 Compliant
- Flexible PCIe packet size configuration: 128 byte, 256 byte and 512 byte options

Applications

- PC-based DVR system
- Video analytic system

Block Diagram



Pin Descriptions

ANALOG INTERFACE PINS (40)

| NAME | NUMBER | TYPE | DESCRIPTION |
|-------|--------|------|------------------------|
| VIN1A | 139 | A | Composite video inputs |
| VIN1B | 140 | A | Composite video inputs |
| VIN1C | 141 | A | Composite video inputs |
| VIN1D | 142 | A | Composite video inputs |
| VIN2A | 4 | A | Composite video inputs |
| VIN2B | 3 | A | Composite video inputs |
| VIN2C | 2 | A | Composite video inputs |
| VIN2D | 1 | A | Composite video inputs |
| VIN3A | 7 | A | Composite video inputs |
| VIN3B | 8 | A | Composite video inputs |
| VIN3C | 9 | A | Composite video inputs |
| VIN3D | 10 | A | Composite video inputs |
| VIN4A | 16 | A | Composite video inputs |
| VIN4B | 15 | A | Composite video inputs |
| VIN4C | 14 | A | Composite video inputs |
| VIN4D | 13 | A | Composite video inputs |
| VIN5A | 42 | A | Composite video inputs |
| VIN5B | 41 | A | Composite video inputs |
| VIN5C | 40 | A | Composite video inputs |
| VIN5D | 39 | A | Composite video inputs |
| VIN6A | 33 | A | Composite video inputs |
| VIN6B | 34 | A | Composite video inputs |
| VIN6C | 35 | A | Composite video inputs |
| VIN6D | 36 | A | Composite video inputs |
| VIN7A | 30 | A | Composite video inputs |
| VIN7B | 29 | A | Composite video inputs |
| VIN7C | 28 | A | Composite video inputs |
| VIN7D | 27 | A | Composite video inputs |
| VIN8A | 21 | A | Composite video inputs |
| VIN8B | 22 | A | Composite video inputs |
| VIN8C | 23 | A | Composite video inputs |

TW6869

| NAME | NUMBER | TYPE | DESCRIPTION |
|-------|--------|------|------------------------|
| VIN8D | 24 | A | Composite video inputs |
| AIN1 | 133 | A | Analog audio inputs |
| AIN2 | 134 | A | Analog audio inputs |
| AIN3 | 135 | A | Analog audio inputs |
| AIN4 | 136 | A | Analog audio inputs |
| AIN5 | 48 | A | Analog audio inputs |
| AIN6 | 47 | A | Analog audio inputs |
| AIN7 | 46 | A | Analog audio inputs |
| AIN8 | 45 | A | Analog audio inputs |

PCI EXPRESS INTERFACE (7)

| NAME | NUMBER | TYPE | DESCRIPTION |
|----------|--------|------|---|
| TX_M | 87 | O | High-Speed Differential Transmit Pair |
| TX_P | 88 | O | |
| RX_P | 90 | I | High-Speed Differential Receive Pair |
| RX_M | 91 | I | |
| REXT | 93 | IO | Reference Resistor Connection. 190Ω 1% precision resistor to ground |
| REFCLK_P | 95 | I | Differential Reference Clock Input |
| REFCLK_M | 96 | I | |

SYSTEM CONTROL PINS (50)

| NAME | NUMBER | TYPE | DESCRIPTION |
|------------|---|------|--|
| XTALI | 109 | IO | System reference clock crystal input (27MHz) |
| XTALO | 110 | IO | System reference clock crystal output |
| PERST_N | 84 | I | System reset. |
| TEST[1:0] | 53,52 | I | Test mode selection, tie to ground |
| GPIO[42:0] | 129,128,127,126,125, 124,123,122,121,118, 117,116,115,114,113, 108,107,106,105,104, 103,102,101,81,80,79, 78,77,76,75,70,69,68, 67,66,65,64,63,62,59, 58,57,56 | IO | GPIO control ports |
| T_SEL | 54 | I | NC |

TW6869

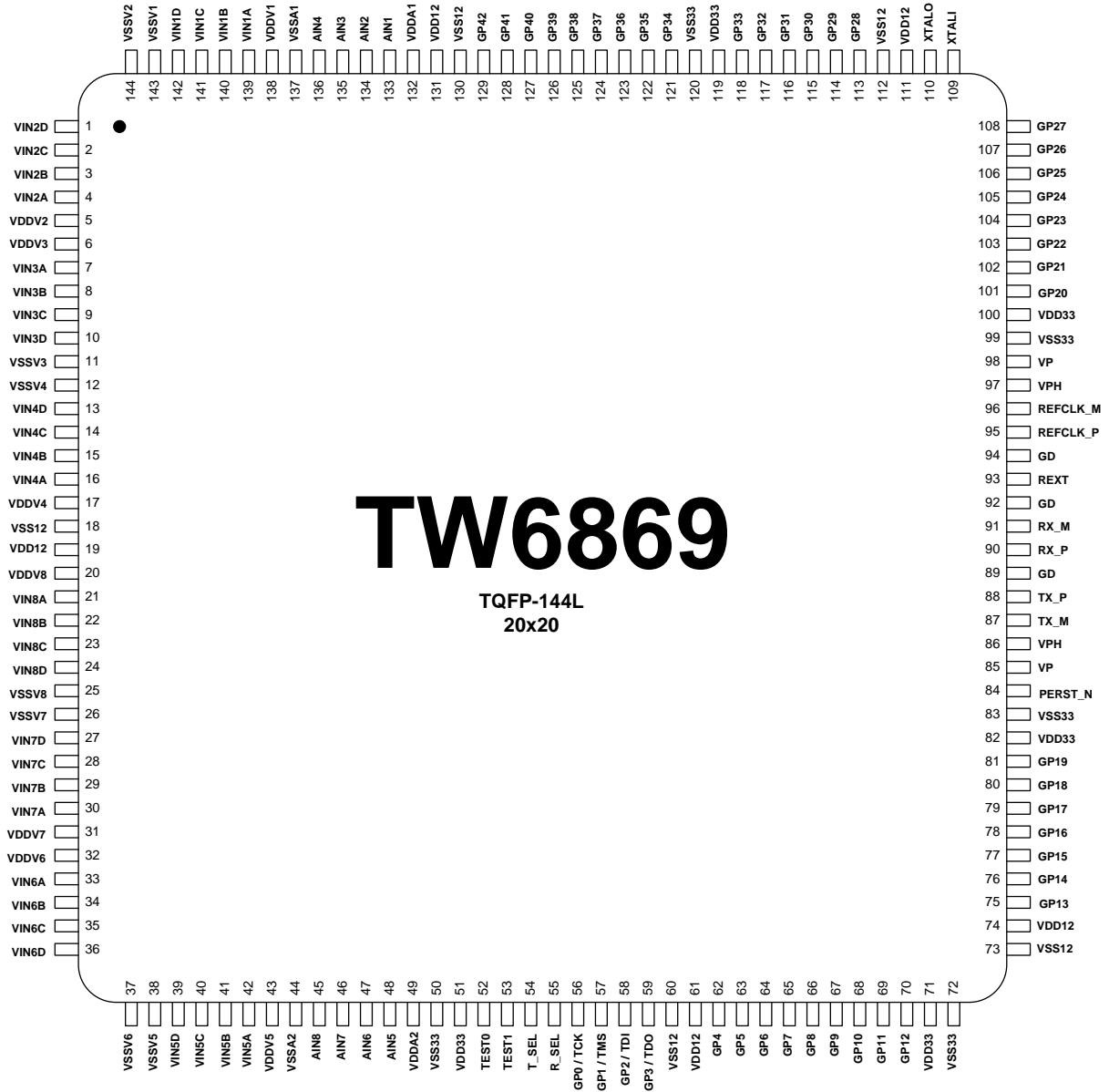
| NAME | NUMBER | TYPE | DESCRIPTION |
|-------|--------|------|-------------|
| R_SEL | 55 | I | NC |

POWER / GROUND PINS (47)

| NAME | NUMBER | TYPE | DESCRIPTION |
|-------|---------------------------|------|----------------------------------|
| VP | 85,98 | P | Low-Voltage Supply (1.2V) |
| VPH | 86,97 | P | High-Voltage I/O Supply (3.3V) |
| GD | 89,92,94 | G | Digital Ground |
| VDD33 | 51,71,82,100,119 | P | Digital I/O Power, 3.3V |
| VSS33 | 50,72,83,99,120 | G | Digital Ground |
| VDD12 | 19,61,74,111,131 | P | Digital Core Power, 1.2V |
| VSS12 | 18,60,73,112,130 | G | Digital Core Ground |
| VDDA | 132,49 | P | Analog Power for Audio ADC, 3.3V |
| VSSA | 137,44 | G | Analog Ground for Audio ADC |
| VDDV | 138,5,6,17,20,31,32,43 | P | Analog Power for Video ADC, 3.3V |
| VSSV | 143,144,11,12,25,26,37,38 | G | Analog Ground for Video ADC |

Pin Configuration

144 TQFP PIN DIAGRAM (TOP -> BOTTOM VIEW)



Ordering Information

| PART NUMBER (NOTE 1) | PART MARKING | PACKAGE (PB-FREE) | PKG. DWG. # |
|---------------------------------|-------------------------|------------------------------|------------------------|
| TW6869-TA1-CR | TW6869 TA1-CR | 144 LEAD TQFP (20mmx20mm) | Q144.20X20C |
| TW6869-TA1-CRH (Note 2) | TW6869 TA1-CRH | 144 LEAD TQFP (20mmx20mm) | Q144.20X20C |

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. "H" version supports Industrial Temperature operation. See **Supply Current and Power Dissipation** table on page 115.

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Functional Description

Video Decoder

VIDEO INPUT FORMATS

The TW6869 has built-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW6869 supports all common video formats as shown in Table 1.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW6869

| FORMAT | LINES | FIELDS | FSC | COUNTRY |
|---------------------------|-------|--------|-------------------|---|
| NTSC-M | 525 | 60 | 3.579545MHz | U.S., many others |
| NTSC-Japan ⁽¹⁾ | 525 | 60 | 3.579545MHz | Japan |
| PAL-B, G, N | 625 | 50 | 4.433619MHz | Many |
| PAL-D | 625 | 50 | 4.433619MHz | China |
| PAL-H | 625 | 50 | 4.433619MHz | Belgium |
| PAL-I | 625 | 50 | 4.433619MHz | Great Britain, others |
| PAL-M | 525 | 60 | 3.575612MHz | Brazil |
| PAL-CN | 625 | 50 | 3.582056MHz | Argentina |
| SECAM | 625 | 50 | 4.406MHz 4.250MHz | France, Eastern Europe, Middle East, Russia |
| PAL-60 | 525 | 60 | 4.433619MHz | China |
| NTSC (4.43) | 525 | 60 | 4.433619MHz | Transcoding |

Notes: (1). NTSC-Japan has 0 IRE setup.

ANALOG FRONTEND

The TW6869 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the V_ADC_PWDN register. The TW6869 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. Therefore, there is no need for external components in the analog input pin except for an AC coupling capacitor and a termination resistor. Figure 1 shows the frequency response of the anti-aliasing filter.

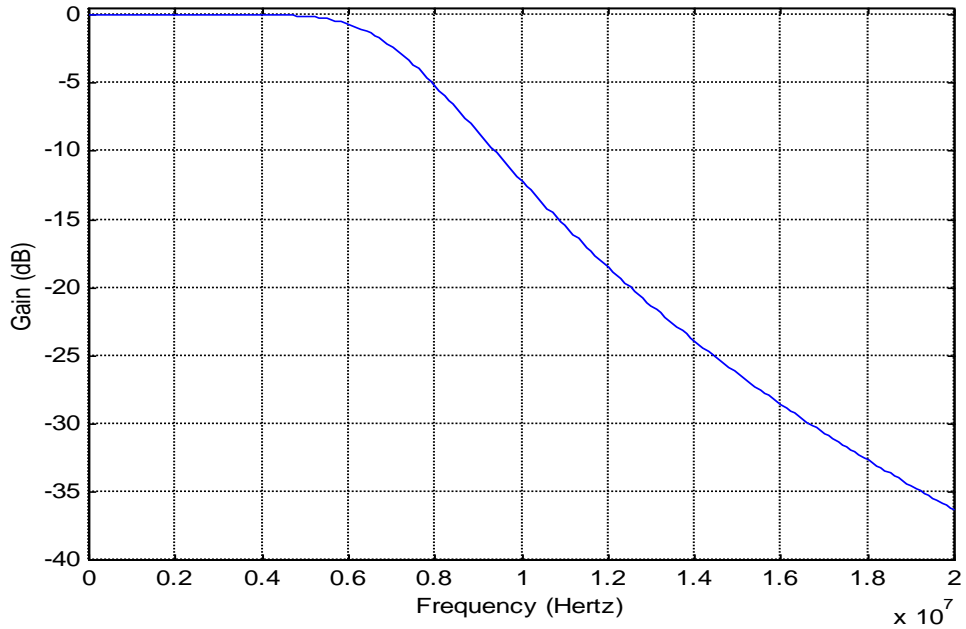


FIGURE 1. THE FREQUENCY RESPONSE OF ANTI-ALIASING FILTER

Decimation Filter

The digitized composite video data is over-sampled to simplify the design of the analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. Figure 2 shows the characteristic of the decimation filter.

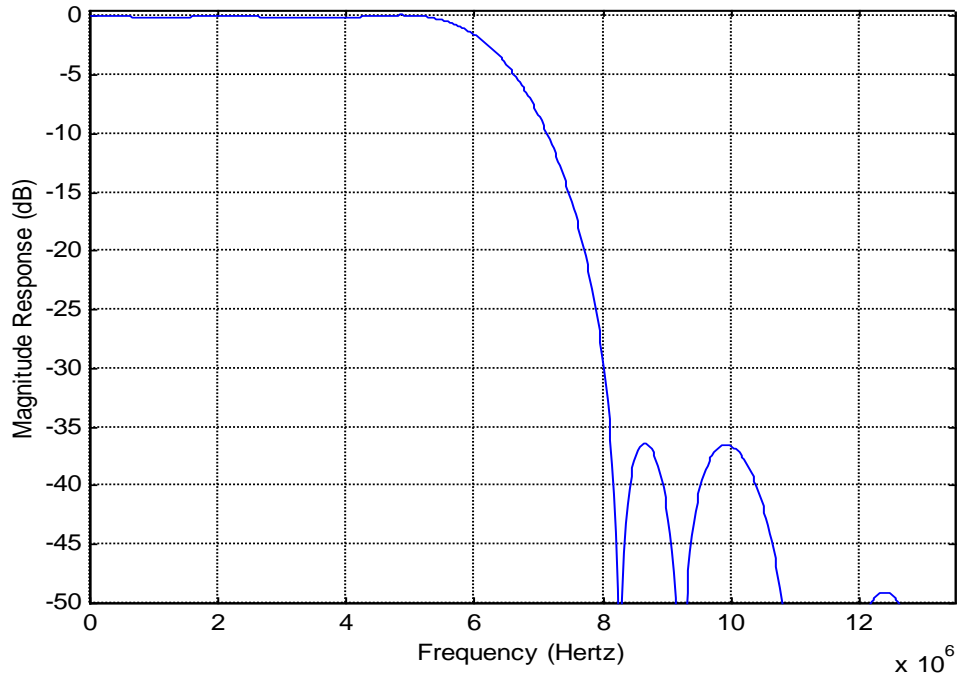


FIGURE 2. THE CHARACTERISTIC OF THE DECIMATION FILTER

AUTOMATIC GAIN CONTROL AND CLAMPING

All four analog channels have built-in clamping circuits that restore the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

SYNC PROCESSING

The sync processor of TW6869 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals, such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input.

Y/C SEPARATION

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the TW6869 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there are always two lines processing delay at the output except for the component input mode, which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Figure 3 shows the frequency response of the notch filter for each system NTSC and PAL. Figure 4 shows the frequency response of Chroma Band Pass Filter Curves.

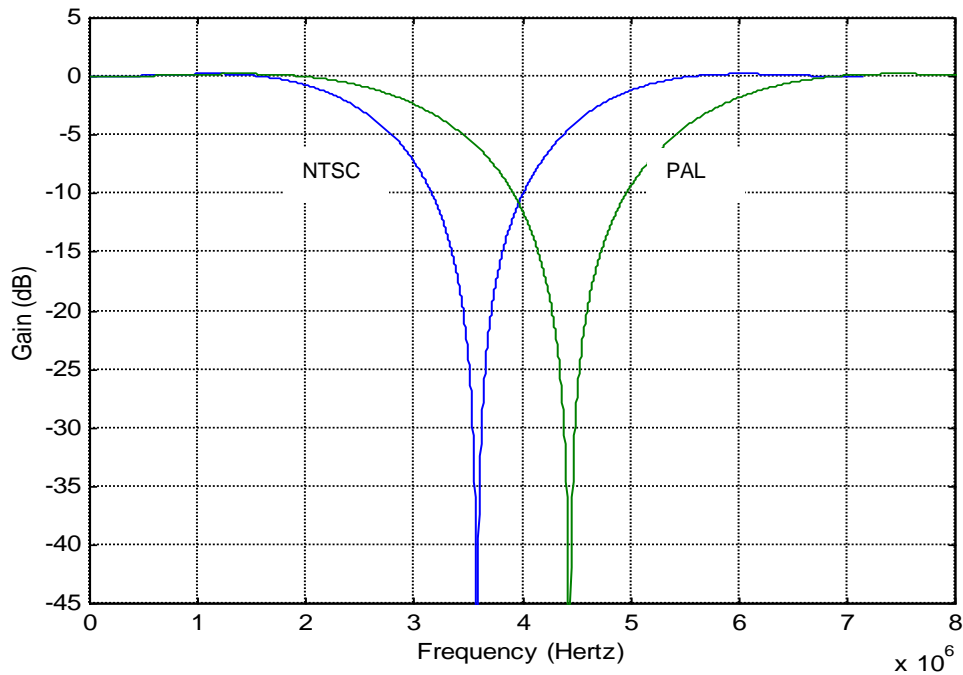


FIGURE 3. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR PAL

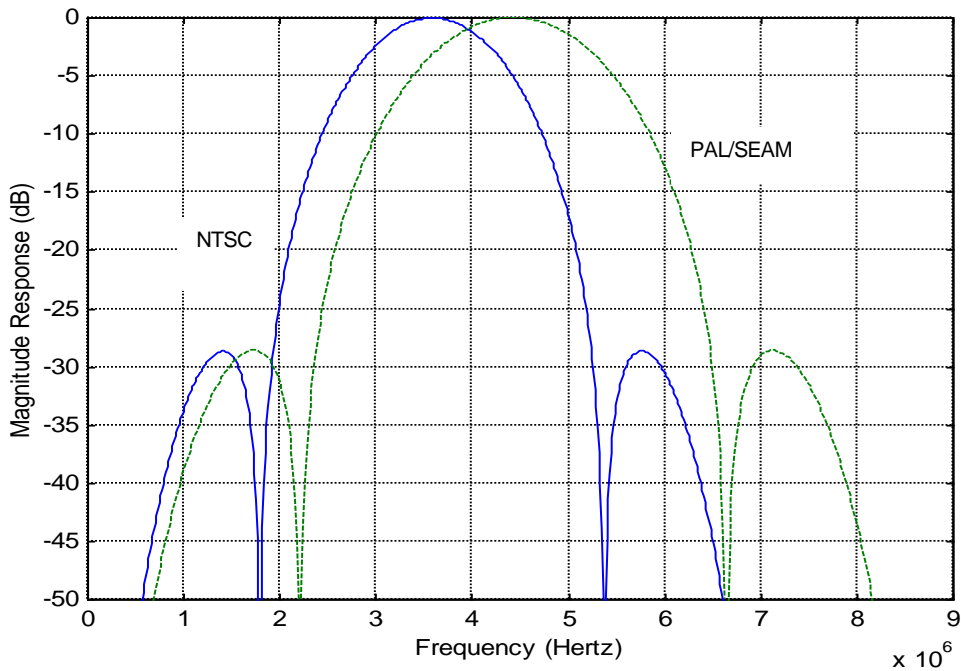


FIGURE 4. CHROMA BAND PASS FILTER CURVES

COLOR DECODING

Chrominance Demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto a different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Figure 5 shows the frequency response of Chrominance Low-Pass Filter Curves.

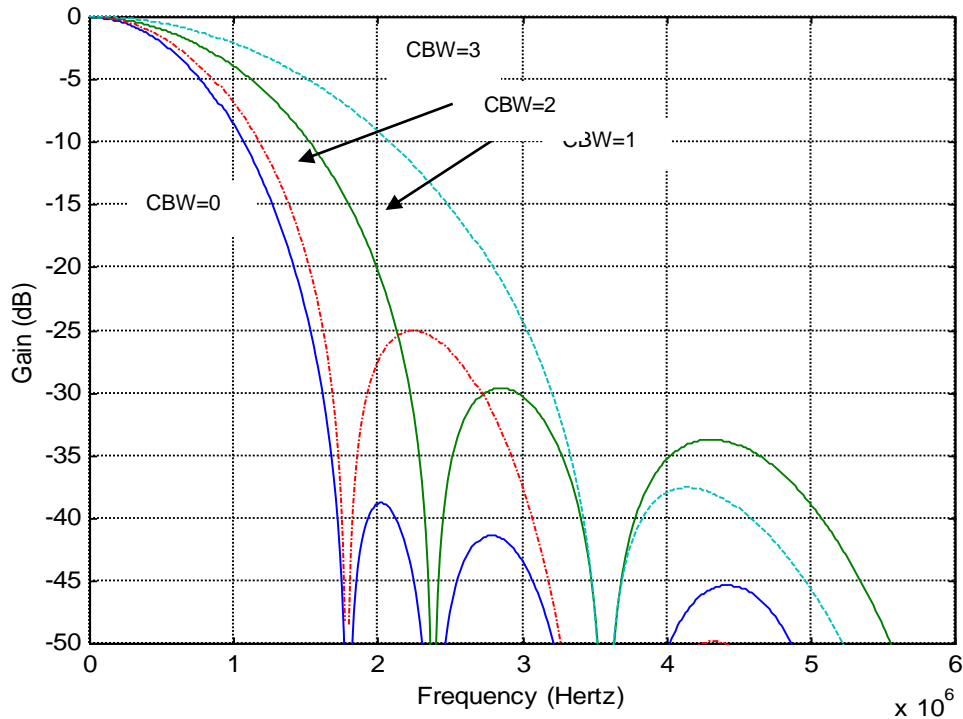


FIGURE 5. CHROMINANCE LOW-PASS FILTER CURVES

ACC (Automatic Color Gain Control)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The range of ACC control is -6db to +24db.

CHROMINANCE PROCESSING

Chrominance Gain, Offset and Hue Adjustment

When decoding NTSC signals, TW6869 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (Color Transient Improvement)

The TW6869 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

LUMINANCE PROCESSING

The TW6869 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW6869 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

Figure 6 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

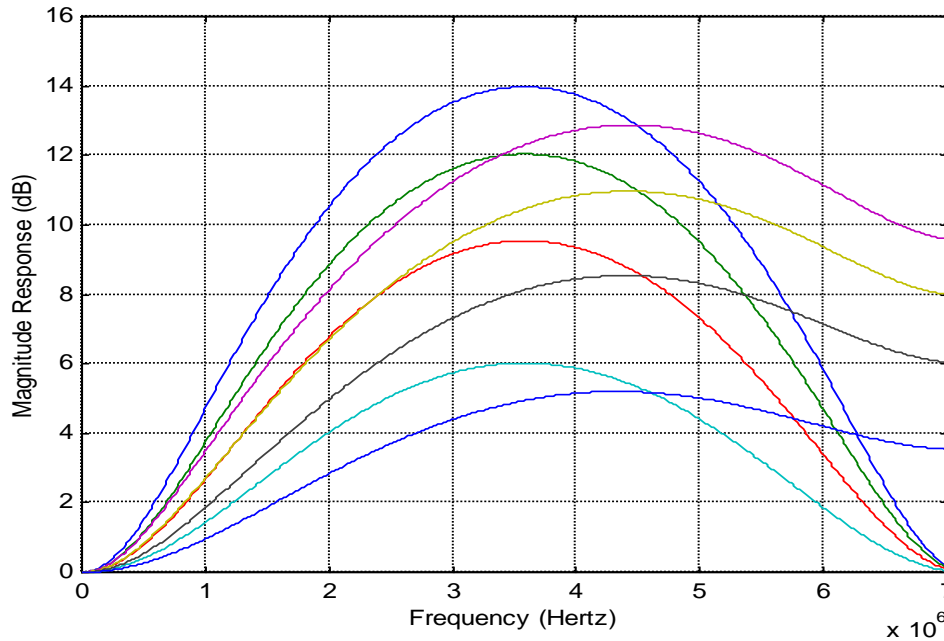


FIGURE 6. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

VIDEO CROPPING

Cropping allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Figure 6. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the un-scaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the un-scaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

$$HDELAY + HACTIVE < \text{Total number of pixels per line}$$

For NTSC output at 13.5MHz pixel rate, the total number of pixels is 858. For PAL output at 13.5MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical

active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

$$VDELAY + VACTIVE < \text{Total number of lines per field}$$

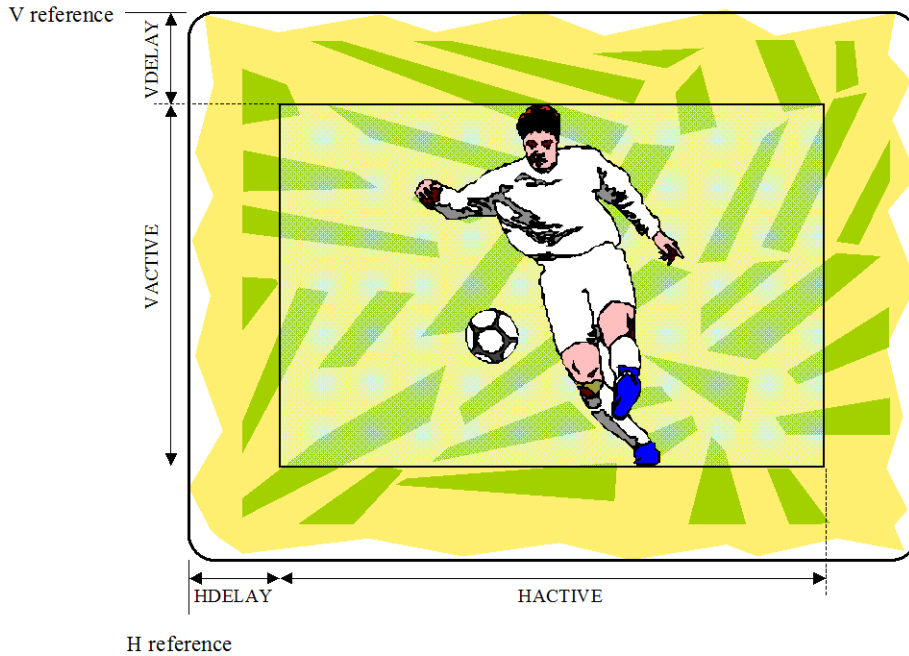


FIGURE 7. THE EFFECT OF CROPPING REGISTERS

VIDEO SCALER

The TW6869 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses simple line dropping algorithm. Therefore, the use of non-integer vertical scaling ration is not recommended.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW6869 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60Hz system and 768 pixels for 50Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register, the 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{\text{pixel_desired}}] * 256$

PAL: $HSCALE = [(720/N_{\text{pixel_desired}})] * 256$

Where: $N_{\text{pixel_desired}}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$$\text{HSCALE} = [(720/320)] * 256 = 576 = 0x0240$$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$$\text{HSCALE} = [(640/320)] * 256 = 512 = 0x200$$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW6869. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. The following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

$$\text{60Hz system: } \text{VSCALE} = [240 / N_{\text{line_desired}}] * 256$$

$$\text{50Hz system: } \text{VSCALE} = [288 / N_{\text{line_desired}}] * 256$$

Where: $N_{\text{line_desired}}$ is the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 2. Figure 8 shows the Horizontal Scaler Pre-Filter Curves.

TABLE 2. HSCALE AND VSCALE VALUE FOR SOME POPULAR VIDEO FORMATS.

| SCALING RATIO | FORMAT | TOTAL RESOLUTION | OUTPUT RESOLUTION | HSCALE VALUES | VSCALE (FRAME) |
|---------------|--------------|------------------|-------------------|---------------|----------------|
| 1:1 | NTSC SQ | 780x525 | 640x480 | 0x0100 | 0x0100 |
| | NTSC CCIR601 | 858x525 | 720x480 | 0x0100 | 0x0100 |
| | PAL SQ | 944x625 | 768x576 | 0x0100 | 0x0100 |
| | PAL CCIR601 | 864x625 | 720x576 | 0x0100 | 0x0100 |
| 2:1 (CIF) | NTSC SQ | 390x262 | 320x240 | 0x0200 | 0x0200 |
| | NTSC CCIR601 | 429x262 | 360x240 | 0x0200 | 0x0200 |
| | PAL SQ | 472x312 | 384x288 | 0x0200 | 0x0200 |
| | PAL CCIR601 | 432x312 | 360x288 | 0x0200 | 0x0200 |
| 4:1 (QCIF) | NTSC SQ | 195x131 | 160x120 | 0x0400 | 0x0400 |
| | NTSC CCIR601 | 214x131 | 180x120 | 0x0400 | 0x0400 |
| | PAL SQ | 236x156 | 192x144 | 0x0400 | 0x0400 |
| | PAL CCIR601 | 216x156 | 180x144 | 0x0400 | 0x0400 |

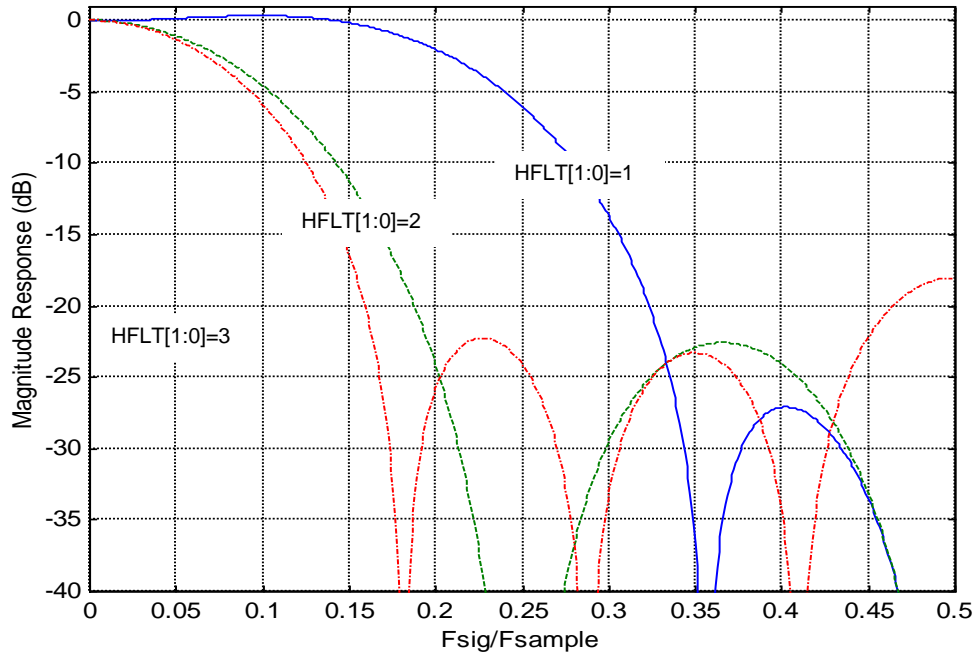


FIGURE 8. HORIZONTAL SCALER PRE-FILTER CURVES

Motion Detection

The TW6869 supports a motion detector for each of the 8 video decoders. The built-in motion detection algorithm uses the difference of luminance level between current and the reference field. To detect motion properly according to situation needed, the TW6869 provides several sensitivity and velocity control parameters for each motion detector. The TW6869 supports manual strobe function to update motion detection so that it is more appropriate for user-defined motion sensitivity control. When motion is detected in any video inputs, the TW6869 updates its motion status registers. Through which the host processor can read the motion information.

Audio Codec

The audio codec in the TW6869 is composed of 8 audio Analog-to-Digital converters, audio mixer and audio detector. The TW6869 can accept 8 analog audio signals, and produce 8 channel digital audio data.

The level of analog audio input signal AIN1 ~ AIN8 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1, AIGAIN2, AIGAIN3 and AIGAIN4 registers and then sampled by each Analog-to-Digital converters.

The TW6869 can mix all of analog audio inputs according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO4 registers. This mixing audio output can also be transferred through PCIe interface.

AUDIO DETECTION

The TW6869 has an audio detector for individual 8 channels. There are 2 kinds of audio detection method defined by the AAMPMD. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1 ~ ADET_TH4 registers.

DMA Controller

This module mainly packs the received video and audio data to the defined maximum payload size and manages the target address of each transaction layer package. It uses round-robin arbitration among DMA channels to choose current on-duty one. The Legacy PCI INT_A compatible interrupt emulation is supported to interrupt PC.

Internal Video & Audio Generator

To assist video debugging, this generator outputs 8 different colorbar patterns for each video DMA channel. Each colorbar pattern includes 7 vertical color bars and 1 horizontal black/grey color whose position and width are adjustable.

To assist audio debugging, this generator outputs 8 different single tones with adjustable sampling rate. The 9th audio pattern is a mixing mode whose tone is chosen from one of others with register setting.

Control Unit

This module handles configuration and control through PCIe to all internal blocks and registers such as DMA controller and PCIe EndPoint Controller.

GPIO & Ext. Controller

This module controls all GPIO pins, configures external TW2864 through serial control pins (SCLK and SDAT), and resets external TW2864 through RST_TO_2864 pin.

PCI Express EndPoint Controller

This controller contains three main PCI Express protocol layers: Transaction later, Data Link Layer, and Physical Layer. It complies with PCI Express Base Specification, Revision 1.1, and PCI Express 2.0 Base Specification, Revision 2.0. It works with external x1 PHY through the standard PHY Interface for PCI Express (PIPE).

PCI Express PHY

This module is PCI express physical layer.

Host Interface

The TW6869 provides with PCI Express interface for programming and controlling.

TW6869

For Video Decoder and Audio Codec CH0~CH3. (*: Read only register/bit)

[B[31:8] are hardwired to 0 in all registers.

| Address | | | | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default | |
|---------|-------|-------|-------|--------------|-----|---------------|---------|---------------------|----------|---------------|-----------|---------------|----------|---------|------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | | | | |
| 0x100 | 0x110 | 0x120 | 0x130 | VIDSTAT* | R | VDLOSS* | HLOCK* | SLOCK* | FIELD* | VLOCK* | RESERVED* | MONO* | DET50* | 0x00 | |
| 0x101 | 0x111 | 0x121 | 0x131 | BRIGHT | R/W | BRIGHTNESS | | | | | | | | 0x00 | |
| 0x102 | 0x112 | 0x122 | 0x132 | CONTRAST | R/W | CONTRAST | | | | | | | | 0x64 | |
| 0x103 | 0x113 | 0x123 | 0x133 | SHARPNESS | R/W | SCURVE | | VSF | | CTI | | SHARPNESS | | 0x11 | |
| 0x104 | 0x114 | 0x124 | 0x134 | SAT_U | R/W | SAT_U | | | | | | | | 0x80 | |
| 0x105 | 0x115 | 0x125 | 0x135 | SAT_V | R/W | SAT_V | | | | | | | | 0x80 | |
| 0x106 | 0x116 | 0x126 | 0x136 | HUE | R/W | HUE | | | | | | | | 0x00 | |
| 0x107 | 0x117 | 0x127 | 0x137 | CROP_HI | R/W | VDELAY[9:8] | | VACTIVE[9:8] | | HDELAY[9:8] | | HACTIVE[9:8] | | 0x02 | |
| 0x108 | 0x118 | 0x128 | 0x138 | VDELAY_LO | R/W | VDELAY[7:0] | | | | | | | | 0x12 | |
| 0x109 | 0x119 | 0x129 | 0x139 | VACTIVE_LO | R/W | VACTIVE[7:0] | | | | | | | | 0xF0 | |
| 0x10A | 0x11A | 0x12A | 0x13A | HDELAY_LO | R/W | HDELAY[7:0] | | | | | | | | 0x0F | |
| 0x10B | 0x11B | 0x12B | 0x13B | HACTIVE_LO | R/W | HACTIVE[7:0] | | | | | | | | 0x00 | |
| 0x10C | 0x11C | 0x12C | 0x13C | MVSN* | R | SF* | PF* | FF* | KF* | CSBAD* | MCVSN* | CSTRIPE* | CTYPE* | 0x00 | |
| 0x10D | 0x11D | 0x12D | 0x13D | STATUS2* | R | VCR* | WKAIR* | WKAIR1* | VSTD* | NINL* | 0 | 0 | 0 | 0x00 | |
| 0x10E | 0x11E | 0x12E | 0x13E | SDT | R/W | DETSTUS* | | STDNOW* | | ATREG | | STANDARD | | 0x07 | |
| 0x10F | 0x11F | 0x12F | 0x13F | STD_EN | R/W | ATSTART | PAL60EN | PALCEN | PALMEN | NTSC44EN | SECAMEN | PALBEN | NTSCEN | 0x7F | |
| 0x140 | 0x150 | 0x160 | 0x171 | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| 0x141 | 0x151 | 0x161 | 0x172 | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| 0x142 | 0x152 | 0x162 | 0x173 | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| 0x143 | 0x153 | 0x163 | 0x174 | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| 0x144 | 0x154 | 0x164 | 0x174 | VSCALE_LO | R/W | VSCALE[7:0] | | | | | | | | 0x00 | |
| 0x145 | 0x155 | 0x165 | 0x175 | SCALE_HI | R/W | VSCALE[11:8] | | | | HSACLE[11:8] | | | | 0x11 | |
| 0x146 | 0x156 | 0x166 | 0x176 | HSCALE_LO | R/W | HSCALE[7:0] | | | | | | | | 0x00 | |
| 0x147 | 0x157 | 0x167 | 0x177 | F2CROP_HI | R/W | V2DELAY[9:8] | | V2ACTIVE[9:8] | | H2DELAY[9:8] | | H2ACTIVE[9:8] | | 0x02 | |
| 0x148 | 0x158 | 0x168 | 0x178 | F2VDELAY_LO | R/W | V2DELAY[7:0] | | | | | | | | 0x12 | |
| 0x149 | 0x159 | 0x169 | 0x179 | F2VACTIVE_LO | R/W | V2ACTIVE[7:0] | | | | | | | | 0xF0 | |
| 0x14A | 0x15A | 0x16A | 0x17A | F2HDELAY_LO | R/W | H2DELAY[7:0] | | | | | | | | 0x0F | |
| 0x14B | 0x15B | 0x16B | 0x17B | F2HACTIVE_LO | R/W | H2ACTIVE[7:0] | | | | | | | | 0x00 | |
| 0x14C | 0x15C | 0x16C | 0x17C | F2VSCALE_LO | R/W | V2SCALE[7:0] | | | | | | | | 0x00 | |
| 0x14D | 0x15D | 0x16D | 0x17D | F2SCALE_HI | R/W | V2SCALE[11:8] | | | | H2SACLE[11:8] | | | | 0x11 | |
| 0x14E | 0x15E | 0x16E | 0x17E | F2HSCALE_LO | R/W | H2SCALE[7:0] | | | | | | | | 0x00 | |
| 0x14F | 0x15F | 0x16F | 0x17F | F2CNT | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F2CNT | 0x00 | |
| 0x1A0 | 0x1A1 | 0x1A2 | 0x1A3 | RESERVED | R | CVSTD | | | NT50 | RESERVED | | | | | 0x08 |
| 0x1A4 | 0x1A5 | 0x1A6 | 0x1A7 | IDCNTL | R/W | IDX | | NSEN/SSEN/PSEN/WKTH | | | | | | 0x1A | |
| 0x180 | | | | SRST | R/W | 0 | 0 | 0 | AUDIORST | VDEC4RST | VDEC3RST | VDEC2RST | VDEC1RST | 0x00 | |
| 0x181 | | | | ACNTL | R/W | 0 | IREF | VREF | 0 | CLKPDN | 0 | YFLEN | YSV | 0x02 | |

TW6869

For Video Decoder and Audio Codec CH0~CH3. (*: Read only register/bit)

B[31:8] are hardwired to 0 in all registers.

| Address | | | | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default | |
|---------|-------------|-----|-----|------------|-----|---------------|--------|---------------|---------|---------------|-------------|---------------|-------------|---------|------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | | | | |
| | 0x182 | | | ACNTL2 | R/W | CTEST | YCLEN | 0 | AFLTEN | GTEST | VLPF | CKLY | CKLC | 0x10 | |
| | 0x183 | | | CNTRL1 | R/W | PBW | DEM | PALSW | SET7 | COMB | HCOMP | YCOMB | PDLY | 0xCC | |
| | 0x184 | | | CKHY | R/W | GMEN | CKHY | | | HSDLY | | | | 0x00 | |
| | 0x185 | | | SHCOR | R/W | SHCOR | | | 0 | 0 | 0 | 0 | | 0x80 | |
| | 0x186 | | | CORING | R/W | CTCOR | | CCOR | | VCOR | | CIF | | 0x44 | |
| | 0x187 | | | CLMPG | R/W | CLPEND | | | CLPST | | | | 0x50 | | |
| | 0x188 | | | IAGC | R/W | NMGAIN | | | WPGAIN | | | 0 | 0x22 | | |
| | 0x189 | | | VSCL | R/W | 0 | FC27 | VYCOMB | VCCOMB | WBILINE | | | | 0x40 | |
| | 0x18A | | | PEAKWT | R/W | PEAKWT | | | | | | | | 0xD8 | |
| | 0x18B | | | CLMPL | R/W | CLMPLD | CLMPL | | | | | | | 0xBC | |
| | 0x18C | | | SYNCT | R/W | SYNCTD | SYNCT | | | | | | | 0xB8 | |
| | 0x18D | | | MISSCNT | R/W | MISSCNT | | | | HSWIN | | | | 0x44 | |
| | 0x18E | | | PCLAMP | R/W | PCLAMP | | | | | | | | 0x38 | |
| | 0x18F | | | VCNTL1 | R/W | VLCKI | | VLCKO | | VMODE | DETV | AFLD | VINT | 0x00 | |
| | 0x190 | | | VCNTL2 | R/W | BSHT | | | VSHT | | | | | 0x00 | |
| | 0x191 | | | CKILL | R/W | CKILMAX | | | CKILMIN | | | | | 0x78 | |
| | 0x192 | | | COMB | R/W | COMBMD | HTL | | | VTL | | | | 0x44 | |
| | 0x193 | | | LDLY | R/W | CKLM | YDLY | | | 0 | 0 | BP | HPF_RES | 0x30 | |
| | 0x194 | | | MISC1 | R/W | HPLC | ENCNT | PALC | SDET | TBCEN | BYPASS | SYOUT | 0 | 0x14 | |
| | 0x195 | | | LOOP | R/W | HPM | | ACCT | | SPM | | CBW | | 0xA5 | |
| | 0x196 | | | MISC2 | R/W | NKILL | PKILL | SKILL | CBAL | FCS | LCS | CCS | BST | 0xE0 | |
| | 0x197 | | | CLMD | R/W | FRM | | YNR | | CLMD | | PSP | | 0x05 | |
| | 0x198~0x19F | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| | 0x1A8 | | | HFLT21 | R/W | HFLT2 | | | HFLT1 | | | | | 0x00 | |
| | 0x1A9 | | | HFLT43 | R/W | HFLT4 | | | HFLT3 | | | | | 0x00 | |
| | 0x1AA | | | AGCEN | R/W | AGCEN4 | AGCEN3 | AGCEN2 | AGCEN1 | AGCGAIN4[8] | AGCGAIN3[8] | AGCGAIN2[8] | AGCGAIN1[8] | 0x00 | |
| | 0x1AB | | | AGCGAIN1 | R/W | AGCGAIN1[7:0] | | | | | | | | 0xF0 | |
| | 0x1AC | | | AGCGAIN2 | R/W | AGCGAIN2[7:0] | | | | | | | | 0xF0 | |
| | 0x1AD | | | AGCGAIN3 | R/W | AGCGAIN3[7:0] | | | | | | | | 0xF0 | |
| | 0x1AE | | | AGCGAIN4 | R/W | AGCGAIN4[7:0] | | | | | | | | 0xF0 | |
| | 0x1AF | | | VSH21 | R/W | RESERVED | VSH2 | | | RESERVED | VSH1 | | | | 0x00 |
| | 0x1B0 | | | VSH43 | R/W | RESERVED | VSH4 | | | RESERVED | VSH3 | | | | 0x00 |
| | 0x1B1~0x1B2 | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| | 0x1B3 | | | AADC0FS_H | R/W | AADC40FS[9:8] | | AADC30FS[9:8] | | AADC20FS[9:8] | | AADC10FS[9:8] | | | 0x00 |
| | 0x1B4 | | | AADC10FS_L | R/W | AADC10FS[7:0] | | | | | | | | 0x00 | |
| | 0x1B5 | | | AADC20FS_L | R/W | AADC20FS[7:0] | | | | | | | | 0x00 | |
| | 0x1B6 | | | AADC30FS_L | R/W | AADC30FS[7:0] | | | | | | | | 0x00 | |

TW6869

For Video Decoder and Audio Codec CH0~CH3. (*: Read only register/bit)

B[31:8] are hardwired to 0 in all registers.

| Address | | | | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default | | |
|-------------|-----|-----|-----|-------------|-----|------------------|-------------|----------------|------------|----------------|-------------|----------------|-------------|---------|------|------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | | | | | |
| 0x1B7 | | | | AADC4OFS_L | R/W | AADC4OFS[7:0] | | | | | | | | | 0x00 | |
| 0x1B8 | | | | AUDADC_H* | R | AUD4ADC[9:8]* | | AUD3ADC[9:8]* | | AUD2ADC[9:8]* | | AUD1ADC[9:8]* | | | 0x00 | |
| 0x1B9 | | | | AUD1ADC_L* | R | AUD1ADC[7:0]* | | | | | | | | | 0x00 | |
| 0x1BA | | | | AUD2ADC_L* | R | AUD2ADC[7:0]* | | | | | | | | | 0x00 | |
| 0x1BB | | | | AUD3ADC_L* | R | AUD3ADC[7:0]* | | | | | | | | | 0x00 | |
| 0x1BC | | | | AUD4ADC_L* | R | AUD4ADC[7:0]* | | | | | | | | | 0x00 | |
| 0x1BD | | | | ADJAADC_H* | R | ADJAADC4[9:8]* | | ADJAADC3[9:8]* | | ADJAADC2[9:8]* | | ADJAADC1[9:8]* | | | 0x00 | |
| 0x1BE | | | | ADJAADC1_L* | R | ADJAADC1[7:0]* | | | | | | | | | 0x00 | |
| 0x1BF | | | | ADJAADC2_L* | R | ADJAADC2[7:0]* | | | | | | | | | 0x00 | |
| 0x1C0 | | | | ADJAADC3_L* | R | ADJAADC3[7:0]* | | | | | | | | | 0x00 | |
| 0x1C1 | | | | ADJAADC4_L* | R | ADJAADC4[7:0]* | | | | | | | | | 0x00 | |
| 0x1C2~0x1CD | | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | |
| 0x1CE | | | | ANAPWDN | R/W | AAUTOMUTE | RESERVED | RESERVED | A_ADC_PWDN | V4_ADC_PWDN | V3_ADC_PWDN | V2_ADC_PWDN | V1_ADC_PWDN | 0x00 | | |
| 0x1CF | | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | | |
| 0x1D0 | | | | AIGAIN1 | R/W | 0 | AIGAIN1 | | | | | | | | | 0x20 |
| 0x1D1 | | | | AIGAIN2 | R/W | 0 | AIGAIN2 | | | | | | | | | 0x20 |
| 0x1D2 | | | | AIGAIN3 | R/W | 0 | AIGAIN3 | | | | | | | | | 0x20 |
| 0x1D3 | | | | AIGAIN4 | R/W | 0 | AIGAIN4 | | | | | | | | | 0x20 |
| 0x1D4~0x1DB | | | | RESERVED | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | | |
| 0x1DC | | | | MIX_MUTE | R/W | LAWMD | | MIX_DERATIO | MIX_MUTE | | | | | | 0x00 | |
| 0x1DD | | | | MIX_RATIO21 | R/W | MIX_RATIO2 | | | | MIX_RATIO1 | | | | | 0x00 | |
| 0x1DE | | | | MIX_RATIO43 | R/W | MIX_RATIO4 | | | | MIX_RATIO3 | | | | | 0x00 | |
| 0x1DF | | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | | |
| 0x1E0 | | | | MIX_OUTSEL | R/W | VADCCKPOL | AADCCKPOL | ADACCKPOL | MIX_OUTSEL | | | | | | 0x14 | |
| 0x1E1 | | | | ADET | R/W | AAAMPMD | ADET_FILTER | | | ADET_TH4[4] | ADET_TH3[4] | ADET_TH2[4] | ADET_TH1[4] | 0xC0 | | |
| 0x1E2 | | | | ADET_TH21 | R/W | ADET_TH2[3:0] | | | | ADET_TH1[3:0] | | | | | 0xAA | |
| 0x1E3 | | | | ADET_TH43 | R/W | ADET_TH4[3:0] | | | | ADET_TH3[3:0] | | | | | 0xAA | |
| 0x1E4 | | | | ADET_TH43 | R/W | 0 | AOFFCORE | DOUT_RST | DIV_RST | ACALEN | ASAVE[2:0] | | | | 0xAA | |
| 0x1E5~0x1FB | | | | RESERVED | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | | |
| 0x1FC | | | | AADC_TEST | R/W | 0 | ASYN SERIAL | AADC_PFTST | AINSWFIX | AINSWNUM | | | | | | 0x00 |
| 0x1FD | | | | VADC_TEST | R/W | 0 | 0 | 0 | 0 | 0 | VADC_PFTST | VADC_PFSEL | | | 0x00 | |
| 0x1FE | | | | DEV_ID_H* | R | DEV_ID[5:4]*: 0h | | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | | |
| 0x1FF | | | | DEV_ID_L* | R | DEV_ID[3:0]*: 7h | | | | 0 | 0 | 0 | 1 | 0x71 | | |

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For PCIe Endpoint Controller (*: Read only register/bit)

| Byte Offset Address | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default |
|---------------------|----------|-----------------|------|----------------------|------|------|------|------|------|------|---------|
| 0x00 | B3 | EP_HEADER_REG0* | R | DEVICE_ID* | | | | | | | 0x68 |
| | B2 | | | VENDOR_ID* | | | | | | | 0x64 |
| | B1 | | | | | | | | | | 0x17 |
| | B0 | | | | | | | | | | 0x97 |
| 0x04 | B3 | EP_HEADER_REG1 | R/W | STATUS_REG | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x10 |
| | B1 | | | COMMAND_REG | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x08 | B3 | EP_HEADER_REG2* | R | CLASS_CODE* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | REVISION_ID* | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x01 |
| 0x0C | B3 | EP_HEADER_REG3 | R/W | BIST* | | | | | | | 0x00 |
| | B2 | | | HEADER_TYPE* | | | | | | | 0x00 |
| | B1 | | | LATENCY_TIMER* | | | | | | | 0x00 |
| | B0 | | | CACHE_LINE_SIZE | | | | | | | 0x00 |
| 0x10 | B3 | EP_HEADER_REG4* | R | BASE_ADDRESS_REG0* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x08 |
| 0x14 | B3 | EP_HEADER_REG5* | R | BASE_ADDRESS_REG1* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x18 | B3 | EP_HEADER_REG6* | R | BASE_ADDRESS_REG2* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x1C | B3 | EP_HEADER_REG7* | R | BASE_ADDRESS_REG3* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x20 | B3 | EP_HEADER_REG8* | R | BASE_ADDRESS_REG4* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x24 | B3 | EP_HEADER_REG9* | R | BASE_ADDRESS_REG5* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x28 | B3 | EP_HEADER_REGA* | R | CARDBUS_CIS_POINTER* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x2C | B3 | EP_HEADER_REGB* | R | SUBSYSTEM_ID* | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | SUBSYSTEM_VENDOR_ID* | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |

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For PCIe Endpoint Controller (*: Read only register/bit)

| Byte Offset Address | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default | |
|---------------------|----------|-------------------|------|-------------------------|------|------|------|------|------|------|-------------------|------|
| 0x30 | B3 | EP_HEADER_REGC | R/W | EXPANSION_ROM_BASE_ADDR | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | 0x00 | |
| | B0 | | | | | | | | | | 0x00 | |
| 0x34 | B3 | EP_HEADER_REGD* | R* | RESERVED | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | 0x00 | |
| 0x38 | B3 | RESERVED | R | RESERVED | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | 0x00 | |
| | B0 | | | | | | | | | | 0x00 | |
| 0x3C | B3 | EP_HEADER_REGF* | R | RESERVED | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | INTERRUPT_PIN* | 0x01 |
| | B0 | | | | | | | | | | INTERRUPT_LINE* | 0xFF |
| 0x40 | B3 | EP_PM_CAP_REG0* | R | PMC* | | | | | | | 0xC9 | |
| | B2 | | | | | | | | | | 0xC3 | |
| | B1 | | | | | | | | | | NEXT_CAP_POINTER* | 0x50 |
| | B0 | | | | | | | | | | CAP_ID* | 0x01 |
| 0x44 | B3 | EP_PM_CAP_REG1 | R/W | DATA* | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | PMCSR_BSE_EXT* | 0x00 |
| | B0 | | | | | | | | | | PMCSR | 0x00 |
| 0x48~0x6C | B3 | RESERVED | | RESERVED | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | 0x00 | |
| | B0 | | | | | | | | | | 0x00 | |
| 0x70 | B3 | EP_PCIE_CAP_REG0* | R | PCIE_CAP_REG* | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x12 | |
| | B1 | | | | | | | | | | NEXT_CAP_POINTER* | 0x00 |
| | B0 | | | | | | | | | | CAP_ID* | 0x10 |
| 0x74 | B3 | EP_PCIE_CAP_REG1* | R | DEVICE_CAP* | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x00 | |
| | B1 | | | | | | | | | | 0x87 | |
| | B0 | | | | | | | | | | 0x22 | |
| 0x78 | B3 | EP_PCIE_CAP_REG2 | R/W | DEVICE_STATUS | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x10 | |
| | B1 | | | | | | | | | | 0x20 | |
| | B0 | | | | | | | | | | 0x10 | |
| 0x7C | B3 | EP_PCIE_CAP_REG3* | R | LINK_CAP* | | | | | | | 0x00 | |
| | B2 | | | | | | | | | | 0x07 | |
| | B1 | | | | | | | | | | 0x3C | |
| | B0 | | | | | | | | | | 0x11 | |
| 0x80 | B3 | EP_PCIE_CAP_REG4 | R/W | LINK_STATUS* | | | | | | | 0x10 | |
| | B2 | | | | | | | | | | 0x11 | |
| | B1 | | | | | | | | | | 0x00 | |
| | B0 | | | | | | | | | | 0x00 | |
| 0x80 | B3 | LINK_CONTROL | R/W | LINK_STATUS* | | | | | | | 0x10 | |
| | B2 | | | | | | | | | | 0x11 | |
| | B1 | | | | | | | | | | 0x00 | |
| | B0 | | | | | | | | | | 0x00 | |

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For PCIe Endpoint Controller (*: Read only register/bit)

| Byte Offset Address | Mnemonic | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | Default |
|---------------------|----------|------------------|------|------------------------------|------|------|------|------|------|------|---------|
| 0x84~0x9C | B3 | RESERVED | R | RESERVED | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x100 | B3 | EP_ERR_CAP_REG0* | R | ENHANCE_CAP_HEADER* | | | | | | | 0x14 |
| | B2 | | | | | | | | | | 0x01 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x01 |
| 0x104 | B3 | EP_ERR_CAP_REG1 | R/W | UNCORRECTABLE_ERROR_STATUS | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x108 | B3 | EP_ERR_CAP_REG2 | R/W | UNCORRECTABLE_ERROR_MASK | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x10C | B3 | EP_ERR_CAP_REG3 | R/W | UNCORRECTABLE_ERROR_SEVERITY | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x06 |
| | B1 | | | | | | | | | | 0x20 |
| | B0 | | | | | | | | | | 0x30 |
| 0x110 | B3 | EP_ERR_CAP_REG4 | R/W | CORRECTABLE_ERROR_STATUS | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x114 | B3 | EP_ERR_CAP_REG5 | R/W | CORRECTABLE_ERROR_MASK | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x20 |
| | B0 | | | | | | | | | | 0x00 |
| 0x118 | B3 | EP_ERR_CAP_REG6 | R/W | ADVANCE_ERROR_CAP_CONTROL | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0xA0 |
| 0x11C | B3 | EP_ERR_CAP_REG7 | R | HEADER_LOG_1ST_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x120 | B3 | EP_ERR_CAP_REG8 | R | HEADER_LOG_2ND_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x124 | B3 | EP_ERR_CAP_REG9 | R | HEADER_LOG_3RD_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |
| 0x128 | B3 | EP_ERR_CAP_REGA | R | HEADER_LOG_4TH_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | | 0x00 |

REGISTER DESCRIPTION

DMA Controller

| Index | | INT_STATUS | | | | | | | | Default |
|-------|----|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x00 | B3 | BAD_FMT_7 | BAD_FMT_6 | BAD_FMT_5 | BAD_FMT_4 | BAD_FMT_3 | BAD_FMT_2 | BAD_FMT_1 | BAD_FMT_0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | DMA_TOUT | 0 | 0x00 |
| | B1 | INTSTA_DMA15 | INTSTA_DMA14 | INTSTA_DMA13 | INTSTA_DMA12 | INTSTA_DMA11 | INTSTA_DMA10 | INTSTA_DMA9 | INTSTA_DMA8 | 0x00 |
| | B0 | INTSTA_DMA7 | INTSTA_DMA6 | INTSTA_DMA5 | INTSTA_DMA4 | INTSTA_DMA3 | INTSTA_DMA2 | INTSTA_DMA1 | INTSTA_DMA0 | 0x00 |

- BAD_FMT_7** B[31] Bad incoming data format flag of video input -7
 0 = no error detected
 1 = wrong format detected from the incoming data
 * This bit status is controlled by DMA_CONFIG[31:24]
 ** BAD_FMT = P_BAD | P_OV
 See register VIDEO_PARSER_STATUS
- BAD_FMT_6** B[30] Bad incoming data format flag of video input -6
- BAD_FMT_5** B[29] Bad incoming data format flag of video input -5
- BAD_FMT_4** B[28] Bad incoming data format flag of video input -4
- BAD_FMT_3** B[27] Bad incoming data format flag of video input -3
- BAD_FMT_2** B[26] Bad incoming data format flag of video input -2
- BAD_FMT_1** B[25] Bad incoming data format flag of video input -1
- BAD_FMT_0** B[24] Bad incoming data format flag of video input -0
-
- DMA_TOUT** B[17] Time out flag of DMA channels
-
- INTSTA_DMA[15:0]** B[15:0] Interrupt request from DMA Channel-15 to Channel 0
 0 = no interrupt
 1 = interrupt

| Index | | PB_STATUS | | | | | | | | Default |
|-------|----|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x01 | B3 | FFLAG_DMA7 | FFLAG_DMA6 | FFLAG_DMA5 | FFLAG_DMA4 | FFLAG_DMA3 | FFLAG_DMA2 | FFLAG_DMA1 | FFLAG_DMA0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | PBFLAG_DMA15 | PBFLAG_DMA14 | PBFLAG_DMA13 | PBFLAG_DMA12 | PBFLAG_DMA11 | PBFLAG_DMA10 | PBFLAG_DMA9 | PBFLAG_DMA8 | 0xFF |
| | B0 | PBFLAG_DMA7 | PBFLAG_DMA6 | PBFLAG_DMA5 | PBFLAG_DMA4 | PBFLAG_DMA3 | PBFLAG_DMA2 | PBFLAG_DMA1 | PBFLAG_DMA0 | 0xFF |

- FFLAG_DMA7 B[31] Field flag of DMA Channel-7
 0 = Field 1
 1 = Field 2
 * It is valid only under block DMA mode. See PHASE_REF
- FFLAG_DMA6 B[30] Field flag of DMA Channel-6
 FFLAG_DMA5 B[29] Field flag of DMA Channel-5
 FFLAG_DMA4 B[28] Field flag of DMA Channel-4
 FFLAG_DMA3 B[27] Field flag of DMA Channel-3
 FFLAG_DMA2 B[26] Field flag of DMA Channel-2
 FFLAG_DMA1 B[25] Field flag of DMA Channel-1
 FFLAG_DMA0 B[24] Field flag of DMA Channel-0
- PBFLAG_DMA15 B[15] PB flag of DMA Channel-15
 0 = P
 1 = B
- PBFLAG_DMA14 B[14] PB flag of DMA Channel-14
 PBFLAG_DMA13 B[13] PB flag of DMA Channel-13
 PBFLAG_DMA12 B[12] PB flag of DMA Channel-12
 PBFLAG_DMA11 B[11] PB flag of DMA Channel-11
 PBFLAG_DMA10 B[10] PB flag of DMA Channel-10
 PBFLAG_DMA9 B[9] PB flag of DMA Channel-9
 PBFLAG_DMA8 B[8] PB flag of DMA Channel-8
 PBFLAG_DMA7 B[7] PB flag of DMA Channel-7
 PBFLAG_DMA6 B[6] PB flag of DMA Channel-6
 PBFLAG_DMA5 B[5] PB flag of DMA Channel-5
 PBFLAG_DMA4 B[4] PB flag of DMA Channel-4
 PBFLAG_DMA3 B[3] PB flag of DMA Channel-3
 PBFLAG_DMA2 B[2] PB flag of DMA Channel-2
 PBFLAG_DMA1 B[1] PB flag of DMA Channel-1
 PBFLAG_DMA0 B[0] PB flag of DMA Channel-0

| Index | | DMA_CMD | | | | | | | | Default |
|-------|----|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x02 | B3 | DMA_ENABLE | BOND_OPT_1 | BOND_OPT_0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | RESET_DMA15 | RESET_DMA14 | RESET_DMA13 | RESET_DMA12 | RESET_DMA11 | RESET_DMA10 | RESET_DMA9 | RESET_DMA8 | 0xFF |
| | B0 | RESET_DMA7 | RESET_DMA6 | RESET_DMA5 | RESET_DMA4 | RESET_DMA3 | RESET_DMA2 | RESET_DMA1 | RESET_DMA0 | 0xFF |

- DMA_ENABLE B[31] General DMA enable bit
0 = stop
1 = start
- BOND_OPT B[30:29] Bonding status (READ ONLY)
- RESET_DMA16 B[16] Reset for DMA Channel-16
0 = reset
1 = normal
- RESET_DMA15 B[15] Reset for DMA Channel-15
- RESET_DMA14 B[14] Reset for DMA Channel-14
- RESET_DMA13 B[13] Reset for DMA Channel-13
- RESET_DMA12 B[12] Reset for DMA Channel-12
- RESET_DMA11 B[11] Reset for DMA Channel-11
- RESET_DMA10 B[10] Reset for DMA Channel-10
- RESET_DMA9 B[9] Reset for DMA Channel-9
- RESET_DMA8 B[8] Reset for DMA Channel-8
- RESET_DMA7 B[7] Reset for DMA Channel-7
- RESET_DMA6 B[6] Reset for DMA Channel-6
- RESET_DMA5 B[5] Reset for DMA Channel-5
- RESET_DMA4 B[4] Reset for DMA Channel-4
- RESET_DMA3 B[3] Reset for DMA Channel-3
- RESET_DMA2 B[2] Reset for DMA Channel-2
- RESET_DMA1 B[1] Reset for DMA Channel-1
- RESET_DMA0 B[0] Reset for DMA Channel-0

| Index | | FIFO_STATUS | | | | | | | | Default |
|-------|----|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x03 | B3 | OV7 | OV6 | OV5 | OV4 | OV3 | OV2 | OV1 | OV0 | 0x00 |
| | B2 | BAD_PTR_7 | BAD_PTR_6 | BAD_PTR_5 | BAD_PTR_4 | BAD_PTR_3 | BAD_PTR_2 | BAD_PTR_1 | BAD_PTR_0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | VDLOSS7 | VDLOSS6 | VDLOSS5 | VDLOSS4 | VDLOSS3 | VDLOSS2 | VDLOSS1 | VDLOSS0 | 0x00 |

- BAD_FMT_7** B[31] DMA FIFO overflow flag of DMA channel-7
 0 = no overflow
 1 = overflow
- BAD_FMT_6** B[30] DMA FIFO overflow flag of DMA Channel-6
- BAD_FMT_5** B[29] DMA FIFO overflow flag of DMA Channel -5
- BAD_FMT_4** B[28] DMA FIFO overflow flag of DMA Channel -4
- BAD_FMT_3** B[27] DMA FIFO overflow flag of DMA Channel -3
- BAD_FMT_2** B[26] DMA FIFO overflow flag of DMA Channel -2
- BAD_FMT_1** B[25] DMA FIFO overflow flag of DMA Channel -1
- BAD_FMT_0** B[24] DMA FIFO overflow flag of DMA Channel -0
-
- BAD_PTR_7** B[23] DMA FIFO pointer error in DMA Channel-7
 0 = no error
 1 = has error
- BAD_PTR_6** B[22] DMA FIFO pointer error in DMA Channel-6
- BAD_PTR_5** B[21] DMA FIFO pointer error in DMA Channel-5
- BAD_PTR_4** B[20] DMA FIFO pointer error in DMA Channel-4
- BAD_PTR_3** B[19] DMA FIFO pointer error in DMA Channel-3
- BAD_PTR_2** B[18] DMA FIFO pointer error in DMA Channel-2
- BAD_PTR_1** B[17] DMA FIFO pointer error in DMA Channel-1
- BAD_PTR_0** B[16] DMA FIFO pointer error in DMA Channel-0
-
- VDLOSS_7** B[7] Video signal lost for Channel-7
 0 = no error
 1 = has error
- VDLOSS_6** B[6] Video signal lost for Channel-6
- VDLOSS_5** B[5] Video signal lost for Channel-5
- VDLOSS_4** B[4] Video signal lost for Channel-4
- VDLOSS_3** B[3] Video signal lost for Channel-3
- VDLOSS_2** B[2] Video signal lost for Channel-2
- VDLOSS_1** B[1] Video signal lost for Channel-1
- VDLOSS_0** B[0] Video signal lost for Channel-0

| Index | | VIDEO_CHANNEL_ID | | | | | | | | Default |
|-------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x04 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 7 | | | 6 | | | 5 | | 0x92 |
| | B1 | 4 | | | 3 | | | | | 0x46 |
| | B0 | 2 | | 1 | | | 0 | | | 0x88 |

| Index | | VIDEO_PARSER_STATUS | | | | | | | | Default |
|-------|----|---------------------|--------|--------|--------|--------|--------|--------|--------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x05 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | P_OV7 | P_OV7 | P_OV7 | P_OV7 | P_OV7 | P_OV7 | P_OV7 | P_OV7 | 0x00 |
| | B0 | P_BAD7 | P_BAD6 | P_BAD5 | P_BAD4 | P_BAD3 | P_BAD2 | P_BAD1 | P_BAD0 | 0x00 |

P_OV7 **B[15]** Parser FIFO overflow flag for video input-7
P_OV6 **B[14]** Parser FIFO overflow flag for video input-6
P_OV5 **B[13]** Parser FIFO overflow flag for video input-5
P_OV4 **B[12]** Parser FIFO overflow flag for video input-4
P_OV3 **B[11]** Parser FIFO overflow flag for video input-3
P_OV2 **B[10]** Parser FIFO overflow flag for video input-2
P_OV1 **B[9]** Parser FIFO overflow flag for video input-1
P_OV0 **B[8]** Parser FIFO overflow flag for video input-0
 * These status bits are kept asserted until been read

P_BAD7 **B[7]** Parser found bad format at incoming video input-7
P_BAD 6 **B[6]** Parser found bad format at incoming video input-6
P_BAD 5 **B[5]** Parser found bad format at incoming video input-5
P_BAD 4 **B[4]** Parser found bad format at incoming video input-4
P_BAD 3 **B[3]** Parser found bad format at incoming video input-3
P_BAD 2 **B[2]** Parser found bad format at incoming video input-2
P_BAD 1 **B[1]** Parser found bad format at incoming video input-1
P_BAD 0 **B[0]** Parser found bad format at incoming video input-0
 * The status bits are kept asserted until been read

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| Index | | SYS_SOFT_RST | | | | | | | | Default |
|-------|----|--------------|-----|-----|-----|--------------|----------------|----------------|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x06 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | RESET_AV_REG | RESET_DMA_CTRL | RESET_DEC_INTF | RESET_EXT_PHY | 0x07 |

| | | |
|----------------|------|--|
| RESET_AV_REG | B[3] | Reset for registers of internal AV decoder. |
| RESET_DMA_CTRL | B[2] | Reset for DMA controller. |
| RESET_DEC_INTF | B[1] | Reset for decode interface. |
| RESET_EXT_PHY | B[0] | Reset for external PHY. It is a software reset, active low and self clear. |

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| Index | | DMA_PAGE_TABLE_ADDR | | | | | | | | Default |
|-------|----|------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x08 | B3 | PAGE_TABLE0_ADDR (Channel 0) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0x09 | B3 | PAGE_TABLE1_ADDR (Channel 0) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD0 | B3 | PAGE_TABLE0_ADDR (Channel 1) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD1 | B3 | PAGE_TABLE1_ADDR (Channel 1) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD2 | B3 | PAGE_TABLE0_ADDR (Channel 2) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD3 | B3 | PAGE_TABLE1_ADDR (Channel 2) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD4 | B3 | PAGE_TABLE0_ADDR (Channel 3) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD5 | B3 | PAGE_TABLE1_ADDR (Channel 3) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD6 | B3 | PAGE_TABLE0_ADDR (Channel 4) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD7 | B3 | PAGE_TABLE1_ADDR (Channel 4) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD8 | B3 | PAGE_TABLE0_ADDR (Channel 5) | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0xD9 | B3 | PAGE_TABLE1_ADDR (Channel 5) | | | | | | | | 0x00 |

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| Index | | DMA_PAGE_TABLE_ADDR | | | | | | | Default |
|-------|----|------------------------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xDA | B3 | PAGE_TABLE0_ADDR (Channel 6) | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xDB | B3 | PAGE_TABLE1_ADDR (Channel 6) | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xDC | B3 | PAGE_TABLE0_ADDR (Channel 7) | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xDD | B3 | PAGE_TABLE1_ADDR (Channel 7) | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

PAGE_TABLE0_ADDR B[31:0] The address of page0 table

PAGE_TABLE1_ADDR B[31:0] The address of page1 table

Driver needs to allocate 2 pages of Non-Pageable memory, and saves allocated addresses to these 2 registers for each video DMA channel

Each page is 4096-bytes continuously buffer.

Every 8-bytes (2 DWord) is called one Descriptor. Each page has 4096/8=512 video descriptors.

The following is the video descriptor's data structure (little endian format)

B[63:32] = target address of DMA

B[31:30] = descriptor status

0 = Host buffer unavailable

1 = Host buffer available

2 = This buffer has been filled by DMA successfully

3 = This buffer has been filled by DMA with error

B[29] = new frame flag

B[28:21] = do not care

B[20:14] = do not care

B[13] = do not care

B[12:0] = total byte length requirement

| Index | | DMA_CHANNEL_ENABLE | | | | | | | | Default |
|-------|----|--------------------|-----------|-----------|-----------|-----------|-----------|----------|-----------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x0A | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ENA_DMA16 | 0x00 |
| | B1 | ENA_DMA15 | ENA_DMA14 | ENA_DMA13 | ENA_DMA12 | ENA_DMA11 | ENA_DMA10 | ENA_DMA9 | ENA_DMA8 | 0x00 |
| | B0 | ENA_DMA7 | ENA_DMA6 | ENA_DMA5 | ENA_DMA4 | ENA_DMA3 | ENA_DMA2 | ENA_DMA1 | ENA_DMA0 | 0x00 |

| | | |
|-----------|-------|-----------------------|
| ENA_DMA16 | B[16] | Enable DMA Channel-16 |
| ENA_DMA15 | B[15] | Enable DMA Channel-15 |
| ENA_DMA14 | B[14] | Enable DMA Channel-14 |
| ENA_DMA13 | B[13] | Enable DMA Channel-13 |
| ENA_DMA12 | B[12] | Enable DMA Channel-12 |
| ENA_DMA11 | B[11] | Enable DMA Channel-11 |
| ENA_DMA10 | B[10] | Enable DMA Channel-10 |
| ENA_DMA9 | B[9] | Enable DMA Channel-9 |
| ENA_DMA8 | B[8] | Enable DMA Channel-8 |
| ENA_DMA7 | B[7] | Enable DMA Channel-7 |
| ENA_DMA6 | B[6] | Enable DMA Channel-6 |
| ENA_DMA5 | B[5] | Enable DMA Channel-5 |
| ENA_DMA4 | B[4] | Enable DMA Channel-4 |
| ENA_DMA3 | B[3] | Enable DMA Channel-3 |
| ENA_DMA2 | B[2] | Enable DMA Channel-2 |
| ENA_DMA1 | B[1] | Enable DMA Channel-1 |
| ENA_DMA0 | B[0] | Enable DMA Channel-0 |

| Index | | DMA_CONFIG | | | | | | | | Default |
|-------|----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0B | B3 | MASK_BAD_FMT7 | MASK_BAD_FMT6 | MASK_BAD_FMT5 | MASK_BAD_FMT4 | MASK_BAD_FMT3 | MASK_BAD_FMT2 | MASK_BAD_FMT1 | MASK_BAD_FMT0 | 0x00 |
| | B2 | MASK_BAD_PTR7 | MASK_BAD_PTR6 | MASK_BAD_PTR5 | MASK_BAD_PTR4 | MASK_BAD_PTR3 | MASK_BAD_PTR2 | MASK_BAD_PTR1 | MASK_BAD_PTR0 | 0x00 |
| | B1 | MASK_OV_7 | MASK_OV_6 | MASK_OV_5 | MASK_OV_4 | MASK_OV_3 | MASK_OV_2 | MASK_OV_1 | MASK_OV_0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | ENA_CPL_WAIT | ENA_INTX | 0 | BIG_ENDIAN | 0x04 |

MASK_BAD_FMT B[31:24] Mask bad format error of incoming data of DMA Channel
 0 = mask off, no report
 1 = ON

MASK_BAD_PTR B[23:16] Enable DMA FIFO pointer check of DMA Channel
 0 = mask off, no report
 1 = ON

MASK_OVF B[15:8] Enable DMA FIFO overflow check of DMA Channel
 0 = mask off, no report
 1 = ON

ENA_CPL_WAIT B[3] Wait for CPL done during initialization stage
 0 = disable
 1 = enable

ENA_INTX B[2] INTx enable, should be set to 1 by driver

BIG_ENDIAN B[0] Big endian enable
 0 = little endian
 1 = big endian

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| Index | | DMA_TIMER_INTERVAL | | | | | | | | Default |
|-------|----|---------------------|-----|----------------------|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x0C | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | DMA_INT_TIMER[21:16] | | | | | | 0x09 |
| | B1 | DMA_INT_TIMER[15:0] | | | | | | | | 0x89 |
| | B0 | | | | | | | | | 0x68 |

DMA_INT_TIMER B[21:0] Minimum time span for DMA interrupting host.

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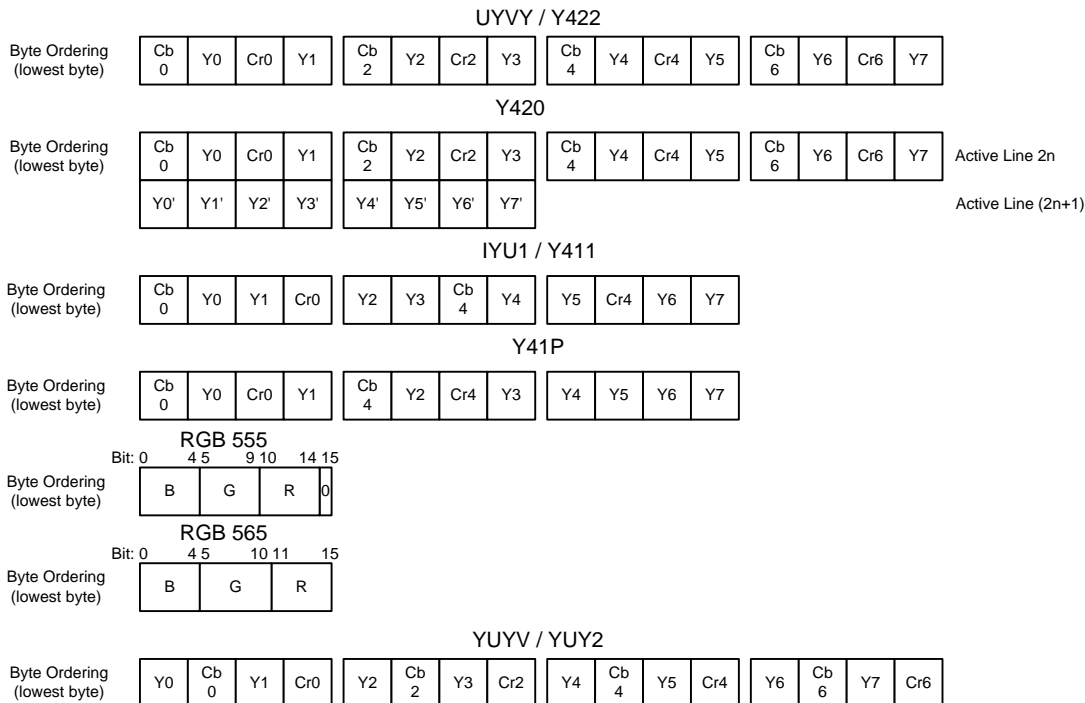
| Index | | DMA_CHANNEL_TIMEOUT | | | | | | | | Default |
|-------|----|--------------------------|-----|------------------|-----|--------------------------|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x0D | B3 | 0 | 0 | PRE_TIMEOUT_OFST | | | | | | 0x14 |
| | B2 | DMA_DAT_CH_TIMEOUT[11:4] | | | | | | | | 0x0C |
| | B1 | DMA_DAT_CH_TIMEOUT[3:0] | | | | DMA_VDO_CH_TIMEOUT[11:8] | | | | 0x85 |
| | B0 | DMA_VDO_CH_TIMEOUT[7:0] | | | | | | | | 0x84 |

PRE_TIMEOUT_OFST B[29:24] Offset from pre timeout to final timeout
DMA_DAT_CH_TIMEOUT B[23:12] Service timeout of each DMA data channel
DMA_VDO_CH_TIMEOUT B[11:0] Service timeout of each DMA video channel
 Note: It should be set a big value to avoid time out.

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| Index | | DMA_CHANNEL_CONFIG | | | | | | | Default |
|-------|----|---------------------|-------------------|---------------------|-------------------|---------------------|------------|------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x10 | B3 | VIN_MUX_SEL0 | FIELD_OUT0 | ENA_FIELD_DR OP0 | ENA_MASTER0 | MASTER_CHID0 | ENA_VDECIO | 0x00 | |
| | B2 | ENA_HDECIO | VIDEO_OUT_FORMAT0 | | END_IDX_DMA0[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA0[5:0] | | | | START_IDX_DMA0[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA0[7:0] | | | | | | | 0x00 |
| 0x11 | B3 | VIN_MUX_SEL1 | FIELD_OUT1 | ENA_FIELD_DR OP1 | ENA_MASTER1 | MASTER_CHID1 | ENA_VDEC1 | 0x00 | |
| | B2 | ENA_HDEC1 | VIDEO_OUT_FORMAT1 | | END_IDX_DMA1[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA1[5:0] | | | | START_IDX_DMA1[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA1[7:0] | | | | | | | 0x00 |
| 0x12 | B3 | VIN_MUX_SEL2 | FIELD_OUT2 | ENA_FIELD_DR OP2 | ENA_MASTER2 | MASTER_CHID2 | ENA_VDEC2 | 0x00 | |
| | B2 | ENA_HDEC2 | VIDEO_OUT_FORMAT2 | | END_IDX_DMA2[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA2[5:0] | | | | START_IDX_DMA2[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA2[7:0] | | | | | | | 0x00 |
| 0x13 | B3 | VIN_MUX_SEL3 | FIELD_OUT3 | ENA_FIELD_DR OP3 | ENA_MASTER3 | MASTER_CHID3 | ENA_VDEC3 | 0x00 | |
| | B2 | ENA_HDEC3 | VIDEO_OUT_FORMAT3 | | END_IDX_DMA3[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA3[5:0] | | | | START_IDX_DMA3[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA3[7:0] | | | | | | | 0x00 |
| 0x14 | B3 | VIN_MUX_SEL4 | FIELD_OUT4 | ENA_FIELD_DR OP4 | ENA_MASTER4 | MASTER_CHID4 | ENA_VDEC4 | 0x00 | |
| | B2 | ENA_HDEC4 | VIDEO_OUT_FORMAT4 | | END_IDX_DMA4[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA4[5:0] | | | | START_IDX_DMA4[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA4[7:0] | | | | | | | 0x00 |
| 0x15 | B3 | VIN_MUX_SEL5 | FIELD_OUT5 | ENA_FIELD_DR OP5 | ENA_MASTER5 | MASTER_CHID5 | ENA_VDEC5 | 0x00 | |
| | B2 | ENA_HDEC5 | VIDEO_OUT_FORMAT5 | | END_IDX_DMA5[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA5[5:0] | | | | START_IDX_DMA5[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA5[7:0] | | | | | | | 0x00 |
| 0x16 | B3 | VIN_MUX_SEL6 | FIELD_OUT6 | ENA_FIELD_DR OP6 | ENA_MASTER6 | MASTER_CHID6 | ENA_VDEC6 | 0x00 | |
| | B2 | ENA_HDEC6 | VIDEO_OUT_FORMAT6 | | END_IDX_DMA6[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA6[5:0] | | | | START_IDX_DMA6[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA6[7:0] | | | | | | | 0x00 |
| 0x17 | B3 | VIN_MUX_SEL7 | FIELD_OUT7 | ENA_FIELD_DR OP7 | ENA_MASTER7 | MASTER_CHID7 | ENA_VDEC7 | 0x00 | |
| | B2 | ENA_HDEC7 | VIDEO_OUT_FORMAT7 | | END_IDX_DMA7[9:6] | | | | 0x00 |
| | B1 | END_IDX_DMA7[5:0] | | | | START_IDX_DMA7[9:8] | | | 0x00 |
| | B0 | START_IDX_DMA7[7:0] | | | | | | | 0x00 |

| | | |
|------------------|----------|--|
| VIN_MUX_SEL | B[31:30] | Analog Mux input selection for build-in video decoder 1~4 respectively 0 = Select input 0 1 = Select input 1 2 = Select input 2 3 = Select input 3 |
| FIELD_OUT | B[29] | Which field dropped (applicable for master only) 0 = Field1 dropped 1 = Field2 dropped |
| ENA_FIELD_DROP | B[28] | Drop off field 0 = no drop 1 = drop |
| ENA_MASTER | B[27] | Master or slave 0 = slave 1 = master |
| MASTER_CHID | B[26:25] | Master channel # of the current one. For master channel, it is itself |
| ENA_VDECI | B[24] | Vertical (line) decimation 0 = No decimation 1 = 2:1 Decimation |
| ENA_HDECI | B[23] | Horizontal (pixel) decimation 0 = No decimation 1 = 2:1 Decimation |
| VIDEO_OUT_FORMAT | B[22:20] | Set output video format 000b = UYVY / Y422 001b = Y420 010b = IYU1 / Y411 011b = Y41P 100b = RGB 555 101b = RGB 565 110b = YUYV / YUY2 111b = Reserved |



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END_IDX_DMA B[19:10] end_idx of DMA
 START_IDX_DMA B[9: 0] start_idx of DMA

NOTE: B[29:25] are used for field dropping purpose.

(1) DMA0-3 and DMA4-7 are 2 big groups.

(2) Master means this DMA channel has higher priority to drop preferred field (odd/even), and slave means this channel is affected by master. Whenever master channel is sending data, it must drop the received.

| Index | DMA_PB_CONFIG | | | | | | | | Default |
|-------|---------------|-----|-----|-----|-----|-----|-----|-----|-------------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18 | DMA8_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x19 | DMA8_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x1A | DMA9_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x1B | DMA9_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x1C | DMAA_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x1D | DMAA_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x1E | DMAB_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x1F | DMAB_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x20 | DMAC_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x21 | DMAC_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x22 | DMAD_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x23 | DMAD_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x24 | DMAE_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x25 | DMAE_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x26 | DMAF_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x27 | DMAF_B_ADDR | | | | | | | | 0x0000_0000 |
| 0x28 | DMA10_P_ADDR | | | | | | | | 0x0000_0000 |
| 0x29 | DMA10_B_ADDR | | | | | | | | 0x0000_0000 |

DMA_P/B_ADDR [31:0] Starting addresses for DMA Channel-8 ~ Channel-16.
 Each Channel has 2 starting addresses for P-buffer and B-buffer respectively.
 These buffer addresses are allocated by Driver during initialization. They are called as Common Buffer. Driver needs to copy data from these buffers to their destination

| Index | | VIDEO_CONTROL1 | | | | | | | | Default |
|-------|----|----------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x2A | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | SYS_MODE_DMA7 | SYS_MODE_DMA6 | SYS_MODE_DMA5 | SYS_MODE_DMA4 | SYS_MODE_DMA3 | 0x00 |
| | B1 | SYS_MODE_DMA2 | SYS_MODE_DMA1 | SYS_MODE_DMA0 | 0 | 0 | VSCL_ENA_1 | 0 | 0 | 0x00 |
| | B0 | HACL_ENA_0 | VSCL_ENA_0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x01 |

SYS_MODE_DMA7 B[20] System mode for DMA Channel-7
 0 = 525 Lines
 1 = 625 Lines

SYS_MODE_DMA6 B[19] System mode for DMA Channel-6
SYS_MODE_DMA5 B[18] System mode for DMA Channel-5
SYS_MODE_DMA4 B[17] System mode for DMA Channel-4
SYS_MODE_DMA3 B[16] System mode for DMA Channel-3
SYS_MODE_DMA2 B[15] System mode for DMA Channel-2
SYS_MODE_DMA1 B[14] System mode for DMA Channel-1
SYS_MODE_DMA0 B[13] System mode for DMA Channel-0

B[10] set the input format of DMA Channel-4~Channel-7.

VSCL_ENA_1 B[10] Vertical scaler
 0 = Disabled
 1 = Enabled (360x240)

B[7:6] set the input format of DMA Channel-0~Channel-3.

HACL_ENA_0 B[7] Horizontal scaler
 0 = Disabled (full D1)
 1 = Enabled - 360x480(B[6]=0) or 360x240(B[6]=1)

VSCL_ENA_0 B[6] Vertical scaler
 0 = Disabled
 1 = Enabled (360x240) – B[7] must be “1”

| Index | | VIDEO_CONTROL2 | | | | | | | | Default |
|-------|----|----------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x2B | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | RST_GEN7 | RST_GEN6 | RST_GEN5 | RST_GEN4 | RST_GEN3 | RST_GEN2 | RST_GEN1 | RST_GEN0 | 0xFF |
| | B1 | PAT_SEL_GEN7 | PAT_SEL_GEN6 | PAT_SEL_GEN5 | PAT_SEL_GEN4 | PAT_SEL_GEN3 | PAT_SEL_GEN2 | PAT_SEL_GEN1 | PAT_SEL_GEN0 | 0x00 |
| | B0 | EXT_VDAT_ENA7 | EXT_VDAT_ENA6 | EXT_VDAT_ENA5 | EXT_VDAT_ENA4 | EXT_VDAT_ENA3 | EXT_VDAT_ENA2 | EXT_VDAT_ENA1 | EXT_VDAT_ENA0 | 0xFF |

- RST_GEN7** B[23] **Reset control for YUV Generator-7**
0 = reset
1 = not reset
- RST_GEN6** B[22] **Reset control for YUV Generator-6**
- RST_GEN5** B[21] **Reset control for YUV Generator-5**
- RST_GEN4** B[20] **Reset control for YUV Generator-4**
- RST_GEN3** B[19] **Reset control for YUV Generator-3**
- RST_GEN2** B[18] **Reset control for YUV Generator-2**
- RST_GEN1** B[17] **Reset control for YUV Generator-1**
- RST_GEN0** B[16] **Reset control for YUV Generator-0**
-
- PAT_SEL_GEN7** B[15] **Pattern selector for YUV Generator-7**
0 = Color Bar
1 = Sequenced Data
- PAT_SEL_GEN6** B[14] **Pattern selector for YUV Generator-6**
- PAT_SEL_GEN5** B[13] **Pattern selector for YUV Generator-5**
- PAT_SEL_GEN4** B[12] **Pattern selector for YUV Generator-4**
- PAT_SEL_GEN3** B[11] **Pattern selector for YUV Generator-3**
- PAT_SEL_GEN2** B[10] **Pattern selector for YUV Generator-2**
- PAT_SEL_GEN1** B[9] **Pattern selector for YUV Generator-1**
- PAT_SEL_GEN0** B[8] **Pattern selector for YUV Generator-0**
-
- EXT_VDAT_ENA7** B[7] **selection for each video DMA Channel-7**
0 = Use build in YUV Generator
1 = Use external inputs
- EXT_VDAT_ENA6** B[6] **selection for each video DMA Channel-6**
- EXT_VDAT_ENA5** B[5] **selection for each video DMA Channel-5**
- EXT_VDAT_ENA4** B[4] **selection for each video DMA Channel-4**
- EXT_VDAT_ENA3** B[3] **selection for each video DMA Channel-3**
- EXT_VDAT_ENA2** B[2] **selection for each video DMA Channel-2**
- EXT_VDAT_ENA1** B[1] **selection for each video DMA Channel-1**
- EXT_VDAT_ENA0** B[0] **selection for each video DMA Channel-0**

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| Index | | AUDIO_CONTROL1 | | | | | | | Default |
|-------|----|----------------------------|-------------|----------|-----|--------------------------|--------------|------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x2C | B3 | BYTE_LENGTH_DMA8TO16[12:5] | | | | | | | 0x80 |
| | B2 | BYTE_LENGTH_DMA8TO16[4:0] | | | | INT_GEN_ADAT_RATE[13:11] | | | 0x07 |
| | B1 | INT_GEN_ADAT_RATE[10:3] | | | | | | | 0xA1 |
| | B0 | INT_GEN_ADAT_RATE[2:0] | PAT_SEL_ADO | MIX_MODE | | | EXT_ADAT_ENA | 0x21 | |

- BYTE_LENGTH_DMA8TO16** B[31:19] Total byte length requirement of Audio DMA Channel-8 ~ Channel-16 (default: 4096 bytes)
- INT_GEN_ADAT_RATE** B[18:5] Internal audio generator sampling rate
For example, if sampling rate is 8k, the value should be 125M/8K = 15625 = 0x3d09 (default)
- PAT_SEL_ADO** B[4] Pattern selector for internal audio signal generator
0 = Sine wave
1 = Sequenced Data
- MIX_MODE** B[3:1] Mix mode of internal mixed audio generator
111b = output audio channel-7 data
....
000b = output audio channel-0 data
- EXT_ADAT_ENA** B[0] 0 = Use build-in sine waveform generator for Ch8-ChB
1 = Use external inputs

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| Index | | AUDIO_CONTROL2 | | | | | | | Default |
|-------|----|---------------------|-----|----------------------|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x2D | B3 | 0 | 0 | AUDIO_CLK_REF[29:24] | | | | | 0x3D |
| | B2 | | | | | | | | 0x09 |
| | B1 | AUDIO_CLK_REF[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

AUDIO_CLK_REF B[29:0] Audio sampling frequency reference
 $A_{ref} = (2^{24}) * 125\text{MHz} / (256 * F_s)$

| Sampling Rate (kHz) | Value (HEX) |
|------------------------|----------------|
| 8 | 0x3D09_0000 |
| 16 | 0x1E84_8000 |
| 32 | 0x0F42_4000 |
| 44.1 | 0x0B12_7795 |
| 48 | 0x0A2C_2AAA |

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| Index | | PHASE_REF | | | | | | | | Default |
|-------|----|----------------|-----|-----------------|-----|-----------|-----|-----------|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x2E | B3 | DMA_MODE7 | | DMA_MODE6 | | DMA_MODE5 | | DMA_MODE4 | | 0x00 |
| | B2 | DMA_MODE3 | | DMA_MODE2 | | DMA_MODE1 | | DMA_MODE0 | | 0x00 |
| | B1 | 0 | 0 | PHASE_REF[13:8] | | | | | | 0x14 |
| | B0 | PHASE_REF[7:0] | | | | | | | | 0x4D |

- DMA_MODE7** B[31:30] DMA mode configuration of DMA Channel-7
00b = S & G mode
01b = Reserved
10b = Frame mode
11b = Field mode
- DMA_MODE6** B[29:28] DMA mode configuration of DMA Channel-6
- DMA_MODE5** B[27:26] DMA mode configuration of DMA Channel-5
- DMA_MODE4** B[25:24] DMA mode configuration of DMA Channel-4
- DMA_MODE3** B[23:22] DMA mode configuration of DMA Channel-3
- DMA_MODE2** B[21:20] DMA mode configuration of DMA Channel-2
- DMA_MODE1** B[19:18] DMA mode configuration of DMA Channel-1
- DMA_MODE0** B[17:16] DMA mode configuration of DMA Channel-0
-
- PHASE_REF** B[13:0] Phase reference for rate conversion at each Video DMA channel. Valid range is [4800:5400].

| Index | | GPIO_REG | | | | | | | | Default |
|-------|----|----------|---------|---------|---------|---------|---------|---------|---------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x2F | B3 | GPP_C15 | GPP_C14 | GPP_C13 | GPP_C12 | GPP_C11 | GPP_C10 | GPP_C9 | GPP_C8 | 0xFF |
| | B2 | GPP_C7 | GPP_C6 | GPP_C5 | GPP_C4 | GPP_C3 | GPP_C2 | SDA_C1 | GPP_C0 | 0xFF |
| | B1 | GPP_D15 | GPP_D14 | GPP_D13 | GPP_D12 | GPP_D11 | GPP_D10 | GPP_D9 | GPP_D8 | 0x00 |
| | B0 | GPP_D7 | GPP_D6 | GPP_D5 | GPP_D4 | GPP_D3 | GPP_D2 | DPP_D1 | GPP_D0 | 0x00 |
| 0xE0 | B3 | GPP_C31 | GPP_C30 | GPP_C29 | GPP_DC8 | GPP_C27 | GPP_C26 | GPP_C25 | GPP_C24 | 0xFF |
| | B2 | GPP_C23 | GPP_C22 | GPP_C21 | GPP_DC0 | GPP_C19 | GPP_C18 | DPP_C17 | GPP_C16 | 0xFF |
| | B1 | GPP_D31 | GPP_D30 | GPP_D29 | GPP_D28 | GPP_D27 | GPP_D26 | GPP_D25 | GPP_D24 | 0x00 |
| | B0 | GPP_D23 | GPP_D22 | GPP_D21 | GPP_D20 | GPP_D19 | GPP_D18 | DPP_D17 | GPP_D16 | 0x00 |
| 0xE1 | B3 | GPP_C47 | GPP_C46 | GPP_C45 | GPP_C44 | GPP_C43 | GPP_C42 | GPP_C41 | GPP_C40 | 0xFF |
| | B2 | GPP_C39 | GPP_C38 | GPP_C37 | GPP_C36 | GPP_C35 | GPP_C34 | DPP_C33 | GPP_C32 | 0xFF |
| | B1 | GPP_D47 | GPP_D46 | GPP_D45 | GPP_D44 | GPP_D43 | GPP_D42 | GPP_D41 | GPP_D40 | 0x00 |
| | B0 | GPP_D39 | GPP_D38 | GPP_D37 | GPP_D36 | GPP_D35 | GPP_D34 | DPP_D33 | GPP_D32 | 0x00 |

GPP_Cn I/O control of GPIO pin
 0 = Pin is output
 1 = Pin is input

.....
 GPP_Dn GPIO pin

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| Index | | INTL_HBAR_CTRL | | | | | | | | Default |
|-------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x30 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR0 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR0 | | | | | | | | 0x0A |
| 0x31 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR1 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR1 | | | | | | | | 0x14 |
| 0x32 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR2 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR2 | | | | | | | | 0x1E |
| 0x33 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR3 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR3 | | | | | | | | 0x28 |
| 0x34 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR4 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR4 | | | | | | | | 0x32 |
| 0x35 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR5 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR5 | | | | | | | | 0x3C |
| 0x36 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR6 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR6 | | | | | | | | 0x46 |
| 0x37 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | HEIGHT_HBAR7 | | | | | | | | 0x0A |
| | B0 | ST_LINE_HBAR7 | | | | | | | | 0x50 |

HEIGHT_HBAR B[15:8] Height (lines) of horizontal bar.
 ST_LINE_HBAR B[7:0] Start line (position) of horizontal bar, ranges at [10 = 255]

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| Index | | AUDIO_CONTROL3 | | | | | | | | Default |
|-------|----|----------------|-----|-----|-----|-----|-----|-----|--------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x38 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OUT_BITWIDTH | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x40 |

OUT_BITWIDTH B[8] Audio DMA output bit width
 0 = 16 bits
 1 = 8 bits

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| Index | | VIDEO_FIELD_CTRL | | | | | | | Default |
|-------|----|--------------------|----------------|---------------------|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x39 | B3 | FLD_CTRL_ENA 0 | START_ FLD0 | FLD_OUT_OPT0[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT0[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3A | B3 | FLD_CTRL_ENA 1 | START_ FLD1 | FLD_OUT_OPT1[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT1[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3B | B3 | FLD_CTRL_ENA 2 | START_ FLD2 | FLD_OUT_OPT2[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT2[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3C | B3 | FLD_CTRL_ENA 3 | START_ FLD3 | FLD_OUT_OPT3[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT3[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3D | B3 | FLD_CTRL_ENA 4 | START_ FLD4 | FLD_OUT_OPT4[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT4[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3E | B3 | FLD_CTRL_ENA 5 | START_ FLD5 | FLD_OUT_OPT5[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT5[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x3F | B3 | FLD_CTRL_ENA 6 | START_ FLD6 | FLD_OUT_OPT6[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT6[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x40 | B3 | FLD_CTRL_ENA 7 | START_ FLD7 | FLD_OUT_OPT7[29:24] | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | FLD_OUT_OPT7[23:0] | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

FLD_CTRL_ENA B[31] Enable bit for each field control register
0 = output both odd and even field
1 = output according to B20~B0

START_FLD B[30] Starting field control bit
0 = starting from field 2
1 = starting from field 1

FLD_OUT_OPT B[29:0] Output flag of consecutive 30(NTSC)/25(PAL) fields.
0 = not output
1 = output

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| Index | | HSCALER_CTRL | | | | | | | Default |
|-------|----|---------------|------------------|-----|-----|------------|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x42 | B3 | HSCALER_ENA0 | PHASE_REF0[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF0[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF0[0] | END_POS0[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS0[2:0] | | | START_POS0 | | | 0xCA |
| 0x43 | B3 | HSCALER_ENA1 | PHASE_REF1[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF1[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF1[0] | END_POS1[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS1[2:0] | | | START_POS1 | | | 0xCA |
| 0x44 | B3 | HSCALER_ENA2 | PHASE_REF2[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF2[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF2[0] | END_POS2[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS2[2:0] | | | START_POS2 | | | 0xCA |
| 0x45 | B3 | HSCALER_ENA3 | PHASE_REF3[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF3[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF3[0] | END_POS3[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS3[2:0] | | | START_POS3 | | | 0xCA |
| 0x46 | B3 | HSCALER_ENA4 | PHASE_REF4[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF4[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF4[0] | END_POS4[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS4[2:0] | | | START_POS4 | | | 0xCA |
| 0x47 | B3 | HSCALER_ENA5 | PHASE_REF5[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF5[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF5[0] | END_POS5[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS5[2:0] | | | START_POS5 | | | 0xCA |
| 0x48 | B3 | HSCALER_ENA6 | PHASE_REF6[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF6[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF6[0] | END_POS6[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS6[2:0] | | | START_POS6 | | | 0xCA |
| 0x49 | B3 | HSCALER_ENA7 | PHASE_REF7[15:9] | | | | | | 0x7C |
| | B2 | | PHASE_REF7[8:1] | | | | | | 0x71 |
| | B1 | PHASE_REF7[0] | END_POS7[9:3] | | | | | | 0xD8 |
| | B0 | | END_POS7[2:0] | | | START_POS7 | | | 0xCA |

HSCALER_ENA B[31] Customize horizontal scaler enable bit
 0 = disable
 1 = enable

PHASE_REF B[30:15] Scaler phase reference. Its calculation is
 $Phase_ref = (END_POS - START_POS) * (2^{16}) / Total_Active_Pixel_Per_Line$
 For example,
 START_POS = 10, END_POS = 710,
 Total_Active_Pixel_Per_Line = 720,
 $Phase_ref = (710 - 10) * 2^{16} / 720 = 0xF8E3$

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| | | |
|-----------|---------|---|
| END_POS | B[14:5] | End pixel position of each line. This pixel will NOT be shown and the setting must be an even number. |
| START_POS | B[4:0] | Start pixel position of each line. This pixel will be shown and the setting must be an even number. |

| Index | | VIDEO_SIZE | | | | | | | | Default |
|-------|----|--------------|-----------|-----|-----|-----|---------------|-----|------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x4A | B3 | VS_EN0 | VS_F2_EN0 | 0 | 0 | 0 | 0 | 0 | V_SIZE0[8] | 0x00 |
| | B2 | V_SIZE0[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE0[10:8] | | | 0x02 |
| | B0 | H_SIZE0[7:0] | | | | | | | | 0xD0 |
| 0x4B | B3 | VS_EN1 | VS_F2_EN1 | 0 | 0 | 0 | 0 | 0 | V_SIZE1[8] | 0x00 |
| | B2 | V_SIZE1[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE1[10:8] | | | 0x02 |
| | B0 | H_SIZE1[7:0] | | | | | | | | 0xD0 |
| 0x4C | B3 | VS_EN2 | VS_F2_EN2 | 0 | 0 | 0 | 0 | 0 | V_SIZE2[8] | 0x00 |
| | B2 | V_SIZE2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE2[10:8] | | | 0x02 |
| | B0 | H_SIZE2[7:0] | | | | | | | | 0xD0 |
| 0x4D | B3 | VS_EN3 | VS_F2_EN3 | 0 | 0 | 0 | 0 | 0 | V_SIZE3[8] | 0x00 |
| | B2 | V_SIZE3[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE3[10:8] | | | 0x02 |
| | B0 | H_SIZE3[7:0] | | | | | | | | 0xD0 |
| 0x4E | B3 | VS_EN4 | VS_F2_EN4 | 0 | 0 | 0 | 0 | 0 | V_SIZE4[8] | 0x00 |
| | B2 | V_SIZE4[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE4[10:8] | | | 0x02 |
| | B0 | H_SIZE4[7:0] | | | | | | | | 0xD0 |
| 0x4F | B3 | VS_EN5 | VS_F2_EN5 | 0 | 0 | 0 | 0 | 0 | V_SIZE5[8] | 0x00 |
| | B2 | V_SIZE5[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE5[10:8] | | | 0x02 |
| | B0 | H_SIZE5[7:0] | | | | | | | | 0xD0 |
| 0x50 | B3 | VS_EN6 | VS_F2_EN6 | 0 | 0 | 0 | 0 | 0 | V_SIZE6[8] | 0x00 |
| | B2 | V_SIZE6[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE6[10:8] | | | 0x02 |
| | B0 | H_SIZE6[7:0] | | | | | | | | 0xD0 |
| 0x51 | B3 | VS_EN7 | VS_F2_EN7 | 0 | 0 | 0 | 0 | 0 | V_SIZE7[8] | 0x00 |
| | B2 | V_SIZE7[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE7[10:8] | | | 0x02 |
| | B0 | H_SIZE7[7:0] | | | | | | | | 0xD0 |

| | | |
|----------|----------|---|
| VS_EN | B[31] | Customize video size enable bit 0 = disable 1 = enable |
| VS_F2_EN | B[30] | Enable to field 2 video size control registers 0 = Field 2 video size controlled by VIDEO_SIZE _x 1 = Field 2 video size controlled by VIDEO_SIZE _{x_F2} |
| V_SIZE | B[24:16] | Height of field. |
| H_SIZE | B[10:0] | Width of field |

Note: “x” means DMA channel number (0~7)

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| Index | | VIDEO_SIZE_F2 | | | | | | | | Default |
|-------|----|-----------------|-----|-----|-----|-----|------------------|-----|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x52 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE0_F2[8] | 0x00 |
| | B2 | V_SIZE0_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE0_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE0_F2[7:0] | | | | | | | | 0xD0 |
| 0x53 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE1_F2[8] | 0x00 |
| | B2 | V_SIZE1_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE1_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE1_F2[7:0] | | | | | | | | 0xD0 |
| 0x54 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE2_F2[8] | 0x00 |
| | B2 | V_SIZE2_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE2_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE2_F2[7:0] | | | | | | | | 0xD0 |
| 0x55 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE3_F2[8] | 0x00 |
| | B2 | V_SIZE3_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE3_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE3_F2[7:0] | | | | | | | | 0xD0 |
| 0x56 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE4_F2[8] | 0x00 |
| | B2 | V_SIZE4_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE4_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE4_F2[7:0] | | | | | | | | 0xD0 |
| 0x57 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE5_F2[8] | 0x00 |
| | B2 | V_SIZE5_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE5_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE5_F2[7:0] | | | | | | | | 0xD0 |
| 0x58 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE6_F2[8] | 0x00 |
| | B2 | V_SIZE6_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE6_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE6_F2[7:0] | | | | | | | | 0xD0 |
| 0x59 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_SIZE7_F2[8] | 0x00 |
| | B2 | V_SIZE7_F2[7:0] | | | | | | | | 0xF0 |
| | B1 | 0 | 0 | 0 | 0 | 0 | H_SIZE7_F2[10:8] | | | 0x02 |
| | B0 | H_SIZE7_F2[7:0] | | | | | | | | 0xD0 |

V_SIZE_F2
H_SIZE_F2

B[24:16]
B[10:0]

Height of field 2.
Width of field 2.

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| Index | MD_CONF | | | | | | | | Default | |
|-------|---------|---------------------|-----|------------|-------------|----------|----------------------|-----|---------|------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | | |
| 0x60 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD0_TSCALE | | MD0_ENABLE | MD0_ACT_FLD | MD0_MODE | MD0_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD0_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD0_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x61 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD1_TSCALE | | MD1_ENABLE | MD1_ACT_FLD | MD1_MODE | MD1_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD1_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD1_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x62 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD2_TSCALE | | MD2_ENABLE | MD2_ACT_FLD | MD2_MODE | MD2_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD2_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD2_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x63 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD3_TSCALE | | MD3_ENABLE | MD3_ACT_FLD | MD3_MODE | MD3_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD3_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD3_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x64 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD4_TSCALE | | MD4_ENABLE | MD4_ACT_FLD | MD4_MODE | MD4_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD4_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD4_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x65 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD5_TSCALE | | MD5_ENABLE | MD5_ACT_FLD | MD5_MODE | MD5_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD5_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD5_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x66 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD6_TSCALE | | MD6_ENABLE | MD6_ACT_FLD | MD6_MODE | MD6_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD6_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD6_THRESHOLD[7:0] | | | | | | | | 0x10 |
| 0x67 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD7_TSCALE | | MD7_ENABLE | MD7_ACT_FLD | MD7_MODE | MD7_THRESHOLD[17:16] | | | 0x05 |
| | B1 | MD7_THRESHOLD[15:8] | | | | | | | | 0x04 |
| | B0 | MD7_THRESHOLD[7:0] | | | | | | | | 0x10 |

| | | |
|-------------|----------|---|
| MD_TSCALE | B[23:21] | Scale amount of threshold (T<<TSCALE) |
| MD_ENABLE | B[20] | Enable Motion Detection 0: disable 1: enable |
| MD_ACT_FLD | B [19] | Motion Detection Active Field 0: Field 0 1: Field 1 |
| MD_MODE | B [18] | Motion Detection Block Size 0: Block size is 16x16 1: Block size is 32x32 |
| MD_TRESHOLD | B[17:0] | Threshold for Motion or Static |

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| Index | | MD_INIT | | | | | | | | Default |
|-------|----|---------|-----|-----|-----|-----|-----|-----|----------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x68 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD0_INIT | 0x00 |
| 0x69 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD1_INIT | 0x00 |
| 0x6A | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD2_INIT | 0x00 |
| 0x6B | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD3_INIT | 0x00 |
| 0x6C | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD4_INIT | 0x00 |
| 0x6D | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD5_INIT | 0x00 |
| 0x6E | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD6_INIT | 0x00 |
| 0x6F | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD7_INIT | 0x00 |

MD_INIT

B[0]

Motion Detection Read Pointer Initialization. By Writing any value to it, the read pointer will be reset.

| Index | | MD_MAPO | | | | | | | | Default |
|-------|----|-----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x70 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD0_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD0_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD0_MAPO[7:0] | | | | | | | | 0x00 |
| 0x71 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD1_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD1_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD1_MAPO[7:0] | | | | | | | | 0x00 |
| 0x72 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD2_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD2_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD2_MAPO[7:0] | | | | | | | | 0x00 |
| 0x73 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD3_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD3_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD3_MAPO[7:0] | | | | | | | | 0x00 |
| 0x74 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD4_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD4_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD4_MAPO[7:0] | | | | | | | | 0x00 |
| 0x75 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD5_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD5_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD5_MAPO[7:0] | | | | | | | | 0x00 |
| 0x76 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD6_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD6_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD6_MAPO[7:0] | | | | | | | | 0x00 |
| 0x77 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | MD7_MAPO[23:16] | | | | | | | | 0x00 |
| | B1 | MD7_MAPO[15:8] | | | | | | | | 0x00 |
| | B0 | MD7_MAPO[7:0] | | | | | | | | 0x00 |

MD_MAPO B[23:0] Map of motion detection output for blocks of current slice.

Note: Video Frame is partitioned into multiple slices (Number of vertical blocks). After MD_INIT, the output of first slice will be read through one register read operation and read pointer will be moved to the next slice. Host can issue read command until all the slices have been read. MD_MAPO[0] maps to the first block in current slice.

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| Index | | ADDR_P_DMA | | | | | | | Default |
|-------|----|-------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x80 | B3 | ADDR_P_DMA0 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x88 | B3 | ADDR_P_DMA1 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x90 | B3 | ADDR_P_DMA2 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x98 | B3 | ADDR_P_DMA3 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xA0 | B3 | ADDR_P_DMA4 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xA8 | B3 | ADDR_P_DMA5 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xB0 | B3 | ADDR_P_DMA6 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xB8 | B3 | ADDR_P_DMA7 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

ADDR_P_DMA B[31:0] Start address of P-buffer for DMA Channel-0 ~ Channel-7.

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| Index | WHP_DMA | | | | | | | | Default | |
|-------|---------|--------------------|-------------------|-----|-----|---------------------|-----|-----|---------|------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | | |
| 0x81 | B3 | HEIGHT0[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT0[1:0] | LINE_WIDTH0[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH0 [4:0] | | | | ACTIVE_WIDTH0[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH0[7:0] | | | | | | | | 0xA0 |
| 0x89 | B3 | HEIGHT1[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT1[1:0] | LINE_WIDTH1[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH1[4:0] | | | | ACTIVE_WIDTH1[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH1[7:0] | | | | | | | | 0xA0 |
| 0x91 | B3 | HEIGHT2[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT2[1:0] | LINE_WIDTH2[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH2[4:0] | | | | ACTIVE_WIDTH2[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH2[7:0] | | | | | | | | 0xA0 |
| 0x99 | B3 | HEIGHT3[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT3[1:0] | LINE_WIDTH3[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH3[4:0] | | | | ACTIVE_WIDTH3[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH3[7:0] | | | | | | | | 0xA0 |
| 0xA1 | B3 | HEIGHT4[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT4[1:0] | LINE_WIDTH4[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH4[4:0] | | | | ACTIVE_WIDTH4[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH4[7:0] | | | | | | | | 0xA0 |
| 0xA9 | B3 | HEIGHT5[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT5[1:0] | LINE_WIDTH5[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH5[4:0] | | | | ACTIVE_WIDTH5[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH5[7:0] | | | | | | | | 0xA0 |
| 0xB1 | B3 | HEIGHT6[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT6[1:0] | LINE_WIDTH6[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH6[4:0] | | | | ACTIVE_WIDTH6[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH6[7:0] | | | | | | | | 0xA0 |
| 0xB9 | B3 | HEIGHT7[9:2] | | | | | | | | 0x3C |
| | B2 | HEIGHT7[1:0] | LINE_WIDTH7[10:5] | | | | | | | 0x2E |
| | B1 | LINE_WIDTH7[4:0] | | | | ACTIVE_WIDTH7[10:8] | | | | 0xA5 |
| | B0 | ACTIVE_WIDTH7[7:0] | | | | | | | | 0xA0 |

For DMA Channel-0~Channel-7:

HEIGHT B[31:22] Total active lines
 LINE_WIDTH B[21:11] Total bytes per line
 ACTIVE_WIDTH B[10:0] Total active bytes per line

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| Index | | ADDR_B_DMA | | | | | | | Default |
|-------|----|-------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x82 | B3 | ADDR_B_DMA0 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x8A | B3 | ADDR_B_DMA1 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x92 | B3 | ADDR_B_DMA2 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x9A | B3 | ADDR_B_DMA3 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xA2 | B3 | ADDR_B_DMA4 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xAA | B3 | ADDR_B_DMA5 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xB2 | B3 | ADDR_B_DMA6 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xBA | B3 | ADDR_B_DMA7 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

ADDR_B_DMA B[31:0] Start address of B-buffer for DMA Channel-0 ~ Channel-7.

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| Index | | F2_ADDR_P_DMA | | | | | | | Default |
|-------|----|----------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x84 | B3 | F2_ADDR_P_DMA0 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x8C | B3 | F2_ADDR_P_DMA1 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x94 | B3 | F2_ADDR_P_DMA2 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x9C | B3 | F2_ADDR_P_DMA3 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xA4 | B3 | F2_ADDR_P_DMA4 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xAC | B3 | F2_ADDR_P_DMA5 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xB4 | B3 | F2_ADDR_P_DMA6 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xBC | B3 | F2_ADDR_P_DMA7 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

F2_ADDR_P_DMA B[31:0] Start address of Field 2 P-buffer for DMA Channel-0 ~ Channel-7.

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| Index | F2_WHP_DMA | | | | | | | | Default | |
|-------|------------|-----------------------|----------------------|-----|-----|------------------------|-----|-----|---------|------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | | |
| 0x85 | B3 | F2_HEIGHT0[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT0[1:0] | F2_LINE_WIDTH0[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH0 [4:0] | | | | F2_ACTIVE_WIDTH0[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH0[7:0] | | | | | | | | 0xA0 |
| 0x8D | B3 | F2_HEIGHT1[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT1[1:0] | F2_LINE_WIDTH1[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH1[4:0] | | | | F2_ACTIVE_WIDTH1[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH1[7:0] | | | | | | | | 0xA0 |
| 0x95 | B3 | F2_HEIGHT2[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT2[1:0] | F2_LINE_WIDTH2[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH2[4:0] | | | | F2_ACTIVE_WIDTH2[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH2[7:0] | | | | | | | | 0xA0 |
| 0x9D | B3 | F2_HEIGHT3[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT3[1:0] | F2_LINE_WIDTH3[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH3[4:0] | | | | F2_ACTIVE_WIDTH3[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH3[7:0] | | | | | | | | 0xA0 |
| 0xA5 | B3 | F2_HEIGHT4[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT4[1:0] | F2_LINE_WIDTH4[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH4[4:0] | | | | F2_ACTIVE_WIDTH4[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH4[7:0] | | | | | | | | 0xA0 |
| 0xAD | B3 | F2_HEIGHT5[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT5[1:0] | F2_LINE_WIDTH5[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH5[4:0] | | | | F2_ACTIVE_WIDTH5[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH5[7:0] | | | | | | | | 0xA0 |
| 0xB5 | B3 | F2_HEIGHT6[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT6[1:0] | F2_LINE_WIDTH6[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH6[4:0] | | | | F2_ACTIVE_WIDTH6[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH6[7:0] | | | | | | | | 0xA0 |
| 0xBD | B3 | F2_HEIGHT7[9:2] | | | | | | | | 0x3C |
| | B2 | F2_HEIGHT7[1:0] | F2_LINE_WIDTH7[10:5] | | | | | | | 0x2E |
| | B1 | F2_LINE_WIDTH7[4:0] | | | | F2_ACTIVE_WIDTH7[10:8] | | | | 0xA5 |
| | B0 | F2_ACTIVE_WIDTH7[7:0] | | | | | | | | 0xA0 |

For DMA Channel-0~Channel-7:

F2_HEIGHT B[31:22] Total active lines in field 2
F2_LINE_WIDTH B[21:11] Total bytes per line in field 2
F2_ACTIVE_WIDTH B[10:0] Total active bytes per line in field 2

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| Index | | F2_ADDR_B_DMA | | | | | | | Default |
|-------|----|----------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x86 | B3 | F2_ADDR_B_DMA0 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x8E | B3 | F2_ADDR_B_DMA1 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x96 | B3 | F2_ADDR_B_DMA2 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x9E | B3 | F2_ADDR_B_DMA3 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xA6 | B3 | F2_ADDR_B_DMA4 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xAE | B3 | F2_ADDR_B_DMA5 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xB6 | B3 | F2_ADDR_B_DMA6 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0xBE | B3 | F2_ADDR_B_DMA7 | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

F2_ADDR_P_DMA B[31:0] Start address of Field 2 B-buffer for DMA Channel-0 ~ Channel-7.

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| Index | | RG_NRDET_CFG | | | | | | | | Default |
|-------|----|-----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0xC0 | B3 | RG_NRDET_PARA3 | | | | | | | | 0x14 |
| | B2 | RG_NRDET_PARA2 | | | | | | | | 0x32 |
| | B1 | RG_NRDET_PARA1 | | | | | | | | 0x3C |
| | B0 | RG_NRDET_PARA0 | | | | | | | | 0xAA |
| 0xC1 | B3 | RG_NRDET_PARA7 | | | | | | | | 0x14 |
| | B2 | RG_NRDET_PARA6 | | | | | | | | 0x14 |
| | B1 | RG_NRDET_PARA5 | | | | | | | | 0xA5 |
| | B0 | RG_NRDET_PARA4 | | | | | | | | 0x28 |
| 0xC2 | B3 | RG_NRDET_PARA11 | | | | | | | | 0x28 |
| | B2 | RG_NRDET_PARA10 | | | | | | | | 0xA5 |
| | B1 | RG_NRDET_PARA9 | | | | | | | | 0xAA |
| | B0 | RG_NRDET_PARA8 | | | | | | | | 0x0F |
| 0xC3 | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | RG_NRDET_PARA14 | | | | | | | | 0x0F |
| | B1 | RG_NRDET_PARA13 | | | | | | | | 0x14 |
| | B0 | RG_NRDET_PARA12 | | | | | | | | 0xAA |

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| Index | | RG_NRDET_CFG | | | | | | | Default |
|-------|----|--------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0xC4 | B3 | RG_NR2D_THD4 | | | | | | | 0x0F |
| | B2 | RG_NR2D_THD3 | | | | | | | 0x08 |
| | B1 | RG_NR2D_THD2 | | | | | | | 0x0A |
| | B0 | RG_NR2D_THD1 | | | | | | | 0x05 |
| 0xC5 | B3 | RG_NR2D_THD8 | | | | | | | 0xF0 |
| | B2 | RG_NR2D_THD7 | | | | | | | 0x19 |
| | B1 | RG_NR2D_THD6 | | | | | | | 0x25 |
| | B0 | RG_NR2D_THD5 | | | | | | | 0x19 |

These registers are used to configure NR2D detection thresholds.

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| Index | | PIN_CFG_CTRL | | | | | | | | Default |
|-------|----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0xFB | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | ACH7 DTEST | ACH6 DTEST | ACH5 DTEST | ACH4 DTEST | ACH3 DTEST | ACH2 DTEST | ACH1 DTEST | ACH0 DTEST | 0x00 |
| | B1 | VCH7 DTEST | VCH6 DTEST | VCH5 DTEST | VCH4 DTEST | VCH3 DTEST | VCH2 DTEST | VCH0 DTEST | VCH0 DTEST | 0x00 |
| | B0 | 0 | 0 | | 0 | 0 | 0 | Mode1 | Mode0 | 0xA0 |

This register is cleared to default value only by hardware reset.

- ACHDTEST B[23:16] Audio codec input data selection
 - 0 = From internal AFE
 - 1 = From external Pin

- VCHDTEST B[15:8] Video Decoder input data selection
 - 0 = From internal AFE
 - 1 = From external Pin

- Mode B[1:0] Pin configuration
 - 0 = JTAG Enable
 - 1 = Debug Port Enable
 - 2 = Full GPIO
 - 3 = External ADC input data

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| Index | | DBGPORT_CTRL | | | | | | | | Default |
|-------|----|---------------|-----------|-----|-----|-----|-----|-----|------|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0xFC | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | MSB16_EN | BLOCK_SEL | | | | | | | 0x00 |
| | B0 | SUBMODULE_SEL | | | | | | | 0x00 | |

MSB16_EN B[15] Enable MSB 16 bits of debug signal at output ports
0 = disable (so LSB 16 bits are wired to ports)
1 = enable

BLOCK_SEL B[14:8] Block selection for debug port output
SUBMODULE_SEL B[7:0] Sub-module of block selection

| BLOCK_SEL | SUBMODULE_SEL | DEBUG PORTS |
|-----------|---------------|----------------------|
| 0 | 0x0 | PIPE Interface |
| | 0x1 | PCIE EndPoint |
| | 0x2 | PCIE EndPoint |
| | 0x3 | Status of DMA Parser |
| | 0x4 | I2S Receiver |
| 1 | 0x0 | DMA_CH0 |
| | 0x1 | DMA_CH1 |
| | 0x2 | DMA_CH2 |
| | 0x3 | DMA_CH3 |
| | 0x4 | DMA_CH4 |
| | 0x5 | DMA_CH5 |
| | 0x6 | DMA_CH6 |
| | 0x7 | DMA_CH7 |
| | 0x8 | DMA_CH8 |
| | 0x9 | DMA_CH9 |
| | 0xA | DMA_CH10 |
| | 0xB | DMA_CH11 |
| | 0xC | DMA_CH12 |
| | 0xD | DMA_CH13 |
| | 0xE | DMA_CH14 |
| 0xF | DMA_CH15 | |
| 0x10 | Schedule | |
| 0x11 | MSI | |
| 0x12 | Client | |
| 0x13 | Cpl | |
| 0x14 | DMA_CH16 | |
| 2 | 0x0 | Parser1 |
| | 0x1 | Parser2 |
| | 0x2 | Parser3 |
| | 0x3 | Parser4 |
| | 0x4 | Parser5 |
| | 0x5 | Parser6 |
| | 0x6 | Parser7 |
| | 0x7 | Parser8 |

| Index | | EP_REG_ADDR | | | | | | | | Default |
|-------|----|-------------|-----|-----|-----|-------------|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0xFE | B3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| | B1 | 0 | 0 | 0 | 0 | EP_REG_ADDR | | | | 0x00 |
| | B0 | EP_REG_ADDR | | | | | | | | 0x00 |

EP_REG_ADDR B[11:0] Address of PCIE_EP core register
 Note: DWORD aligned

| Index | | EP_REG_DATA | | | | | | | | Default |
|-------|----|-------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0xFF | B3 | EP_REG_DATA | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

EP_REG_DATA B[31:0] Data read from or write to PCIE_EP core register
 Note:
 (1) It must follow EP_REG_ADDR, and couldn't be used alone.
 (2) Write steps:
 (a) write target PCIE_EP register address to "EP_REG_ADDR";
 (b) write target data to "EP_REG_DATA".
 (3) Read steps:
 (a) write target PCIE_EP register address to "EP_REG_ADDR";
 (b) read data from "EP_REG_DATA".

Video Decoder & Audio Codec (CH0 ~ CH3)

(Starting from 0x100)

(B[31:8] are hardwired to 0 in all registers)

| Index | | | | VIDEO STATUS REGISTER | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------|-------|-------|-------|-------|-----|------|-------|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x100 | 0x110 | 0x120 | 0x130 | VDLOSS | HLOCK | SLOCK | FIELD | VLOCK | 0 | MONO | DET50 | 0x00 |

VDLOSS B[7] 1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register)
0 = Video detected.

HLOCK B[6] 1 = Horizontal sync PLL is locked to the incoming video source.
0 = Horizontal sync PLL is not locked.

SLOCK B[5] 1 = Sub-carrier PLL is locked to the incoming video source.
0 = Sub-carrier PLL is not locked.

FIELD B[4] 0 = Odd field is being decoded.
1 = Even field is being decoded.

VLOCK B[3] 1 = Vertical logic is locked to the incoming video source.
0 = Vertical logic is not locked.

MONO B[1] 1 = No color burst signal detected.
0 = Color burst signal detected.

DET50 B[0] 0 = 60Hz source detected
1 = 50Hz source detected
The actual vertical scanning frequency depends on the current standard invoked.

| Index | | | | BRIGHTNESS Control Register | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x101 | 0x111 | 0x121 | 0x131 | BRIGHT | | | | | | | | 0x00 |

BRIGHT B[7:0] These bits control the brightness. They have value of -128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.

| Index | | | | CONTRAST Control Register | | | | | | | | Default |
|-------|-------|-------|-------|---------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x102 | 0x112 | 0x122 | 0x132 | CNRST | | | | | | | | 0x64 |

CNRST B[7:0] These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 (`100_0000`) has no effect on the video data.

| Index | | | | SHARPNESS Control Register | | | | | | | | Default |
|-------|-------|-------|-------|----------------------------|-----|-----|-----|-------|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x103 | 0x113 | 0x123 | 0x133 | SCURVE | VSF | CTI | | SHARP | | | | 0x11 |

- SCURVE** B[7] This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT.
0 = low
1 = center
- VSF** B[6] This bit is for internal used.
- CTI** B[5:4] CTI level selection. 0 = None. 3 = highest.
- SHARP** B[3:0] These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.

| Index | | | | Chroma (U) Control Register | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x104 | 0x114 | 0x124 | 0x134 | SAT_U | | | | | | | | 0x80 |

- SAT_U** B[7:0] These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.

| Index | | | | Chroma (V) Control Register | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x105 | 0x115 | 0x125 | 0x135 | SAT_V | | | | | | | | 0x80 |

- SAT_V** B[7:0] These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.

| Index | | | | Hue Control Register | | | | | | | | Default |
|-------|-------|-------|-------|----------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x106 | 0x116 | 0x126 | 0x136 | HUE | | | | | | | | 0x00 |

- HUE** B[7:0] These bits control the color hue as 2's complement number. They have value from +36° (7Fh) to -36° (80h) with an increment of 0.28°. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC system.

| Index | | | | Cropping Control Register | | | | | | | | Default |
|-------|-------|-------|-------|---------------------------|-----|------------|-----|-----------|-----|------------|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x107 | 0x117 | 0x127 | 0x137 | VDELAY_HI | | VACTIVE_HI | | HDELAY_HI | | HACTIVE_HI | | 0x02 |

- VDELAY_HI** B[7:6] These bits are bit 9 to 8 of the 10-bit Vertical Delay register.
- VACTIVE_HI** B[5:4] These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg0x109 for its shadow register.
- HDELAY_HI** B[3:2] These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.
- HACTIVE_HI** B[1:0] These bits are bit 9 to 8 of the 10-bit HACTIVE register.

| Index | | | | Vertical Delay Register Low | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x108 | 0x118 | 0x128 | 0x138 | VDELAY_LO | | | | | | | | 0x12 |

- VDELAY_LO** B[7:0] These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.

| Index | | | | Vertical Active Register Low | | | | | | | | Default |
|-------|-------|-------|-------|------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x109 | 0x119 | 0x129 | 0x139 | VACTIVE_LO | | | | | | | | 0xF0 |

- VACTIVE_LO** B[7:0] These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output.
- The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x10E/11E/12E/13E is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.

| Index | | | | Horizontal Delay Register Low | | | | | | | | Default |
|-------|-------|-------|-------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10A | 0x11A | 0x12A | 0x13A | HDELAY_LO | | | | | | | | 0x0F |

- HDELAY_LO** B[7:0] These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video.
- The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These registers can be accessed using the same index address by first changing the decoding format to the corresponding standard.

| Index | | | | Horizontal Active Register Low | | | | | | | | Default |
|-------|-------|-------|-------|--------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10B | 0x11B | 0x12B | 0x13B | HACTIVE_LO | | | | | | | | 0x D0 |

HACTIVE_LO B[7:0] These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.

| Index | | | | Macrovision Detection | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------|-----|-----|-----|--------|--------|----------|--------|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10C | 0x11C | 0x12C | 0x13C | SF* | PF* | FF* | KF* | CSBAD* | MVCSN* | CSTRIPE* | CTYPE* | 0x00 |

Read only register

SF B[7] This bit is for internal use.

PF B[6] This bit is for internal use.

FF B[5] This bit is for internal use.

KF B[4] This bit is for internal use.

CSBAD B[3] 1 = Macrovision color stripe detection may be un-reliable

MVCSN B[2] 1 = Macrovision AGC pulse detected.
0 = Not detected.

CSTRIPE B[1] 1 = Macrovision color stripe protection burst detected.
0 = Not detected.

CTYPE B[0] This bit is valid only when color stripe protection is detected, i.e. Cstripe=1.
1 = Type 2 color stripe protection
0 = Type 3 color stripe protection

| Index | | | | Chip STATUS II | | | | | | | | Default |
|-------|-------|-------|-------|----------------|--------|---------|-------|--------|----------|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10D | 0x11D | 0x12D | 0x13D | VCR* | WKAIR* | WKAIR1* | VSTD* | NINTL* | RESERVED | | | 0x00 |

Read only register

VCR B[7] VCR signal indicator.

WKAIR B[6] Weak signal indicator 2.

WKAIR1B[5] Weak signal indicator controlled by WKTH.

VSTD B[4] 1 = Standard signal
0 = Non-standard signal

NINTL B[3] 1 = Non-interlaced signal
0 = interlaced signal

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| Index | | | | Standard Selection | | | | | | | | Default |
|-------|-------|-------|-------|--------------------|---------|-----|-----|-------|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10E | 0x11E | 0x12E | 0x13E | DETSTATUS* | STDNOW* | | | ATREG | STD | | | 0x07 |

DETSTATUS B[7] 0 = Idle
 1 = detection in progress

STDNOW B[6:4] Current standard invoked
 0 = NTSC(M)
 1 = PAL (B,D,G,H,I)
 2 = SECAM
 3 = NTSC4.43
 4 = PAL (M)
 5 = PAL (CN)
 6 = PAL 60
 7 = Not valid

ATREG B[3] 1 = Disable the shadow registers.
 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard

STD B[2:0] Standard selection
 0 = NTSC(M)
 1 = PAL (B,D,G,H,I)
 2 = SECAM
 3 = NTSC4.43
 4 = PAL (M)
 5 = PAL (CN)
 6 = PAL 60
 7 = Auto detection

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| Index | | | | Standard Recognition | | | | | | | | Default |
|-------|-------|-------|-------|----------------------|---------|---------|---------|---------|--------|---------|---------|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10F | 0x11F | 0x12F | 0x13F | ATSTART | PAL6_EN | PALN_EN | PALM_EN | NT44_EN | SEC_EN | PALB_EN | NTSC_EN | 0x7F |

- ATSTART B[7] Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.
- PAL6_EN B[6] 1 = enable recognition of PAL60.
0 = disable recognition.
- PALN_EN B[5] 1 = enable recognition of PAL (CN).
0 = disable recognition.
- PALM_EN B[4] 1 = enable recognition of PAL (M).
0 = disable recognition.
- NT44_EN B[3] 1 = enable recognition of NTSC 4.43.
0 = disable recognition.
- SEC_EN B[2] 1 = enable recognition of SECAM.
0 = disable recognition
- PALB_EN B[1] 1 = enable recognition of PAL (B,D,G,H,I).
0 = disable recognition
- NTSC_EN B[0] 1 = enable recognition of NTSC (M).
0 = disable recognition

| Index | | | | Vertical Scaling Register, Low | | | | | | | | Default |
|-------|-------|-------|-------|--------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x144 | 0x154 | 0x164 | 0x174 | VSCALE_LO | | | | | | | | 0x00 |

VSCALE_LO B[7:0] These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register

| Index | | | | Scaling Register, High | | | | | | | | Default |
|-------|-------|-------|-------|------------------------|-----|-----|-----|-----------|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x145 | 0x155 | 0x165 | 0x175 | VSCALE_HI | | | | HSCALE_HI | | | | 0x11 |

- VSCALE_HI B[7:4] These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.
- HSCALE_HI B[3:0] These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.

| Index | | | | Horizontal Scaling Register, Low | | | | | | | | Default |
|-------|-------|-------|-------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x146 | 0x156 | 0x166 | 0x176 | HSCALE_LO | | | | | | | | 0x00 |

HSCALE_LO B[7:0] These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.

| Index | | | | Cropping Control Register-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|-----------------------------------|-----|-------------|-----|------------|-----|-------------|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x147 | 0x157 | 0x167 | 0x177 | V2DELAY_HI | | V2ACTIVE_HI | | H2DELAY_HI | | H2ACTIVE_HI | | 0x02 |

This register is for field 2 setting:

V2DELAY_HI B[7:6] These bits are bit 9 to 8 of the 10-bit Vertical Delay register.

V2ACTIVE_HI B[5:4] These bits are bit 9 to 8 of the 10-bit VACTIVE register.

H2DELAY_HI B[3:2] These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.

H2ACTIVE_HI B[1:0] These bits are bit 9 to 8 of the 10-bit HACTIVE register.

| Index | | | | Vertical Delay Register Low-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|-------------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x148 | 0x158 | 0x168 | 0x178 | V2DELAY_LO | | | | | | | | 0x12 |

This register is for field 2 setting:

V2DELAY_LO B[7:0] These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.

| Index | | | | Vertical Active Register Low-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|--------------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x149 | 0x159 | 0x169 | 0x179 | V2ACTIVE_LO | | | | | | | | 0xF0 |

This register is for field 2 setting:

V2ACTIVE_LO B[7:0] These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output.

| Index | | | | Horizontal Delay Register Low-Field2 | | | | | | | | Default |
|-------|-------|-------|-------|--------------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14A | 0x15A | 0x16A | 0x17A | H2DELAY_LO | | | | | | | | 0xF |

This register is for field 2 setting:

H2DELAY_LO B[7:0] These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video.

| Index | | | | Horizontal Active Register Low-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|--|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14B | 0x15B | 0x16B | 0x17B | H2ACTIVE_LO | | | | | | | | 0xD0 |

This register is for field 2 setting:

H2ACTIVE_LO B[7:0] These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.

| Index | | | | Vertical Scaling Register, Low-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|--|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14C | 0x15C | 0x16C | 0x17C | V2SCALE_LO | | | | | | | | 0x00 |

This register is for field 2 setting:

V2SCALE_LO B[7:0] These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register

| Index | | | | Scaling Register, High- Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|---------------------------------|-----|-----|-----|------------|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14D | 0x15D | 0x16D | 0x17D | V2SCALE_HI | | | | H2SCALE_HI | | | | 0x11 |

This register is for field 2 setting:

V2SCALE_HI B[7:4] These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.

H2SCALE_HI B[3:0] These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.

| Index | | | | Horizontal Scaling Register, Low-Field 2 | | | | | | | | Default |
|-------|-------|-------|-------|--|-----|-----|-----|-----|-----|-----|-----|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14E | 0x15E | 0x16E | 0x17E | H2SCALE_LO | | | | | | | | 0x00 |

This register is for field 2 setting:

H2SCALE_LO B[7:0] These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.

| Index | | | | F2CNT | | | | | | | | Default |
|-------|-------|-------|-------|-------|-----|-----|-----|-----|-----|-----|-------|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x14F | 0x15F | 0x16F | 0x17F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F2CNT | 0x00 |

F2CNT B[0] Field 2 configuration registers
 0 = Field2 Video Capture Controlled by VDELAY, VACTIVE, HDELAY, HACTIVE, VSCALE, HSCALE registers.
 1 = Field2 Video Capture Controlled by V2DELAY, V2ACTIVE, H2DELAY, and H2ACTIVE, V2SCALE, H2SCALE field2 registers

| Index | | | | RESERVED | | | | | | | | Default | |
|-------|-------|-------|-------|----------|----------|-----|-----|-----|----------|-----|-----|---------|------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | | |
| 0x1A0 | 0x1A1 | 0x1A2 | 0x1A3 | 0 | RESERVED | | | | RESERVED | | | | 0x08 |

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| Index | | | | ID Detection Control | | | | | | | | Default |
|-------|-------|-------|-------|----------------------|------|-----|-----|-----|-----|-----|------|---------|
| CH1 | CH2 | CH3 | CH4 | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1A4 | 0x1A5 | 0x1A6 | 0x1A7 | IDX | NSEN | | | | | | 0x1A | |
| | | | | | SSEN | | | | | | 0x20 | |
| | | | | | PSEN | | | | | | 0x1C | |
| | | | | | WKTH | | | | | | 0x11 | |

IDX **B[7:6]** These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.

B[5:0]

NSEN **IDX = 0** controls the NTSC color carrier detection sensitivity (NSEN).

SSEN **IDX = 1** controls the SECAM ID detection sensitivity (SSEN).

PSEN **IDX = 2** controls the PAL ID detection sensitivity (PSEN).

WKTH **IDX = 3** controls the weak signal detection sensitivity (WKTH).

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| Index | Software Reset Control Register | | | | | | | | Default |
|-------|---------------------------------|-----|-----|----------|----------|----------|----------|----------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x180 | 0 | 0 | 0 | AUDIORST | VDEC4RST | VDEC3RST | VDEC2RST | VDEC1RST | 0x00 |

- AUDIORST** B[4] A 1 written to this bit resets the Audio portion to its default state but all register content remain unchanged. This bit is self-resetting.
- VDEC4RST** B[3] A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.
- VDEC3RST** B[2] A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.
- VDEC2RST** B[1] A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.
- VDEC1RST** B[0] A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.

| Index | Analog Control Register | | | | | | | | Default |
|-------|-------------------------|------|------|----------|--------|-----------|-------|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x181 | RESERVED | IREF | VREF | RESERVED | CLKPDN | AINSWTEST | YFLEN | YSV | 0x02 |

- IREF B[6] 0 = Internal current reference 1.
 1 = Internal current reference increase 30%.
- VREF B[5] 0 = Internal voltage reference.
 1 = Internal voltage reference shut down.
- CLKPDNB[3] 0 = Normal clock operation.
 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active.
- AINSWTEST B[2] 0 = Normal operation(must be 0)
 1 = AINSWTEST
- YFLEN B[1] Analog Video CH1/CH2/CH3/CH4 anti-alias filter control
 1 = enable
 0 = disable
- YSV B[0] Analog Video CH1/CH2/CH3/CH4 Reduced power mode
 1 = enable
 0 = disable

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| Index | Analog Control Register2 | | | | | | | | Default |
|-------|--------------------------|------|--------|--------|-------|------|------|------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x182 | CTEST | YCLN | CKIPOL | AFLTEN | GTEST | VLPF | CKLY | CKLC | 0x10 |

- CTEST B[7] Clamping control for debugging use.(Test purpose only)
- YCLN B[6] 1 = Y channel clamp disabled(Test purpose only)
0 = Enabled.
- CKIPOL B[5] 27MHz clock output signal rise/fall timing.
0 = change by 54MHz clock output falling edge.
1 = change by 54MHz clock output rising edge.
- AFLTEN B[4] 1 = Analog Audio input Anti-Aliasing Filter enabled
0 = Disabled.(**must be 0 for no Audio Input cross-talk**) (default)
- GTEST B[3] 1 = Test.(Test purpose only)
0 = Normal operation
- VLPF B[2] Clamping filter control.
- CKLY B[1] Clamping current control 1.
- CKLC B[0] Clamping current control 2.

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| Index | Control Register I | | | | | | | | Default |
|-------|--------------------|-----|-------|------|------|-------|-------|------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x183 | PBW | DEM | PALSW | SET7 | COMB | HCOMP | YCOMB | PDLY | 0xCC |

| | | |
|-------------------|-------------|--|
| PBW | B[7] | 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW |
| DEM | B[6] | Reserved |
| PALSW | B[5] | 1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal. |
| SET7 | B[4] | 1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level. |
| COMB | B[3] | 1 = Adaptive comb filter for NTSC and PAL(recommended). Not for SECAM. 0 = Notch filter. For SECAM |
| HCOMP B[2] | | 1 = Adaptive comb filter for NTSC and PAL(recommended). Not for SECAM. 0 = Notch filter. For SECAM. |
| YCOMB B[1] | | 1 = Bypass Comb filter when no burst presence 0 = No bypass |
| PDLY | B[0] | PAL delay line. 0 = enabled. 1 = disabled. |

| Index | Color Killer Hysteresis Control Register | | | | | | | | Default |
|-------|--|------|-----|-----|-------|-----|-----|------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x184 | GMEN | CKHY | | | HSDLY | | | 0x00 | |

| | | |
|--------------|---------------|--|
| GMEN | B[7] | Reserved |
| CKHY | B[6:5] | Color killer hysteresis. 00b – fastest 01b – fast 10b – medium 11b – slow |
| HSDLY | B[4:0] | Reserved for test. |

| Index | Vertical Sharpness | | | | | | | | Default |
|-------|--------------------|-----|-----|-----|----------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x185 | SHCOR | | | | RESERVED | | | | 0x80 |

SHCOR B[7:4] These bits provide coring function for the sharpness control.

| Index | Coring Control Register | | | | | | | | Default |
|-------|-------------------------|-----|------|-----|------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x186 | CTCOR | | CCOR | | VCOR | | CIF | | 0x44 |

CTCOR B[7:6] These bits control the coring for CTI.

CCOR B[5:4] These bits control the low level coring function for the Cb/Cr output.

VCOR B[3:2] These bits control the coring function of vertical peaking.

CIF B[1:0] These bits control the IF compensation level.

- 00b = None
- 01b = 1.5dB
- 10b = 3dB
- 11b = 6dB

| Index | Clamping Gain | | | | | | | | Default |
|-------|---------------|-----|-----|-----|-------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x187 | CLPEND | | | | CLPST | | | | 0x50 |

CLPEND B[7:4] These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.

CLPST B[3:0] These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.

| Index | Individual AGC Gain | | | | | | | | Default |
|-------|---------------------|-----|-----|-----|--------|-----|-----|----------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x188 | NMGAIN | | | | WPGAIN | | | RESERVED | 0x22 |

NMGAIN B[7:4] These bits control the normal AGC loop maximum correction value.

WPGAIN B[3:0] Peak AGC loop gain control.

| Index | Individual AGC Gain | | | | | | | | Default |
|-------|---------------------|------|--------|--------|----------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x189 | RESERVED | FC27 | VYCOMB | VCCOMB | VVBILINE | | | | 0x40 |

- FC27** **B[6]** **1 = normal ITU-R656 operation**
 0 = squared pixel mode
VYCOMB **B[5]** **independent vscaler control**
VCCOMB **B[4]** **independent vscaler control**
VVBILINE **B[3:0]** **VBI line enable**

| Index | White Peak Threshold | | | | | | | | Default |
|-------|----------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18A | PEAKWT | | | | | | | | 0xD8 |

- PEAKWT** **B[7:0]** **These bits control the white peak detection threshold. Setting 'FF' can disable this function.**

| Index | Clamp level | | | | | | | | Default |
|-------|-------------|-------|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18B | CLMPLD | CLMPL | | | | | | | 0xBC |

- CLMPLD** **B[7]** **0 = Clamping level is set by CLMPL.**
 1 = Clamping level preset at 60d.
CLMPL **B[6:0]** **These bits determine the clamping level of the Y channel.**

| Index | Sync Amplitude | | | | | | | | Default |
|-------|----------------|-------|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18C | SYNCTD | SYNCT | | | | | | | 0xB8 |

- SYNCTD** **B[7]** **0 = Reference sync amplitude is set by SYNCT.**
 1 = Reference sync amplitude is preset to 38h.
SYNCT **B[6:0]** **These bits determine the standard sync pulse amplitude for AGC reference.**

| Index | Sync Miss Count Register | | | | | | | | Default |
|-------|--------------------------|-----|-----|-----|-------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18D | MISSCNT | | | | HSWIN | | | | 0x44 |

MISSCNT B[7:4] These bits set the threshold for horizontal sync miss count threshold.

HSWIN B[3:0] These bits determine the VCR mode detection threshold.

| Index | Clamp Position Register | | | | | | | | Default |
|-------|-------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18E | PCLAMP | | | | | | | | 0x38 |

PCLAMP B[7:0] These bits set the clamping position from the PLL sync edge

| Index | Vertical Control I | | | | | | | | Default |
|-------|--------------------|-----|-------|-----|-------|------|------|------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x18F | VLCKI | | VLCKO | | VMODE | DETV | AFLD | VINT | 0x00 |

VLCKI B[7:6] Vertical lock in time.

0 = fastest

3 = slowest.

VLCKO B[5:4] Vertical lock out time.

0 = fastest

3 = slowest.

VMODE B[3] This bit controls the vertical detection window.

1 = search mode.

0 = vertical count down mode.

DETV B[2] 1 = recommended for special application only.

0 = Normal Vsync logic

AFLD B[1] Auto field generation control

0 = Off

1 = On

VINT B[0] Vertical integration time control.

1 = short

0 = normal

| Index | Vertical Control II | | | | | | | | Default |
|-------|---------------------|-----|-----|-----|------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x190 | BSHT | | | | VSHT | | | | 0x00 |

BSHT B[7:4] Burst PLL center frequency control.

VSHT B[3:0] Vsync output delay control in the increment of half line length.

| Index | Color Killer Level Control | | | | | | | | Default |
|-------|----------------------------|-----|-----|-----|---------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x191 | CKILMAX | | | | CKILMIN | | | | 0x78 |

CKILMAX B[7:5] These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.

CKILMIN B[4:0] These bits control the color killer threshold. Larger value gives lower killer level.

| Index | Comb Filter Control | | | | | | | | Default |
|-------|---------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x192 | HTL_MD | HTL | | | VTL | | | | 0x44 |

HTL_MDB[7] 0 = adaptive mode
 1 = fixed comb

HTL B[6:4] Adaptive Comb filter threshold control 1.

VTL B[3:0] Adaptive Comb filter threshold control 2.

| Index | Luma Delay and H Filter Control | | | | | | | | Default |
|-------|---------------------------------|------|-----|-----|-----|-------|-----|---------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x193 | CKLM | YDLY | | | 0 | ASAVE | BP | HPF_RES | 0x30 |

CKLM B[7] Color Killer mode
 0 = normal
 1 = fast (for special application)

YDLY B[6:4] Luma delay fine adjustment. This 2's complement number provides -4 to +3 unit delay control.

ASAVE B[2] Audio ADC power saving control

BP B[1] Audio ADC input buffer bypass

HPF_RES B[0] Audio ADC High Pass Filter Resistance Control

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| Index | Miscellaneous Control I | | | | | | | | Default |
|-------|-------------------------|-------|------|------|--------|--------|-------|----------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x194 | HPLC | EVCNT | PALC | SDET | TBC_EN | BYPASS | SYOUT | RESERVED | 0x14 |

- HPLC** B[7] Reserved for internal use.
- EVCNT** B[6] 1 = Even field counter in special mode.
0 = Normal operation
- PALC** B[5] Reserved for future use.
- SDET** B[4] ID detection sensitivity. A '1' is recommended.
- TBC_EN** B[3] 1 = Internal TBC enable. Total pixel per line on Video active line is always 858x2 for NTSC/PAL-M(60Hz) and 864x2 for PAL/SECAM(50Hz).
0 = TBC off.
- BYPASS**B[2] It controls the standard detection and should be set to '1' in normal use.
- SYOUT** B[1] 1 = Hsync output is disabled when video loss is detected
0 = Hsync output is always enabled

| Index | LOOP Control Register | | | | | | | | Default |
|-------|-----------------------|-----|------|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x195 | HPM | | ACCT | | SPM | | | | 0xA5 |

- HPM** B[7:6] Horizontal PLL acquisition time.
0 = Normal; 1 = Auto2; 2 = Auto1; 3 = Fast
- ACCT** B[5:4] ACC time constant
0 = No ACC; 1 = slow; 2 = medium; 3 = fast
- SPM** B[3:2] Burst PLL control.
0 = Slowest; 1 = Slow; 2 = Fast; 3 = Fastest
- CBW** B[1:0] Chroma low pass filter bandwidth control.
Refer to filter curves.

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| Index | Miscellaneous Control II | | | | | | | | Default |
|-------|--------------------------|-------|-------|------|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x196 | NKILL | PKILL | SKILL | CBAL | FCS | LCS | CCS | BST | 0xE0 |

- NKILL** B[7] 1 = Enable noisy signal color killer function in NTSC mode.
0 = Disabled.
- PKILL** B[6] 1 = Enable automatic noisy color killer function in PAL mode.
0 = Disabled.
- SKILL** B[5] 1 = Enable automatic noisy color killer function in SECAM mode.
0 = Disabled.
- CBAL** B[4] 0 = Normal output
1 = special output mode.
- FCS** B[3] 1 = Force decoder output value determined by CCS.
0 = Disabled.
- LCS** B[2] 1 = Enable pre-determined output value indicated by CCS when
video loss is detected.
0 = Disabled.
- CCS** B[1] When FCS is set high or video loss condition is detected when LCS
is set high, one of two colors display can be selected.
1 = Blue color.
0 = Black.
- BST** B[0] 1 = Enable blue stretch.
0 = Disabled.

| Index | Miscellaneous Control II | | | | | | | | Default |
|-------|--------------------------|-----|-----|-----|------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x197 | FRM | | YNR | | CLMD | | PSP | | 0x05 |

- FRM** B[7:6] Free run mode control
0 = Auto 2 = default to 60Hz 3 = default to 50Hz
- YNR** B[5:4] Y HF noise reduction
0 = None 1 = smallest 2 = small 3 = medium
- CLMD** B[3:2] Clamping mode control.
0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A
- PSP** B[1:0] Slice level control
0 = low 1 = medium 2 = high

| Index | Horizontal Scaler Pre-filter Control | | | | | | | | Default |
|-------|--------------------------------------|-----|-----|-----|-------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1A8 | HFLT2 | | | | HFLT1 | | | | 0x00 |
| 0x1A9 | HFLT4 | | | | HFLT3 | | | | 0x00 |

HFLT Pre-filter selection for Video CH1/CH2/CH3/CH4 horizontal scaler
 If HSCALE[11-8]=1, HFLT [3:0] controls the peaking function.
 If HSCALE[11-8]>1, HFLT [2:0] function is below.

1** = Bypass

000 = Auto selection based on Horizontal scaling ratio. (default)
 001 = Recommended for CIF size image
 010 = Recommended for QCIF size image
 011 = Recommended for ICON size image

| Index | Video AGC Control | | | | | | | | Default |
|-------|-------------------|--------|--------|--------|-----------------|-----------------|-----------------|-----------------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1AA | AGCEN4 | AGCEN3 | AGCEN2 | AGCEN1 | AGCGAIN4 [8] | AGCGAIN3 [8] | AGCGAIN2 [8] | AGCGAIN1 [8] | 0x00 |
| 0x1AB | AGCGAIN1[7:0] | | | | | | | | 0xF0 |
| 0x1AC | AGCGAIN2[7:0] | | | | | | | | 0xF0 |
| 0x1AD | AGCGAIN3[7:0] | | | | | | | | 0xF0 |
| 0x1AE | AGCGAIN4[7:0] | | | | | | | | 0xF0 |

AGCEN Select Video AGC loop function on AIN1 ~ AIN4
 0 = AGC loop function enabled (recommended for most application cases) (default)
 1 = AGC loop function disabled. Gain is set by AGCGAIN1~4

AGCGAIN These registers control the AGC gain when AGC loop is disabled.
 Default value is 0xF0.

| Index | Vertical Peaking Level Control | | | | | | | | Default |
|-------|--------------------------------|-------|-----|-----|----------|-------|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1AF | RESERVED | VSHP2 | | | RESERVED | VSHP1 | | | 0x00 |
| 0x1B0 | RESERVED | VSHP4 | | | RESERVED | VSHP3 | | | 0x00 |

VSHP Select Video Vertical peaking level. (*)
 0 none. (default)
 7 highest

*Note: VSHP must be set to '0' if Reg0x183 COMB = 0.

| Index | Audio ADC Digital Input Offset Control | | | | | | | | Default |
|-------|--|-----|---------------|-----|---------------|-----|---------------|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1B3 | AADC4OFS[9:8] | | AADC3OFS[9:8] | | AADC2OFS[9:8] | | AADC1OFS[9:8] | | 0x00 |
| 0x1B4 | AADC1OFS[7:0] | | | | | | | | 0x00 |
| 0x1B5 | AADC2OFS[7:0] | | | | | | | | 0x00 |
| 0x1B6 | AADC3OFS[7:0] | | | | | | | | 0x00 |
| 0x1B7 | AADC4OFS[7:0] | | | | | | | | 0x00 |

Digital ADC input data offset control. Digital ADC input data is adjusted by

$$ADJAADCn = AUDnADC + AADCnOFS.$$

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

| Index | Analog Audio ADC Digital Output Value | | | | | | | | Default |
|-------|---------------------------------------|-----|---------------|-----|---------------|-----|---------------|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1B8 | AUD4ADC[9:8]* | | AUD3ADC[9:8]* | | AUD2ADC[9:8]* | | AUD1ADC[9:8]* | | 0x00 |
| 0x1B9 | AUD1ADC[7:0]* | | | | | | | | 0x00 |
| 0x1BA | AUD2ADC[7:0]* | | | | | | | | 0x00 |
| 0x1BB | AUD3ADC[7:0]* | | | | | | | | 0x00 |
| 0x1BC | AUD4ADC[7:0]* | | | | | | | | 0x00 |

These bits are read only.

AUDnADC shows current Analog Audio n ADC Digital Output Value by 2's format.

| Index | Adjusted Analog Audio ADC Digital input Value | | | | | | | | Default |
|-------|---|-----|----------------|-----|----------------|-----|----------------|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1BD | ADJAADC4[9:8]* | | ADJAADC3[9:8]* | | ADJAADC2[9:8]* | | ADJAADC1[9:8]* | | 0x00 |
| 0x1BE | ADJAADC1[7:0]* | | | | | | | | 0x00 |
| 0x1BF | ADJAADC2[7:0]* | | | | | | | | 0x00 |
| 0x1C0 | ADJAADC3[7:0]* | | | | | | | | 0x00 |
| 0x1C1 | ADJAADC4[7:0]* | | | | | | | | 0x00 |

These bits are read only.

ADJAADCn shows current adjusted Audio ADC Digital input data value by 2's format. These value show the first input data value in front of Digital Audio Decimation Filtering process.

| Index | Analog Power Down | | | | | | | | Default |
|-------|-------------------|----------|----------|------------|------------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1CE | AAUTOMUTE | RESERVED | RESERVED | A_ADC_PWDN | V_ADC_PWDN | | | | 0x00 |

AAUTOMUTE B[7] 1 = When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200.
0 = No effect (default)

A_ADC_PWDN B[4] Power down the audio ADC
0 = Normal operation (default)
1 = Power down

V_ADC_PWDN B[3:0] Power down the video ADC
V_ADC_PWDN[3:0] stands for CH4 to CH1.
0 = Normal operation (default)
1 = Power down

| Index | Analog Audio Input Gain | | | | | | | | Default |
|-------|-------------------------|---------|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1D0 | 0 | AIGAIN1 | | | | | | | 0x20 |
| 0x1D1 | 0 | AIGAIN2 | | | | | | | 0x20 |
| 0x1D2 | 0 | AIGAIN3 | | | | | | | 0x20 |
| 0x1D3 | 0 | AIGAIN4 | | | | | | | 0x20 |

AIGAIN Select the amplifier's gain for each analog audio input AIN1 ~ AIN4.
Gain Steps: 128
Gain Range: 0.5~2.484375
Gain Step Size: 0.015625
Gain Default : 1.00

| Index | Mix Mute Control | | | | | | | | Default |
|-------|------------------|-----|-------------|----------|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1DC | LAWMD | | MIX_DERATIO | MIX_MUTE | | | | | 0x00 |

- LAWMD** B[7:6] Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin.
0 = PCM output (default)
1 = SB(Signed MSB bit in PCM data is inverted) output
2 = u-Law output
3 = A-Law output
- MIX_DERATIO** B[5] Disable the mixing ratio value for all audio.
0 = Apply individual mixing ratio value for each audio (default)
1 = Apply nominal value for all audio commonly
- MIX_MUTE** B[3:0] Enable the mute function for each audio. It effects only for mixing.
MIX_MUTE[0] : Audio input AIN1.
MIX_MUTE[1] : Audio input AIN2.
MIX_MUTE[2] : Audio input AIN3.
MIX_MUTE[3] : Audio input AIN4.
MIX_MUTE[4] : Playback audio input.
It effects only for single chip or the last stage chip
0 = Normal (default)
1 = Muted

| Index | Mix Ratio Value | | | | | | | | Default |
|-------|-----------------|-----|-----|-----|------------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1DD | MIX_RATIO2 | | | | MIX_RATIO1 | | | | 0x00 |
| 0x1DE | MIX_RATIO4 | | | | MIX_RATIO3 | | | | 0x00 |

MIX_RATIO

Define the ratio values for audio mixing.

MIX_RATIO1 : Audio input AIN1.

MIX_RATIO2 : Audio input AIN2.

MIX_RATIO3 : Audio input AIN3.

MIX_RATIO4 : Audio input AIN4.

It effects only for single chip or the last stage chip.

0 0.25(Recommended for more than 4x AIN1/AIN2/AIN3/AIN4) (default)

1 0.31

2 0.38

3 0.44

4 0.50

5 0.63

6 0.75

7 0.88

8 1.00

9 1.25

10 1.50

11 1.75

12 2.00

13 2.25

14 2.50

15 2.75

| Index | Mix Output Selection | | | | | | | | Default | |
|-------|----------------------|---------------|---------------|------------|-----|-----|-----|-----|---------|------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | | |
| 0x1E0 | VADCCK POL | AADCCK POL | ADACCK POL | MIX_OUTSEL | | | | | | 0x14 |

| | | |
|------------|--------|---|
| VADCCKPOL | B[7] | Test purpose only. 0 (default) |
| AADCCKPOL | B[6] | Test purpose only. 0 (default) |
| ADACCKPOL | B[5] | Test purpose only. 0 (default) |
| MIX_OUTSEL | B[4:0] | Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10 Select record audio of channel 11 11 Select record audio of channel 12 12 Select record audio of channel 13 13 Select record audio of channel 14 14 Select record audio of channel 15 15 Select record audio of channel 16 16 Select playback audio of the first stage chip 17 Select playback audio of the second stage chip 18 Select playback audio of the third stage chip 19 Select playback audio of the last stage chip 20 Select mixed audio (default) |

| Index | Audio Detection Period | | | | | | | | Default |
|-------|------------------------|-------------|-----|-----|-------------|-------------|-------------|-------------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1E1 | AAMPMD | ADET_FILTER | | | ADET_TH4[4] | ADET_TH3[4] | ADET_TH2[4] | ADET_TH1[4] | 0xC0 |

- AAMPMD** B[7] Define the audio detection method.
0 = Detect audio if absolute amplitude is greater than threshold (default)
1 = Detect audio if differential amplitude is greater than threshold
- ADET_FILTER** B[6:5] Select the filter for audio detection
0 = Wide LPF (default)
.....
7 = Narrow LPF

| Index | Audio Detection Threshold | | | | | | | | Default |
|-------|---------------------------|-------------|-----|-----|---------------|-------------|-------------|-------------|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1E1 | AAMPMD | ADET_FILTER | | | ADET_TH4[4] | ADET_TH3[4] | ADET_TH2[4] | ADET_TH1[4] | 0xC0 |
| 0x1E2 | ADET_TH2[3:0] | | | | ADET_TH1[3:0] | | | | 0xAA |
| 0x1E3 | ADET_TH4[3:0] | | | | ADET_TH3[3:0] | | | | 0xAA |

- ADET_TH** Define the threshold value for audio detection.
ADET_TH1: Audio input AIN1.
ADET_TH2: Audio input AIN2.
ADET_TH3: Audio input AIN3.
ADET_TH4: Audio input AIN4.
0 Low value (default)
. .
. .
31 High value

If fs=8kHz Audio Clock setting mode:
Reg0x1E1=0xC0, Reg0x1E2=0xAA, Reg0x1E3=0xAA are typical setting value.
If fs=16kHz/32kHz/44.1kHz/48kHz Audio Clock setting mode:
Reg0x1E1=0xE0, Reg0x1E2=0xBB, Reg0x1E3=0xBB are typical setting value.

| Index | AADC_TEST | | | | | | | | Default |
|-------|-----------|-------------|------------|-----------|-----------|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1FC | 0 | ASYN SERIAL | AADC_PFTST | AINSW FIX | AINSW NUM | | | | 0x00 |

Audio ADC test controls These bits are not for normal usage

| Index | VADC_TEST | | | | | | | | Default |
|-------|-----------|-----|-----|-----|-----|------------|------------|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1FD | 0 | 0 | 0 | 0 | 0 | VADC_PFTST | VADC_PFSEL | | 0x00 |

Video ADC test controls These bits are not for normal usage

| Index | Device ID | | | | | | | | Default |
|-------|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x1FE | DEV_ID[5:4]*: 0h | | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| 0x1FF | DEV_ID[3:0]*: 7h | | | | 0 | 0 | 0 | 1 | 0x71 |

DEV_ID Device ID (0x07)

Video Decoder & Audio Codec (CH4~CH7)

(Starting from 0x200)

The map for video decoder 4~7 and Audio codec 4~7 is the same as Video Decoder 0~3 Audio 0~3. The only difference is that it starts from 0x200.

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PCIe Endpoint Controller

| Offset | | EP_HEADER_REG0 | | | | | | | | Default |
|--------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x00 | B3 | DEVICE_ID | | | | | | | | 0x68 |
| | B2 | | | | | | | | | 0x64 |
| | B1 | VENDOR_ID | | | | | | | | 0x17 |
| | B0 | | | | | | | | | 0x97 |

| | | |
|-----------|----------|-----------|
| DEVICE_ID | B[31:16] | Device ID |
| VENDOR_ID | B[15: 0] | Vendor ID |

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| Offset | | EP_HEADER_REG1 | | | | | | | | Default |
|--------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x04 | B3 | STATUS_REG | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x10 |
| | B1 | COMMAND_REG | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

| | | | |
|-------------|----------|--|------------------------|
| STATUS_REG | B[31] | Detected parity error | |
| | B[30] | Signaled system error | |
| | B[29] | Received master abort | |
| | B[28] | Received target abort | |
| | B[27] | Signaled target abort | |
| | B[26:25] | 2'b00 | |
| | B[24] | Master data parity error | |
| | B[23:21] | 3'b000 | |
| | B[20] | Capabilities list. Indicates presence of an extended capability item. Hardwired to 1 | |
| | B[19] | INTx status | |
| | B[18:16] | Reserved | |
| COMMAND_REG | | B[15:11] | Reserved |
| | | B[10] | INTx assertion disable |
| | | B[9] | 1'b0 |
| | | B[8] | SERR# enable |
| | | B[7] | 1'b0 |
| | | B[6] | Parity error response |
| | | B[5:3] | 3'b000 |
| | | B[2] | Bus master enable |
| | | B[1] | Memory space enable |
| | B[0] | I/O space enable | |

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| Offset | | EP_HEADER_REG2 | | | | | | | | Default |
|--------|----|----------------|------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x08 | B3 | CLASS_CODE | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | REVISION_ID | 0x01 | | | | | | | |

CLASS_CODE B[31:24] Base class code
 B[23:16] Subclass code
 B[15:8] Programming interface

REVISION_ID B[7:0] Revision ID

| Offset | | EP_HEADER_REG3 | | | | | | | | Default |
|--------|----|-----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x0C | B3 | BIST | | | | | | | | 0x00 |
| | B2 | HEADER_TYPE | | | | | | | | 0x00 |
| | B1 | LATENCY_TIMER | | | | | | | | 0x00 |
| | B0 | CACHE_LINE_SIZE | | | | | | | | 0x00 |

BIST B[31:24] 8'h00

HEADER_TYPE B[23] 1'b0
 B[22:16] Configuration header format (hardwired to 0 for type 0.)

LATENCY_TIMER B[15:8] 8'h00

CACHE_LINE_SIZE B[7:0] 8'h00

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| Offset | | EP_HEADER_REG4~ EP_HEADER_REG9 | | | | | | | | Default |
|--------|----|--------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10 | B3 | BASE_ADDRESS_REG0 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x08 |
| 0x14 | B3 | BASE_ADDRESS_REG1 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0x18 | B3 | BASE_ADDRESS_REG2 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0x1C | B3 | BASE_ADDRESS_REG3 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0x20 | B3 | BASE_ADDRESS_REG4 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |
| 0x24 | B3 | BASE_ADDRESS_REG5 | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

BASE_ADDRESS B[31:4] BAR base address bits
 B[3] If BAR is a memory BAR, bit 3 indicates if the memory region is prefetchable:
 0 = Non-prefetchable
 1 = Prefetchable
 If BAR is an I/O BAR, bit 3 is the second least significant bit of the base address.
 B[2:1] 2'b00
 B[0] 0 = BAR is a memory BAR
 1 = BAR is an I/O BAR

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| Offset | | EP_HEADER_REGA | | | | | | | | Default |
|--------|----|---------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x28 | B3 | CARDBUS_CIS_POINTER | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

CARDBUS_CIS_POINTER B[31:0] CardBus CIS pointer

| Offset | | EP_HEADER_REGB | | | | | | | | Default |
|--------|----|---------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x2C | B3 | SUBSYSTEM_ID | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | SUBSYSTEM_VENDOR_ID | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

SUBSYSTEM_ID B[31:16] Subsystem ID
 SUBSYSTEM_VENDOR_ID B[15:0] Subsystem Vendor ID

| Index | | EP_HEADER_REGC | | | | | | | | Default |
|-------|----|-------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x30 | B3 | EXPANSION_ROM_BASE_ADDR | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

EXPANSION_ROM_BASE_ADDR
 B[31:11] Expansion ROM Address
 B[10:1] Reserved
 B[0] Expansion ROM Enable

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| Offset | | EP_HEADER_REGD | | | | | | | | Default |
|--------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x34 | B3 | | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | CAP_PTR |

CAP_PTR B[7:0] First capability pointer. Points to Power Management Capability structure by default.

| Offset | | EP_HEADER_REGF | | | | | | | | Default |
|--------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x3C | B3 | RESERVED | | | | | | | | 0x00 |
| | B2 | RESERVED | | | | | | | | 0x00 |
| | B1 | INTERRUPT_PIN | | | | | | | | 0x01 |
| | B0 | INTERRUPT_LINE | | | | | | | | 0xFF |

INTERRUPT_PIN B[15:8] Interrupt pin. Identifies the legacy interrupt Message that the device (or device function) uses.
 01h: The device (or function) uses INTA
 02h: The device (or function) uses INTB
 03h: The device (or function) uses INTC
 04h: The device (or function) uses INTD

INTERRUPT_LINE B[7:0] Interrupt line

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| Offset | | EP_PM_CAP_REG0 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x40 | B3 | PMC | | | | | | | | 0xC9 |
| | B2 | | | | | | | | | 0xC3 |
| | B1 | NEXT_CAP_POINTER | | | | | | | | 0x50 |
| | B0 | CAP_ID | | | | | | | | 0x01 |

PMC **Power Management Capabilities Register**

B[31:27] PME_Support
 Identifies the power states from which the EP Controller can generate PME Messages. A value of 0 for any bit indicates that the device (or function) is not capable of generating PME Messages while in that power state:
 Bit 27: If set, PME Messages can be generated from D0
 Bit 28: If set, PME Messages can be generated from D1
 Bit 29: If set, PME Messages can be generated from D2
 Bit 30: If set, PME Messages can be generated from D3hot
 Bit 31: If set, PME Messages can be generated from D3cold

B[26] D2 Support
B[25] D1 Support
B[24:22] AUX Current
B[21] Device Specific Initialization (DSI)
B[20] Reserved
B[19] PME Clock (1'b0)
B[18:16] Power Management Specification Version

NEXT_CAP_POINTER **B[15:8] Next capability pointer**

CAP_ID **B[7:0] Power Management capability ID**

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| Offset | | EP_PM_CAP_REG1 | | | | | | | | Default |
|--------|----|----------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x44 | B3 | DATA | | | | | | | | 0x00 |
| | B2 | PMCSR_BSE_EXT | | | | | | | | 0x00 |
| | B1 | PMCSR | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

DATA B[31:24] 8'h00

PMCSR_BSE_EXT B[23] Bus Power/Clock Control enable (hardwired to 0)
 B[22] B2/B3 support (hardwired to 0)
 B[21:16] Reserved

PMCSR B[15] PME status
 B[14:13] Data scale (not supported)
 B[12:9] Data select (not supported)
 B[8] PME enable. A value of 1 indicates that the device is enabled
 to generate PME
 B[7:4] Reserved
 B[3] No soft reset
 B[2] Reserved
 B[1:0] Power state
 Controls the device power state:
 00b: D0
 01b: D1
 10b: D2
 11b: D3

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| Offset | | EP_PCIE_CAP_REG0 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x70 | B3 | PCIE_CAP_REG | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x12 |
| | B1 | NEXT_CAP_POINTER | | | | | | | | 0x00 |
| | B0 | CAP_ID | | | | | | | | 0x10 |

PCIE_CAP_REG

- B[31:30] Reserved
- B[29:25] Interrupt message number
- B[24] Slot implemented (it must 0 for an EP device.)
- B[23:20] Device port type
- B[19:16] PCI Express capability version

NEXT_CAP_POINTER B[15:8] Next capability pointer

CAP_ID B[7:0] PCI Express capability ID

| Offset | | EP_PCIE_CAP_REG1 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x74 | B3 | DEVICE_CAP | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x87 |
| | B0 | | | | | | | | | 0x22 |

DEVICE_CAP

- B[31:28] Reserved
- B[27:26] Captured slot power limit scale. From Message from RC, upstream port only.
- B[25:18] Captured slot power limit value. From Message from RC, upstream port only.
- B[17:16] Reserved
- B[15] Role-Based error reporting
- B[14:12] 3'b000
- B[11:9] Endpoint L1 acceptable latency
- B[8:6] Endpoint L0s acceptable latency
- B[5] Extended tag field supported
- B[4:3] Phantom function supported (must be 0)
- B[2:0] Max_Payload_Size supported

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| Offset | | EP_PCIE_CAP_REG2 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x78 | B3 | DEVICE_STATUS | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x10 |
| | B1 | DEVICE_CONTROL | | | | | | | | 0x20 |
| | B0 | | | | | | | | | 0x10 |

DEVICE_STATUS

B[31:22] Reserved

B[21] Transaction pending
Set to 1 when Non-Posted Requests are not yet completed and clear when they are completed.

B[20] Aux power detected
Set to 1 if Aux power detected.

B[19] Unsupported request detected
Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

B[18] Fatal error detected
Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

B[17] Non-Fatal error detected
Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

B[16] Correctable error detected
Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

DEVICE_CONTROL

B[15] Reserved

B[14:12] Max_Read_Request_Size

B[11] Enable no snoop

B[10] AUX power PM enable

B[9] Phantom function enable

B[8] Extended tag field enable

B[7:5] Max_Payload_Size

B[4] Enable relaxed ordering

B[3] Unsupported request reporting enable

B[2] Fatal error reporting enable

B[1] Non-Fatal error reporting enable

B[0] Correctable error reporting enable

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| Offset | | EP_PCIE_CAP_REG3 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x7C | B3 | LINK_CAP | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x07 |
| | B1 | | | | | | | | | 0x3C |
| | B0 | | | | | | | | | 0x11 |

- LINK_CAP**
- B[31:24] Port number
 - B[23:22] Reserved
 - B[21] Link bandwidth notification capability
Set to 1 for Endpoint devices.
 - B[20] Data Link Layer active reporting capable
Set to 1 for Endpoint devices.
 - B[19] Surprise down error reporting capable
Not supported, hardwired to 0x0
 - B[18] Clock power management
 - B[17:15] L1 exit latency
 - B[14:12] L0s exit latency
 - B[11:10] Active state link PM support
 - B[9:4] Maximum link width
 - B[3:0] Maximum link speed

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| Offset | | EP_PCIE_CAP_REG4 | | | | | | | | Default |
|--------|----|------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x80 | B3 | LINK_STATUS | | | | | | | | 0x10 |
| | B2 | | | | | | | | | 0x11 |
| | B1 | LINK_CONTROL | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

- LINK_STATUS**
- B[31] Link autonomous bandwidth status
 - B[30] Link bandwidth management status
 - B[29] Data Link Layer active (hardwired to 0)
 - B[28] Slot clock configuration
 - B[27] Link training (hardwired to 0)
 - B[26] Reserved
 - B[25:20] Negotiated link width
Set automatically by hardware after Link initialization.
 - B[19:16] Link speed
The negotiated Link speed: 2.5 Gbps
- LINK_CONTROL**
- B[15:12] Reserved
 - B[11] Link autonomous bandwidth interrupt enable (reserved for Endpoints)
 - B[10] Link bandwidth management interrupt enable (reserved for Endpoints)
 - B[9] Hardware autonomous width disable (not supported)
 - B[8] Enable clock Power Management
Hardwired to 0 if Clock Power Management is disabled in the Link Capabilities register.
 - B[7] Extended synch
 - B[6] Common clock configuration
 - B[5] Retrain link (hardwired to 0)
 - B[4] Link disable (hardwired to 0)
 - B[3] Read completion boundary (RCB)
 - B[2] Reserved
 - B[1:0] Active state link PM control

| Offset | | EP_ERR_CAP_REG0 | | | | | | | | Default |
|--------|----|--------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x100 | B3 | ENHANCE_CAP_HEADER | | | | | | | | 0x14 |
| | B2 | | | | | | | | | 0x01 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x01 |

ENHANCE_CAP_HEADER

- B[31:20] Next capability offset
- B[19:16] Capability version
- B[15:0] PCI Express extended capability ID
Default value is 0x1 for Advanced Error Reporting.

| Offset | | EP_ERR_CAP_REG1 | | | | | | | | Default |
|--------|----|----------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x104 | B3 | UNCORRECTABLE_ERROR_STATUS | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

UNCORRECTABLE_ERROR_STATUS

- B[31:21] Reserved
- B[20] Unsupported request error status
- B[19] ECRC error status
- B[18] Malformed TLP status
- B[17] Receiver overflow status
- B[16] Unexpected completion status
- B[15] Completer abort status
- B[14] Completion timeout status
- B[13] Flow control protocol error status
- B[12] Poisoned TLP status
- B[11:6] Reserved
- B[5] Surprise down error status (not supported)
- B[4] Data link protocol error status
- B[3:0] Reserved

| Offset | | EP_ERR_CAP_REG2 | | | | | | | | Default |
|--------|----|--------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x108 | B3 | UNCORRECTABLE_ERROR_MASK | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

UNCORRECTABLE_ERROR_MASK

- B[31:21] Reserved
- B[20] Unsupported request error mask
- B[19] ECRC error mask
- B[18] Malformed TLP mask
- B[17] Receiver overflow mask
- B[16] Unexpected completion mask
- B[15] Completer abort mask
- B[14] Completion timeout mask
- B[13] Flow control protocol error mask
- B[12] Poisoned TLP mask
- B[11:6] Reserved
- B[5] Surprise down error mask (not supported)
- B[4] Data link protocol error mask
- B[3:0] Reserved

| Offset | | EP_ERR_CAP_REG3 | | | | | | | | Default |
|--------|----|------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x10C | B3 | UNCORRECTABLE_ERROR_SEVERITY | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x06 |
| | B1 | | | | | | | | | 0x20 |
| | B0 | | | | | | | | | 0x30 |

UNCORRECTABLE_ERROR_SEVERITY

- B[31:21] Reserved
- B[20] Unsupported request error severity
- B[19] ECRC error severity
- B[18] Malformed TLP severity
- B[17] Receiver overflow severity
- B[16] Unexpected completion severity
- B[15] Completer abort severity
- B[14] Completion timeout severity
- B[13] Flow control protocol error severity
- B[12] Poisoned TLP severity
- B[11:6] Reserved
- B[5] Surprise down error severity (not supported)
- B[4] Data link protocol error severity
- B[3:0] Reserved

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| Offset | | EP_ERR_CAP_REG4 | | | | | | | | Default |
|--------|----|--------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x110 | B3 | CORRECTABLE_ERROR_STATUS | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0x00 |

CORRECTABLE_ERROR_STATUS

- B[31:14] Reserved
- B[13] Advisory non-fatal error status
- B[12] Reply timer timeout status
- B[11:9] Reserved
- B[8] REPLAY_NUM rollover status
- B[7] Bad DLLP status
- B[6] Bad TLP status
- B[5] Reserved
- B[4:0] Receiver error status

| Offset | | EP_ERR_CAP_REG5 | | | | | | | | Default |
|--------|----|------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x114 | B3 | CORRECTABLE_ERROR_MASK | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x20 |
| | B0 | | | | | | | | | 0x00 |

CORRECTABLE_ERROR_MASK

- B[31:14] Reserved
- B[13] Advisory non-fatal error mask
- B[12] Reply timer timeout mask
- B[11:9] Reserved
- B[8] REPLAY_NUM rollover mask
- B[7] Bad DLLP mask
- B[6] Bad TLP mask
- B[5] Reserved
- B[4:0] Receiver error mask

| Offset | | EP_ERR_CAP_REG6 | | | | | | | | Default |
|--------|----|---------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] | |
| 0x118 | B3 | ADVANCE_ERROR_CAP_CONTROL | | | | | | | | 0x00 |
| | B2 | | | | | | | | | 0x00 |
| | B1 | | | | | | | | | 0x00 |
| | B0 | | | | | | | | | 0xA0 |

ADVANCE_ERROR_CAP_CONTROL

- B[31:9] Reserved
- B[8] ECRC check enable
- B[7] ECRC check capable
- B[6] ECRC generation enable
- B[5] ECRC generation capability
- B[4:0] First error pointer

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| Offset | | EP_ERR_CAP_REG7~ EP_ERR_CAP_REGA | | | | | | | Default |
|--------|----|----------------------------------|-----|-----|-----|-----|-----|-----|---------|
| | | [7] | [6] | [5] | [4] | [3] | [2] | [1] | |
| 0x11C | B3 | HEADER_LOG_1ST_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x120 | B3 | HEADER_LOG_2RD_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x124 | B3 | HEADER_LOG_3RD_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |
| 0x128 | B3 | HEADER_LOG_4TH_DW | | | | | | | 0x00 |
| | B2 | | | | | | | | 0x00 |
| | B1 | | | | | | | | 0x00 |
| | B0 | | | | | | | | 0x00 |

These 4 header registers collect the header for the TLP corresponding to a detected error.

Parametric Information

Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|---------------------------|--------------------|------|-----|-----|-------|
| VDDA (Measured to VSSA) | VDDA _{VM} | -0.5 | | 4.5 | V |
| VDDV (Measured to VSSV) | VDDV _{AM} | -0.5 | | 4.5 | V |
| VDD12 (Measured to VSS12) | VDD12 _M | -0.5 | | 2.3 | V |
| VDD33 (Measured to VSS33) | VDD33 _M | -0.5 | | 4.5 | V |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---------------------------|--------------------|------|-----|------|-------|
| VDDA (Measured to VSSA) | VDDA _{VM} | 3.0 | 3.3 | 3.6 | V |
| VDDV (Measured to VSSV) | VDDV _{AM} | 3.0 | 3.3 | 3.6 | V |
| VDD12 (Measured to VSS12) | VDD12 _M | 1.08 | 1.2 | 1.32 | V |
| VDD33 (Measured to VSS33) | VDD33 _M | 3.0 | 3.3 | 3.6 | V |

DC Electrical Parameters

| PARAMETER | SYMBOL | MIN (NOTE 1) | TYP | MAX (NOTE 1) | UNITS |
|--|-----------------|--------------|------|--------------|-------|
| Digital Inputs | | | | | |
| Input High Voltage (TTL) | V _{IH} | 2.0 | | 3.6 | V |
| Input Low Voltage (TTL) | V _{IL} | -0.3 | | 0.8 | V |
| Input Leakage Current (@V _I = 2.5V or 0V) | I _L | | | ±10 | µA |
| Input Capacitance | C _{IN} | | 6 | | pF |
| Digital Outputs | | | | | |
| Output High Voltage | V _{OH} | 2.4 | | | V |
| Output Low Voltage | V _{OL} | | | 0.4 | V |
| High Level Output Current (@V _{OH} = 2.4V) | I _{OH} | 9.3 | 18.2 | 29.2 | mA |
| Low Level Output Current (@V _{OL} = 0.4V) | I _{OL} | 7.4 | 11.8 | 16.5 | mA |
| Tri-state Output Leakage Current (@V _O = 2.5V or 0V) | I _{oz} | | | ±10 | µA |
| Output Capacitance | C _O | | 6 | | pF |
| Analog Pin Input Capacitance | C _A | | 6 | | pF |

NOTE :

- Parameters with MIN and/or MAX limits are tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Supply Current and Power Dissipation

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|------------------|-----|-------|-----|-------|
| Analog Video Supply Current (VDDV, 3.3V) | I _{DDV} | | 110 | | mA |
| Analog Audio Supply Current (VDDA, 3.3V) | I _{DDA} | | 37 | | mA |
| Digital Internal Supply Current (VDD12, 1.2V) | I _{DDI} | | 190 | | mA |
| Digital I/O Supply Current (VDDV, 3.3V) | I _{DDS} | | 4 | | mA |
| PCIe Core Current (VP, 1.2V) | I _{VP} | | 21 | | mA |
| PCIe IO Current (VPH, 3.3V) | I _{VPH} | | 21 | | mA |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Ambient Operating Temperature (H version only) | | -40 | | +85 | °C |
| Total Power Dissipation | P | | 820.7 | | mW |

Video Decoder Parameter 1

| PARAMETER | SYMBOL | MIN (NOTE 1) | TYP | MAX (NOTE 1) | UNITS |
|----------------------------------|------------------|--------------|---------|--------------|-------|
| ADCs | | | | | |
| ADC Resolution | ADCR | | 10 | | Bits |
| ADC Integral Non-linearity | AINL | | ±1 | | LSB |
| ADC Differential Non-Linearity | ADNL | | ±1 | | LSB |
| ADC Clock Rate | f _{ADC} | 24 | 27 | 30 | MHz |
| Video Bandwidth (-3db) | BW | | 10 | | MHz |
| Horizontal PLL | | | | | |
| Line Frequency (50Hz) | f _{LN} | | 15.625 | | kHz |
| Line Frequency (60Hz) | f _{LN} | | 15.734 | | kHz |
| Static Deviation | Δf _H | | | 6.2 | % |
| Subcarrier PLL | | | | | |
| Subcarrier Frequency (NTSC-M) | f _{sc} | | 3579545 | | Hz |
| Subcarrier Frequency (PAL-BDGHI) | f _{sc} | | 4433619 | | Hz |
| Subcarrier Frequency (PAL-M) | f _{sc} | | 3575612 | | Hz |
| Subcarrier Frequency (PAL-N) | f _{sc} | | 3582056 | | Hz |
| Lock In Range | Δf _H | | | | Hz |
| Oscillator Input | | | | | |
| Nominal Frequency | | | 27 | | MHz |
| Deviation | | | | ±50 | ppm |
| Duty cycle | | | | 55 | % |

NOTE :

- Parameters with MIN and/or MAX limits are tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Video Decoder Parameter 2

| PARAMETER | SYMBOL | MIN (NOTE 1) | TYP | MAX (NOTE 1) | UNITS |
|--------------------------------|--------|-----------------|------|-----------------|--------|
| Lock Specification | | | | | |
| Sync Amplitude Range | | 1 | | 200 | % |
| Color Burst Range | | 5 | | 200 | % |
| Horizontal Lock Range | | -5 | | 5 | % |
| Vertical Lock Range | | 45 | | 65 | Hz |
| Fsc Lock Range | | | ±450 | | Hz |
| Color Burst Position Range | | | ±2.2 | | µs |
| Color Burst Width Range | | 1 | | | cycle |
| Video Bandwidth | | | | | |
| B/W | | | 6 | | MHz |
| Noise Specification | | | | | |
| SNR (Luma Flat Field) | | | 57 | | dB |
| Nonlinear Specification | | | | | |
| Y Nonlinearity | | | 0.5 | 0.7 | % |
| Differential Phase | DP | | 0.4 | 0.6 | Degree |
| Differential Gain | DG | | 0.6 | 0.8 | % |
| Chroma Specification | | | | | |
| Hue Accuracy | | | 1 | | Degree |
| Chroma ACC Range | | | | 400 | % |
| Chroma Amplitude Error | | | 1 | | % |
| Chroma Phase Error | | | 0.3 | | % |
| Chroma Luma Intermodulation | | | 0.2 | | % |
| K-Factor | | | | | |
| K2T | | | 0.5 | | % |
| Kpulse/bar | | | 0.5 | | % |

NOTE :

- Parameters with MIN and/or MAX limits are tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Analog Audio Parameters

| PARAMETER | SYMBOL | MIN (NOTE 3) | TYP | MAX (NOTE 3) | UNITS |
|---|--------------------|--------------|-----|--------------|-------|
| Analog Audio Input Characteristics | | | | | |
| AIN1-4 Input Impedance | RINX | 10 | | | kΩ |
| Interchannel Gain Mismatch | | | 0.2 | | dB |
| Input Voltage Range | | | | 2 | Vpp |
| Full Scale Input Voltage (Note 1) | V _{IFULL} | | 1 | | Vpp |
| Interchannel Isolation (Note 2) | | | 90 | | dB |

NOTES:

1. Tested at input gain of 0 dB, Fin = 1kHz.
2. Tested at input gain of 0 dB, Fs = 8 kHz and 16kHz.
3. Parameters with MIN and/or MAX limits are tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Audio Decimation Filter Response

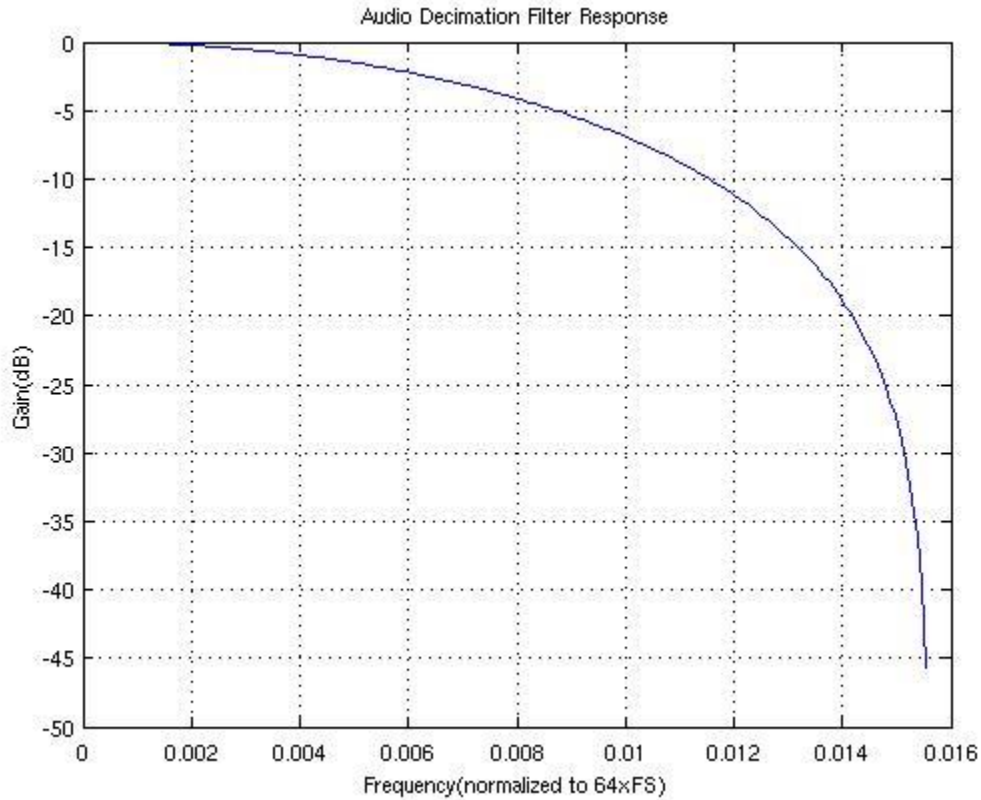
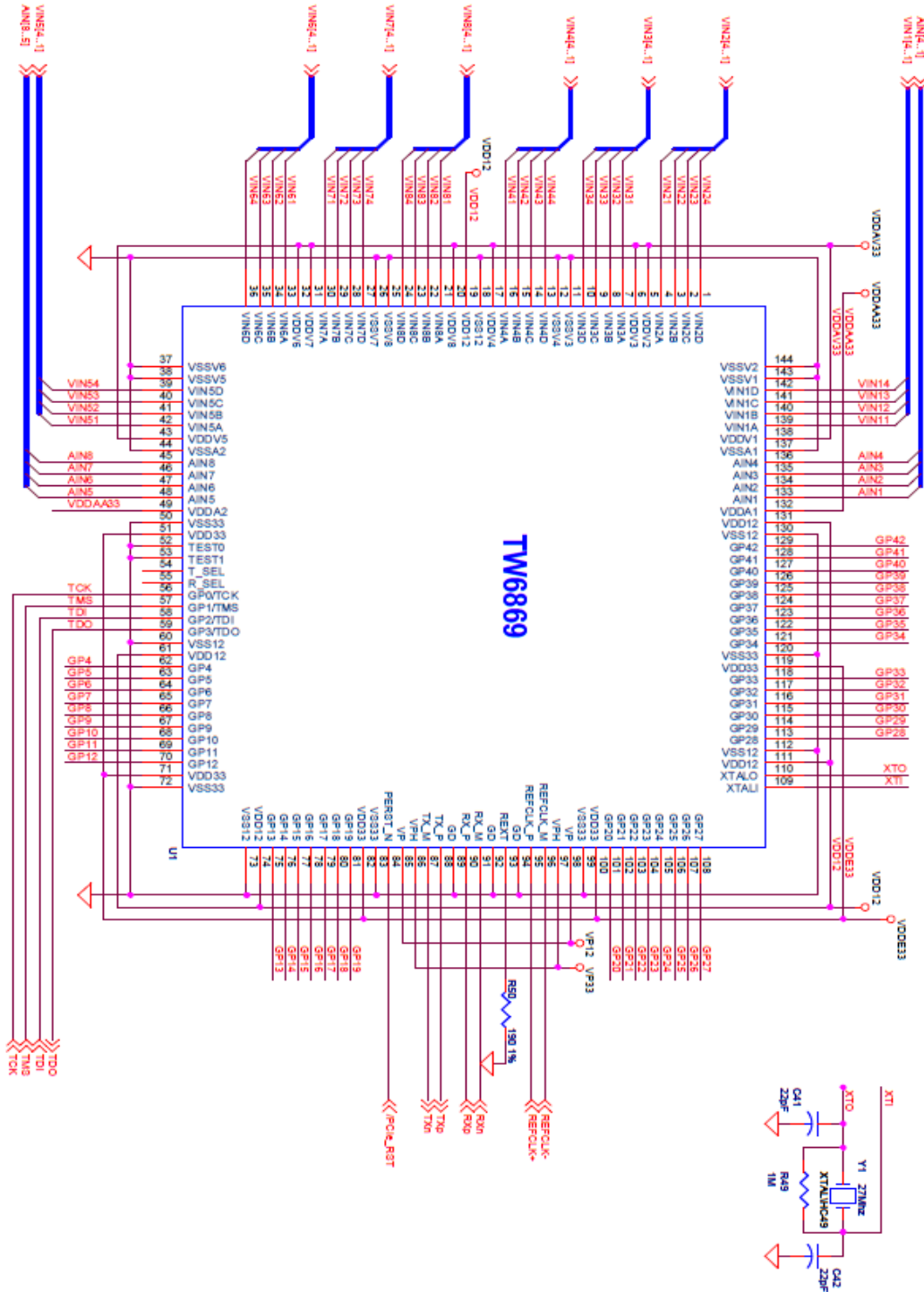


FIGURE 9. (*) 0.016 LINE = 0.016X64XFS

Application Schematic

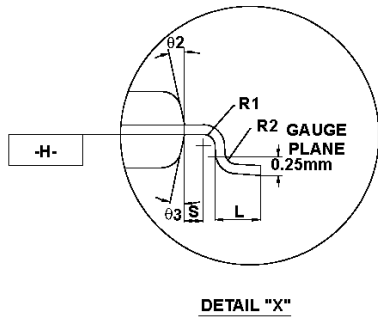
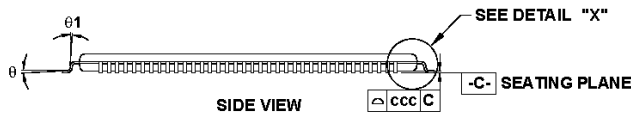
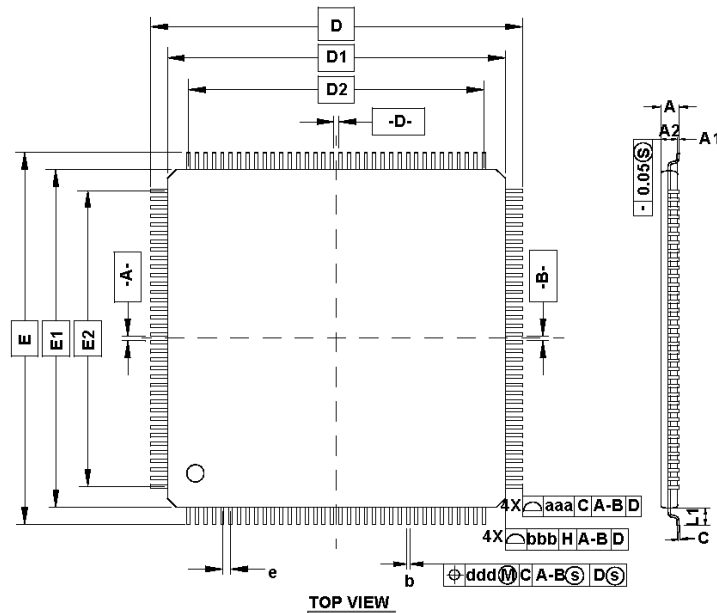


Package Outline Drawing

Q144.20x20C

144 LEAD THIN QUAD FLATPACK PACKAGE (TQFP)

Rev 0, 2/12



| SYMBOL | MILLIMETERS | | | MILLIMETERS | | |
|--------|-------------|------|------|-------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.00 | 1.10 | 1.20 | 0.039 | 0.043 | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| D | 22.00 BSC | | | 0.866 BSC | | |
| D1 | 20.00 BSC | | | 0.787 BSC | | |
| E | 22.00 BSC | | | 0.866 BSC | | |
| E1 | 20.00 BSC | | | 0.787 BSC | | |
| R2 | 0.08 | - | 0.20 | 0.003 | - | 0.008 |
| R1 | 0.08 | - | - | 0.003 | - | - |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | - | - | 0° | - | - |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 | 0.004 | - | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | - | - | 0.008 | - | - |

| SYMBOL | 144L | | | | | |
|---------------------------------|-------------|------|------|-------------|-------|-------|
| | MILLIMETERS | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| D2 | 17.50 | | | 0.689 | | |
| E2 | 17.50 | | | 0.689 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

NOTES:

- Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
- Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
- Control dimensions are in millimeters.

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Revision History

TABLE 3 DATASHEET REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|----------|--------------------|--|
| FN7867.2 | September 26, 2016 | Updated part marking for TW6869-TA1-CRH to be TW6869 TA1-CRH and about Intersil section. |
| FN7867.1 | February 29, 2012 | Initial release |

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