

NTSC/PAL/SECAM Video Decoder with Component Input and Progressive Output Support

TW9912

Features

Video decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Software selectable analog input control
- Built-in analog anti-alias filter.
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for the Y channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, and sharpness.
- Automatic color control and color killer
- Chroma IF compensation
- Detection of level of Macrovision copy protection
- VBI slicer supporting CC and WSS data services

- VBI data pass through, raw ADC data output

Programmable output cropping *Analog Video Input*

- Triple 10-bit ADCs with independent clamping and gain control
- Supports 480i/480p/576i/576p analog component input with SOG

Digital Output

- ITU-R 656 compatible YCbCr(4:2:2) output format
- Progressive ITU-R 656 output format support for both interlaced and progressive inputs.

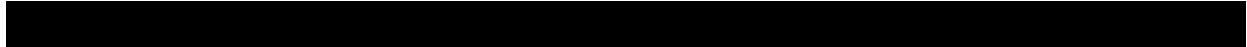
Miscellaneous

- Two wire MPU serial bus interface
- Power save and Power down mode
- Low power consumption
- Single 27MHz crystal for all operations
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format decoding
- 3.3V tolerant I/O
- 1.8V/3.3 V power supply
- 48pin QFN package

Order Information

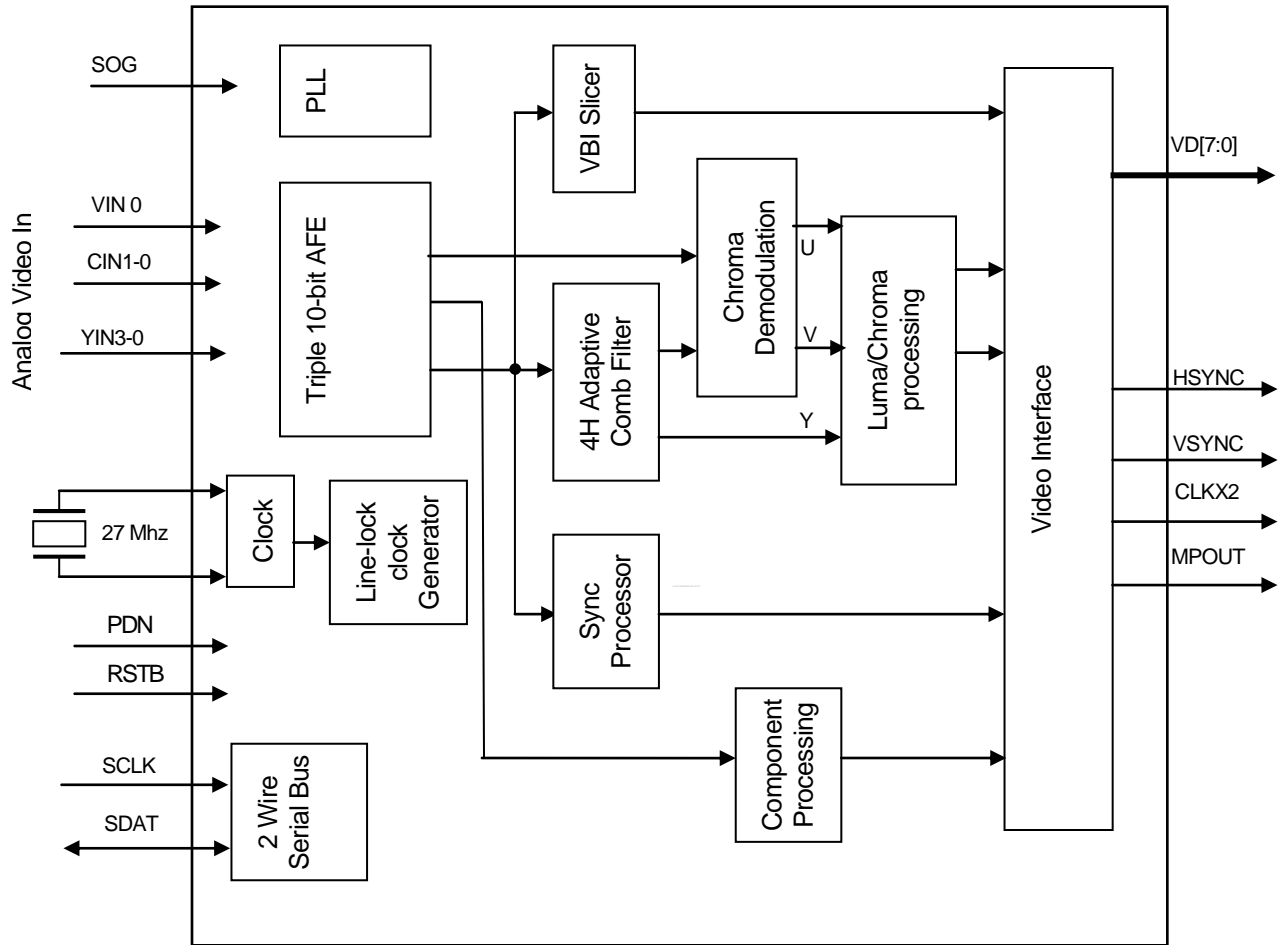
Package Description

Part #	Name	Description	Pin Count	Body Size
TW9912-DBNA1-GR	QFN 48	Quad Flat No-Lead Package	48	7 x 7 mm ²



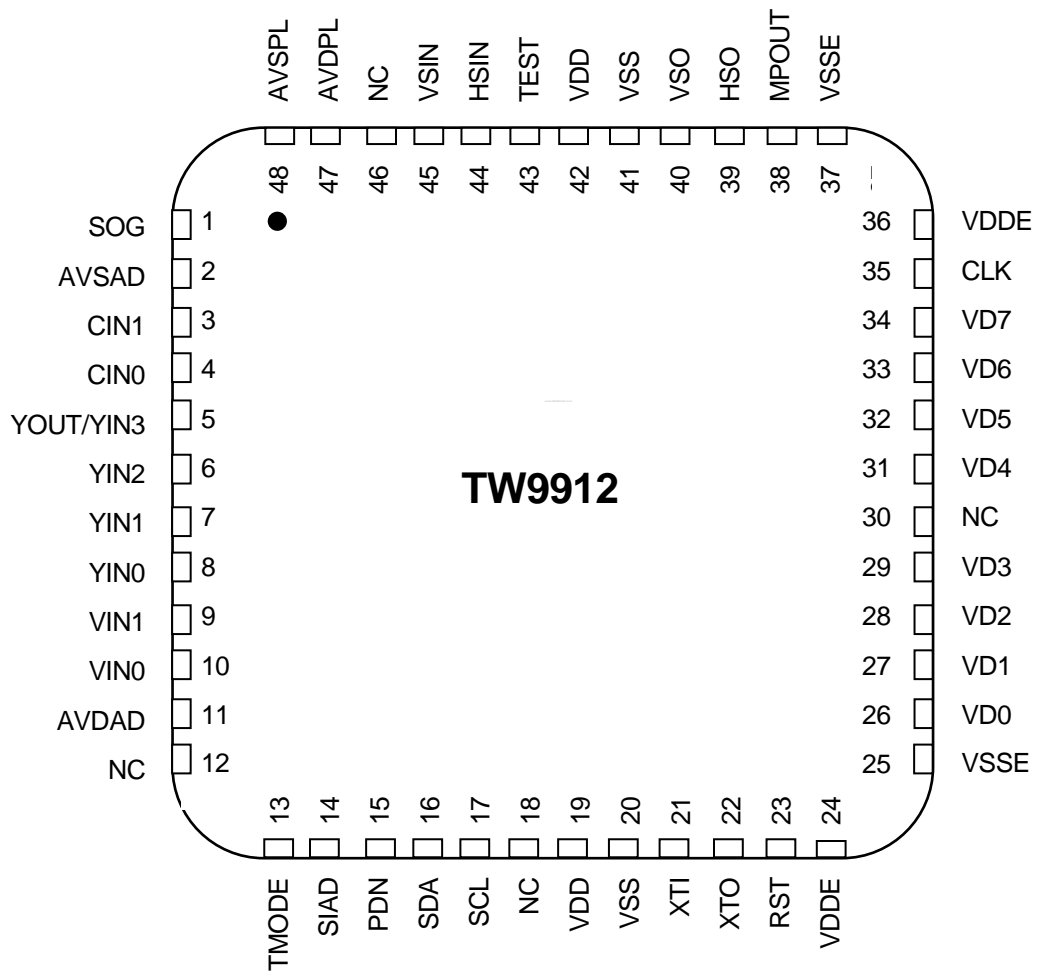
Functional Description

Figure 1: TW9912 Block Diagram



Pin Diagram

48 PIN QFN



Pin Description

Pin#	I/O	Pin Name	Description
Analog video signals			
1	I	SOG	Sync-on-Green input for use with 480p/576p input
3	I	CIN1	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
4	I	CIN0	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
5	I/O	YOUT /YIN3	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor. In output mode, it outputs selected Y input.
6	I	YIN2	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor.
7	I	YIN1	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor.
8	I	YIN0	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor.
9	I	VIN1	Analog Cr input. Connect unused input to AGND through 0.1uF capacitor.
10	I	VIN0	Analog Cr input. Connect unused input to AGND through 0.1uF capacitor.
Clock Signals			
21	I	XTI	Clock input. A 27MHz fundamental (or 3rd overtone) crystal or a single-ended oscillator can be connected.
22	O	XTO	Clock output or used with XTI for form the crystal oscillator.
Host Interface			
17	I	SCLK	The MPU Serial interface Clock Line.
16	I/O	SDAT	The MPU Serial interface Data Line.
14	I	SIAD	The MPU Serial interface address selection.
General signals			
23	I	RSTB	Low active hardware reset pin
15	I	PDN	High active power down control pin.
13	I	TMODE	Test mode control pin. Should be tied to GND for normal operation.
43	I	TEST	Test mode control pin. Should be tied to GND for normal operation.
44	I	HSIN	Reserved for test purpose
45	I	VSIN	Reserved for test purpose.
Video output Signals			
38	O	MPOUT	Multi-purpose output pin. The output function can be selected by RTSEL of register 0x19
39	O	HSYNC	Horizontal sync and multi-purpose output pin. See register for control information.
40	O	VSYNC	Vertical Sync and multi-purpose output. See register for control information.
35	O	CLKO	Data Clock output. See register for control information.

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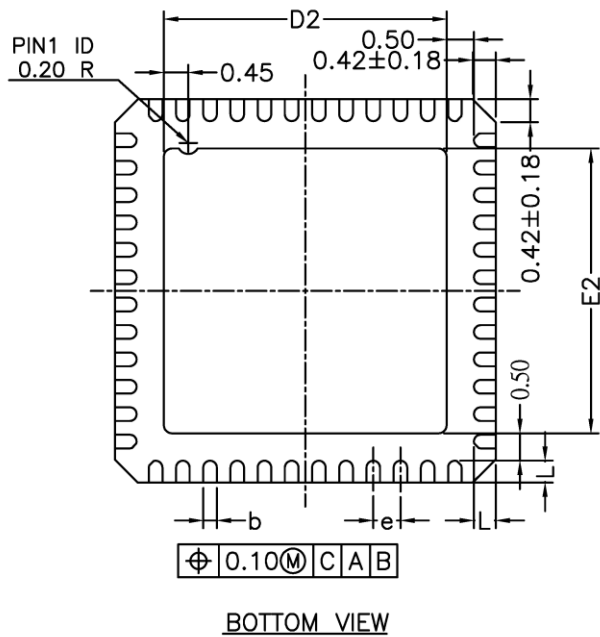
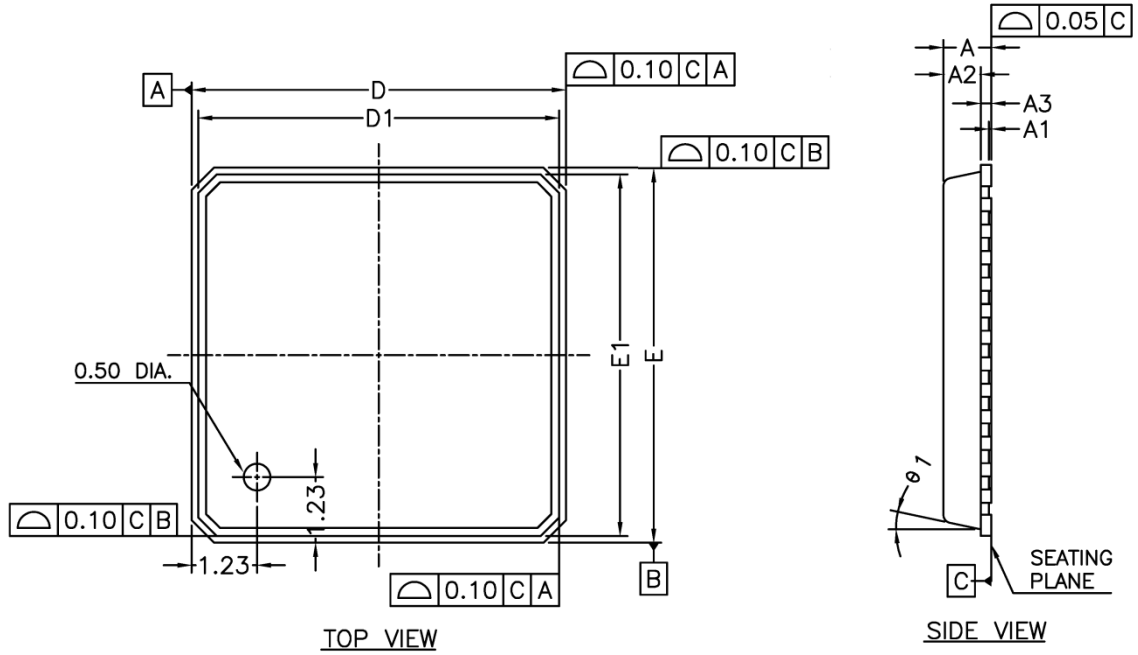
Pin#	I/O	Pin Name	Description
34 33 32 31 29 28 27 26	I/O	VD[7-0]	Digitized video data output of 4:2:2 YCbCr. VD[7] is the MSB.
12,18,30,46		NC	No connection

Power and Ground Pins

Pin#	I/O	Pin Name	Description
19,42	I	VDD	1.8V digital core power.
20,41	I	VSS	1.8V digital core return
25, 36	I	VDD33	3.3V digital I/O power.
24, 37	I	VSS33	3.3V digital I/O return
11	I	AVD	1.8V analog ADC supply
2	I	AVS	1.8V analog ADC return
47	I	AVDPLL	1.8V PLL supply
48	I	AVSPLL	1.8V PLL return

Mechanical Data

48 PIN QFN



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.2 REF.			0.008 REF.		
b	0.20	0.25	0.32	0.008	0.010	0.013
D	7.00 BSC.			0.276 BSC.		
D1	6.75 BSC.			0.266 BSC.		
D2	5.00	5.20	5.40	0.197	0.205	0.213
E	7.00 BSC.			0.276 BSC.		
E1	6.75 BSC.			0.266 BSC.		
E2	5.00	5.20	5.40	0.197	0.205	0.213
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 BSC.			0.020 BSC.		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

* CONTROLLING DIMENSION : MM

NOTES:

1. All dimensions are in millimeters.
2. Dimension applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
3. Package warpage MAX 0.08mm.
4. Package corners unless otherwise specified are R0.175± 0.025mm