TENTATIVE

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HITACHI

LIQUID CRYSTAL DISPLAY MODULE
TECHNICAL DATA
4.01" 345(RGB)*800 Module (60 pins)
(TX10D04VM0AAA)

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(NOTES)

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RECORD OF REVISIONS

Date	Sheet No.	Summary

3. GENERAL SPECIFICATIONS

(1)	Product Name	TX10D04VM0AAA
(2)	Module Dimensions	45.1 (W) mm × 103.6 (H) mm × 1.7 (t) mm (Excluding I/F-FPC and electronic components)
(3)	Active Area Dimensions	40.365 (W) mm × 93.6 (H) mm
(4)	Pixel Pitch	0.117 (W) mm × 0.117 (H) mm
(5)	Resolution	345 × 3 (R, G, B) (W) × 800 (H) dots
(6)	Color Pixel Arrangement	RGB Vertical Stripe
(7)	Display Mode	Transmissive Type, Normally Black Mode, In-Plane Switching Mode
(8)	Number of Colors	262,144 Colors / 16,777,216 Colors
(9)	Viewing Direction	-
(10)	Backlight	Light Emitting Diode (LED), 6 LEDs are parallel connection Backlight current : 20 mA/LED (typ)
(11)	Weight	20g
(12)	Power Supply Voltage Note (1)	Vcc = 2.8+/-0.1 V , DDVDH = 2.8+/-0.1 V
(13)	Interface I/O Power Supply Note (2)	IOVcc = 1.8+/-0.1 V The same voltage as "H" level of a customer's interface signal must be supplied to IOVcc.
(14)	LCD Driver IC	BD663478 (Source and Power IC) BD663432 (Gate)x2
(15)	Interface	18-bit/24-bit RGB Interface + SPI (Clock synchronous serial interface)
(16)	RoHS, Halogen free	This product is halogen-free product and comply with RoHS directive.

Note (1) IOVCC is the reference voltage for adjusting the I/O signal level of BD663478 & BD663432. IOVCC voltage must be determined according to a customer's system.

Note (2) DDVDH must be configured so that it is at the same potential level as Vcc and connected to a separate power supply.

4. ABSOLUTE MAXIMUM RATINGS

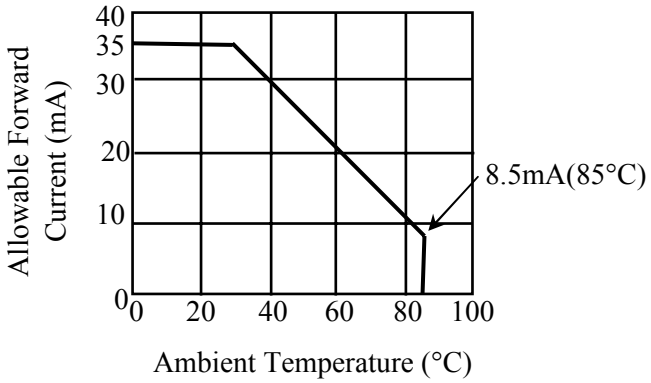
4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD VSS = 0 V, Ta = 25°C

Item	Symbol	Min.	Max.	Unit	Note
Power Supply for Interface	IOVcc	-0.3	3.6	V	(1)
Power Supply for Logic and Analog	Vcc DDVDH	-0.3	3.6	V	(1)
Input Voltage	Vi	-0.3	IOVcc+0.3	V	(2)
LED Reverse Voltage	VR	-	5	V	
LED Forward Current	ILED	-	Note (3)	mA	per LED
Static Electricity	-	-	±2	kV	(4)

Notes (1) Keep all Voltages no lower than GND.

(2) Applies to the SCL , DOTCLK , HSYNC , VSYNC , ENABLE , SDI , CS , RESET and D0 to D23.

(3) Ambient Temperature vs. Allowable Forward Current



(4) 100pF-1.5 kohm, 25°C-70%RH
Static electricity discharge is to be aimed at the center of the active area.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Remarks
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	70°C	-30°C	80°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C 85%RH max.
Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.

(2) Background color slightly changes depending on ambient temperature and viewing angle.
The speed of response is slower at 0°C.
The temperature for operating in the table above apply to operation only.
Visual qualities, such as contrast and speed of response,
to be evaluated at Ta = 25°C Operating.

5. ELECTRICAL CHARACTERISTICS

LCD Module VSS=0 V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage for I/O interface	IOVcc	-	1.7	1.8	1.9	V	-
Power Supply Voltage for Logic and Analog	Vcc DDVDH	-	2.7	2.8	2.9	V	(1)
Input Voltage for Logic Circuits	Vi	"H" level	0.80 × IOVcc	-	I/OVcc	V	(2), (3)
		"L" level	0	-	0.20 × IOVcc		
Output Voltage for Logic Circuits	Vo	"H" level	0.80 × IOVcc	-	-	V	(2), (3)
		"L" level	-	-	0.20 × IOVcc		
Input / Output Leak Current	ILi	-	-1.0	-	1.0	µA	
Power Supply Current	Icc	All White	-	3.1	3.85	mA	(4), (6)
		Deep Standby	-	0.1	10.0	µA	(5), (7)
	DDVDH	All White	-	10.8	13.2	mA	(4), (6)
		Deep Standby	-	0.1	10.0	µA	(5), (7)
LED Forward Voltage	VLED	-	-	3.2	3.5	V	(8)
LED Forward Current	ILED	-	-	20	Note (9)	mA	(8)
LED Reverse Current	IR	-	-	-	50	µA	(8)

Notes (1) DDVDH must be configured so that it is at the same potential level as Vcc and connected to a separate power supply.

(2) IOVcc = 1.7V to 1.9V

(3) Input : SCL , DOTCLK , HSYNC , VSYNC , ENABLE , SDI , CS , RESET and D0 to D23
Output : Maker ID , LEDPWM and SDO

(4) IOVcc = 1.8V , Vcc = DDVDH = 2.8 V, fFLM = 95 Hz, Frame inversion mode.

(5) IOVcc = 1.8V , Vcc = DDVDH = 2.8 V, Deep standby mode.

(6) Operation Mode : Refer to Item 8.4.1, State (b).

(7) Operation Mode : Refer to Item 8.4.1, State (d).

(8) Shows the value per LED.

(9) The operating current of LED should be determined within the maximum rating of the temperature environmental condition.

6. OPTICAL CHARACTERISTICS

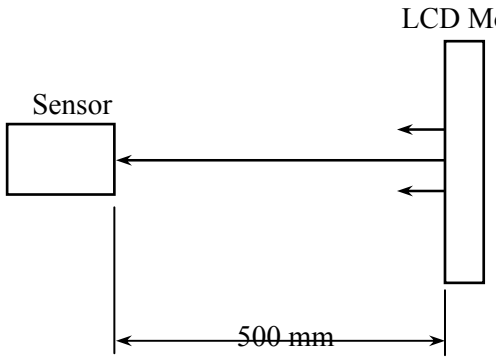
LCD (With Front window and Touch Panel , BACKLIGHT ON)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness		B	φ=0°, θ=0°	300	400	-	cd/m²	(1), (2)
Brightness Uniformity		-	φ=0°, θ=0°	80	85	-	%	(2), (3), (5)
Viewing angle		φ1+φ2	θ=0°, CR≥10	-	170	-	deg	(4), (6), (7)
			θ=90°, CR≥10	-	170	-		
Contrast Ratio		CR	φ=0°, θ=0°	300	500	-	-	(6)
Response time		tr + tf	φ=0°, θ=0°	-	35	60	ms	(8)
Color Tone (Primary Color)	Red	x	φ=0°, θ=0°	0.57	0.64	0.71	-	-
		y		0.27	0.34	0.41		
	Green	x		0.26	0.33	0.40		
		y		0.56	0.63	0.70		
	Blue	x		0.08	0.15	0.22		
		y		0.03	0.10	0.17		
NTSC Ratio		-	φ=0°, θ=0°	62	67	-	%	-

Measurement Conditions

Measurement environment : Dark room
Ambient temperature : Ta=25°C
Sequence : Refer to Item 8.4.1 State (b)
Power supply voltage : IOVcc = 1.8V , Vcc = DDVDH = 2.8V
Backlight current : I_{LED} = 20 mA/1LED

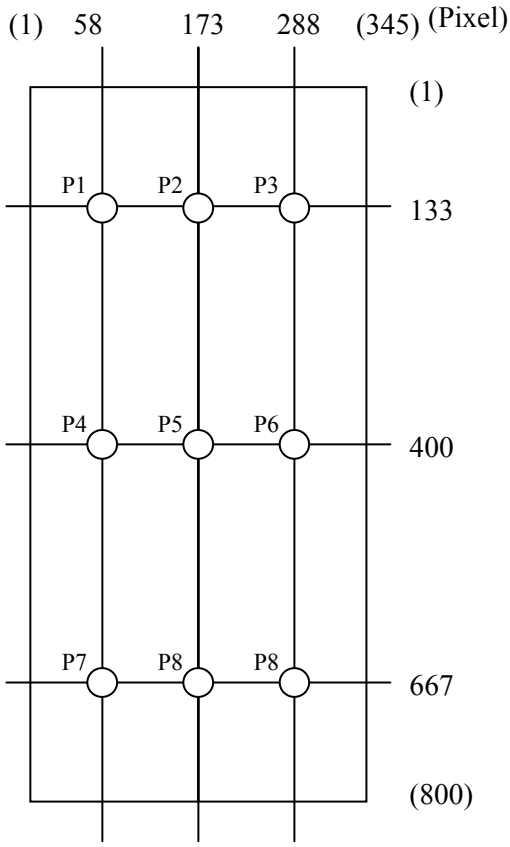
Notes (1) Definition of Brightness "B"



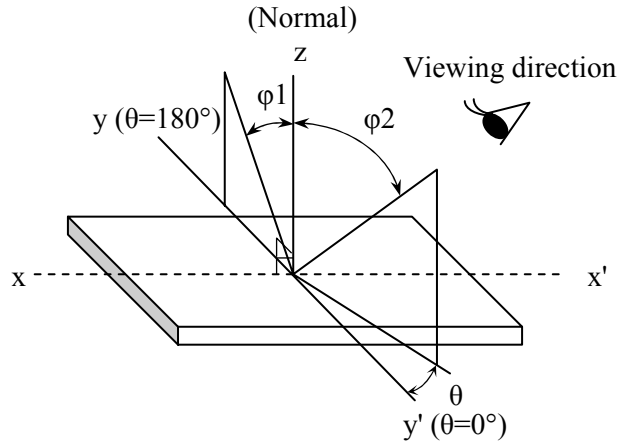
Sensor : MINOLTA's CS-1000 or equivalent
Measuring point : Center of LCD's active area

(2) Display image for measurement : All White

(3) Measurement point



Notes(4) Definition of θ and φ



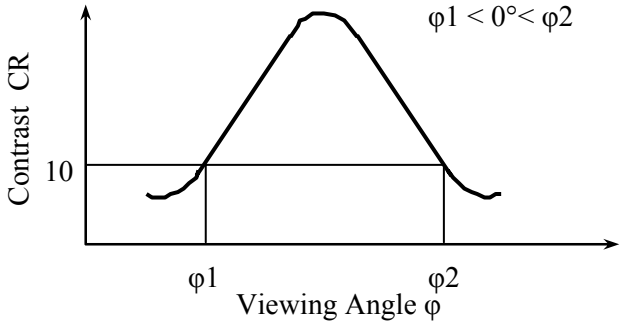
(5) Definition of Brightness Uniformity

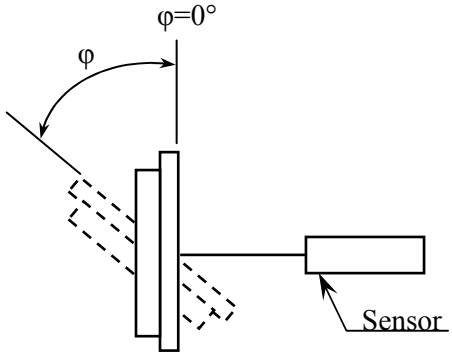
$$\text{Brightness Uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\ (\%)$$

(6) Definition of Contrast "CR"

$$\text{CR} = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

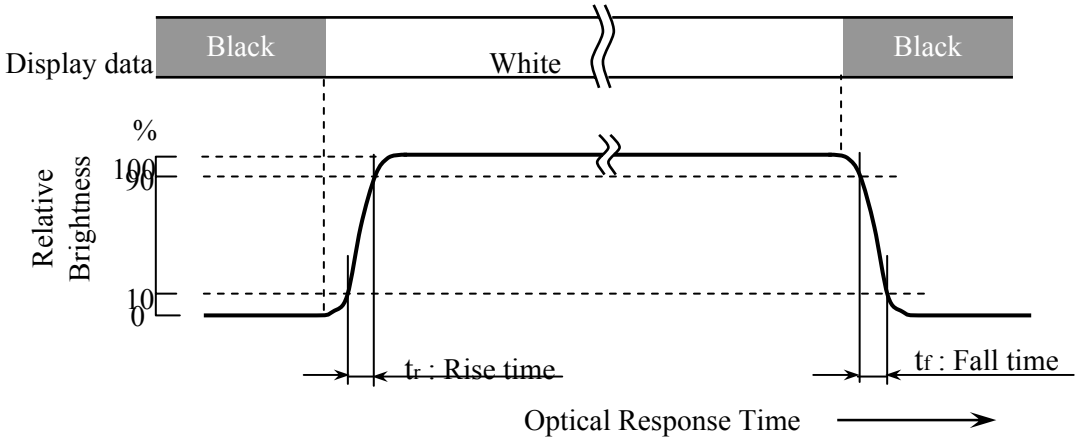
(7) Definition of Viewing Angle φ1 and φ2



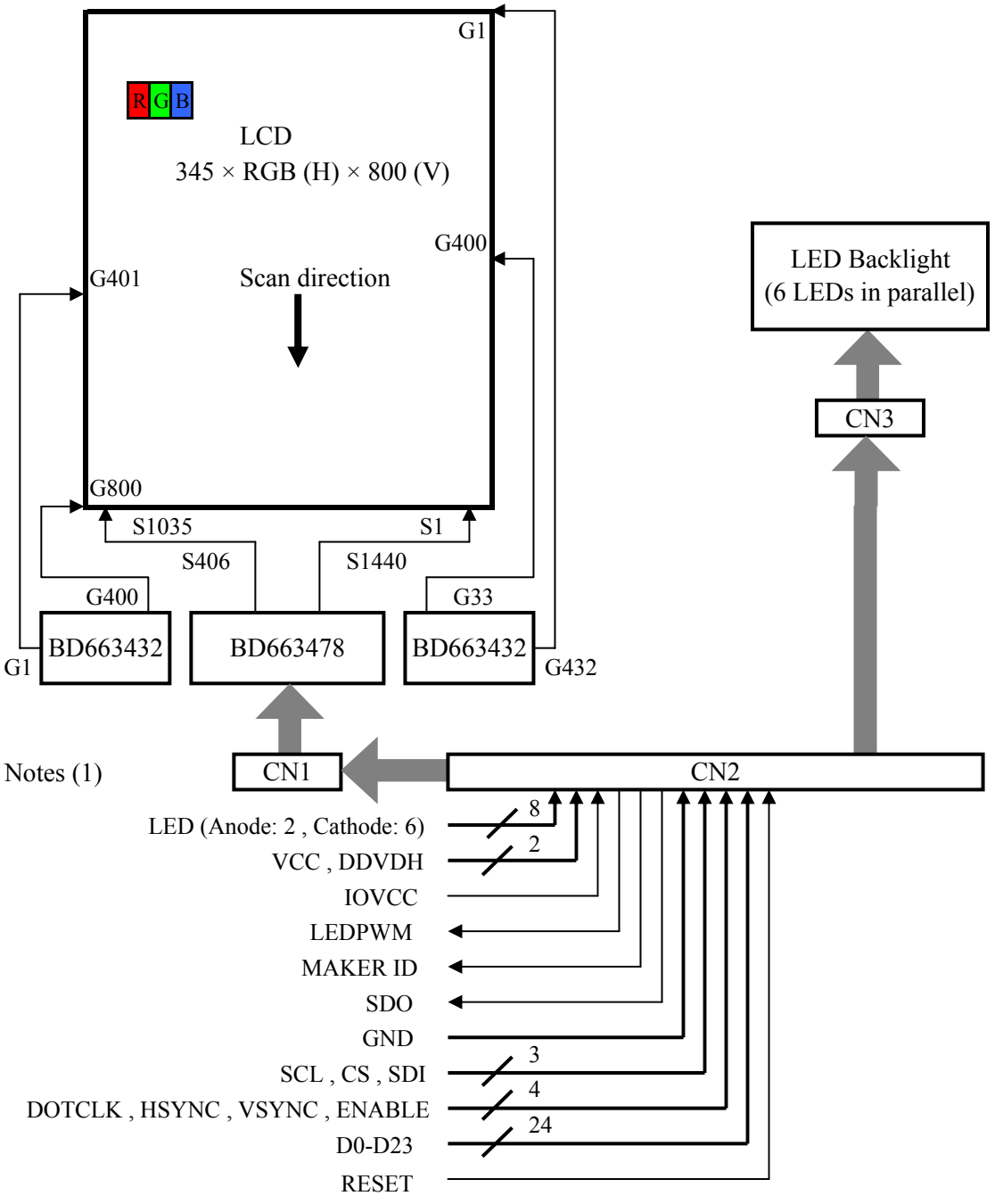


Sensor : TOPCON's BM-5A or equivalent

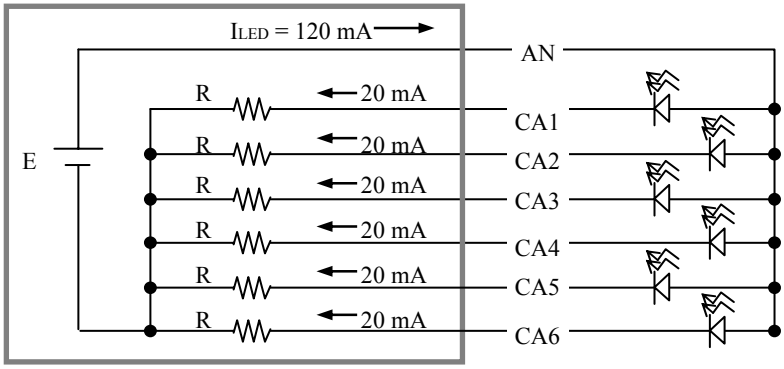
(8) Definition of Optical Response Time



7. BLOCK DIAGRAM



(2) Please connect the resistor (R = 200 ohm) for current control between LED (cathode) and GND in the customer's system.



8. INTERFACE

8.1 INTERNAL PIN CONNECTION

Pin No.	Signal	I/O	Function	Driver's Signal name
1	AN(LED)	-	Power Supply for LED	-
2	CA1(LED)	-	GND for LED	-
3	CA3(LED)	-	GND for LED	-
4	CA5(LED)	-	GND for LED	-
5	MAKER ID(Low)	O	Maker ID(Low: GND level)	-
6	IOVCC	-	Power Supply for Interface (1.8V)	-
7	OPEN	-	OPEN (Hitachi)	-
8	LEDPWM	O	Dimmer Control Signal for LED Driver	LEDPWM
9	SCL	I	Synchronous clock signal	SCL
10	SDO	O	Serial data output	SDO
11	DOTCLK	I	Dot Clock Signal	PCLK
12	HSYNC	I	Line Synchronous Signal	HSYNC
13	ENABLE	I	Data Enable Signal for When RGB Interface is selected	EN
14	RESET	I	Reset	RESET*
15	DB0	I	Data Bus (Display data)	DB0
16	DB2	I	Data Bus (Display data)	DB2
17	DB4	I	Data Bus (Display data)	DB4
18	DB6	I	Data Bus (Display data)	DB6
19	DB8	I	Data Bus (Display data)	DB8
20	DB10	I	Data Bus (Display data)	DB10
21	DB12	I	Data Bus (Display data)	DB12
22	DB14	I	Data Bus (Display data)	DB14
23	DB16	I	Data Bus (Display data)	DB16
24	DB18	I	Data Bus (Display data)	DB18
25	DB20	I	Data Bus (Display data)	DB20
26	DB22	I	Data Bus (Display data)	DB22
27	GND	-	GND	-
28	GND	-	GND	-
29	GND	-	GND	-
30	GND	-	GND	-
31	GND	-	GND	-
32	GND	-	GND	-
33	GND	-	GND	-
34	GND	-	GND	-
35	DB23	I	Data Bus (Display data)	DB23
36	DB21	I	Data Bus (Display data)	DB21
37	DB19	I	Data Bus (Display data)	DB19
38	DB17	I	Data Bus (Display data)	DB17
39	DB15	I	Data Bus (Display data)	DB15
40	DB13	I	Data Bus (Display data)	DB13
41	DB11	I	Data Bus (Display data)	DB11
42	DB9	I	Data Bus (Display data)	DB9
43	DB7	I	Data Bus (Display data)	DB7
44	DB5	I	Data Bus (Display data)	DB5

Pin No.	Signal	I/O	Function	Driver's Signal name
45	DB3	I	Data Bus (Display data)	DB3
46	DB1	I	Data Bus (Display data)	DB1
47	GND	-	GND	-
48	GND	-	GND	-
49	VSYNC	I	Frame synchronous signal	VSYNC
50	GND	-	GND	-
51	GND	-	GND	-
52	SDI	I	Serial data input	SDI
53	CS	I	Chip Select	CS*
54	GND	-	GND	-
55	DDVDH	-	Power Supply for Logic and Analog (2.8V)	-
56	VCC	-	Power Supply for Logic and Analog (2.8V)	-
57	CA6(LED)	-	GND for LED	-
58	CA4(LED)	-	GND for LED	-
59	CA2(LED)	-	GND for LED	-
60	AN(LED)	-	Power Supply for LED	-

LCM Connector : AXT560124 (Panasonic) , Suitable Connector : AXT660124 (Panasonic)

8.2 INTERFACE MODE SETTING

8.2.1 SPI INTERFACE MODE

SPI interface is controled by CS, SCL,and SDI.
The all instructions of this module consist on 8bit x 2transfer (IM pin is fixed to "0" on FPC).
Please transfer index register set or instruction after Device code (6bit) , RS(1bit) and RW (1bit).
Device ID code(6bit) of this module is "011100"(IM pin is fixed to "0" on FPC).

IM(pin)	Interface mode	Remarks
0	SPI (8-bit 2-transfer)	MSB 8 bit only becomes valid within the chip

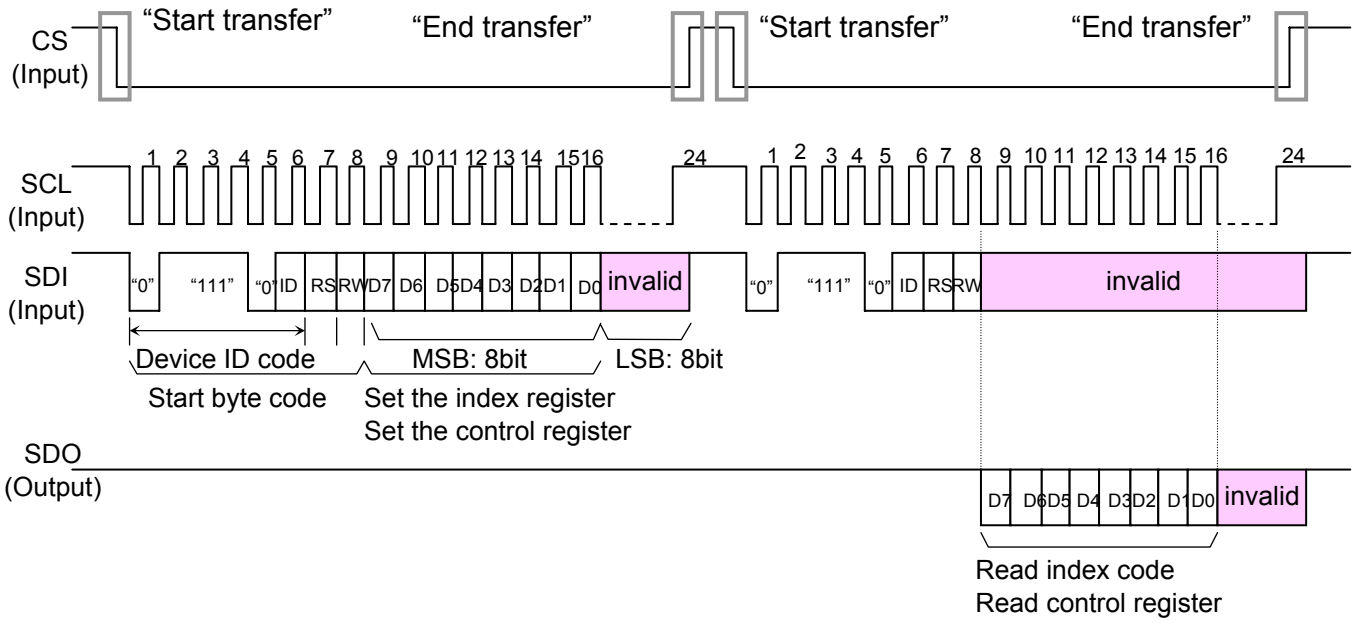
Input bit settings		Internal status of the LSI	D7~0 input							
			D7	D6	D5	D4	D3	D2	D1	D0
RS	RW		↓	↓	↓	↓	↓	↓	↓	↓
0	0	Index register (IB) write	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
1	0	Control register (IB) write	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

Notes (1) IB is a common data bus of the index register and control register.

D7-0 Input Data Allocation at the Time of Write Operation

1	1	Device code read	0	1	1	1	1	0	0	0
RS	RW	Internal status of the LSI	↓	↓	↓	↓	↓	↓	↓	↓
Input bit settings			D7	D6	D5	D4	D3	D2	D1	D0
			D7~0 output							

D7-0 Output Data at the Time of Read Operation



Notes (1) The comparison of the ID values in the start byte codes must be set with the ID pin.
(2) This waveform shall not be construed to determine the timing of the signals.

Basic Input/Output Waveforms of Clock Synchronized Serial (SPI) 8 Bit Interface

8.2.2 RGB INTERFACE MODE

24-bit RGB Interface mode :

RGB Interface Input data	D 23	D 22	D 21	D 20	D 19	D 18	D 17	D 16

Instruction Register settings		RGB Equiv.	R7	R6	R5	R4	R3	R2	R1	R0
SS	BGR									
0	0	Output pin	S(3n + 1)							
0	1		S(3n + 3)							
1	0		S(1438 – 3n)							
1	1		S(1440 – 3n)							

RGB Interface Input data	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8

Instruction Register settings		RGB equiv.	G7	G6	G5	G4	G3	G2	G1	G0
SS	BGR									
0	0	Output pin	S(3n + 2)							
0	1		S(3n + 2)							
1	0		S(1439 – 3n)							
1	1		S(1439 – 3n)							

RGB Interface Input data	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

Instruction Register settings		RGB equiv.	B7	B6	B5	B4	B3	B2	B1	B0
SS	BGR									
0	0	Output pin	S(3n + 3)							
0	1		S(3n + 1)							
1	0		S(1440 – 3n)							
1	1		S(1438 – 3n)							

18-bit RGB Interface mode :

RGB Interface Input data	D 23	D 22	D 21	D 20	D 19	D 18

Instruction Register settings		RGB Equiv.	R7	R6	R5	R4	R3	R2	R1	R0
SS	BGR									
0	0	Output pin	S(3n + 1)							
0	1		S(3n + 3)							
1	0		S(1438 – 3n)							
1	1		S(1440 – 3n)							

RGB Interface Input data	D 15	D 14	D 13	D 12	D 11	D 10

Instruction Register settings		RGB equiv.	G7	G6	G5	G4	G3	G2	G1	G0
SS	BGR									
0	0	Output pin	S(3n + 2)							
0	1		S(3n + 2)							
1	0		S(1439 – 3n)							
1	1		S(1439 – 3n)							

RGB Interface Input data	D 7	D 6	D 5	D 4	D 3	D 2

Instruction Register settings		RGB equiv.	B7	B6	B5	B4	B3	B2	B1	B0
SS	BGR									
0	0	Output pin	S(3n + 3)							
0	1		S(3n + 1)							
1	0		S(1440 – 3n)							
1	1		S(1438 – 3n)							

8.3 INTERFACE TIMING

8.3.1 Clock synchronized Serial Interface Timing Characteristics (Write sequence)

IOVcc = 1.65 to 2.8 V , Vcc = DDVDH = 2.8 V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	tSCYCW	ns	Fig. 1	105	-	19000
Serial clock low-level pulse width	tSCL	ns	Fig. 1	42	-	-
Serial clock high-level pulse width	tSCH	ns	Fig. 1	42	-	-
Serial clock rise/fall time	tSCr/tSCf	ns	Fig. 1	-	-	19
Chip select setup time	tCSU	ns	Fig. 1	21	-	-
Chip select hold time	tCH	ns	Fig. 1	63	-	-
Serial input data setup time	tSISU	ns	Fig. 1	32	-	-
Serial input data hold time	tSIH	ns	Fig. 1	32	-	-

8.3.2 Clock synchronized Serial Interface Timing Characteristics (Read sequence)

IOVcc = 1.65 to 2.8 V , Vcc = DDVDH = 2.8 V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	tSCYCR	ns	Fig. 1	370	-	19000
Serial clock low-level pulse width	tSCL	ns	Fig. 1	160	-	-
Serial clock high-level pulse width	tSCH	ns	Fig. 1	160	-	-
Serial clock rise/fall time	tSCr/tSCf	ns	Fig. 1	-	-	19
Chip select hold time	tCH	ns	Fig. 1	63	-	-
Serial output data setup time	tSOD	ns	Fig. 1	-	-	140
Serial output data hold time	tSOH	ns	Fig. 1	4	-	-

8.3.3 Reset Timing Characteristics

IOVcc = 1.65 to 2.8 V , Vcc = DDVDH = 2.8 V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Reset low-level width	tRES	ms	Fig. 2	2	-	-
Reset rise time	trRES	μs	Fig. 2	-	-	9

8.3.4 RGB Interface Timing Characteristics

IOVcc = 1.65 to 2.8 V , Vcc = DDVDH = 2.8 V

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
PCLK cycle time	tCYCD	ns	Fig. 3	27	-	-
PCLK low-level pulse width	PWDL	ns	Fig. 3	13	-	-
PCLK high-level pulse width	PWDH	ns	Fig. 3	13	-	-
VSYNC setup time	tVSYNCS	clock	Fig. 3	0	-	-
HSYNC setup time	tHSYNCS	clock	Fig. 3	0	-	-
ENABLE setup time	tENS	ns	Fig. 3	6	-	-
ENABLE hold time	tENH	ns	Fig. 3	11	-	-
RGB data setup time	tPDS	ns	Fig. 3	6	-	-
RGB data hold time	tPDH	ns	Fig. 3	11	-	-
PCLK/VSYNC/HSYNC Rise/fall time	trgbr / trgbf	ns	Fig. 3	-	-	9

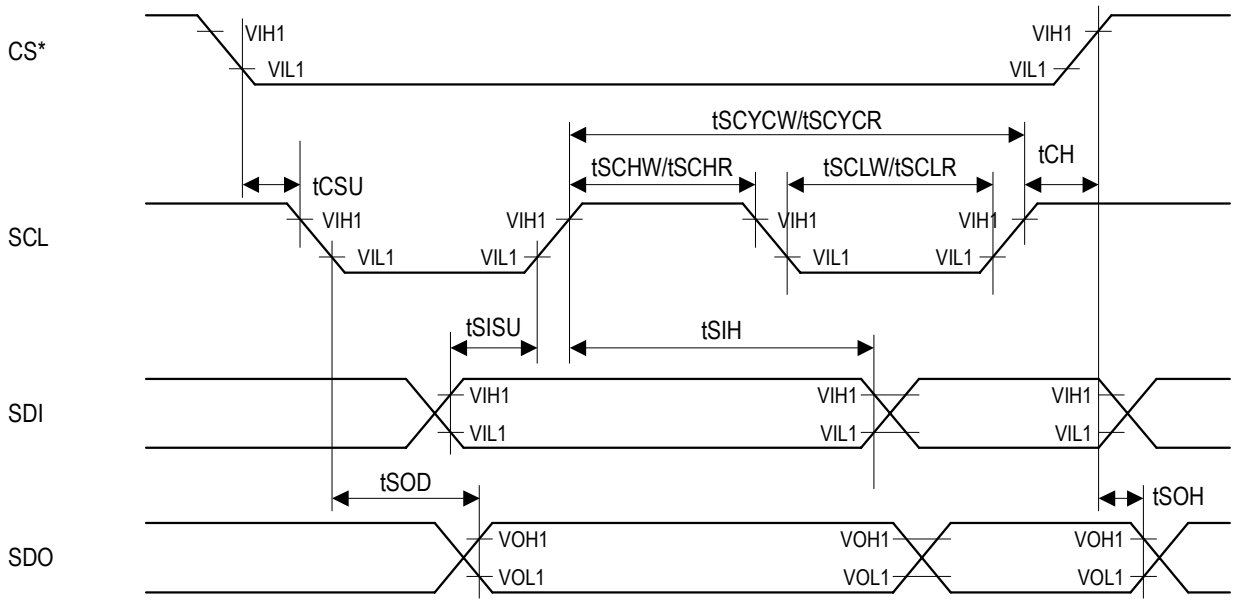


Fig.1 Clock Synchronized Serial Peripheral Interface (SPI) timing

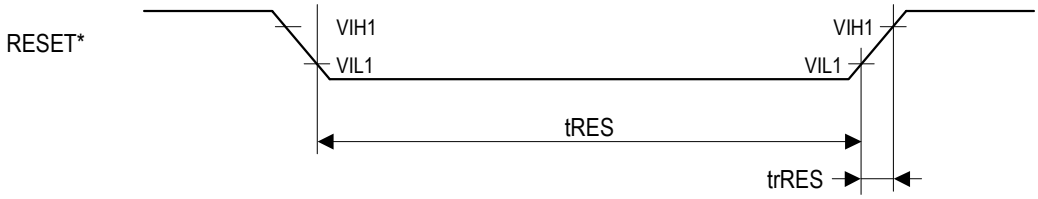


Fig.2 Reset Timing

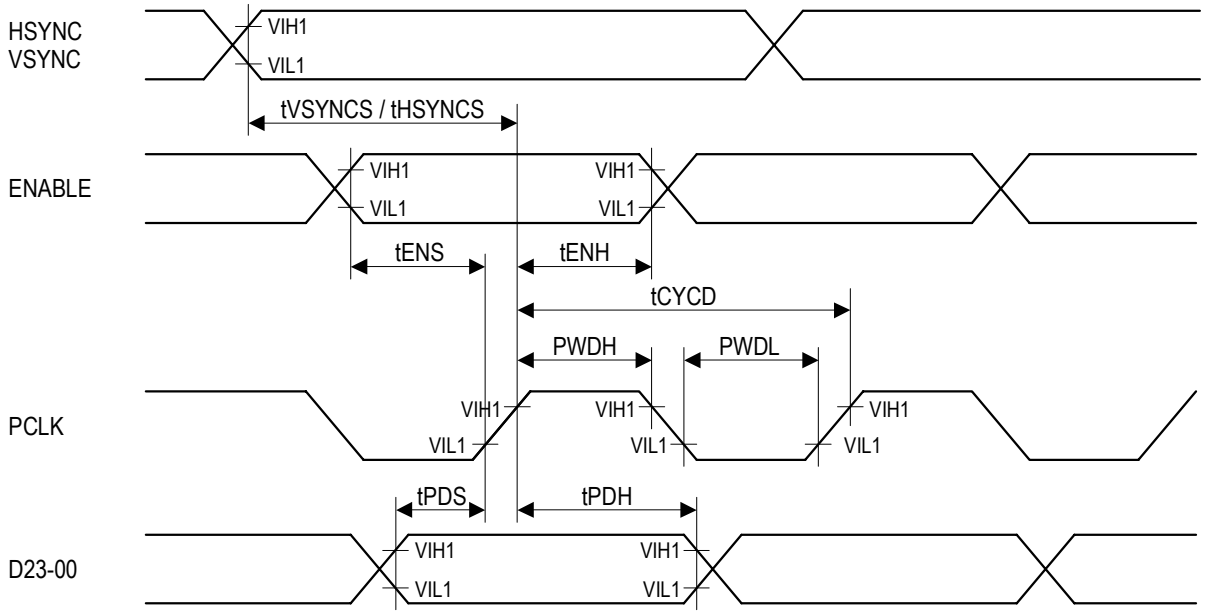
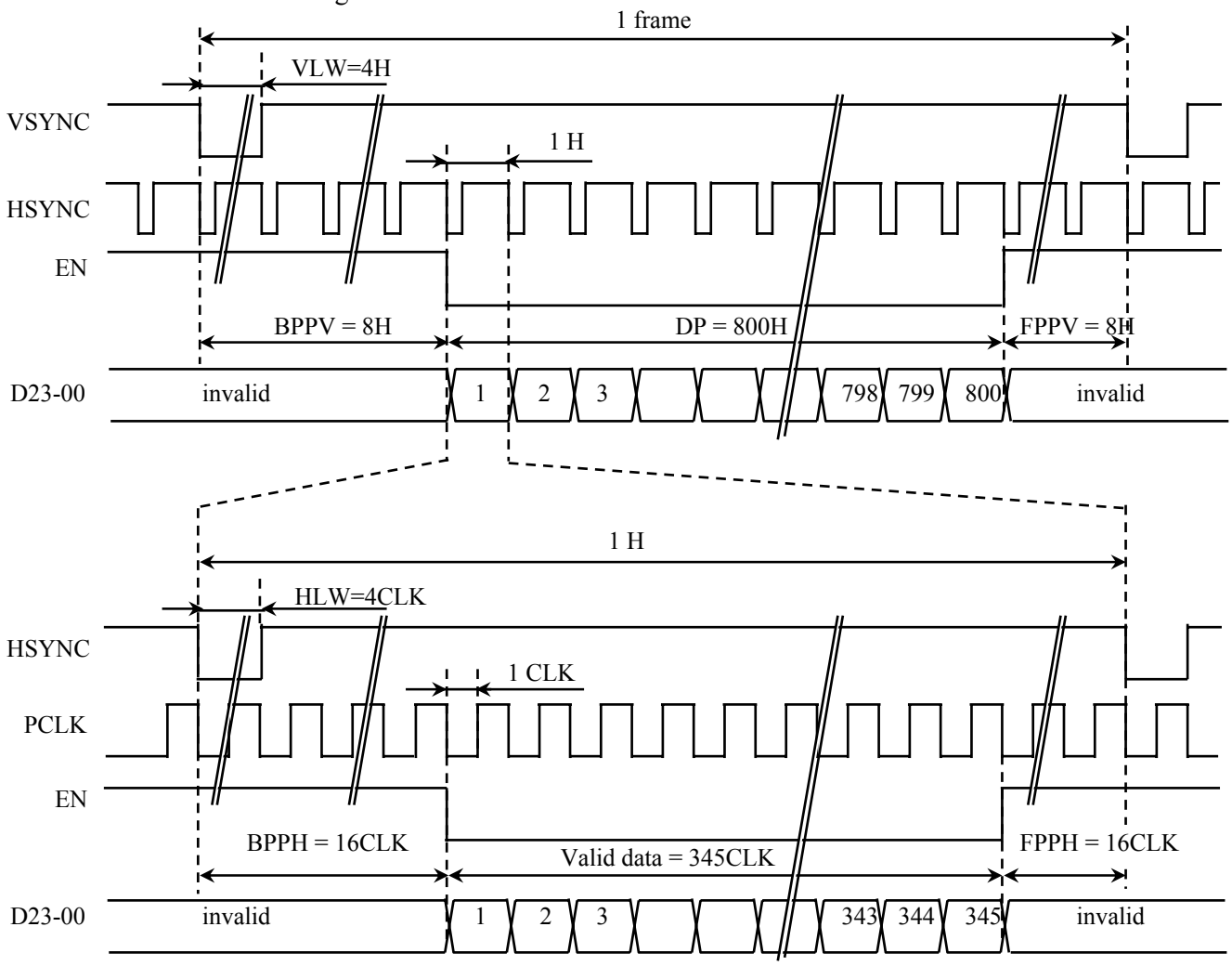


Fig.3 RGB Interface Timing

8.3.5 RGB Interface Timing



BPP : Back porch period
FPP : Front porch period
DP : Display operation period

HLW : The period in which HSYNC is low level
VLW : The period in which VSYNC is low level

(a) PCLK = 29.23MHz

Item	min	typ	max	Unit	Remarks
HLW	1	4	-	CLK	
BPPH	10	16	68	CLK	
FPPH	16	16	100	CLK	
VLW	1	4	-	H	
BPPV	3	8	255	H	
FPPV	8	8	-	H	
DP	-	800	864	H	

(b)

Item	min	typ	max	Unit	Remarks
fFLM	(90)	95	(100)	Hz	
PCLK	27.61	29.23	30.76	MHz	

The number of raster-rows of 1 frame : BPPV + DP + FPPV

fDOTCLK = fFLM x (800+ BPPV + FPPV) x (345 + BPPH + FPPH)

Notes

(1) Dot clock signal (DOTCLK) must be always supplied.
(2) Front and back porch periods must be set before and after the display operation period (DP).
(3) Front porch period continues until the next input of VSYNC signal.
(4) This value is a value that uses a typical value of table (a).
(5) If the relationship of timing of the falling edges of VSYNC and HSYNC is NOT as shown in Figure A below, the vertical back porch must be specified as shown in Figure B.

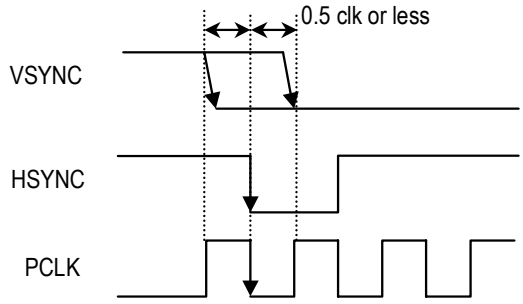


Figure A. VSYNC Timing

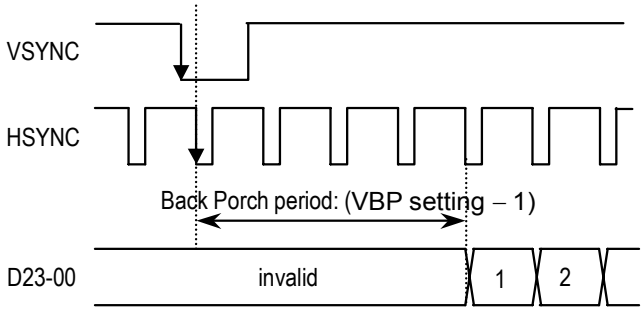
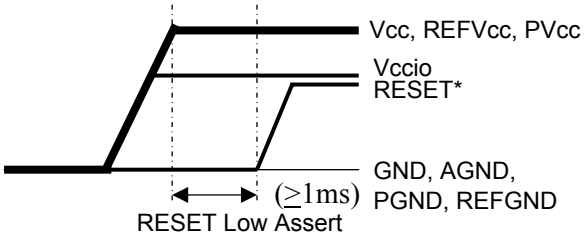


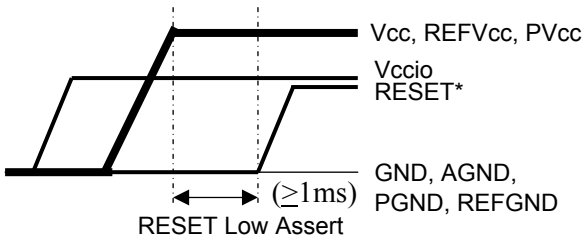
Figure B. Vertical Direction Back Porch Specification

8.3.6 Power on/off and display-on sequence timinng

Turn On the power of Vccio first, then Vcc, REFVcc and PVcc in that order, or all of the power supplies at once (simultaneously). When turning on the power, be sure to set the RESET* to the GND level.



Power Supply ON Sequence (1)

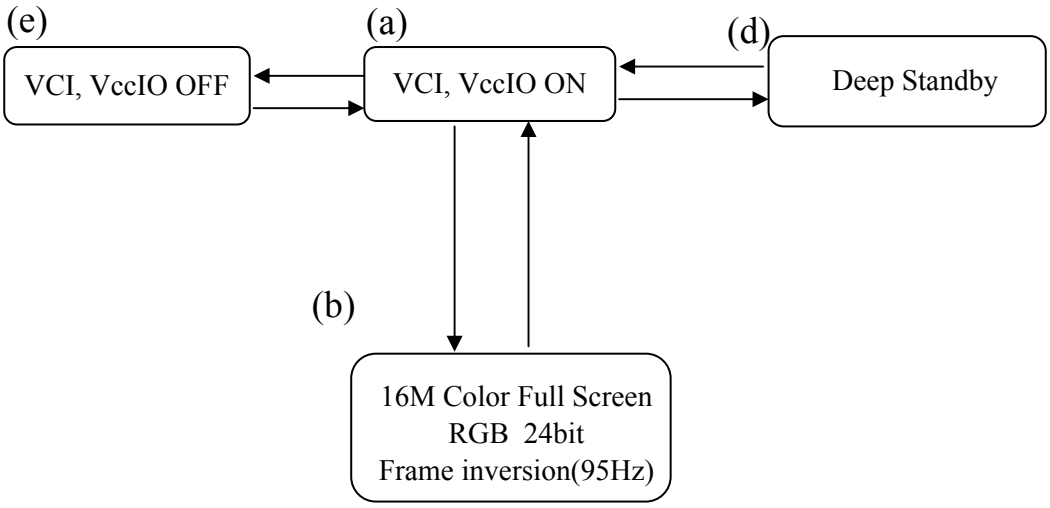


Power Supply On Sequence (2)

Please drop each voltage by the order opposite to and the relation when the power supply is on when you turn off the power supply.

8.4 REGISTER SETTING

(1) STATE TRANSITION DIAGRAM OF OPERATION MODE



(2) SEQUENCE

State (e) -> (a)

Previous data

1	Vcc, Vci, VccIO simultaneous on	Vcc, Vci, VccIO on	
2	Reset	RESET* = "L"	
3		wait	1 ms
4		RESET* = "H"	
5		wait	2 ms

State (a) -> (e)

Previous data

1	Vcc, Vci, VccIO simultaneous off	Vcc, Vci, VccIO off	

State (b) -> (a)

Previous data

1	Display control: D=10	R01h	0x2A		
2	wait 20 ms	wait	20 ms		
3	Display setting: GON=0, TE=1	R0Eh	0xB4	add	
4	Display control: DTE=0, D=00, CON=0	R01h	0x00		
5	wait 20 ms	wait	20 ms		
6				DDVDH=Hi-Z	
7				wait	100 ms
8	Power control: SAP=0	R40h	0x00		
9	Power control: AP=0, PON=0, COM=0	R41h	0x00		
10	wait 80 ms	wait	80 ms		
11	Display setting: GON=0, TE=1			R0Eh	0xB4
12	wait for transferring			wait	100 us

State (a) -> (d)

Previous data

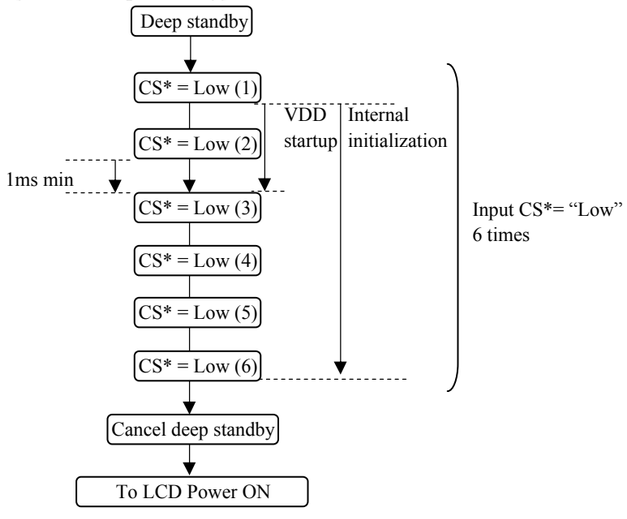
1	Deep standby	R40h	0x04

State (d) -> (a)

Previous data

1	DSTB mode cancellation (1)	R40h	0x00
2	wait 1 ms	wait	1 ms
3	DSTB mode cancellation (1)	R40h	0x00
4	DSTB mode cancellation (1)	R40h	0x00

[Cancel Deep Standby]



Take an interval of 1ms min. between the second and the third times of the CS* = Low.

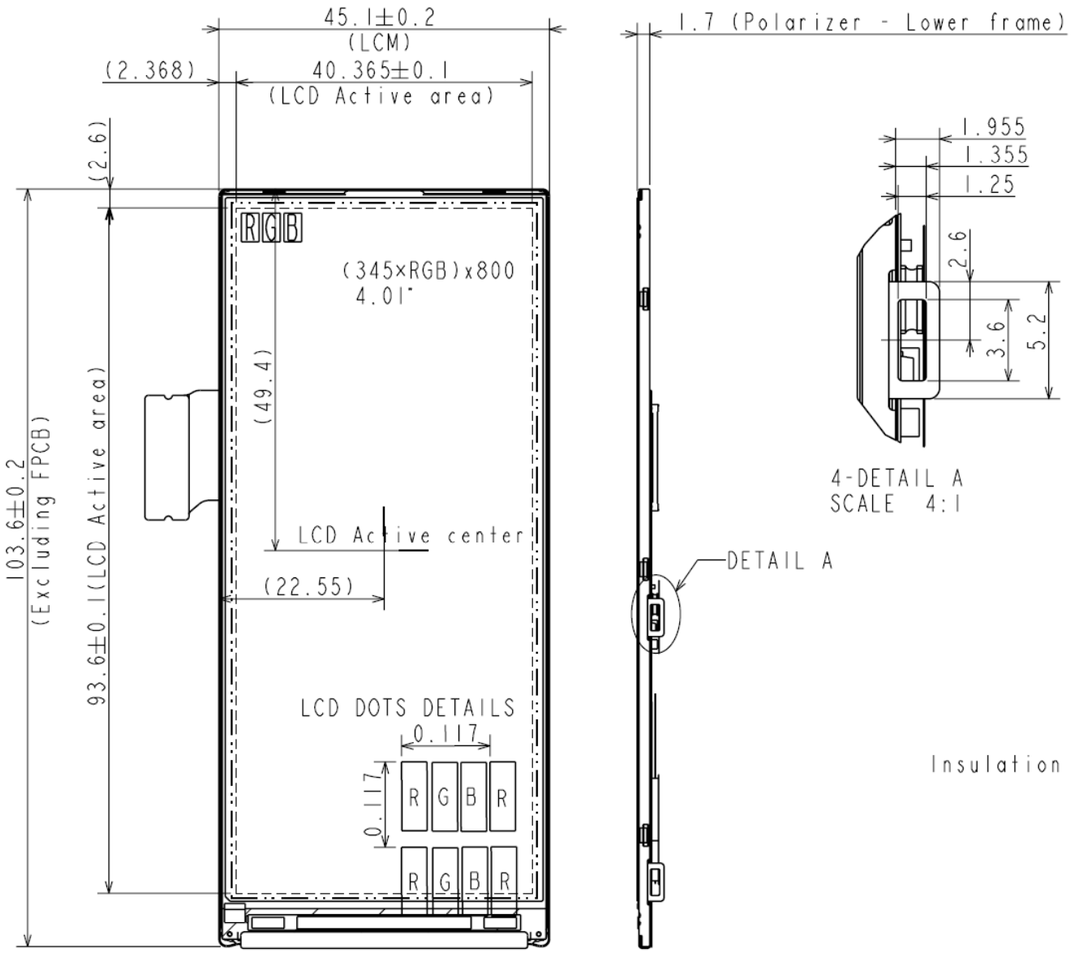
State (a) -> (b)

Previous data

1				R52h	0x95
2	Power setting: SAP=0	R40h	0x00		
3	Power setting: AP=0, PON=0, COM=0	R41h	0x00		
4	Display control: D=00, DTE=0	R01h	0x00		
5	GON=0, MS=1, SM=1, MNT=0, TE=1	R0Eh	0xB4		
6	wait for transferring	wait	100 us		
7	Power setting:	R42h	0x03		
8	Power setting: DC0=0, DC1=4	R43h	0x40		
9	Power setting: VCOMG=1, CHU=CLU=2	R44h	0xA7		0xA3
10	Power setting: VC=0, BT=6	R45h	0x60		0x00
11	Power setting: VRD=A, APR=1	R46h	0xA1		
12	Power setting:	R47h	0xA7		0xA9
13	Power setting: VDV=12	R49h	0x12		
14	Power setting:	R4Ah	0xA0		
15	Power setting:	R4Bh	0x58		0x54
16	Power setting:	R4Ch	0x25		
17	Power setting: RGVLT=1, RGPRO=1	R4Dh	0x15		0x45
18				R4Fh	0x21
19	Display setting: NL=1	R02h	0x11		
20	Display setting: EL=0, BC=0	R03h	0x00		
21	Display setting: HBP=B (16clk)	R04h	0x0B		
22	Display setting: VBP=8	R05h	0x08		
23	Display setting: DPL=HPL=VPL=EPL=0, ENE=0	R06h	0x00		
24	Display setting: SS=BGR=1, REV=0	R08h	0x03		
25	Display setting: SDTE=3	R09h	0x03		0x00
26	Display setting: EQWE=0, EQWE2=0	R0Ah	0x00		
27	Display setting: GNP=0	R0Ch	0x00		
28	Outline sharpening: EEE=0, COE=4	R10h	0x40		
29	Outline sharpening: EHSA=000	R11h	0x00		
30		R12h	0x00		
31	Outline sharpening: EHEA=13F	R13h	0x3F		
32		R14h	0x01		
33	Outline sharpening: EVSA=000	R15h	0x00		
34		R16h	0x00		
35	Outline sharpening: EVEA=31F	R17h	0x1F		
36		R18h	0x03		
37	Contrast: CNTR=80	R19h	0x80		
38	Contrast: CNTG=80	R1Ah	0x80		
39	Contrast: CNTB=80	R1Bh	0x80		
40	Bright: BRTR=40	R1Ch	0x40		
41	Bright: BRTG=40	R1Dh	0x40		
42	Bright: BRTB=40	R1Eh	0x40		
43	Analog: HYP=5, HIZ=3	R50h	0x53		
44	Analog: SPBS=1			R59h	0x01
45	Analog γ (1)	R60h	0x05		
46	Analog γ (2)	R61h	0x04		0x00
47	Analog γ (3)	R62h	0x12		0x24
48	Analog γ (4)	R63h	0x44		0x45
49	Analog γ (5)	R64h	0x51		0x41
50	Analog γ (6)	R65h	0x00		0x41
51	Analog γ (7)	R66h	0x05		0x01
52	Analog γ (8)	R67h	0x06		0x05
53	Analog γ (9)	R68h	0x00		
54	Analog γ (10)	R69h	0x50		
55	Analog γ (11)	R6Ah	0x01		
56	Analog γ (12)	R6Bh	0x14		
57	Analog γ (13)	R6Ch	0x14		
58	Analog γ (14)	R6Dh	0x54		
59	Analog γ (15)	R6Eh	0x42		
60	Analog γ (16)	R6Fh	0x02		0x00
61	Analog γ (17)	R70h	0x05		
62	Analog γ (18)	R71h	0x00		
63	Digital γ: GMRA=20	R80h	0x20		
64	Digital γ: GMRB=40	R81h	0x40		
65	Digital γ: GMRC=80	R82h	0x80		
66	Digital γ: GMRD=C0	R83h	0xC0		
67	Digital γ: GMGA=20	R84h	0x20		
68	Digital γ: GMGB=40	R85h	0x40		
69	Digital γ: GMGC=80	R86h	0x80		
70	Digital γ: GMGD=C0	R87h	0xC0		
71	Digital γ: GMBA=20	R88h	0x20		
72	Digital γ: GMBB=40	R89h	0x40		
73	Digital γ: GMBC=80	R8Ah	0x80		
74	Digital γ: GMBD=C0	R8Bh	0xC0		
75	Display setting: GON=1, TE=1	R0Eh	0xB5		
76	wait for transferring	wait	100 us		
77	Power setting: AP=2	R41h	0x02		
78	Power setting: SAP=1	R40h	0x10		
79	wait 20 ms	wait	20 ms		
80				DDVDH=5.8V ON	
81				wait	50 ms
82	Power setting: PON=1, COM=1	R41h	0x32		
83	wait 60 ms	wait	60 ms		
84				R41	0x72
85				wait	60 ms
86	Display control: D=01,BE=0	R01h	0x01		0x41
87	wait 20 ms	wait	20 ms		
88	Display control: D=11,CON=1,BE=0	R01h	0x23		0x63
89	wait 20 ms	wait	20 ms		
90	Display control: DTE=1	R01h	0x2B		0x6B

9. DIMENSIONAL OUTLINE

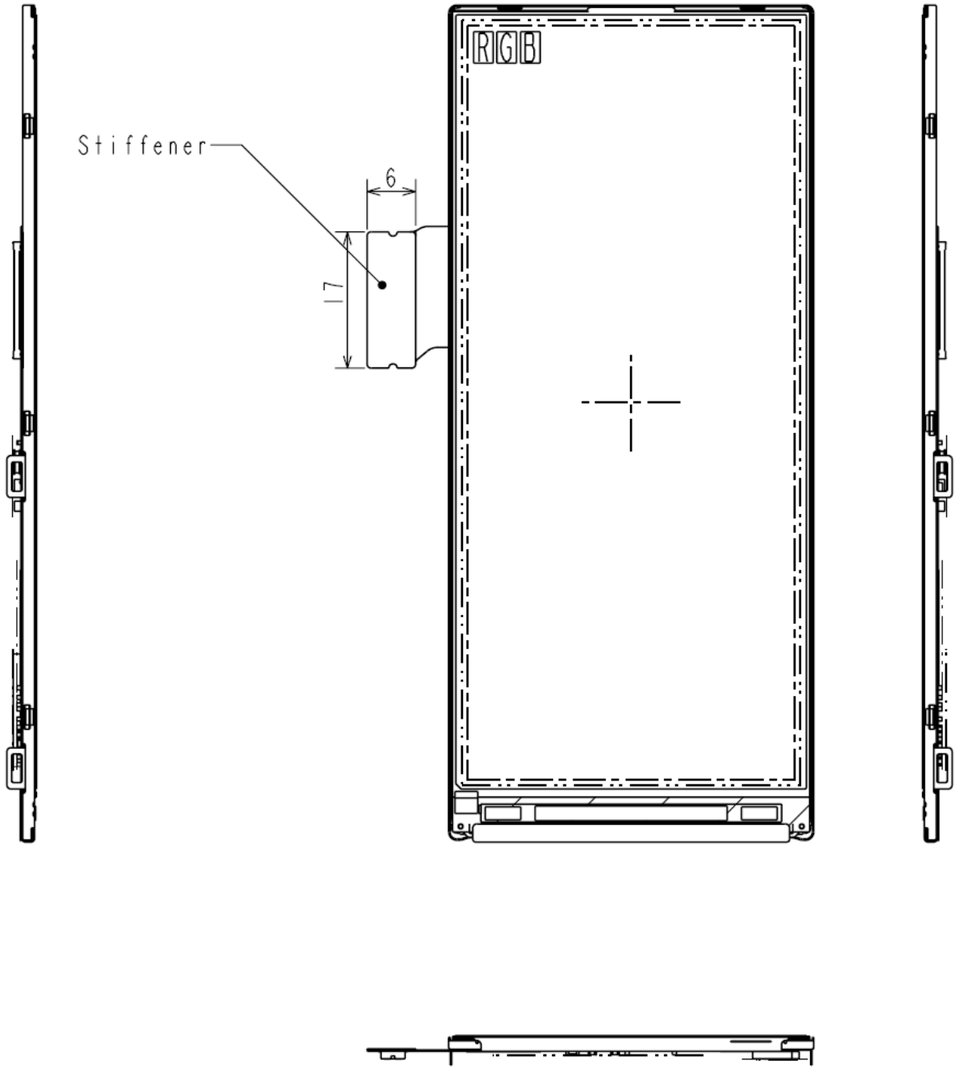
(1) TX10D04VM0AAA

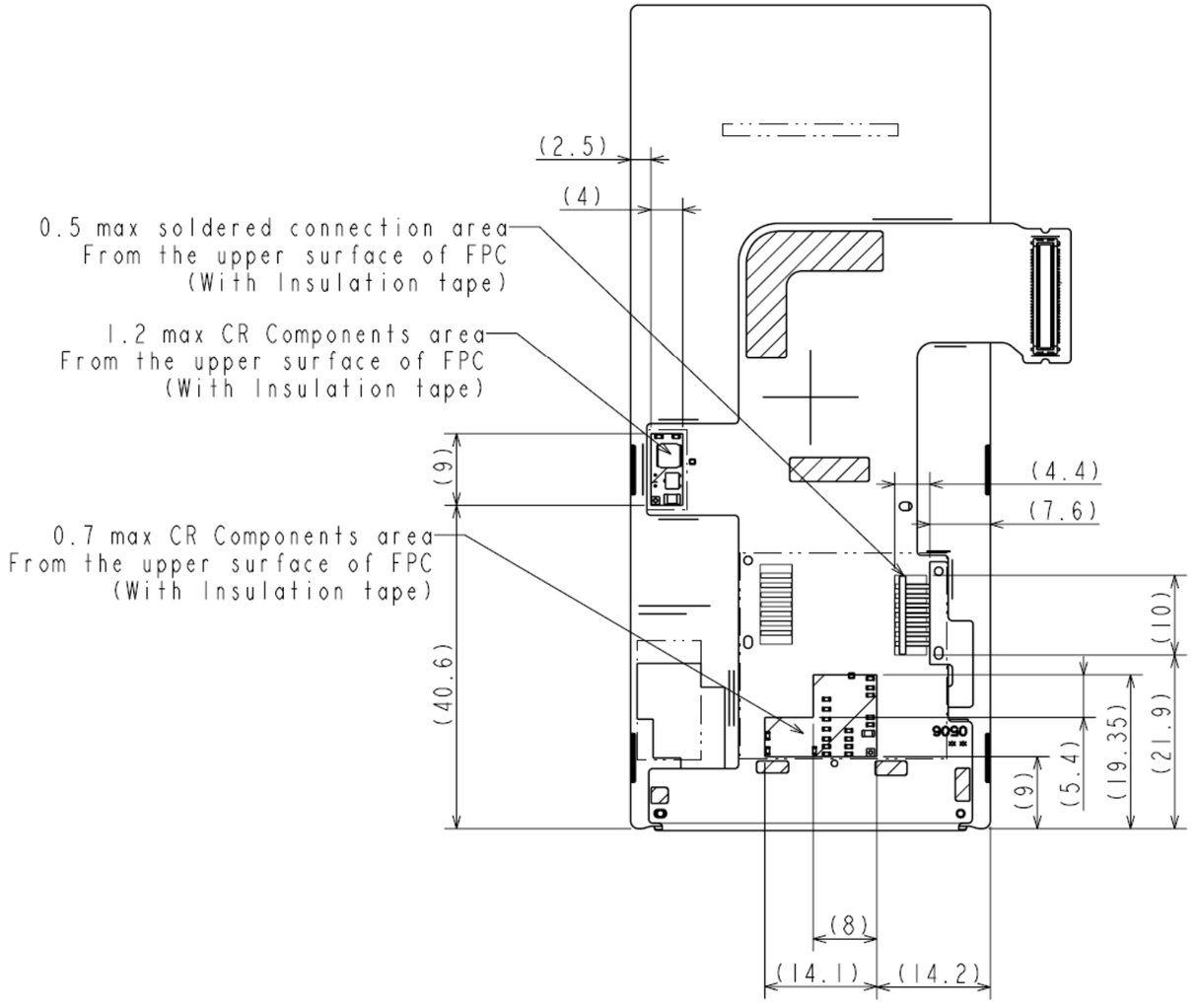


No.	SIGNAL
1	AN(LED)
2	CA1(LED)
3	CA3(LED)
4	CA5(LED)
5	Maker ID(GND Level)
6	IOVCC(1.8±0.1V)
7	OPEN
8	LED PWM
9	SCL
10	SDO
11	DOTCLK
12	HSYNC
13	ENABLE
14	RESET
15	DB0
16	DB2
17	DB4
18	DB6
19	DB8
20	DB10
21	DB12
22	DB14
23	DB16
24	DB18
25	DB20
26	DB22
27	GND
28	GND
29	GND
30	GND
31	GND
32	GND
33	GND
34	GND
35	DB23
36	DB21
37	DB19
38	DB17
39	DB15
40	DB13
41	DB11
42	DB9
43	DB7
44	DB5
45	DB3
46	DB1
47	GND
48	GND
49	VSYNC
50	GND
51	GND
52	SDI
53	CS
54	GND
55	DDVDH(2.8±0.1V)
56	VCC(2.8±0.1V)
57	CA6(LED)
58	CA4(LED)
59	CA2(LED)
60	AN(LED)

Note (1)The unspecified tolerance : ±0.3
(2)CN1 : Panasonic 60pin BtoB AXT560124
(3)Recommend Voltage : IOVCC=1.8±0.1V
VCC=2.8±0.1V , DDVDH=2.8±0.1V
(4)DDVDH must be configured so that it is at the same potential level as Vcc and connected to a separate power supply.
(5)Measurement of thickness is used by the micro meter.
(Mitsutoyo : MDC-25M or equivalent)

Scale : NTS Unit : mm





Scale : NTS Unit : mm
Note : The unspecified tolerance : ±0.3

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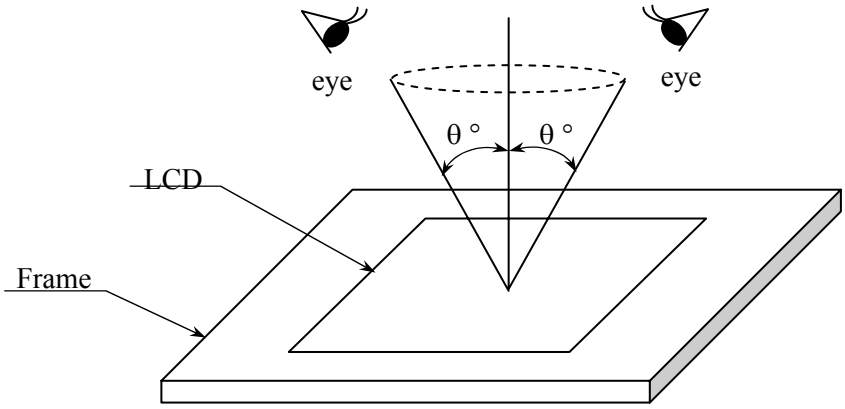
10. VISUAL INSPECTION

10.1 INSPECTION CONDITION

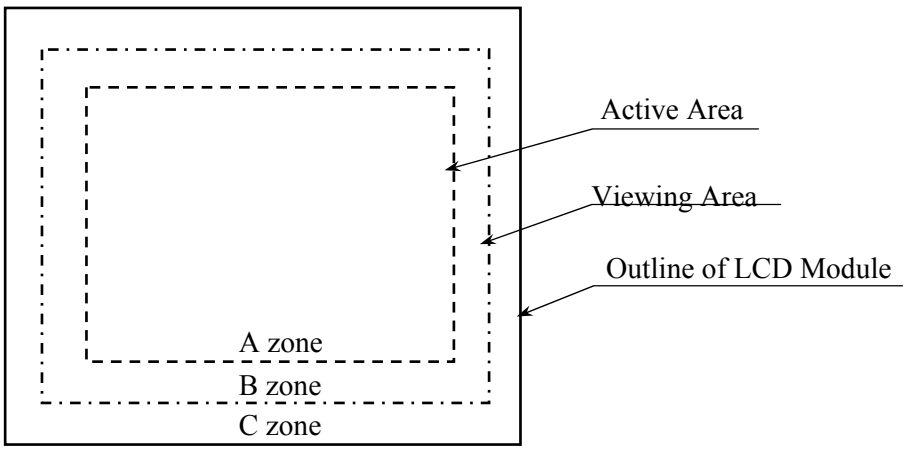
(1) Ambient illumination : 1000 lx
(2) Distance between inspector's eyes and LCD Modu : Approximately 30 cm
(3) Viewing angle θ : ≤ 30° for LCD Cosmetic Inspection
(4) Refer to the Measurement Conditions described in Item 6 for the conditions other than specified here.



10.2 DEFINITION OF ZONE

The LCD module is divided into four zones for visual inspections as follows.

A zone : Active Area (For dimensions, see Item 9, DIMENSIONAL OUTLINE)
B zone : Viewing Area but Active Area (For dimensions, see Item 9, DIMENSIONAL OUTLINE)
C zone : Whole LCD module except the Viewing Area (Including FPC and frame)



10.3 COSMETIC SPECIFICATION

No.	Item			Maximum Acceptable Number	Unit	Applied Zone	LCD Module	Back light	Note
1	Dot defect	Bright dot	Single	1	pcs	A	On		(1), (2), (3), (4), (6), (10), (11)
			Consecutive	0					
		Dark dot	Single	3					
			Consecutive	0					
		Total Number		3					
2	Line Defect			0	pcs	A	On		-
3	Displaying Quality (Uneven Brightness, Spot)			Serious one is not allowed.	-	A	On		(6)
4	Foreign Particles, Stain (Linear) [mm] W: Width L: Length	W≤0.02	L: Ignored	Ignored	pcs	A, B	On		(5), (6), (7), (8), (9)
		0.02<W ≤0.03	L≤3.0	5					
			3.0<L	0					
		0.03<W ≤0.05	L≤3.0	4					
			3.0<L	0					
		0.05<W	-	Refer to Item 5.					
5	Foreign Particles, Stain (Circular), Bubble [mm] D: Average Diam.	D≤0.25		Ignored	pcs	A, B	On		(5), (6), (7), (8), (9)
		0.25<D≤0.30		6					
		0.30<D		3					
6	Scratch (Linear) [mm] W: Width, L: Length	W≤0.1	L: Ignored	Ignored	pcs	A, B	On		(5), (6), (7), (8), (9)
		0.1<W	L≤7.0	4					
			7.0<L	0					
7	Scratch (Circular) ,Dig [mm] D: Average Diam.	D≤0.2		Ignored	pcs	A, B	On		(5), (6), (7), (8), (9)
		0.2<D≤0.4		4					
		0.4<D		0					
8	Foreign Particles, Stain (Linear) [mm] W: Width L: Length	W≤0.02	L: Ignored	Ignored	pcs	A, B	Off		(5), (6), (7), (8), (9),(12)
		0.02<W ≤0.03	L≤3.0	5					
			3.0<L	0					
		0.03<W ≤0.05	L≤3.0	4					
			3.0<L	0					
		0.05<W	-	Refer to Item 9.					
9	Foreign Particles, Stain (Circular), Bubble [mm] D: Average Diam.	D≤0.25		Ignored	pcs	A, B	Off		(5), (6), (7), (8), (9),(12)
		0.25<D≤0.40		5					
		0.40<D		3					
10	Scratch (Linear) [mm] W: Width, L: Length	W≤0.1	L: Ignored	Ignored	pcs	A, B	Off		(5), (6), (7), (8), (9)
		0.1<W	L≤7.0	4					
			7.0<L	0					
11	Scratch (Circular) ,Dig [mm] D: Average Diam.	D≤0.3		Ignored	pcs	A, B	Off		(5), (6), (7), (8), (9)
		0.3<D≤0.5		4					
		0.5<D		0					
12	Scratch, Dent in Frame			Serious one is not allowed	-	C	Off		(6)
13	Scratch on FPC				-	C	Off		(6)

Notes (1) A defect whose area is more than 50% of the dot is regarded as a Dot Defect.

(2) A dot whose brightness with an all black screen is more than 30% of the normal white dot level is regarded as a Bright Dot Defect.

(3) A dot whose brightness with an all white screen is less than 60% of the normal white dot level is defined as a Dark Dot Defect.

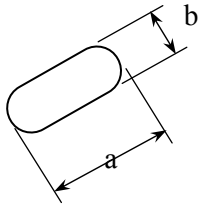
(4) Defective dots which are not adjacent are each considered as a single Dot Defect.

(5) Anything which can be easily wiped off the display surface is disregarded as a defect.

(6) In the event of a dispute, both parties should discuss items required for resolution, such as limit samples.

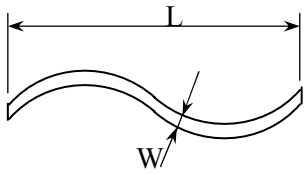
(7) Definitions for D, W and L are as follows.

Definition of D



$$D = \frac{a + b}{2} \text{ (mm)}$$

Definition of W and L



(8) The standard does not apply to any items found in C zone.

(9) Ignore anything unrecognized with the backlight on.

(10) When n defective dots are consecutive i.e. two or more defective dots are adjacent to each other, they are defined as an N consecutive Dot Defect.

(11) Refer to the standard No.5 (circular foreign particles) for the bright dot, caused by foreign particle, and which can be seen in changed colors from different viewing angles.

(12) Foreign Particles(Bright)

Specification : Refer to limited sample
Condition : LCD module -----Off
: Backlight ---------Off

11. PRECAUTIONS IN DESIGN

11.1 GENERAL ATTENTION

(1) The LCD module covered by this specification has been designed specifically for a mobile phone application. When used for other applications, we do not warrant any of the content of these specifications including quality and safety sections. Furthermore, this module has not been explicitly developed for medical equipment critically related to human life such as life support apparatus.

(2) Never attempt to disassemble this LCD module. There is a danger of burns, electric shock, and injury. If the module is disassembled, we do not warrant any of these specifications including quality and safety sections.

11.2 PRECAUTIONS AGAINST ELECTROSTATIC DISCHARGE

This module employs C-MOS LSI(s), which are sensitive and vulnerable to electrostatic discharge. Any operator should be grounded with suitable anti-ESD equipment such as a wrist band when handling the module. Avoid touching terminal pins directly.

11.3 HANDLING PRECAUTIONS

(1) Do not subject the LCD module to a humid environment for any extended period. If the ambient storage temperature is over 35°C, steps should be taken to avoid high humidity. The polarizer can deteriorate under high temperatures and high humidity. Additionally, this can also cause the polarizer to bubble and peel. Please store/operate the LCD module within the specified temperatures and humidity ranges.

(2) As polarizer material tends to be easily scratched, the LCD module must be handled with due care to avoid touching, pressure or rubbing by any material which is harder than 3H pencil lead (e.g. metal fixings, tweezers, glass, etc)

(3) No pressure more than 1.96 Pa must be applied to the LCD module surface. If pressure is exerted over an area of less than 1 cm2, the maximum pressure must not exceed 1.96 N.

(4) As adhesives containing organic materials are used for securing upper and lower polarizers, these can be deteriorated by chemical reaction with chemicals such as acetone, toluene, ethanol and isopropyl alcohol (IPA). The following solvent is recommended for use : Normal hexane. Please contact us if it is necessary to use chemicals other than these mentioned above.

(5) Lightly wipe the surface with a clean, soft material such as a cotton swab or cleaning cloth for glasses, dampened with the recommended chemical. Always wipe the surface horizontally or vertically. Never wipe using a circular motion and avoid excess pressure or scrubbing. To prevent the display surface from damage and to maintain in a good state, it is generally sufficient, to wipe the surface with a cotton swab.

(6) If spittle or a water drop comes in contact with the display area, immediately wipe it off. Liquids can damage the display surface resulting in deformation and faded color.

(7) Condensation on the LCD module may cause staining, dirtying or damage to the polarizer. If it is necessary to move the display from an area of lower ambient temperature to a higher one, it is required to let them normalize to the new ambient temperature before unpacking or use.

(8) Touching the display area or the terminal pins with bare hands or contaminating them should be avoided. In our experience, staining on the display area and poor insulation between terminals are often caused by being touched with bare hands. (Some cosmetics are detrimental to polarizers.)

(9) As the display is made of glass, it is possible to break under shock loads, especially the periphery can be easily cracked or chipped in handling. Please handle the module with care and prevent it from being dropped.

(10) Never bend nor scratch the interface part. These actions can cause poor electrical contact.

(11) Since the top and bottom areas of bent FPC tend to be easily damaged, be very careful not to push or hold in those areas.

(12) Be careful not to apply local stress to the back of the LCD module. This will potentially cause scratching to the backlight guide, or result in a non-uniformity issue. Pay extra attention to the interface connector portion at the time of connector insertion.

(13) Please insert the FPC into the connector first, keeping the FPC parallel to the connector's opening. Be sure to lock the connector before securing the module.

11.4 OPERATION PRECAUTION

(1) Noise spikes can cause a malfunction of the circuit. Recommended condition of spike noise level is: Vcc = ±200 mV (over and under shoot voltage).

(2) Response time depends on temperature (at a lower temperature, it becomes longer). Brightness and color are also temperature dependant.

(3) Be aware of the possibility of condensation under a sudden temperature change. Formation of dewdrops can cause damage to polarizer or electrical contacts and result inferior displaying or malfunction. And even after the condensation has dispersed, smears or spots may occur on the display surface.

(4) When a fixed pattern is displayed for a long period, afterimage is likely to occur.

(5) As the LCD module provides a high frequency circuit, sufficient countermeasures against electromagnetic noise, such as shielding, may be required.

(6) Do not connect nor disconnect the module to or from main system with power applied.

(7) Provide light shielding so that the driver is not exposed to light. Exposure to strong light may cause malfunction of the driver.

11.5 STORAGE

When storing the LCD modules as spare parts, the following precautions are necessary.

(1) Store the LCD modules in a dark place; do not expose them to sunlight or fluorescent light. Keep the temperature between 10 and 30°C, and the humidity between 55% and 75%RH.

(2) The polarizer surface should not come in contact with any other object. It is recommended that the LCD modules are stored in the container in which they were shipped.

11.6 SAFETY

This LCD module is a glass product. In case of damage, ensure operators wear a pair of protective gloves whilst handling it. Additionally, if any liquid (liquid crystal) accidentally comes into contact with skin, immediately wash it off with soap and water.

11.7 MECHANICAL DESIGN

The design of the mobile phone case for this LCD module should be well studied so that any shock will not be transferred to the LCD module. When the mobile phone is dropped and the case provides insufficient shock absorption, the LCD module may become damaged.

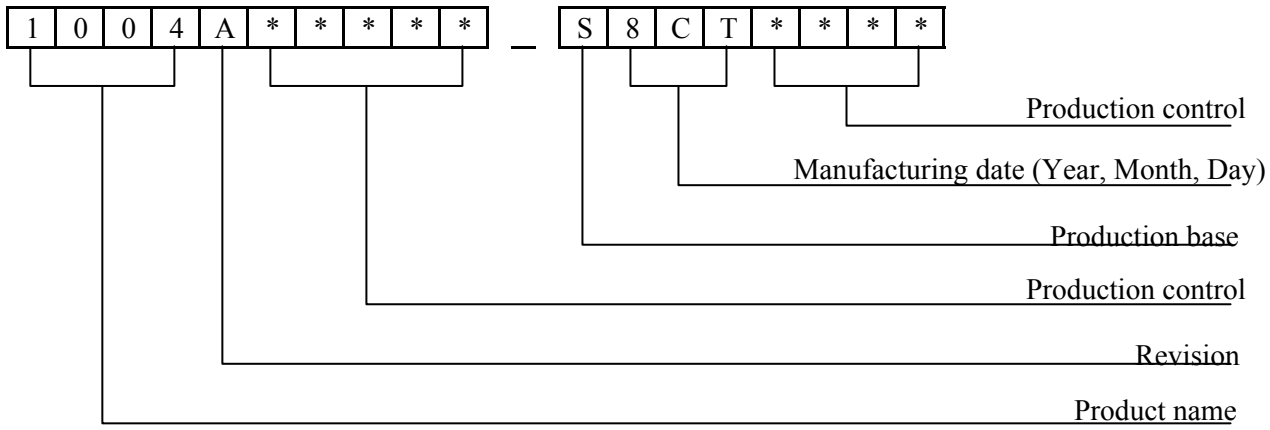
11.8 ENVIRONMENTAL PROTECTION

(1) Abide by national laws, legislation and local regulations when disposing of this LCD module.

(2) This LCD module complies with RoHS Directive.

12. DESIGNATION OF LOT MARK

Lot mark is printed on the back of the LCD module.



Revision	Description of change
A	

Year	Figure in lot mark
2008	8
2009	9
2010	0
2011	1

Month	Figure in lot mark	Month	Figure in lot mark
Jan.	1	July	7
Feb.	2	Aug.	8
Mar.	3	Sep.	9
Apr.	4	Oct.	A
May	5	Nov.	B
June	6	Dec.	C

Day	1	2	3	4	5	6	7	8	9
Figure in lot mark	1	2	3	4	5	6	7	8	9

Day	10	11	12	13	14	15	16	17	18	19
Figure in lot mark	A	B	C	D	E	F	G	H	J	K

Day	20	21	22	23	24	25	26	27	28	29
Figure in lot mark	L	M	N	P	Q	R	S	T	U	V

Day	30	31
Figure in lot mark	W	X

Production base	Figure in lot mark
Hitachi Displays	H
Hitachi Display Device (Suzhou)	S

Print example

1004A00000_S8CT0001

13. PRECAUTIONS FOR USE

(1) A limit sample shall be provided by both parties when both parties agree to its necessity. Judgment by limit sample shall take effect after the limit sample has been established and confirmed by both parties.

(2) Under the following situations, handling of the problem should be decided through immediate discussion and agreement between responsible people of both parties.

a) When a question arises concerning the specifications.

b) When a new item which is not mentioned in the specification occurs.

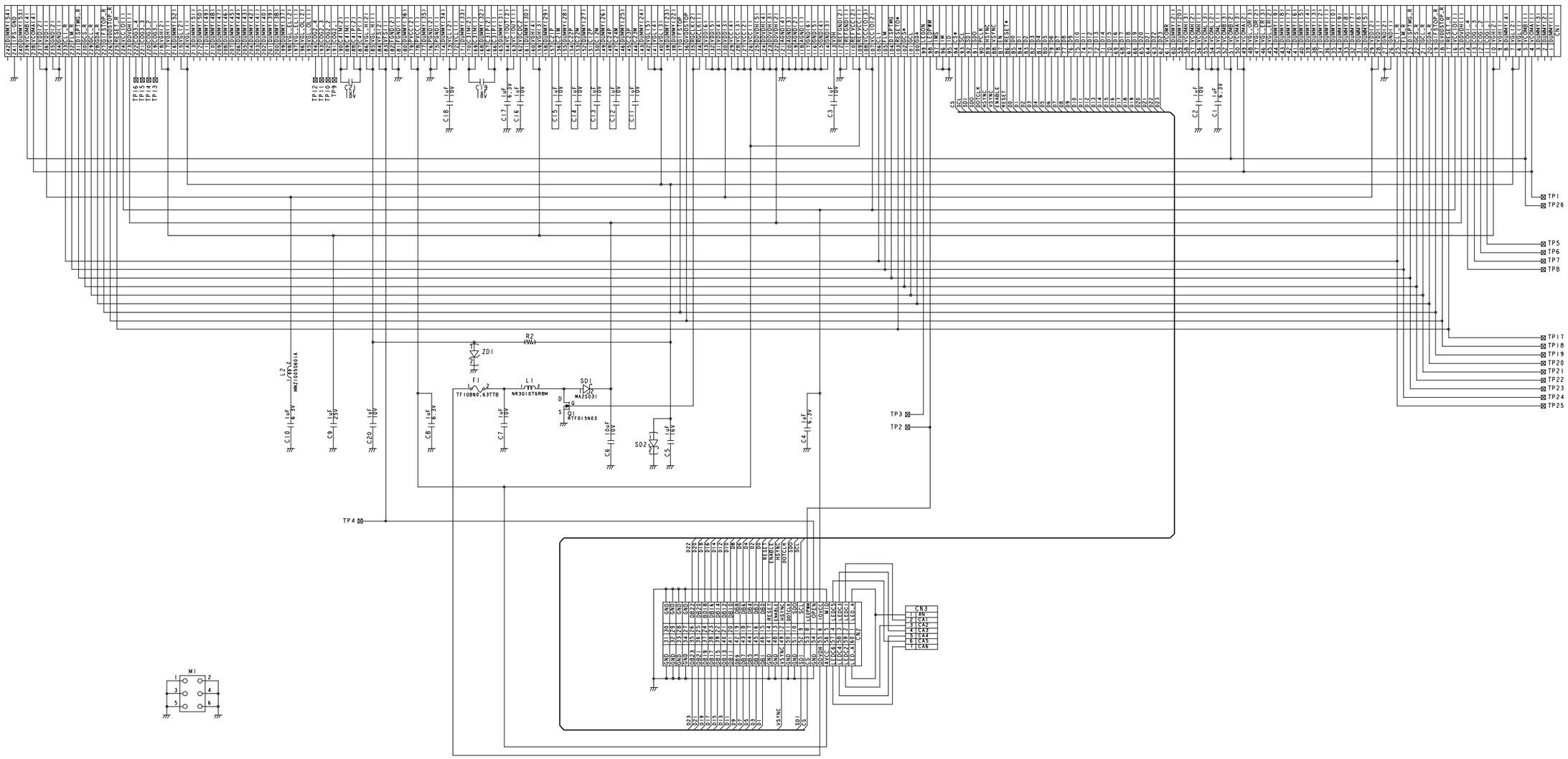
c) When the customer changes any item of inspection specification or operating condition and reports it to Hitachi, and an issue with the specification arises because of this change.

d) When a new issue is found with the customer's operating set for sample evaluation.

(3) All the specifications in this document become effective immediately after approval signatures of both parties are in place.

14. CIRCUIT DIAGRAM

14.1 FPC CIRCUIT DIAGRAM



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