KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

TENTATIVE

FOR MESSRS : _____ DATE : Jul. 8th,2016

TECHNICAL DATA

TX11D200VM1AAA

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ACCEPTED BY:_____ PROPOSED BY: Oblack Tsai

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 4.4” VGA of 4:3 format of LTPS(Lower temperature Poly-Silicon) TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially .This display is RoHS compliant , and LED backlight are applied on this display.

Part Name	TX11D200VM1AAA
Module Dimensions	96.82(W) mm x 78.7(H) mm x 4.385 max. (D) mm (include 4 pillars)
LCD Active Area	89.664(W) mm x 67.248(H) mm
Pixel Pitch	0.140(W) mm x 0.140(H) mm
Resolution	640 x 3(RGB)(W) x 480(H) Dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Reflective color TFT; Normal Black
Display Type	Active Matrix
Number of Colors	8 Colors(1-bit)
Backlight	Light Emitting Diode (LED)
Weight	52g
Interface	SPI ; 10 pins
Power Supply Voltage	3.3V for LCD; 9.0V for Backlight
Power Consumption	(TBD) W for LCD ;(TBD)W for backlight
Viewing Direction	6 O’clock
Feature	MIP(Memory in pixel) Reflective type LCD

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	(TBD)	V	-
Input Voltage of Logic	V_I	V_{SS}-0.3	V_{DD}+0.3	V	-
Operating Temperature	T_{op}	-20	70	˚C	Note 1
Storage Temperature	T_{st}	-30	80	˚C	Note 1
Backlight Input Voltage	V_{BL+}	8.4	9.6	V	-

Note 1: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Optical performances and response time would be different in temperatures other than 25˚C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\ ^{\circ}C,\ V_{SS} = 0V$

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	Analog	V_{DDA}	2.7	3.0	3.3	V	-
		V_{SSA}	-	0	-		-
	Logic	V_{DD}	2.7	3.0	3.3		Note 1
		V_{SS}	-	0	-		Note 2
Input Signal Voltage	Hi	V_{IH}	V_{DD}-0.1	V_{DD}	V_{DD}		Note 3
	Low	V_{IL}	V_{SS}	V_{SS}	V_{SS}+0.1		

Note 1: Apply to EXTMODE = ”H”.

Note 2: Apply to EXTMODE = “L”.

Note 3: Apply to SCLK, SI, SCS, DISP, EXTCOMIN.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	-	8.4	9	9.6	V	Note1
LED Forward Current	I_{LED}	-		17.5	25	mA	Note 2
LED lifetime	-	I_{LED}=17.5 mA	-	50K	-	hrs	-

Note 1: As Fig. 5.1 shown LED current is constant, V_{LED} and I_{LED} is many to one relationship, the above V_{LED} range is defined to obtain 17.5 mA.

Note 2: Estimated lifetime is specified as the time to reduce 50% brightness by applying 17.5 mA at 25°C.

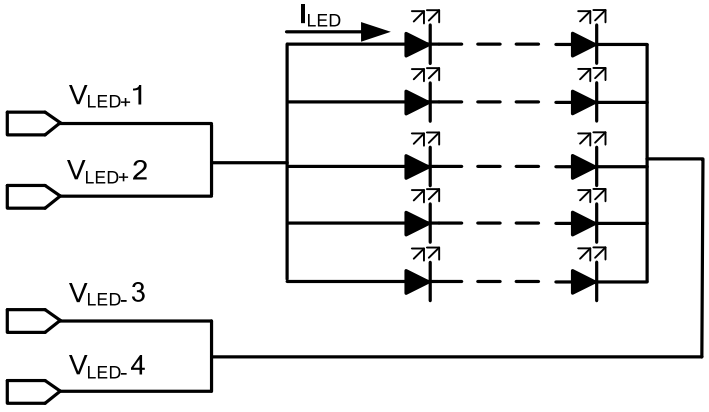


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 20 minutes.
- The ambient temperature is $25 \pm 5^{\circ}C$.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1 and Fig 6.3.

For transmission mode

$T_a = 25\ ^{\circ}C$, $V_{DD} = 3.0V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White	-	I_{LED}=17.5 mA	-	10	-	cd/m^2	Note 1
Brightness Uniformity	-	-	70	-	-	%	Note 2
Contrast Ratio	CR	-	-	10	-	-	Note 3

For reflection mode

$T_a = 25\ ^{\circ}C$, $V_{DD} = 3.0V$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness Reflection Ratio		-	-	-	34	-	%	-
Contrast Ratio		CR	-	-	13	-	-	Note 3
Response Time		Tr + Tf	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	(TBD)	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	11	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}, CR \geq 2$	-	75	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}, CR \geq 2$	-	80	-		
		θ y	$\phi = 90^{\circ}, CR \geq 2$	-	70	-		
		θ y′	$\phi = 270^{\circ}, CR \geq 2$	-	80	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	0.59	-	-	Note 6
		Y		-	0.35	-		
	Green	X		-	0.43	-		
		Y		-	0.47	-		
	Blue	X		-	0.30	-		
		Y		-	0.36	-		
	White	X		-	0.48	-		
		Y		-	0.41	-		

Note 1: The brightness and reflective ratio is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Max. Brightness} - \text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

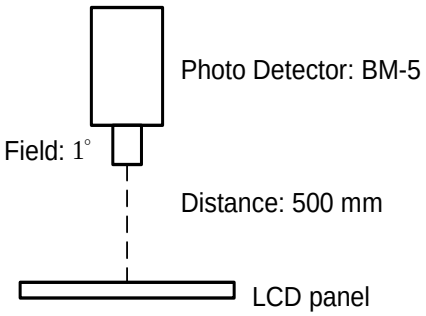


Fig 6.1

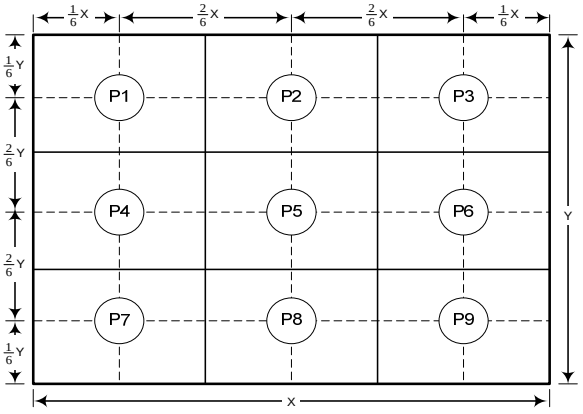


Fig 6.2

Note 3: The contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.4. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.

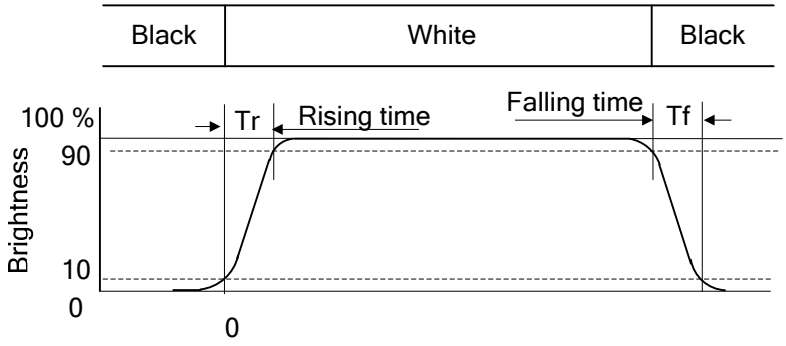


Fig 6.4

Note 5: The definition of viewing angle is shown in Fig. 6.5. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version; 85° viewing angle can be obtained from each viewing direction.

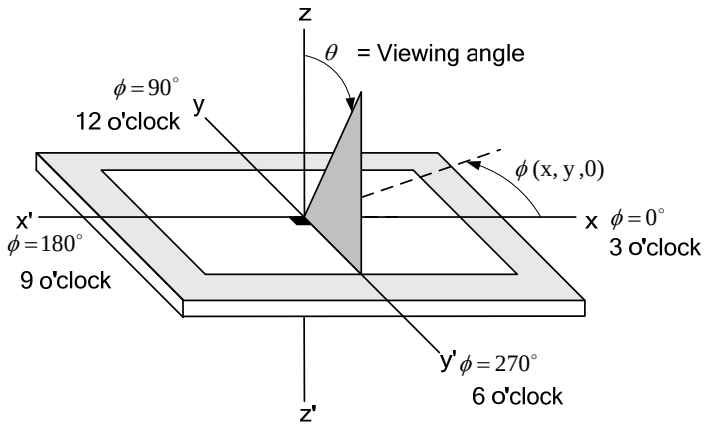
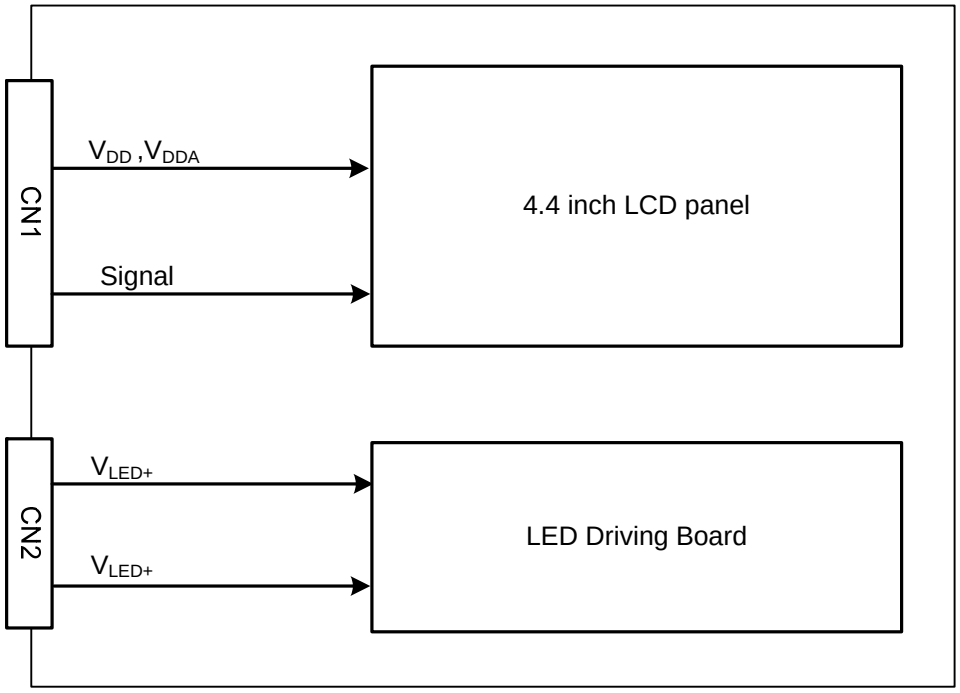


Fig 6.5

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note 1: Signals are SCLK, SI, SCS, EXTCOMIN, DISP and EXTMODE.

8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

CN1 pin assignment of LCD interface is as below:

Pin No.	Symbol	Function	Remark
1	SCLK	Serial Clock Signal	
2	SI	Serial Data Input Signal	
3	SCS	Chip Select Signal	
4	EXTCOMIN	COM Inversion Signal Input	
5	DISP	Display ON/OFF Control	Note 1
6	V_{DDA}	Power Supply for Analog	
7	V_{DD}	Power Supply for Logic	
8	EXTMODE	COM Inversion Mode Select Terminal	Note 2
9	V_{SS}	Logic Ground	
10	V_{SSA}	Analog Ground	

Note 1: The DISP signal is only for display. Pixel memory would not be changed.

"H": Pixel memory will be displayed.

"L": Black pattern will be displayed and pixel memory will be saved.

Note 2: "H": Enable EXTCOMIN signal, connect to V_{DD}.

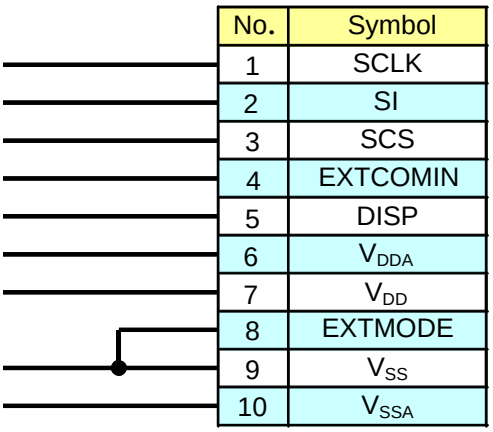
"L": Enable serial input flag, connect to V_{SS}.

CN2 pin assignment of Backlight is as below:

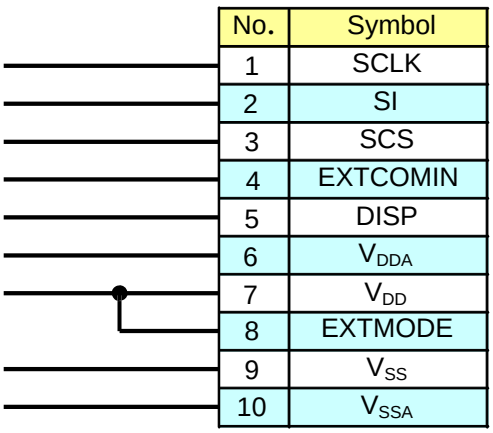
Pin No.	Signal	Level	Function
1	V_{LED}+	-	Power Supply for LED
2	V_{LED}+	-	Power Supply for LED
3	V_{LED}-	-	GND
4	V_{LED}-	-	GND

8.2 RECOMMENDED CIRCUIT

EXTMODE=L : COM Signal Serial Input



EXTMODE=H : COM Signal External Input



8.3 TIMING CHART

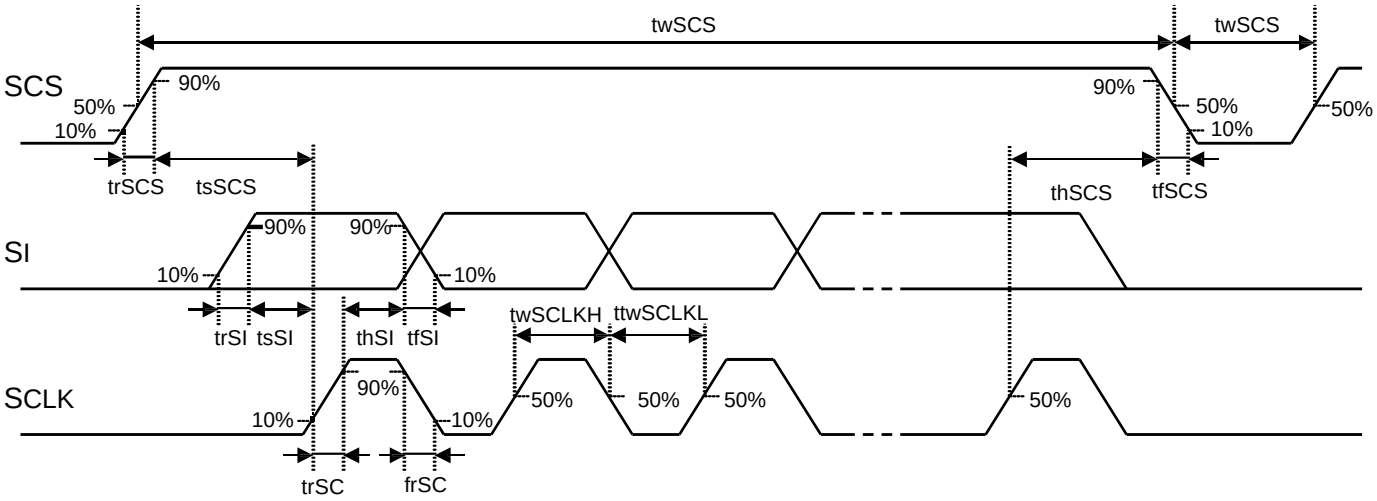


Fig. 8.1 SPI Timing

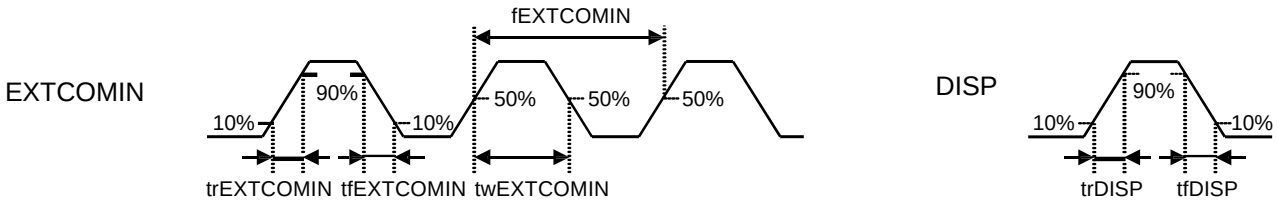


Fig. 8.2 COM Inversion and DISP Timing

8.4 TIMING TABLE

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Frame frequency	fV	1	-	12.15	Hz	All lines data update
Clock frequency	fSCLK	-	1.00	2.0	MHz	
Vertical cycle	tV	464.66	-	1000	ms e c	
COM frequency	fCOM	0.5	-	60.0	Hz	
SCS rising time	trSCS	-	-	50	nsec	
SCS falling time	tfSCS	-	-	50	nsec	
SCS High width	twSCSH	464.66	-	-	µsec	Data update mode
		15.8	-	-	µsec	No update mode
SCS Low width	twSCSL	6.0	-	-	µsec	
SCS settling time	ts SCS	6.0	-	-	µsec	
SCS holding time	thSCS	2.0	-	-	µsec	
SI rising time	trSI	-	-	50	nsec	
SI falling time	tfSI	-	-	50	nsec	
SI settling time	ts SI	200	450	-	nsec	
SI holding time	thSI	250	500	-	nsec	
SCLK rising time	trSCLK	-	-	50	nsec	
SCLK falling time	tfSCLK	-	-	50	nsec	
SCLK High width	twSCLKH	250	500	-	nsec	Note 1
SCLK Low width	twSCLKL	250	500	-	nsec	Note 1
EXTCOMIN frequency	fEXTCOMIN	1	-	120	Hz	Note 2
EXTCOMIN rising time	trEXTCOMIN	-	-	50	nsec	
EXTCOMIN falling time	tfEXTCOMIN	-	-	50	nsec	
EXTCOMIN High width	twEXTCOMIN	2.0	-	-	µsec	
DISP rising time	trDISP	-	-	50	nsec	
DISP falling time	tfDISP	-	-	50	nsec	

Note 1: twSCLKH and twSCLKL should be approximately the same length, if possible.

Note 2: EXTCOMIN frequency should be made lower than frame frequency.

Note 3: Depends on number of vertical-lines and horizontal-lines.

8.5 MODE

8.5.1 Mode Select

M0	M1	M2	M3	M4	M5	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0	Mode
L	L/H	L	L	-	-											No Update
L	L/H	L	H	L/H	L/H											Blinking
L	L/H	H	L/H	L/H	L/H											All Clear
H	L/H	L	L/H	L/H	-	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0	Data Update
H	L/H	H	L/H	L/H	L/H											No Update
Mode (6bit)						Gate Line Address (10bit)										-

Function table

M0=L or M0=H/M2=H

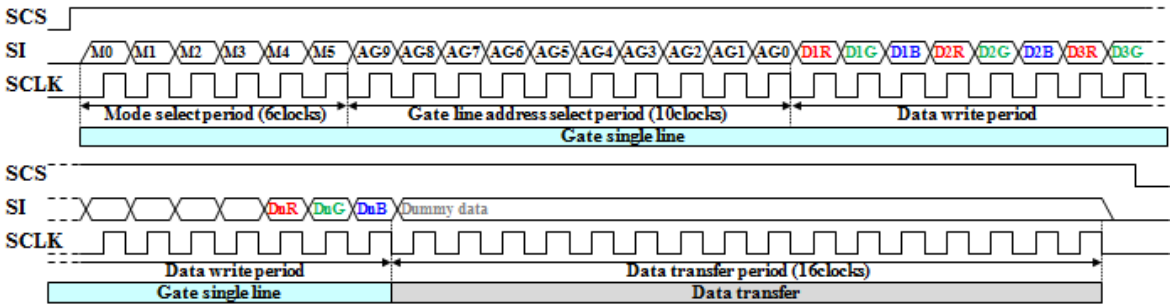
Mode	M3	M4	M5
B linking OFF	L	-	-
B linking Black	H	L	L
B linking White	H	H	L
B linking Inversion	H	-	H

M0=H/M2=L

Mode	M3	M4	M5
3Bit Data Input	L	L	-
1Bit Data Input	L	H	-
4Bit Data Input	H	-	-

Note 1: Unassigned bit and AG9-8 : No care, it can be H or L (L is Recommended).

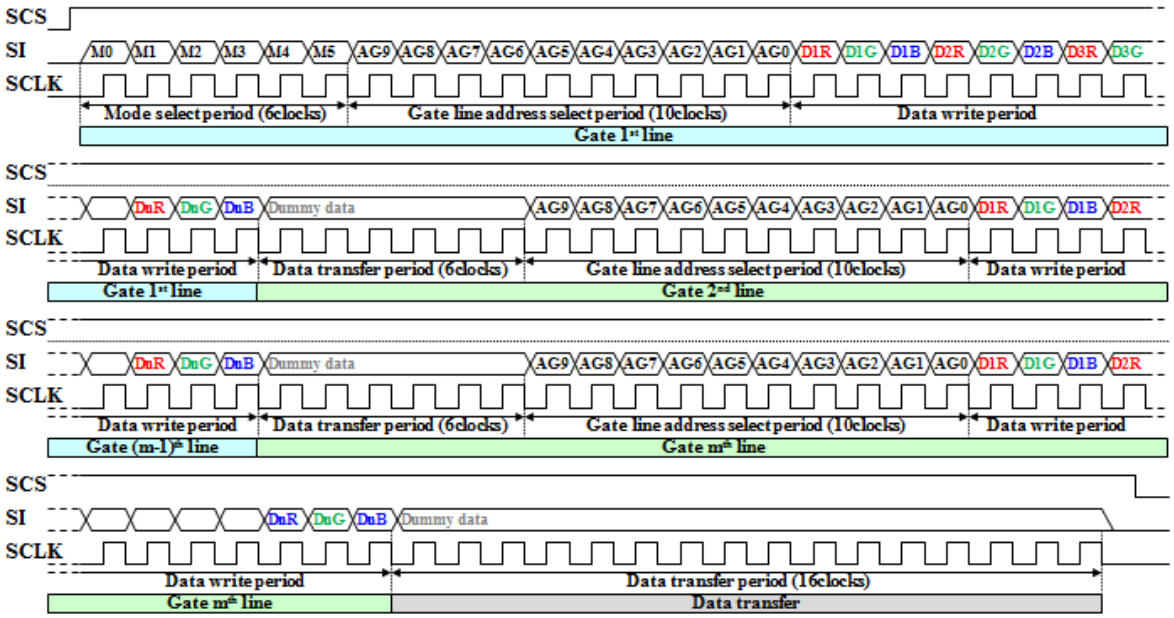
8.5.2 Single line update mode (to update data for only one specified line data)



Bit	Level	Description	Remark
M0	H	Data update mode	Mode flag
M1	H	When EXTMODE="L", output COM="H".	COM inversion flag
	L	When EXTMODE="L", output COM="L".	
	L/H	Invalid data when EXTMODE="H".	
M2	L	Data update mode	All clear flag
M3	L	Setting must be "L".	Data-bit control flag
M4	L		
M5	L/H	Invalid data	Don't care
AG9-AG0	-	Refer to the Gate line address table	Gate line address (10bit)
Data write	-	n =640 (Number of horizontal line) Input serially the pixel data in the order of Red-Green-Blue	Pixel memory data
Data transfer	L/H	Need transfer period which is 16clocks after the last data.	Dummy data

M0, M2 flags are cleared by SCS="L", and M3, M4 flags are cleared by DISP="L".

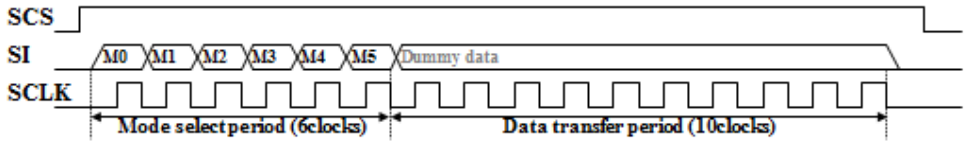
8.5.3 Multiple lines update mode (to update arbitrary multiple lines data)



Bit	Level	Description	Remark
M0	H	Data update mode	Mode flag
M1	H	When EXTMODE="L", output COM="H".	COM inversion flag
	L	When EXTMODE="L", output COM="L".	
	L/H	Invalid data when EXTMODE="H",	
M2	L	Data update mode	All clear flag
M3	L	Setting must be "L".	Data-bit control flag
M4	L		
M5	L/H	Invalid data	Don't care
AG9-AG0	-	Refer to the Gate line address table	Gate line address (10bit)
Data write	-	n =640 (Number of horizontal line) m=480 (Number of vertical line) Input serially the pixel data in the order of Red-Green-Blue	Pixel memory data
Data transfer	L/H	Need transfer period which is 6clocks between the gate line and the next gate line and 16clocks after the last data	Dummy data

M0, M2 flags are cleared by SCS="L", and M3, M4 flags are cleared by DISP="L".

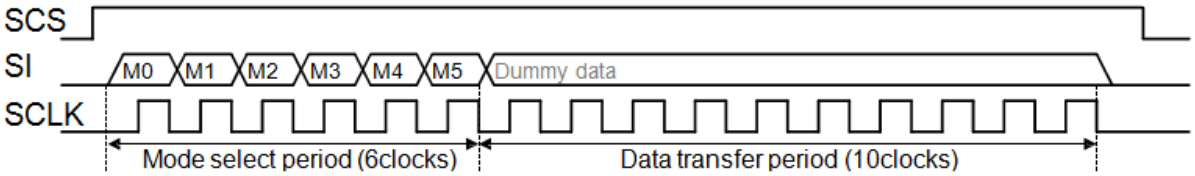
8.5.4 No-update mode (to maintain the current memory data)



Bit	Level	Description	Remark
M0	L/H	Set “L” or “H” to both M0 and M2	Mode flag
M1	H	When EXTMODE=“L”, outputs COM=“H”.	COM inversion flag
	L	When EXTMODE=“L”, outputs COM=“L”.	
	L/H	Invalid data when EXTMODE=“H”,	
M2	L/H	Set “L” or “H” to both M0 and M2.	All clear flag
M3	L	No-update mode and blinking mode is terminated	Blinking flag
	H	Blinking mode. Refer to the 8.5.6 for details.	
M4	L/H	Invalid data	-
M5			
Data transfer	L/H	Need transfer period which is 10clocks	Dummy data

M0, M2 flags are cleared by SCS=“L”, and M3 flag is cleared by DISP=“L”.

8.5.5 All clear mode (to clear memory data and write black pattern as initial)

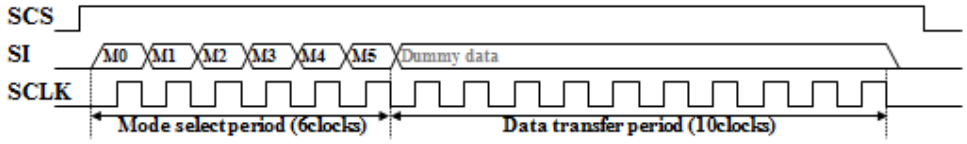


Bit	Level	Description	Remark
M0	L	No-update mode	Mode flag
M1	H	When EXTMODE=“L”, outputs COM=“H”	COM inversion flag
	L	When EXTMODE=“L”, outputs COM=“L”	
	L/H	Invalidate when EXTMODE=“H”,	
M2	H	all clear mode	All clear flag
M3	L	Blinking mode is terminated.	Blinking flag
	H	Blinking mode. Refer to the 8.5.6 for details.	
M4	L/H	Valid data when M3=“H” Invalid data when M3=“L”	Blinking mode flag
M5			
Data transfer	L/H	Need transfer period which is 10clocks	Dummy data

M0, M2 flags are cleared by SCS=“L”, and M3, M4 flags are cleared by DISP=“L”.

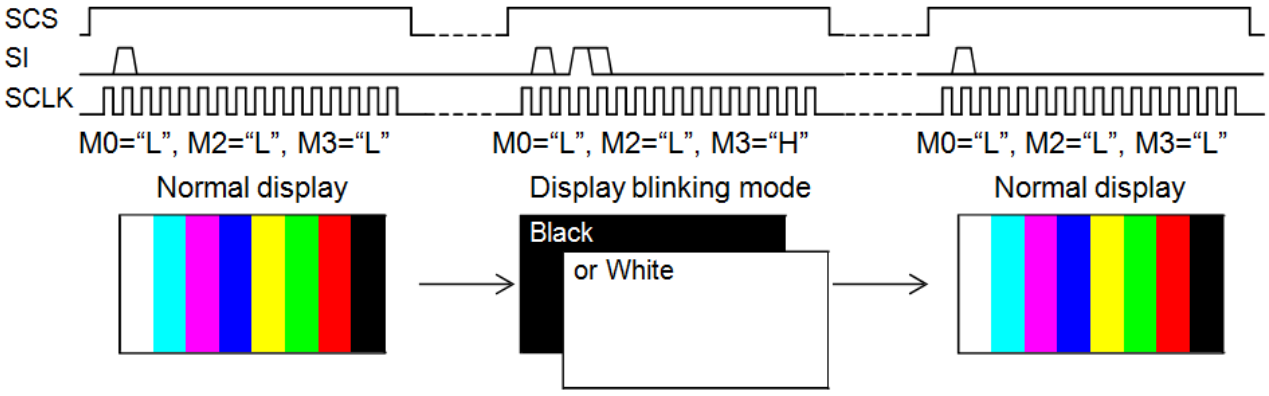
Display gives priority to blinking flag (M3).

8.5.6 Blinking mode (to display black or white pattern without updating memory data)



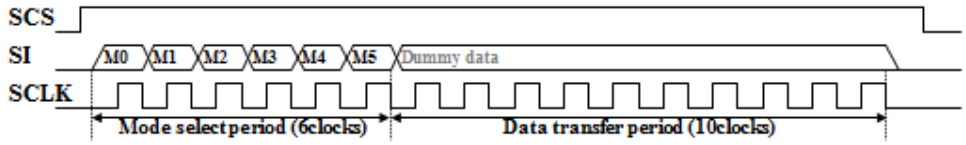
Bit	Level	Description	Remark
M0	L	No-update mode	Mode flag.
M1	H	When EXTMODE="L", outputs COM="H".	COM inversion flag.
	L	When EXTMODE="L", outputs COM="L".	
	L/H	Invalidate when EXTMODE="H",	
M2	L	No-update mode	All clear flag
	H	All clear mode,refer to the 8.5.5	
M3	L	No-update mode and blinking mode is terminated	Blinking flag
	H	Blinking mode and display blinking color	
M4	L	Blinking color is black	Blinking color flag
	H	Blinking color is white	
M5	L	Blinking color mode.	Blinking inversion flag
Data transfer	L/H	Need transfer period which is 10clocks	Dummy data

M0, M2 flags are cleared by SCS="L", and M3-M5 flags are cleared by DISP="L".



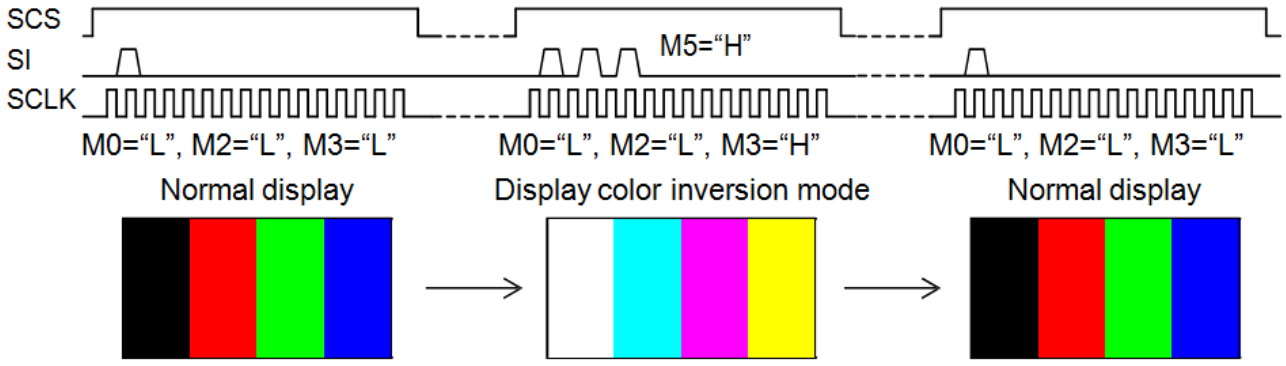
Blink display to alternate between normal display and display blinking mode.

8.5.7 Display color inversion mode (to display inversed pattern without updating memory data)



Bit	Level	Description	Remark
M0	L	No-update mode	Mode flag
M1	H	When EXTMODE="L", outputs COM="H".	COM inversion flag
	L	When EXTMODE="L", outputs COM="L".	
	L/H	Invalidate when EXTMODE="H",	
M2	L	No-update mode	All clear flag
	H	All clear mode,refer to the 8.5.5	
M3	L	No-update mode and blinking mode is terminated	Blinking flag
	H	Blinking mode and display color inversion	
M4	L/H	Invalidate when M5="H"	Blinking color flag
		refer to the 8.5.6 when M5="L"	
M5	H	Color inverted	Color inversion flag
Data transfer	L/H	Need transfer period which is 10clocks	Dummy data

M0, M2 flags are cleared by SCS="L", and M3,M5 flags are cleared by DISP="L".

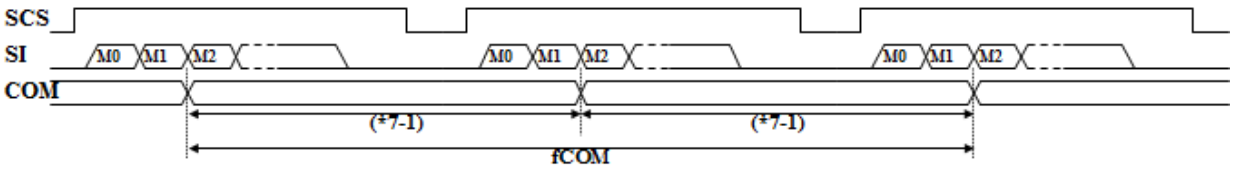


Blink display to alternate between normal display and display blinking mode.

8.6 COM INVERSION

There are two types of inputs.

8.6.1. COM polarity serial input / EXTMODE="L"



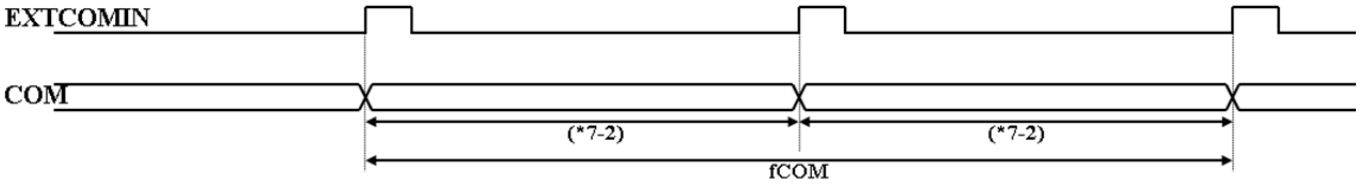
M1 : COM inversion flag. In case of "H", outputs COM="H". In case of "L", outputs COM="L".

COM polarity inversion has been changed by M1 flag statement.

Note 1: The periods of positive and negative polarity should be same length as much as possible.

8.6.2 EXTCOMIN signal / EXTMODE="H"

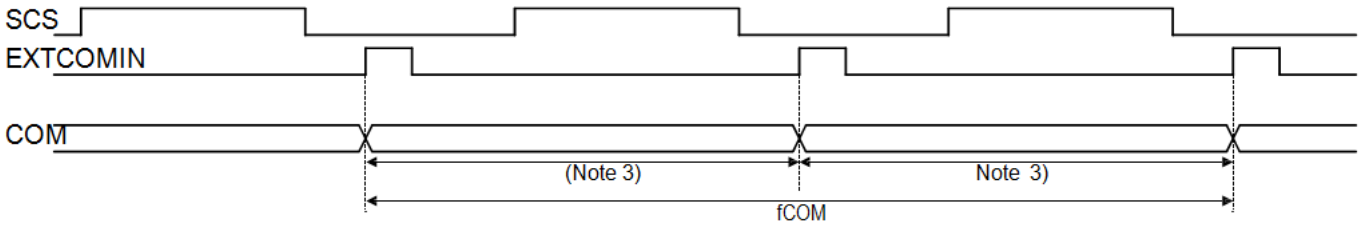
In case of EXTCOMIN input when the SCS signal is "H"



Note 1: COM polarity inversion has been changed by the falling timing of SCS. COM polarity (positive or negative) is controlled by internal circuit.

Note 2: The periods of positive and negative polarity should be same length as much as possible.

In case of EXTCOMIN input when the SCS signal is "L"

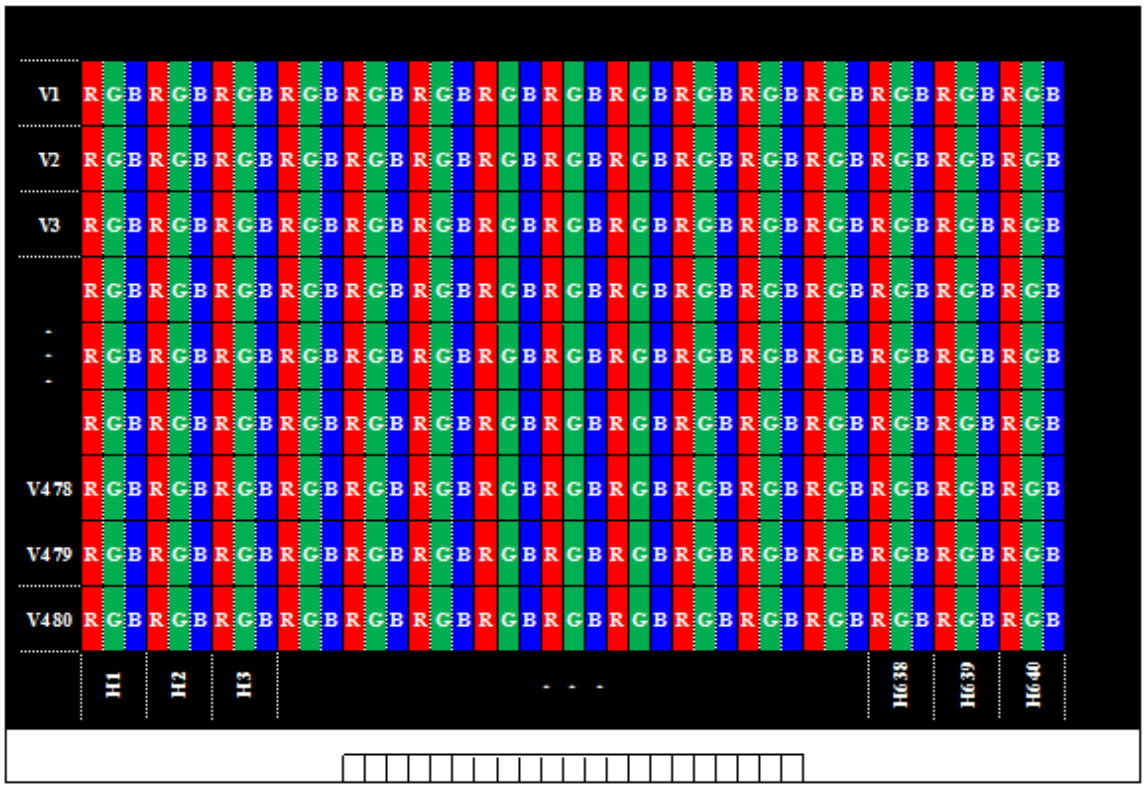


COM polarity inversion has been changed by the rising timing of EXTCOMIN.

COM polarity (positive or negative) is controlled by internal circuit.

Note 3: The periods of positive and negative polarity should be same length as much as possible

8.7 PIXEL MEMORY ADDRESS MAP



LCD Top View

8.8 GATE LINE ADDRESS TABLE

V	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	1	1	1
8	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	1	0	0	1
10	0	0	0	0	0	0	1	0	1	0
11	0	0	0	0	0	0	1	0	1	1
12	0	0	0	0	0	0	1	1	0	0
13	0	0	0	0	0	0	1	1	0	1
14	0	0	0	0	0	0	1	1	1	0
15	0	0	0	0	0	0	1	1	1	1
16	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	1	0	0	0	1
18	0	0	0	0	0	1	0	0	1	0
19	0	0	0	0	0	1	0	0	1	1
20	0	0	0	0	0	1	0	1	0	0
21	0	0	0	0	0	1	0	1	0	1
22	0	0	0	0	0	1	0	1	1	0
23	0	0	0	0	0	1	0	1	1	1
24	0	0	0	0	0	1	1	0	0	0
25	0	0	0	0	0	1	1	0	0	1
26	0	0	0	0	0	1	1	0	1	0
27	0	0	0	0	0	1	1	0	1	1
28	0	0	0	0	0	1	1	1	0	0
29	0	0	0	0	0	1	1	1	0	1
30	0	0	0	0	0	1	1	1	1	0
31	0	0	0	0	0	1	1	1	1	1
32	0	0	0	0	1	0	0	0	0	0
33	0	0	0	0	1	0	0	0	0	1
34	0	0	0	0	1	0	0	0	1	0
35	0	0	0	0	1	0	0	0	1	1
36	0	0	0	0	1	0	0	1	0	0
37	0	0	0	0	1	0	0	1	0	1
38	0	0	0	0	1	0	0	1	1	0
39	0	0	0	0	1	0	0	1	1	1
40	0	0	0	0	1	0	1	0	0	0
41	0	0	0	0	1	0	1	0	0	1
42	0	0	0	0	1	0	1	0	1	0
43	0	0	0	0	1	0	1	0	1	1
44	0	0	0	0	1	0	1	1	0	0
45	0	0	0	0	1	0	1	1	0	1
46	0	0	0	0	1	0	1	1	1	0
47	0	0	0	0	1	0	1	1	1	1
48	0	0	0	0	1	1	0	0	0	0
49	0	0	0	0	1	1	0	0	0	1
50	0	0	0	0	1	1	0	0	1	0
51	0	0	0	0	1	1	0	0	1	1
52	0	0	0	0	1	1	0	1	0	0
53	0	0	0	0	1	1	0	1	0	1
54	0	0	0	0	1	1	0	1	1	0
55	0	0	0	0	1	1	0	1	1	1
56	0	0	0	0	1	1	1	0	0	0
57	0	0	0	0	1	1	1	0	0	1
58	0	0	0	0	1	1	1	0	1	0
59	0	0	0	0	1	1	1	0	1	1
60	0	0	0	0	1	1	1	1	0	0
61	0	0	0	0	1	1	1	1	0	1
62	0	0	0	0	1	1	1	1	1	0
63	0	0	0	0	1	1	1	1	1	1
64	0	0	0	1	0	0	0	0	0	0
65	0	0	0	1	0	0	0	0	0	1
66	0	0	0	1	0	0	0	0	1	0
67	0	0	0	1	0	0	0	0	1	1
68	0	0	0	1	0	0	0	1	0	0
69	0	0	0	1	0	0	0	1	0	1
70	0	0	0	1	0	0	0	1	1	0
71	0	0	0	1	0	0	0	1	1	1
72	0	0	0	1	0	0	1	0	0	0
73	0	0	0	1	0	0	1	0	0	1
74	0	0	0	1	0	0	1	0	1	0
75	0	0	0	1	0	0	1	0	1	1
76	0	0	0	1	0	0	1	1	0	0
77	0	0	0	1	0	0	1	1	0	1
78	0	0	0	1	0	0	1	1	1	0
79	0	0	0	1	0	0	1	1	1	1
80	0	0	0	1	0	1	0	0	0	0
81	0	0	0	1	0	1	0	0	0	1
82	0	0	0	1	0	1	0	0	1	0
83	0	0	0	1	0	1	0	0	1	1
84	0	0	0	1	0	1	0	1	0	0
85	0	0	0	1	0	1	0	1	0	1
86	0	0	0	1	0	1	0	1	1	0
87	0	0	0	1	0	1	0	1	1	1
88	0	0	0	1	0	1	1	0	0	0
89	0	0	0	1	0	1	1	0	0	1
90	0	0	0	1	0	1	1	0	1	0
91	0	0	0	1	0	1	1	0	1	1
92	0	0	0	1	0	1	1	1	0	0
93	0	0	0	1	0	1	1	1	0	1
94	0	0	0	1	0	1	1	1	1	0
95	0	0	0	1	0	1	1	1	1	1
96	0	0	0	1	1	0	0	0	0	0
97	0	0	0	1	1	0	0	0	0	1
98	0	0	0	1	1	0	0	0	1	0
99	0	0	0	1	1	0	0	0	1	1
100	0	0	0	1	1	0	0	1	0	0
101	0	0	0	1	1	0	0	1	0	1
102	0	0	0	1	1	0	0	1	1	0
103	0	0	0	1	1	0	0	1	1	1
104	0	0	0	1	1	0	1	0	0	0
105	0	0	0	1	1	0	1	0	0	1
106	0	0	0	1	1	0	1	0	1	0
107	0	0	0	1	1	0	1	0	1	1
108	0	0	0	1	1	0	1	1	0	0
109	0	0	0	1	1	0	1	1	0	1
110	0	0	0	1	1	0	1	1	1	0
111	0	0	0	1	1	0	1	1	1	1
112	0	0	0	1	1	1	0	0	0	0
113	0	0	0	1	1	1	0	0	0	1
114	0	0	0	1	1	1	0	0	1	0
115	0	0	0	1	1	1	0	0	1	1
116	0	0	0	1	1	1	0	1	0	0
117	0	0	0	1	1	1	0	1	0	1
118	0	0	0	1	1	1	0	1	1	0
119	0	0	0	1	1	1	0	1	1	1
120	0	0	0	1	1	1	1	0	0	0
121	0	0	0	1	1	1	1	0	0	1
122	0	0	0	1	1	1	1	0	1	0
123	0	0	0	1	1	1	1	0	1	1
124	0	0	0	1	1	1	1	1	0	0
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127	0	0	0	1	1	1	1	1	1	1
128	0	0	1	0	0	0	0	0	0	0
129	0	0	1	0	0	0	0	0	0	1
130	0	0	1	0	0	0	0	0	1	0
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134	0	0	1	0	0	0	0	1	1	0
135	0	0	1	0	0	0	0	1	1	1
136	0	0	1	0	0	0	1	0	0	0
137	0	0	1	0	0	0	1	0	0	1
138	0	0	1	0	0	0	1	0	1	0
139	0	0	1	0	0	0	1	0	1	1
140	0	0	1	0	0	0	1	1	0	0
141	0	0	1	0	0	0	1	1	0	1
142	0	0	1	0	0	0	1	1	1	0
143	0	0	1	0	0	0	1	1	1	1
144	0	0	1	0	0	1	0	0	0	0
145	0	0	1	0	0	1	0	0	0	1
146	0	0	1	0	0	1	0	0	1	0
147	0	0	1	0	0	1	0	0	1	1
148	0	0	1	0	0	1	0	1	0	0
149	0	0	1	0	0	1	0	1	0	1
150	0	0	1	0	0	1	0	1	1	0
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152	0	0	1	0	0	1	1	0	0	0
153	0	0	1	0	0	1	1	0	0	1
154	0	0	1	0	0	1	1	0	1	0
155	0	0	1	0	0	1	1	0	1	1
156	0	0	1	0	0	1	1	1	0	0
157	0	0	1	0	0	1	1	1	0	1
158	0	0	1	0	0	1	1	1	1	0
159	0	0	1	0	0	1	1	1	1	1
160	0	0	1	0	1	0	0	0	0	0
161	0	0	1	0	1	0	0	0	0	1
162	0	0	1	0	1	0	0	0	1	0
163	0	0	1	0	1	0	0	0	1	1
164	0	0	1	0	1	0	0	1	0	0
165	0	0	1	0	1	0	0	1	0	1
166	0	0	1	0	1	0	0	1	1	0
167	0	0	1	0	1	0	0	1	1	1
168	0	0	1	0	1	0	1	0	0	0
169	0	0	1	0	1	0	1	0	0	1
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182	0	0	1	0	1	1	0	1	1	0
183	0	0	1	0	1	1	0	1	1	1
184	0	0	1	0	1	1	1	0	0	0
185	0	0	1	0	1	1	1	0	0	1
186	0	0	1	0	1	1	1	0	1	0
187	0	0	1	0	1	1	1	0	1	1
188	0	0	1	0	1	1	1	1	0	0
189	0	0	1	0	1	1	1	1	0	1
190	0	0	1	0	1	1	1	1	1	0
191	0	0	1	0	1	1	1	1	1	1
192	0	0	1	1	0	0	0	0	0	0
193	0	0	1	1	0	0	0	0	0	1
194	0	0	1	1	0	0	0	0	1	0
195	0	0	1	1	0	0	0	0	1	1
196	0	0	1	1	0	0	0	1	0	0
197	0	0	1	1	0	0	0	1	0	1
198	0	0	1	1	0	0	0	1	1	0
199	0	0	1	1	0	0	0	1	1	1
200	0	0	1	1	0	0	1	0	0	0
201	0	0	1	1	0	0	1	0	0	1
202	0	0	1	1	0	0	1	0	1	0
203	0	0	1	1	0	0	1	0	1	1
204	0	0	1	1	0	0	1	1	0	0
205	0	0	1	1	0	0	1	1	0	1
206	0	0	1	1	0	0	1	1	1	0
207	0	0	1	1	0	0	1	1	1	1
208	0	0	1	1	0	1	0	0	0	0
209	0	0	1	1	0	1	0	0	0	1
210	0	0	1	1	0	1	0	0	1	0
211	0	0	1	1	0	1	0	0	1	1
212	0	0	1	1	0	1	0	1	0	0
213	0	0	1	1	0	1	0	1	0	1
214	0	0	1	1	0	1	0	1	1	0
215	0	0	1	1	0	1	0	1	1	1
216	0	0	1	1	0	1	1	0	0	0
217	0	0	1	1	0	1	1	0	0	1
218	0	0	1	1	0	1	1	0	1	0
219	0	0	1	1	0	1	1	0	1	1
220	0	0	1	1	0	1	1	1	0	0
221	0	0	1	1	0	1	1	1	0	1
222	0	0	1	1	0	1	1	1	1	0
223	0	0	1	1	0	1	1	1	1	1
224	0	0	1	1	1	0	0	0	0	0
225	0	0	1	1	1	0	0	0	0	1
226	0	0	1	1	1	0	0	0	1	0
227	0	0	1	1	1	0	0	0	1	1
228	0	0	1	1	1	0	0	1	0	0
229	0	0	1	1	1	0	0	1	0	1
230	0	0	1	1	1	0	0	1	1	0
231	0	0	1	1	1	0	0	1	1	1
232	0	0	1	1	1	0	1	0	0	0
233	0	0	1	1	1	0	1	0	0	1
234	0	0	1	1	1	0	1	0	1	0
235	0	0	1	1	1	0	1	0	1	1
236	0	0	1	1	1	0	1	1	0	0
237	0	0	1	1	1	0	1	1	0	1
238	0	0	1	1	1	0	1	1	1	0
239	0	0	1	1	1	0	1	1	1	1
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241	0	0	1	1	1	1	0	0	0	1
242	0	0	1	1	1	1	0	0	1	0
243	0	0	1	1	1	1	0	0	1	1
244	0	0	1	1	1	1	0	1	0	0
245	0	0	1	1	1	1	0	1	0	1
246	0	0	1	1	1	1	0	1	1	0
247	0	0	1	1	1	1	0	1	1	1
248	0	0	1	1	1	1	1	0	0	0
249	0	0	1	1	1	1	1	0	0	1
250	0	0	1	1	1	1	1	0	1	0
251	0	0	1	1	1	1	1	0	1	1
252	0	0	1	1	1	1	1	1	0	0
253	0	0	1	1	1	1	1	1	0	1
254	0	0	1	1	1	1	1	1	1	0
255	0	0	1	1	1	1	1	1	1	1

V	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
256	0	1	0	0	0	0	0	0	0	0
257	0	1	0	0	0	0	0	0	0	1
258	0	1	0	0	0	0	0	0	1	0
259	0	1	0	0	0	0	0	0	1	1
260	0	1	0	0	0	0	0	1	0	0
261	0	1	0	0	0	0	0	1	0	1
262	0	1	0	0	0	0	0	1	1	0
263	0	1	0	0	0	0	0	1	1	1
264	0	1	0	0	0	0	1	0	0	0
265	0	1	0	0	0	0	1	0	0	1
266	0	1	0	0	0	0	1	0	1	0
267	0	1	0	0	0	0	1	0	1	1
268	0	1	0	0	0	0	1	1	0	0
269	0	1	0	0	0	0	1	1	0	1
270	0	1	0	0	0	0	1	1	1	0
271	0	1	0	0	0	0	1	1	1	1
272	0	1	0	0	0	1	0	0	0	0
273	0	1	0	0	0	1	0	0	0	1
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1
276	0	1	0	0	0	1	0	1	0	0
277	0	1	0	0	0	1	0	1	0	1
278	0	1	0	0	0	1	0	1	1	0
279	0	1	0	0	0	1	0	1	1	1
280	0	1	0	0	0	1	1	0	0	0
281	0	1	0	0	0	1	1	0	0	1
282	0	1	0	0	0	1	1	0	1	0
283	0	1	0	0	0	1	1	0	1	1
284	0	1	0	0	0	1	1	1	0	0
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286	0	1	0	0	0	1	1	1	1	0
287	0	1	0	0	0	1	1	1	1	1
288	0	1	0	0	1	0	0	0	0	0
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290	0	1	0	0	1	0	0	0	1	0
291	0	1	0	0	1	0	0	0	1	1
292	0	1	0	0	1	0	0	1	0	0
293	0	1	0	0	1	0	0	1	0	1
294	0	1	0	0	1	0	0	1	1	0
295	0	1	0	0	1	0	0	1	1	1
296	0	1	0	0	1	0	1	0	0	0
297	0	1	0	0	1	0	1	0	0	1
298	0	1	0	0	1	0	1	0	1	0
299	0	1	0	0	1	0	1	0	1	1
300	0	1	0	0	1	0	1	1	0	0
301	0	1	0	0	1	0	1	1	0	1
302	0	1	0	0	1	0	1	1	1	0
303	0	1	0	0	1	0	1	1	1	1
304	0	1	0	0	1	1	0	0	0	0
305	0	1	0	0	1	1	0	0	0	1
306	0	1	0	0	1	1	0	0	1	0
307	0	1	0	0	1	1	0	0	1	1
308	0	1	0	0	1	1	0	1	0	0
309	0	1	0	0	1	1	0	1	0	1
310	0	1	0	0	1	1	0	1	1	0
311	0	1	0	0	1	1	0	1	1	1
312	0	1	0	0	1	1	1	0	0	0
313	0	1	0	0	1	1	1	0	0	1
314	0	1	0	0	1	1	1	0	1	0
315	0	1	0	0	1	1	1	0	1	1
316	0	1	0	0	1	1	1	1	0	0
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318	0	1	0	0	1	1	1	1	1	0
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326	0	1	0	1	0	0	0	1	1	0
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364	0	1	0	1	1	0	1	1	0	0
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430	0	1	1	0	1	0	1	1	1	0
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432	0	1	1	0	1	1	0	0	0	0
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436	0	1	1	0	1	1	0	1	0	0
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468	0	1	1	1	0	1	0	1	0	0
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476	0	1	1	1	0	1	1	1	0	0
477	0	1	1	1	0	1	1	1	0	1
478	0	1	1	1	0	1	1	1	1	0
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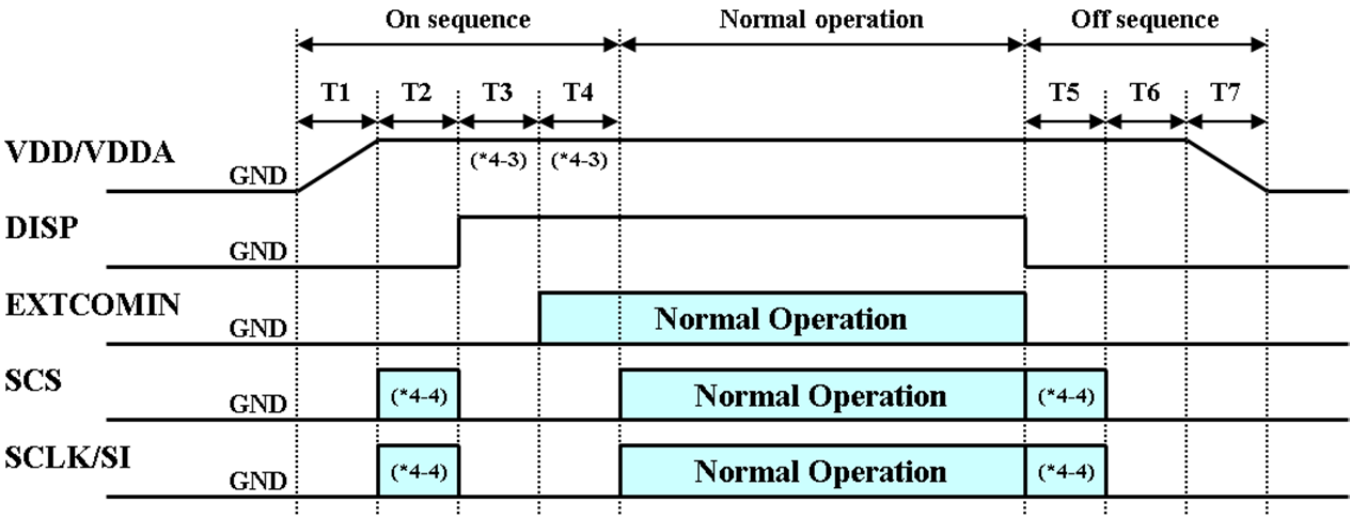
480	0	1	1	1	1	0	0	0	0	0

8.9 POWER SUPPLY SEQUENCR



[On sequence]

T1 : Power supply rising time. (Depends on external power supply)

T2 : Pixel memory initialization. 1-tV(refer to 8.3.3) or more initialize with M2 (all clear flag) or write black data to all pixel memories (data update).

T3 : Release time for internal latch circuits. 30usec or more

T4 : COM polarity initialization time. 30usec or more

[Normal operation]

Duration of normal operation

[Off sequence]

T5 : Pixel memory initialization. Same as T2.

T6 : COM and latch circuits initialization. 30usec or more

T7 : Power supply falling time. (Depends on external power supply)

[Remark]

V_{DD} and V_{DDA} should rise simultaneously or V_{DD} should rise first.

V_{DD} and V_{DDA} should fall simultaneously or V_{DDA} should fall first.

Note 1: It is allowed to replace T3 and T4 mutually.

In case of starting EXTCOMIN before rising DISP, EXTCOMIN is ignored during DISP="L". Also, it is allowed to start simultaneously DISP and EXTCOMIN.

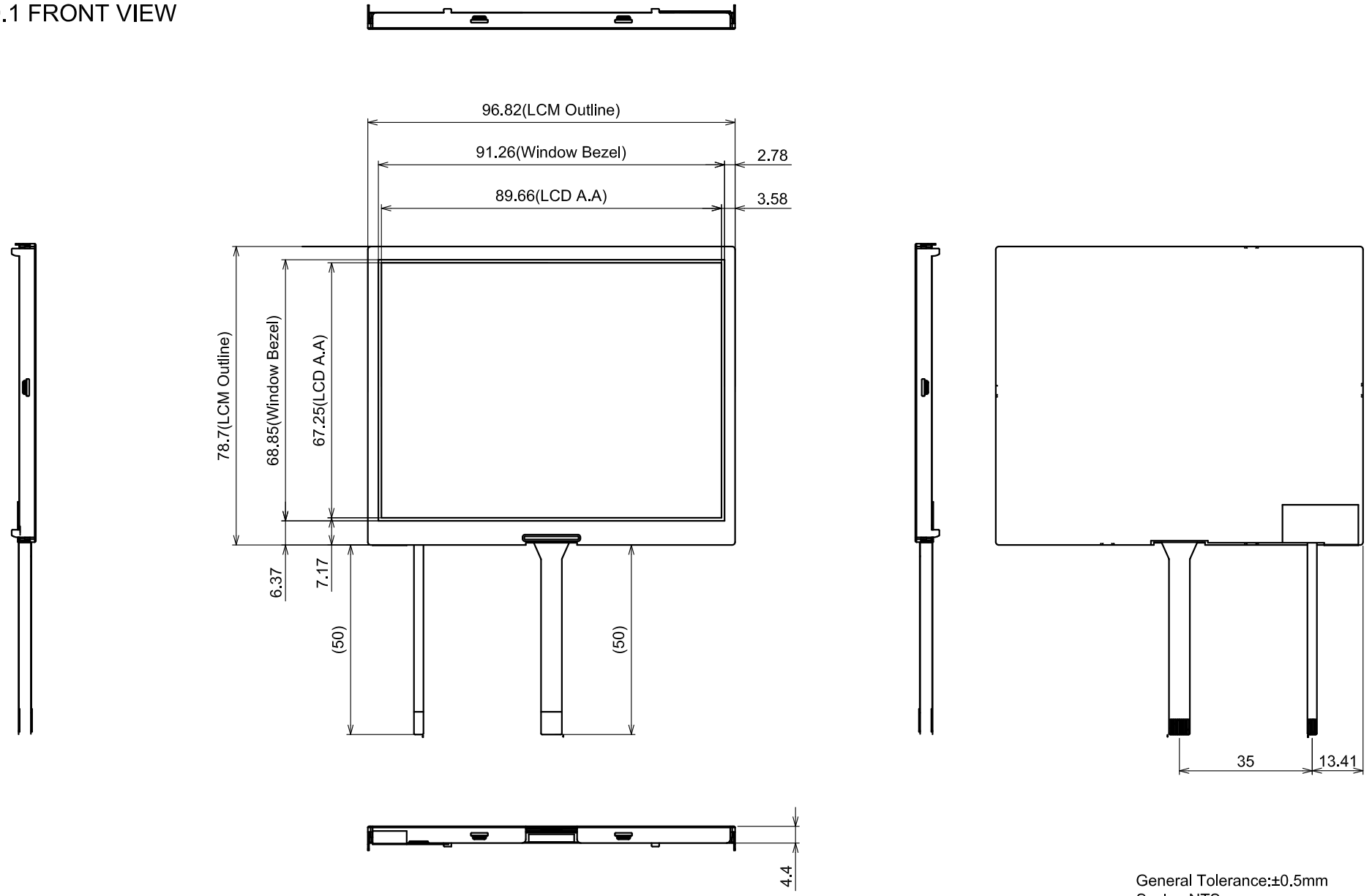
In that case, need 100usec or more (200usec or less) before normal operation.

Note 2: Pixel memory initialization.

Use M2 (all clear flag : refer to the 8.4.5), or write black data to all pixel memories (refer to the data update mode).

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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