

TECHNICAL DATA

TX38D95VC1CAH

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RECORD OF REVISION

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S C O P E

This specification is applied to the following TFT Liquid Crystal Display Module with Back-light unit.

Note : Inverter device for Back-light is not built in and so it needs to be prepared on yoursides.

- Type name : TX38D95VC1CAH
- Display Area : H304.5×V228.375 [mm]
- Display Dots : H(1400×3)×V1050 [dots]
(Display Pixels) (H1400×V1050 pixels)
- Voltage of VDD : 3.3V
- Pixel Pitch : H0.2175×V0.2175
- Color Pixel Arrangement : R·G·B Vertical Stripe
- Display Mode : Transmissive &
Normally White Mode
- Color Number : 262k Colors
- Direction with Wider Viewing Angle : Lower side of 6 o'clock
(Azimuth $\phi=270^\circ$)
- Dimensions Outlines : 315(W)×240(H)×6.8MAX(T) [mm]
- Weight : Approximately 660 [g]
- Interface : 2ch-LVDS
- Surface Polarizing Film : Polarizing Film with Antiglare Coating
- Back-light : One Cold Cathode Florescent Lamp
(Lower side)
Back-light inverter is not
contained in Module.

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		UNIT	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	10	40	-20	60	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	—	4.9 (0.5G)	—	19.6 (2G)	m/s ²	3), 5)
Shock	—	29.4 (3G)	—	490 (50G)		4), 5)
Corrosive Gas	NOT ACCEPTABLE		NOT ACCEPTABLE		—	
Illuminance at LCD surface	—	50,000	—	50,000	lx	

Note 1) Environmental temperature and humidity of this unit, not of system installed with this unit.

At low temperature the brightness of CFL drop and the life time of CFL become to be short.

2) Ambient temp. $T_a \leq 40^\circ\text{C}$: 85%RH MAX. without condensation
 $T_a > 40^\circ\text{C}$: Absolute humidity must be lower than the saturated vapor of 85%RH at 40°C . without condensation

3) Vibration frequency : 20~50Hz. (Except resonance frequency)

4) 7ms of pulse width.

5) With mounting protective spacer(ref.page 4-2/2)

1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

V_{SS}=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD	0	4.0	V	
Electrostatic Durability	VESD0	± 100		v	1), 2)
	VESD1	± 8		kV	1), 3)

Note 1) Discharge circuit : 200pF-250Ω, Surrounding : 25℃-70%RH.

2) The specification is applicable to I/F Connector pins.

3) The specification is applicable to metal bezel and LCD glass.

(2) BACK-LIGHT UNIT

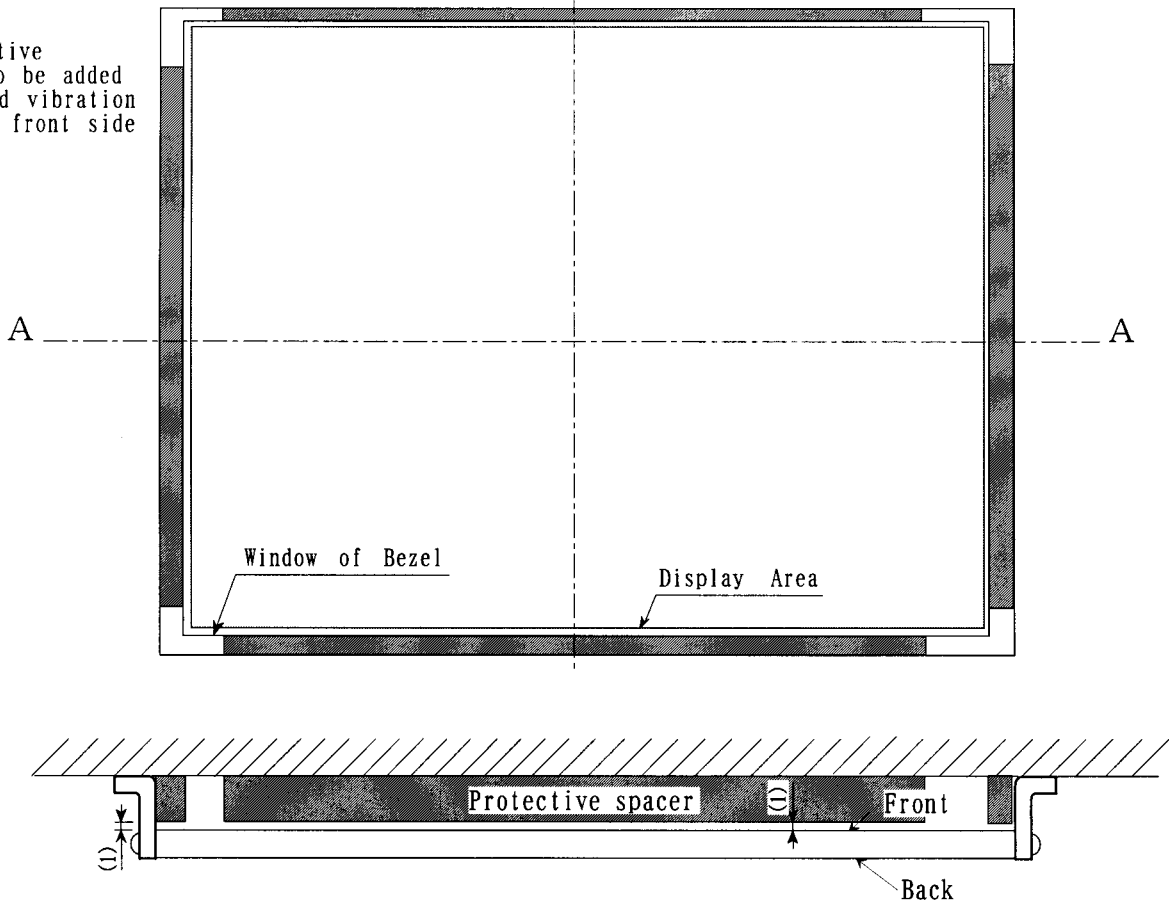
GND=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Lamp Current	IL	0	7.0	mArms	1)
Lamp Voltage	VL	0	2000	Vrms	

Note 1) At Lamp start-up time.

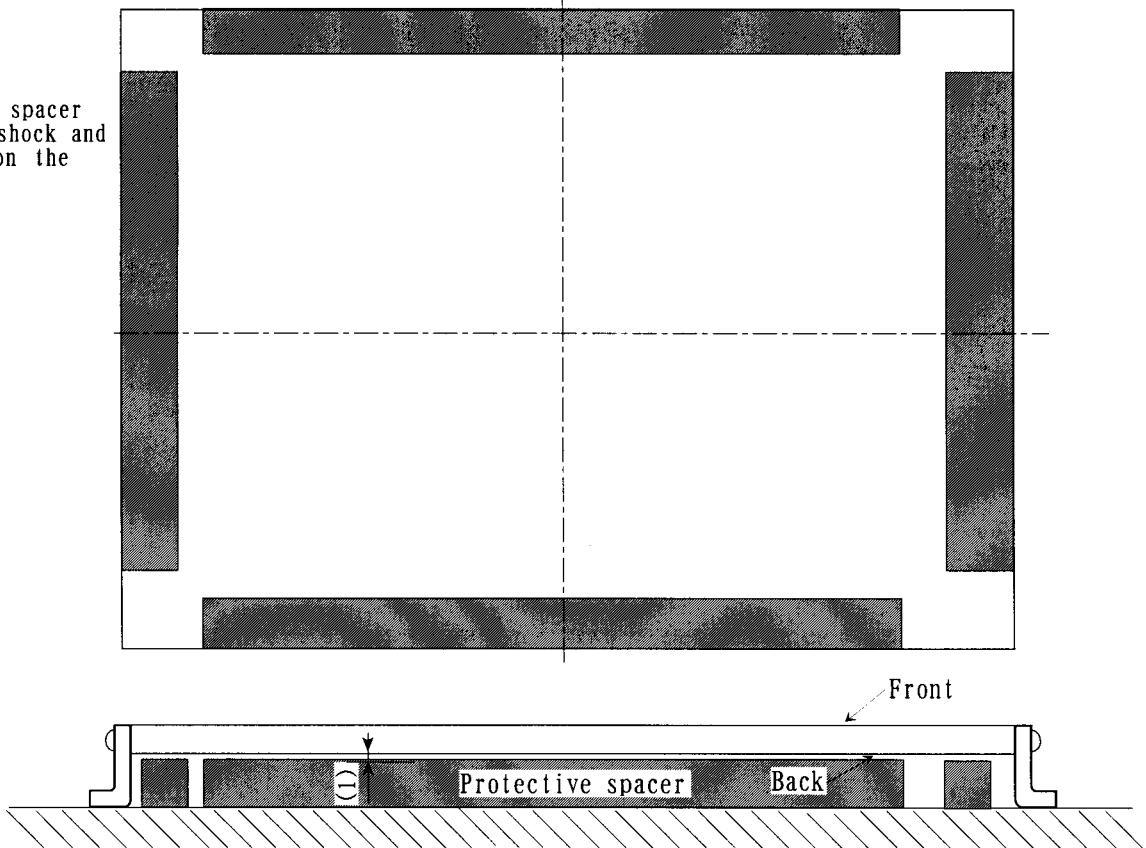
Adding protective spacer at shock & vibration test
 Shaded area is to be supported with additional spacer.

- (1) This protective spacer is to be added at shock and vibration test on the front side



Shaded area is to be supported with additional spacer.

- (2) This protective spacer is to be added shock and vibration test on the back side



2. OPTICAL CHARACTERISTICS

The following items are measured on the conditions that this unit operation (TFT panel and Back-light) and measuring systems are stable.

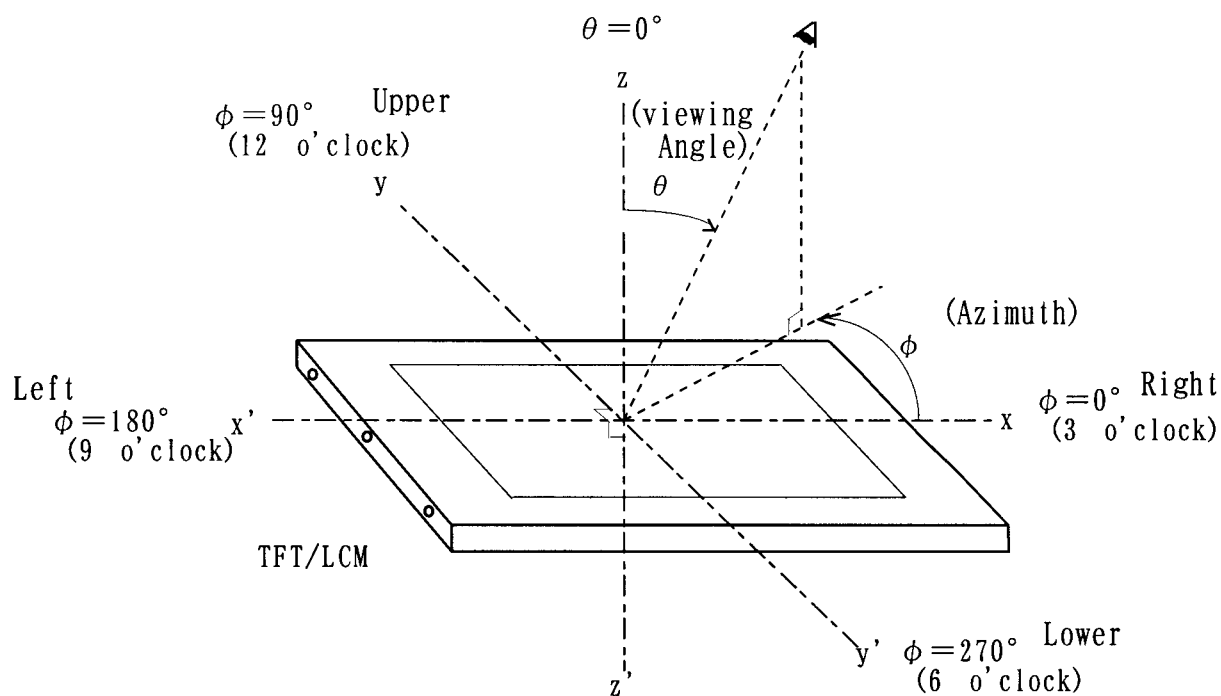
The ambient light excluding The Back-light unit is nothing.

- Measuring equipment : TOPCON BM-7, Prichard 1980B, or equivalent
- Measuring point : Active area center

Temperature of LCD=25°C, VDD=3.3V, fv=60Hz, IL=6mA,
Back-Light operation Frequency=50kHz

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio		CR	$\theta = 0^\circ$ Note 1)	100	—	—	—	2)
Response Time	RISE	tr		—	37	—	ms	3)
	FALL	tf		—	20	—		
Brightness (White)		Bwh		100	150	—	cd/m ²	
Color of CIE	Red	x		0.55	0.58	0.61	—	
		y		0.30	0.33	0.36		
	Green	x		0.27	0.30	0.33		
		y		0.54	0.57	0.60		
	Blue	x		0.12	0.15	0.18		
		y		0.11	0.14	0.17		
	White	x		0.29	0.32	0.35		
		y		0.30	0.33	0.36		

Note 1) Definition of Viewing Angle



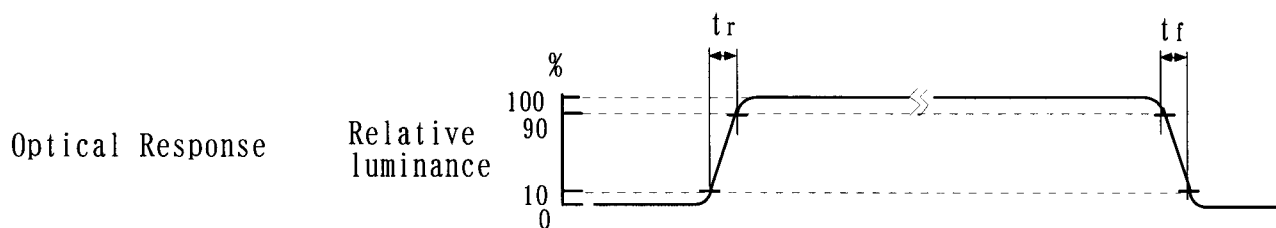
Note 2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

These Brightness is measured on the center of screen.

* Measurement in the darkroom.

Note 3) Definition of Response Time



1. ELECTRICAL CHARACTERISTICS

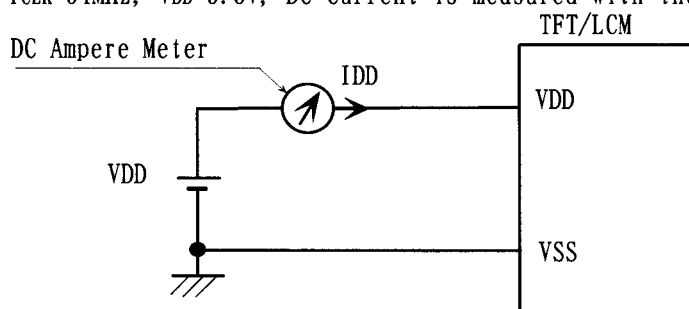
(1) TFT LIQUID CRYSTAL DISPLAY MODULE

Ta=25°C, Vss=0V

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	Hi	V _{IH}	—	+100	mV	1)
	Lo	V _{IL}	—	—		
Power Supply Current	I _{DD}	—	530	900	mA	2), 3)
Vsync Frequency	f _v	—	60	65	Hz	4)
Hsync Frequency	f _H	—	61	76	kHz	4)
DCLK Frequency	f _{CLK}	51	54	57	MHz	4)

Note 1) Common Mode Voltage V_{CM}=+1.25V

2) f_v=60Hz, f_{CLK}=54MHz, VDD=3.3V, DC Current is measured with the method as below.



Typical value is measured when displaying vertical with 63th gray scale. Maximum is measured when displaying Vertical-stripe(Black-7 Gray scale)

- 3) Current capacity for VDD power supply should be larger than 3A, so that the fuse built in the unit(Maximum) could appropriately work in the abnormal.
4) For LVDS Transmitter Input.

(2) BACK-LIGHT UNIT

Ta=25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Lamp Current	I _L	4.0	—	6.0	mArms	1), 2), 5)
		—	—	10	mA0-peak	
Lamp Voltage	V _L	—	690	—	Vrms	
Frequency	f _L	40	50	70	kHz	3)
Starting Lamp Voltage	V _s	Ta=25°C	1100	—	Vrms	4)
		Ta=10°C	1500	—		4)

NOTE 1) Higher I_L cause the short life time of CFL.

2) DC current cause irregular fluorescence and the short life of CFL.

3) Lamp operation frequency may produce interference with Hsync frequency, which causes rolling or flickering screen. Therefore lamp operation frequency shall be as different as possible from Hsync frequency, to avoid interference.

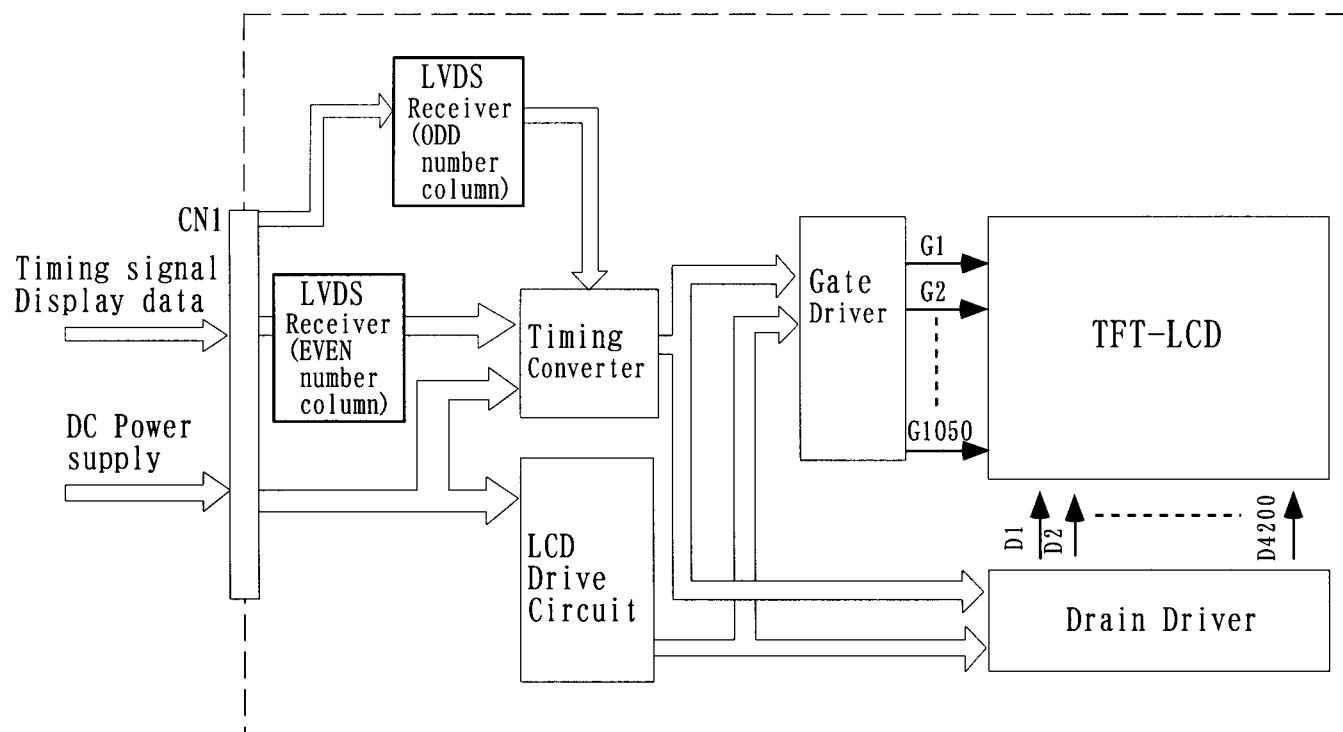
4) Lamp start-up voltage should be more than V_s(min)

5) Reducing Lamp current increases Lamp voltage and generally increases Lamp operation frequency.

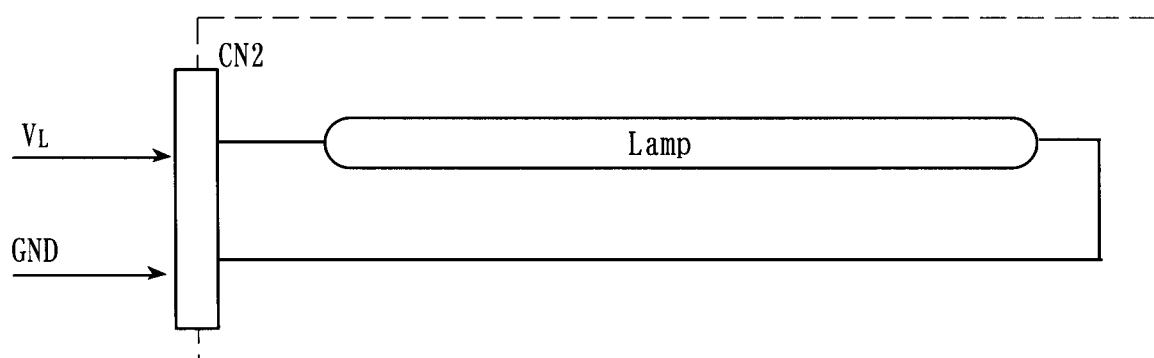
CFL inverter should be designed with taking account of minimizing the leakage current from the high-voltage output.

4. BLOCK DIAGRAM

(1) TFT LIQUID CRYSTAL DISPLAY MODULE



(2) BACK-LIGHT UNIT



5. INTERFACE PIN CONNECTION

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

CN1 «JAE FI-SEB20P-HF-A or Compatible»

Pin No	SYMBOL	FUNCTION	NOTE
1	VDD	Power Supply 3.3V nominal	2)
2	VDD	Power Supply 3.3V nominal	2)
3	VSS	Ground	1)
4	VSS	Ground	1)
5	R1in0-	LVDS Differential Data INPUT (-) for Odd	
6	R1in0+	LVDS Differential Data INPUT (+) for Odd	
7	R1in1-	LVDS Differential Data INPUT (-) for Odd	
8	R1in1+	LVDS Differential Data INPUT (+) for Odd	
9	R1in2-	LVDS Differential Data INPUT (-) for Odd	
10	R1in2+	LVDS Differential Data INPUT (+) for Odd	
11	R1CLK-	LVDS Differential Clock INPUT (-) for Odd	
12	R1CLK+	LVDS Differential Clock INPUT (+) for Odd	
13	R2in0-	LVDS Differential Data INPUT (-) for Even	
14	R2in0+	LVDS Differential Data INPUT (+) for Even	
15	R2in1-	LVDS Differential Data INPUT (-) for Even	
16	R2in1+	LVDS Differential Data INPUT (+) for Even	
17	R2in2-	LVDS Differential Data INPUT (-) for Even	
18	R2in2+	LVDS Differential Data INPUT (+) for Even	
19	R2CLK-	LVDS Differential Clock INPUT (-) for Even	
20	R2CLK+	LVDS Differential Clock INPUT (+) for Even	

Note 1) All Vss pins should be connected to GND(0V).

Metal bezel is connected internally to Vss.

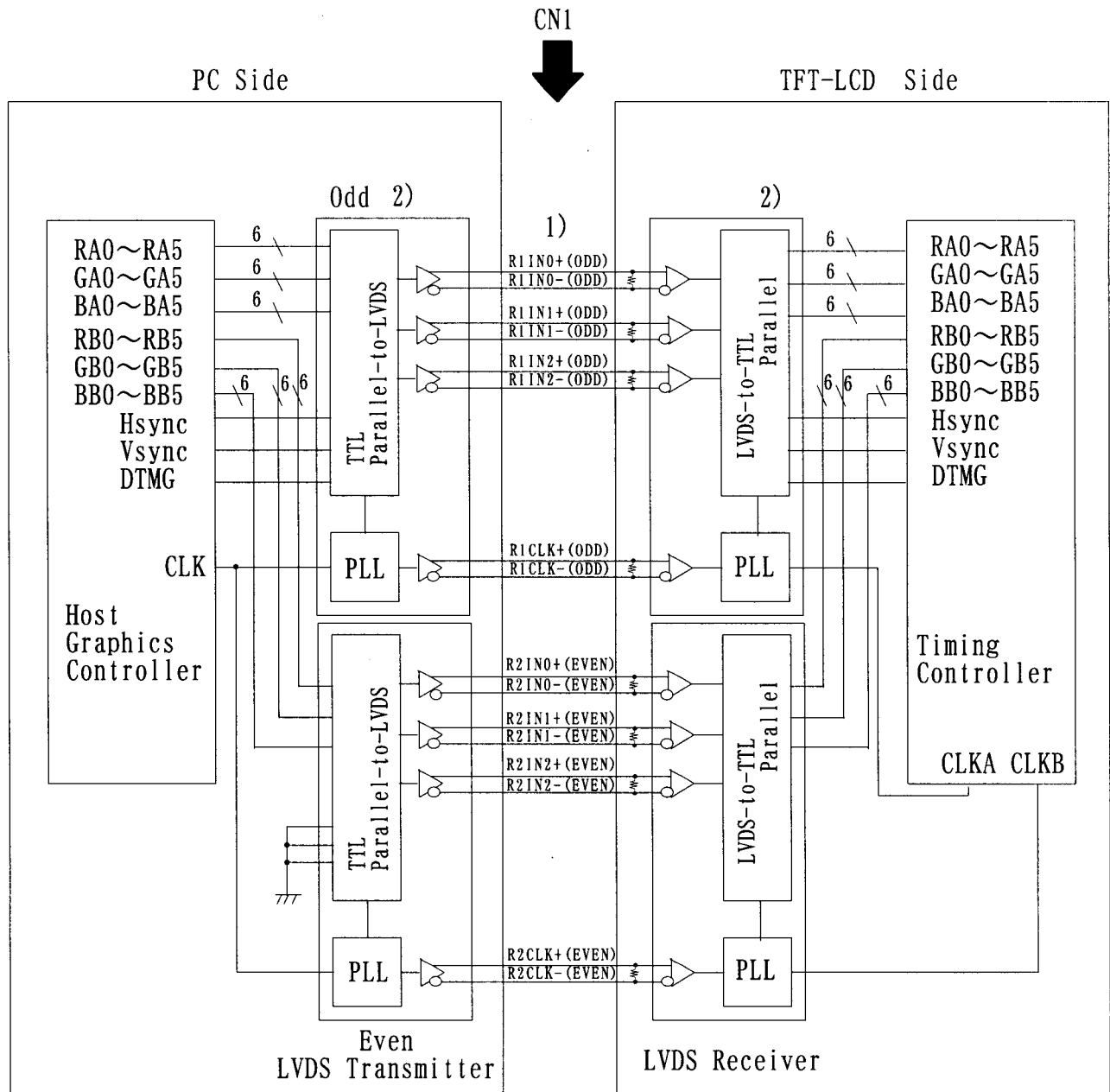
2) All Vdd pins should be connected to +3.3V.

(2) BACK-LIGHT UNIT

CN2 «JST BHSR-02VS-1»

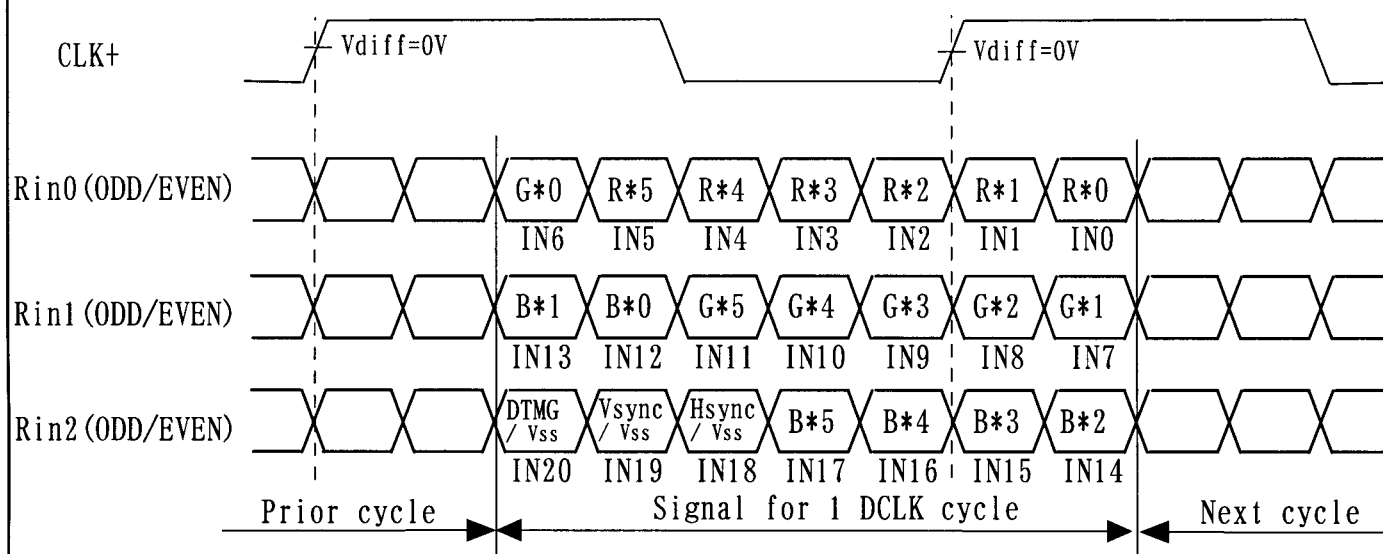
Pin No	SYMBOL	DESCRIPTION
1	V _L	Power Supply
2	GND	GND (0V)

LVDS INTERFACE



- NOTE: 1) LVDS cable impedance should be 100 ohms per signal line when each 2-lines(+,-) is used in differential mode.
 2) LVDS transmitter is not contained in the Module.
 3) Odd data ; RA0~RA5, GA0~GA5, BA0~BA5, Hsync, Vsync, DTMG
 Even data ; RB0~RB5, GA0~GA5, BB0~BB5, Vss, Vss, Vss

LVDS INPUT SIGNAL



Pin connection in case of using
TI SN75LVDS84
Odd Data

Graphic Controller output	Transmitter SN75LVDS84
DCLK	CLK IN(26)
RA0	IN0 (44)
RA1	IN1 (45)
RA2	IN2 (47)
RA3	IN3 (48)
RA4	IN4 (1)
RA5	IN5 (3)
GA0	IN6 (4)
GA1	IN7 (6)
GA2	IN8 (7)
GA3	IN9 (9)
GA4	IN (10)
GA5	IN11 (12)
BA0	IN12 (13)
BA1	IN13 (15)
BA2	IN14 (16)
BA3	IN15 (18)
BA4	IN16 (19)
BA5	IN17 (20)
Hsync	IN18 (22)
Vsync	IN19 (23)
DTMG	IN20 (25)

EVEN

Graphic Controller output	Transmitter SN75LVDS84
DCLK	CLK IN(26)
RB0	IN0 (44)
RB1	IN1 (45)
RB2	IN2 (47)
RB3	IN3 (48)
RB4	IN4 (1)
RB5	IN5 (3)
GB0	IN6 (4)
GB1	IN7 (6)
GB2	IN8 (7)
GB3	IN9 (9)
GB4	IN (10)
GB5	IN11 (12)
BB0	IN12 (13)
BB1	IN13 (15)
BB2	IN14 (16)
BB3	IN15 (18)
BB4	IN16 (19)
BB5	IN17 (20)
Vss	IN18 (22)
Vss	IN19 (23)
Vss	IN20 (25)

- 1) () indicate pin NO (IC).
- 2) Even IN18~20 are connected to Vss

CORRESPONDENCE BETWEEN INPUT DATA AND _

SCREEN IMAGE FOR LVDS TRANSMITTER

Display data of each adjacent two pixels are latched during one cycle of DCLK.

(1, 1)			(1, 2)		
RA	GA	BA	RB	GB	BB

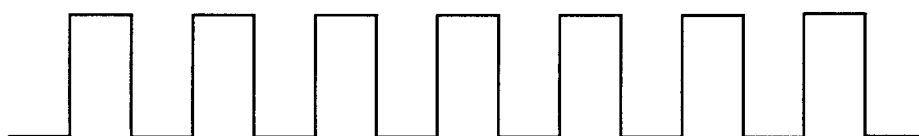
First Pixel Data : RA0~RA5, GA0~GA5, BA0~BA5

Second Pixel Data : RB0~RB5, GB0~GB5, BB0~BB5

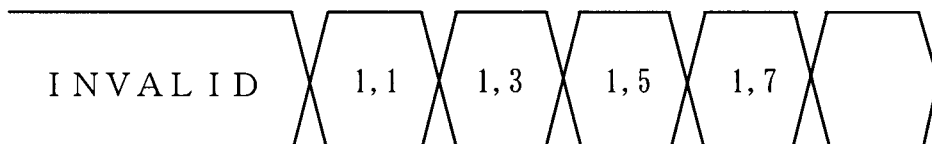
1, 1	1, 2	1, 3	-----	1, 1400
2, 1	2, 2	2, 3	-----	2, 1400
3, 1	3, 2	3, 3	-----	3, 1400
:	:	:		:
:	:	:		:
:	:	:		:
1050, 1	1050, 2	1050, 3	-----	1050, 1400

Location of screen corresponding to each input data

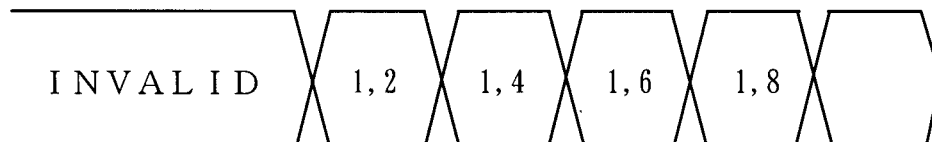
DCLK



RA0~RA5
GA0~GA5
BA5~BA5



RB0~RB5
GB0~GB5
BB5~BB5



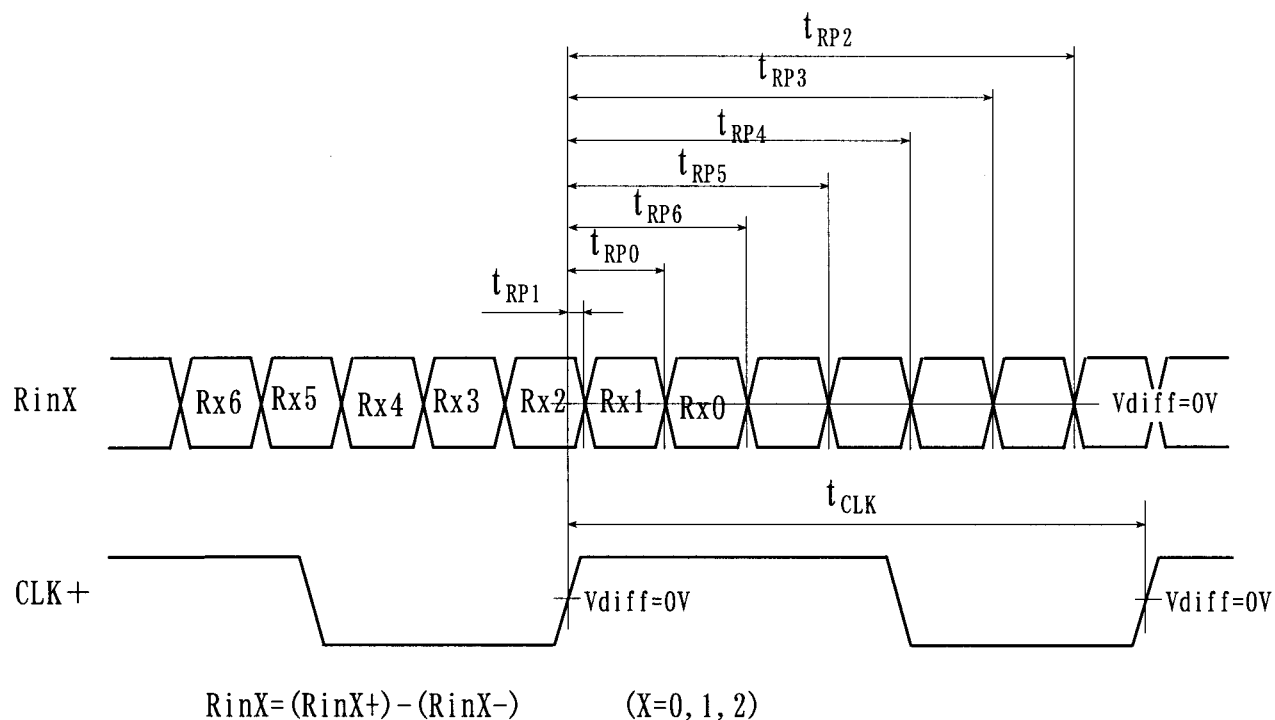
RELATIONSHIP BETWEEN DISPLAYED COLOR AND INPUT DATA

INPUT DATA COLOR		R DATA						G DATA						B DATA					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB			LSB			MSB			LSB			MSB			LSB		
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED (2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
	RED (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	GREEN (2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
	GREEN (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
	BLUE (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...

- Note 1) Definition of gray scale :
Color(n) --- number in parenthesis indicates gray scale level.
Larger number corresponds to brighter level.
2) Data : 1:High, 0:Low

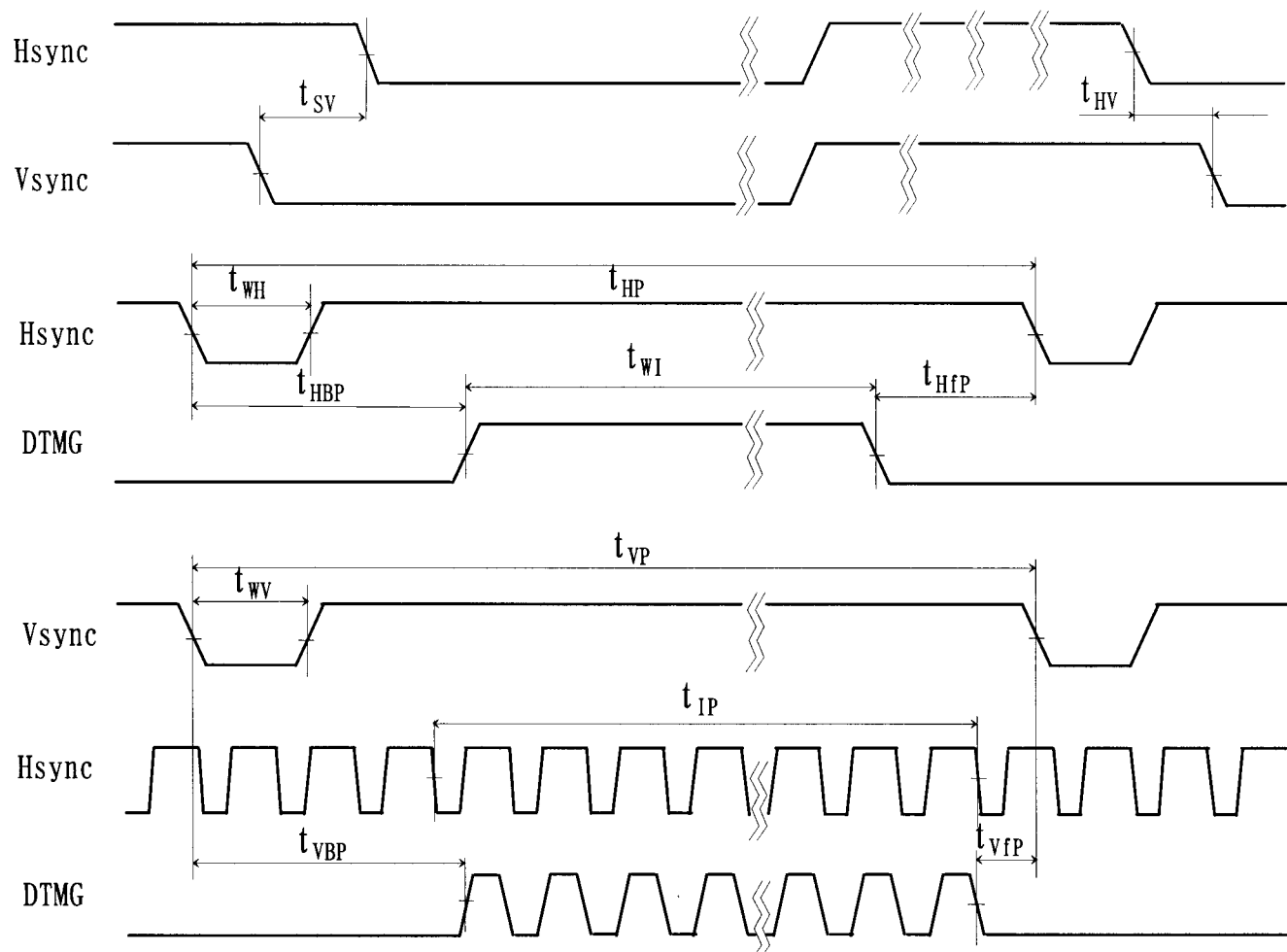
6. Interface timing

(1) LVDS receiver timing (Interface of TFT module)



ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
DCLK	Frequency	$1/t_{CLK}$	51	54	57	MHz
RinX (X=0, 1, 2)	0 data position	t_{RP0}	$\frac{1}{7}t_{CLK}-0.49$	$\frac{1}{7}t_{CLK}$	$\frac{1}{7}t_{CLK}+0.49$	
	1st data position	t_{RP1}	-0.49	0	+0.49	
	2nd data position	t_{RP2}	$\frac{6}{7}t_{CLK}-0.49$	$\frac{6}{7}t_{CLK}$	$\frac{6}{7}t_{CLK}+0.49$	
	3rd data position	t_{RP3}	$\frac{5}{7}t_{CLK}-0.49$	$\frac{5}{7}t_{CLK}$	$\frac{5}{7}t_{CLK}+0.49$	
	4th data position	t_{RP4}	$\frac{4}{7}t_{CLK}-0.49$	$\frac{4}{7}t_{CLK}$	$\frac{4}{7}t_{CLK}+0.49$	
	5th data position	t_{RP5}	$\frac{3}{7}t_{CLK}-0.49$	$\frac{3}{7}t_{CLK}$	$\frac{3}{7}t_{CLK}+0.49$	
	6th data position	t_{RP6}	$\frac{2}{7}t_{CLK}-0.49$	$\frac{2}{7}t_{CLK}$	$\frac{2}{7}t_{CLK}+0.49$	

(2) timing converter timing
(Input timing for transmitter)



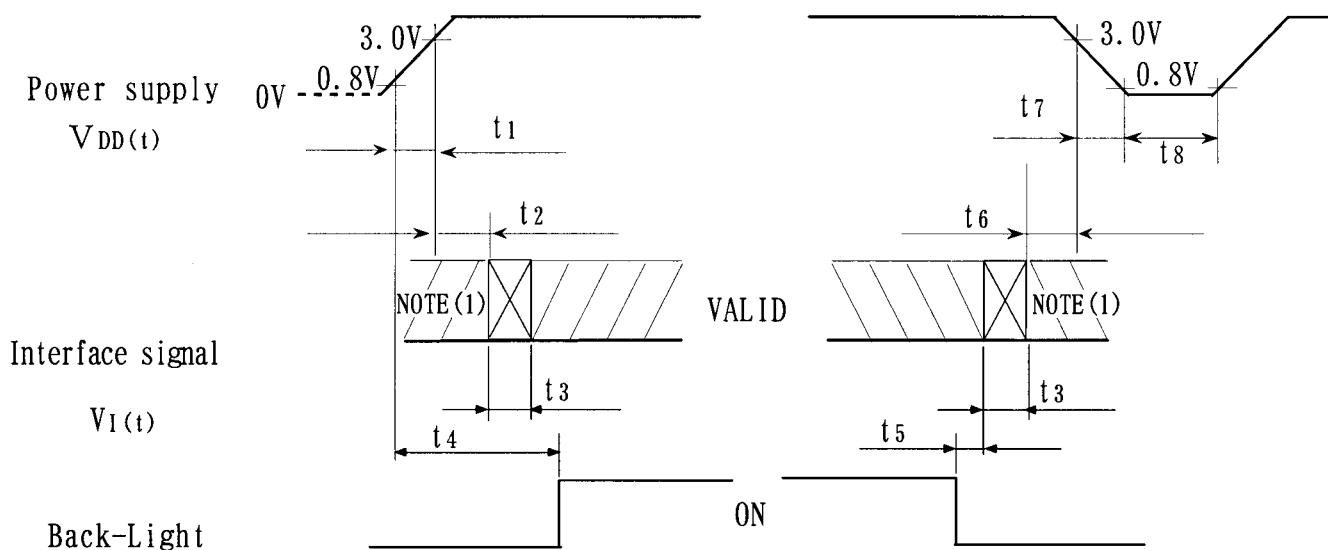
The timings except mentioned on the above should conform to the specifications of LVDS transmitter in your system.

	Item	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Hsync	Period	t_{HP}	820	844	1023	t_{CLK}	
	Width-Active	t_{WH}	(10)	—	(240)		
Vsync	Set up Time	t_{SV}	(-2)	—	—	t_{CLK}	for Hsync signal
	Hold time	t_{HV}	(0)	—	—		
	period	t_{VP}	1059	1068	2047	t_{HP}	
	Width-Active	t_{WV}	1	—	(120)	t_{HP}	
DTMG	Width-Active	t_{WI}	700	700	700	t_{CLK}	
	Period	t_{IP}	1050	1050	1050	t_{HP}	
	Horizontal Back Porch	t_{HBP}	(32)	—	(120)	t_{CLK}	
	Horizontal Front Porch	t_{HFP}	(0)	—	—		
	Vertical Back Porch	t_{VBP}	3	—	—	t_{HP}	1)
	Vertical Front Porch	t_{VFP}	0	—	—		

NOTE In addition to the above, t_{VBP} and t_{VFP} should be

1) $t_{VBP} + t_{VFP} \geq 3 \times t_{HP}$

(3) TIMING BETWEEN INTERFACE SIGNAL AND POWER SUPPLY



POWER ON

$t_1 \leq 15\text{ms}$

$0 < t_2 \leq 45\text{ms}$

$0 \leq t_3 \leq 5\text{ms}$

$0.1\text{s} \leq t_4$

POWER OFF

$5\text{ms} \leq t_5$

$0 \leq t_6 \leq 45\text{ms}$

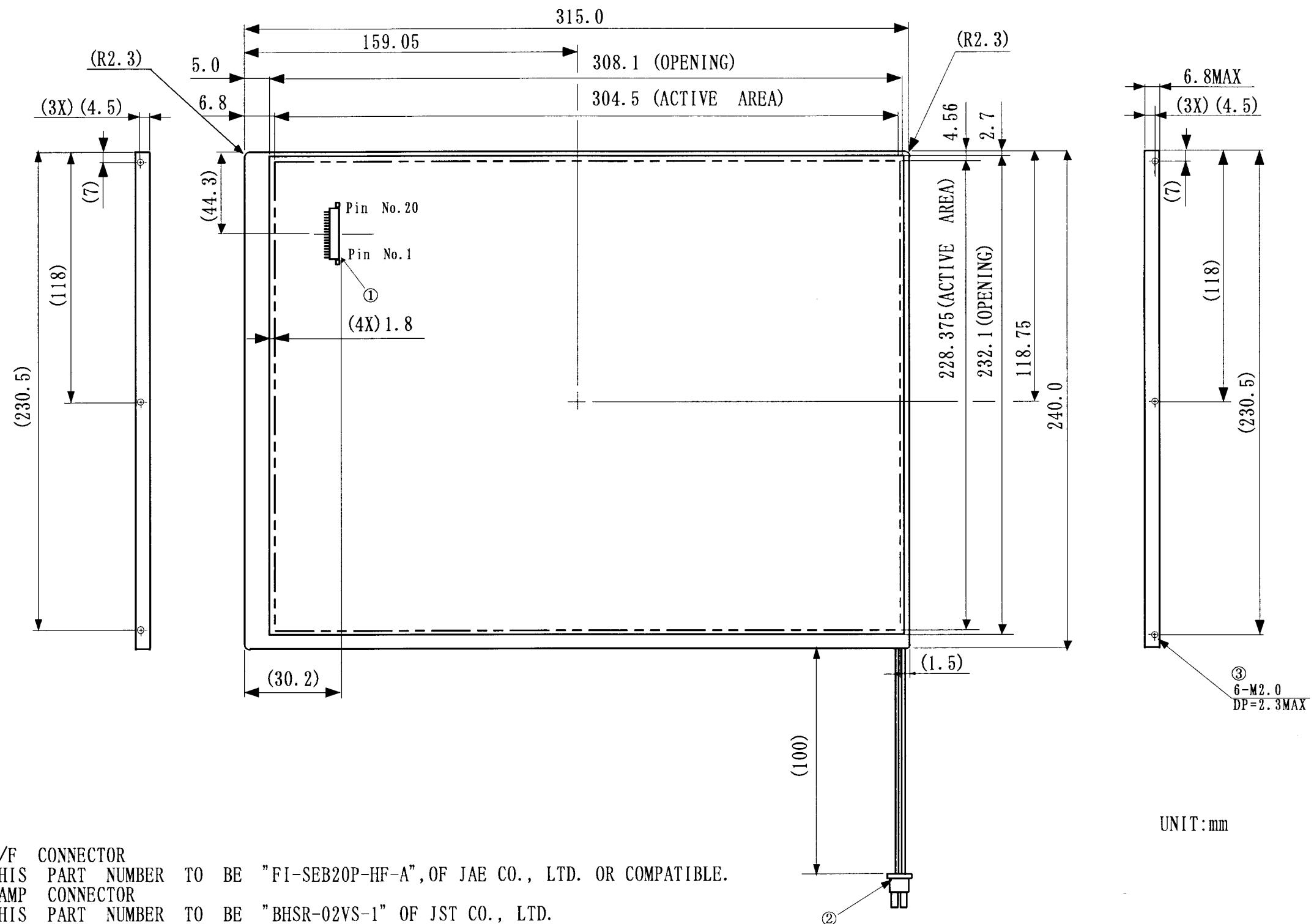
$0 \leq t_7 \leq 20\text{ms}$

$0.4\text{s} \leq t_8$

NOTE(1) All input are in the High impedance state during t_2 .

(2) t_3 is needed for the signal transition between input High impedance state and valid state specified at 6(1) & (2).

7. DIMENSIONAL OUTLINE



NOTES

- ① I/F CONNECTOR
THIS PART NUMBER TO BE "FI-SEB20P-HF-A", OF JAE CO., LTD. OR COMPATIBLE.
- ② LAMP CONNECTOR
THIS PART NUMBER TO BE "BHSR-02VS-1" OF JST CO., LTD.
- ③ THESE HOLES TO BE USED FOR MOUNTING LCD MODULE IN THE SYSTEM ENCLOSURE.
MAXIMUM TORQUE FOR THE SCREW IN MOUNTING PANEL : 0.245N·m (2.5kgf·cm)
MAXIMUM PULL FOR THE SCREW IN MOUNTING PANEL : 29.4N (3kgf)
- ④ THE UNSPECIFIED TOLERANCE : $\pm 0.5\text{mm}$

UNIT: mm