HITACHI

Displays, Hitachi, Ltd.

DATE : Nov 22, 2001

TECHNICAL DATA

Product Name : TX43D15VC0CAD

CONTENTS

RECORD OF REVISION

Date	The upper section:Before revision The lower section:After revision Sheet No.	Page	Summary

DESCRIPTION

The following specifications are applied to the following Super-TFT module.

Note : Inverter for back light unit is not built in a module.

Product Name : TX43D15VC0CAD

General Specifications

Effective Display Area	:(H)337.92X(V)270.336	(mm)
Number of Pixels	:(H)1280X(V)1024	(pixels)
Pixel Pitch	:(H)0.264X(V)0.264	(mm)
Color Pixel Arrangement	:R G B Vertical Stripe	
Display Mode	:Transmissive Mode Normally Black Mode	
Top Polarizer Type	:Anti-glare	
Number of Colors	:16,777,216	(colors)
Viewing Angle Range	:Super Wide Version (Horizontal & Vertical : 170°, CR>=10)	
Input Signal	:2-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	:4 pcs. of CCFL	
External Dimensions	:(H)384X(V)306X(t)20	(mm)
Weight	:max.(2100)	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	14.7 (2G)	m/s 2	3)
Shock	-	29.4(3G)	-	980 (100G)	m/s 2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illuminance of LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.

The temperature at the center of rear surface should be less than 60°C on the condition of operating. The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

High temp storage : 60 deg./240hrs, Low temp storage : -20 deg./240hrs. High temp operation at 50 deg. : 240hrs, Low temp operation at 0 deg. : 240hrs.

2) Ta<= 40 °C-------Relative humidity should be less than 95%RH max. Dew is prohibited.

Ta> 40 °C--------Relative humidity should be lower than the moisture of the 95%RH at 40°C.

3) Frequency of the vibration is between 10Hz and 500Hz. (Remove the resonance point)
Sweep time : 20 min, Duration : X, Y, Z each 120 min.

4) Pulse width of the shock is 2 ms (sine wave) .

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	6.5	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	+/-100		V	2),3)
	V_{ESD1}	+/-8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.

2)Discharge Coefficient:200pF-250 ohm, Environmental:25°C-70%RH

3)It is applied to I/F connector pins.

4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	IL	—	7.0	mArms	1)
Input Voltage	VL	—	1800	Vrms	2)

Note 1)The specification shall be applied to each CFL. The specification is defined at ground line.

2)The specification shall be applied at connector pins for a CFL at start-up.

3)The life time of a back-light is min. 50,000 hrs under the condition of IL=6.0mA & Ta=25deg.

2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

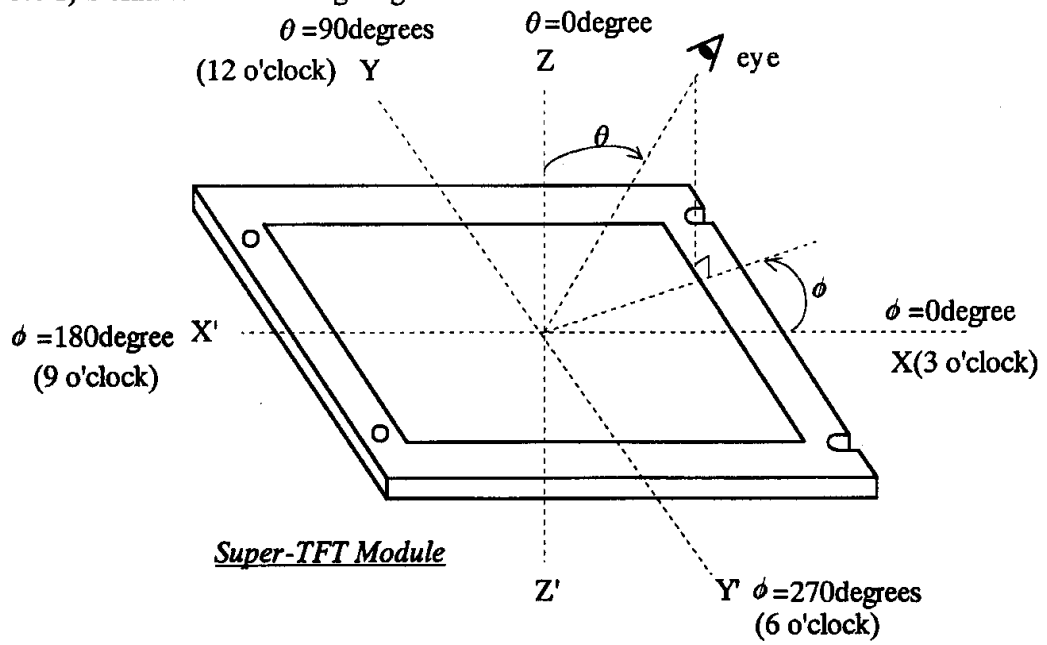
Measuring equipment:Prichard 1980A, or equivalent

Temperature of LCD surface=25°C,VDD=5.0V,fV=60Hz

IL=6.5mA(average of 4pieces of CFLs)

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR	θ =0deg. 1)	250	400	-	-	2)
Response Time	Rise	ton		-	15	30	ms	3)
	Fall	toff		-	15	30	ms	3)
Brightness of white		Bwh		170	200	-	cd/m2	
Brightness uniformity		Buni		-	-	20	%	4)
Color Chromaticity (CIE)	Red	x		0.615	0.64	0.665	-	
		y		0.315	0.34	0.365		
	Green	x		0.275	0.30	0.325		
		y		0.595	0.62	0.645		
	Blue	x		0.125	0.15	0.175		
		y		0.045	0.07	0.095		
	White	x		0.285	0.31	0.335		
		y		0.305	0.33	0.355		
Variation of color		Δx, Δy		-	-	0.02	-	Same color at θ =0° Measuring points : Note 4)
Variation of Color Position (CIE)	Red	Δx	θ =+50deg. φ =0deg, 90deg, 180deg, 270deg. 1)	-	-	0.04	-	5) [Gray scale =255]
		Δy		-	-	0.04		
	Green	Δx		-	-	0.04		
		Δy		-	-	0.04		
	Blue	Δx		-	-	0.04		
		Δy		-	-	0.04		
	White	Δx		-	-	0.04		
		Δy		-	-	0.04		
Contrast Ratio at 80 deg.		CR80 deg.		10	-	-	-	
Cross talk		CT1		-	-	TBD	%	6)
		CT2		-	-	TBD	%	7)

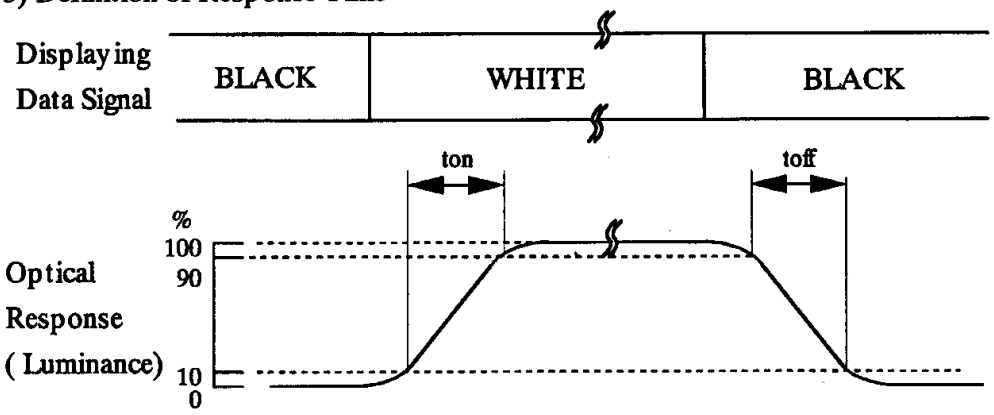
Note 1) Definition of Viewing Angle



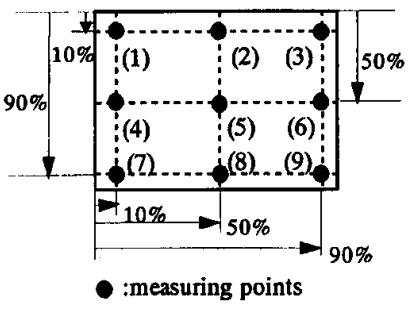
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level) and gray scale. The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{|\,Bmax \text{ or } Bmin - Bave\,|}{Bave} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

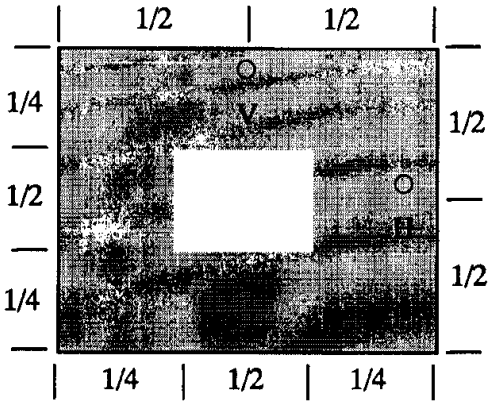
$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9}(B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at θ=0degree and at θ =50degrees & ϕ =0degree, 90degrees, 180degrees, 270degrees.

6) Cross talk 1 shall be measured at V and H position.

$$\text{Cross talk Ratio(CT1)} = 100\times \frac{|\text{Brightness at pattern A} - \text{Brightness at pattern B}|}{\text{Brightness at pattern A}}$$

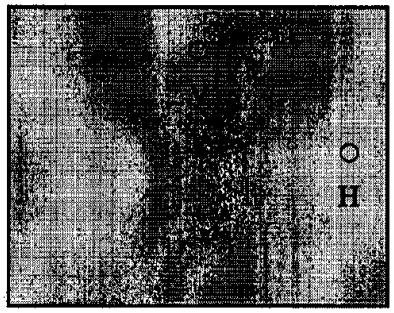
(Background : 128-gray)
Pattern A



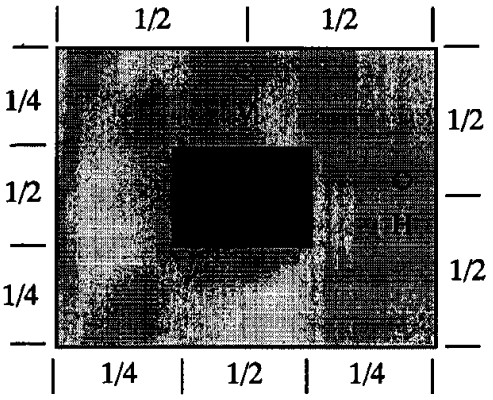
(Background : 128-gray, Window : 255-gray)
Pattern B

7) Cross talk 2 shall be measured at V and H position.

$$\text{Cross talk Ratio(CT2)} = 100\times \frac{|\text{Brightness at pattern C} - \text{Brightness at pattern D}|}{\text{Brightness at pattern C}}$$



(Background : 183-gray)
Pattern C



(Background : 183-gray, Window : 0-gray)
Pattern D

Cross talk (CT2) is guaranteed by cheak of cross talk (CT1).

Displays, Hitachi, Ltd.	Date	Nov.22,2001	Sheet No.	3284PS 2605-TX43D15VC0CAD-1	Page	5-3/3

3. ELECTRICAL CHARACTERISTICS

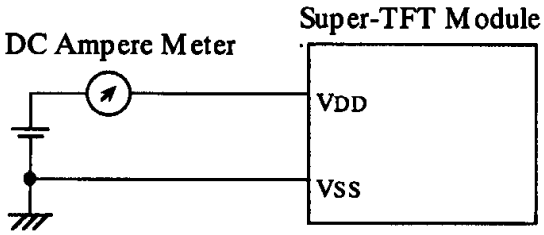
3.1 TFT-LCD Module

Ta=25°C, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	4.5	5	5.5	V	
Power Supply Current	IDD	-	-	(1.0)	A	1),2),3)
Vsync Frequency	fv	-	-	60	Hz	
Hsync Frequency	fH	-	-	64	kHz	
DCLK Frequency	fCLK	40	54	54	MHz	
Input Signals	VI	-	-	-	V	4)

Dimensions in parentheses are reference value.

Note 1) DC current at fv=60Hz, fCLK=54MHz and VDD=5.0V



2) Current fuse(2.0A) is built in a module.
Current capacity of power supply for VDD should be larger than 5A, so that the fuse can be opened at the trouble of power supply.

3) The picture on maximum current is white picture.

4) Characteristics of input signals are shown in LVDS data sheets. (Receiver:THC63LVDF84A)

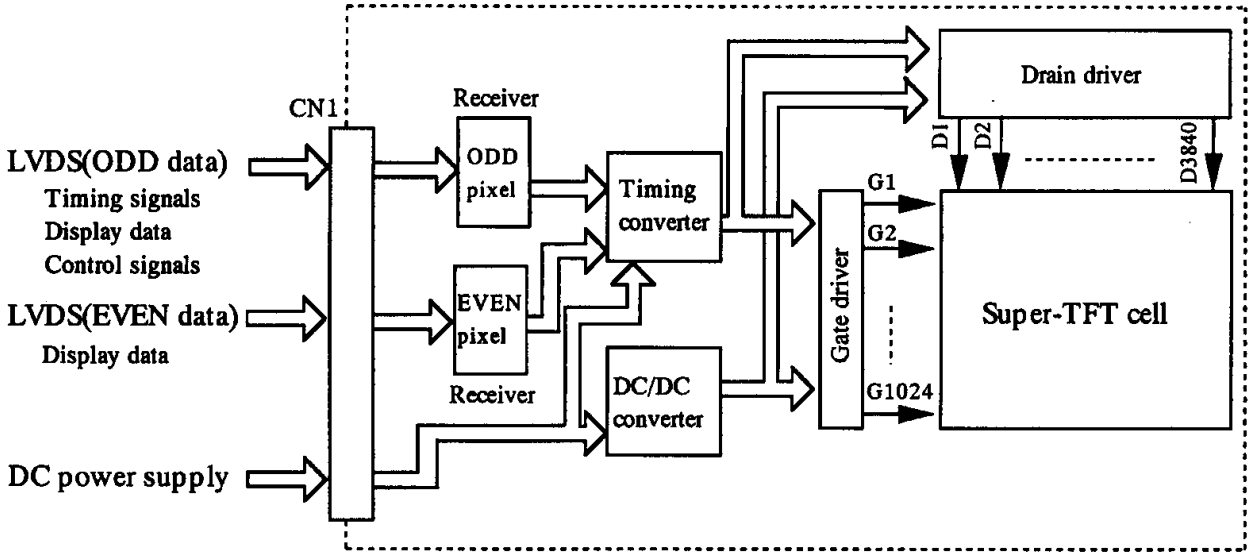
3.2 Back Light

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Input Current	IL	6.0	6.5	7.0	mArms	
Input Voltage	VL	-	700	740	Vrms	
Frequency	f0	40	56	80	kHz	1)
Kick-Off Voltage	Vs	1500	-	1750	V	Ta=0deg

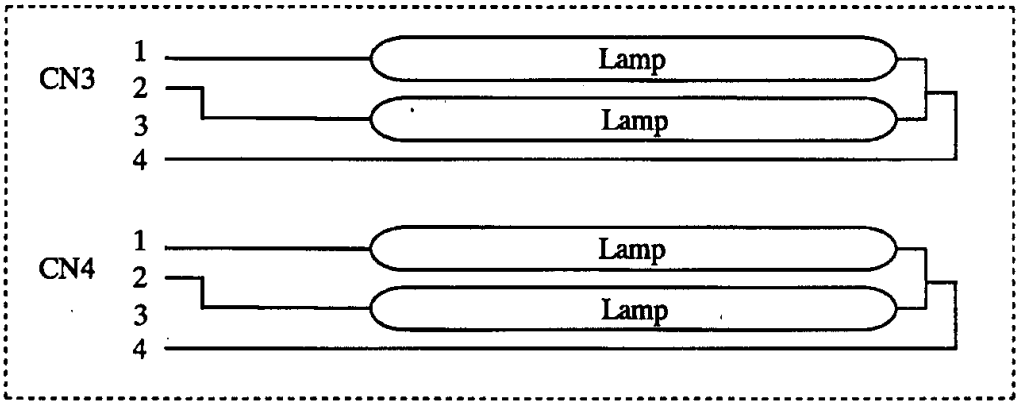
Notes 1) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



Displays, Hitachi, Ltd.	Date	Nov.22,2001	Sheet No.	3284PS 2607-TX43D15VC0CAD-1	Page	7-1/1

5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD MODULE

CN1 : JAE FI-X30S-HF
(Matching connector : JAE FI-X30H or FI-X30M)

Pin No.	Symbol	Function	
1	RAIN0-	ODD pixel data	2)
2	RAIN0+		
3	RAIN1-	ODD pixel data	2)
4	RAIN1+		
5	RAIN2-	ODD pixel data	2)
6	RAIN2+		
7	Vss	GND (0V)	1)
8	RACLKIN-	ODD pixel clock	2)
9	RACLKIN+		
10	RAIN3-	ODD pixel data	2)
11	RAIN3+		
12	RBIN0-	EVEN pixel data	2)
13	RBIN0+		
14	Vss	GND (0V)	1)
15	RBIN1-	EVEN pixel data	2)
16	RBIN1+		
17	Vss	GND (0V)	1)
18	RBIN2-	EVEN pixel data	2)
19	RBIN2+		
20	RBCLKIN-	EVEN pixel clock	2)
21	RBCLKIN+		
22	RBIN3-	EVEN pixel data	2)
23	RBIN3+		
24	Vss	GND (0V)	1)
25	NC	No connection	3)
26	DE	DE Out	
27	NC	No connection	3)
28	VDD	Power supply (+5V)	4)
29	VDD		
30	VDD		

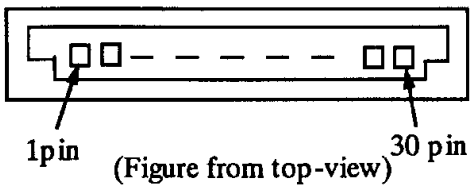
Notes 1) All Vss pins should be grounded.

2) RnINm+ and RnINm- (n=A,B m=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

3) Please keep open.

4) All VDD pins should be connected to +5.0 V(typ.).

5) Pin assignment is as follows.



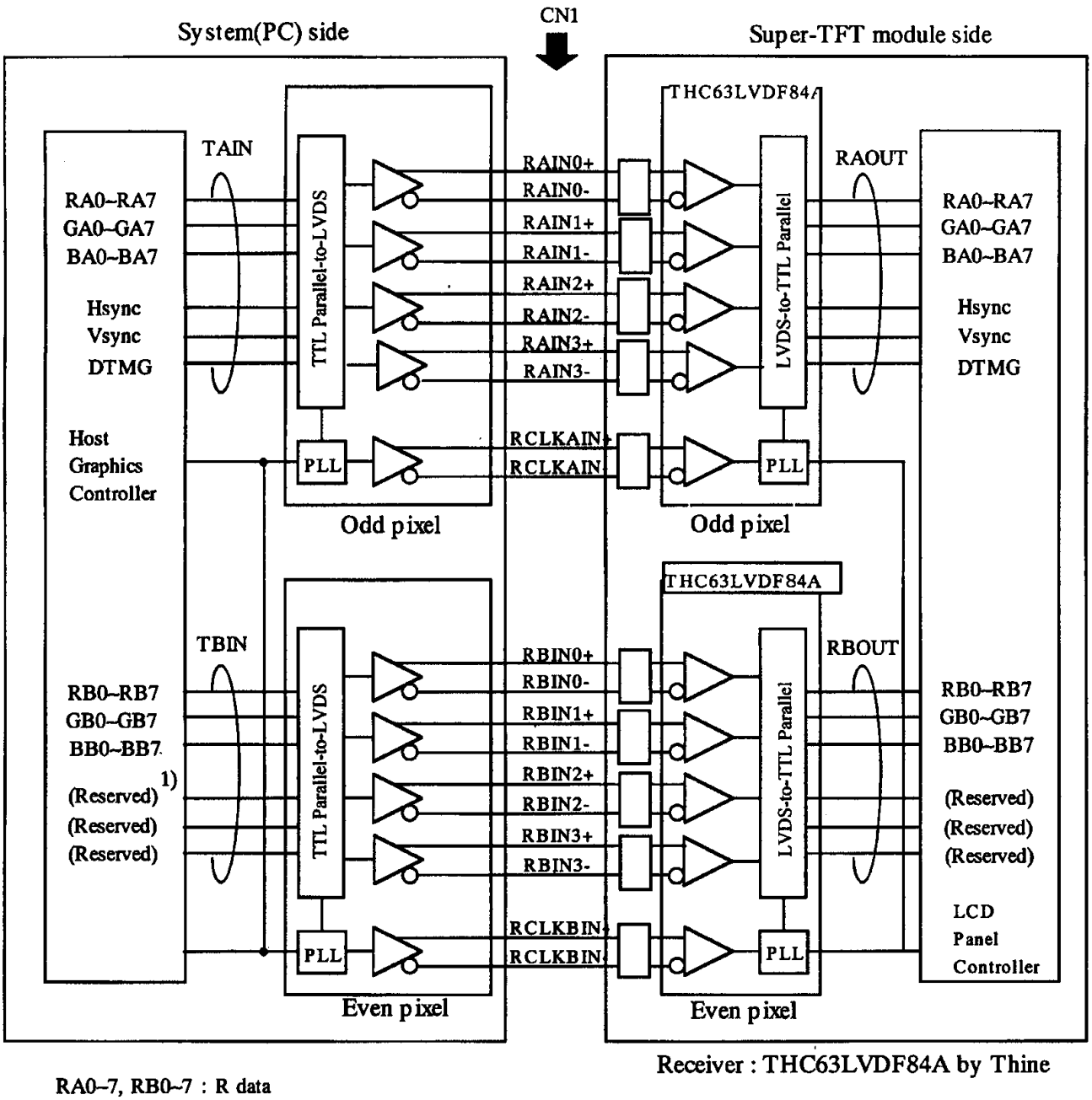
(Figure from top-view)

5. 2 BACK-LIGHT UNIT

CN3、CN4: JST BHR-04VS-1

Pin No.	SYMBOL	Function
1	VL	Power Supply
2	VL	Power Supply
3	NC	
4	GND	GND

BLOCK DIAGRAM OF INTERFACE



RA0–7, RB0–7 : R data
GA0–7, GB0–7 : G data
BA0–7, BB0–7 : B data
Hsync : Horizontal synchronization
Vsync: Vertical synchronization
DTMG : Display timing data

Notes 1) RSVD(reserved) pins on a transmitter should be connected with Vss.

2) The system must have a LVDS transmitter to drive a module.

3) The impedance of LVDS cable should be 50 ohms per a signal line or about 100 ohms per a twist-pair line when it is used differentially.

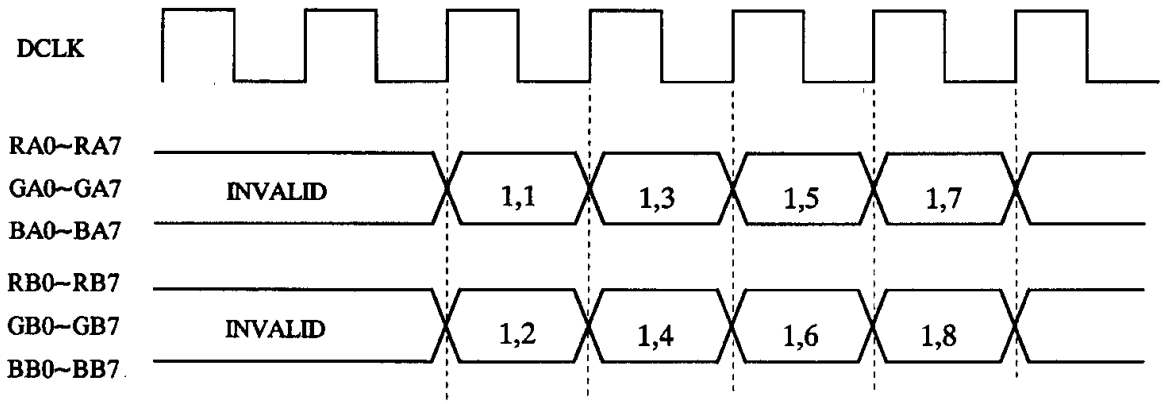
LVDS INTERFACE

	INPUT SIGNAL	Transmitter pin	Transmitter INPUT	Interface connector System side	Interface connector Super-TFT modu	Receiver THC63LVDF84A pin	Receiver THC63LVDF84A OUTPUT	
LVDS Odd	RA0	51	TAIN0	TA OUT0+	RA IN0+	27	RAOUT0	RA0
	RA1	52	TAIN1			29	RAOUT1	RA1
	RA2	54	TAIN2			30	RAOUT2	RA2
	RA3	55	TAIN3			32	RAOUT3	RA3
	RA4	56	TAIN4	TA OUT0-	RA IN0-	33	RAOUT4	RA4
	RA5	3	TAIN6			35	RAOUT6	RA5
	GA0	4	TAIN7			37	RAOUT7	GA0
	GA1	6	TAIN8	TA OUT1+	RA IN1+	38	RAOUT8	GA1
	GA2	7	TAIN9			39	RAOUT9	GA2
	GA3	11	TAIN12			43	RAOUT12	GA3
	GA4	12	TAIN13			45	RAOUT13	GA4
	GA5	14	TAIN14	TA OUT1-	RA IN1-	46	RAOUT14	GA5
	BA0	15	TAIN15			47	RAOUT15	BA0
	BA1	19	TAIN18			51	RAOUT18	BA1
	BA2	20	TAIN19	TA OUT2+	RA IN2+	53	RAOUT19	BA2
	BA3	22	TAIN20			54	RAOUT20	BA3
	BA4	23	TAIN21			55	RAOUT21	BA4
	BA5	24	TAIN22			1	RAOUT22	BA5
	HSYNC	27	TAIN24			3	RAOUT24	HSYNC
	VSYNC	28	TAIN25	TA OUT2-	RA IN2-	5	RAOUT25	VSYNC
	DTMG	30	TAIN26			6	RAOUT26	DTMG
	RA6	50	TAIN27	TA OUT3+	RA IN3+	7	RAOUT27	RA6
	RA7	2	TAIN5			34	RAOUT5	RA7
	GA6	8	TAIN10			41	RAOUT10	GA6
	GA7	10	TAIN11			42	RAOUT11	GA7
	BA6	16	TAIN16			49	RAOUT16	BA6
	BA7	18	TAIN17	TA OUT3-	RA IN3-	50	RAOUT17	BA7
	RSVD 1)	25	TAIN23			2	RAOUT23	RSVD
	DCLK	31	TCLKA IN	TCLKA OUT+ TCLKA OUT-	RCLKA IN+ RCLKA IN-	26	RCLKA OUT	DCLK
LVDS Even	RB0	51	TBIN0	TB OUT0+	RB IN0+	27	RBOUT0	RB0
	RB1	52	TBIN1			29	RBOUT1	RB1
	RB2	54	TBIN2			30	RBOUT2	RB2
	RB3	55	TBIN3			32	RBOUT3	RB3
	RB4	56	TBIN4	TB OUT0-	RB IN0-	33	RBOUT4	RB4
	RB5	3	TBIN6			35	RBOUT6	RB5
	GB0	4	TBIN7			37	RBOUT7	GB0
	GB1	6	TBIN8	TB OUT1+	RB IN1+	38	RBOUT8	GB1
	GB2	7	TBIN9			39	RBOUT9	GB2
	GB3	11	TBIN12			43	RBOUT12	GB3
	GB4	12	TBIN13			45	RBOUT13	GB4
	GB5	14	TBIN14	TB OUT1-	RB IN1-	46	RBOUT14	GB5
	BB0	15	TBIN15			47	RBOUT15	BB0
	BB1	19	TBIN18			51	RBOUT18	BB1
	BB2	20	TBIN19	TB OUT2+	RB IN2+	53	RBOUT19	BB2
	BB3	22	TBIN20			54	RBOUT20	BB3
	BB4	23	TBIN21			55	RBOUT21	BB4
	BB5	24	TBIN22			1	RBOUT22	BB5
	RSVD 1)	27	TBIN24			3	RBOUT24	RSVD
	RSVD 1)	28	TBIN25	TB OUT2-	RB IN2-	5	RBOUT25	RSVD
	RSVD 1)	30	TBIN26			6	RBOUT26	RSVD
	RB6	50	TBIN27	TB OUT3+	RB IN3+	7	RBOUT27	RB6
	RB7	2	TBIN5			34	RBOUT5	RB7
	GB6	8	TBIN10			41	RBOUT10	GB6
	GB7	10	TBIN11			42	RBOUT11	GB7
	BB6	16	TBIN16			49	RBOUT16	BB6
	BB7	18	TBIN17	TB OUT3-	RB IN3-	50	RBOUT17	BB7
	RSVD 1)	25	TBIN23			2	RBOUT23	RSVD
	DCLK	31	TCLKB IN	TCLKB OUT+ TCLKB OUT-	RCLKB IN+ RCLKB IN-	26	RCLKB OUT	DCLK

	(1, 1)			(1, 2)	
RA	GA	BA	RB	GB	BB

Odd pixel : RA0~RA7 : R data
GA0~GA7 : G data
BA0~BA7 : B data
Even pixel : RB0~RB7 : R data
GA0~GA7 : G data
BB0~BB7 : B data

1,1	1,2	1,3	----------	1,1280
2,1	2,2	2,3	----------	2,1280
3,1	3,2	3,3	----------	3,1280
⋮	⋮	⋮		⋮
1024,1	1024,2	1024,3	----------	1024,1280



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color \ Input data		R data								G data								B data							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENDA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

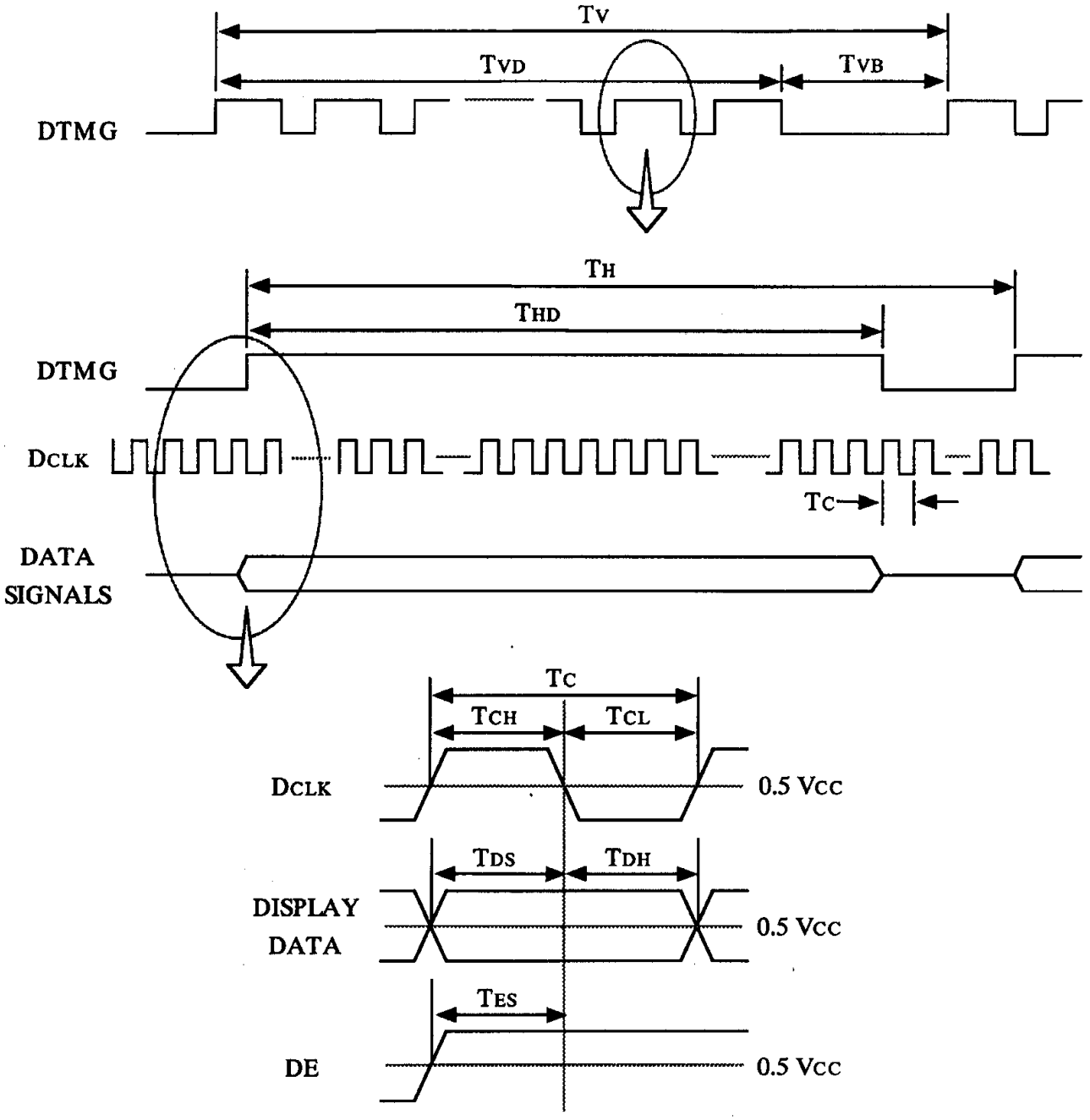
Notes 1) Definition of gray scale : Color (n)

n indicates gray scale level. Higher n means brighter level.

2) Data signals : 1:High, 0:Low

6. TIMING DIAGRAMS OF INTERFACE TIMING

6.1 Timing diagrams of interface signal (DTMG only mode)

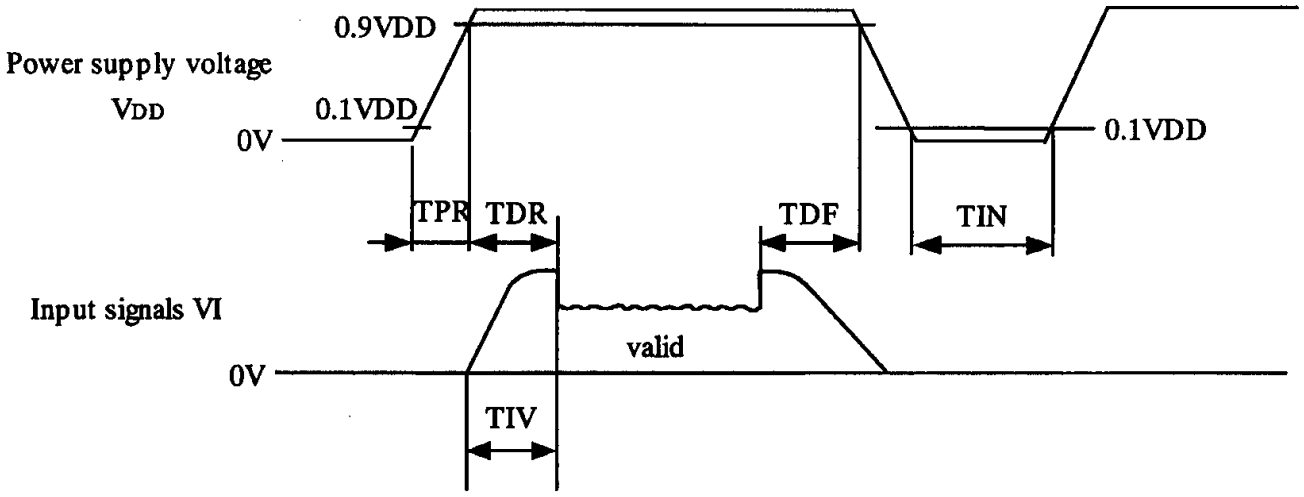


6.2 Timing Parameters (DTMG only mode)

2p xl/clk

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock	Frequency	1/Tc	40	-	54	MHz	
	High Time	Tch	4	-	-	nsec	
	Low Time	Tcl	4	-	-	nsec	
Data	Setup Time	Tds	4	-	-	nsec	
	Hold Time	Tdh	4	-	-	nsec	
Data Enable	Setup Time	Tes	4	-	-	nsec	
Frame Frequency	Cycle	Tv	-	16.7	16.7	msec	
			1032	1066	1066	lines	
Vertical Active Display Term	Display Period	Tvd	1024	1024	1024	lines	
	Vertical Blank Period	Tvb	8	-	-	lines	
One Line Scanning Time	Cycle	Th	672	-	844	clocks	
Horizontal Active Display Term	Display Period	Thd	640	640	640	clocks	

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

0ms ≤TPR ≤ 10ms

0ms ≤ TDR ≤ 50ms

0ms ≤TDF ≤50ms

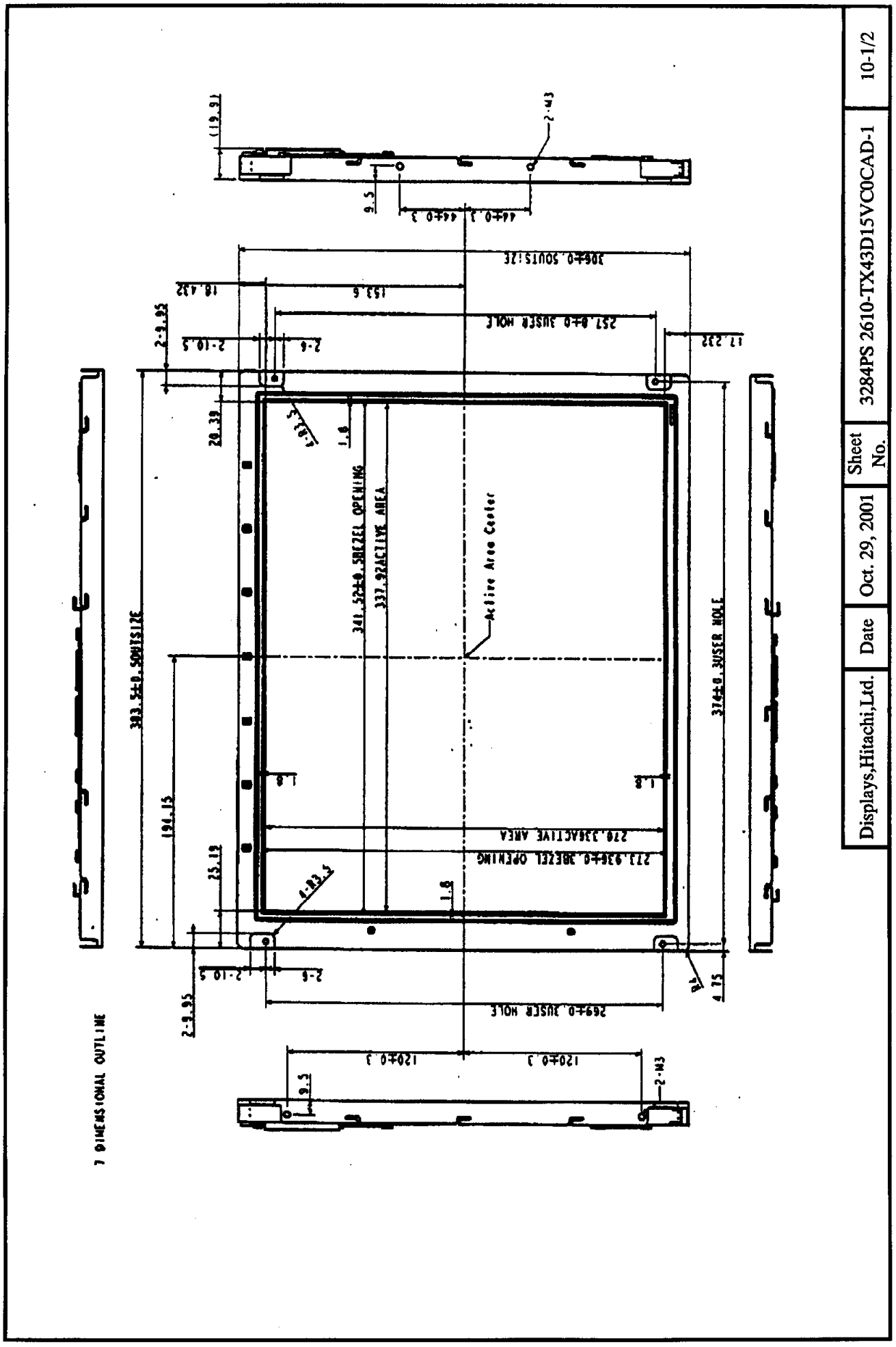
TIN ≥ 1s

TIV ≤ 3ms

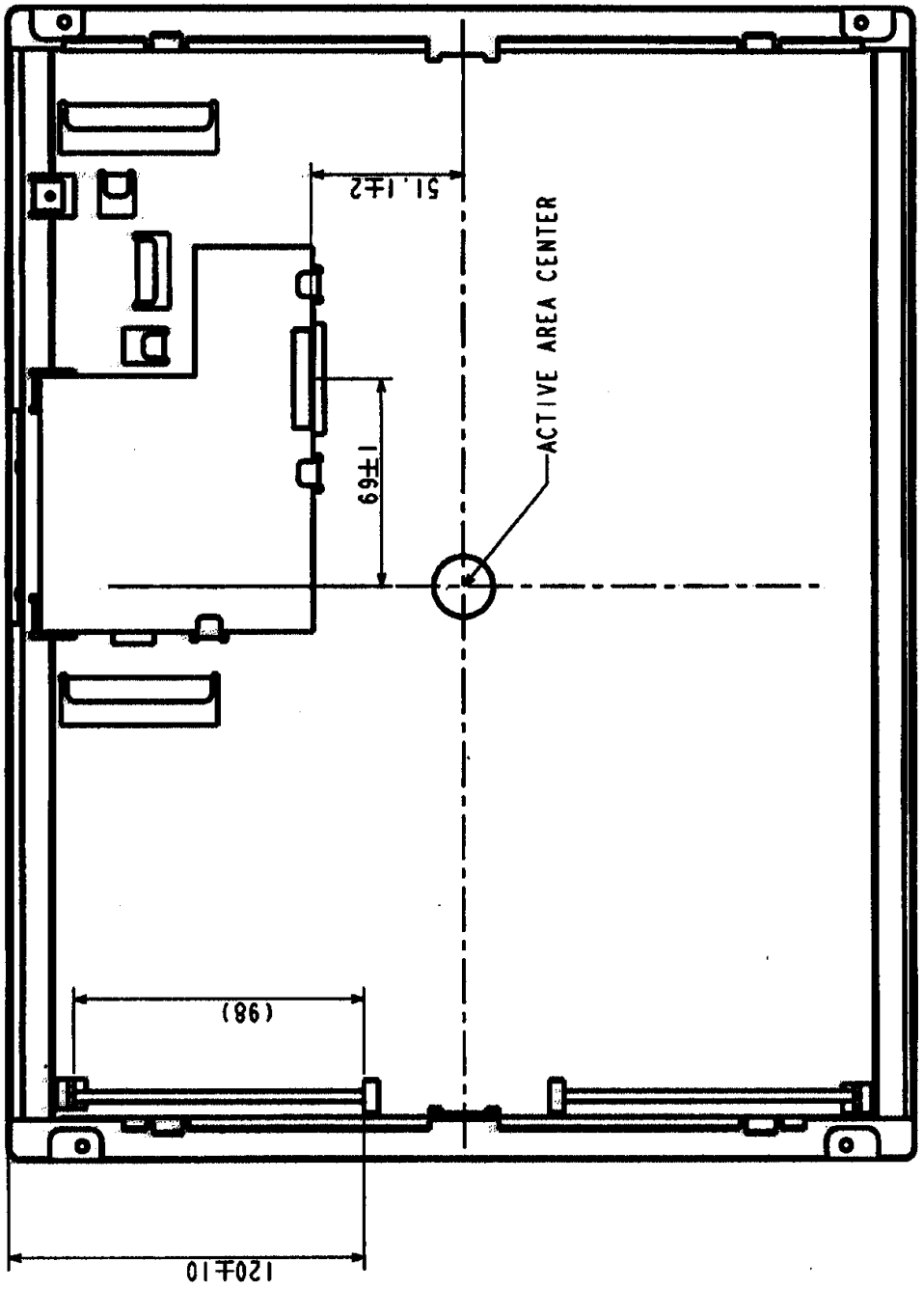
Notes 1) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.

2) T4 should be measured after the module has been fully discharged between power off and on period.

3) Interface signal shall not be kept at high impedance when the power is on.



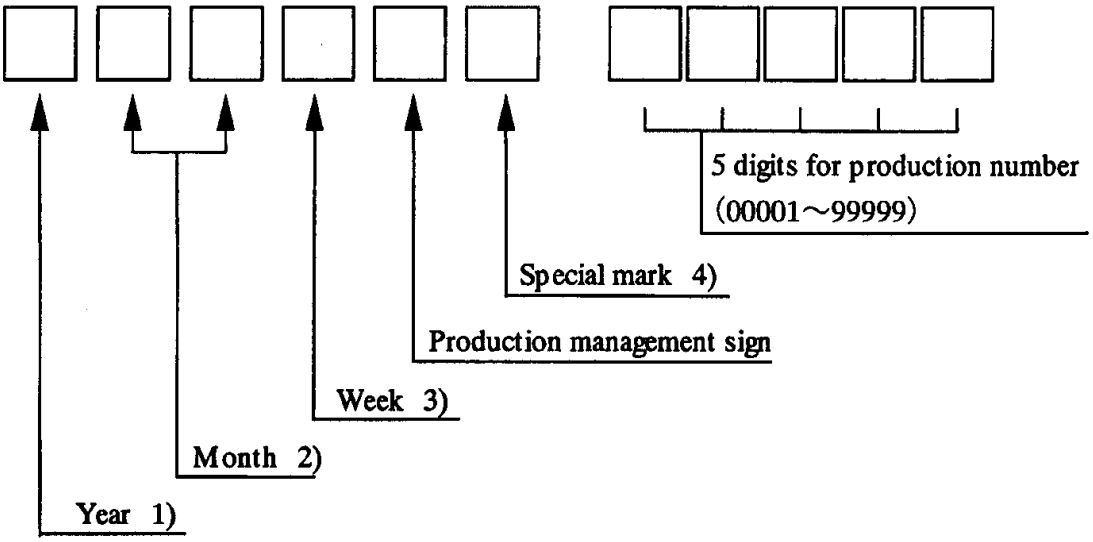
Displays,Hitachi,Ltd.	Date	Oct. 29, 2001	Sheet No.	3284PS 2610-TX43D15VC0CAD-1	10-1/2



Displays,Hitachi,Ltd.	Date	Oct. 29, 2001	Sheet No.	3284PS 2610-TX43D15VC0CAD-1	10-2/2

8. DESIGNATION OF LOT MARK

8.1 LOT MARK



Notes

1)

Year	Mark
2001	1
2002	2
2003	3
2004	4

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Day)	Mark
1～7	1
8～14	2
15～21	3
22～28	4
29～31	5

4) It is the mark that was opened up by production person to take correspondence with production number.

8.2 Revision (REV.) control

REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

8.3 Location of lot mark

Lot mark is printed on a label. The label is on the metallic bezel as shown in 7. External Dimensional. The style of character will be changed without notice.