TENTAIVE

HITACHI

Hitachi Displays, Ltd.

DATE : Apr. 26, 2007

TECHNICAL DATA

TX54D13VC0CAA

CONTENTS

The information described in this technical specification is tentative and it is possible to be changed without prior notice.

RECORD OF REVISION

Date	The upper section : Before revision The lower section : After revision Sheet No.	Page	Summary

APPLICATION

In the case of applying this product for such as control and safey device of transportation facilities (airplane, train, automobile, ship, etc), equipments aiming for rescue and security, and the other safety related devices which should secure higher reliability and safety, please make it sure that proper countermeasure such as fail-safe functions and enough system design for the protection are mandatory.

Please do not apply this product for equipments or devices which need exceedingly high reliability, such as aerospace applications, telecommunication facilities (trunk lines), nuclear related equipments or plants, and critical life support devices or applications. Usage style of this product is limited to Landscape mode. Optical characteristics mentioned in this spec. sheet is applied for only initial stage after delivery, and the characteristics will be changed by long time usage. Reliability of this product is secured as normal office use.

DESCRIPTION

The following specifications are applied to the following Super-TFT module.

Note : Inverter for back light unit is not built in this module.

Product Name : TX54D13VC0CAA

General Specifications

Effective Display Area	: (H)432.0×(V)324.0	(mm)
Number of Pixels	: (H)1,600×(V)1,200	(pixels)
Pixel Pitch	: (H)0.270×(V)0.270	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-glare	
Number of Colors	: 16,777,216 colors	
Viewing Angle Range	: Super Wide Version	
Input Signal	: 2-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 6 pcs. of CCFL	
External Dimensions	: (H)460.6×(V)362×(t)25	(mm)
Weight	: Max. 4,000 (g)	(Typ. 3,450 (g))

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	14.7 (1.5G)	m/s^2	3)
Shock	-	29.4(3G)	-	294 (30G)	m/s^2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the center glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 60℃ on the condition of operating.
Function of module is guaranteed in above operating temperature range, but optical characteristics is specified for only 25℃ operating condition.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≤40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta> 40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	13.5	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient：200pF-250Ω, Environmental：25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	IL	—	7.0	mArms	1)
Input Voltage	VL	—	1800	Vrms	2)

Note 1)The specification shall be applied to each CFL. The specification is defined at ground line.
2)The specification shall be applied at connector pins for a CFL at start-up.

2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

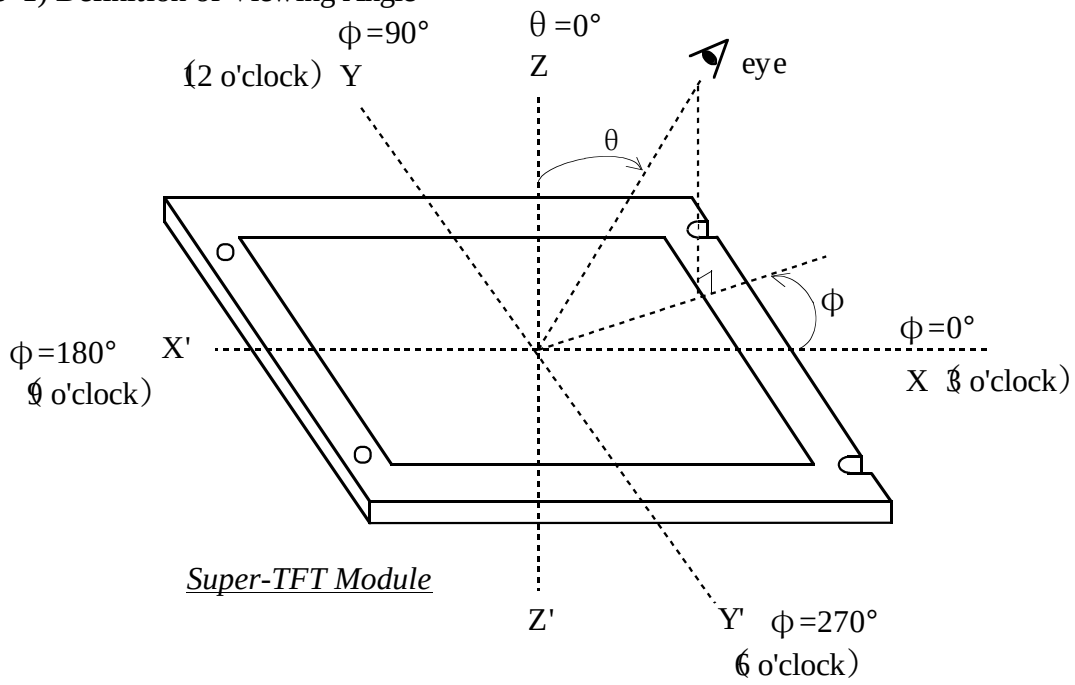
Measuring equipment :Pritchard 1980A, or equivalent [N.I.S.T (Standard Source A)]

Temperature of LCD surface＝25℃,、VDD＝12.0V、f V＝60Hz、

IL=6.5mA (average of 6 pieces of CFLs)

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR	θ＝0° 1)	600	900	-	-	2)
Response Time	Rise	ton		-	(11)	TBD	ms	3)
	Fall	toff		-	(14)	TBD	ms	3)
Brightness of white		Bwh		240	300	-	cd/m 2	
Brightness uniformity		Buni		-	-	33	%	4)
Color Chromaticity (CIE)	Red	χ		0.61	0.64	0.67	-	[Gray scale =255]
		y		0.30	0.33	0.36		
	Green	χ		0.26	0.29	0.32		
		y		0.57	0.60	0.63		
	Blue	χ		0.12	0.15	0.18		
		y		0.03	0.06	0.09		
	White	χ		0.28	0.31	0.34		
		y		0.30	0.33	0.36		
Variation of Color Position (CIE)	Red	Δ χ	θ =+50° φ=0°,90° 180°,270° 1)	-	-	0.04	-	5) [Gray scale =255]
		Δ y		-	-	0.04		
	Green	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	Blue	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	White	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
Contrast Ratio at 85°		CR85°	θ =85° φ=0°,90° 180°,270° 1)	10	-	-	-	

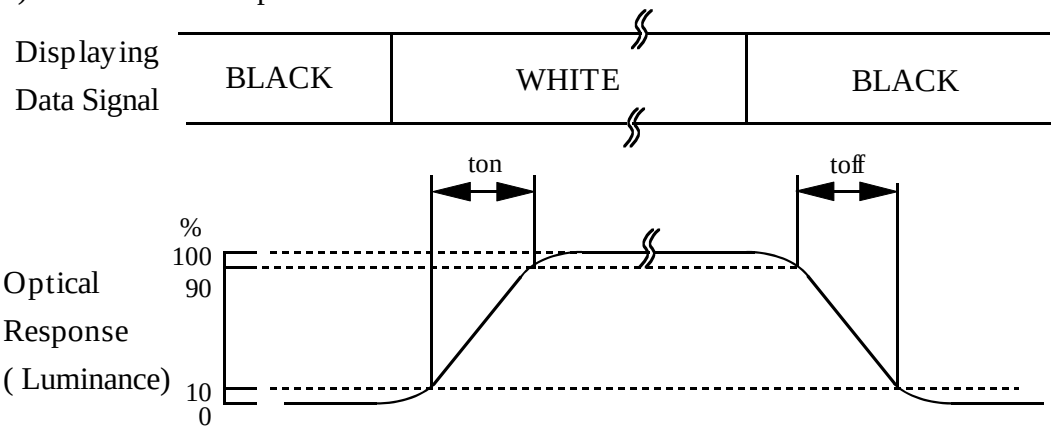
Note 1) Definition of Viewing Angle



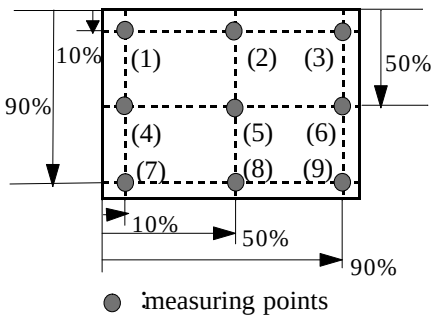
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \left(\frac{Bmax}{Bmin} \right)^{-1} \times 100$$

where, Bmax = Maximum brightness
Bmin = Minimum brightness

5) Variation of color position on CIE is defined as difference between colors at θ =0 ° and at θ =50°& ϕ=0°,90°,180°,270°.

3. ELECTRICAL CHARACTERISTICS

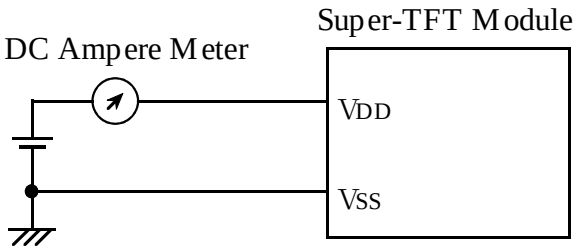
3.1 TFT-LCD Module

Ta=25°C, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	11.0	12.0	13.0	V	
Power Supply Current	I_{DD}	—	TBD	TBD	A	1),2),3)
Vsync Frequency	f_V	57	60	63	Hz	
Hsync Frequency	f_H	—	72	(75)	kHz	
DCLK Frequency	f_{CLK}	40	67.5	(81)	MHz	

Dimensions in parentheses are reference value.

Note 1) DC current at fv=60Hz, fCLK=67.5MHz and VDD=12V



2) Current capacity of power supply for VDD should be larger than 5A, so that the fuse can be opened at the trouble of power supply.

3) The picture on maximum current is white picture.

3.2 Back Light

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Input Current	IL	3.0	6.5	7.0	mArms	1)
Input Voltage	VL	-	800	-	Vrms	
Frequency	f0	40	54	65	kHz	2)
Kick-Off Voltage	Vs	1500	-	1750	V	3)

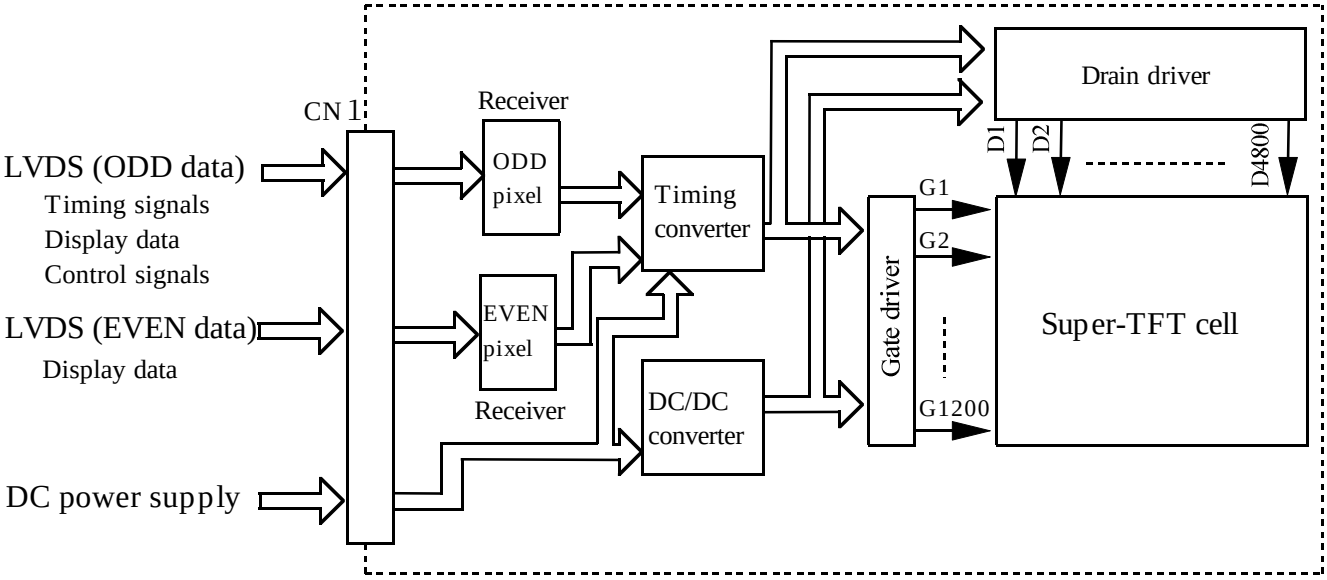
Notes 1) The specification shall be applied to each CFL. The specification is defined at ground line.

2) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.

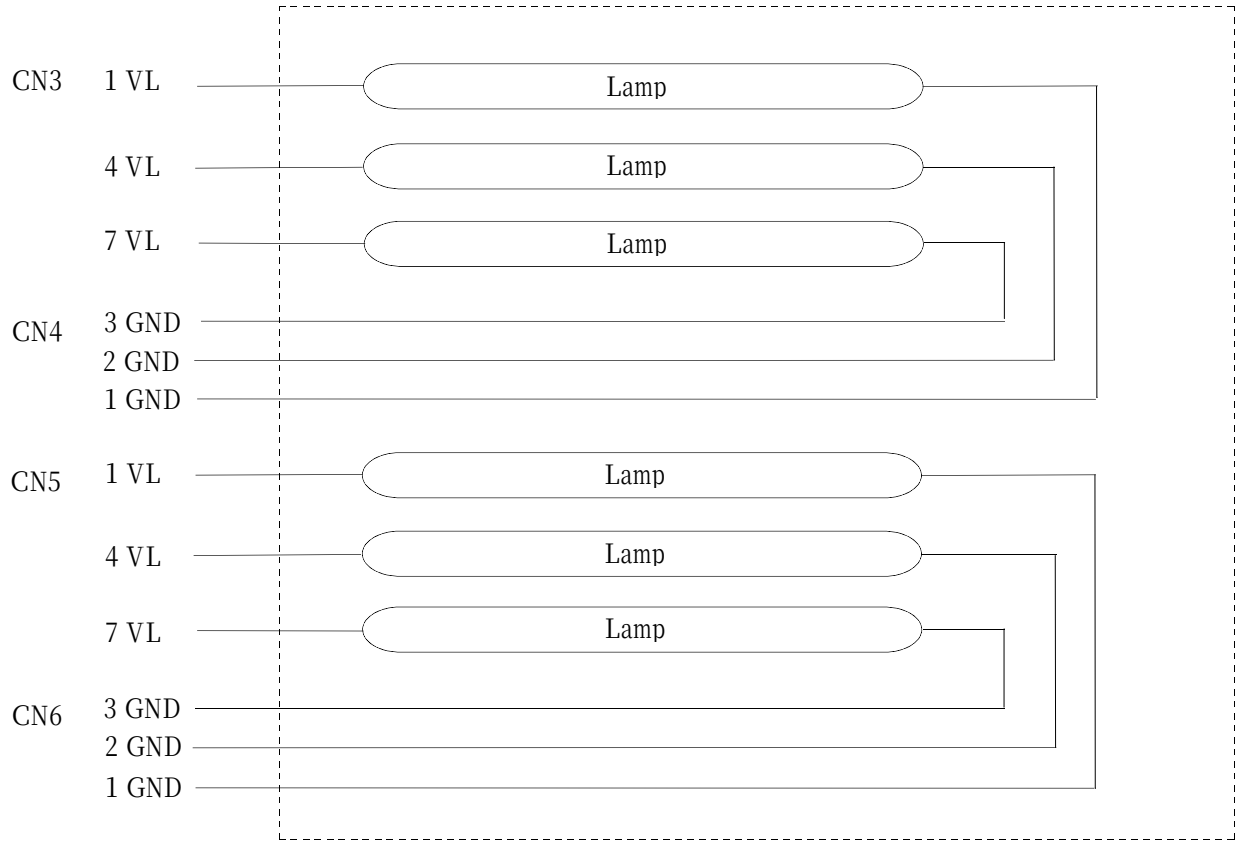
3) Ta = 0°C

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD MODULE

CN1 : JAE FI-X30S-HF
(Matching connector : JAE FI-X30H or FI-X30M)

Pin No.	Symbol	Function	
1	RAIN0-	ODD pixel data	2)
2	RAIN0+		
3	RAIN1-	ODD pixel data	2)
4	RAIN1+		
5	RAIN2-	ODD pixel data	2)
6	RAIN2+		
7	Vss	GND (0V)	1)
8	RACLKIN-	ODD pixel clock	2)
9	RACLKIN+		
10	RAIN3-	ODD pixel data	2)
11	RAIN3+		
12	RBIN0-	EVEN pixel data	2)
13	RBIN0+		
14	Vss	GND (0V)	1)
15	RBIN1-	EVEN pixel data	2)
16	RBIN1+		
17	Vss	GND (0V)	1)
18	RBIN2-	EVEN pixel data	2)
19	RBIN2+		
20	RBCLKIN-	EVEN pixel clock	2)
21	RBCLKIN+		
22	RBIN3-	EVEN pixel data	2)
23	RBIN3+		
24	Vss	GND (0V)	1)
25	NC	No connection	3)
26	DE	No connection	3)
27	NC	No connection	3)
28	VDD	Power supply (12V)	4)
29	VDD		
30	VDD		

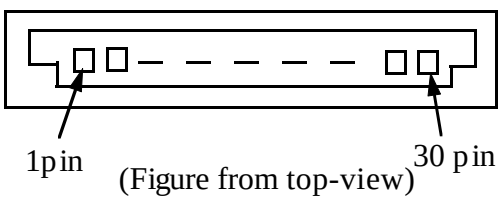
Notes 1) All Vss pins should be grounded.

2) RnINm+ and RnINm- (n=A,B m=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

3) Please keep open.

4) All VDD pins should be connected to +12.0 V(typ.).

5) Pin assignment is as follows.



(Figure from top-view)

5. 2 BACK-LIGHT UNIT

CN3,CN5 : JST XHP-7

(Matching connector : S7B-HX-A, JST B7B-XH-A or B7B-XH-2

Pin No.	SYMBOL	Function
1	V_L	Power Supply
2	NC	No connection
3	NC	No connection
4	V_L	Power Supply
5	NC	No connection
6	NC	No connection
7	V_L	Power Supply

CN4,CN6 : JST BHR-03VS-1

(Matching connector: SM03(4.0)B-BHS-1-TB)

Pin No.	SYMBOL	Function
1	GND	GND
2	GND	GND
3	GND	GND

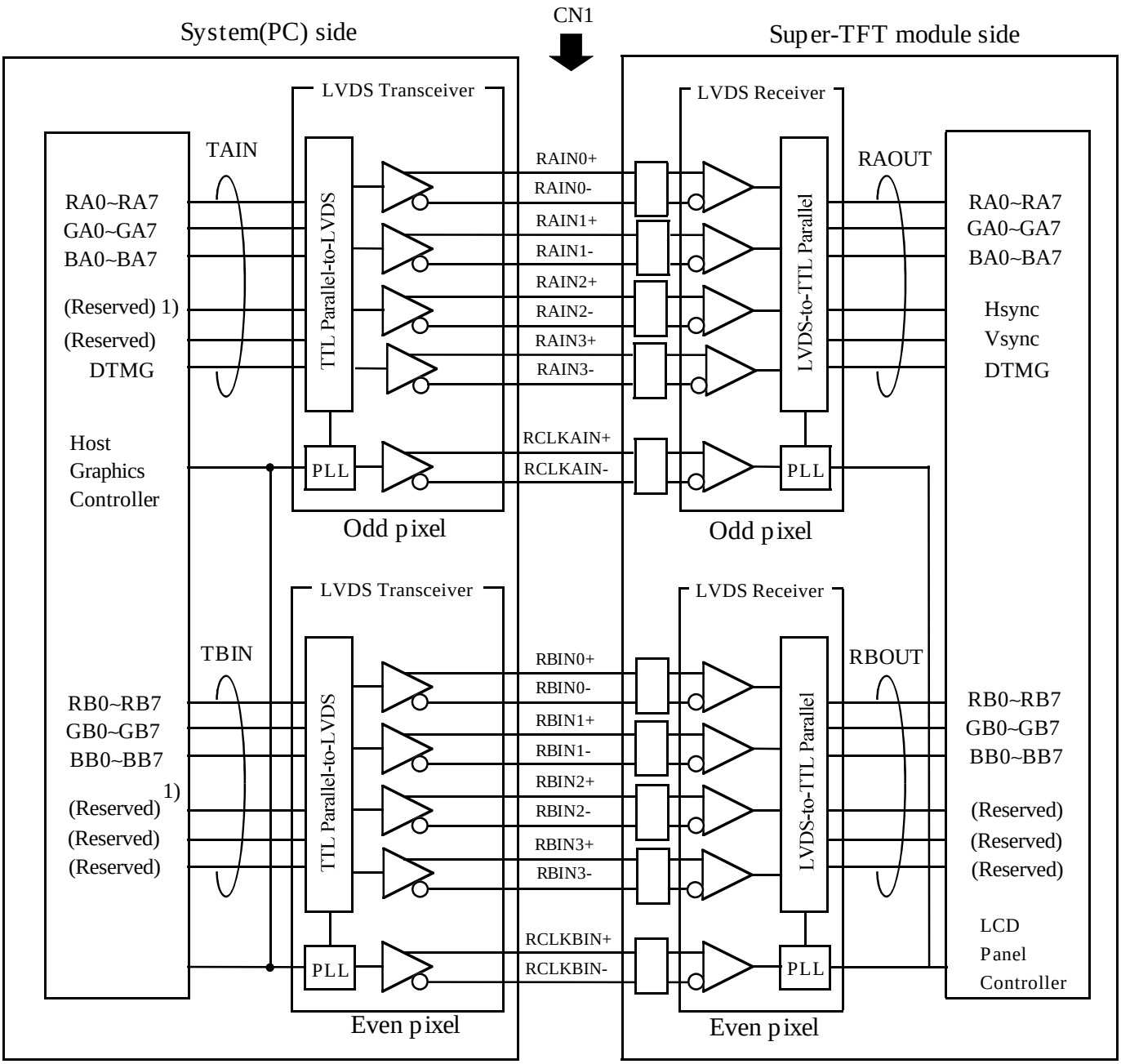
Notes 1) There are parasitic capacitors between 3CCFLs.The different capacitance of these parasitic capacitors send the one-sided electric current to the specific CCFL. this phenomenon causes the drop of the optical characteristics.

To avoid this phenomenon, The inverter driving CCFLs should be applied as follows;

(1) One transformer should cover to supply VL and IL for only one CCFL.

(2) Providing detector to monitor IL current level for every each CCFL is recommended, but monitoring of only maximum current level among the 3CCFLs is also acceptable if the recommendation is not easily implemented at design of a inverter.

BLOCK DIAGRAM OF INTERFACE



Receiver : Equivalent of THC63LVDF84B by Thine

RA0~7, RB0~7 : R data
GA0~7, GB0~7 : G data
BA0~7, BB0~7 : B data
DTMG : Display timing data

Notes 1) RSVD(reserved) pins on a transmitter should be connected with Vss.

2) The system must have a LVDS transmitter to drive a module.

3) The impedance of LVDS cable should be 50 ohms per a signal line or about 100 ohms per a twist-pair line when it is used differentially.

LVDS INTERFACE

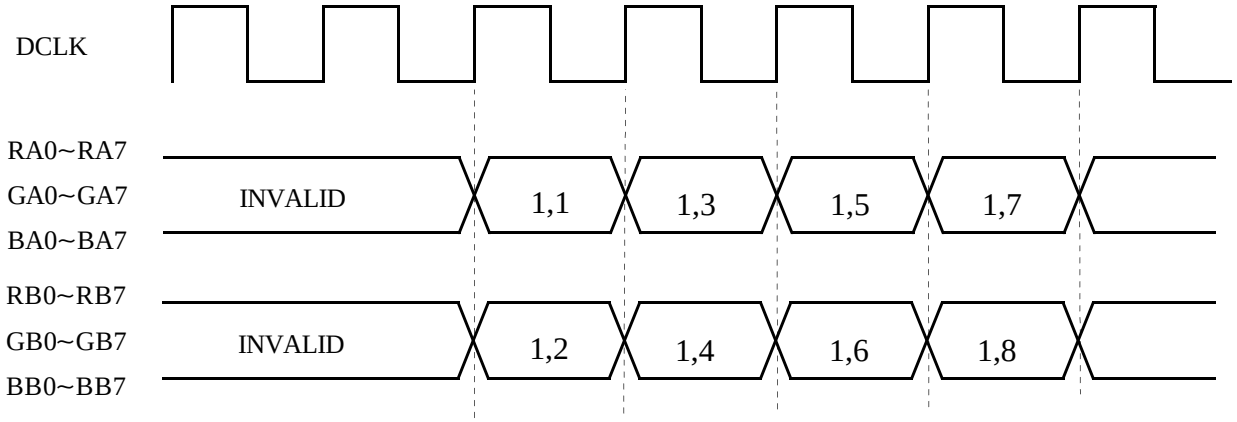
	INPUT SIGNAL	Transmitter		Interface connector		Receiver		TFT control input
		pin	INPUT	System side	Super-TFT module	pin	OUTPUT	
LVDS Odd	RA0	51	TAIN0	TA OUT0+	RA IN0+	27	RAOUT0	RA0
	RA1	52	TAIN1			29	RAOUT1	RA1
	RA2	54	TAIN2			30	RAOUT2	RA2
	RA3	55	TAIN3			32	RAOUT3	RA3
	RA4	56	TAIN4	TA OUT0-	RA IN0-	33	RAOUT4	RA4
	RA5	3	TAIN6			35	RAOUT6	RA5
	GA0	4	TAIN7			37	RAOUT7	GA0
	GA1	6	TAIN8	TA OUT1+	RA IN1+	38	RAOUT8	GA1
	GA2	7	TAIN9			39	RAOUT9	GA2
	GA3	11	TAIN12			43	RAOUT12	GA3
	GA4	12	TAIN13			45	RAOUT13	GA4
	GA5	14	TAIN14	TA OUT1-	RA IN1-	46	RAOUT14	GA5
	BA0	15	TAIN15			47	RAOUT15	BA0
	BA1	19	TAIN18			51	RAOUT18	BA1
	BA2	20	TAIN19	TA OUT2+	RA IN2+	53	RAOUT19	BA2
	BA3	22	TAIN20			54	RAOUT20	BA3
	BA4	23	TAIN21			55	RAOUT21	BA4
	BA5	24	TAIN22			1	RAOUT22	BA5
	RSVD 1)	27	TAIN24			3	RAOUT24	RSVD
	RSVD 1)	28	TAIN25	TA OUT2-	RA IN2-	5	RAOUT25	RSVD
	DTMG	30	TAIN26			6	RAOUT26	DTMG
	RA6	50	TAIN27	TA OUT3+	RA IN3+	7	RAOUT27	RA6
	RA7	2	TAIN5			34	RAOUT5	RA7
	GA6	8	TAIN10			41	RAOUT10	GA6
	GA7	10	TAIN11			42	RAOUT11	GA7
	BA6	16	TAIN16			49	RAOUT16	BA6
	BA7	18	TAIN17	TA OUT3-	RA IN3-	50	RAOUT17	BA7
	RSVD 1)	25	TAIN23			2	RAOUT23	RSVD
	DCLK	31	TCLKA IN	TCLKA OUT+ TCLKA OUT-	RCLKA IN+ RCLKA IN-	26	RCLKA OUT	DCLK
LVDS Even	RB0	51	TBIN0	TB OUT0+	RB IN0+	27	RBOUT0	RB0
	RB1	52	TBIN1			29	RBOUT1	RB1
	RB2	54	TBIN2			30	RBOUT2	RB2
	RB3	55	TBIN3			32	RBOUT3	RB3
	RB4	56	TBIN4	TB OUT0-	RB IN0-	33	RBOUT4	RB4
	RB5	3	TBIN6			35	RBOUT6	RB5
	GB0	4	TBIN7			37	RBOUT7	GB0
	GB1	6	TBIN8	TB OUT1+	RB IN1+	38	RBOUT8	GB1
	GB2	7	TBIN9			39	RBOUT9	GB2
	GB3	11	TBIN12			43	RBOUT12	GB3
	GB4	12	TBIN13			45	RBOUT13	GB4
	GB5	14	TBIN14	TB OUT1-	RB IN1-	46	RBOUT14	GB5
	BB0	15	TBIN15			47	RBOUT15	BB0
	BB1	19	TBIN18			51	RBOUT18	BB1
	BB2	20	TBIN19	TB OUT2+	RB IN2+	53	RBOUT19	BB2
	BB3	22	TBIN20			54	RBOUT20	BB3
	BB4	23	TBIN21			55	RBOUT21	BB4
	BB5	24	TBIN22			1	RBOUT22	BB5
	RSVD 1)	27	TBIN24			3	RBOUT24	RSVD
	RSVD 1)	28	TBIN25	TB OUT2-	RB IN2-	5	RBOUT25	RSVD
	RSVD 1)	30	TBIN26			6	RBOUT26	RSVD
	RB6	50	TBIN27	TB OUT3+	RB IN3+	7	RBOUT27	RB6
	RB7	2	TBIN5			34	RBOUT5	RB7
	GB6	8	TBIN10			41	RBOUT10	GB6
	GB7	10	TBIN11			42	RBOUT11	GB7
	BB6	16	TBIN16			49	RBOUT16	BB6
	BB7	18	TBIN17	TB OUT3-	RB IN3-	50	RBOUT17	BB7
	RSVD 1)	25	TBIN23			2	RBOUT23	RSVD
	DCLK	31	TCLKB IN	TCLKB OUT+ TCLKB OUT-	RCLKB IN+ RCLKB IN-	26	RCLKB OUT	DCLK

CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

	(1, 1)			(1, 2)	
RA	**GA**	**BA**	**RB**	**GB**	**BB**

Odd pixel : RA0~RA7 : R data
GA0~GA7 : G data
BA0~BA7 : B data
Even pixel : RB0~RB7 : R data
GA0~GA7 : G data
BB0~BB7 : B data

1,1	1,2	1,3	----------	1,1600
2,1	2,2	2,3	----------	2,1600
3,1	3,2	3,3	----------	3,1600
1200,1	1200,2	1200,3	----------	1200,1600



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input data	R data								G data								B data							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

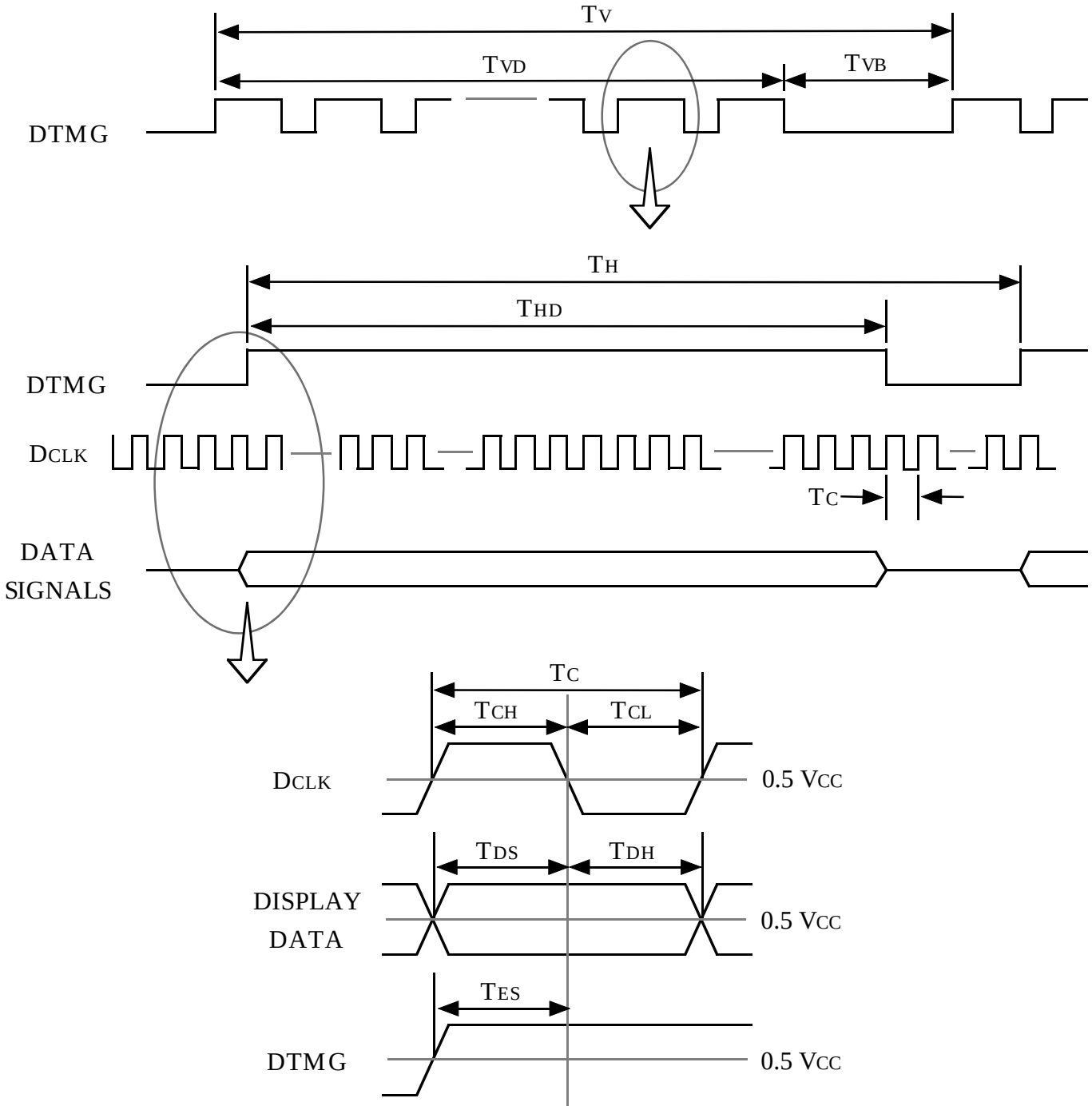
Notes 1) Definition of gray scale : Color (n)

n indicates gray scale level. Higher n means brighter level.

2) Data signals : 1:High, 0:Low

6. TIMING DIAGRAMS OF INTERFACE TIMING

6.1 Timing diagrams of interface signal

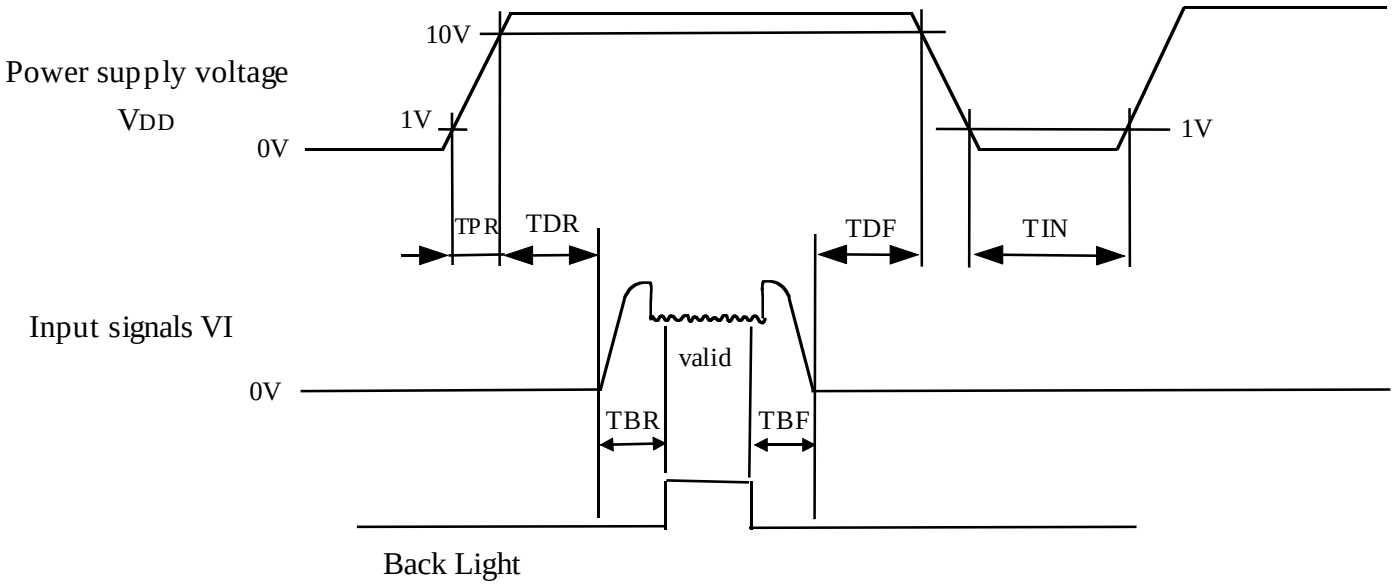


6.2 Timing Parameters

2pxl/clk

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock	Frequency	1/T_C	40	67.5	(81)	MHz	
	High Time	T_{CH}	4	-	-	nsec	
	Low Time	T_{CL}	4	-	-	nsec	
Data	Setup Time	T_{DS}	4	-	-	nsec	
	Hold Time	T_{DH}	4	-	-	nsec	
DTMG	Setup Time	T_{ES}	4	-	-	nsec	
Frame Frequency	Cycle	T_V	(15.9)	16.7	(17.5)	msec	
			1203	1203	(1270)	lines	
Vertical Active Display Term	Display Period	T_{VD}	1200	1200	1200	lines	
	Vertical Blank Period	T_{VB}	3	3	(70)	lines	
One Line Scanning Time	Cycle	T_H	840	936	(1080)	clocks	
Horizontal Active Display Term	Display Period	T_{HD}	800	800	800	clocks	

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

$0ms \leq TPR \leq 10ms$

$10ms \leq TDR \leq 50ms$

$0ms \leq TDF \leq 50ms$

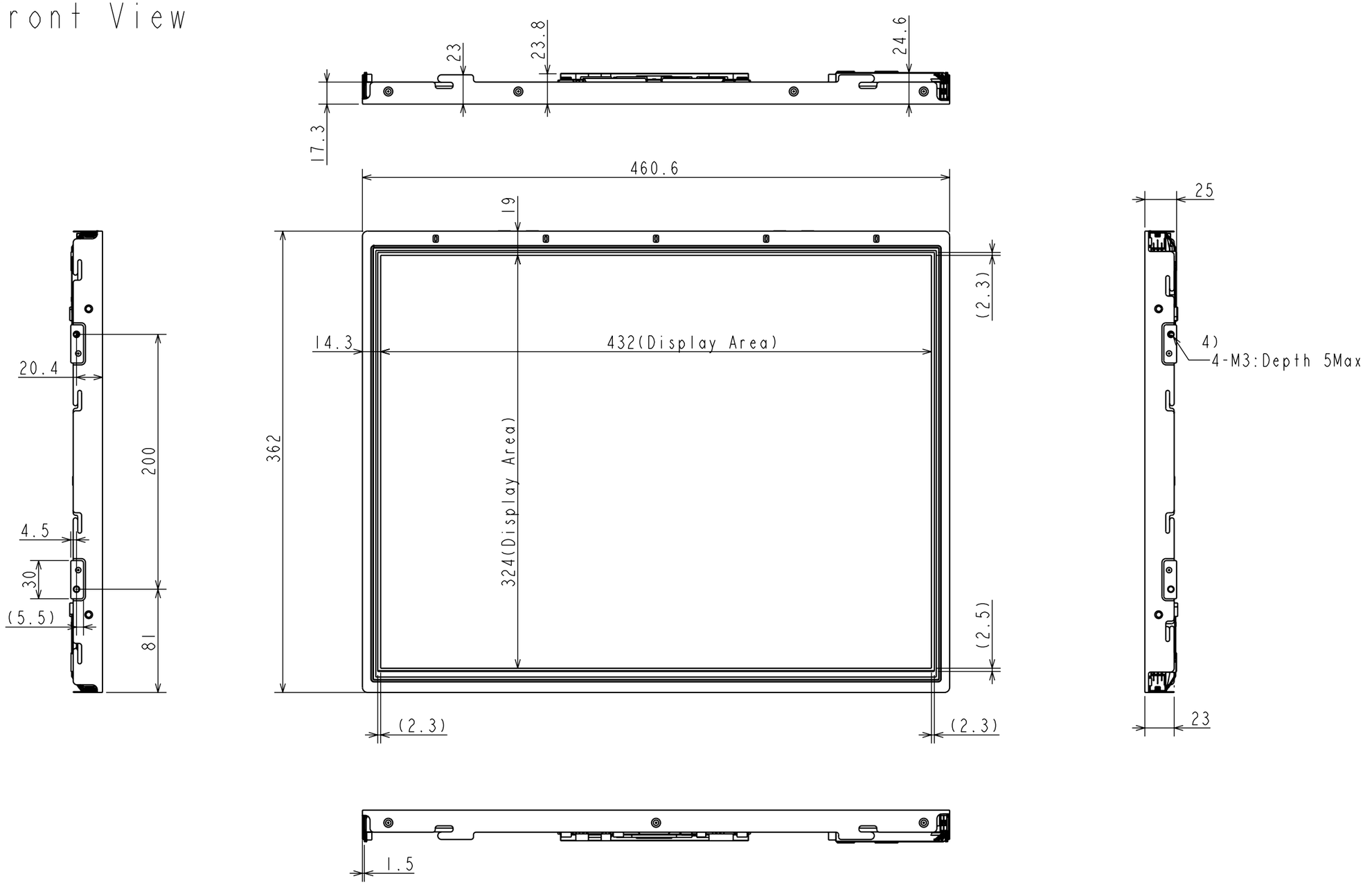
$TIN \geq 1s$

$TBR \leq 500ms$

$TBF \leq 100ms$

7. Dimensional Outline

(1)Front View



Note 1) Dimension in parentheses are reference value.
2) Tolerance not specified is +/-0.5mm.
3) Measure the thickness with 9.8×10^4Pa(1.0kgf/cm^2) Pressure.
4) Maximum torque for the screw in mounting module : 0.784Nm.

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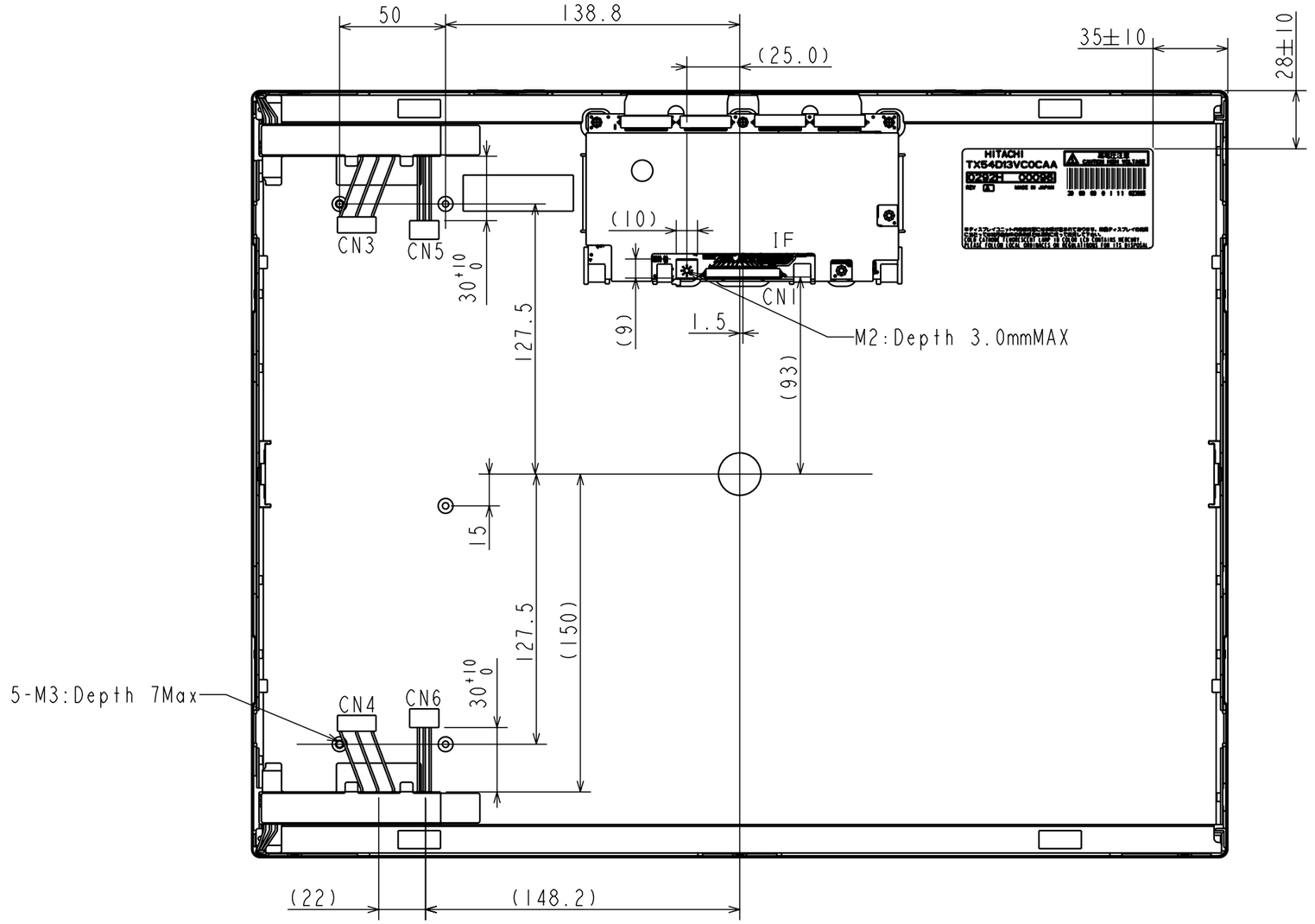
(2)Back View



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