

**To : Shenzhen JLD Electronics Co., Ltd**

Date : June 05, 2013

<b>TECHNICAL DATA</b>	
<b>Product Name</b>	<b>TX54D82MM0BAA</b>

(NOTES)

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**RECORD OF REVISION**

Date	The upper section : Before revision The lower section : After revision		Summary
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## DESCRIPTION

Note : The LED for the backlight unit is integrated within this module.

**Product Name : TX54D82MM0BAA**

### GENERAL SPECIFICATIONS

Effective Display Area	: (H)422.4 × (V)337.92	(mm)
Number of Pixels	: (H)2,560 × (V)2,048	(pixels)
Sensor Area	: Top/Right of Landscape Number of pixels (H)440 × (V)16	(pixels)
Aspect ratio	: 5:4	
Pixel Pitch	: (H)0.165 × (V)0.165	(mm)
Pixel Arrangement	: 3 subpixel per 1 pixel , Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Frame frequency	: 50 Hz	
Top Polarizer Type	: Anti-glare (Surface hardness: 2H)	
Supported Grayscale	: 10-bits per each subpixel	
LCM Mode	: IPS-NEO	
Input Signal	: 4-channel LVDS (LVDS = Low Voltage Differential Signaling)	
Back Light	: Edge Light Type with white LED	
External Dimensions	: (H)459.8 × (V)375.3 × (t)(43.0)	
Weight	: 4200g max (3950g typ.)	
RoHS	:Compliance	

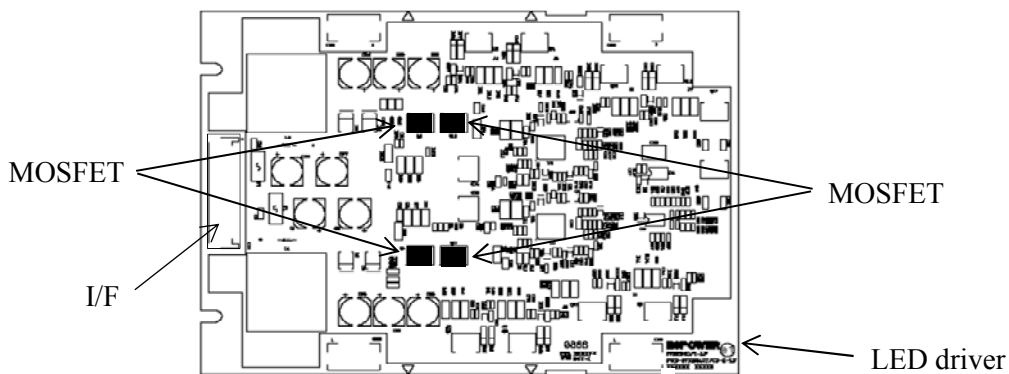
# 1. ABSOLUTE MAXIMUM RATINGS

## 1.1 ENVIRONMENT ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Panel surface Temperature	0	60	-20	60	°C	1)
Humidity	2)		2)		%RH	1)
Vibration	-	2.45 (0.25G)	-	9.8 (1.0G)	m/s <sup>2</sup>	3)
Shock	-	14.7 (1.5G)	-	294 (30G)	m/s <sup>2</sup>	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
TCON Surface Temperature	-	85	-	85	°C	6)
LED Driver parts Temperature	-	85	-	85	°C	7)

### Notes

- 1) Temperature and Humidity should be applied to the panel surface of the TFT module and not to the system installed with the module.
- 2)  $T_a \leq 40^\circ\text{C}$  : Relative humidity should be less than 85%RH max. Dew is prohibited.  
 $T_a > 40^\circ\text{C}$  : Relative humidity should be lower than the moisture of the 85%RH at  $40^\circ\text{C}$  .
- 3) Frequency of vibration is between 15Hz and 100Hz, except resonance point and z-direction ( panel face top and bottom ).
- 4) Pulse width of the shock wave pattern is 10ms approximately.
- 5) LCD module should be mounted with chassis by screwed all 8 positions, which 4 positions are top and bottom side, other 4 positions are on right and left side.
- 6) FPGA-IC
- 7) MOSFET : MOSFET are placed at below on LED driver board.



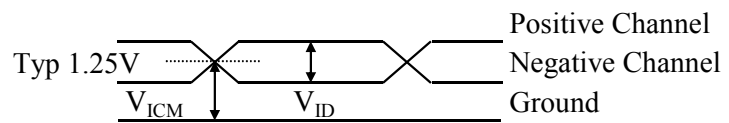
## 1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

### (1) TFT-LCD Module

$V_{SS} = 0 \text{ V}$

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	$V_{DD}$	-0.3	13.2	V	
Input Differential voltage swing	$V_{ID}$	100	900	mV	1)
Input common mode voltage	$V_{ICM}$	500	1800	mV	1)
Electrostatic Durability	$V_{ESD0}$	$\pm 100$		V	2),3)
	$V_{ESD1}$	$\pm 8$		kV	2),4)

Notes 1) It is applied to LVDS specifications.



- 2) Discharge Coefficient: 200pF-250 $\Omega$ , Environmental: 25°C-70%RH
- 3) It is applied to I/F connector pins.
- 4) It is applied to the surface of a metallic bezel and a LCD panel.

### (2) Back Light Inverter

$V_{SS} = 0 \text{ V}$

Item	Symbol	Min.	Max.	Unit	Note
Input Voltage	$V_{IN}$	-0.3	30.0	V	
ON/OFF Control Input Voltage	ON/OFF	0	6.0	V	
PWM signal Voltage	$V_{pwm}$	0	6.0	V	

## **2. INITIAL OPTICAL CHARACTERISTICS**

The following initial optical characteristics are measured under stable conditions.

It takes about 30 minutes to reach stable conditions.

The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent environment.

All initial optical characteristics items should be applied when panels have been shipped.

Measuring equipment : CS-2000 , CA-210, or EZ-contrast

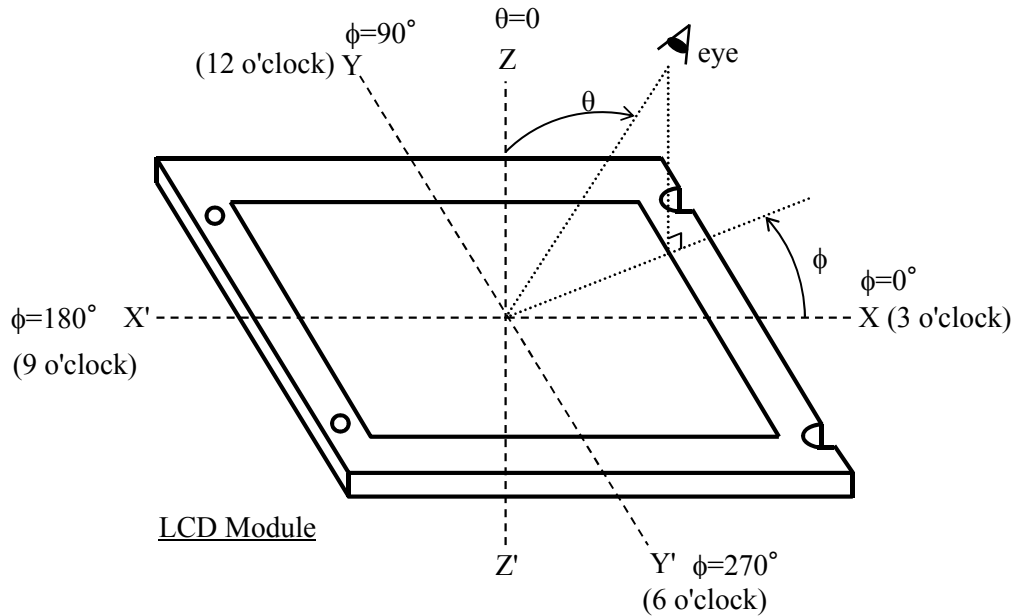
Ambient Temperature =25°C, V<sub>DD</sub>=12.0V, V<sub>IN</sub>=24V , fV=50Hz

### **2.1 SPECIFICATION**

Item		Condition	Min.	Typ.	Max.	Unit	Notes
Contrast ratio		$\theta = 0^\circ$	900	1200	—	—	1), 2)
Contrast ratio	CR88°	$\phi = 0, 90, 180, 270$	50	—	—		1)
Brightness	Bwh	$\theta = 0^\circ$	850	1200	—	cd/m <sup>2</sup>	6)
Brightness uniformity	Buni 1023	$\theta = 0^\circ$ Gray scale = 1023	75	—	—	%	4)
	Buni 511	$\theta = 0^\circ$ Gray scale = 511	70	—	—	%	
Color chromaticity	White	x	0.264	0.294	0.324	—	1)
		y	0.279	0.309	0.339		
Variation of color point by viewing angle (Gray scale = 1023)		$\theta = \pm 80$ $\phi = 0, 90, 180, 270$	—	—	0.04	$\Delta u'v'$	5)
Response time	Rise	ton	—	25	—	ms	3)
	Fall	toff					

Notes

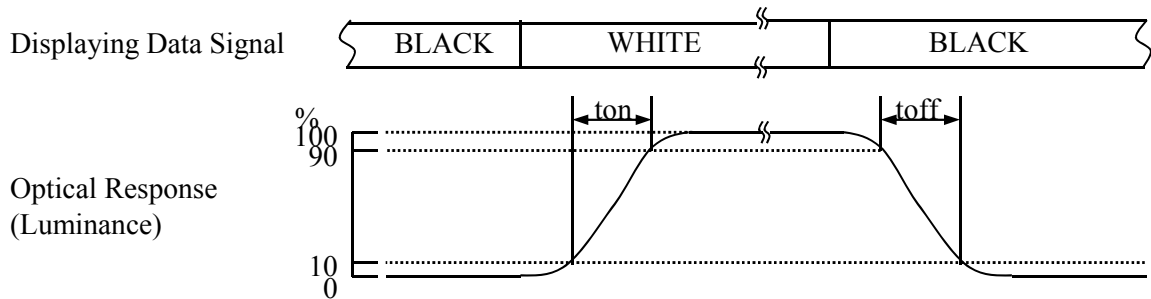
1) Definition of Viewing Angle ( gray scale = 1023 )



2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



Panel surface temperature = 45°C

4) Definition of Brightness Uniformity

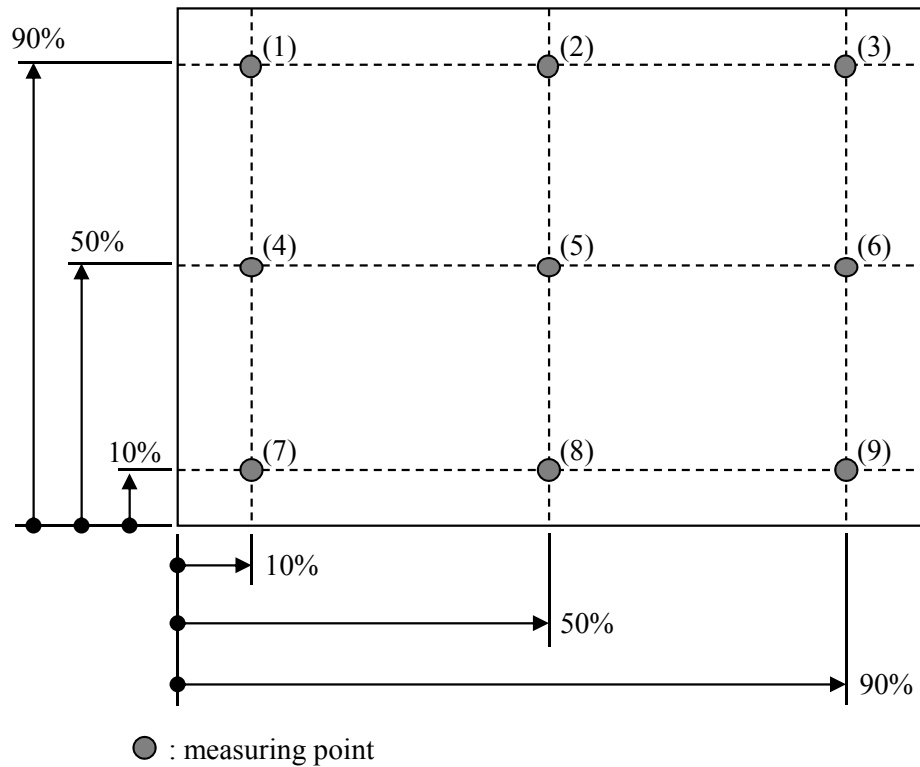
Display pattern is white (511/1023 level). The brightness uniformity is defined by the following equation. Brightness at each point is measured and then Buni can be calculated using the maximum and minimum brightness values.

$$Buni = \left( \frac{B_{min}}{B_{max}} \right) \times 100$$

where, Bmax = Maximum brightness measured.

Bmin = Minimum brightness measured.





5) Variation of color position on CIE is defined as difference between colors for TFT-LCD module.

$$u' = \frac{4x}{-2x + 12y + 3} \quad v' = \frac{9y}{-2x + 12y + 3}$$

6) PWM dimming signal Voltage should be 3.0V.

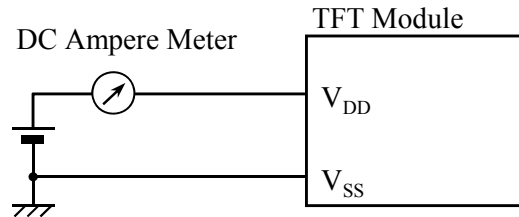
### 3. ELECTRICAL CHARACTERISTICS

#### 3.1 TFT-LCD MODULE

Ta=25°C, V<sub>SS</sub>=0V

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	11.4	12.0	12.6	V	
Power Supply Current	I <sub>DD</sub>	-	1.3	1.5	A	1),2)
Ripple Voltage of Power Supply	V <sub>DDR</sub>	-	-	0.15	V	

Notes 1) DC current at f<sub>V</sub>=50.0Hz, f<sub>CLK</sub>=74MHz, V<sub>DD</sub>=12.0V and display pattern is a full White (1023).



- 2) A protection fuse is built into this module. Current capacity of the power supply for V<sub>DD</sub> should be greater than 6A, so that the fuse can 'blow' if there is a problem with the power supply.

#### 3.2 BACK LIGHT

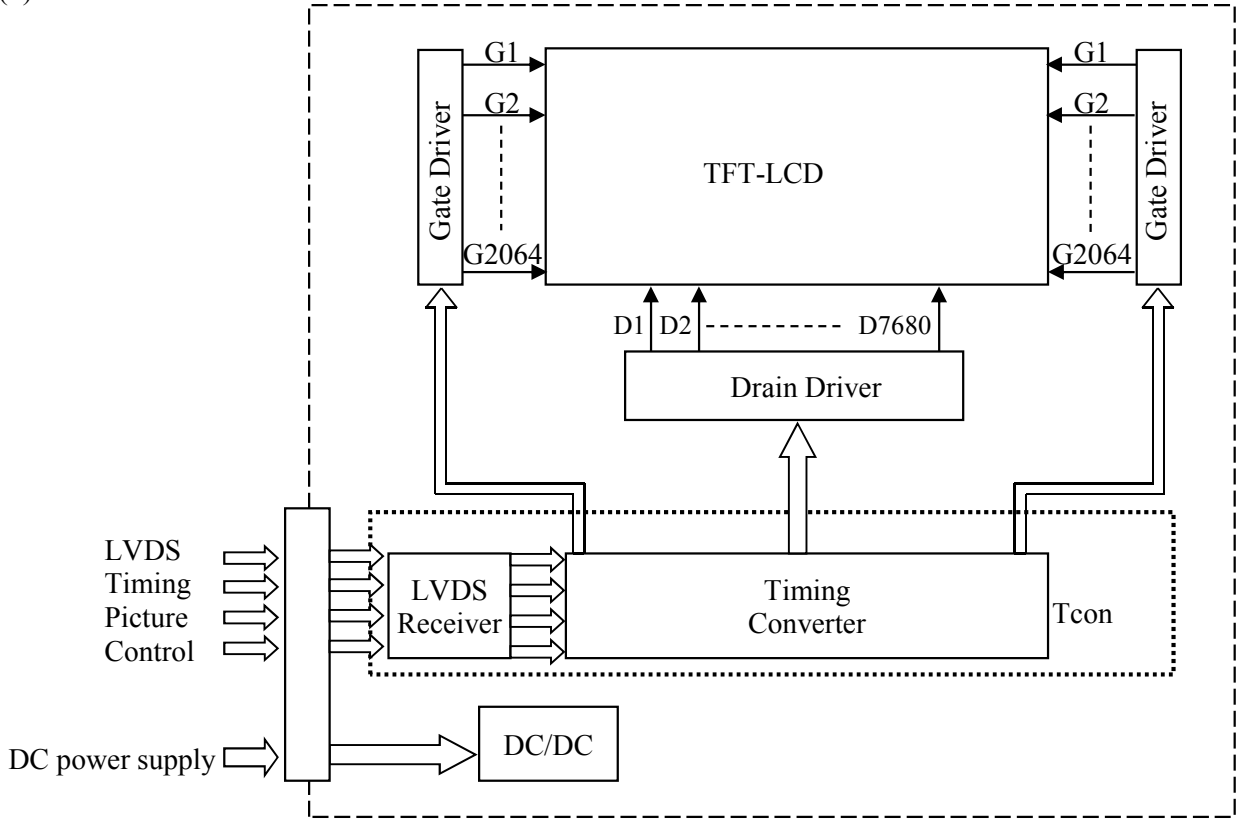
Ta=25°C

Item	Symbol	Value			Unit	Note	
		Min	Typ	Max			
Input Voltage	V <sub>in</sub>	21.6	24	26.4	V		
Input Current	I <sub>in</sub>	-	1.9	2.5	A		
Input Power	P <sub>in</sub>	-	46	54	W		
ON/OFF Control Input Voltage	ON	ON/OFF	2.5	3.3	5.0	V	
	OFF		0	-	0.5	V	
PWM dimming signal Input Voltage	PWM	Hight	2.5	3.3	5.0	Vdc	
		Low	0	-	0.9		
PWM Duty	-	5	-	100	%		
PWM Frequency	PWMf	150	-	1000	Hz	1)	

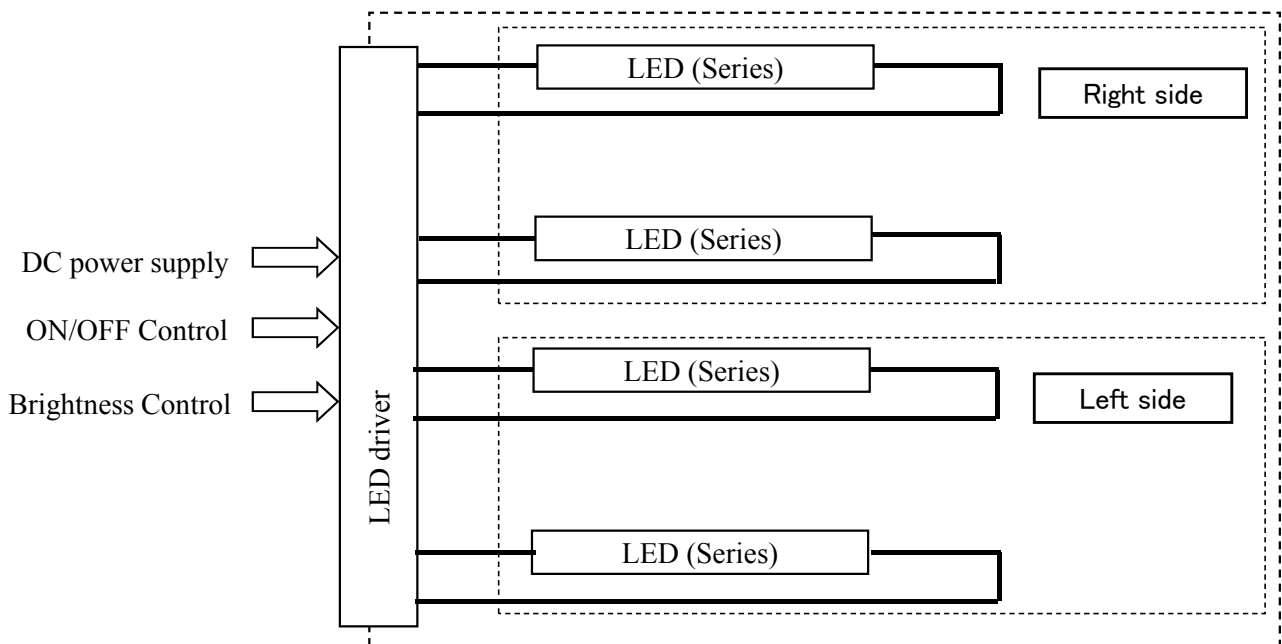
- 1) In order to avoid interference image on screen such as beat noise, please pay attention and keep PWM drive frequency away from the multiple number of panel drive frequency.

#### 4. BLOCK DIAGRAM

##### (1) TFT Module



##### (2) Back light unit



## 5. INTERFACE PIN ASSIGNMENT

### 5.1 TFT-LCD MODULE

INPUT CONNECTOR : HIROSE

Plug FX15S-41S-0.5SH (PCB connector side)

FX15S-41P-C (cable side)

LEFT I/F connector (CN1) (CH1, 2)

Power Supply	1	V <sub>DD</sub>
	2	V <sub>DD</sub>
	3	V <sub>DD</sub>
	4	V <sub>DD</sub>
	5	V <sub>DD</sub>
	6	V <sub>SS</sub>
	7	V <sub>SS</sub>
	8	V <sub>SS</sub>
	9	V <sub>SS</sub>
CH1	10	ARX0n
	11	ARX0p
	12	ARX1n
	13	ARX1p
	14	V <sub>SS</sub>
	15	ARX2n
	16	ARX2p
	17	ACLKn
	18	ACLKp
	19	V <sub>SS</sub>
	20	ARX3n
	21	ARX3p
	22	ARX4n
	23	ARX4p
	24	V <sub>SS</sub>
CH2	25	BRX0n
	26	BRX0p
	27	BRX1n
	28	BRX1p
	29	V <sub>SS</sub>
	30	BRX2n
	31	BRX2p
	32	BCLKn
	33	BCLKp
	34	V <sub>SS</sub>
	35	BRX3n
	36	BRX3p
	37	BRX4n
	38	BRX4p
	39	V <sub>SS</sub>
	40	TEST
	41	TEST

RIGHT I/F connector (CN2) (CH3, 4)

Power Supply	1	V <sub>DD</sub>
	2	V <sub>DD</sub>
	3	V <sub>DD</sub>
	4	V <sub>DD</sub>
	5	V <sub>DD</sub>
	6	V <sub>SS</sub>
	7	V <sub>SS</sub>
	8	V <sub>SS</sub>
	9	V <sub>SS</sub>
CH3	10	CRX0n
	11	CRX0p
	12	CRX1n
	13	CRX1p
	14	V <sub>SS</sub>
	15	CRX2n
	16	CRX2p
	17	CCLKn
	18	CCLKp
	19	V <sub>SS</sub>
	20	CRX3n
	21	CRX3p
	22	CRX4n
	23	CRX4p
	24	V <sub>SS</sub>
CH4	25	DRX0n
	26	DRX0p
	27	DRX1n
	28	DRX1p
	29	V <sub>SS</sub>
	30	DRX2n
	31	DRX2p
	32	DCLKn
	33	DCLKp
	34	V <sub>SS</sub>
	35	DRX3n
	36	DRX3p
	37	DRX4n
	38	DRX4p
	39	V <sub>SS</sub>
	40	TEST
	41	TEST

Notes 1) All V<sub>SS</sub> pins should be grounded.

2) All V<sub>DD</sub> pins should be connected to +12.0 V (typ.).

3) TEST Pins are only for Japan Display use. (Must be kept open and do not connect any input.)

## 5.2 BACK-LIGHT UNIT

CN3 : JST S14B-PH-SM4-TB (Inverter PCB Connector side)

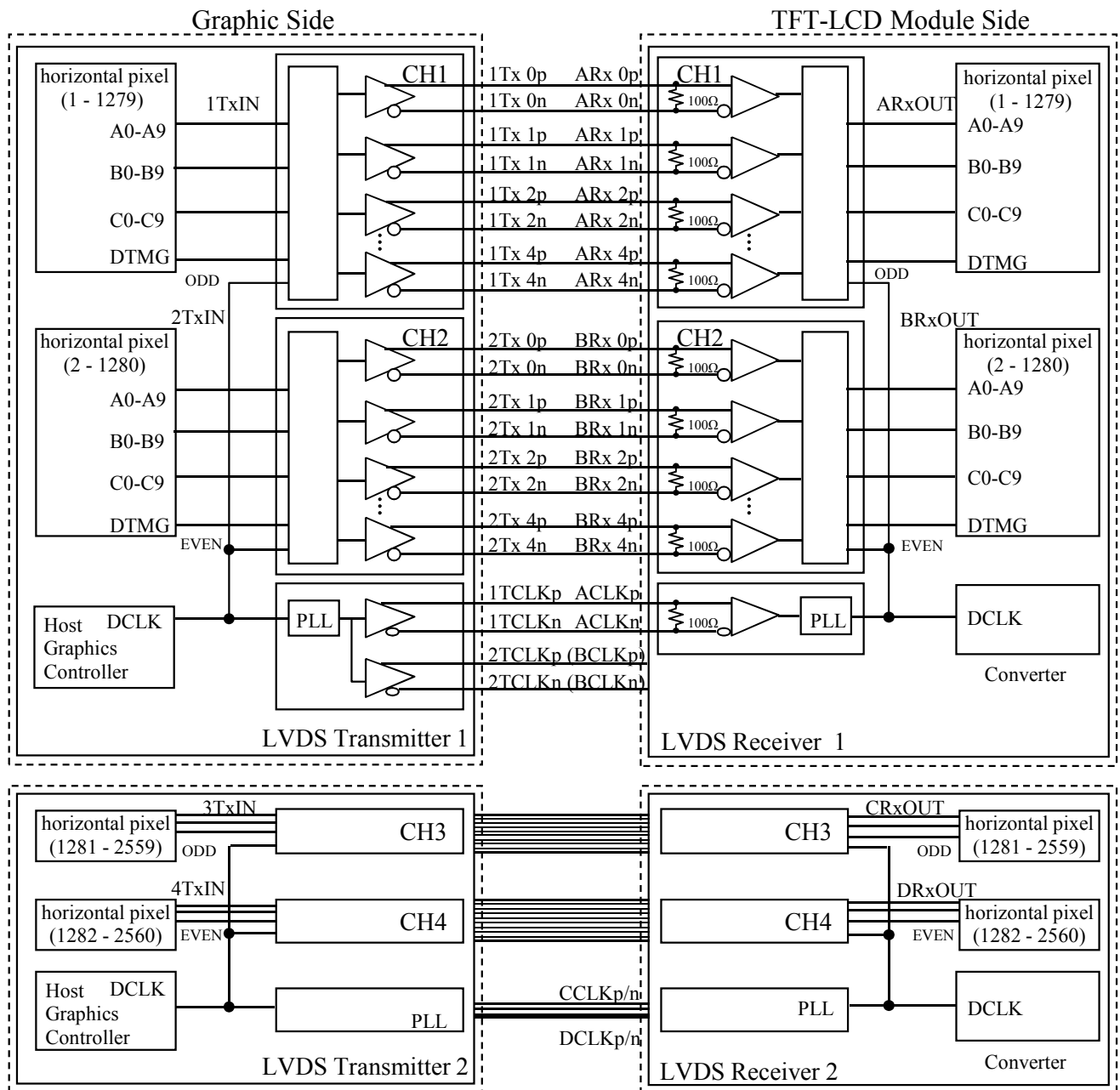
(Matching connector : JST PHR-14 (Cable side))

Pin No.	Symbol	Description	Note
1	$V_{IN}$	Power Supply (typ. 24.0V)	1)
2	$V_{IN}$		
3	$V_{IN}$		
4	$V_{IN}$		
5	$V_{IN}$		
6	$V_{SS}$	GND (0V)	2)
7	$V_{SS}$		
8	$V_{SS}$		
9	$V_{SS}$		
10	$V_{SS}$		
11	NC	Not Connecting	
12	ON/OFF	High : Lamp ON, Low : Lamp OFF	3)
13	NC	Not Connecting	
14	PWM	PWM Dimming signal	4)

### Notes

- 1) All  $V_{IN}$  pins should be connected to +24.0V (Typ.).
- 2) All  $V_{SS}$  pins should be grounded. The metal bezel is internally connected to GND.
- 3) High level : 2.5 ~ 5.0V, Low level : 0 ~ 0.5V
- 4) High level : 2.5 ~ 5.0V, Low level : 0 ~ 0.9V

### 5.3 BLOCK DIAGRAM OF INTERFACE

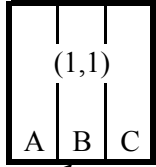


- A 0 ~ A 9 : A SUB Pixel data
- B 0 ~ B 9 : B SUB Pixel data
- C 0 ~ C 9 : C SUB Pixel data
- DTMG : Display timing signal
- DCLK : Dot Clock (DCLK of CH2, 4 are not used.)

Notes 1) The host system must have the transmitter in-situ to drive the module.  
 2) LVDS cable impedance should be 100 ohms per twisted-pair line when used differentially.

## 5.4 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent pixel is latched during one cycle of DCLK.



pixel : A 0 ~ A 9 : A SUB Pixel data  
 B 0 ~ B 9 : B SUB Pixel data  
 C 0 ~ C 9 : C SUB Pixel data

1,1	3,1	5,1	...	1279,1	2,1	4,1	6,1	...	1280,1	1281,1	1283,1	1285,1	...	2559,1	1282,1	1284,1	1286,1	...	2560,1	
1,2	3,2	5,2	...	1279,2	2,2	4,2	6,2	...	1280,2	1281,2	1283,2	1285,2	...	2559,2	1282,2	1284,2	1286,2	...	2560,2	
1,3	3,3	5,3	...	1279,3	2,3	4,3	6,3	...	1280,3	1281,3	1283,3	1285,3	...	2559,3	1282,3	1284,3	1286,3	...	2560,3	
1,4	3,4	5,4	...	1279,4	2,4	4,4	6,4	...	1280,4	1281,4	1283,4	1285,4	...	2559,4	1282,4	1284,4	1286,4	...	2560,4	
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1,2064	3,2064	5,2064	...	1279,2064	2,2064	4,2064	6,2064	...	1280,2064	1281,2064	1283,2064	1285,2064	...	2559,2064	1282,2064	1284,2064	1286,2064	...	2560,2064	

CH1 (LEFT\_ODD)

CH2 (LEFT\_EVEN)

CH3 (RIGHT\_ODD)

CH4 (RIGHT\_EVEN)

### 5.5 RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Input		A SUB Pixel Data								B SUB Pixel Data								C SUB Pixel Data															
		A9	A8	A7	...	A3	A2	A1	A0	B9	B8	B7	...	B3	B2	B1	B0	C9	C8	C7	...	C3	C2	C1	C0								
Color		MSB								LSB								MSB								LSB							
		Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A (1023)	1		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B (1023)	0		0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C (1023)	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B(1023) C(1023)	0		0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A(1023) C(1023)	1		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A(1023) B(1023)	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
White	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
A	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	A (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	A (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	A (1022)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	A (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	B (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	B (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	B (1022)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	B (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	C	C (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
C (2)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
C (1022)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
C (1023)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Notes 1) Definition of gray scale :

Color (n) : Number in parenthesis indicates gray scale level. Larger n corresponds to a brighter level.

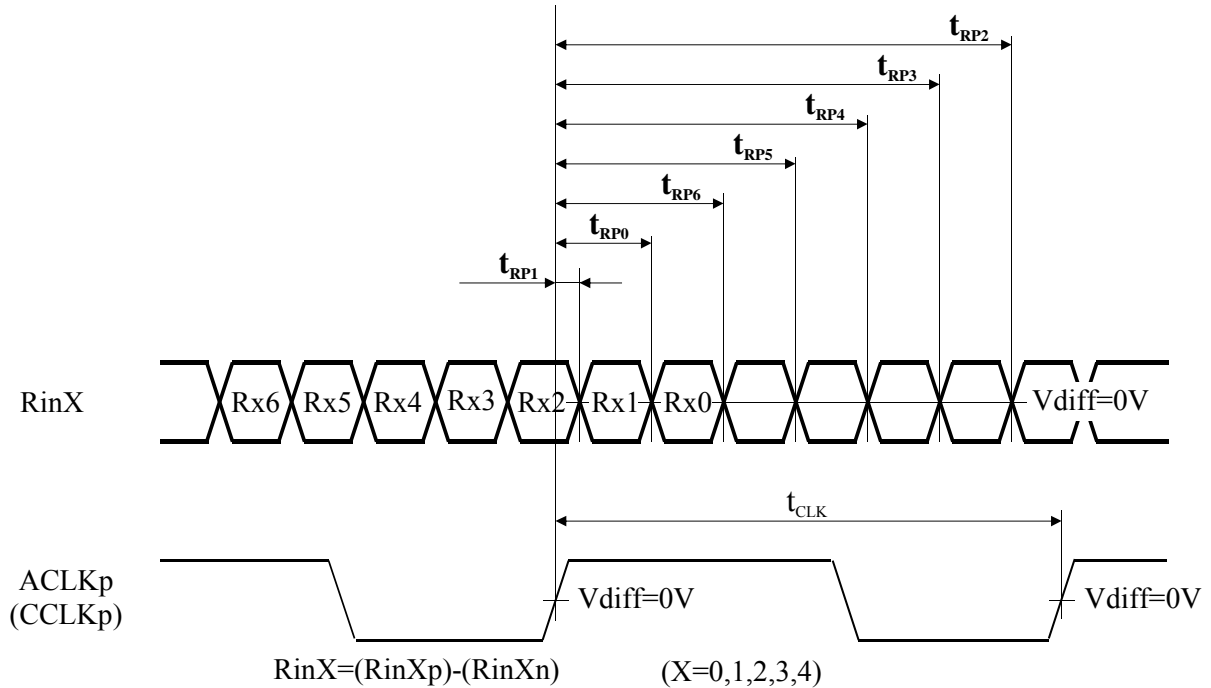
2) Data : 1 : High, 0 : Low



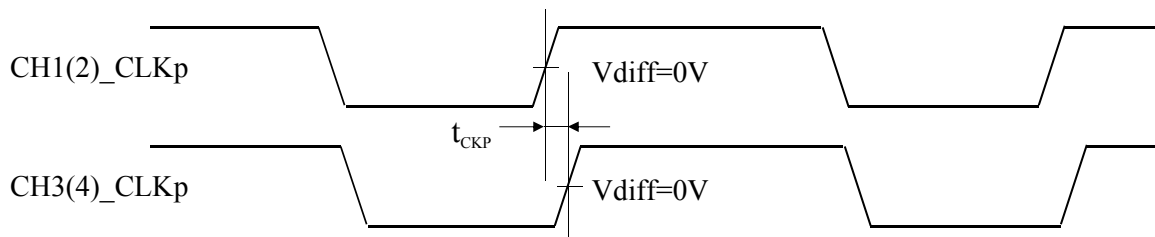
## 6. INTERFACE TIMING

### 6.1 LVDS RECEIVER TIMING CHARACTERISTICS

(Regulation with the Input Terminal of the Module)

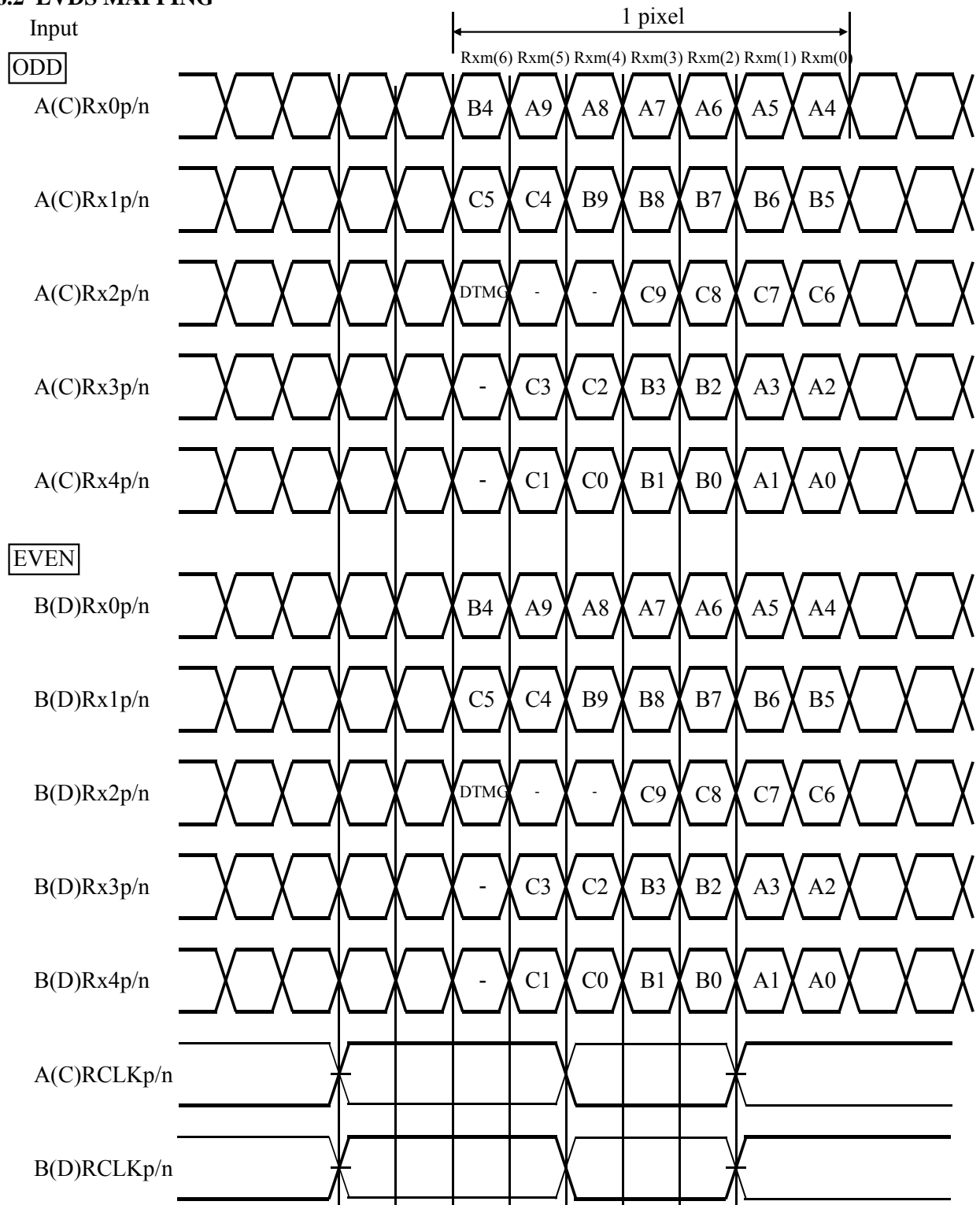


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCLK	Parameter	$1/t_{CLK}$	71	74	76	MHz
$t_{sk}$	Data Skew Margin	-	-400	0	+400	ps
RinX (X=0,1,2,3,4)	Input Data Position0	$t_{RP0}$	$1/7t_{CLK} - t_{sk}$	$1/7t_{CLK}$	$1/7t_{CLK} + t_{sk}$	ns
	Input Data Position1	$t_{RP1}$	$0 - t_{sk}$	0	$0 + t_{sk}$	
	Input Data Position2	$t_{RP2}$	$6/7t_{CLK} - t_{sk}$	$6/7t_{CLK}$	$6/7t_{CLK} + t_{sk}$	
	Input Data Position3	$t_{RP3}$	$5/7t_{CLK} - t_{sk}$	$5/7t_{CLK}$	$5/7t_{CLK} + t_{sk}$	
	Input Data Position4	$t_{RP4}$	$4/7t_{CLK} - t_{sk}$	$4/7t_{CLK}$	$4/7t_{CLK} + t_{sk}$	
	Input Data Position5	$t_{RP5}$	$3/7t_{CLK} - t_{sk}$	$3/7t_{CLK}$	$3/7t_{CLK} + t_{sk}$	
	Input Data Position6	$t_{RP6}$	$2/7t_{CLK} - t_{sk}$	$2/7t_{CLK}$	$2/7t_{CLK} + t_{sk}$	



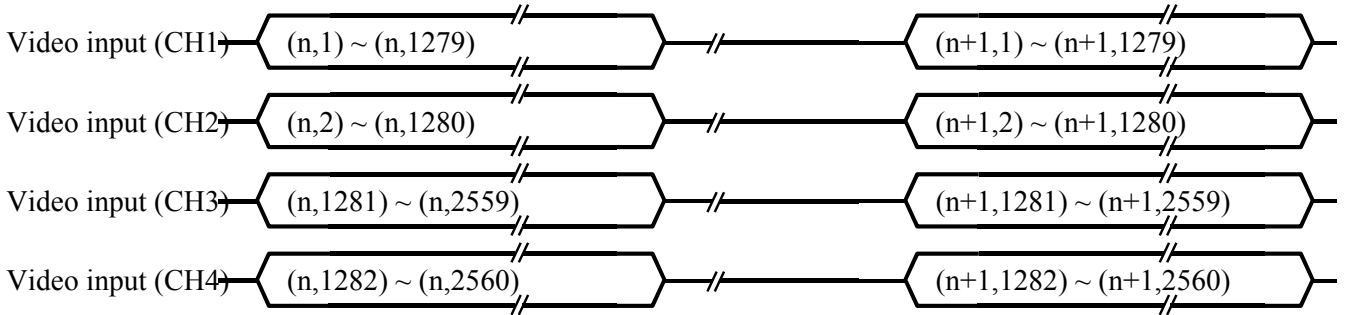
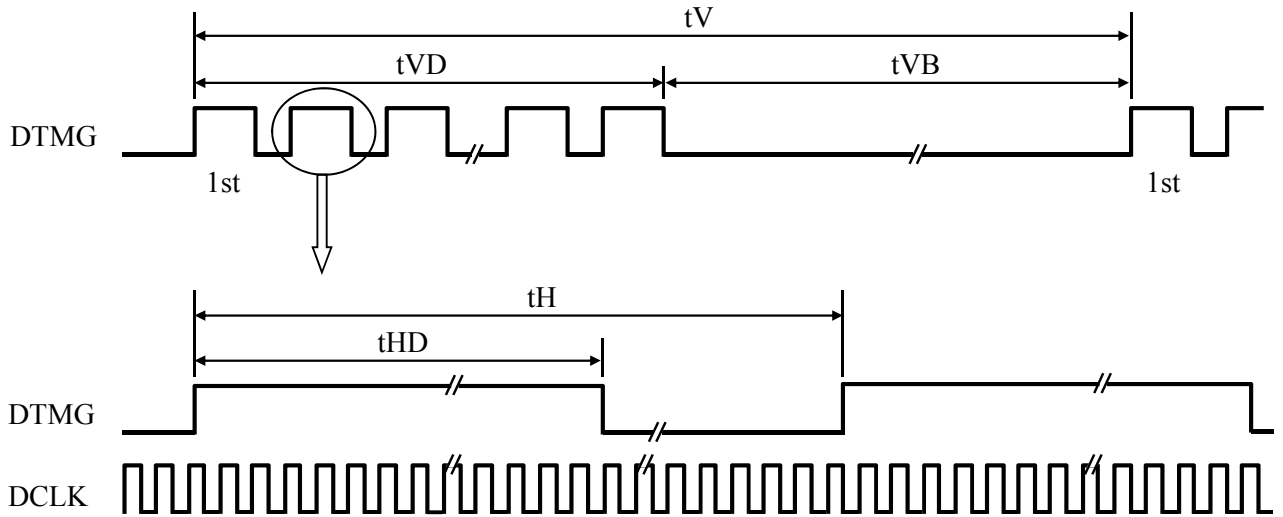
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLKp	Input CLK Position	$t_{CKP}$	-1	0	+1	DCLK

## 6.2 LVDS MAPPING



A0 ~ A9 : Pixel A Data (9;MSB, 0;LSB)  
 B0 ~ B9 : Pixel B Data (9;MSB, 0;LSB)  
 C0 ~ C9 : Pixel C Data (9;MSB, 0;LSB)  
 DTMG : Display timing signal  
 RCLK : Dot Clock

### 6.3 TIMING CHART



(n=1,2,3, ~ 2064)

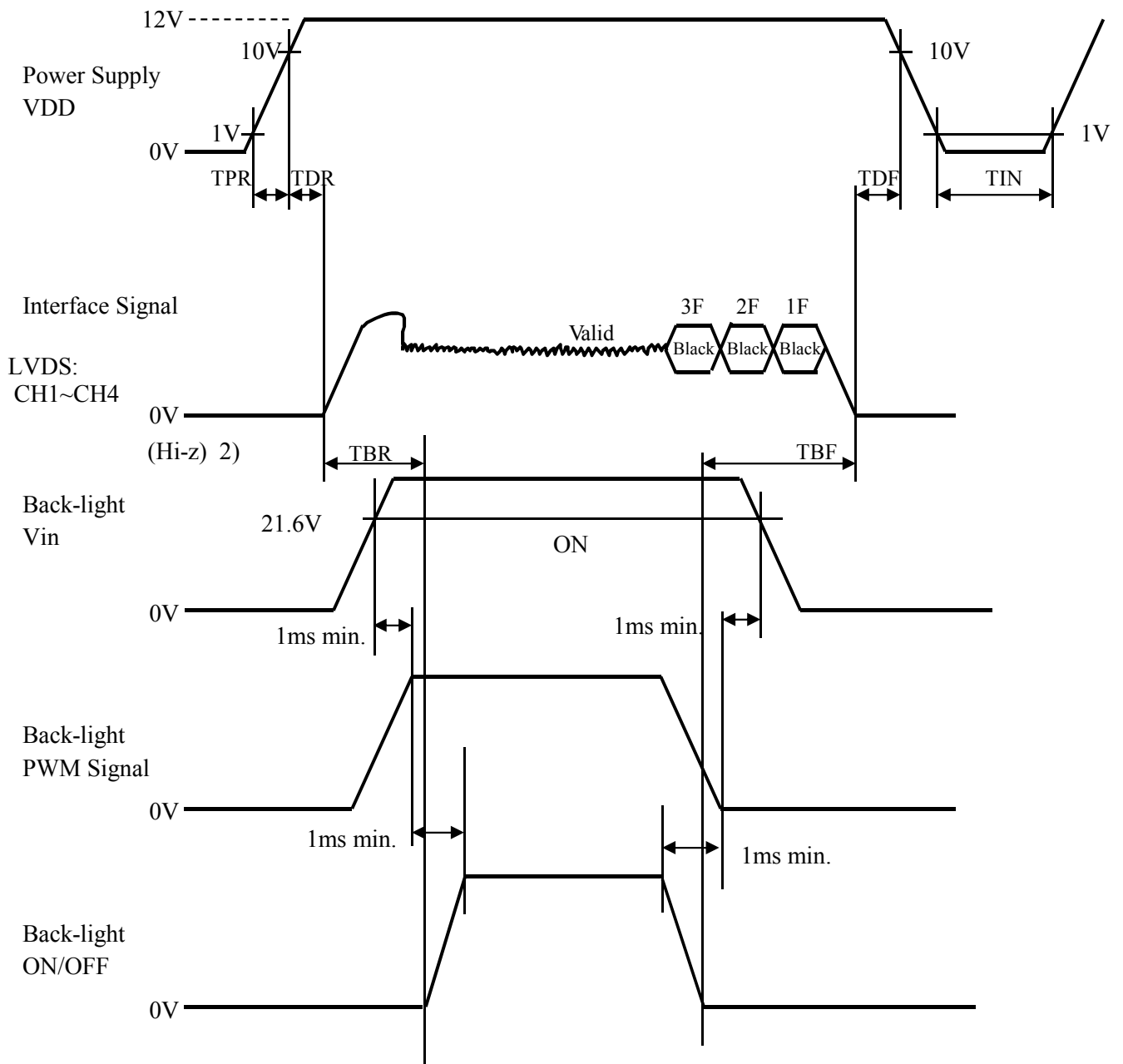
## 6.4 INTERFACE TIMING SPECIFICATIONS

Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame	Frequency	$f_V$	49	50	51	Hz	
DCLK	Frequency	$1/t_{CYC}$	71	74	76	MHz	1)
	Duty	$t_{CH}/t_{CYC}$	45	50	55	%	
DTMG	Period (Hor)	$t_H$	698	712	1023	tCK	
	Width Active (Hor)	$t_{HD}$	640	640	640	tCK	
	Period (Ver)	$t_V$	2072	2076	2303	tH	
	Width Active (Ver)	$t_{VD}$	2064	2064	2064	tH	
	DTMG Jitter	$\Delta t_{VB}$	-1	0	1	tH	

### Note

- 1) Since DCLK and inverter driving frequency are optimized, please be noted that DCLK should be set within this spec. Otherwise, optical side effect may happen.

## 6.5 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



### Notes

1) Timing of the power supply voltage and input signals should be set using the following specifications.

$$0.5\text{ms} \leq \text{TPR} \leq 10\text{ms}$$

$$10\text{ms} \leq \text{TDR} \leq 50\text{ms}$$

$$-10\text{ms} \leq \text{TDF} \leq 50\text{ms}$$

$$\text{TIN} \geq 1\text{s}$$

$$\text{TBR} \geq 500\text{ms}$$

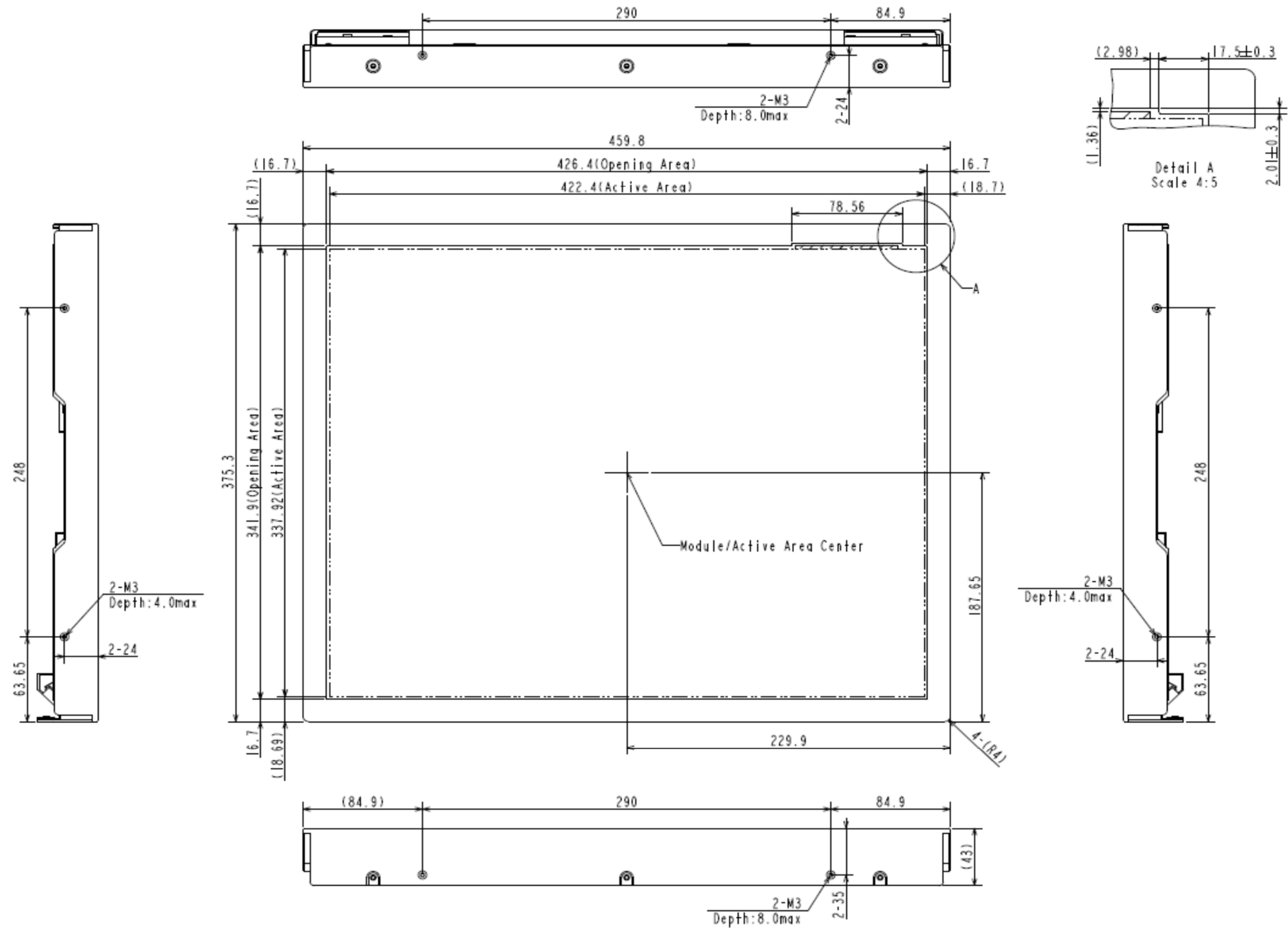
$$\text{TBF} \geq 100\text{ms}$$

\*Before the end of the Interface Signal, black image is shown for the last 3 frames. Refer to above Interface Signal Timing.

2) LVDS signals must be Low or High-impedance (Hi-z) state when VDD is off.

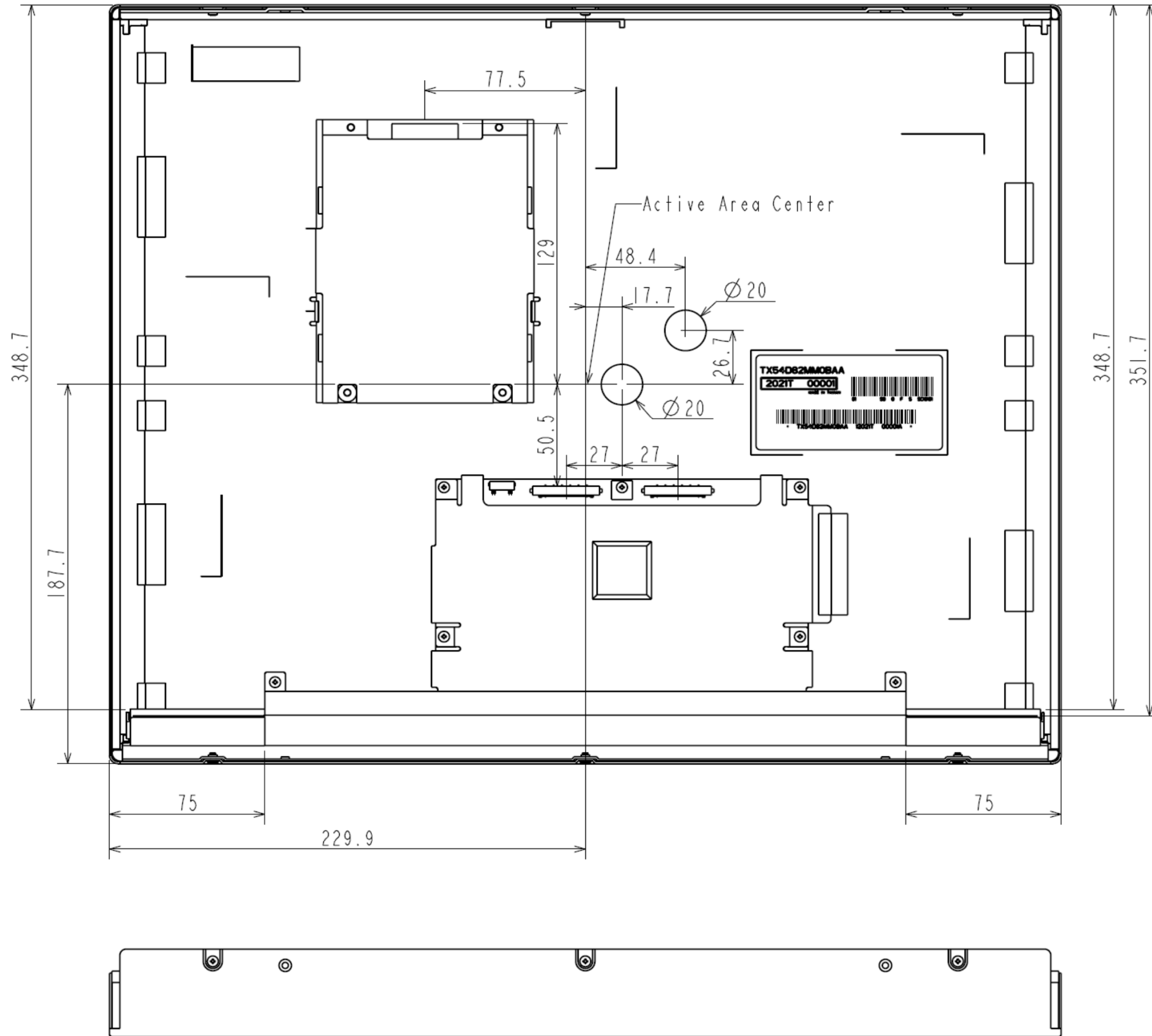
# 7. DIMENSIONAL OUTLINE

## (1) FRONT VIEW



- Note 1) Dimension in parentheses are reference value.  
 2) Tolerance not specified is  $\pm 0.5\text{mm}$   
 3) Maximum force for the screw in mounting module :  $0.49\text{n/m}$ .

(2) REAR VIEW

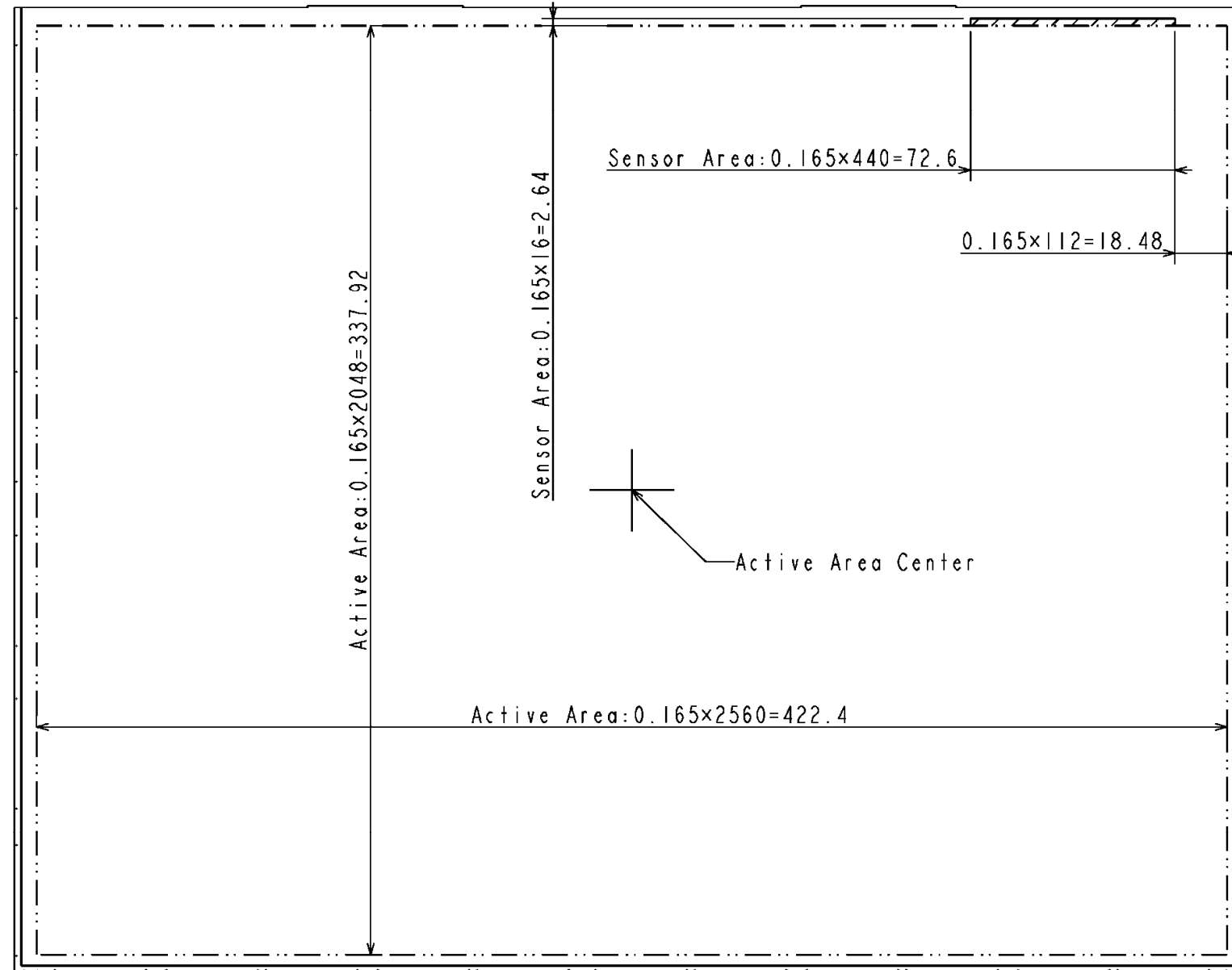


Scale:NTS  
Unit:mm

(3) ACTIVE AREA / SENSOR AREA

[Upper side]

[Lower side]

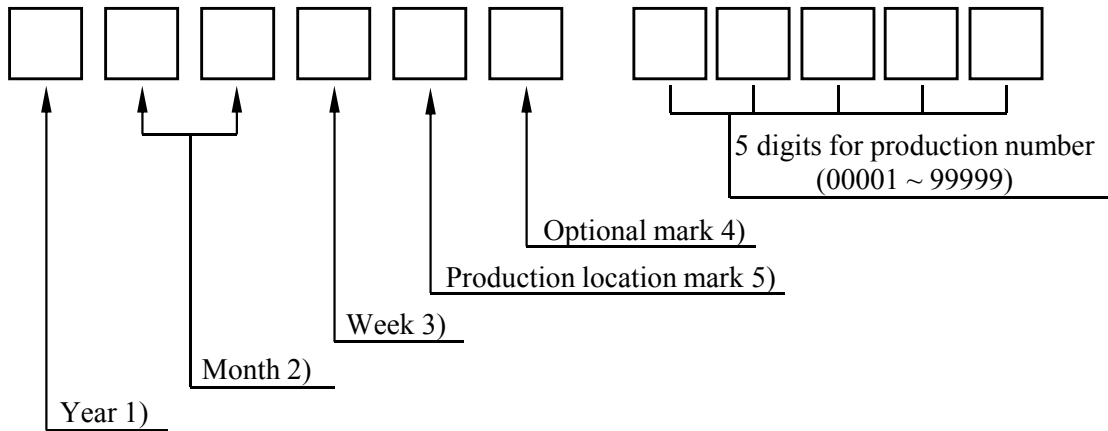


Unit : mm  
Scale : NTS



## 8. DESIGNATION OF LOT MARK

### 8.1 LOT MARK



Notes

1)

Year	Mark
2013	3
2014	4
2015	5
2016	6
2017	7

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Day)	Mark
1 ~ 7	1
8 ~ 14	2
15 ~ 21	3
22 ~ 28	4
29 ~ 31	5

4) for Japan Display internal use only.

5)

Production management sign	
T	Made in Taiwan

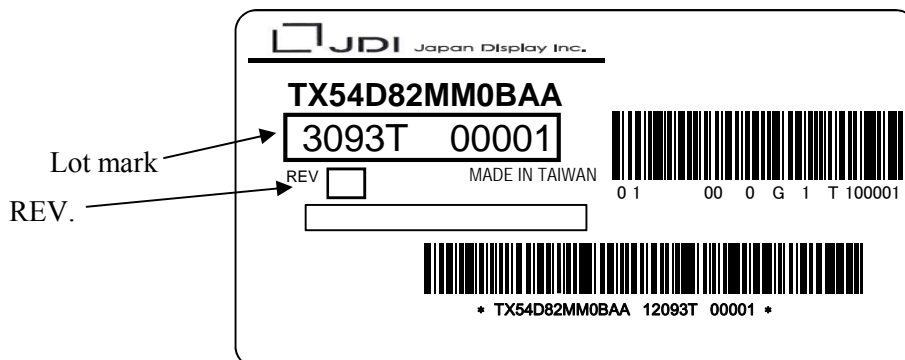
### 8.2 Revision (REV.) control

Revision version is denoted by letter A through Z, except I and O, for Japan Display manufacturing convenience.

Rev.	Note
A	—

### 8.3 Location of lot mark

The Lot mark is printed on a label which is attached to the rear bezel, as shown in 7. External Dimensional. The style of character can be changed without prior notice.

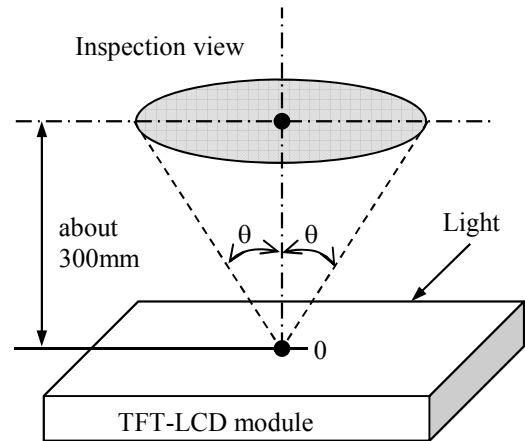


## 9. COSMETIC SPECIFICATIONS

### 9.1 CONDITIONS FOR COSMETIC INSPECTION

#### (1) Viewing zone

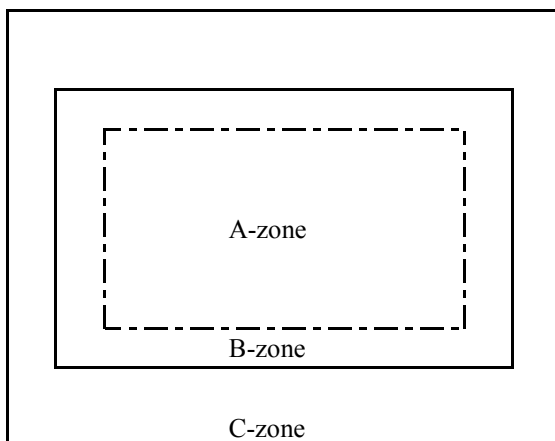
- a) The figure shows the correspondence between eyes (of inspector) and TFT-LCD module.
  - $q < 45^\circ$  : when non-operating inspection
  - $q < 5^\circ$  : when operating inspection
- b) Inspection should be executed only from front side and only A-zone.  
Cosmetic of B-zone and C-zone are ignore.  
(refer to 9.2 DEFINITION OF ZONE)



#### (2) Environmental

- a) Temperature :  $25^\circ\text{C}$
- b) Ambient light : sufficient darker condition when operating inspection.  
: about 1000 lx and non-directive when non-operating inspection.
- c) Back-light : when non-operating inspection, back-light should be off.

### 9.2 DEFINITION OF ZONE



- A-zone : Display area (pixel area).
- B-zone : Area between A-zone and C-zone.
- C-zone : Metal bezel area.  
(Include I/F connector)

### 9.3 COSMETIC SPECIFICATIONS

When displaying conditions are not stable (ex. at turn on or off), the following specifications are not applied.

	No.	Item			Max. acceptable number A-zone	Unit	Note		
Operating inspection	1	Dot Defect	Sparkle mode	1-dot	$560 \leq S$	0	pcs	1), 2)	
					$204 \leq S < 560$	12			
					Total	12			
						2-dot	0	pcs	1), 2)
					3-dot	0			
					4-dots	0			
					Density	2	pcs/ $\phi$ 20mm		
				Black mode	1-dot	13	pcs	3), 4)	
					2-dots	2	Units	3), 5)	
					3-dots	0			
					4-dots	0			
					Density	2	pcs/ $\phi$ 20mm	6)	
				Total		15	pcs		
				Total (Without slightly bright dot)			15	pcs	—
			2	Line defect			5% ND filter	—	—
	3	Uneven brightness			not allowed.				
	4	Stain inclusion Line shape W: width (mm) L: length (mm)	W < 0.1	L < 1.0	4	pcs	7)		
				L $\geq$ 1.0	0				
	5	Stain inclusion Dot shape D: ave. dia. (mm)	D $\leq$ 0.22		Ignore	pcs	7)		
			D $\leq$ 0.4		5				
			0.4 < D $\leq$ 0.6		4				
			D > 0.6		0				
	6	Scratch on polarizer Line shape W: width (mm) L: length (mm)	W $\leq$ 0.02	L: Ignore	Ignore	pcs	8)		
			W $\leq$ 0.04	L $\leq$ 40	10				
				L > 40	0				
			W $\leq$ 0.08	L $\leq$ 20	10				
				L > 20	0				
			W > 0.08	—	0				
	7	Scratch on polarizer Dot shape D: ave. dia. (mm)	D $\leq$ 0.2		Ignore	pcs	8)		
			D $\leq$ 0.6		10				
			D > 0.6		0				

	No.	Item	Max. acceptable number		Unit	Note
			A-zone			
non-operating inspection	8	Bubbles, peeling in polarizer [ D: ave. dia. (mm) ]	$D \leq 0.3$	Ignore	pcs	8)
			$D \leq 0.5$	10		
			$D \leq 1.0$	5		
			$D > 1.0$	0		
	9	Wrinkles on polarizer	Serious one is not allowed.		—	—

Notes 1) Sparkle mode: Brightness of dot is defined in ABC grayscale level.

2) Bright dot (A,B,C) : Brightness of dot  $\geq 560$  grayscale level.

Tiny Bright dot (A,B,C): Brightness of dot  $\geq 204$  grayscale level.

3) Black mode: brightness of dot is less than 70% at white. (visible to eye)

4) 1 dot: defect dot is isolated, not attached to other defect dot.

5) N dots: N defect dots are consecutive. (N means the number of defects dots)

6) Density: number of defect dots inside 20mm  $\phi$ .

7) Those stains which can be wiped out easily are acceptable.

8) Polarizer area inside of B-zone is not applied.

## **10. PRECAUTION**

Please pay close attention to the following precautions whilst using, handling and mounting the TFT module.

### **10.1 Precaution for handling and mounting**

- (1) Applying excessive force to any part of the module may result in partial deformation of the frame or mould, which could result in permanent damage to the display.
- (2) The module should be held gently and firmly using both hands. In order to avoid internal damage never hold the module by just one hand. Also never drop or hit the module.
- (3) The module should be installed using the mounting holes of the module.
- (4) Uneven force such as twisted stress should not be applied directly to the module once it is mounted within the cover case. The cover case must have sufficient strength such that any external forces are not transmitted directly to the module.
- (5) It is recommended that you maintain a gap between the display module and the rear chassis so as to avoid any mechanical stress being passed to the module.

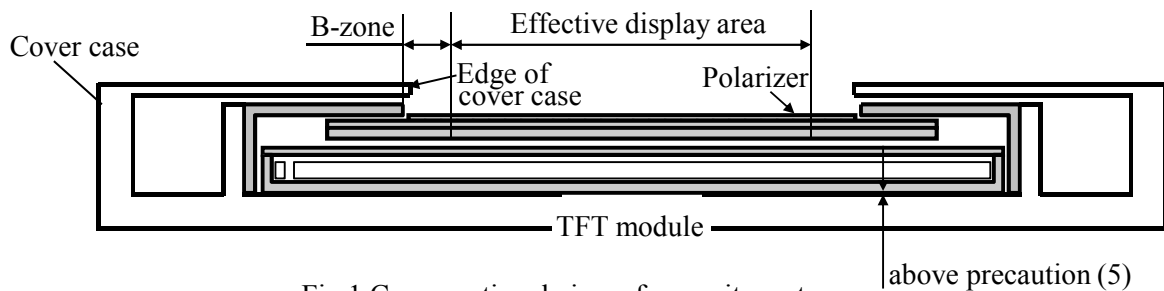


Fig.1 Cross sectional view of a monitor set

- (6) The edge of the cover case should be positioned with more than a 1mm overlap from the edge of the module's upper frame.
- (7) A transparent protective plate should be added to the front of the display in order to protect both the polarizer and TFT cell. The transparent protective plate should have sufficient strength such that the plate can not be deformed, due to external forces, and touch the module. Polarizer surface hardness is 2H.
- (8) Materials containing acetic acid and chlorine should not be used for the cover case nor for other parts which are positioned in close proximity to the module. This is because the Acetic acid will attack the polarizer, whilst the chlorine will attack the electric circuits by way of electro-chemical reaction.
- (9) The front polarizer on the TFT cell should be handled carefully, due to its softness, and must not be touched, pushed or rubbed with glass, tweezers or anything harder than an HB pencil lead.  
The surface of the polarizer should not be touched nor rubbed with bare hands, greasy or dusty clothes.
- (10) If the surface of the polarizer becomes dirty it should be gently wiped using an absorbent cotton (Traysee CC clean cloth), chamois or other soft material, slightly dampened with petroleum benzene. IPA (isopropyl alcohol) is recommended to clean away the traces of adhesive which is used to attach the front/rear polarizers to the TFT cell. Other cleaning chemicals such as acetone, toluene and alcohol should not be used to clean adhesives because they cause chemical damage to the polarizer.
- (11) Saliva or water drops should be immediately wiped off. Otherwise, the affected portion of the polarizer may become deformed and its color may fade.
- (12) The module should not be opened or modified, under any circumstances, as this may cause it to malfunction.

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- (13) The metallic bezel of the module should not be handled with bare hand or dirty gloves. Otherwise, the color of the metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls whilst the module is handled during incoming inspection and production assembly processes.
- (14) Please pay attention to the packing and handling not to apply strong Z axis vibration. Because during our vibration test, of course we didn't have any functional failure, but we observed very tiny bright dots (within spec though) at Z axis direction.

**10.2 Precaution to operation**

- (1) Spike noise could result in the mis-operation of this module. The level of spike noise should be as follows:  
 $-200\text{mV} \leq \text{over- and under- shoot of VDD} \leq +200\text{mV}$   
VDD including over- and under- shoot should not exceed the absolute maximum ratings.
- (2) Optical response times, luminance and chromaticity depend on the temperature of the TFT module.
- (3) Sudden temperature changes may cause dew on and/or in the module. Dew can cause damage to the polarizer and/or electrical contacting areas of the module. Dew causes fading of the image quality.
- (4) Using screen saver is recommended that it avoids any potential of sticking image.
- (5) This module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by the system manufacturers. Grounding and shielding methods may be effective to minimize such interference.
- (6) Noise may be heard when the back-light is operated. If necessary, sufficient suppression should be done by the system manufacturers.
- (7) The module should not be connected or disconnected whilst the main system is operating.
- (8) Connecting or disconnecting the I/F cables, whilst the power and data signals are present, could result in permanent damage to the module. The I/F connectors should only be connected and disconnected after the power supply and data signal have been turned off.
- (9) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.

**10.3 Electrostatic discharge control**

- (1) This module consists of a TFT cell and electronic circuits with CMOS-ICs, which are very susceptible to electrostatic discharge. Persons who are handling the module should be grounded through adequate methods such as a wrist band. I/F connector pins should not be touched directly with bare hands.
- (2) The polarizer protective film should be removed slowly so as to avoid an excessive build-up of electrostatic charge.

**10.4 Precaution to strong light exposure**

- (1) The module should not be exposed to strong light. Otherwise, characteristics of the polarizer and color filter, may be degraded.

**10.5 Precaution to storage**

When modules are stored, for long period's of time, the following precautions should be taken:

- (1) Modules should be stored in a dark place. It is prohibited to apply direct sunlight or fluorescent light during storage. Modules should be stored between 0 to 35°C at normal humidity (60%RH or less).
- (2) The surface of the polarizer should not come into direct contact with other objects.  
It is recommended that modules should be stored in the original Japan Display shipping box.

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### **10.6 Precaution to handling protection film**

- (1) The protective film for polarizers should be peeled off slowly and carefully by people who are electrically grounded with adequate methods such as wrist bands. Also ionized air should be blown over the module during the peeling process.  
Dust on the polarizer should be blown off gently using an ionized nitrogen gun.
- (2) The protective film should be peeled off carefully to avoid it rubbing on the polarizer. If the film rubs together with the polarizer it is possible that a small amount of adhesive may remain on the polarizer.
- (3) The module with protective film should be stored under the conditions explained in 9.5 (1). However, in case's where the storage time is excessive, some adhesive may remain on the polarizer even after the protective film has been removed. In the case where a module is stored at higher temperatures and/or higher humidity, adhesive may remain on the polarizer. Any remaining adhesive may cause non-uniformity of the displayed image.

### **10.7 Safety**

- (1) Since both the TFT cell is made of glass, handling of any broken module's should be carried out with the utmost care so as to avoid any injury. Hands which have come into direct contact with liquid crystal material should be washed immediately and thoroughly.
- (2) The module should not be taken apart during operation so that back-light drives by high voltage.

### **10.8 Use restrictions and limitations**

- (1) In no event shall Japan Display, Ltd. be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility there of in advance. These limitations apply to all causes action in aggregate, including without limitation breach of contract, breach of warranty, negligence, strict liability, misrepresentation and other torts.
- (2) This product is not authorized for military applications or other applications which pose a significant risk of personal injury.

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