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奇菱科技 CHILIN

Specifications (Preliminary)

Doc. No1.

Customer	
Customer Type	
CLT Type	**TX6A11/TX6A12 42” Full HD_60Hz**
Date	**2010-09-02**
Revision number	**Ver. 1**
Code	**10190163-A0/10190168-A0**
Open Cell Type	**CMI V420H2-P01**

Customer Approved

CHILIN TECHNOLOGY				
QRA	**Manufacture**	**Approved**	**Checked**	**Design**
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Revision History

Version	Date	Page	Section	Description
0	2010/08/31	All	All	
1	2010/9/2	18	1.4.2.2	Modify Input Voltage Min. & Max Value

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1.0 APPLIED TYPE

This model adopts : CMI V420H2-P01 (OPEN CELL）.

Therefore, please refer to specifications of 42” Full HD TFT-LCD module for a driving method and an electrical characteristic of cell.

1.1 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42" diagonal)	mm	
Bezel Opening Area	937.2(H) x 530.2(V)	mm	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Sub-Pixel Pitch	0.1615(H) x 0.4845(V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Normally Black	-	
Surface Treatment	Anti Glare + 3H	-	

1.2 MECHANICAL SPECIFICATIONS

Item		Typ.	Unit	Note
Module Size	Horizontal(H)	973.2	mm	
	Vertical(V)	566.2	mm	
	Depth(D)	19.2	mm	To Frame Rear
Weight		8	Kg	

1.3 ABSOLUTE MAXIMUM RATING

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	℃	(1)
Operating Ambient Temperature	TOP	0	50	℃	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta≦40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta＞40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber.

Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

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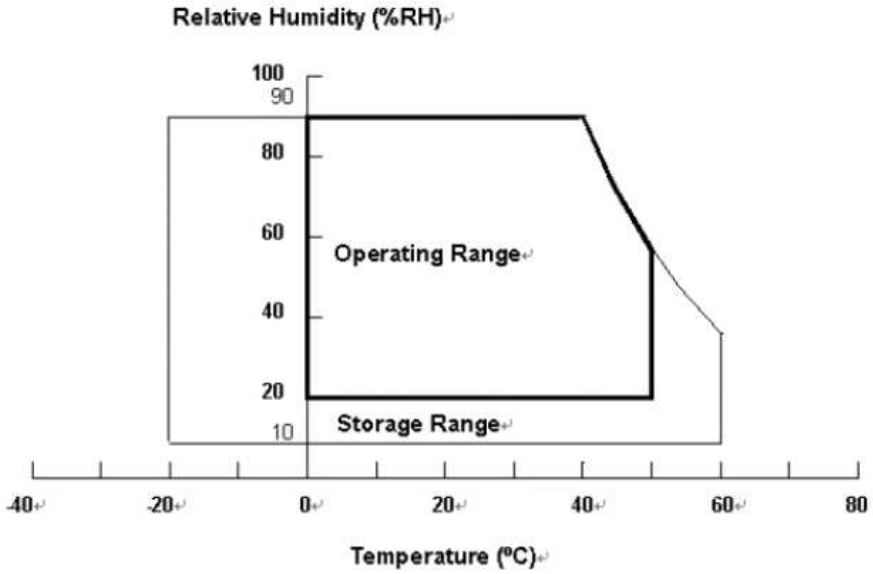
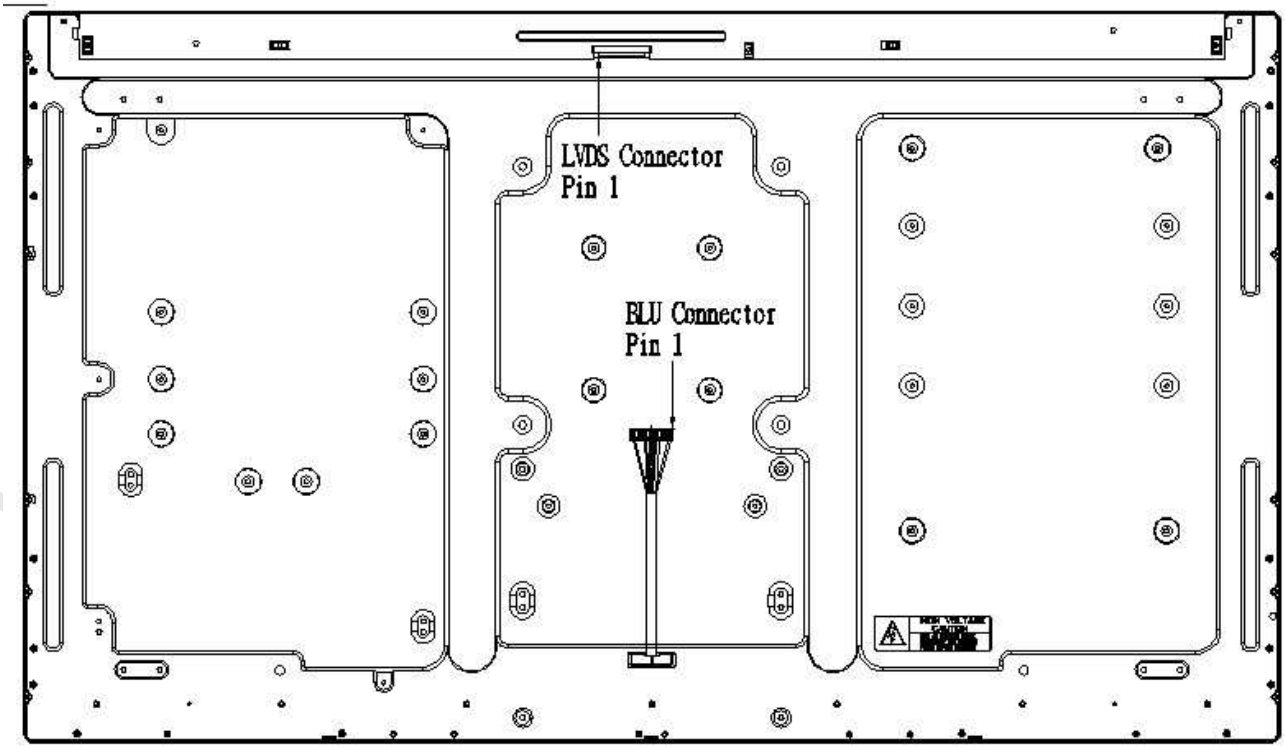


Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

1.4 LCM MODULE INTERFACE DEFINITION



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1.4.1 CELL INFORMATION

1.4.1.1 REFERENCE TO CMI V420H2-P01 SPECIFICATION

1.4.1.2 LVDS INPUT CONNECTOR PIN ASSIGNMENT

Pin	Name	Description	Note
1	GND	Ground	
2	SCL	Series clock input	
3	SDA	Series data input	
4	N.C.	No Connection	(2)
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3), (5)
8	N.C.	No Connection	(2)
9	ODSEL	Overdrive Lookup Table Selection	(4), (6)
10	TST_PGM	Write protect input	
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(7)
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input	(7)
20	ECLK+	Even pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(7)
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(7)
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input	(7)
36	OCLK+	Odd pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(7)
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	

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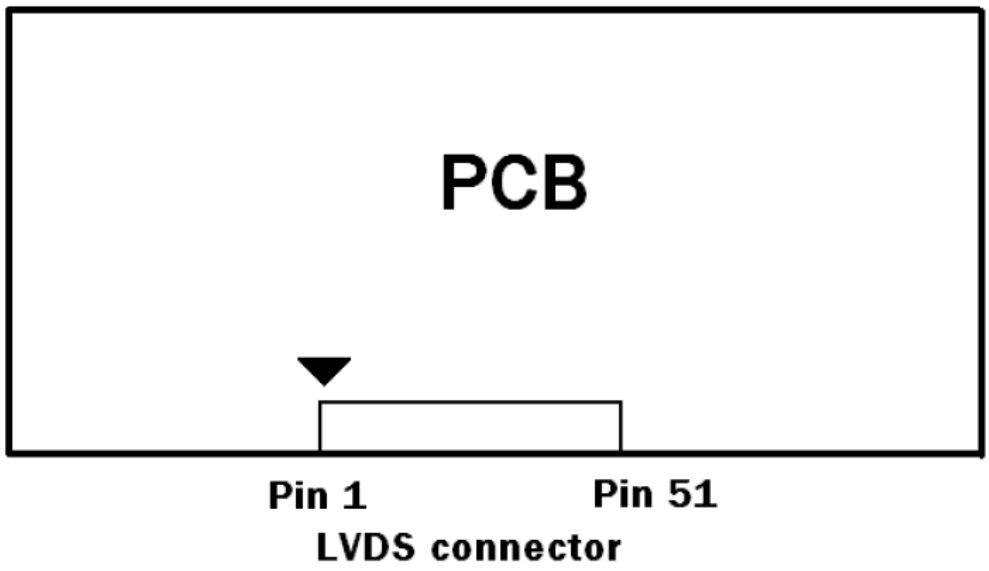
51	VCC	+12V power supply	

Note (1) Using connector: FI-RE51S-HF or equivalent

Mating LVDS transmitter: THC63LVDM83A (LVDF83A)

LVDS connector pin order defined as follows



Note (2) Reserved for internal use. Please leave it open.

Note (3) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

Low = Open or connect to GND, High = Connect to +3.3V

ODDEL	Note
L or open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

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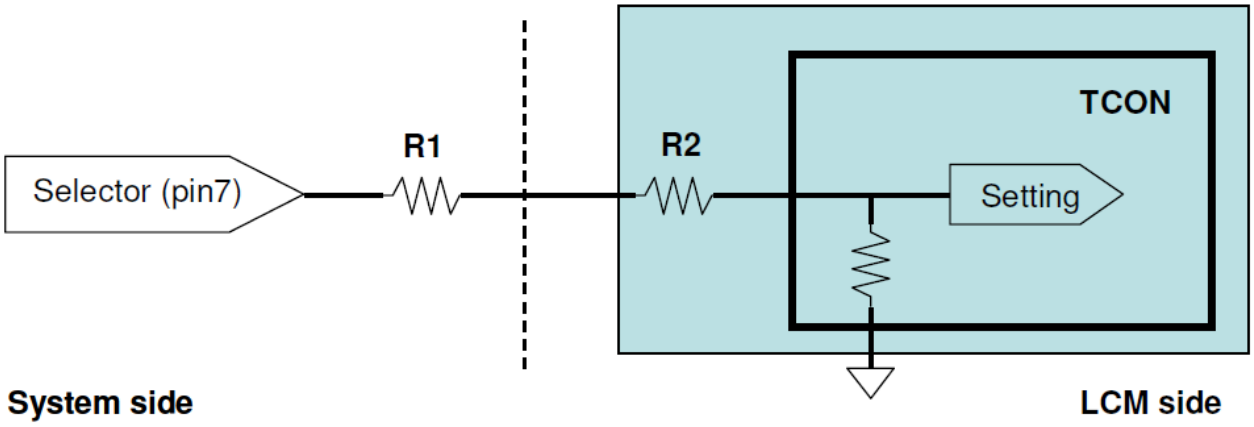
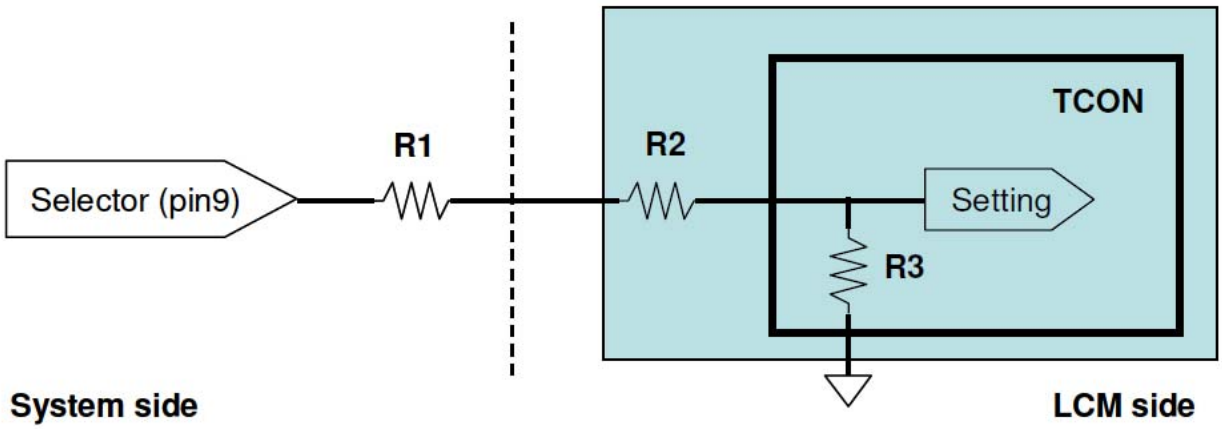


Note (6) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should



Note (7) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

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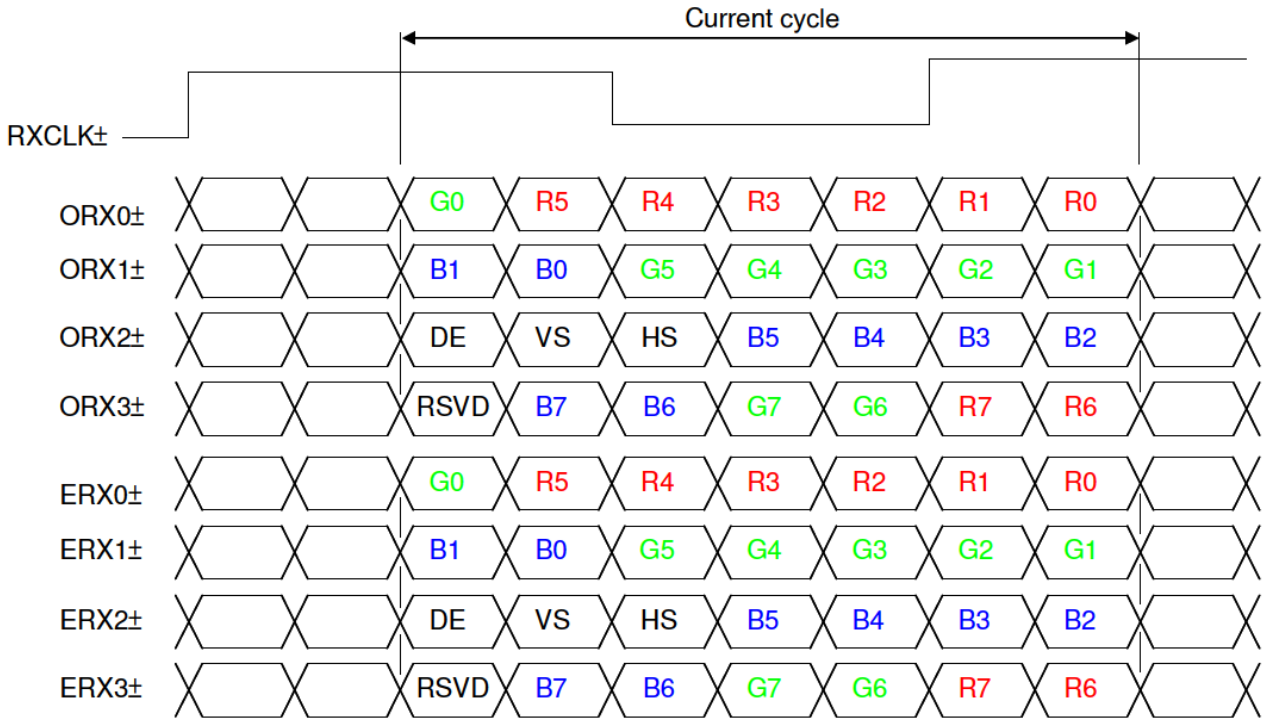
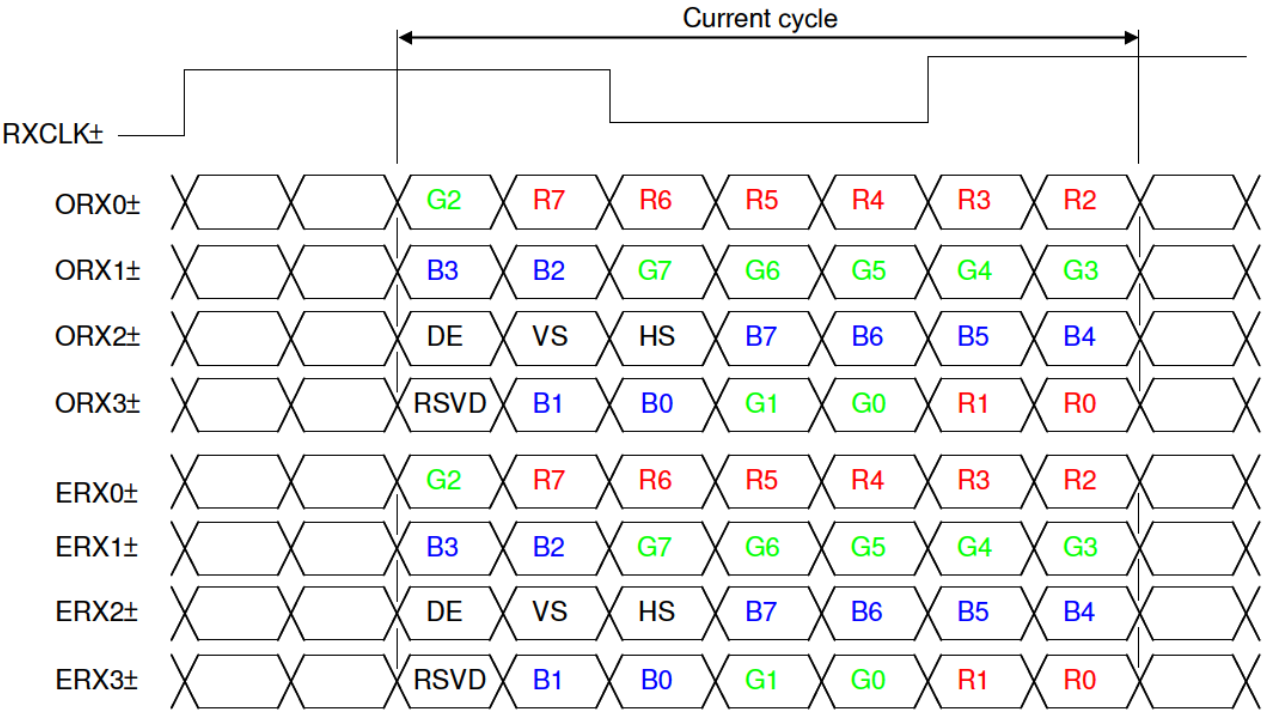
1.4.1.3 LVDS INTERFACE

VESA LVDS format: (SELLVDS pin=L)



JEDIA LVDS format: (SELLVDS pin=H)



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R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

1.4.1.4 ELECTRICAL CHARACTERISTICS FOR LVDS RECEIVER

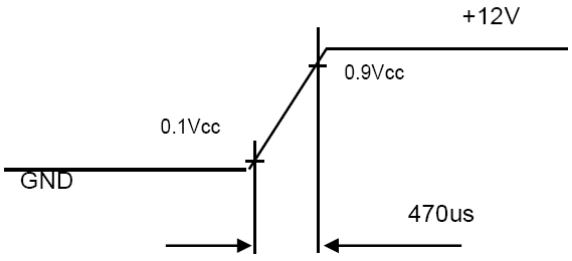
Ta = 25 ± 2 ºC

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	3.5	A	(2)
Power Supply Current	White Pattern	-	-	0.98	-	A	(3)
	Horizontal Stripe	-	-	0.98	1.2	A	
	Black Pattern	-	-	0.51	-	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:

Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

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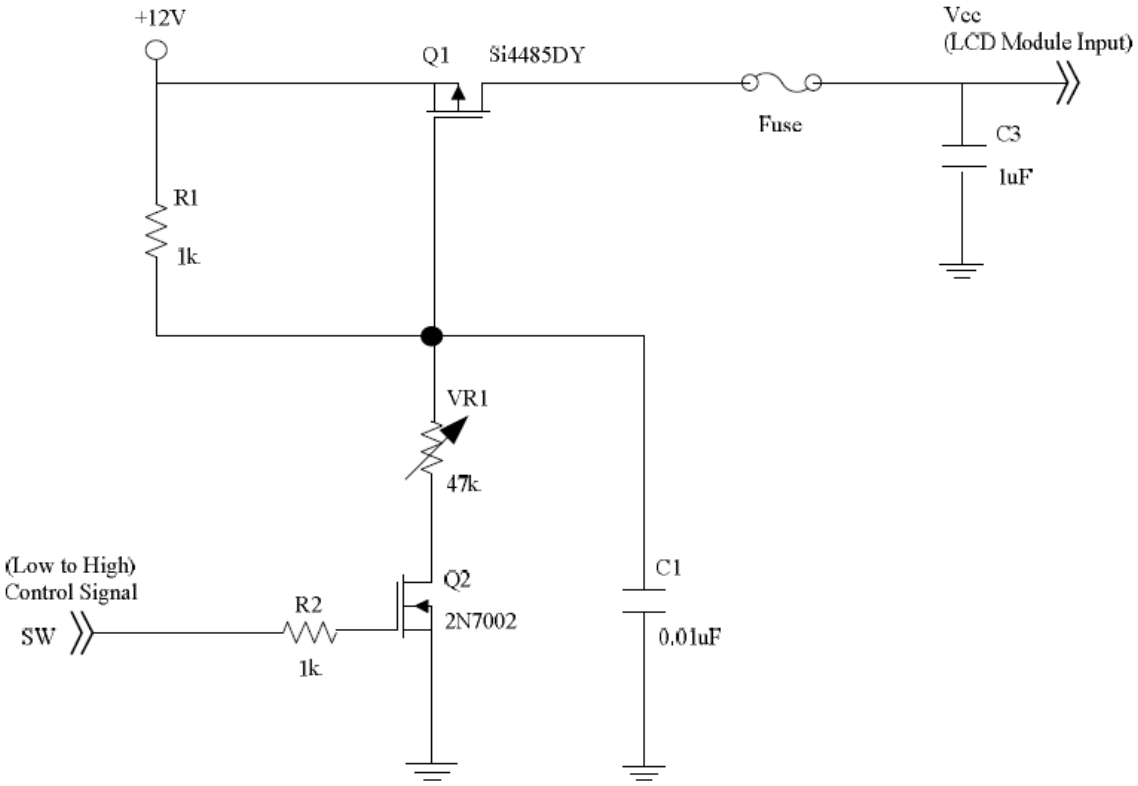
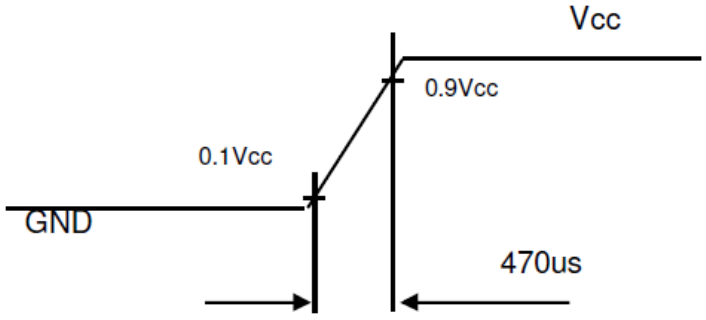


Vcc rising time is 470us



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Note (3) The specified power supply current is under the conditions at Vcc = 12V, Ta = 25±2°C, fv = 60Hz, whereas a power dissipation check pattern below is displayed.

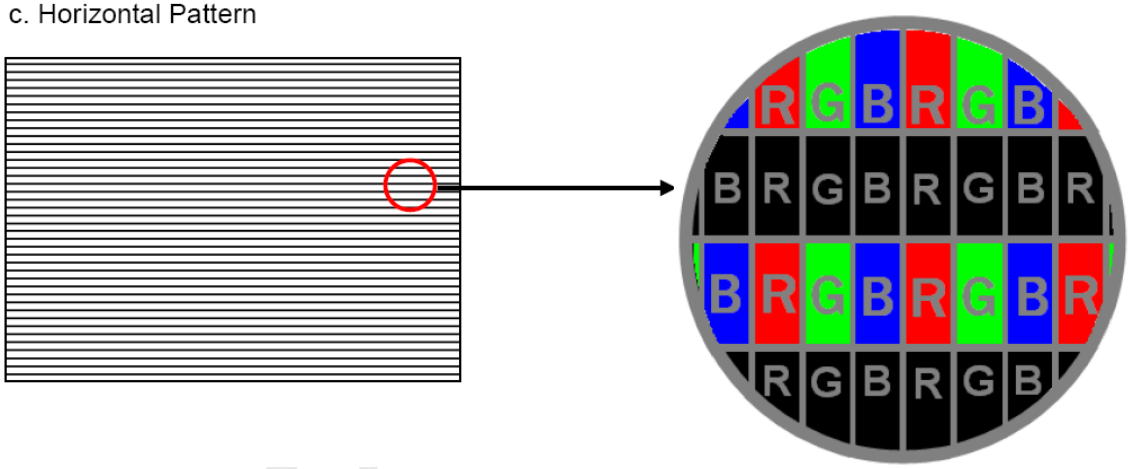
a. White Pattern

Active Area

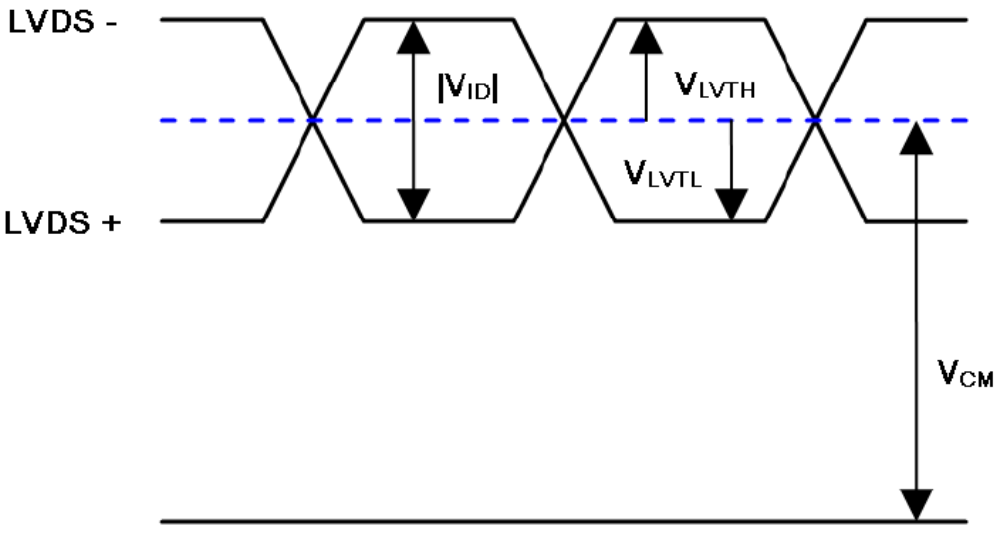
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



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1.4.1.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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1.4.1.6 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25±2℃)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin}(=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	Ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

Note(1) Please make sure the range of pixel clock has follow the below equation:

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

Note(2) This module is operated in DE only mode and please follow the input signal timing diagram below:

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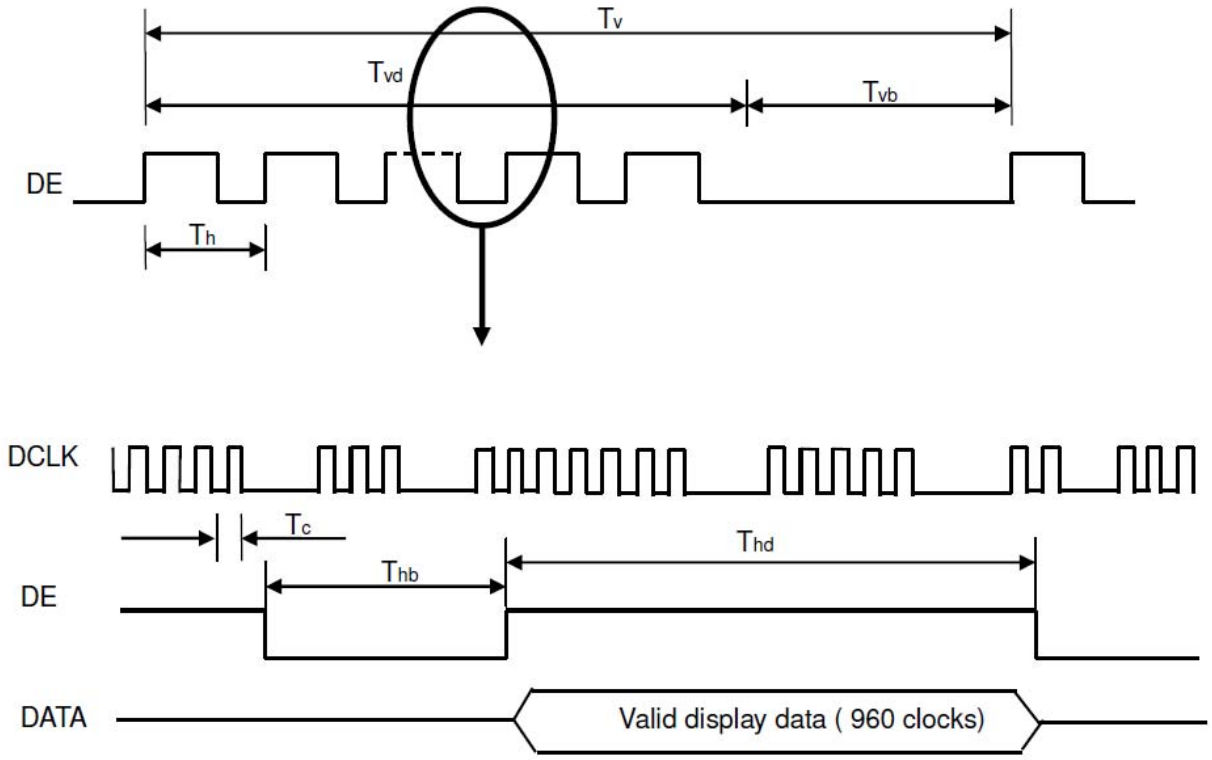
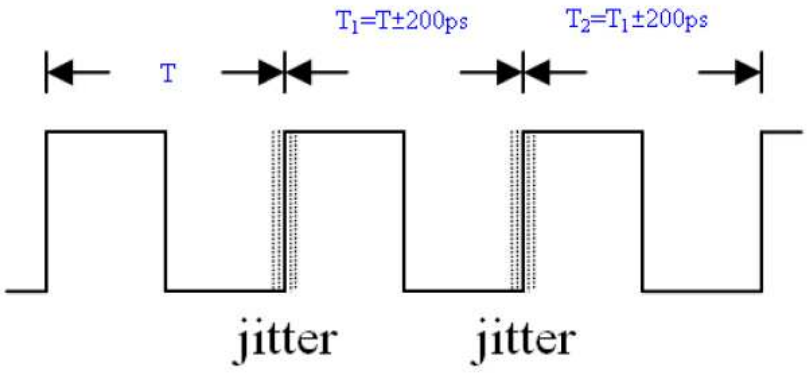


Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T1 – TI



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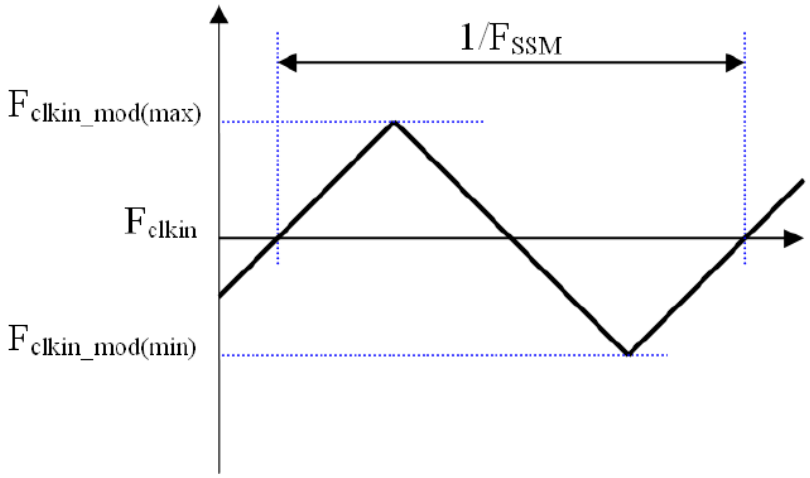
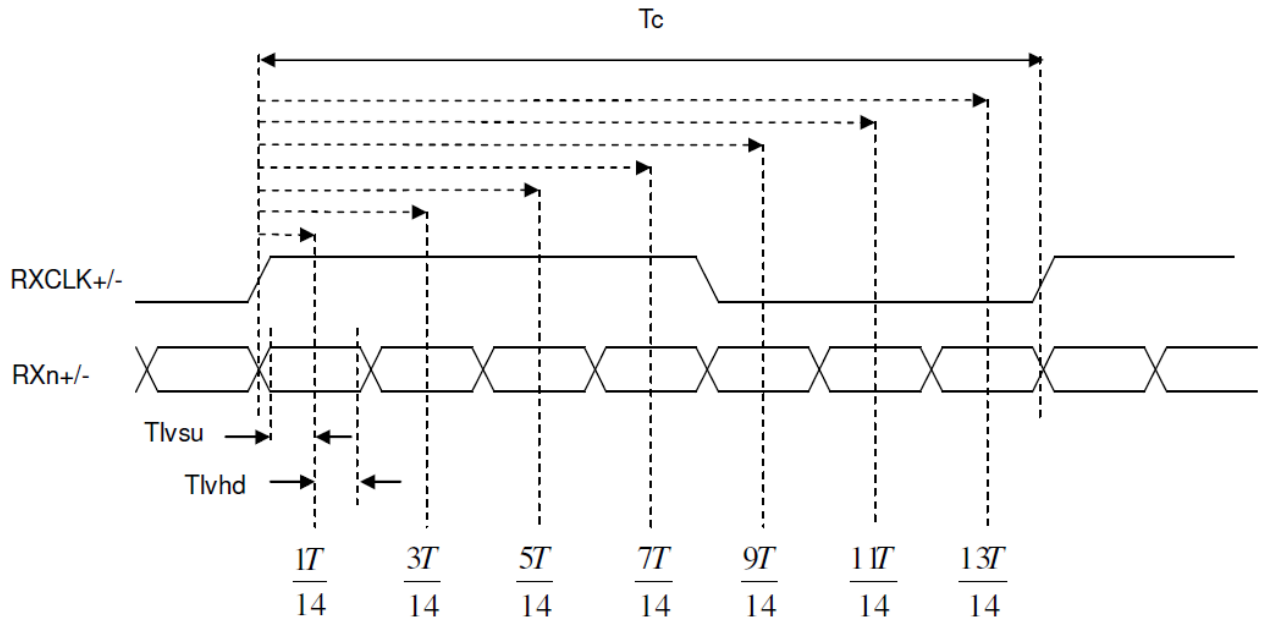
Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) : (ODSEL) = H/L or open for 50/60Hz frame rate. Please refer to 4.1 for detail information

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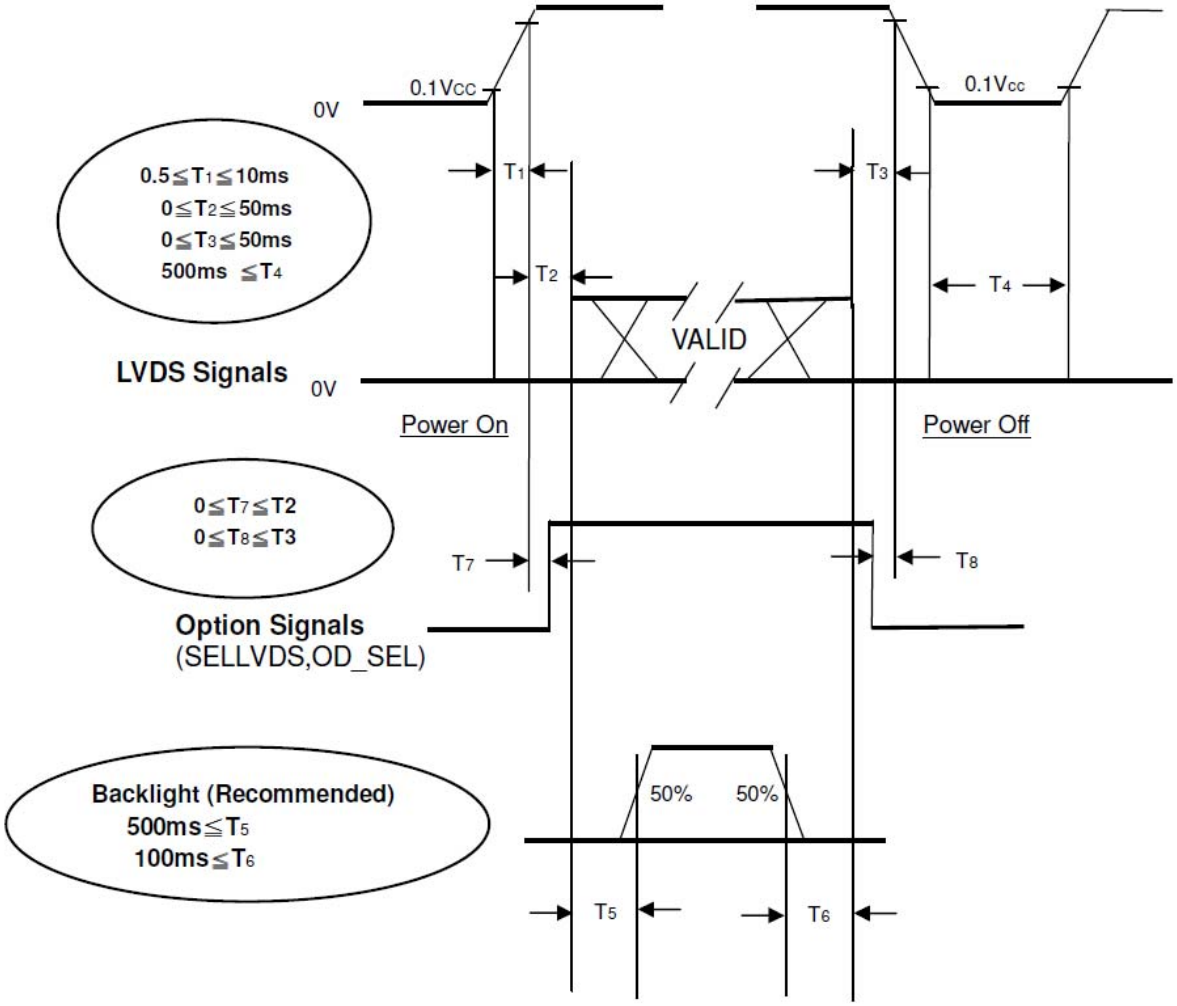
1.4.1.7 CELL ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

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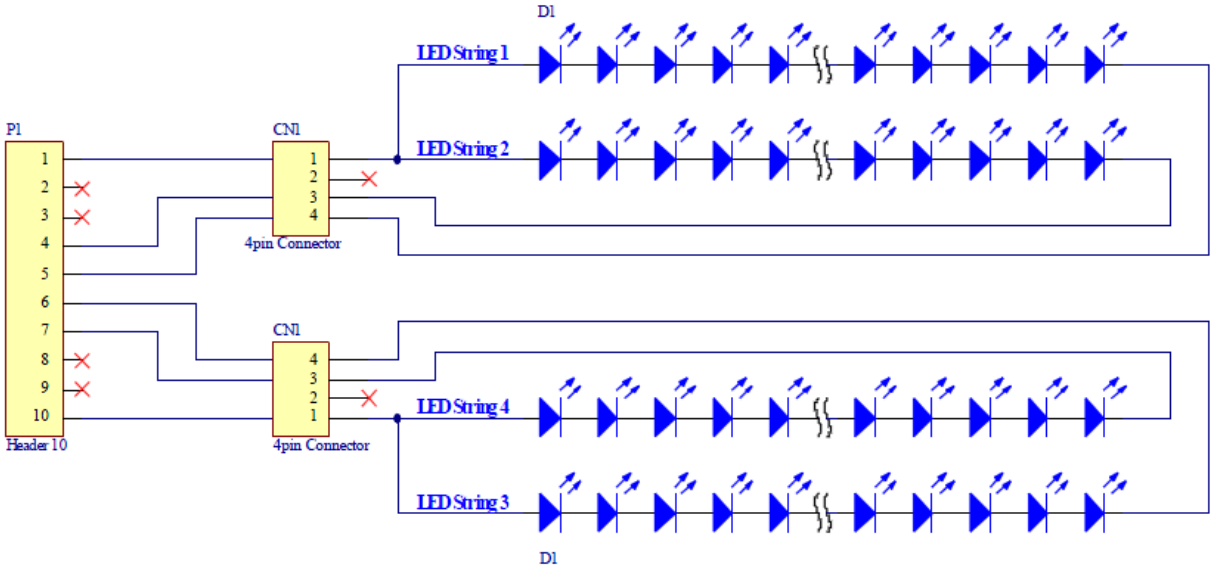
1.4.2 LED BACKLIGHT MODULE

1.4.2.1 LED BACKLIGHT LIGHT ON CONNECTOR PIN DEFINITION AND SCHEMATIC



INPUT Connector : JST PHR-10 or equivalent

Pin No.	Symbol	Description
1	LED+	Anode(+) of LED string1 and 2
2	NC	No Connection
3	NC	No Connection
4	LED2-	Cathode(-) of LED string2
5	LED1-	Cathode(-) of LED string1
6	LED3-	Cathode(-) of LED string3
7	LED4-	Cathode(-) of LED string4
8	NC	No connection
9	NC	No connection
10	LED+	Anode(+) of LED string3 and 4

1.4.2.2 LED BACKLIGHT LED RATING SPECIFICATION

Ta=25°C

Item	Min.	Typ.	Max.	Unit	Remark
Input Voltage	99.0	-	122.1	V	Constant Current = 125mA
Input Current (Per String)	120	125	130	mA	

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1.4.3 LED ABSOLUTE MAXIMUM RATING (ELECTRICAL)

Ta=25°C

Item	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Forward Voltage	V_F	3.0	-	3.6	V	IF=120mA
LED Forward Current	I_F		120	150	mA	
LED Reverse Voltage	V_R		5		V	
LED Power Dissipation	P_D		600		mW	
ESD (HBM)	-	1500	-	-	V	(2)
ESD (MM)	-	150	-	-	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Static electricity or surge voltage can damage the LEDs. All equipment, machinery and the treatment persons must be properly grounded. It is recommended to use a wristband or anti-electrostatic glove when handling the LED. And don't touch interface pin directly.

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2.0 OPTICAL SPECIFICATIONS

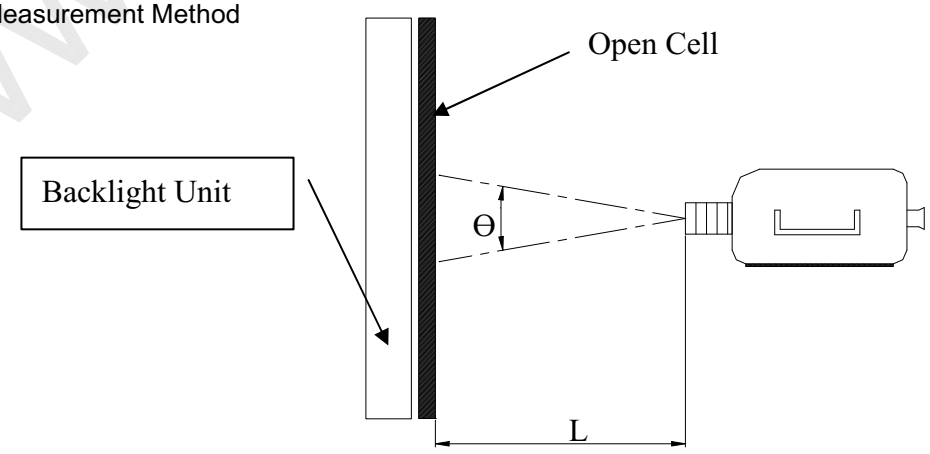
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°,θy=0° Viewing Normal Angle	4000	5000	—	—	(1), (2), (4), (6)
Response Time		Gray to Gray		—	6.5	12	ms	(1), (2), (5), (6)
Luminance		L0		350	380	—	cd/m^2	(1), (2), (6)
Uniformity		△L		70	75	—	%	(1), (2), (7)
Color Chromaticity	White	Wx		Typ –0.03	0.279	Typ +0.03	—	(1), (2), (6)
		Wy			0.292			
	Red	Rx			0.637		—	
		Ry			0.335			
	Green	Gx			0.328		—	
		Gy			0.641			
	Blue	Bx			0.145		—	
		By			0.046			
Viewing Angle	Horizontal	θx+	Luminance(θ) Equal to 1/3 L0	47	50	—	Deg.	(1), (2), (3), (6)
		θx-		47	50	—		
	Vertical	θy+		37	40	—		
		θy-		37	40	—		

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.

Any outstanding stain (or mura) and/or any outstanding difference of Chromaticity between any parts of the active area will cause Backlight Assembly and LCM to be rejected.

Note (2) Measurement Method



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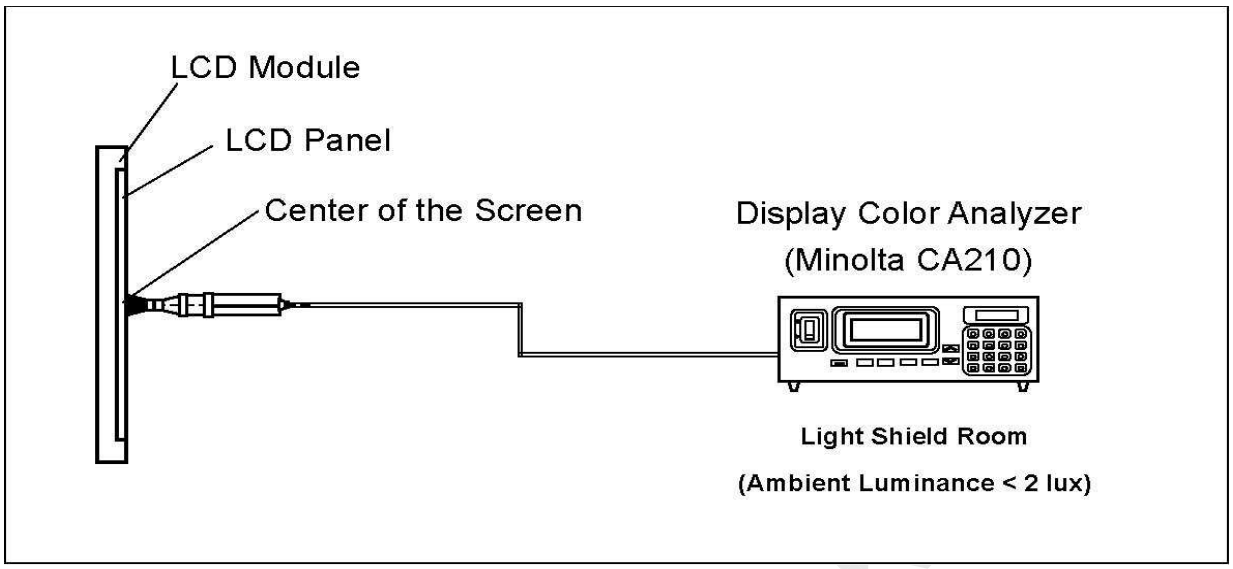
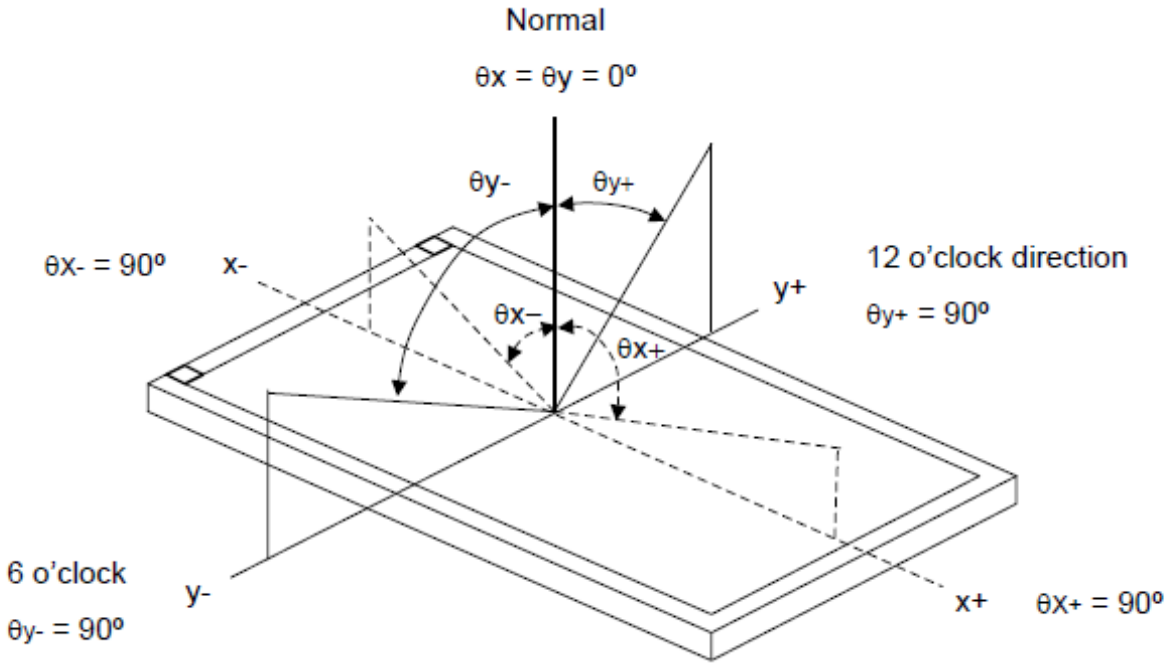


E / Item	CA210
Angle Θ	±2.5°
Distance L	3cm

Note (3) Definition of Viewing Angle(θx, θy):



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Note (4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255/L0

L1023: Luminance of gray level 255

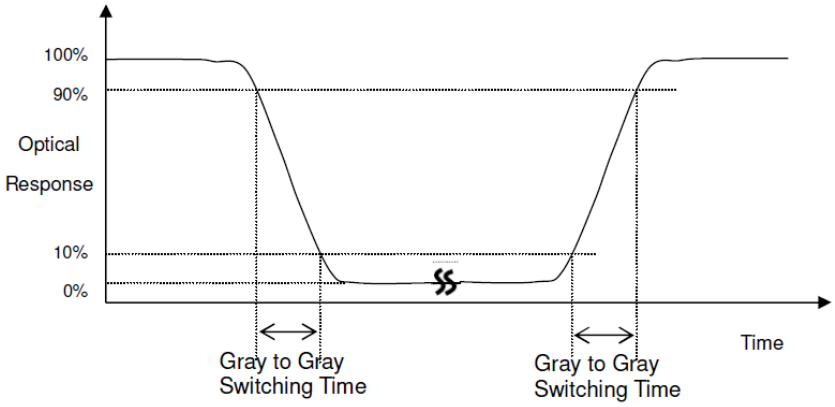
L0: Luminance of gray level 0

CR = CR(0), where CR(X) is corresponding to the Contrast Ratio of the point X at Figure in Note(7)

Note (5) Definition of Gray to Gray Switching Time:

The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.



Note (6) This shall be measured at center of the screen.

Note (7) Definition of White Uniformity (△W):

White uniformity is defined as the following with nine points of the white luminance

△W = Minimum [L (0) ~ L (8)] / L(0)

where L (X) is referred to the white luminance of the point X in the figure below.

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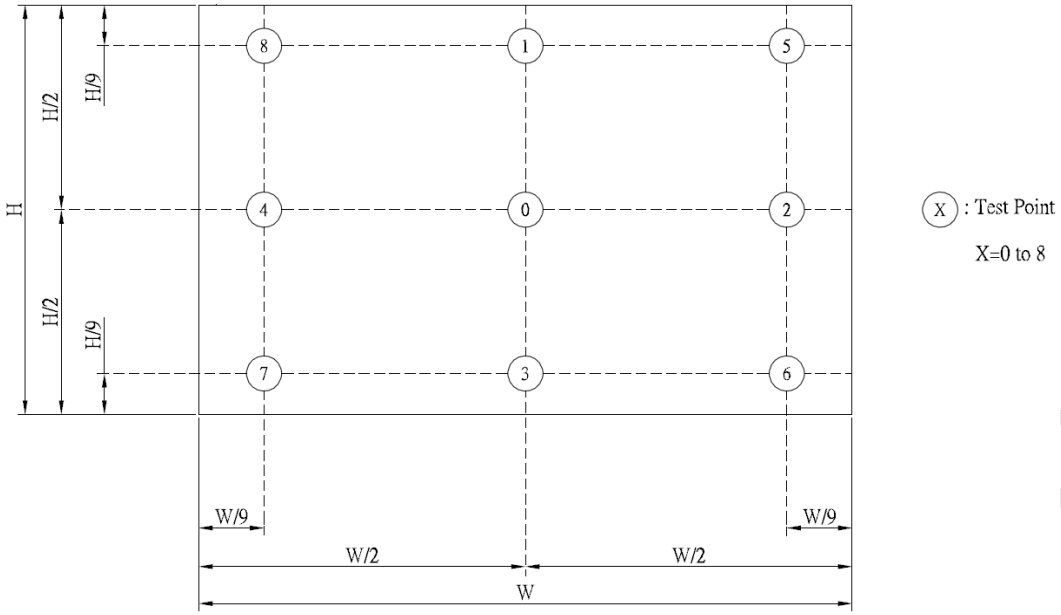

Note (8)

Contrast ratio and response time is corresponded to the original open-cell specification of V420H2-P01 defined by CHIMEI INNOLUX.

3.0 RELIABILITY TEST ITEM

	Test Items	Q'ty	Condition
1	High Temperature Operation	3	50℃，300hrs
2	High Temperature And High Humidity Operation	3	50℃/ 80%RH，300hrs
3	ESD Contact Mode	3	'+/-8,10KV, 1sec/cycle, class C , 2hrs
4	ESD Air Mode	3	'+/-15KV, 1sec/cycle, class C , 2hrs
5	Mechanical Shock (non-operation)	3	50G, 11ms, half sine wave, 1 times for each direction of ±X,±Y, 35G, 11ms, half sine wave, 1 times for each direction of ±Z
6	Panel Vibration	3	10-200Hz, 1G, 30mm is Max., 30min/cycle, 1cycles for each X,Y,Z.

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4.0 PACKING

4.1 PACKING SPECIFICATIONS

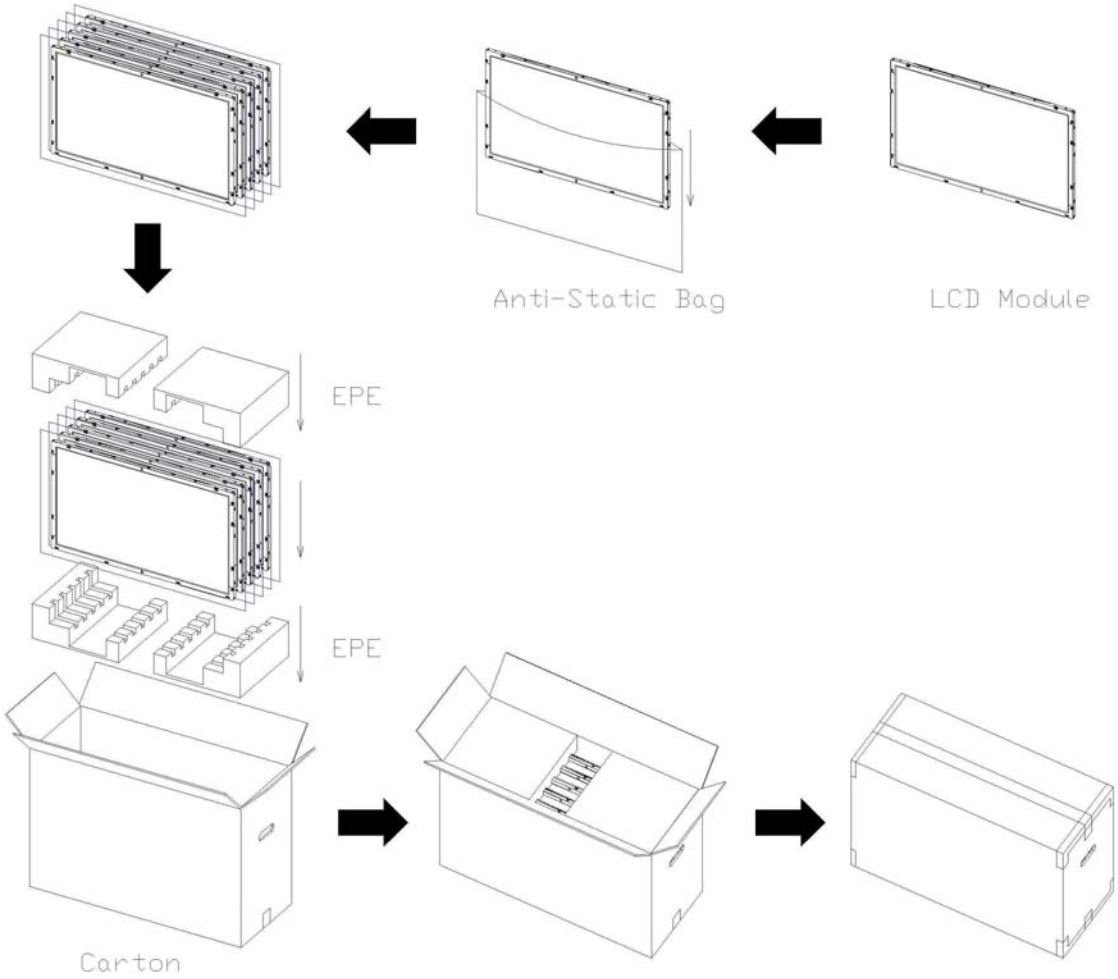
Carton SPECIFICATIONS

（1） 5 LCD modules / 1Box

（2） Box dimensions : 1090（L）× 355（W）× 705（H）mm

（3） Weight : approximately : 42.9 kg (5 modules per box，packaging materials including pallet)

4.2 PACKING METHOD



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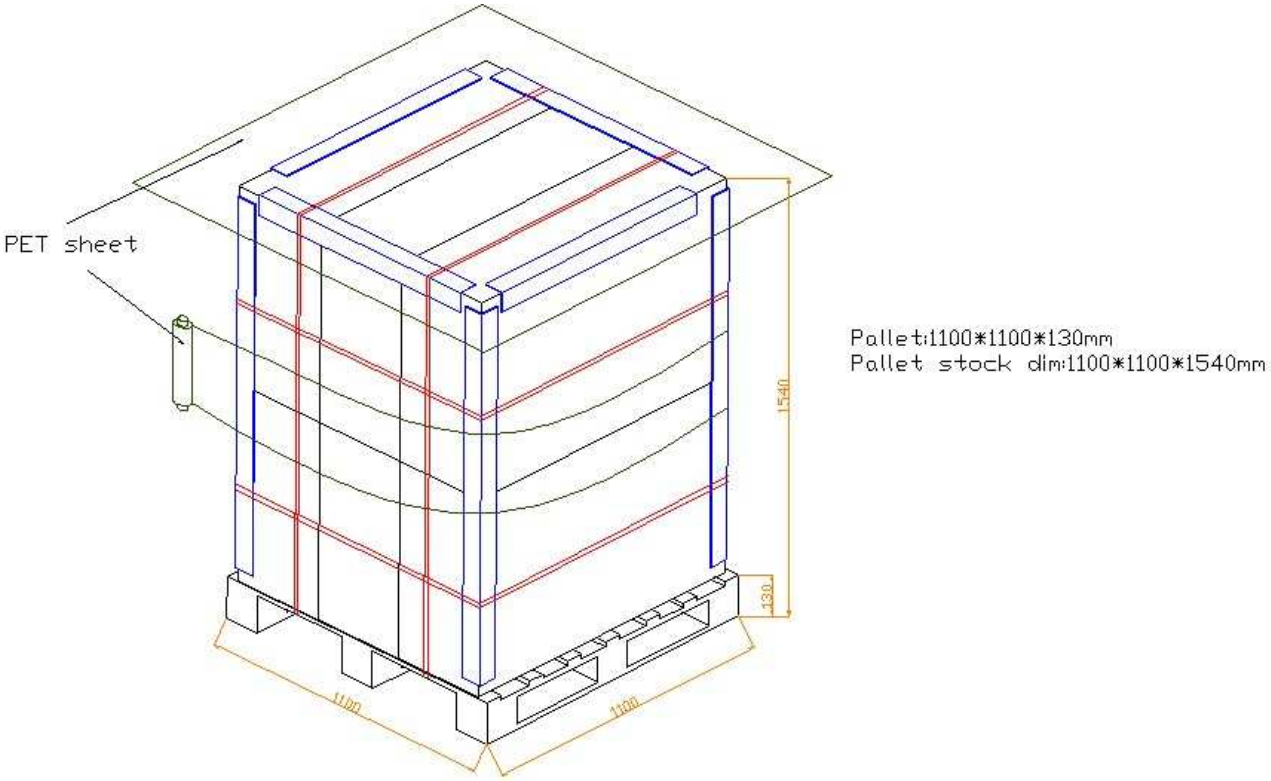
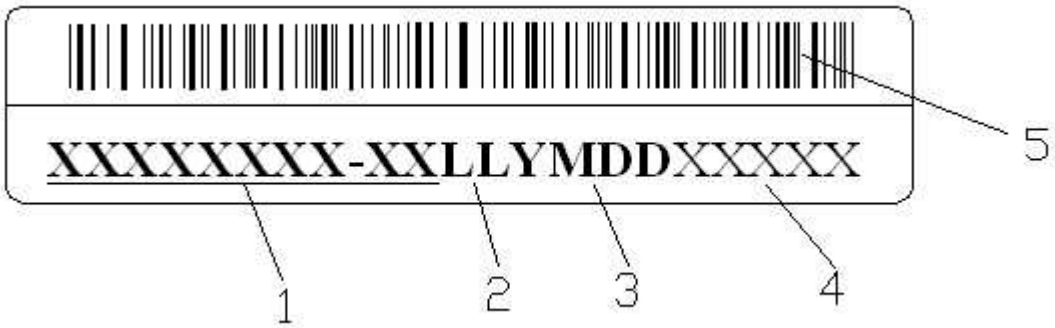


4.3 PACKAGING LABEL

The barcode nameplate is pasted on each backlight as illustration, and its definitions are as following explanation.



1 : LCM Part No : 10190163-A0, 10190168-A0
2 : Make Spaces: C1:CLT , C2:LS , C3:LMO , C4:LCO
3 : Year 2010 : A, 2011 : B, 2012 : C,…… not include I,O,U,V
Month : 1 2 3 4 5 6 7 8 9 X Y Z
Date : 01,02,03,04 ~30,31
4 : Serial No 00001~99999 (Reset every day)
5 : Barcode Format (CODE 93)

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5.0 PRECAUTIONS

5.1 MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because **they cause may chemical damage to the polarizer.**

(8) Wipe off saliva or water drops as soon as possible. Their long time contacting with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

5.2 OPERATING PRECAUTONS

(1) The device listed in the product specification sheets was designed and manufactured for TV application

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer..)

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to **polarizer or electrical contacted parts. And after fading condensation, smear or spot will be occurred.**

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

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5.3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

5.4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

5.5 STORAGE

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

5.6 HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

6.0 LOT NO. GENERATION

According to the customer supply specification

7.0 SALES REGION

TX6A11(10190163-A0) Sales region：Only in China

TX6A12(10190168-A0) Sales region：Worldwide except Japan

8.0 MECHANICAL CHARACTERISTICS

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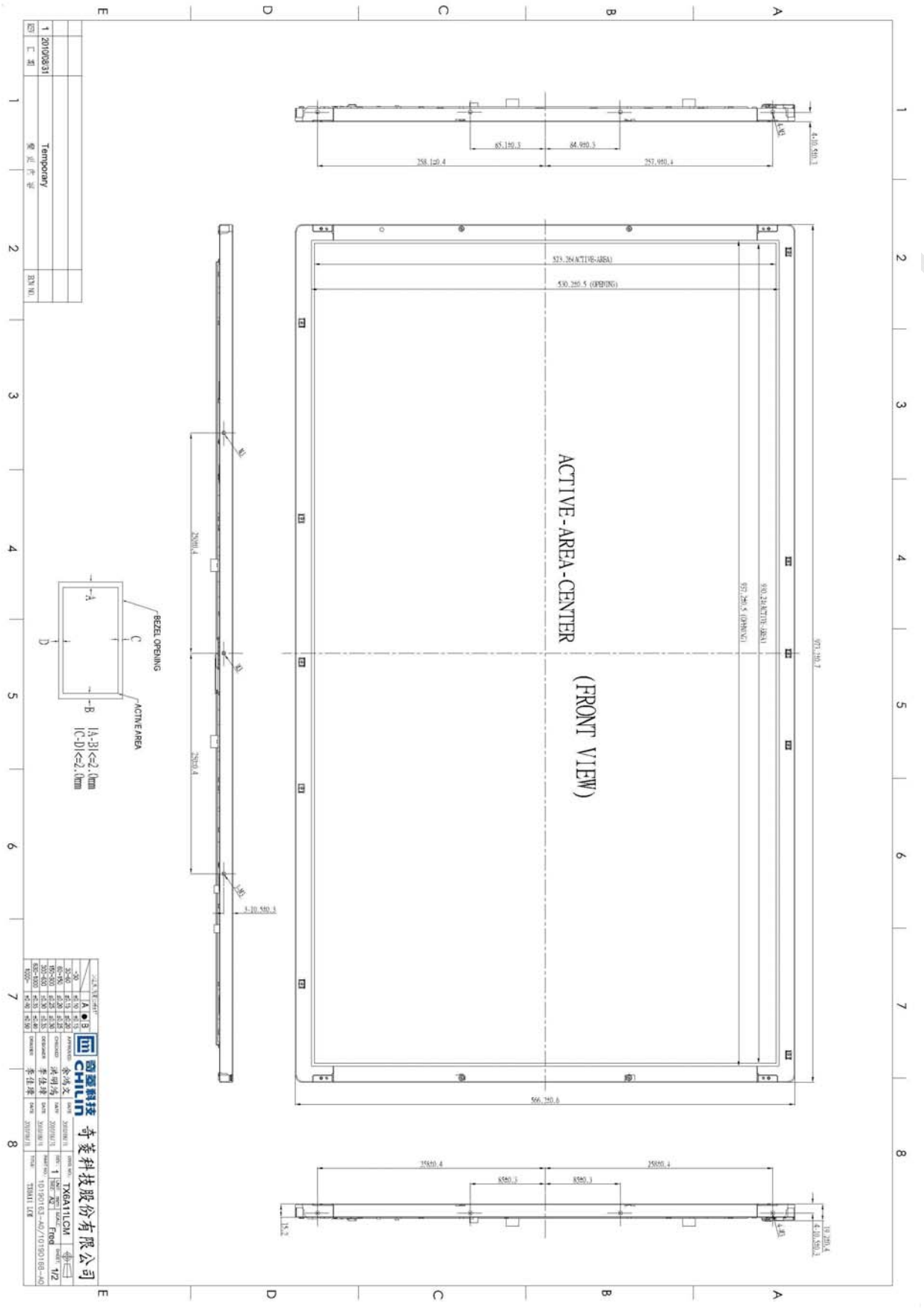

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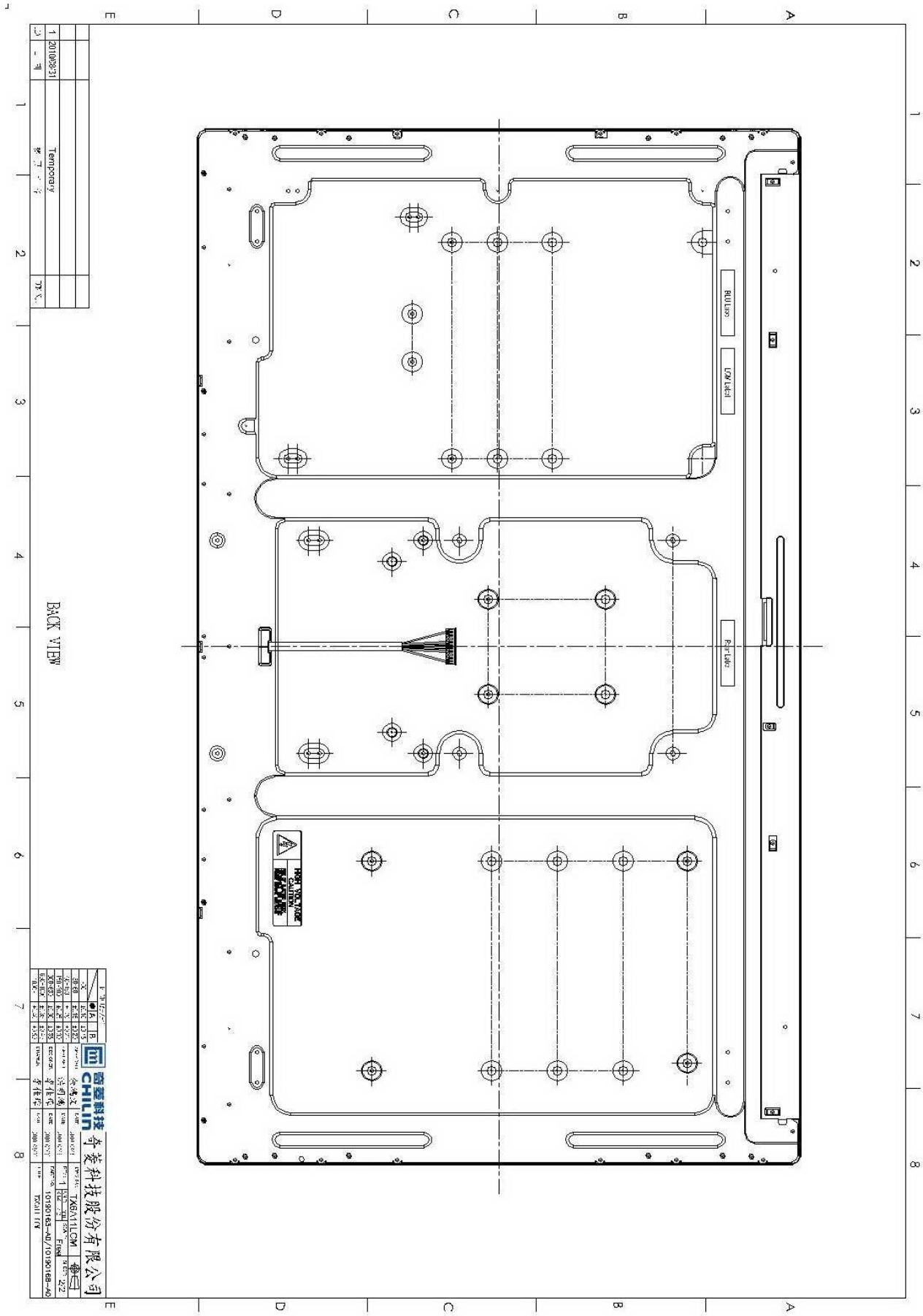

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