QT1F-*Plus* Device
Quad T1 Framer-*Plus*
TXC-03103C

DATA SHEET

FEATURES

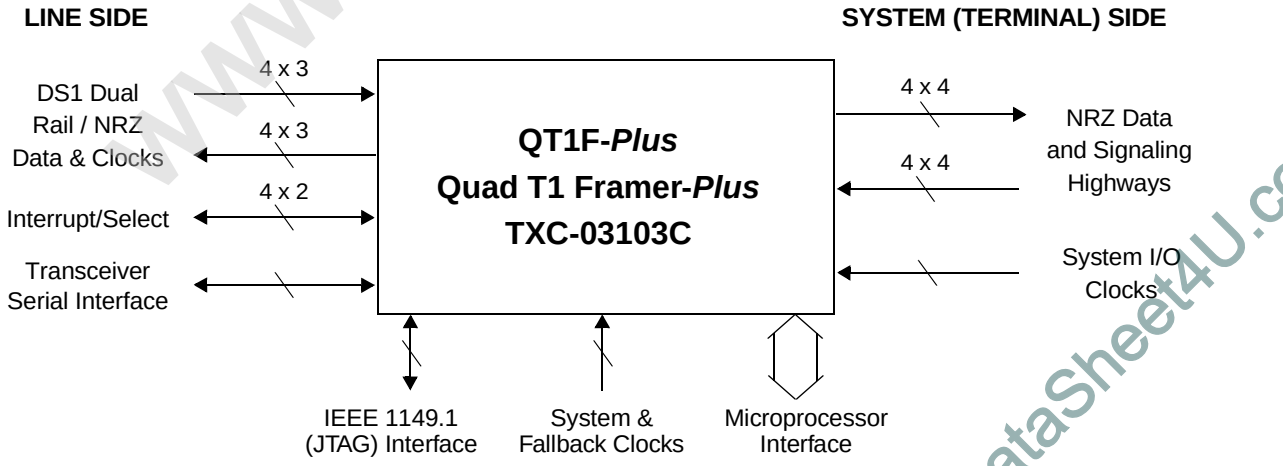
- D4 SF, ESF (including HDLC Link support), and transparent framing modes
- Encodes/decodes AMI/B8ZS and forced ones density line codes
- Fractional T1 gapped clock
- Monitor function for frame pulse, clock and data
- Two-frame slip buffers in both receive and transmit directions
- Supports channel associated and robbed-bit signaling (enabled or processor forced on a per DS0 basis)
- Detects and forces Yellow and AIS alarms; detects OOF, Severely Errored Frame, and Change of Frame Alignment, detects AIS-CI
- Detects, counts and forces line code errors (BPVs and excess zeros), CRC errors (ESF only), and frame bit errors
- Motorola/Intel compatible microprocessor interface
- One-second interrupt input latches counter values and line events into shadow registers
- Local, line remote, payload remote and DS0 channel loopbacks, per DS0 channel inversion
- Processor forcing/monitoring of DS0s for maintenance purposes
- Boundary scan capability (IEEE 1149.1)
- Single +3.3 volt or +5.0 volt power supply
- 128-pin low profile plastic quad flat package

DESCRIPTION

The QT1F-*Plus* (TXC-03103C) is a four-channel DS1 (T1, 1.544 Mbit/s) framer designed with extended features for voice and data communications applications. AMI, B8ZS, and NRZ line codes are supported with full alarm detection and generation per ANSI T1M1.3. The transmit and receive sections of each of the four framers are independent, with individual slip buffers to allow operation in a wide range of switching and transmission products. D4 SF and ESF modes are provided per ANSI T1.403-1998 and AT&T PUB 62411, with per DS0 signaling and DS0 data access and control via a Motorola/Intel-compatible microprocessor interface. For ESF applications, each framer supplies a full duplex HDLC/bit-oriented message controller, supporting back-to-back FDL messages in addition to onboard latching of all required performance parameters; minimal software overhead is required to support either ANSI T1.403-1998 or AT&T PUB 54016 protocols. Diagnostic, test, and maintenance functions are provided, including four loopback modes and boundary scan (IEEE 1149.1).

APPLICATIONS

- SONET/SDH terminal or add/drop multiplexers supporting DS1 byte synchronous operation
- DCS, digital central office or remote digital terminals
- T1 multiplexers
- T1 and fractional T1 CSUs
- ATM products with integrated DS1 interfaces
- LAN routers with integrated DS1 interfaces
- Multichannel DS1 test equipment
- Internet Access Equipment with T1 and Fractional T1 Interfaces



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QUAD T1 FRAMER-*PLUS* FEATURES

The Quad T1 Framer-*Plus* device (QT1F-*Plus*, TXC-03103C, see Note on next page) is a highly-featured four-channel DS1 (T1) framer for use in a wide variety of interface, transmission and switching applications. Four independent DS1 framers are provided in a single monolithic VLSI device using sub-micron CMOS technology. Powered from a single +5.0 volt supply, the four framers dissipate less than a watt typically. Powered from a single +3.3 volt supply, the four framers dissipate less than one third of a watt typically. The QT1F-*Plus* is provided in a rectangular 128-pin low profile plastic quad flat package. Its ambient operating temperature range extends from -40 °C to +85 °C.

The QT1F-*Plus* device has been designed to meet the latest industry standards, namely:

- ANSI T1.403-1998 and T1M1.3-005R1 (April 1993)
- Bellcore GR-499-CORE (Issue 1)
- AT&T Pub. 62411 (Dec. 1990) and Pub. 54016
- IEEE 1149.1- 1990, -1994
- MVIP (Multi-Vendor Integration Protocol)

The following features are independently selectable for each of the four DS1 framers:

Framing Modes:

- D4 SF (Superframe Format) - programmable for Fs, Ft or both frame bits
- ESF (Extended Superframe Format) - FPS bits with or without a valid CRC-6
- Unframed (bypass)
- T1DM and other SF modes with external logic

Line Codes:

- AMI
- B8ZS
- AMI with forced ones density
- NRZ (bypass)
- Selectable polarity (NRZ) and clock edges

Signaling:

- A, AB, 9-state AB signaling for ANSI T.403 Rob and limited support for SLC-96 applications (SF)
- A, AB, ABCD (ESF)
- Per DS0 enable with microprocessor read and substitution in both receive and transmit directions for call control and trunk conditioning
- Signaling freeze on LOS

Clock Management:

- Flexible receive and transmit clock selection, including local oscillator
- Two frame slip buffers for each of receive and transmit paths, with independent bypass
- System side and line side clocks on receive and transmit, each independent

Alarms and Errors:

- Detect and force Yellow and blue (AIS) alarms, detect AIS-CI signature
- Detect Out Of Frame, Loss Of Signal, Severely Errored Frame, Change of Frame Alignment, Transmit Slips and Receive Slips
- Detect, count and force CRC errors (ESF only), frame bit errors and line code errors (bipolar violations, with or without excessive zeros)
- Detect and force frame slips

Fractional T1:

- Gapped Clock programmed DS0 channels
- Receive and Transmit gapped clocks with selection and direction independent

DS0 Control:

- Per DS0 enable (independent receive and transmit) with microprocessor read and substitution in both receive and transmit directions
- Per DS0 inversion in transmit and receive directions (after slip buffer) in both Transmission and MVIP Modes.

Maintenance:

- Loopbacks - line remote, local, payload remote (ESF only) and DS0 channel
- Detect and transmit SF loop-up and loop-down codes
- Full duplex HDLC link controller with bit-oriented code support for HDLC link and 16-byte receive and transmit FIFOs, back-to-back message support
- Boundary Scan (IEEE 1149.1) for input/output pin monitoring

Microprocessor Interface:

- Eight-bit status register for LOS, AIS, OOF, YEL, CFA, SEF, TXSLIP and RXSLIP
- Eight-bit latched event register and interrupt mask register
- CRC (ESF only), code violation and frame bit error counters
- Shadow registers and counters
- Full control of framing, alarm generation and propagation, codec features
- HDLC link control, signaling access/control, DS0 access/control
- Reset, resync, slip buffer and frame bit access

The following features are only selectable for the four framers as a group:

- Transmission Mode ("off line" framing) or MVIP Mode system interfaces
- Serial port to read/write control up to four line interface transceivers, or selection of one of four DS1 line interfaces (receive or transmit) to monitor clock, frame pulse and data
- Microprocessor global reset, masks, polling registers, interrupt polarity and latch edge control
- Two reference clock outputs at 8kHz or 1544 kHz with freeze on LOS
- IEEE 1149.1 boundary scan
- Motorola or Intel microprocessor access with separate address and data buses
- Ability to tristate all outputs for in-circuit testing
- Ability to place line side transmit clock and data to logic low for protection switching
- Synchronization start position is programmable to any receive or transmit bit position on the system side
- External shadow register clock input
- Pseudo-Random Binary Sequence (PRBS) generator and analyzer

Enhancements over the Quad T1 Framer-*Plus* TXC-03103:

- SF mode 9-state signaling for ANSI T-403 Rob and limited support for SLC-96 applications
- Per DS0 inversion in Transmission and MVIP modes
- Frame bits available in MVIP mode, and supports bypass FDL feature in MVIP mode
- AIS-CI detector
- FDL back-to-back message support

BLOCK DIAGRAM

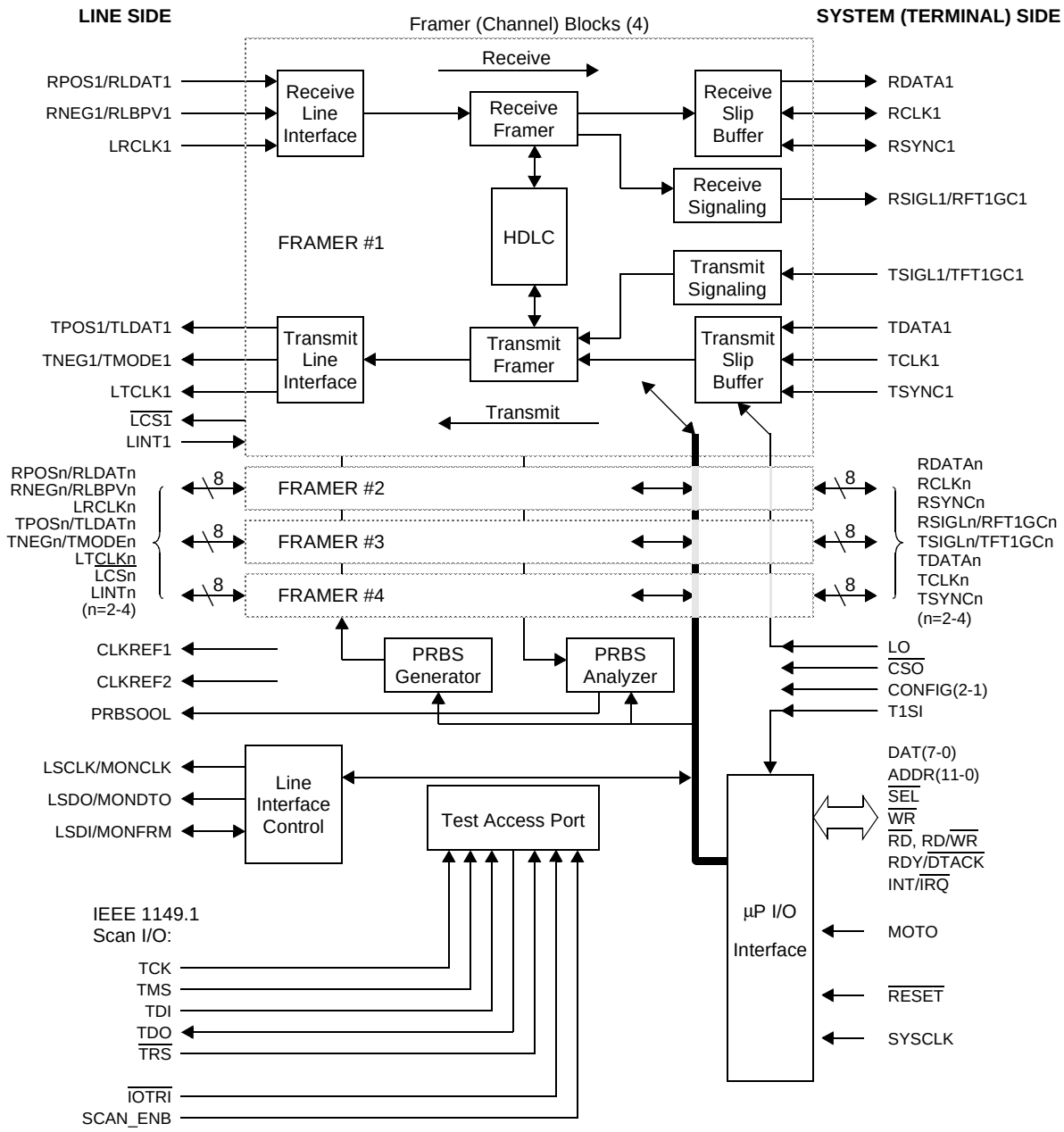


Figure 1. QT1F-*Plus* TXC-03103C Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the Quad T1 Framer-*Plus* (QT1F-*Plus*) is shown in Figure 1. The QT1F-*Plus* consists of the following major blocks: four Framer blocks, Line Interface Control, PRBS Generator, PRBS Analyzer, Microprocessor Input/Output Interface, and Test Access Port.

Each of the four identical Framer blocks consists of the following blocks: Receive and Transmit Line Interface blocks, Receive and Transmit Framer blocks, HDLC block, Receive and Transmit Slip Buffer blocks, and Receive and Transmit Signaling blocks.

The Receive and Transmit Line Interface blocks connect each of the four framers to an external line interface transceiver, which performs the LIU and clock recovery functions. The interface to the external line interface transceiver can be configured for two interface modes: a dual unipolar (rail) interface or a NRZ interface.

When the dual unipolar interface mode is selected, input data from the external line interface transceiver is clocked into the QT1F-*Plus* on pins RPOSn and RNEGn using the recovered receive clock present on the LRCLKn input pin (where n=1-4 identifies one of the four framers). In the transmit direction, unipolar data is clocked out of the QT1F-*Plus* on pins TPOSn and TNEGn by the transmit line clock present on the LTCLKn output pin. For reduced power dissipation in protection switching applications, the LTCLKn, TPOSn, and TNEGn pins for the four framers may be forced low, by placing a low on the $\overline{\text{CSO}}$ pin. Control bits are provided in the memory map which enable the unipolar data to be clocked in and out of the QT1F-*Plus* on either edge of the clocks. For the dual unipolar interface mode, the QT1F-*Plus* provides either a Bipolar with Eight Zero Substitution (B8ZS), or an Alternate Mark Inversion (AMI), coder and decoder function, and Loss Of Signal detection. The Loss Of Signal detector meets the requirements specified in the ANSI T1M1.3 document listed above in the QT1F-*Plus* Features section. A sixteen-bit performance counter is provided for each framer, for counting B8ZS coding violation errors. An option is provided to also count excessive zeros in the coding violations counter.

When the NRZ interface mode is selected, NRZ data is clocked in at the RLDATn pin by the recovered received clock present on the LRCLKn pin. The NRZ data is clocked out of the QT1F-*Plus* on the TLDATn pin by the transmit system clock present on the LTCLKn pin. Control bits are provided in the memory map which enable the NRZ data to be clocked in and out of the QT1F-*Plus* on either edge of the clocks. In NRZ interface mode, the B8ZS or AMI coder and decoder functions are bypassed. However, bipolar violations which are detected in the external line interface transceiver may be clocked into the QT1F-*Plus* on the RLBPVn pin and counted in the associated 16-bit coding violation performance counter. The Remote Line Loopback function for each framer is also implemented in the Line Interface blocks.

The Receive Framer block for each framer performs frame synchronization alignment. The frame synchronization circuit has framing option for the SF and ESF formats. For the SF format, Fs or Ft, or Fs and Ft bits can be used for frame alignment. For the ESF format, FPS, or FPS and a valid CRC-6, may be used. The frame synchronizing circuit meets the framing requirements specified in the ANSI documents. The Out Of Frame alarm criteria can be programmed to use 2 out of 4, 5, or 6 framing bits in error. Framing bit errors and CRC-6 errors are counted in performance counters. The Receive Framer block also monitors and detects the Yellow alarm for either the SF or ESF formats. A non-framing mode can be enabled when the QT1F-*Plus* is configured in the Transmission Modes. The non-framing mode bypasses the Receive Framer block and the Receive Slip Buffer block.

When frame alignment is acquired, the signaling bits are forwarded to the Receive Signaling block for buffering, microprocessor access, and formatting into the signaling highway data stream.

Each Receive Slip Buffer block controls time slot access and retiming for framer n by using a two-frame receive slip buffer that can be optionally bypassed in the Transmission Mode. When the receive slip buffer is enabled, received time slots are written into the buffer by recovered receive clock LRCLKn, and read out as data (RDATAn) from the receive slip buffer by the system input clock RCLKn. A phase shift between the two clocks is detected in this block and a deletion or repetition of one frame of data (24 DS0 channels) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access to the read and write pointers is also provided. The framing bits and signaling bits are not affected by a slip. Slip alarm indications are provided for the microprocessor. The receive slip buffer may be recentered by the microprocessor, or automatically. Individual time slots can be accessed by the microprocessor for the insertion of system idle or out of service codes. When the receive slip buffer is bypassed, the receive clock (RCLKn) and data (RDATAn) are provided as outputs, along with a receive sync signal (RSYNCn).

For 2, 4 or 16-state signaling (robbed-bit signaling), a 96-bit signaling buffer is used to store the signaling bits which have been extracted by the Receive Framer. The signaling buffer may be read, frozen and written to by the microprocessor. This feature permits both signaling to or from the microprocessor (call control) as well as trunk conditioning under control of the microprocessor. If signaling is disabled for a particular channel, the ABCD signaling bits for that time slot will be frozen in their present states. When a loss of signal or an out of frame condition is detected, the signaling bits are also automatically frozen in their present states. The signaling bit states are held until framing has been recovered. Nine-state AB signaling for ANSI T.403 Rob is also supported.

On the terminal side, the system interface interconnects the four framers with the system. For each framer there is a separate receive and transmit highway for the Transmission and MVIP interface modes of operation. The receive highway consists of a data bus (RDATAn), a signaling bus (RSIGLn), a clock (RCLKn), and a synchronization signal (RSYNCn). The transmit highway consists of a data bus (TDATAn), a signaling bus (TSIGLn), a clock (TCLKn), and a synchronization signal (TSYNCn). In the Transmission Mode, the system interface operates at 1.544 MHz, with channels in the data highway, and signaling and alarms on the signaling highway. The receive and transmit system interfaces are synchronized by multiframe pulses that occur at 3-millisecond intervals. Twenty-four frames are sent on the data and signaling highways within the 3-millisecond period, with each of the twenty-four frames consisting of 193 bits (24 DS0 channels plus the framing bit), which correspond to a DS1 frame. The receive and transmit slip buffers can be individually bypassed in this mode.

When the MVIP Mode is selected, the system interface also consists of receive and transmit data highways. However, the receive and transmit system interfaces are synchronized by pulses occurring at 125-microsecond intervals in this mode. The receive and transmit slip buffers must always be enabled in this mode. Each frame consists of 32 time slots which carry the DS0 channels in defined time slots on the data highway. The signaling highway also carries 32 time slots, which contain the signaling states for each channel.

A transmit slip buffer is provided to absorb low speed jitter in the transmit data. Each Transmit Slip Buffer block controls time slot access and retiming for the framer by using a two-frame buffer that can be optionally bypassed in the Transmission Mode. When the transmit slip buffer is enabled, transmit time slots are written into the buffer by the transmit system clock (TCLKn), and they are read out from the buffer by the receive clock (LRCLKn), local oscillator (LO), or transmit system clock (TCLKn). A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (i.e., 24 DS0 channels) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access to the read and write pointers is also provided. Buffer alarm indications are also provided. The slip buffer may be recentered by the microprocessor, or automatically. Individual time slots can be accessed by the microprocessor for the insertion of system idle or out of service codes.

The Transmit Framer block forms the frame (SF or ESF formats) with DS0 channels read from the Transmit Slip Buffer block, and signaling information from the Transmit Signaling block. The HDLC bits (D-bits) in the ESF format can be inserted from the HDLC block or from the system interface (in Transmission Mode only). A 16-bit code word message provided by the microprocessor can also be inserted into the data bits. The CRC-6 is calculated and inserted for the ESF format. The Yellow Alarm Indication is inserted by the microprocessor, or via the signaling highway (TSIGLn). Yellow Alarm for SF format, and loop-up and loop-down codes, can be inserted, if selected. A single frame bit error, or CRC-6 error, can be generated for test purposes. The Transmit Framer and Transmit Slip Buffer can be bypassed if the unframed mode of operation is selected in the Transmission Mode.

Each framer has a full duplex HDLC link controller. The HDLC link controller can be configured to send and receive messages using the 4 kbit/s D-Bits in the ESF format. A 16-byte FIFO is provided in each direction. Interrupt and status alarm support is provided to facilitate FIFO servicing for long messages. The HDLC link controller supports zero bit stuffing/ destuffing, ITU-T CRC generation/checking, flag generation/detection, abort generation/detection, start of frame detection, end of frame detection, and FIFO underflows and overflows.

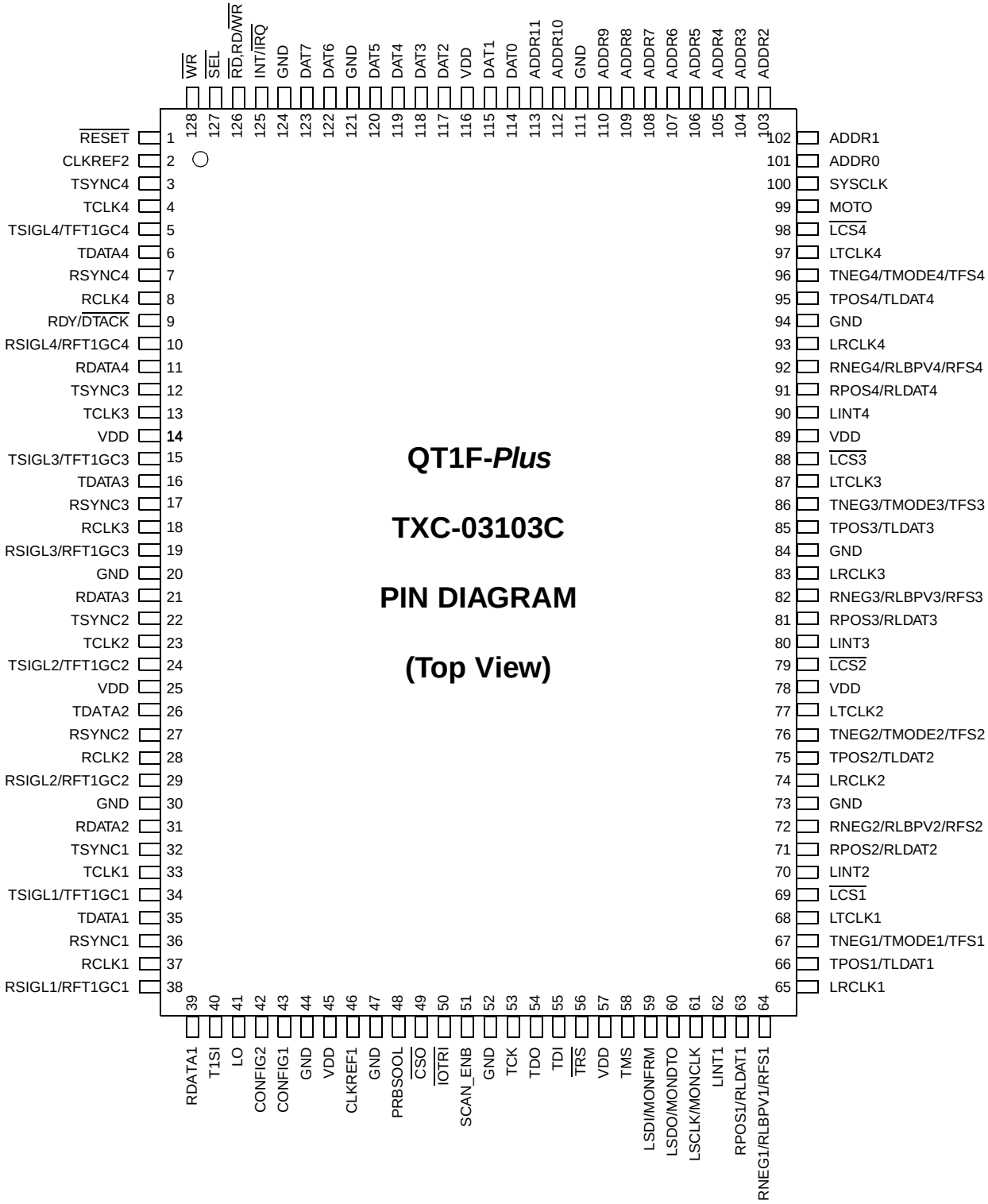
The Line Interface Control block provides a serial port for communicating with an external line interface transceiver. This allows the system microprocessor to control the transceiver through the QT1F-*Plus*. The interface consists of a data output pin (LSDO), clock output pin (LSCLK), and a data input pin (LSDI). These signals are shared between all of the transceivers. Each transceiver is selected by the QT1F-*Plus*, using individual chip select output signals ($\overline{\text{LCS}}$n). In addition, a general purpose input pin (LINTn) can be used to generate a maskable interrupt.

The Test Access Port block includes a five-pin Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This Test Access Port block provides external boundary scan to read and write the QT1F-*Plus* input and output pins from the TAP for board and component testing. In addition, a four-byte read only memory location is provided for reading the TranSwitch manufacturer ID, a five-digit part identification number, and a version number for the part.

To assist in testing, built-in Pseudo Random Binary Sequence (PRBS) Generator and Analyzer blocks are provided. The PRBS Generator and Analyzer support a 2^{15}-1 bit pseudo random binary sequence which is inverted relative to the pattern specified in the ITU-T Recommendation O.151. Each framer may select the PRBS Generator and Analyzer. The output of the Analyzer is provided on pin PRBSOOL. The PRBS framed mode, in which the transmit framer generates framing, is selected by writing a 1 to bit 6 in register 013H (PRBSFR) and is intended for use as a self-test feature. In this mode, the PRBS Generator and Analyzer can only communicate and frame up within the framer itself. The recovered line clock is the clock source for the Analyzer. If the receive slip buffer is enabled, then LRCLK must be its read clock source. The LO pin is the clock source for the Generator. In unframed PRBS mode, which is selected by writing a 0 to PRBSFR, the transmit framer does not generate framing. The QT1F-*Plus* also provides local loopback, remote line loopback, payload remote loopback, automatic remote line loopback (based on loop-up/down patterns received over a 5 second period), and DS0 channel loopback options for each framer.

The QT1F-*Plus* can be configured to operate with either Intel or Motorola compatible microprocessors via the Microprocessor Input/Output Interface block. Interrupt capability is provided with global and individual framer mask bits. An option is provided in software which permits the interrupt polarity to be inverted. An external system clock is used to run the internal state machines.

PIN DIAGRAM



Note: This diagram is rotated relative to the top view shown in the Package Diagram in Figure 46a.

Figure 2. QT1F-*Plus* TXC-03103C Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	14, 25, 45, 57, 78, 89, 116	P		**Power Supply:** +3.3 or +5.0 volt, ±5%, V_{DD} supply voltage.
GND	20, 30, 44, 47, 52, 73, 84, 94, 111, 121, 124	P		**Ground:** 0 volt reference.

* Note: I = Input; O = Output; P = Power; T=Tristate.

Line Interface Signals

Symbol	Pin No.	I/O/P	Type *	Name/Function
RPOSn/ RLDATn (n=4-1)	91 81 71 63	I	TTL	**Receive Unipolar Positive Signal Input:** When control bit RAIL (bit 7 in register X00H) is a 1, the dual unipolar (positive/negative rail) mode is selected, and the RPOSn pin carries the receive positive rail input signal. RPOSn is high whenever a positive pulse is received by the external line interface transceiver. **Receive Line (NRZ) Data Input:** When control bit RAIL (bit 7 in register X00H) is a 0, the NRZ mode is selected, and the RLDATn pin carries the receive NRZ data input signal. RLDATn is normally active high whenever a positive or negative pulse is received by the external line interface transceiver. When control bit RXNRZP (bit 0 in register X01H) is a 1, the QT1F-*Plus* accepts an inverted data signal and RLDATn is active low.
RNEGn/ RLBPVn/ RFSn (n=4-1)	92 82 72 64	I	TTL	**Receive Unipolar Negative Signal Input:** When control bit RAIL (bit 7 in register X00H) is a 1, the dual unipolar (positive/negative rail) mode is selected, and the RNEGn pin carries the receive negative rail input signal. RNEGn is high whenever a negative pulse is received by the external line interface transceiver. **External Receive Bipolar Violation Indication Input:** When control bit RAIL (bit 7 in register X00H) is a 0 and the fast sync option is not selected (control bit RXFS, bit 1 in register X06H, is a 0), the RLBPVn pin provides an input for indications of external bipolar violations detected in the external line interface transceiver. A high indicates a bipolar violation, and increments the internal 16-bit coding violation counter once on a clock cycle. A bipolar violation is clocked in on rising edges of the receive line clock LRCLKn. **Receive Fast Sync:** When control bit RAIL (bit 7 in register X00H) is a 0 and the fast sync mode is selected (control bit RXFS, bit 1 in register X06H, is a 1), this pin is used for a fast sync feature. A pulse on this pin is interpreted as identifying bit 192 of the last frame of the multiframe.

* Note: See Input, Output and Input/Output Parameters section for Type definitions, which depend on the value of V_{DD} selected.

Symbol	Pin No.	I/O/P	Type *	Name/Function
LRCLKn (n=4-1)	93 83 74 65	I	TTL	**Receive Line Clock:** An input for the 1544 kHz recovered clock from the external line interface transceiver. Control bit RXCP (bit 6 in register X01H) determines the clock edge on which the receive line signals RPOSn/RNEGn and RLDATn are to be clocked in (1 for rising edge).
TPOSn/ TLDATn (n=4-1)	95 85 75 66	O	CMOS 2mA	**Transmit Unipolar Positive Signal Output:** When control bit RAIL (bit 7 in register X00H) is a 1, the dual unipolar mode is selected, and the TPOSn pin carries the transmit positive rail output signal. TPOSn is high whenever a positive pulse is to be transmitted by the external line interface transceiver. **Transmit Line (NRZ) Data Output:** When control bit RAIL (bit 7 in register X00H) is a 0, the NRZ mode is selected, and the TLDATn pin carries the transmit NRZ data output signal. TLDATn is normally active high whenever a positive or negative pulse is to be transmitted by the external line interface transceiver. When control bit TXNRZP (bit 5 in register X01H) is a 1, the data output TLDATn is inverted and it is active low.
TNEGn/ TMODEn/ TFSn (n=4-1)	96 86 76 67	O	CMOS 2mA	**Transmit Unipolar Negative Signal Output:** When control bit RAIL (bit 7 in register X00H) is a 1, the dual unipolar mode is selected, and the TNEGn pin carries the transmit negative rail output signal. TNEGn is high whenever a negative pulse is to be transmitted by the external line interface transceiver. **Transmit Mode General Purpose Output:** When control bit RAIL (bit 7 in register X00H) is a 0 and the fast sync mode is not selected (control bit TXFS, bit 0 in register X06H, is a 0), the state written into bit BE (bit 6 in register X00H) is clocked out on rising edges of the transmit line clock LTCLKn. **Transmit Fast Sync:** When control bit RAIL (bit 7 in register X00H) is a 0 and the fast sync mode is selected (control bit TXFS, bit 0 in register X06H is a 1), this pin is used for a fast sync feature providing a sync pulse every 3 ms whether in SF or ESF mode; a pulse is sent on this pin for bit 192 in frame 24 when the ESF framing mode is selected and every other frame number 12 when the SF framing mode is selected. The ESF mode is selected when control bits FMD1 and FMD0 (bits 2-1 in register X04H) are set to 11. The SF mode is selected when the FMD1 and FMD0 bits are written with 01.
LTCLKn (n=4-1)	97 87 77 68	O	CMOS 2mA	**Transmit Line Clock:** A 1544 kHz clock output. Control bit TXCP (bit 7 in register X01H) determines the clock edge on which the transmit line signals TPOSn/TNEGn and TLDATn are to be clocked out (1 for rising edge).

Line Interface Control Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
LINTn (n=4-1)	90 80 70 62	I	TTL	**General Purpose Interrupt Input Port:** When enabled by control bit LIE (bit 1 in register X00H) being set to 1, the signal on this pin is logically OR-gated with the internal loss of signal indication to cause a loss of signal alarm and (if enabled) an interrupt. Control bit LPOL (bit 0 in register X00H) selects the input sense of this pin (1 for active low). This pin is active in both dual unipolar and NRZ modes.
$\overline{\text{LCS}}$n (n=4-1)	98 88 79 69	O	CMOS 2mA	**Line Interface Transceiver Chip Select:** An active low signal that enables communications in both directions between the external line interface transceiver for channel n and the QT1F-*Plus*.
LSCLK/ MONCLK	61	O(T)	CMOS 2mA	**Line Interface Transceiver Clock Signal:** The clock for the transceiver is enabled when the CONFIG2 pin (pin 42) is low. This clock is shared between the four external transceivers. It is used to clock input data, and output data, between the external line interface transceiver and the QT1F-*Plus*. This clock is derived from the signal at pin LO. Output data (LSDO) is clocked out of the QT1F-*Plus* on falling edges of this clock. Input data (LSDI) is clocked into the QT1F-*Plus* on rising edges of this clock. **Monitor Clock Signal:** The monitor feature is enabled when the CONFIG2 pin (pin 42) is high. The MONCLK pin provides either a receive or transmit NRZ clock. The clock in this mode can be tristated by writing a 0 to control bit ESP/EMON (bit 4 in register 013H).
LSDO/ MONDTO	60	O(T)	CMOS 2mA	**Line Interface Transceiver Data Output Signal:** The output data signal for the transceivers is enabled when the CONFIG2 pin (pin 42) is low. The output data signal is shared between the four transceivers. **Monitor Data Signal:** The monitor feature is enabled when the CONFIG2 pin (pin 42) is high. The MONDTO pin provides either a NRZ receive or transmit data signal. This pin can be tristated in this mode by writing a 0 to control bit ESP/EMON (bit 4 in register 013H).
LSDI/ MONFRM	59	I/O	TTL/CMOS 4mA	**Line Interface Transceiver Data Input Signal:** The input data signal from the transceivers is enabled when the CONFIG2 pin (pin 42) is low. The input data signal is shared between the four transceivers. **Monitor Frame:** This pin becomes an output when the CONFIG2 pin is high and a 1 is written to control bit ENMONFR (bit 2 in register 013H). This bit is active high during the bit time of bit 192 and low during other bit times. The frame pulse is clocked out on the rising edges of MONCLK.

Clock Reference Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
CLKREF1	46	O(T)	CMOS 2mA	**Clock Reference 1:** This clock reference output is enabled when control bit ENREF1 (bit 3 in register 019H) is a 1. The clock reference signal can be either a 1544 kHz clock or an 8 kHz clock. When control bit 1544KHZ (bit 4 in register 019H) is a 1, the 1544 kHz reference is selected. The framer from which the clock is derived is determined by selection bits CR1S1 and CR1S0 (bits 1 and 0 in register 019H). This pin is forced low when a loss of signal alarm occurs for the framer selected.
CLKREF2	2	O(T)	CMOS 2mA	**Clock Reference 2:** This clock reference output is enabled when control bit ENREF2 (bit 5 in register 019H) is a 1. The clock reference signal can be either a 1544 kHz clock or an 8 kHz clock. When control bit 1544KHZ (bit 4 in register 019H) is a 1, the 1544 kHz reference is selected. The framer from which the clock is derived is determined by selection bits CR2S1 and CR2S0 (bits 7 and 6 in register 019H). This pin is forced low when a loss of signal alarm occurs for the framer selected.

System Interface Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
TSYNCn (n=4-1)	3 12 22 32	I	TTL	**Transmit Sync Pulse**: This signal is used to synchronize both the frame sync and signaling multiframe sync counters within a QT1F-*Plus* framer and is sourced by the system. The following table is a summary of the sync pulse characteristics used for the various system interfaces. Interface / Width / Polarity / Period / Lead Used Transmission / 1 Clk Cyc / High / 3 ms / TSYNCn MVIP / 1 Clk Cyc / Low / 125 µs / TSYNCn Please note: The sync pulse is also programmable with respect to the transmit data highway.
TCLKn (n=4-1)	4 13 23 33	I	TTL	**Transmit Clock:** This clock is sourced from the system. It is used to clock in the TSYNCn, TSIGLn, and TDATAn signals from the system. The following table is a summary of the clock rates and clock transitions used for clocking in data (D), signaling (S), and the sync pulse. Interface / Rate / Clk in D/S / Clk in SyncL / Lead Used Transmission / 1.544 MHz / Pos. / Pos. / TCLKn MVIP / 2.048 MHz / Neg. / Pos. / TCLKn

Symbol	Pin No.	I/O/P	Type	Name/Function
TDATAn (n=4-1)	6 16 26 35	I	TTL	**Transmit Data Highway Input:** This lead carries the data time slots from the system interface to the QT1F-*Plus*. The following table is a summary of the transmit data highway format. Interface — Format Transmission — DS1 frame (193 bit positions) repeated 24 times on TDATAn MVIP — DS1 frame mapped into 32 time slots on TDATAn
TSIGLn/ TFT1GCn (n=4-1)	5 15 24 34	I/O	TTL/CMOS 4mA	**Transmit Signaling Highway Input:** This lead carries from the system the signals that represent signaling information and an alarm indication (Transmission Mode only), according to the table given below. Interface — Format Transmission — 193-bit frame format repeated 24 times on TSIGLn MVIP — 32 time slots on TSIGLn **Transmit Fractional T1 Gapped Clock Output:** The Transmit Fractional T1 gapped clock feature is enabled when the CONFIG1 pin is low (Transmission Mode) and control bit FT1M (bit 0 in register X02H) is written with a 1. A gapped clock is provided on the pin for the Fractional T1 channel(s) selected. One or more DS0 channels may be selected by writing a 1 to control bits TFD1-TFD24 in registers X3DH-X3FH. The gapped clock has the same phase as the TCLKn clock.
RSYNCn (n=4-1)	7 17 27 36	I/O	TTL/CMOS 4mA	**Receive Sync Pulse:** This signal is used to synchronize external system circuitry from the QT1F-*Plus*. It is an input if the receive slip buffer is enabled, otherwise it is an output. The following table is a summary of the sync pulses used for the various system interfaces. Interface — Width — Polarity — Period — Lead Used Transmission — 1 Clk Cyc — High — 3 ms — RSYNCn MVIP — 1 Clk Cyc — Low — 125 µs — RSYNCn Please note that for the Transmission Mode, the QT1F-*Plus* can source the sync pulse and clock. The selection of input or output is determined by control bit RXC (bit 5 in register X02H); writing a 0 to RXC causes RSYNCn to be an input and writing a 1 to RXC causes RSYNCn to be an output. The sync pulse is also programmable with respect to the receive data highway.

Symbol	Pin No.	I/O/P	Type	Name/Function
RCLKn (n=4-1)	8 18 28 37	I/O	TTL/CMOS 4mA	**Receive Clock:** This clock is used to clock the RDATAn, RSIGLn, and RSYNCn signals from the system or (for RSYNCn) into the system. The following table is a summary of the clock rates and clock transitions used for clocking data (D), signaling (S), and the sync pulse. Interface / Rate / Clk out D/S / Clk in Sync / Lead Used Transmission / 1.544 MHz / Neg. / Pos. / RCLKn MVIP / 2.048 MHz / Pos. / Pos. / RCLKn Note: In the Transmission Mode, RSYNCn is clocked out on negative clock transitions when the sync pulse is an output. The selection of input or output is determined by control bit RXC (bit 5 in register X02H); writing a 0 to RXC causes RCLKn to be an input and writing a 1 to RXC causes RCLKn to be an output.
RDATAn (n=4-1)	11 21 31 39	O	CMOS 2mA	**Receive Data Highway Output:** This lead carries the time slots from the QT1F-*Plus* to the system. The following table is a summary of the receive data highway format. Interface — Format Transmission — DS1 frame (193 bit positions) repeated 24 times on RDATAn MVIP — DS1 frame mapped into 32 time slots on RDATAn
RSIGLn/ RFT1GCn (n=4-1)	10 19 29 38	O	CMOS 2mA	**Receive Signaling Highway Output:** This lead carries to the system the signals that represent signaling information and an alarm indication (Transmission Mode only), according to the table given below. Interface — Format Transmission — 193-bit frame format repeated 24 times on RSIGLn MVIP — 32 time slots on RSIGLn **Receive Fractional T1 Gapped Clock Output:** The Received Fractional T1 gapped clock feature is enabled when the CONFIG1 pin is low (Transmission Mode) and control bit FT1M (bit 0 in register X02H) is written with a 1. A gapped clock is provided on this pin for the Fractional T1 channel(s) selected. One or more DS0 channels may be selected by writing a 1 to control bits RFD1-RFD24 in registers X3AH-X3CH. The gapped clock has the same phase as the RCLKn clock.

Symbol	Pin No.	I/O/P	Type	Name/Function
LO	41	I	TTL	**Local Oscillator Input:** This independent 1544 kHz ± 32 ppm (50 ± 10)% duty cycle clock is an alternate clock source for the transmit line clock (LTCLKn), and for clocking out data from the slip buffer. This clock is selected as the transmit clock source when control bits TXC1 and TXC0 (bits 7 and 6 in register X02H) are both set to 0. On the detection of Loss of Signal, this clock is substituted for the receive line clock (LRCLKn) which becomes RCLKn when control bit RXC (bit 5 in register X02H) is set to a 1. This clock is required for generating LSCLK (pin 61) and the PRBS generator function. When used for the PRBS generator it must be synchronous with TCLKn, where 'n' is the framer sourcing PRBS.

Other Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
T1SI	40	I	TTL	**One Second Shadow Register Signal**: A positive pulse occurring every second which latches the performance counters (CRC-6 Error, Coding Violation, and Frame Bit Error) and PM and FM registers when the shadow register feature is enabled. The performance counters can count without this clock present, but they will not be shadowed. To comply with ANSI T1.403 this clock should be 1.0 Hz ± 32 ppm. The shadow register feature is enabled when a 1 is written to control bit ENPMFM (bit 3 in register 006H). This input is required for automatic loop-up/down code detection.
CONFIG2	42	I	TTL	**Configuration 2 Select Pin**: A low enables the line control interface for communications between the QT1F-*Plus* and the external line interface transceivers. A high disables the line control interface, and configures clock and data pins for a monitor interface. The selection is common to all four framers.
CONFIG1	43	I	TTL	**Configuration 1 Select Pin**: A low configures the QT1F-*Plus* for the Transmission Mode of operation (1544 kbit/s) at the system interface. A high configures the QT1F-*Plus* for the MVIP Mode of operation at the system interface. The selection is common to all four framers.
$\overline{\text{CSO}}$	49	I	TTL	**Power Down**: An active low on this pin forces the transmit clock (LTCLKn), and the transmit unipolar leads (TPOSn and TNEGn) for rail data output signals, of all four framers to the active low state for protection switching purposes.
PRBSOOL	48	O	CMOS 2mA	**PRBS Out Of Lock:** Enabled only in the Transmission Mode and when control bit PRBSEN (bit 5 in register 013H) is a 1. A high indicates the analyzer is out of lock. This pin is low when lock is acquired or when this feature is disabled.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{IOTRI}}$	50	I	TTL	**High Z State:** An active low placed on this pin forces all output pins (except TDO) to a high impedance state for test purposes. This pin must be held high for normal operation.
SCAN_ENB	51	I	TTL	**TranSwitch Test Pin:** This pin is used for manufacturing tests only and must be held low for normal operation.

Boundary Scan

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	53	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock:** This clock is used to shift data in on pin TDI on rising edges, and to shift data out on pin TDO on falling edges. The maximum clock frequency is 10 MHz.
TMS	58	I	TTLp	**IEEE 1149.1 Test Port Mode Select:** This signal is clocked in on rising edges of the clock TCK, and is used to place the Test Access Port Controller into various states as defined in the IEEE 1149.1 standard. This pin must be high for normal framer operation.
TDI	55	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked in to this pin on rising edges of clock TCK.
TDO	54	O(T)	CMOS 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this pin on falling edges of clock TCK. When inactive, this output is forced to the high impedance state.
$\overline{\text{TRS}}$	56	I	TTLp	**IEEE 1149.1 Test Port Reset Pin:** This pin must either be held low, asserted low, or asserted low then high (pulsed low, 10 ns minimum) to asynchronously reset the Test Access Port (TAP) controller. Failure to do so may cause the TAP controller to take control of the QT1F-*Plus* output pins.

Microprocessor Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
MOTO	99	I	TTL	**Motorola / Intel Processor Select:** This pin defines the operating mode of the Microprocessor Input/Output Interface. When it is high, Motorola (M) Mode is selected. When it is low, Intel (I) Mode is selected.
ADDR(11-0)	113, 112, 110-101	I	TTL	**Address Bus (Motorola/Intel Buses):** These pins are address line inputs that are used for accessing a register location for a read/write cycle. High is logic 1. For normal operation ADDR11 may be tied low.
DAT(7-0)	123, 122, 120-117, 115, 114	I/O(T)	CMOS 8mA	**Data Bus:** Bidirectional data lines used for transferring data. High is logic 1.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{SEL}$	127	I	TTLp	**Select:** A low enables data transfers between the microprocessor and the QT1F-*Plus* during a read/write cycle.
$\overline{RD}$ or RD/$\overline{WR}$	126	I	TTL	**Read (I Mode) or Read/Write (M Mode):** Intel Mode - An active low signal generated by the microprocessor for reading the QT1F-*Plus* register locations. Motorola Mode - An active high signal generated by the microprocessor for reading the QT1F-*Plus* register locations. An active low signal is used to write to QT1F-*Plus* register locations.
$\overline{WR}$	128	I	TTL	**Write (I Mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the QT1F-*Plus* register locations. Motorola Mode - Not used (should be set high).
RDY/$\overline{DTACK}$	9	O(T)	CMOS 8mA	**Ready (I Mode) or Data Transfer Acknowledge (M Mode):** Intel Mode - A high is an acknowledgment from the addressed register location that the transfer can be completed. A low indicates that the QT1F-*Plus* cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. This lead is tristated after the low signal.
INT/$\overline{IRQ}$	125	O	CMOS 4mA	**Interrupt:** Intel Mode - A high on this output pin signals an interrupt request to the microprocessor. Motorola Mode - A low on this output pin signals an interrupt request to the microprocessor. The interrupt sense is inverted when a 1 is written to control bit IPOL (bit 4 in register 006H).
$\overline{RESET}$	1	I	TTLp	**Reset:** A low placed on this pin resets the QT1F-*Plus*. The reset must be placed on this pin after the clocks become stable, and must have a minimum duration of 10 cycles of the SYSCLK system clock.
SYSCLK	100	I	TTL	**System Clock:** This asynchronous clock is used by the QT1F-*Plus* to run the internal state machines and counters. The nominal frequency of this clock is 16.0-19.0 MHz with a duty cycle of (50 ± 10)%. This frequency range will provide correct operation with a T1 signal that complies with the frequency range and jitter as specified in AT&T Pub. 62411 or Bellcore GR-499-CORE. When the QT1F-*Plus* is used in a gapped clock situation (e.g., a direct connection to the T1 ports of the M13E device, TXC-03303), the SYSCLK minimum frequency must guarantee that at least 10 rising edges of SYSCLK occur between any two consecutive rising edges of any particular LRCLKn. Note: For V_{DD} = +5.0 volts, nominally, the SYSCLK operating frequency may be extended to 22.0 MHz with a duty cycle of (50 ± 10)%

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Notes 1, 3
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature range	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure level	ME	5		Level	per IPC/JEDEC J-STD-020B
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	Note 4
Latch-up	LU				Meets JEDEC JC 40.2

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. V_{IN} may not exceed the actual operating supply voltage (V_{DD}, either +3.3 volts or +5.0V, ±5%) by more than 0.5 volts.
4. Test method for ESD per per JEDEC JESD22-A114-B.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			27.8	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

+3.3 Volts Supply Voltage

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD} (operating)	3.15	3.30	3.45	V	
I_{DD} (outputs loaded)		30[1]	40[2]	mA	1. All channels operating. Output load 30 pF. SYSCLK at 16 MHz. 2. All channels operating. Output load 30 pF. SYSCLK at 19 MHz.
P_{DD} (outputs loaded)		100[1]	140[2]	mW	
I_{DD} (outputs unloaded)			30	mA	All channels operating. Output load 0 pF. SYSCLK at 16 MHz.
P_{DD} (outputs unloaded)			100	mW	
I_{DD} (outputs loaded)		25		mA	All channels powered down. Output load 30 pF. SYSCLK at 16 MHz.
P_{DD} (outputs loaded)		85		mW	

+5.0 VOLTS SUPPLY VOLTAGE

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD} (operating)	4.75	5.0	5.25	V	
I_{DD} (outputs loaded)		50[1]	70[2]	mA	1. All channels operating. Output load 30 pF. SYSCLK at 16 MHz. 2. All channels operating. Output load 30 pF. SYSCLK at 22 MHz.
P_{DD} (outputs loaded)		250[1]	370[2]	mW	
I_{DD} (outputs unloaded)			50	mA	All channels operating. Output load 0 pF. SYSCLK at 16 MHz.
P_{DD} (outputs unloaded)			265	mW	
I_{DD} (outputs loaded)		40		mA	All channels powered down. Output load 30 pF. SYSCLK at 16 MHz.
P_{DD} (outputs loaded)		200		mW	

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

PARAMETERS FOR +3.3 VOLTS SUPPLY VOLTAGE

Input Parameters for TTL @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current			±10	µA	V_{DD} =3.45; Input = 0 to 3.45
Input capacitance		4.1		pF	

Input Parameters for TTLp @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current	-0.02		-0.50	mA	V_{DD} =3.45; Input = 0 volts
Input capacitance		5.5		pF	

Output Parameters for CMOS4mA @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage current, tristate			±10	µA	V_{DD} =3.45; Input = 0 to 3.45

Output Parameters For CMOS8mA @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			10	ns	C_{LOAD} = 25 pF
Leakage current, tristate			±10	µA	V_{DD} =3.45; Input = 0 to 3.45

Output Parameters For CMOS2mA @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tristate			±10	µA	V_{DD} =3.45; Input = 0 to 3.45

Input/Output Parameters For TTL/CMOS8mA (slew rate controlled) @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.3; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.3; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			10	ns	C_{LOAD} = 25 pF
Leakage current, tristate			±10	µA	V_{DD} =3.45; Input = 0 to 3.45

Input/Output Parameters For TTL/CMOS4mA @ V_{DD} = +3.3V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	3.15 ≤V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤V_{DD} ≤ 3.45
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.3; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.3; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tristate			±10	µA	V_{DD} =3.45; Input = 0 to 3.45

PARAMETERS FOR +5.0 VOLTS SUPPLY VOLTAGE

Input Parameters for TTL @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			±10	µA	V_{DD} =5.25; Input = 0 to 5.25
Input capacitance		4.1		pF	

Input Parameters for TTLp @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current	-0.05		-0.50	mA	V_{DD} =5.25; Input = 0 volts
Input capacitance		5.5		pF	

Output Parameters for CMOS4mA @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD}-0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage current, tristate			±10	µA	V_{DD} =5.25; Input = 0 to 5.25

Output Parameters for CMOS8mA @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD}-0.5			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			10	ns	C_{LOAD} = 25 pF
Leakage current, tristate			±10	µA	V_{DD} =5.25; Input = 0 to 5.25

Output Parameters for CMOS2mA @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tristate			±10	µA	V_{DD} =5.25; Input = 0 to 5.25

Input/Output Parameters for TTL/CMOS8mA (slew rate controlled) @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			10	ns	C_{LOAD} = 25 pF
Leakage Tristate			±10	µA	V_{DD} =5.25; Input = 0 to 5.25

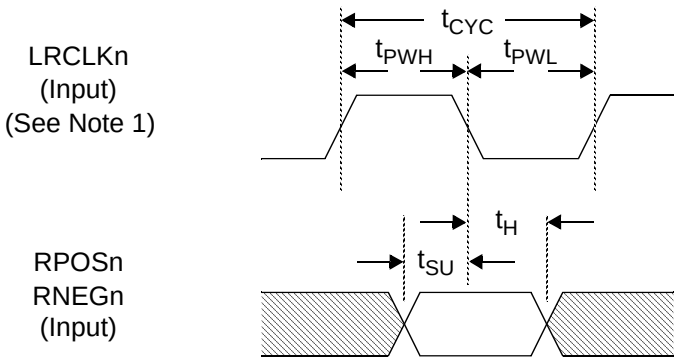
Input/Output Parameters For TTL/CMOS4mA @ V_{DD} = +5.0V

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tristate			±10	µA	V_{DD} =5.25; Input = 0 to 5.25

TIMING CHARACTERISTICS

Detailed timing diagrams for the QT1F-*Plus* are illustrated in Figures 3 through 25, with values of the timing intervals tabulated below the waveform diagrams in each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated.

Figure 3. Dual Unipolar (Rail) Receive Interface Timing

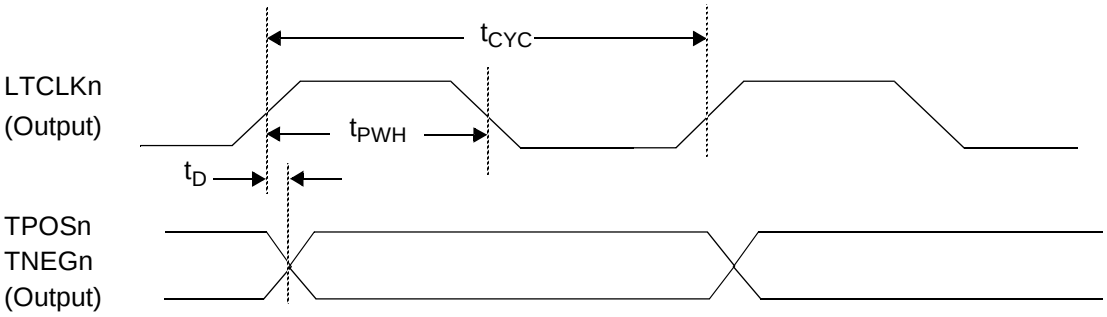


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period (see Note 2)	t_{CYC}		648		ns
LRCLKn high time	t_{PWH}		324		ns
LRCLKn low time	t_{PWL}		324		ns
RPOSn/RNEGn set-up time to LRCLKn↓	t_{SU}	10			ns
RPOSn/RNEGn hold time after LRCLKn↓	t_H	10			ns

Notes:
1. LRCLKn is shown for control bit RXCP (bit 6 in register X01H) set to 0. Data (RPOSn/RNEGn) is clocked in on the rising edges of LRCLKn when control bit RXCP is a 1.
2. The minimum frequency of SYSCLK must guarantee at least 10 rising edges of SYSCLK occur between any two consecutive rising edges of any particular LRCLKn.

Figure 4. Dual Unipolar (Rail) Transmit Interface Timing

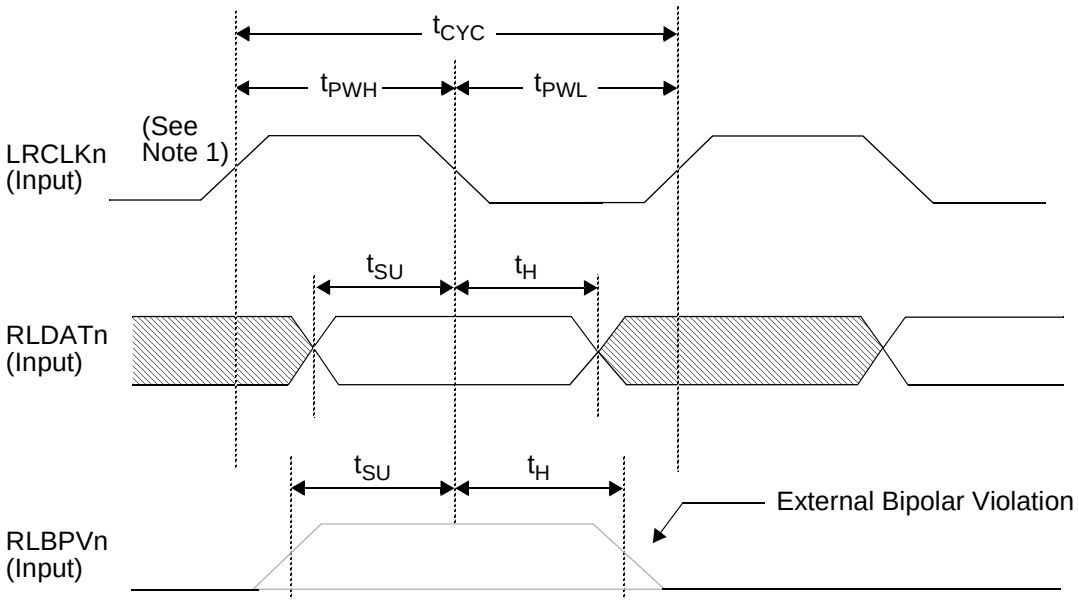


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	t_{CYC}		648		ns
LTCLKn duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TPOSn/TNEGn delay after LTCLKn↑	t_D	0.0	5.0	15	ns

Note: LTCLKn is shown for control bit TXCP (bit 7) in register X01H set to 1. Data is clocked out on falling edges of LTCLKn when control bit TXCP is a 0.

Figure 5. NRZ Receive Interface Timing (External Transceiver)



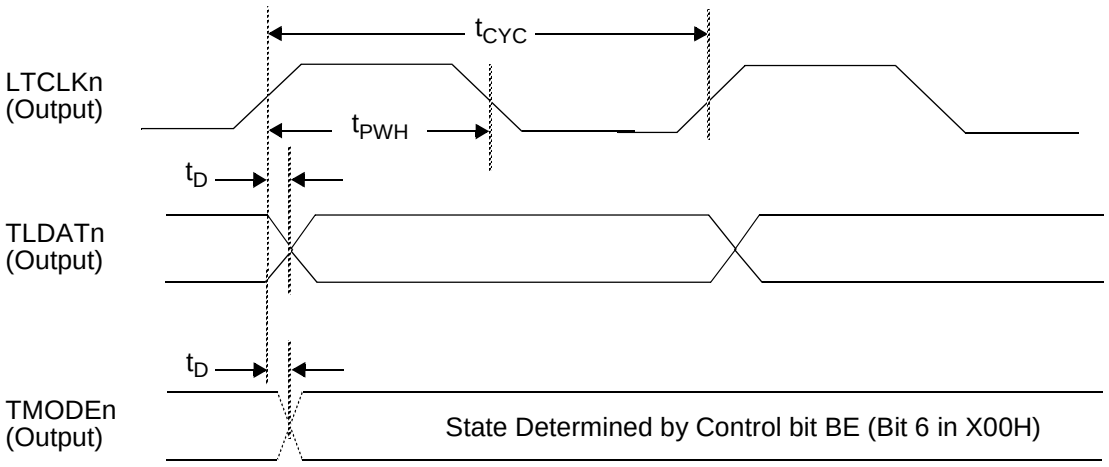
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period (see Note 2)	t_{CYC}		648		ns
LRCLKn high time	t_{PWH}		324		ns
LRCLKn low time	t_{PWL}		324		ns
RLDATn/RLBPVn set-up time to LRCLKn↓	t_{SU}	20			ns
RLDATn/RLBPVn hold time after LRCLKn↓	t_H	20			ns

Notes:

1. LRCLKn is shown for control bit RXCP (bit 6 in register X01H) set to 0. RLDATn and RLBPVn are clocked in on rising edges of LRCLKn when control bit RXCP is a 1. The QT1F-*Plus* accepts an inverted RLDATn signal when control bit RXNRZP (bit 0 in register X01H) is a 1. Control bit RXFS (bit 1 in register X06H) must be set to 0 to use the RLBPVn input.
2. The minimum frequency of SYSCLK must guarantee that at least 10 rising edges of SYSCLK occur between any two consecutive rising edges of any particular LRCLKn.

Figure 6. NRZ Transmit Interface Timing (External Transceiver)

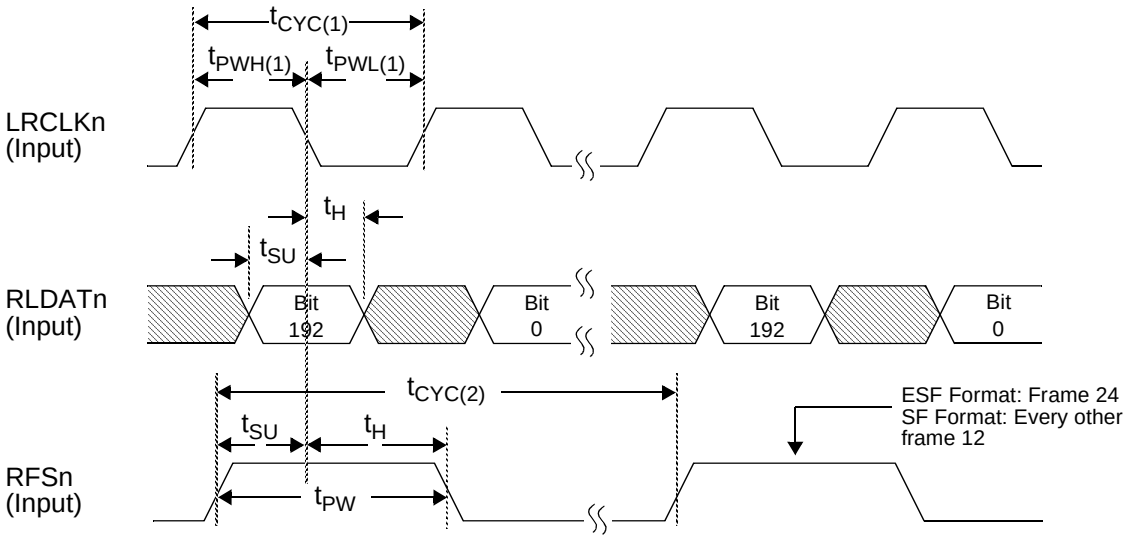


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	t_{CYC}		648		ns
LTCLKn duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
TLDATn/TMODEn delay after LTCLKn↑	t_D	10	15	20	ns

Note: LTCLKn is shown for control bit TXCP (bit 7 in register X01H) set to 1. TLDATn and TMODEn are clocked out on falling edges of LTCLKn when control bit TXCP is a 0. The QT1F-*Plus* provides an inverted TLDATn signal when control bit TXNRZP (bit 5 in register X06H) is a 1. Control bit TXFS (bit 0 in register X06H) must be set to 0 to obtain the TMODEn output.

Figure 7. NRZ Receive Interface Timing (Fast Sync Mode)

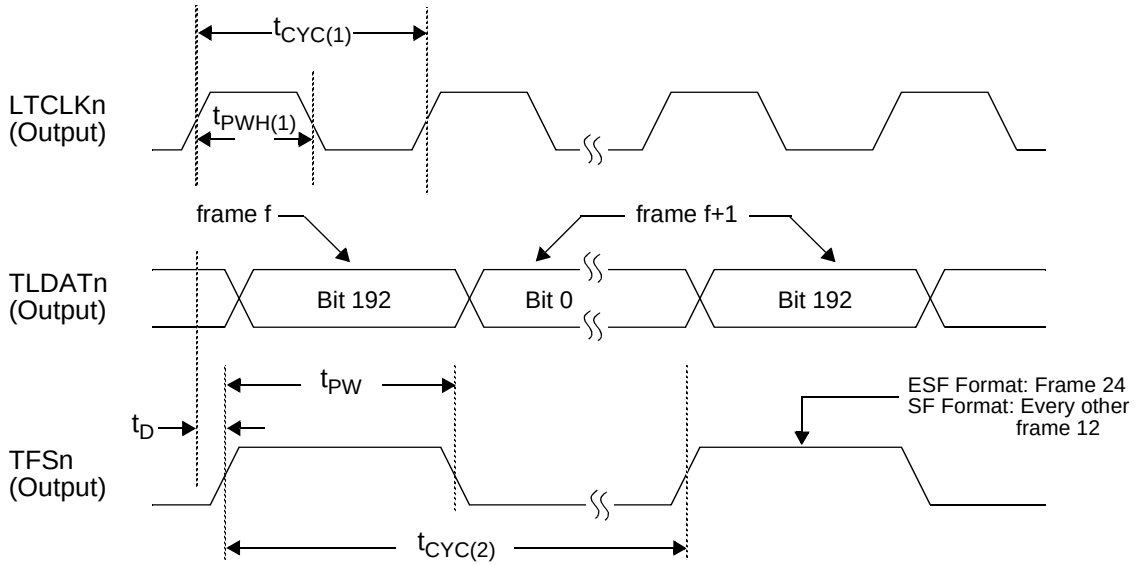


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period	$t_{CYC(1)}$		648		ns
LRCLKn high time	$t_{PWH(1)}$		324		ns
LRCLKn low time	$t_{PWL(1)}$		324		ns
RLDATn/RFSn set-up time to LRCLKn↓	t_{SU}	20			ns
RLDATn/RFSn hold time after LRCLKn↓	t_{H}	20			ns
RFSn period	$t_{CYC(2)}$		3.0		ms
RFSn pulse width high time	t_{PW}		$1 \times t_{CYC(1)}$		ns

Note: LRCLKn is shown for control bit RXCP (bit 6 in register X01H) set to 0. Data is clocked in on rising edges when control bit RXCP is a 1. The QT1F-*Plus* will accept an inverted RLDATn signal when a 1 is written to control bit RXNRZP (bit 0 in register X01H). The fast sync mode is selected by writing a 1 to control bit RXFS (bit 1 in register X06H).

Figure 8. NRZ Transmit Interface Timing (Fast Sync Mode)

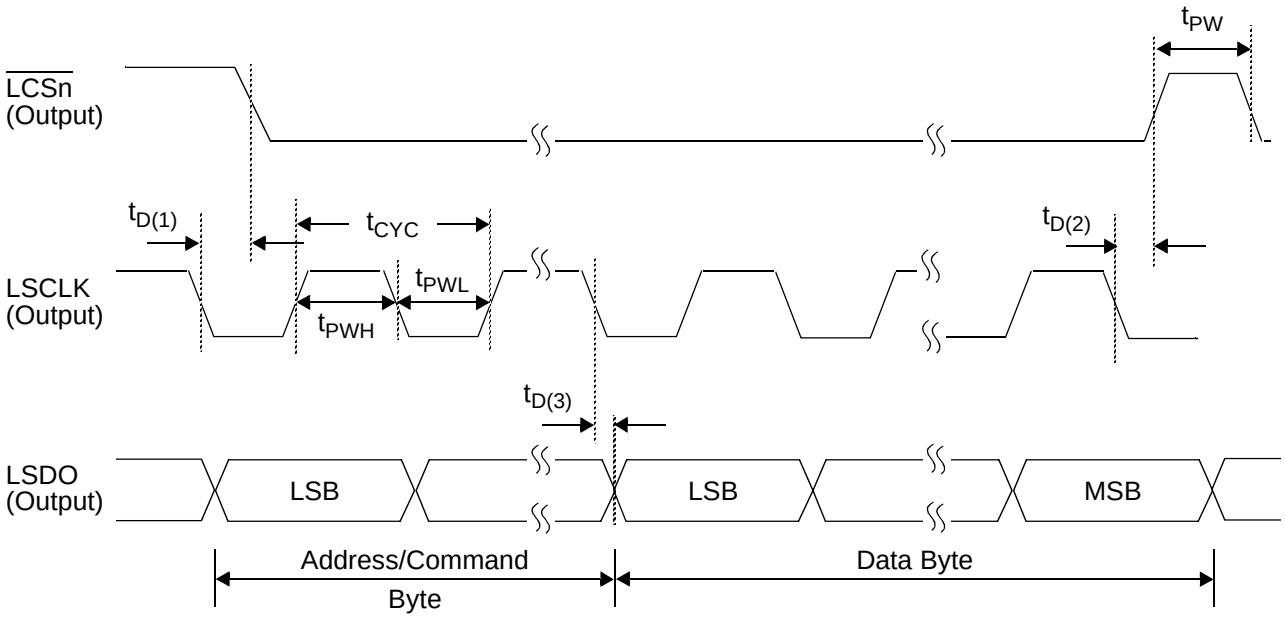


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	$t_{CYC(1)}$		648		ns
LTCLKn duty cycle $t_{PWH(1)}/t_{CYC(1)}$		45	50	55	%
TFSn delay after LTCLKn↑	t_D	5.0	10	15	ns
TFSn pulse width high time	t_{PW}		$1 \times t_{CYC(1)}$		ns
TFSn period	$t_{CYC(2)}$		3.0		ms

Note: LTCLKn is shown for control bit TXCP (bit 7 in register X01H) set to 1. TLDATn/TFSn are clocked out on falling edges of LTCLKn when control bit TXCP is set to 0. The QT1F-*Plus* will output an inverted TLDATn signal when control bit TXNRZP (bit 5 in register X06H) is a 1. The fast sync mode is selected by writing a 1 to control bit TXFS (bit 0 in register X06H).

Figure 9. Serial Port Write Timing

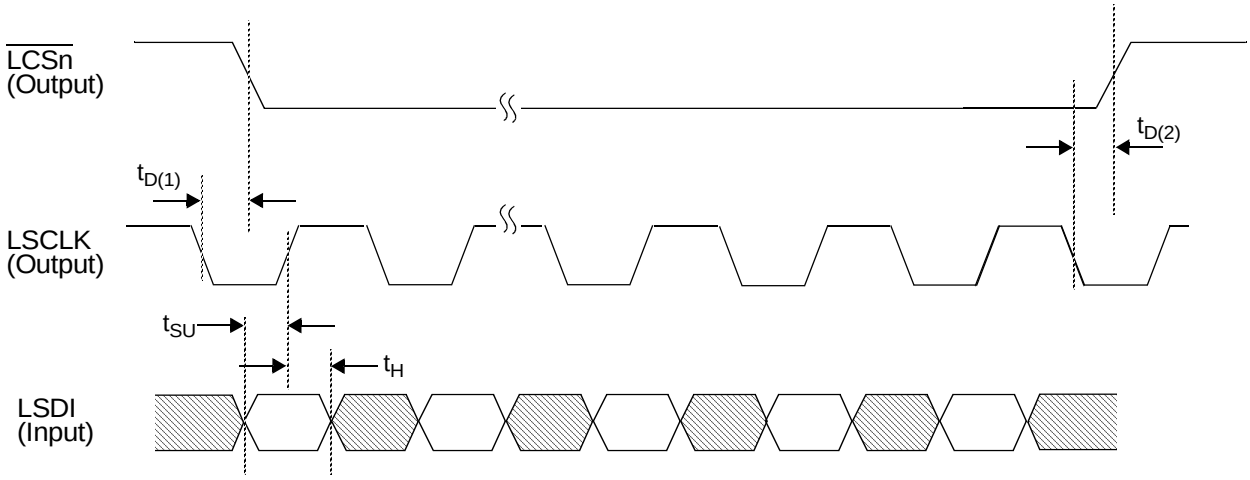


Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{LCSn}}$ pulse width high time	t_{PW}	300			ns
LSCLK clock period (see Note 2)	t_{CYC}		648		ns
LSCLK high time (see Note 3)	t_{PWH}	240	324	408	ns
LSCLK low time (see Note 3)	t_{PWL}	240	324	408	ns
$\overline{\text{LCSn}}\downarrow$ delay after LSCLK$\downarrow$	$t_{D(1)}$	0.0	1.0	5.0	ns
LSDO delay after LSCLK$\downarrow$	$t_{D(3)}$	0.0	1.0	5.0	ns
$\overline{\text{LCSn}}\uparrow$ delay after LSCLK$\downarrow$	$t_{D(2)}$	0.0	1.0	5.0	ns

Notes:
1. The serial port interface for the line interface transceiver is selected when an active low is placed on the CONFIG2 pin (pin 42).
2. The clock period for LSCLK is the same as that of the clock provided on the LO pin (pin 41), since LSCLK is derived from the signal at LO.
3. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK at between 20-22 MHz.

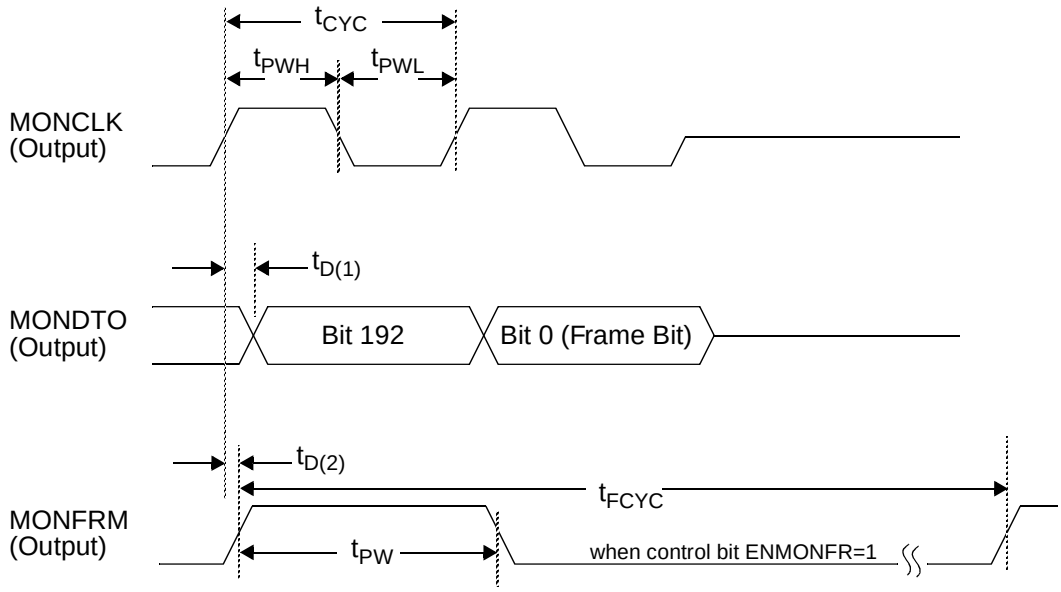
Figure 10. Serial Port Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
LSDI set-up time to LSCLK↑	t_{SU}	20			ns
LSDI hold time after LSCLK↑	t_H	20			ns
$\overline{\text{LCSn}}$↓ delay after LSCLK↓	$t_{D(1)}$	20	25	30	ns
$\overline{\text{LCSn}}$↑ delay after LSCLK↓	$t_{D(2)}$	20	25	30	ns

Notes:
1. The serial port interface for the line interface transceiver is selected when an active low is placed on the CONFIG2 pin (pin 42).
2. The clock period for LSCLK is the same as that of the clock provided on the LO pin (pin 41), since LSCLK is derived from the signal at LO.

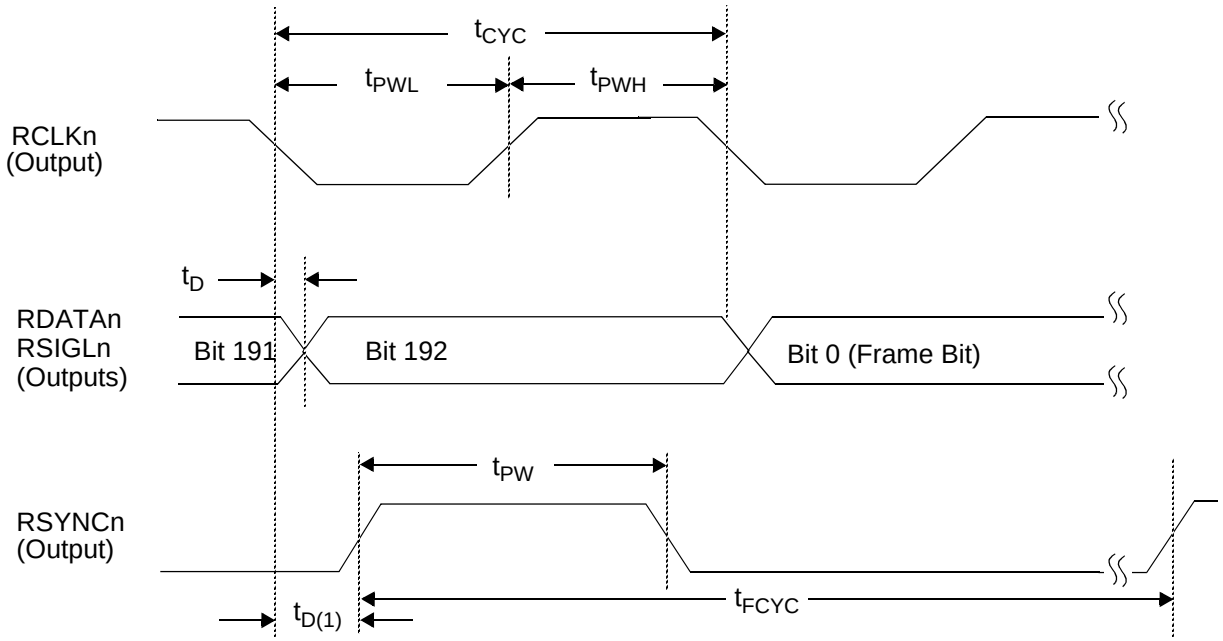
Figure 11. Monitor Mode Timing



Parameter	Symbol	Min	Typ	Max	Unit
MONCLK clock period	t_{CYC}	637	648	700	ns
MONCLK high time	t_{PWH}		324		ns
MONCLK low time	t_{PWL}		324		ns
MONDTO delay after MONCLK↑	$t_{D(1)}$	5.0	10	15	ns
MONFRM delay after MONCLK↑	$t_{D(2)}$	5.0	10	15	ns
MONFRM pulse width	t_{PW}	500	648		ns
MONFRM period	t_{FCYC}		125		µs

Note: The Monitor port is enabled when an active high is placed on the CONFIG2 pin (pin 42). Control bits T1CHCS1 and T1CHCS0 (bits 1, 0 in register 013H) select the channel to be monitored. Control bit RXTX (bit 3 in register 013H) selects either the receive side or transmit side to be monitored. Writing a 0 to control bit ESP/EMON (bit 4 in register 013H) tristate both outputs.
The input signals to the receive framer (MONDTO and MONCLK) are monitored when control bit RXTX is a 1 and control bit ENMONFR (bit 2 in register 013H) is a 0. When control bits RXTX and ENMONFR are equal to 1, the receive framer output is monitored (MONDTO, MONFRM and MONCLK).

Figure 12. Receive Highway Timing - Transmission Mode (Recovered Receive Line Clock)



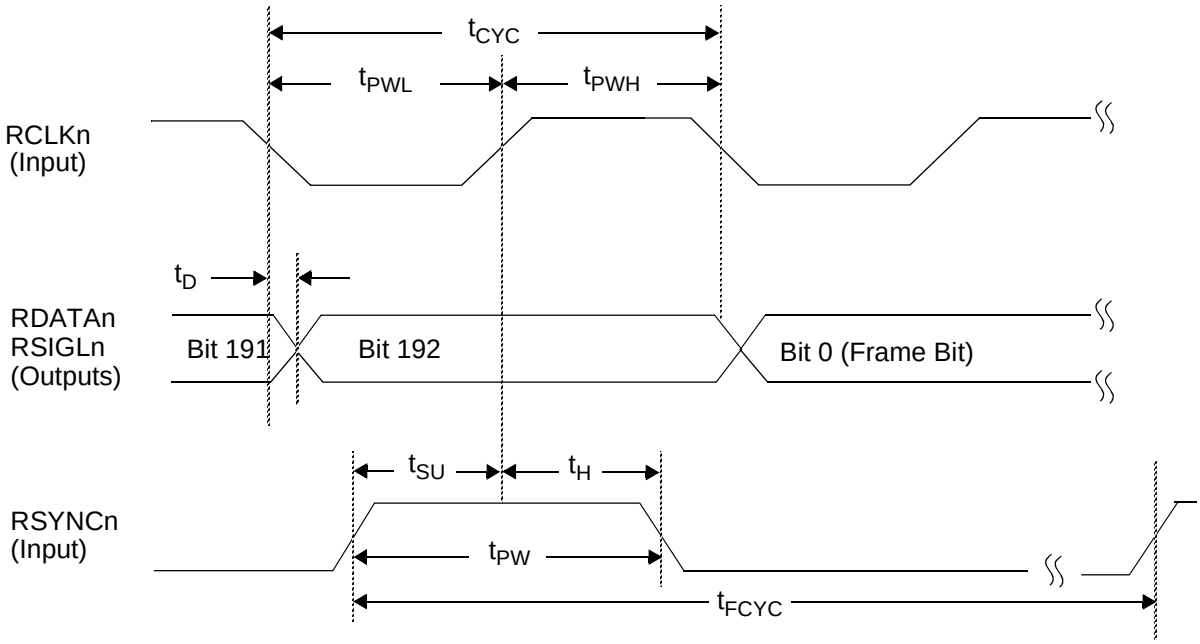
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}		648		ns
RCLKn low time (see Note 2)	t_{PWL}	240	324	408	ns
RCLKn high time (see Note 2)	t_{PWH}	240	324	408	ns
RDATAn/RSIGLn delay after RCLKn↓	t_D	0.0	5.0	10	ns
RSYNCn delay after RCLKn↓	$t_{D(1)}$	0.0	5.0	10	ns
RSYNCn pulse width	t_{PW}	500	648	750	ns
RSYNCn period	t_{FCYC}		3.0		ms

Notes:

1. Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43). The recovered receive line clock (RCLKn) and an internal sync pulse are used to clock out data (RDATAn), signaling (RSIGLn), and the sync pulse (RSYNCn) to the system, when control bits RXC and RSE (bits 5 and 3 in register X02H) are 10 or 11. Control bit RXC selects the clock source, while RSE enables/disables the receive slip buffer. The position of RSYNCn with respect to the RDATAn/RSIGLn signals can be offset. The values written to register 018H will determine the offset. RSYNCn is shown for an offset value equal to zero.
2. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK between 20-22 MHz.

Figure 13. Receive Highway Timing - Transmission Mode (System Clock)



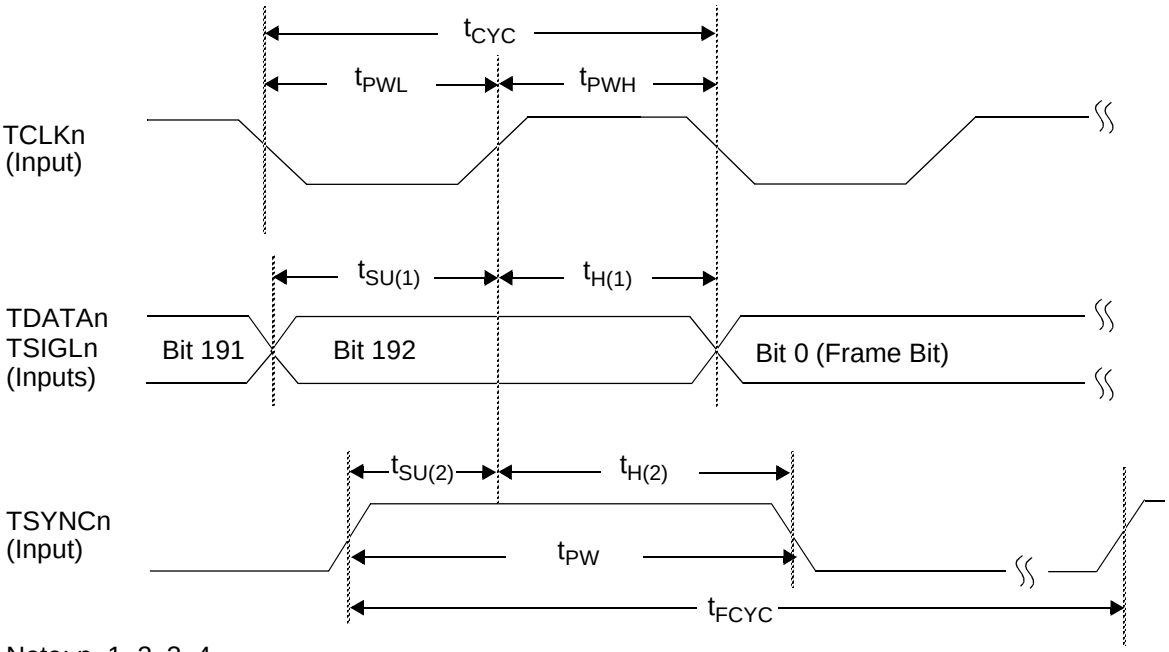
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}		648		ns
RCLKn low time (see Note 3)	t_{PWL}	240	324	408	ns
RCLKn high time (see Note 3)	t_{PWH}	240	324	408	ns
RDATAn/RSIGLn delay after RCLKn↓	t_D	5.0	20	35	ns
RSYNCn setup time to RCLKn↑	t_{SU}	20			ns
RSYNCn hold time after RCLKn↑	t_H	20			ns
RSYNCn period	t_{FCYC}		3.0		ms
RSYNCn pulse width (See Note 2)	t_{PW}		1 x t_{CYC}		ns

Notes:

1. The Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43). The system clock (RCLKn) and sync pulse (RSYNCn) are used to clock data out of the slip buffer when control bits RXC and RSE (bits 5 and 3 in register X02H) are 01. Control bit RXC selects the clock source, while RSE enables/disables the receive slip buffer. The position of RSYNCn with respect to the RDATAn/RSIGLn signals can be offset. The value written to register 018H compensates for any offset. RSYNCn is shown for an offset equal to zero.
2. Only one rising edge of RCLKn may occur during the time interval (t_{PW}) of the positive pulse for the RSYNCn input.
3. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK between 20-22 MHz.

Figure 14. Transmit Highway Timing - Transmission Mode



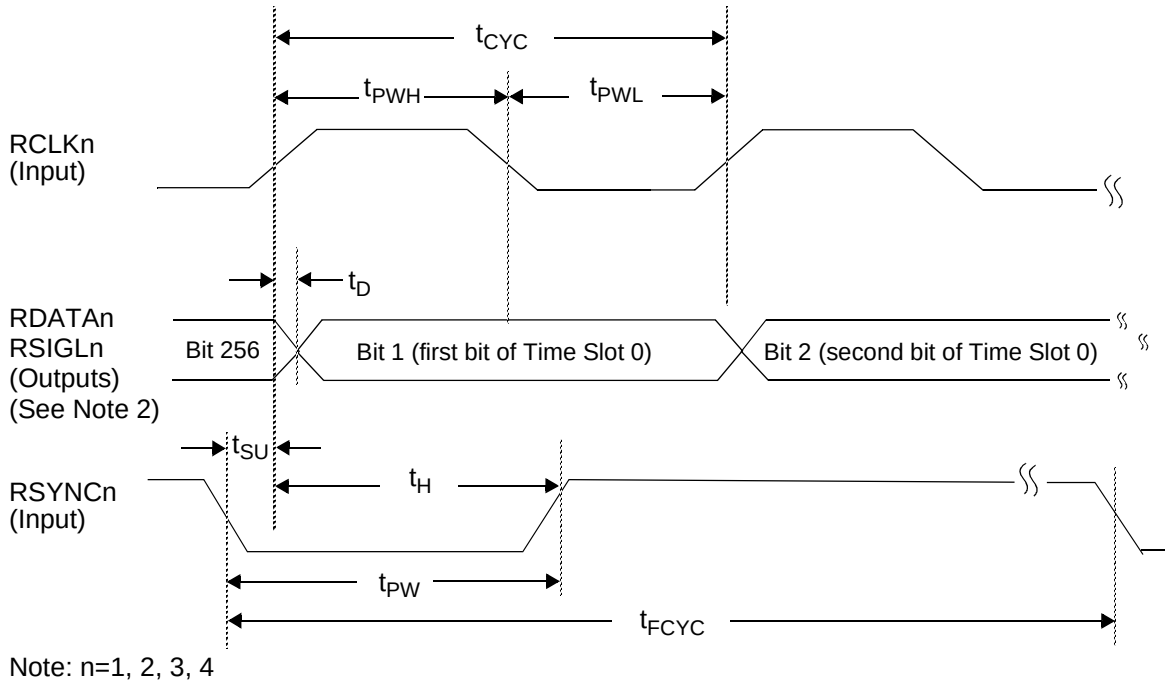
Note: n=1, 2, 3, 4

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}		648		ns
TCLKn low time (see Note 3)	t_{PWL}	240	324	408	ns
TCLKn high time (see Note 3)	t_{PWH}	240	324	408	ns
TDATAn/TSIGLn set-up time to TCLKn↑	$t_{SU(1)}$	20			ns
TDATAn/TSIGLn hold time after TCLKn↑	$t_{H(1)}$	20			ns
TSYNCn set-up time to TCLKn↑	$t_{SU(2)}$	20			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	20			ns
TSYNCn period	t_{FCYC}		3.0		ms
TSYNCn pulse width (See Note 2)	t_{PW}		1 x t_{CYC}		ns

Notes:

1. The Transmission Mode is selected when a low is placed on the CONFIG1 pin (pin 43). The position of TSYNCn may be offset with respect to the TDATAn/TSIGLn signals. The value written to register 017H compensates for any offset. TSYNCn is shown for an offset equal to zero.
2. Only one rising edge of TCLKn may occur during the time interval (t_{PW}) of the positive pulse for the TSYNCn input.
3. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK between 20-22 MHz.

Figure 15. Receive Highway Timing - MVIP Mode

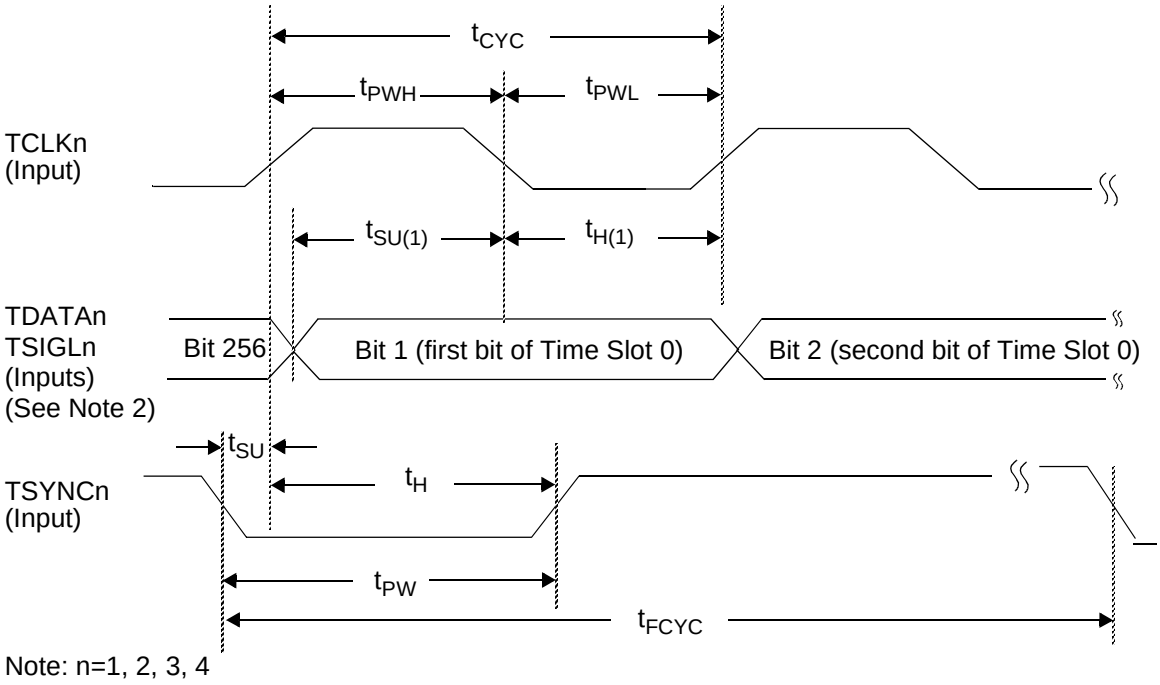


Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	465	488.3	513	ns
RCLKn low time	t_{PWL}	220	244	268	ns
RCLKn high time	t_{PWH}	220	244	268	ns
RDATAn/RSIGLn delay after RCLKn↑	t_D	5.0	8.0	15	ns
RSYNCn set-up time to RCLKn↑	t_{SU}	10			ns
RSYNCn hold time after RCLKn↑	t_H	5.0			ns
RSYNCn pulse width low time	t_{PW}	200	488	500	ns
RSYNCn period	t_{FCYC}		125		µs

Notes:

1. The MVIP Mode is selected when a high is placed on the CONFIG1 pin (pin 43). The receive slip buffer is always enabled in this mode. The position of RSYNCn may be offset with respect to the RDATAn/RSIGLn signals. The value written to register 018H compensates for any offset. RSYNCn is shown for an offset equal to zero.
2. For bit number per MVIP bit identification nomenclature, bit 256 is bit 0 of Time Slot 31, bit 1 is bit 7 of Time Slot 0 and bit 2 is bit 6 of Time Slot 0.

Figure 16. Transmit Highway Timing - MVIP Mode

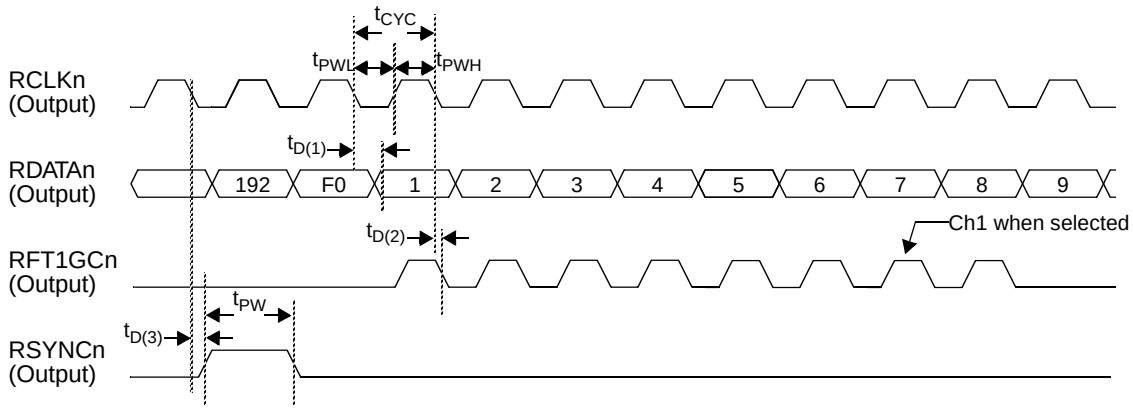


Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	480	488.3	497	ns
TCLKn low time	t_{PWL}	220	244	268	ns
TCLKn high time	t_{PWH}	220	244	268	ns
TDATAn/TSIGLn set-up time to TCLKn↓	$t_{SU(1)}$	10			ns
TDATAn/TSIGLn hold time after TCLKn↓	$t_{H(1)}$	10			ns
TSYNCn set-up time to TCLKn↑	t_{SU}	5.0			ns
TSYNCn hold time after TCLKn↑	t_{H}	5.0			ns
TSYNCn pulse width low time	t_{PW}	200	488	500	ns
TSYNCn period	t_{FCYC}		125		µs

Notes:

1. The MVIP Mode is selected when a high is placed on the CONFIG1 pin (pin 43). The transmit slip buffer is always enabled in this mode. The position of TSYNCn may be offset with respect to the TDATAn/TSIGLn signals. The value written to register 017H compensates for any offset. TSYNCn is shown for an offset equal to zero.
2. For bit number per MVIP bit identification nomenclature, bit 256 is bit 0 of Time Slot 31, bit 1 is bit 7 of Time Slot 0 and bit 2 is bit 6 of Time Slot 0.

Figure 17. Receive Highway Timing - Fractional T1 Gapped Clock (Transmission Mode)

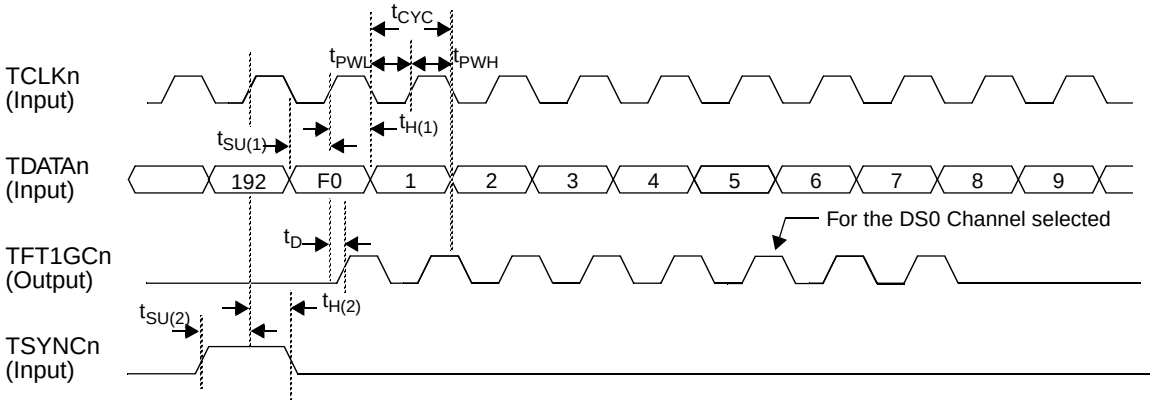


Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}		648		ns
RCLKn low time (see Note 2)	t_{PWL}	240	324	408	ns
RCLKn high time (see Note 2)	t_{PWH}	240	324	408	ns
RDATAn delay after RCLKn↓	$t_{D(1)}$	5.0	10	20	ns
RFT1GCn↓ delay after RCLKn↓	$t_{D(2)}$	12	20	25	ns
RSYNCn delay after RCLKn↓	$t_{D(3)}$	5.0	10	20	ns
RSYNCn pulse width	t_{PW}	500	648	750	ns

Notes

1. The fractional T1 gapped clock feature is enabled when the CONFIG1 pin is low and control bit FT1M (bit 0 in register X02H) is written with a 1. One or more DS0 channels may be selected by writing a 1 to one or more control bits RFD1-RFD24 (in registers X3AH-X3CH).
2. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK between 20-22 MHz.

Figure 18. Transmit Highway Timing - Fractional T1 Gapped Clock (Transmission Mode)

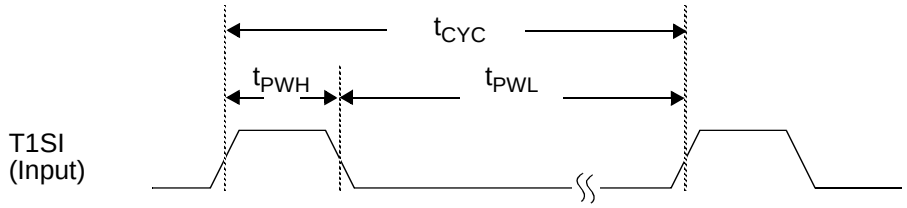


Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}		648		ns
TCLKn low time (see Note 2)	t_{PWL}	240	324	408	ns
TCLKn high time (see Note 2)	t_{PWH}	240	324	408	ns
TDATAn set-up time to TCLKn↑	$t_{SU(1)}$	20			ns
TDATAn hold time after TCLKn↑	$t_{H(1)}$	20			ns
TSYNCn set-up time to TCLKn↑	$t_{SU(2)}$	20			ns
TSYNCn hold time after TCLKn↑	$t_{H(2)}$	20			ns
TFT1GCn output delay from TCLKn↑	t_D	5.0	10	15	ns

Notes

1. The fractional T1 gapped clock feature is enabled when the CONFIG1 pin is low (Transmission Mode) and control bit FT1M (bit 0 in register X02H) is written with a 1. One or more DS0 channels may be selected by writing a 1 to one or more control bits TFD1-TFD24 (in registers X3DH-X3FH).
2. Usually, the minimum high time or low time has to be in the order of 290 ns for the part to be able to function over the entire SYSCLK range of 16-22 MHz. However, if line clock high or low times fall to 240 ns, the device can only operate satisfactorily with the SYSCLK between 20-22 MHz.

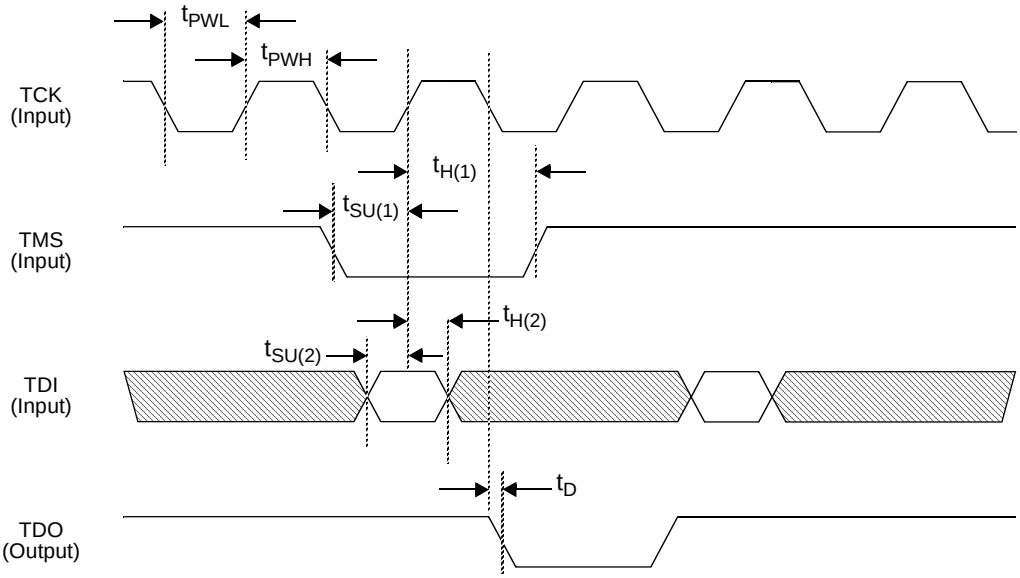
Figure 19. Shadow Register Timing



Parameter	Symbol	Min	Typ	Max	Unit
T1SI clock period	t_{CYC}		1.0		Sec
T1SI pulse width high	t_{PWH}	0.50	50	100	ms
T1SI pulse width low	t_{PWL}	6.0	950	980	ms

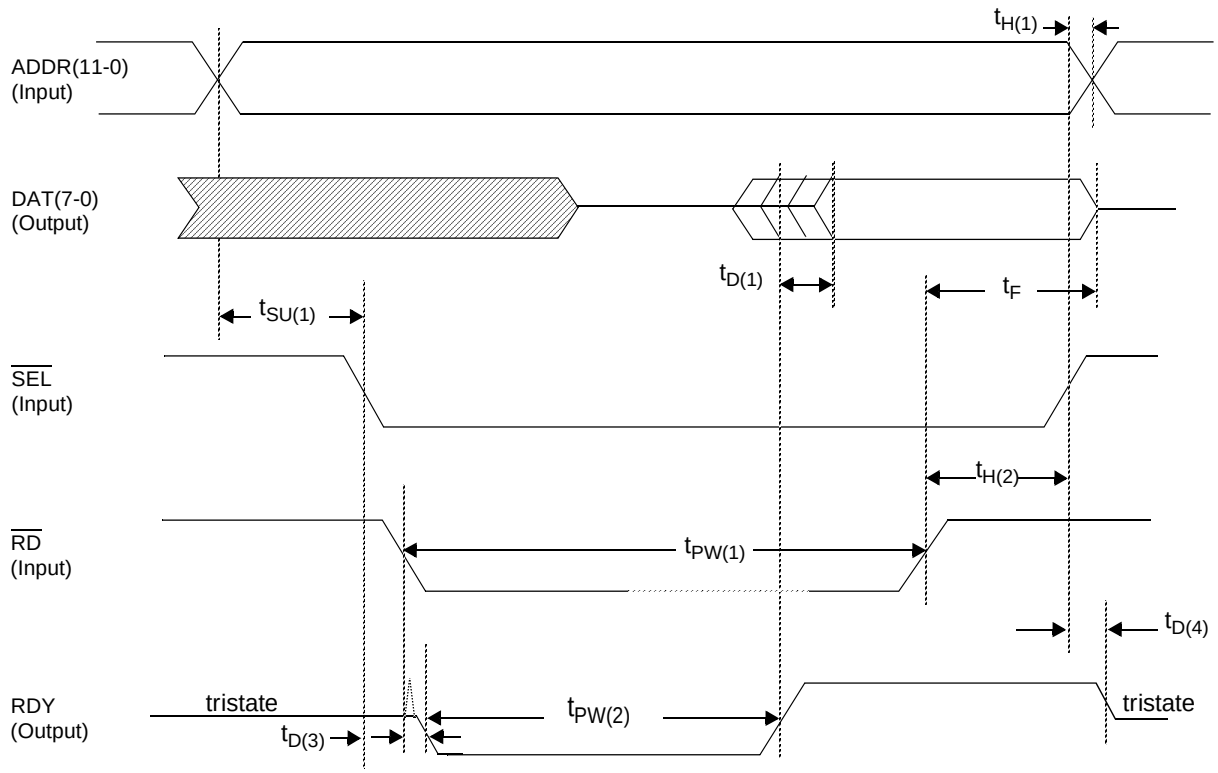
Note: The shadow register feature and this input are enabled when a 1 is written to control bit ENPMFM (bit 3 in register 006H).

Figure 20. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	5.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	5.0	-	ns
TDO delay from TCK↓	t_D	2.0	10	ns

Figure 21. Intel Microprocessor Read Cycle Timing

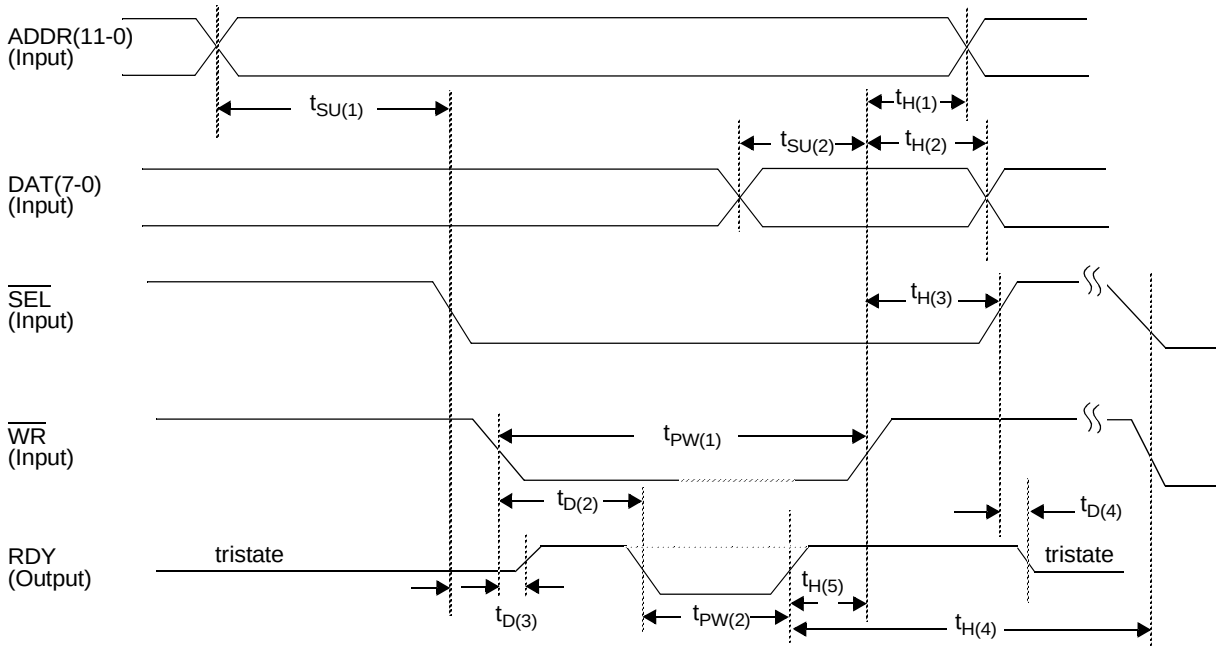


Parameter	Symbol	Min	Typ	Max	Unit
ADDR(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
ADDR(11-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
DAT(7-0) valid delay after RDY$\uparrow$	$t_{D(1)}$		-1/2 cycle of SYSCLK	-10	ns
DAT(7-0) float time after $\overline{RD}\uparrow$	t_F	4.0	10	15	ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{RD}$ pulse width low time (Note 3)	$t_{PW(1)}$	25			ns
RDY pulse width low time	$t_{PW(2)}$	2 cycles of SYSCLK	10 cycles of SYSCLK	15 cycles of SYSCLK	ns
RDY tristate to low delay after the latter of $\overline{SEL}\downarrow$ or $\overline{RD}\downarrow$ (See Note 4)	$t_{D(3)}$	5.0	7.0	20	ns
RDY high to tristate delay after $\overline{SEL}\uparrow$	$t_{D(4)}$	5.0			ns

Notes:

1. The Intel microprocessor bus is selected by placing a low on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 16-19 MHz (22 MHz max for V_{DD} = +5.0 volts).
3. Both $\overline{SEL}$ and $\overline{RD}$ must be simultaneously low for the specified $t_{PW(1)}$ interval.
4. As indicated in the waveform diagram, a brief excursion to the high state, of 2 or 3 ns duration, may occur when the RDY output leaves the tristate condition to go low.

Figure 22. Intel Microprocessor Write Cycle Timing

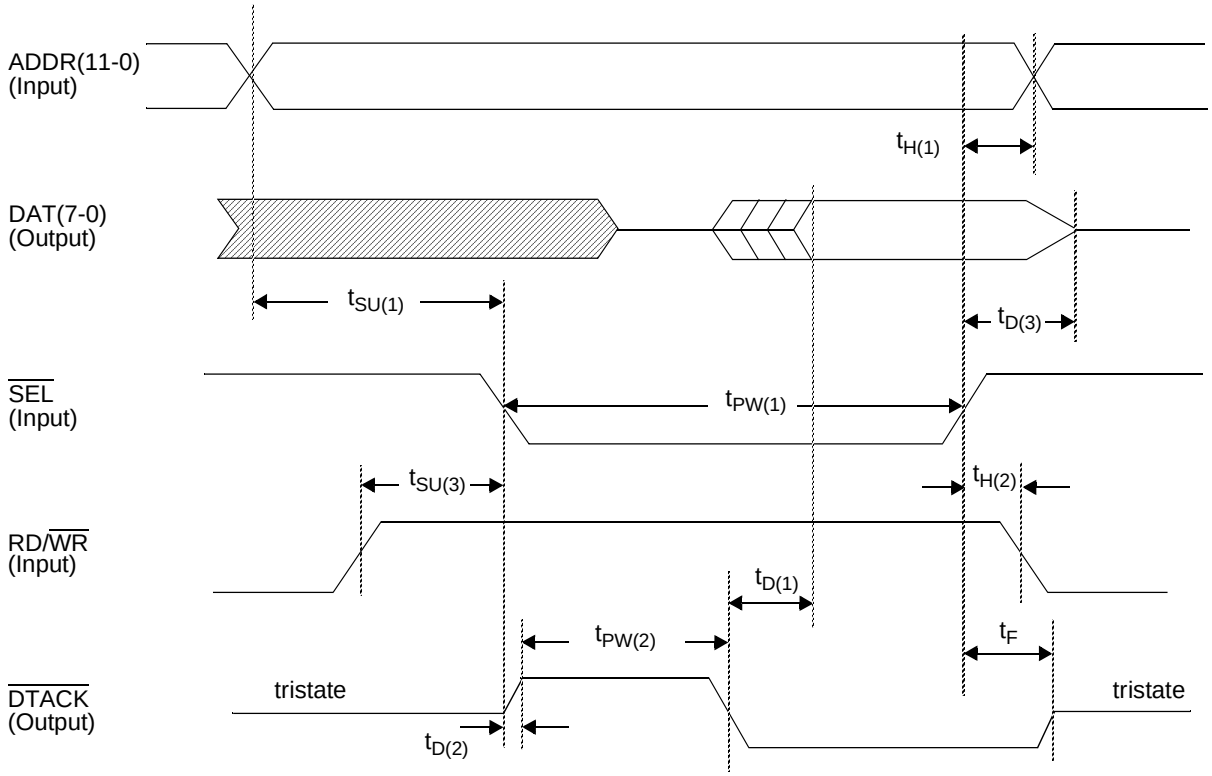


Parameter	Symbol	Min	Typ	Max	Unit
ADDR(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	5.0			ns
ADDR(11-0) hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{H(1)}$	10			ns
DAT(7-0) valid setup time to $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{SU(2)}$	10			ns
DAT(7-0) hold time after $\overline{WR}\uparrow$, $\overline{SEL}\uparrow$ (Note 4)	$t_{H(2)}$	10			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$ (Note 5)	$t_{H(3)}$	0.5			ns
$\overline{WR}$ pulse width low time/$\overline{SEL}$ pulse width low time (Note 5)	$t_{PW(1)}$	50			ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$	4.0	7.0	15	ns
RDY pulse width low time	$t_{PW(2)}$	0.0	7 cycles of SYSCLK*	10 cycles of SYSCLK*	ns
RDY tristate to high delay after the latter of $\overline{SEL}\downarrow$ or $\overline{WR}\downarrow$	$t_{D(3)}$	5.0	7.0	15	ns
RDY high to tristate delay after $\overline{SEL}\uparrow$	$t_{D(4)}$	5.0	7.0	15	ns
$\overline{WR}$ and $\overline{SEL}$ hold time after RDY goes high (Note 4)	$t_{H(5)}$	0.0			ns
RDY$\uparrow$ to $\overline{WR}\downarrow$, or $\overline{SEL}\downarrow$ (Note 6)	$t_{H(4)}$	2 cycles of SYSCLK			ns

Notes:

1. The Intel microprocessor bus is selected by placing a low on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 16-19 MHz (22 MHz max for V_{DD} = +5.0 volts).
3. * Wait states only occur if a write cycle immediately follows a previous read/write cycle (e.g., read, modify, write or word-wide write).
4. The timing is with respect to the earlier of the two rising edges.
5. As long as both $\overline{SEL}$ and $\overline{WR}$ are simultaneously low for the specified $t_{PW(1)}$ interval, $\overline{SEL}$ may rise prior to $\overline{WR}\uparrow$ ($t_{H(3)}$ is a negative Min).
6. When writing to address X0AH (HDLC transmit FIFO) only, allow a minimum of 2 cycles of SYSCLK between RDY$\uparrow$ and $\overline{SEL}\downarrow$ or $\overline{WR}\downarrow$.

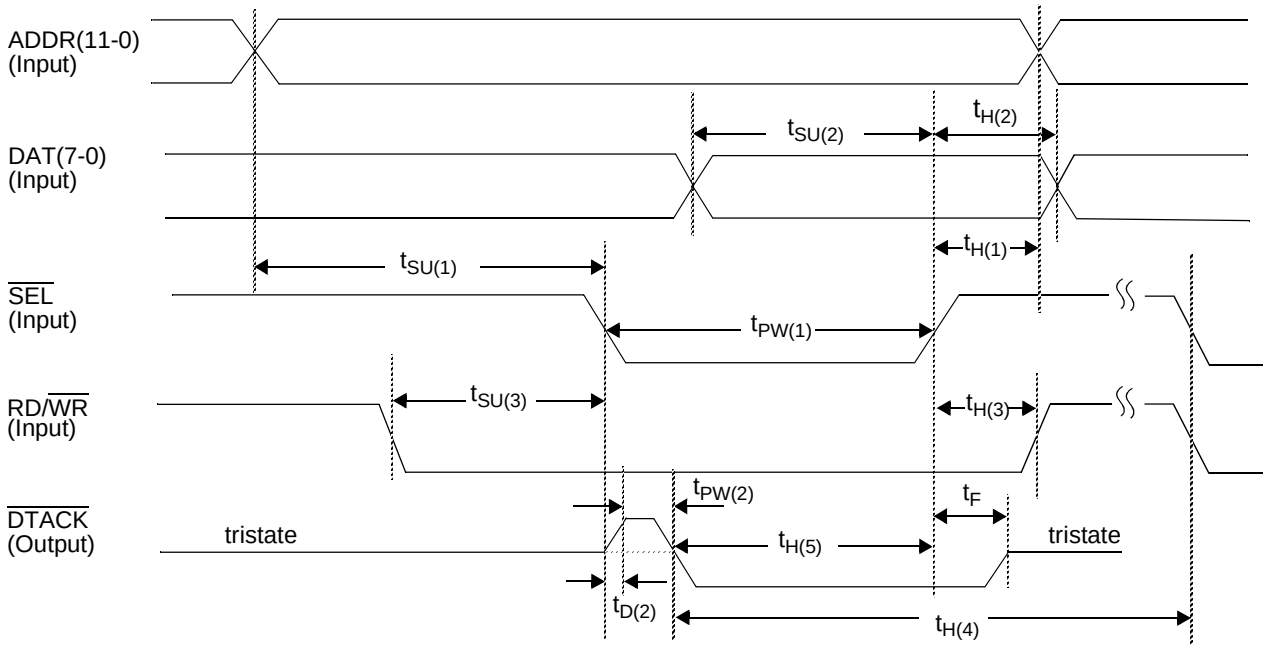
Figure 23. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
ADDR(11-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
DAT(7-0) delay to tristate after $\overline{SEL}\uparrow$	$t_{D(3)}$	3.0			ns
DAT(7-0) valid output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	-1 cycle of SYSCLK	-1/2 cycle of SYSCLK	-10	ns
$\overline{SEL}$ pulse width low time	$t_{PW(1)}$	50			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	10			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{DTACK}$ pulse width high time	$t_{PW(2)}$	2 cycles of SYSCLK	10 cycles of SYSCLK	15 cycles of SYSCLK	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	5.0	8.0	15	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	3.0	8.0	12	ns

Notes:
1. The Motorola microprocessor bus is selected by placing a high on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 16-19 MHz (22 MHz max for V_{DD} = +5.0 volts).

Figure 24. Motorola Microprocessor Write Cycle Timing

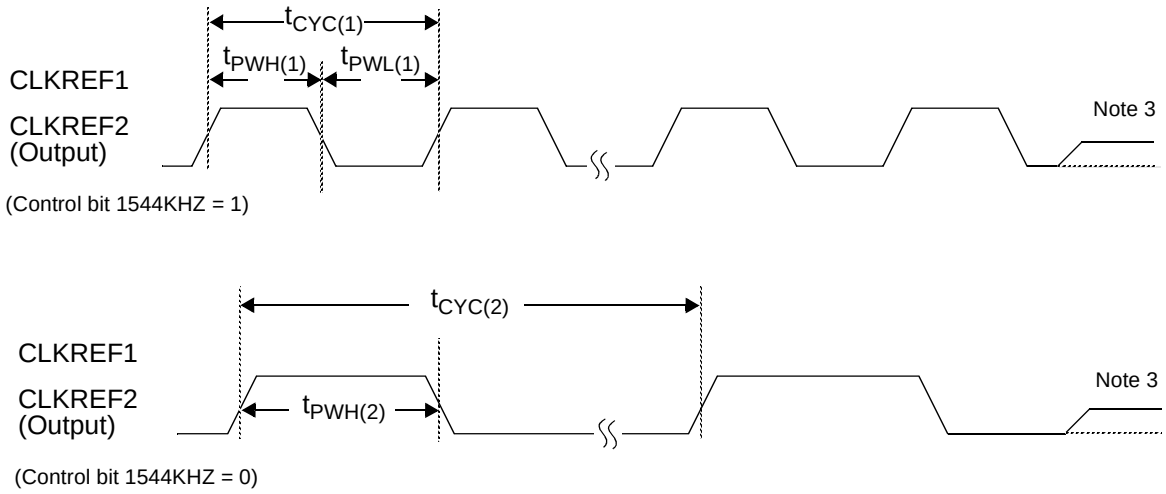


Parameter	Symbol	Min	Typ	Max	Unit
ADDR(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
ADDR(11-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	10			ns
DAT(7-0) valid setup time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	15			ns
DAT(7-0) hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	10			ns
$\overline{SEL}$ pulse width low time (Note 4)	$t_{PW(1)}$	50			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	10			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	10			ns
$\overline{DTACK}$ pulse width high time	$t_{PW(2)}$	0.0	10 cycles of SYSCLK*	15 cycles of SYSCLK*	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	3.0	7.0	12	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	3.0	7.0	12	ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(5)}$	0.0			ns
$\overline{DTACK}\downarrow$ to $\overline{SEL}\downarrow$ or RD/ $\overline{WR}\downarrow$ (Note 5)	$t_{H(4)}$	2 cycles of SYSCLK			ns

Notes:

1. The Motorola microprocessor bus is selected by placing a high on the MOTO pin (pin 99).
2. The system clock has a nominal frequency of 16-19 MHz (22 MHz max for V_{DD} = +5.0 volts).
3. * Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g., read, modify, write or word-wide write).
4. $\overline{SEL}$ and RD/$\overline{WR}$ must both be low simultaneously for the specified $t_{PW(1)}$ period.
5. When writing to address X0AH (HDLC transmit FIFO) only, allow a minimum of 2 cycles of SYSCLK between $\overline{DTACK}\downarrow$ and $\overline{SEL}\downarrow$ or RD/$\overline{WR}\downarrow$.

Figure 25. Clock Reference Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKREF1,2 clock period when control bit 1544KHZ = 1; see note 2	$t_{CYC(1)}$		648		ns
CLKREF1,2 high time when control bit 1544KHZ = 1; see note 2	$t_{PWH(1)}$		324		ns
CLKREF1,2 low time when control bit 1544KHZ = 1; see note 2	$t_{PWL(1)}$		324		ns
CLKREF1,2 clock period when control bit 1544KHZ = 0; see note 2	$t_{CYC(2)}$		125		ms
CLKREF1,2 high time when control bit 1544KHZ = 0; see note 2	$t_{PWH(2)}$	560	648		ns

Notes:

1. CLKREF1 and CLKREF2 output pins are controlled by register 019H. Control bit 1544KHZ selects either a direct clock output when set to 1 or via a divide by 193 circuit when set to 0. Control bits ENREF1 and ENREF2 enables output pins CLKREF1 and CLKREF2 when set to 1; when ENREF1 and ENREF2 are set to 0 CLKREF1 and CLKREF2 are tristated. The particular receive clock LRCLKn used as a reference is selected by control bits CR1S1,2 for CLKREF1 and control bits CR2S1,2 for CLKREF2.
2. The actual clock period and high or low times are a function of the selected clock LRCLKn.
3. A fault detected (LOS or LINT pin active if enabled by control bit LIE) by the particular channel selected for the reference clock will cause CLKREF1,2 to stay low. The output only goes to tristate if control bit ENREF1 or ENREF2 is set to 0.

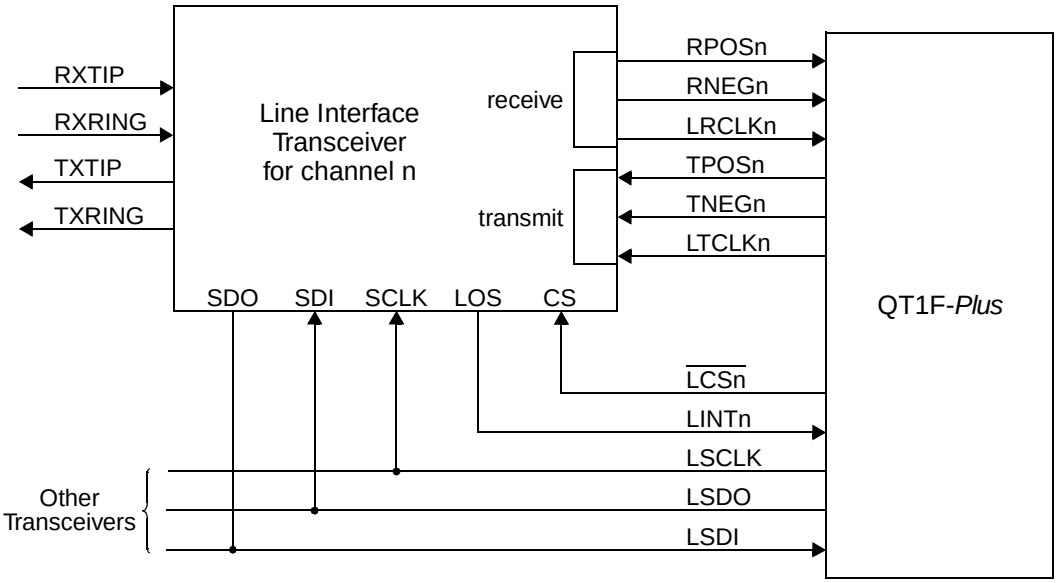
OPERATION

The following sections detail the internal operation of the QT1F-*Plus*.

LINE INTERFACE SELECTION

Each of the four framers in the QT1F-*Plus* can be programmed to provide either a dual unipolar interface or a NRZ interface. The dual unipolar interface is selected when a 1 is written into control bit RAIL (bit 7) in the Framer Configuration register located at address X00H in the memory map. The X stands for the framer selected, and will be equal to the value n used to identify the framer (1 for framer 1, 2 for framer 2, etc.). The B8ZS line or AMI coder/decoder (CODEC) feature can be selected for the dual unipolar interface. The B8ZS CODEC is selected by writing a 1 to control bit BE (bit 6) in the Framer Configuration register X00H. A 0 will select an AMI CODEC. The B8ZS stands for Bipolar with eight Zero Substitution, which is described in ANSI Document ANSI T1.102-1993 and other Bellcore documents.

The clock polarity of the input and output line clocks is selectable by writing the sense required to control bits TXCP and RXCP (bits 7 and 6) in the Framer Configuration register X01H. When a framer is configured for the dual unipolar mode, the line signal is monitored for loss of signal (LOS). LOS is detected if no transitions are present for 175 ± 75 pulse positions. Recovery occurs when a ones density of 12.5% or more is detected in 175 ± 75 pulse positions. The connections between a QT1F-*Plus* framer and external line interface transceivers are shown in Figure 26 below for dual unipolar mode.

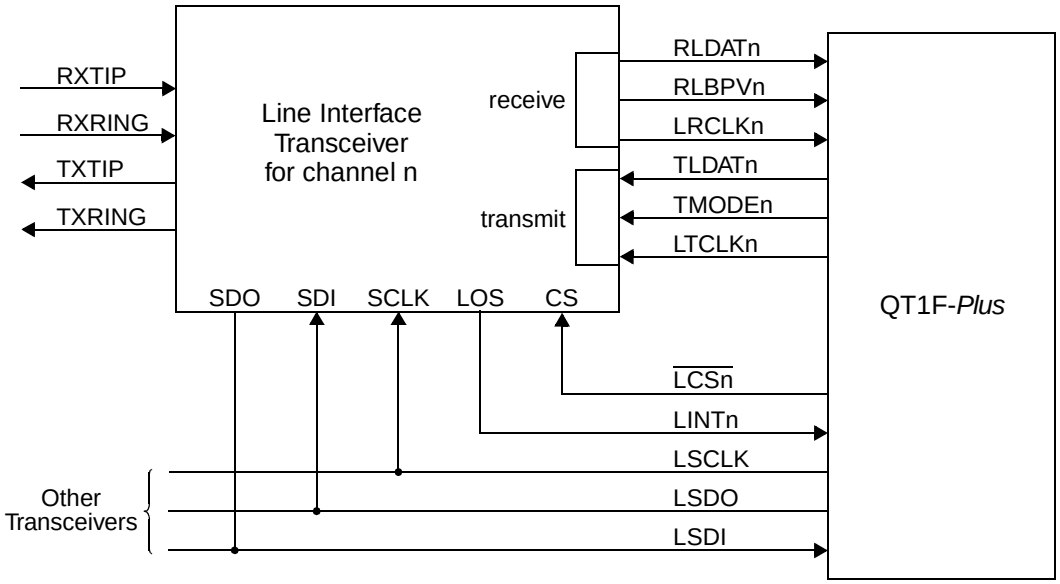


Note: n is the channel number (1, 2, 3, 4)

Figure 26. Line Interface For Dual Unipolar Mode

The NRZ interface is selected when a 0 is written into control bit RAIL (bit 7) in register X00H. The clock polarity of the line input and output clocks is selectable by writing to control bits TXCP and RXCP (bits 7 and 6) in the Framer Configuration register X01H. Options are provided for inverting the polarity of the transmit and receive data pins. A 1 written to control bit TXNRZP (bit 5) in register X01H inverts the polarity of the transmit data signal, TLDATn, while a 1 written to control bit RXNRZP (bit 0) in the same register inverts the polarity of the receive data signal RLDATn. In NRZ mode, the RNEGn pin may be used to input an external indication of coding violations (RLBPVn) or a fast sync pulse for testing purposes (RFSn). External coding violations are counted in a 16-bit performance counter when control bit RXFS (bit 1) in register X06H is a 0. Coding violations are counted when the input is high for rising edges of the line clock LRCLKn. When control bit RXFS is a 1, this pin is used for inputting a receive fast sync pulse.

In the transmit direction, when the NRZ mode is selected, the TNEGn pin becomes a TFSn or TMODEn pin. The pin may be used to output a fast sync pulse (TFSn), or it may be used as a general purpose output pin (TMODEn). When control bit TXFS (bit 0) in register X06H is a 1, a fast sync output pulse is provided on this pin. When control bit TXFS is a 0, this pin can be used as a general purpose output pin. The output state is defined by the value written to bit BE (bit 6) in register X00H. A typical interface between a framer in the QT1F-*Plus* and an external line transceiver is shown in Figure 27 below for the NRZ mode.



Note: n is the channel number (1, 2, 3, 4)

Figure 27. Line Interface For NRZ Mode

LINE INTERFACE CONTROL

This interface permits the microprocessor to have complete control of the four external line interface transceivers through the QT1F-*Plus*. This interface is selected by placing a low on the CONFIG2 pin (pin 42). The line interface control leads are common to all four framers and comprise a data input pin (LSDI), a data output pin (LSDO), and a clock output pin (LSCLK). The clock signal LSCLK is derived from the signal at the LO pin (pin 41) and has the same clock period. Individual chip select pins (LCSn) are used between the QT1F-*Plus* and the external transceivers to determine which of the four external transceivers is to be accessed through the QT1F-*Plus*. In addition, general purpose input leads (LINTn) are provided. The signal on this lead is locally OR-gated with the internal loss of signal alarm when control bit LIE (bit 1) in the Framer Configuration register X00H is a 1. The operating sense of this lead is programmable by control bit LPOL (bit 0) in the Framer Configuration register X00H. The status indication of this pin is given by the LINT status bit (bit 0) in register X15H. Typical interfaces between the QT1F-*Plus* and external line interface transceivers using the line interface control pins are shown in Figures 26 and 27, for the dual unipolar and NRZ interface modes, respectively.

Data to be written to the external transceiver is formatted as a two-byte message. The first byte is an address/command byte and the second byte contains the data to be written or read. Figure 28 illustrates the message and control formats associated with the transceiver serial input/output timing.

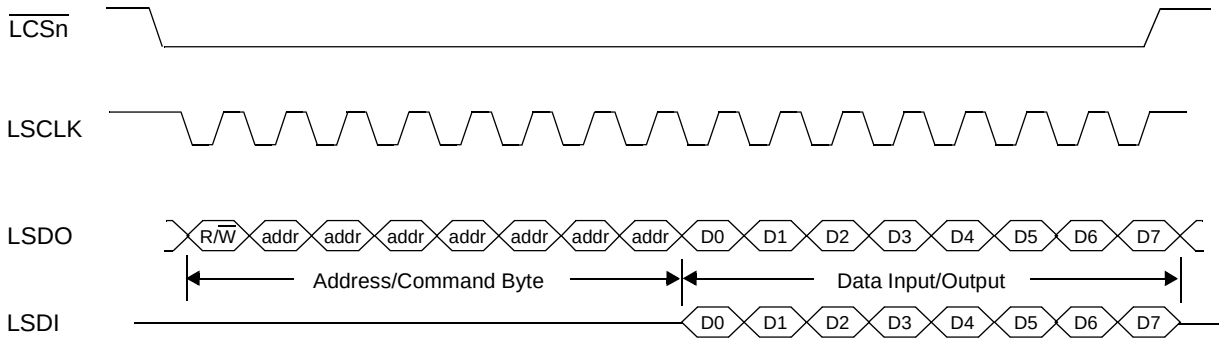


Figure 28. Transceiver Serial Input/Output Timing

The format of the address/command byte depends upon the external transceiver being controlled. Please refer to the transceiver's data sheet for the command/data formats. The interface for controlling the external transceiver operates in the following way. The external transceiver selection (via LCSn) is determined by the value written to two T1CHCS bits (bits 1 and 0) in register 013H. For example, a 00 value selects the transceiver for framer 1 while a 11 value selects the transceiver for framer 4. The microprocessor writes the command byte to LCB7-LCB0 in the Line Interface Control register 010H. This is followed by writing the data byte to LDO7-LDO0 in Line Interface Control register 011H. The serial message is sent on LSDO when a 1 is written to replace the 0 in the ESP/EMON bit (bit 4) in register 013H. The ESP/EMON bit must be first written with a 0, followed by a 1, before another transfer can take place between the QT1F-*Plus* and the external transceiver selected. Broadcast capability to all transceivers is enabled when the control bit BDCST (bit 7) in register 013H is written with a 1. Eight clock cycles later, the selected transceiver will respond by sending serial data on the LSDI input pin. The data is shifted in LSB first to LDI7-LDI0 in the Serial Port Data Input Register 012H.

MONITOR MODE

The monitor mode interface permits the QT1F-*Plus* to provide an external receive or transmit NRZ signal from one of the framers to an external device. This interface is selected by placing a high on the CONFIG2 pin (pin 42). Please note that the pins for this mode are shared with the line control interface, and if the monitor mode is selected, these pins cannot be used to provide a serial interface between the external transceivers and the QT1F-*Plus*. In addition, a 1 must be written into the ESP/EMON control bit (bit 4) in the Global Configuration register 013H to enable the monitor mode interface output pins. A 0 written into this control bit causes these data and clock pins to be tristated, permitting multiple QT1F-*Plus* devices to share an external device.

A 1 written to control bit RXTX (bit 3) in register 013H selects the receive side, while a 0 selects the transmit side. The framer to be monitored is selected by the value written into the two T1CHCS bits (bits 1 and 0) in register 013H. For example, a value of 00 selects framer 1, and a value of 11 selects framer 4. The selected framer NRZ signal is provided on output pin MONDTO (pin 60). The NRZ receive or transmit data is clocked out on rising edges of the clock MONCLK (pin 61).

SYSTEM INTERFACE

The system interface connects each of the four framers within the QT1F-*Plus* to and from the system. The system interface is selected by the CONFIG1 input pin, according to the table given below.

CONFIG1 Pin 43	System Interface
Low	**Transmission Mode.** Data highway, signaling highway, 1.544 MHz clock and 3 ms sync pulse for each framer in both transmit and receive directions. Sync pulse is positive, and one clock cycle wide. The system receive clock and sync pulse may be outputs when slip buffer is bypassed.
High	**MVIP Mode:** Data highway, signaling highway, 2.048 MHz clock, and 125 microsecond sync pulse for each framer in both transmit and receive directions. The slip buffers must be enabled. The system receive and transmit clock and sync pulses are inputs to the QT1F-*Plus*. The negative sync pulses are one clock cycle wide.

For the Transmission and MVIP Modes, each framer has separate transmit and receive interfaces that are referred to as receive and transmit highways. Each highway consists of a data bus (i.e., data highway) RDATAn/TDATAn, a signaling bus (i.e., signaling highway) RSIGLn/TSIGLn, a clock RCLKn/TCLKn, and a synchronization signal RSYNCn/TSYNCn. Internally, each data bus is connected to a two-frame slip buffer, and each signaling bus is connected to a 96-bit signaling buffer. Please note that control bits are provided which enable the slip buffers to be bypassed when the Transmission Mode is selected. For the MVIP Mode, the receive and transmit slip buffers must be enabled by setting control bits RSE (bit 3), and TSE (bit 4) in register X02H to a 1. Please note also that in the Transmission Mode, with the slip buffers bypassed, and the signaling disabled, signaling information contained in the data stream is passed through transparently.

TRANSMISSION MODE

The Transmission Mode is enabled when a low is placed on the CONFIG1 pin (pin 43).

Transmit Highway

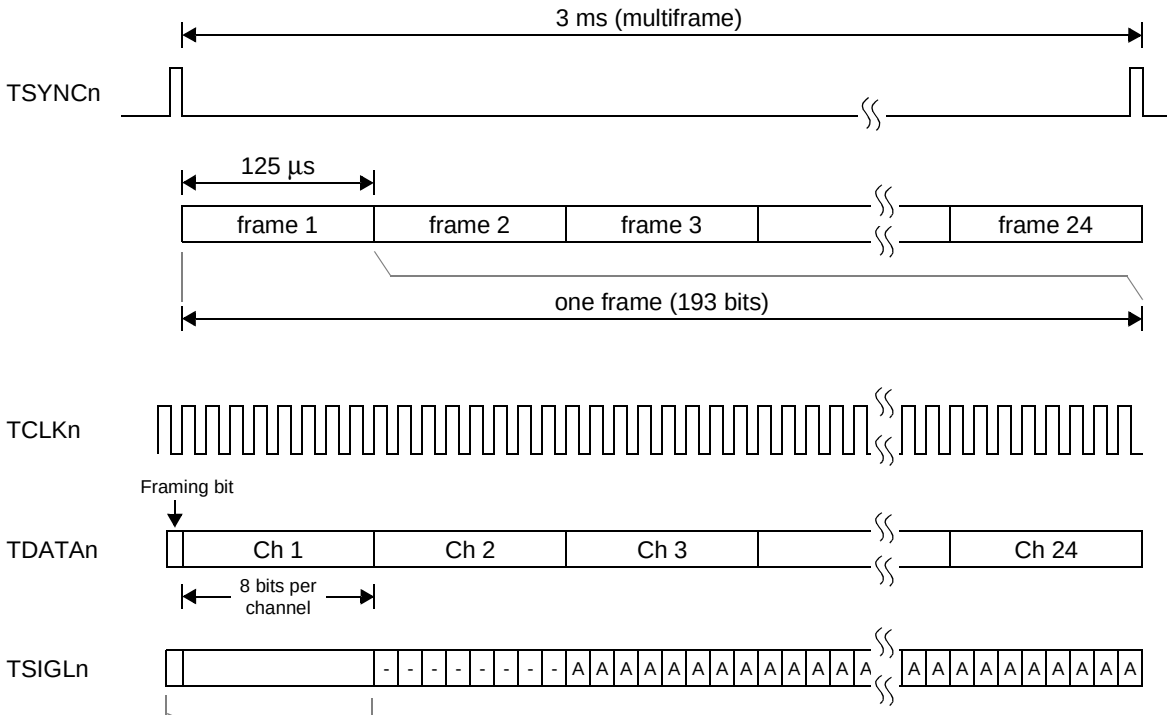
When the Transmission Mode is selected, the transmit highway carries information from the system to the QT1F-*Plus* for each framer. The highway is subdivided into two time division multiplexed buses, one for data (TDATAn), and the other one for signaling and alarms (TSIGLn). The n in the TDATAn and TSIGLn signals represents one of the four framers. The two buses are synchronous with respect to the highway clock (TCLKn), which has a clock rate of 1544 kHz. The data highway is a single bit-serial bus organized into 193-bit groups called frames, with the bits in each group numbered 0 through 192. Each frame consists of 24 DS0 channels, numbered from 1 to 24, as shown in Figure 29. Bit 0 carries the frame synchronization bit and multiframe bit for the SF frame format, and synchronization bits. Also note that 24 frames form a multiframe, with the beginning of each multiframe identified by an active high synchronization pulse (TSYNCn), one (TCLKn) clock cycle wide, which occurs every 3 ms, normally at the end of frame 24. Each multiframe carries one Extended Superframe (ESF) or two regular Superframes (SF). The position of the TSYNCn pulse is programmable to any bit position within the data bus frame using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to bit 8 in DS0 Channel 24 in frame 24 when a value of 00H is written into this register.

The signaling bus (TSIGLn) is also divided into 193-bit frames. Each signaling frame consists of 193 bits of signaling and alarm information for the 24 DS0 channels, numbered from 1 to 24, that are carried on the data bus.

The first bit in the signaling highway is assigned to carry the framing bits for the SF and ESF frame formats. The transmit section of the framer will rewrite the Ft and Fs for the SF frame format. The framer will rewrite the Ft bits, and recalculate the CRC for the ESF frame format. The HDLC link D bits (m-bits) may be inserted from the signaling highway. The sync pulse (TSYNC) determines the start of the frame and the first frame in the multiframe.

The S1, S2, S3 and S4 bits represent the ABCD signaling states associated with each of the DS0 channels. For example, if 16-state signaling is selected, frame 1 will carry the A1, A2, A3 and A4 signaling states in the S1, S2, S3 and S4 bits for DS0 channels 1, 2, 3 and 4. Frame 2 in the multiframe will carry the A5, A6, A7 and A8 signaling states in the S1, S2, S3 and S4 bits for DS0 channels 5, 6, 7 and 8, while frame 24 in the multiframe will carry the D21, D22, D23 and D24 signaling states in the S1, S2, S3 and S4 bits for DS0 channels 21, 22, 23 and 24. The QT1F-*Plus* inserts the signaling bits from the signaling highway into the robbed bit positions if enabled by control bits SE1 through SE24 in registers XE8, XE9, and XEA.

The next bit is defined as the Y bit and defines the system remote defect indication alarm (Yellow) alarm. The next 11 bits are not used. The bits in channels 3 through 24 carry a system AIS alarm indication (A). Status bits VTAIS (bit 3) and VTRDI (bit 2) in register X14H provide the active states of the AIS bits and a remote defect indication on the signaling highway in the Transmission Mode. These VT alarms correspond to alarms that are present for a system SONET byte synchronous interface.



Frame	SF/ESF	16-St. TSIGL; S_1-S_4	TSIGL; S_1-S_4	4-State; S_1-S_4	2-State; S_1-S_4
1	Ft/DI	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04
2	Fs/CRC	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08
3	Ft/DI	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12
4	Fs/Ft	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16
5	Ft/DI	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20
6	Fs/CRC	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24
7	Ft/DI	B01, B02, B03, B04	B01, B02, B03, B04	B01, B02, B03, B04	A01, A02, A03, A04
8	Fs/Ft	B05, B06, B07, B08	B05, B06, B07, B08	B05, B06, B07, B08	A05, A06, A07, A08
9	Ft/DI	B09, B10, B11, B12	B09, B10, B11, B12	B09, B10, B11, B12	A09, A10, A11, A12
10	Fs/CRC	B13, B14, B15, B16	B13, B14, B15, B16	B13, B14, B15, B16	A13, A14, A15, A16
11	Ft/DI	B17, B18, B19, B20	B17, B18, B19, B20	B17, B18, B19, B20	A17, A18, A19, A20
12	Fs/Ft	B21, B22, B23, B24	B21, B22, B23, B24	B21, B22, B23, B24	A21, A22, A23, A24
13	Ft/DI	C01, C02, C03, C04	C01, C02, C03, C04	A01, A02, A03, A04	A01, A02, A03, A04
14	Fs/CRC	C05, C06, C07, C08	C05, C06, C07, C08	A05, A06, A07, A08	A05, A06, A07, A08
15	Ft/DI	C09, C10, C11, C12	C09, C10, C11, C12	A09, A10, A11, A12	A09, A10, A11, A12
16	Fs/Ft	C13, C14, C15, C16	C13, C14, C15, C16	A13, A14, A15, A16	A13, A14, A15, A16
17	Ft/DI	C17, C18, C19, C20	C17, C18, C19, C20	A17, A18, A19, A20	A17, A18, A19, A20
18	Fs/CRC	C21, C22, C23, C24	C21, C22, C23, C24	A21, A22, A23, A24	A21, A22, A23, A24
19	Ft/DI	D01, D02, D03, D04	D01, D02, D03, D04	B01, B02, B03, B04	A01, A02, A03, A04
20	Fs/Ft	D05, D06, D07, D08	D05, D06, D07, D08	B05, B06, B07, B08	A05, A06, A07, A08
21	Ft/DI	D09, D10, D11, D12	D09, D10, D11, D12	B09, B10, B11, B12	A09, A10, A11, A12
22	Fs/CRC	D13, D14, D15, D16	D13, D14, D15, D16	B13, B14, B15, B16	A13, A14, A15, A16
23	Ft/DI	D17, D18, D19, D20	D17, D18, D19, D20	B17, B18, B19, B20	A17, A18, A19, A20
24	Fs/Ft	D21, D22, D23, D24	D21, D22, D23, D24	B21, B22, B23, B24	A21, A22, A23, A24

Figure 29. Transmit Highway - Transmission Mode

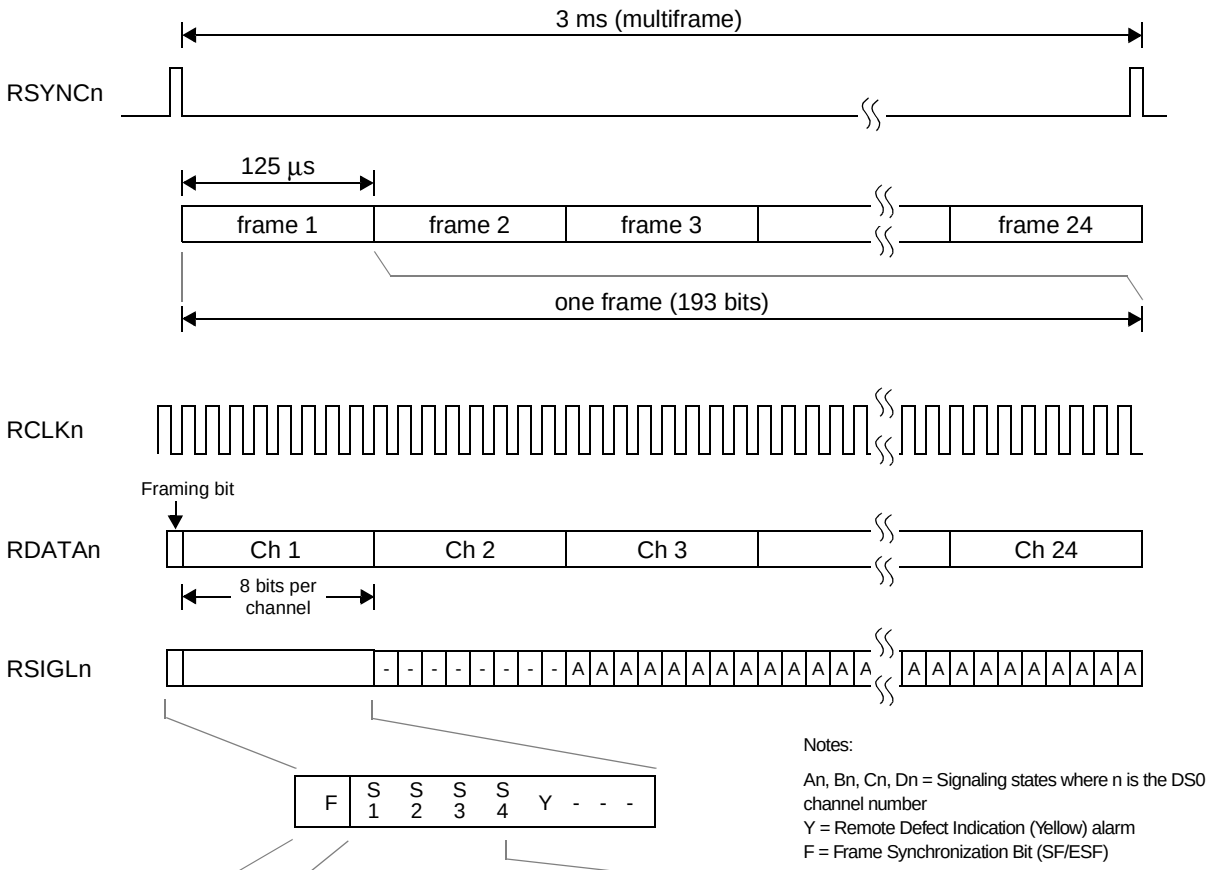
Receive Highway

In the Transmission Mode, the receive highway for each framer carries information from the QT1F-*Plus* to the system. Like the transmit path, the receive highway is also subdivided into two time division multiplexed buses, one for data (RDATAn), and one for signaling and alarms (RSIGLn), where n represents one of the four framers. The two buses are synchronous with the highway clock (RCLKn), which has a clock rate of 1544 kHz. The clock (RCLKn) is either an output to the system or an input from the system. The system clock (RCLKn) or the line clock (LRCLKn) may be the input clock source for the slip buffer when it is enabled. Usually the system clock (RCLKn) is used. The QT1F-*Plus* sources the clock (RCLKn) as an output when the slip buffer is bypassed. The receive slip buffer for a framer is disabled when a 0 is written to the RSE bit (bit 3) in the Framer Configuration register X02H. The clock source selection is determined by the RXC bit (bit 5) in register X02H. A 0 written into this bit position selects the system clock (RCLKn) as the source clock. In addition to controlling the source of the clock, control bit RXC also controls the source of the sync pulse.

The data bus is a single bit-serial bus organized into 193-bit groups called frames, as shown in Figure 30. Each frame consists of 24 time slots, plus a frame synchronization bit, as shown for the transmit interface. Twenty-four frames form a multiframe, with the beginning of each multiframe identified by an active high synchronization pulse (RSYNCn), one (RCLKn) clock cycle wide, which occurs every 3 ms, normally at the end of frame 24. Each multiframe carries one Extended Superframe (ESF) or two regular Superframes (SF). The position of the RSYNCn pulse is programmable to any bit position within the frame using control bits RSD7-RSD0 in register 018H. The synchronization pulse is aligned to bit 8 in DS0 Channel 24 in frame 24 when a value of 00H is written into this register.

The signaling bus (RSIGLn) is also divided into 193-bit frames. Each signaling frame consists of 193 bits of signaling and alarm information for the 24 data channels carried on the data bus. The first bit in the signaling highway carries the framing bits for the SF and ESF frame formats which are the line framing bits. The S1, S2, S3 and S4 bits represent the ABCD signaling states associated with each of the DS0 channels. For example, if 16-state signaling is selected, frame 1 will carry the A1, A2, A3 and A4 signaling states in the S1, S2, S3, and S4 bits for DS0 channels 1, 2, 3 and 4. Frame 2 in the multiframe will carry the A5, A6, A7 and A8 signaling states in the S1, S2, S3 and S4 bits for DS0 channels 5, 6, 7 and 8, while frame 24 in the multiframe will carry the D21, D22, D23 and D24 signaling states in the S1, S2, S3 and S4 bits for DS0 channels 21, 22, 23 and 24.

The next bit is defined as the Y bit and provides the system with the line Yellow alarm status. The next 11 bits are not used. The bits in channels 3 through 24 carry an AIS alarm indication (A). Control bits ENAIS, ENOOF, and ENLOS (bits 2, 1, and 0 of register X03H), when set to 1, enable the A bits to be set to a 1 if AIS, OOF, or LOS is detected.



Frame	SF/ESF	16-St. RSIGL; S_1-S_4	RSIGL; S_1-S_4	4-State; S_1-S_4	2-State; S_1-S_4
1	Ft/DI	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04
2	Fs/CRC	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08
3	Ft/DI	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12
4	Fs/Ft	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16
5	Ft/DI	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20
6	Fs/CRC	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24
7	Ft/DI	B01, B02, B03, B04	B01, B02, B03, B04	B01, B02, B03, B04	A01, A02, A03, A04
8	Fs/Ft	B05, B06, B07, B08	B05, B06, B07, B08	B05, B06, B07, B08	A05, A06, A07, A08
9	Ft/DI	B09, B10, B11, B12	B09, B10, B11, B12	B09, B10, B11, B12	A09, A10, A11, A12
10	Fs/CRC	B13, B14, B15, B16	B13, B14, B15, B16	B13, B14, B15, B16	A13, A14, A15, A16
11	Ft/DI	B17, B18, B19, B20	B17, B18, B19, B20	B17, B18, B19, B20	A17, A18, A19, A20
12	Fs/Ft	B21, B22, B23, B24	B21, B22, B23, B24	B21, B22, B23, B24	A21, A22, A23, A24
13	Ft/DI	C01, C02, C03, C04	C01, C02, C03, C04	A01, A02, A03, A04	A01, A02, A03, A04
14	Fs/CRC	C05, C06, C07, C08	C05, C06, C07, C08	A05, A06, A07, A08	A05, A06, A07, A08
15	Ft/DI	C09, C10, C11, C12	C09, C10, C11, C12	A09, A10, A11, A12	A09, A10, A11, A12
16	Fs/Ft	C13, C14, C15, C16	C13, C14, C15, C16	A13, A14, A15, A16	A13, A14, A15, A16
17	Ft/DI	C17, C18, C19, C20	C17, C18, C19, C20	A17, A18, A19, A20	A17, A18, A19, A20
18	Fs/CRC	C21, C22, C23, C24	C21, C22, C23, C24	A21, A22, A23, A24	A21, A22, A23, A24
19	Ft/DI	D01, D02, D03, D04	D01, D02, D03, D04	B01, B02, B03, B04	A01, A02, A03, A04
20	Fs/Ft	D05, D06, D07, D08	D05, D06, D07, D08	B05, B06, B07, B08	A05, A06, A07, A08
21	Ft/DI	D09, D10, D11, D12	D09, D10, D11, D12	B09, B10, B11, B12	A09, A10, A11, A12
22	Fs/CRC	D13, D14, D15, D16	D13, D14, D15, D16	B13, B14, B15, B16	A13, A14, A15, A16
23	Ft/DI	D17, D18, D19, D20	D17, D18, D19, D20	B17, B18, B19, B20	A17, A18, A19, A20
24	Fs/Ft	D21, D22, D23, D24	D21, D22, D23, D24	B21, B22, B23, B24	A21, A22, A23, A24

Figure 30. Receive Highway - Transmission Mode

MVIP MODE

The MVIP Mode is enabled when a high is placed on the CONFIG1 pin (pin 43).

Transmit Highway

In the MVIP Mode, the transmit highway for each framer in the QT1F-*Plus* carries input information from the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (TDATAn), and one for signaling (TSIGLn). The two buses are synchronous with the highway clock (TCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two time slots, 24 of which carry the 24 DS0 channels, as shown in the table below and in Figure 31.

TDATAn time slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1 DS0 No.	X	1	2	3	X	4	5	6	X	7	8	9	X	10	11	12	X	13	14	15	X	16	17	18	X	19	20	21	X	22	23	24

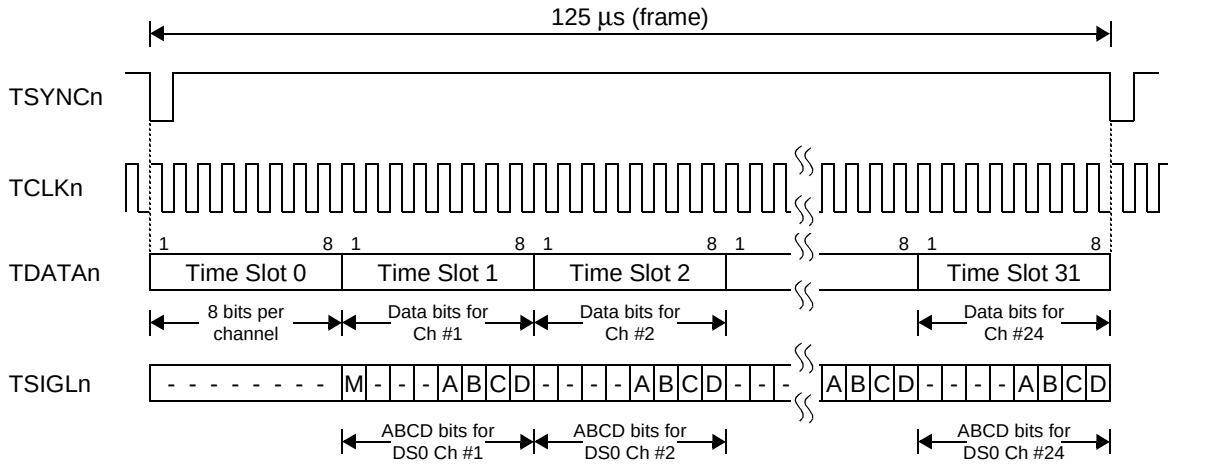
The frame start is identified by a synchronization pulse (TSYNCn), which is one (TCLKn) clock cycle wide and occurs every 125 microseconds. The position of the TSYNCn pulse is programmable to any bit position within the frame using control bits TSD7-TSD0 in register 017H. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The signaling bus (TSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 24 time slots carry the ABCD signaling bits associated with the 24 DS0 channels. Like the Data highway, Time Slots 0, 4, 8, 12, 16, 20, 24 and 28 do not carry signaling information. The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The first four bits in each signaling bus time slot should be set to zero.

The signaling buffer is updated every other frame. The line signaling states are updated once every six frames. For 2 or 4-state signaling, the signaling buffer uses only the A or AB values to update the signaling buffer

The control bit BFDL (bit 1 of register X01H), when set to a 1, will cause the transfer of the m-bits (FDL channel) from the transmit signaling highway (TSIGLn) instead of generating them internally for the ESF mode of operation. In SF mode, the Fs bit is taken from the transmit signaling highway (TSIGLn) instead of being generated internally. Since the m-bits or the Fs bits are taken every other frame, and since no multiframe indication is provided in MVIP Mode, each bit to be bypassed must be present for two frames on TSIGLn. Changes in the slip buffer have no effect on this function. The purpose is to permit an alternative way of generating the FDL channel. Figure 31 details the placement of the m-bit or Fs bit.

Please note that, in MVIP Mode, none of the data highway clocks (RCLKn, TCLKn or the LO clock) should be shut off when the slip buffer is enabled. This could result in constant slip even after the clock(s) are restored.



Notes:
ABCD = Signaling bits for channel c (1-24).
Time Slots 0, 4, 8, 12, 16, 20, 24 and 28 do not carry signaling information and should be set to 0. Time slot 1, bit 1, carriesthe m-bit (ESF) or Fs bit (SF) for optional bypass. Each bit must be present for two consecutive frames.

Figure 31. Transmit Highway - MVIP Mode

Receive Highway

In the MVIP Mode, the receive highway for each framer carries output information from the QT1F-*Plus* to the system. The highway for framer n is subdivided into two time division multiplexed buses, one for data (RDATAn), and one for signaling (RSIGLn). The two buses are synchronous with the highway clock (RCLKn), which has a clock rate of 2048 kHz. The data bus is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty-two time slots, 24 of which carry the 24 DS0 channels, as shown in the table below and in Figure 32.

RDATAn time slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1 DS0 No.	X	1	2	3	X	4	5	6	X	7	8	9	X	10	11	12	X	13	14	15	X	16	17	18	X	19	20	21	X	22	23	24

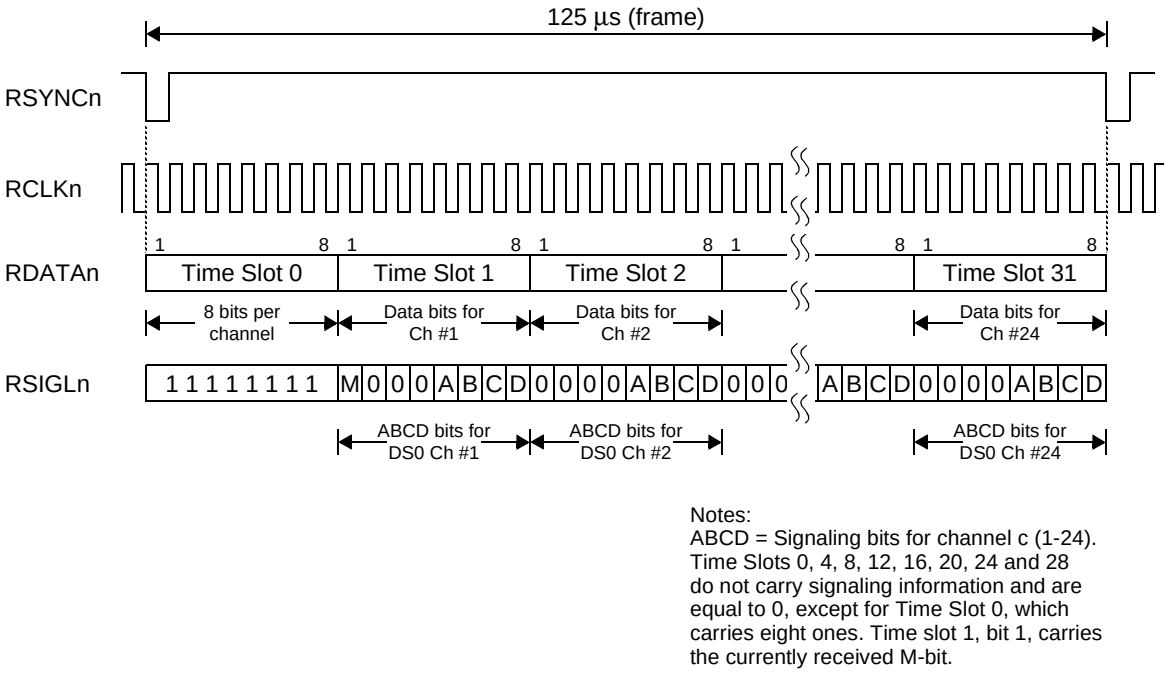
The frame start is identified by a synchronization pulse (RSYNCn), which is one (RCLKn) clock cycle wide and occurs every 125 microseconds. The position of the RSYNCn pulse is programmable by setting the values of the control bits RSD7-RSD0 in register 018H. The effect is always to restart the data and signaling highways during transmit or receive highway channel number 0. This time slot can become 9, 10, 11 or 12 bits long. Since the frame does not provide any information in Time Slot 0 there is no effect on framer performance. The synchronization pulse is aligned to bit 1 in Time Slot 0 when a value of 00H is written into this register.

The frame bits are presented on the receive signaling highway (RSIGLn) as they are received (not delayed or altered as a result of slip buffer slips). The purpose is to allow the FDL channel or frame bits to be accessed separately. The message bit (M-bit) is placed in bit 1 of Time Slot 1, representing the most recent value of the message bit (M-bit)[1]. To account for phase differences between the line and system frames, a small buffer of several bits is to be provided. Figure 32 details the placement of the frame bit in the MVIP Mode. Due to the lack of a multiframe indication in the MVIP Mode, and the difference in functionality between RSIGLn (all frame bits) and TSIGLn (Fs or m-bits repeated), a loopback of RSIGLn to TSIGLn may not pass Fs or m-bits properly.

1. Note that M-bits correspond to F_S bits in the SF mode.

The signaling bus (RSIGLn) is also divided into 256-bit frames. Each signaling frame consists of 32 time slots, of which 24 time slots carry the ABCD signaling bits associated with the 24 DS0 channels. Like the Data highway, Time Slots 0, 4, 8, 12, 16, 20, 24 and 28 do not carry signaling information and are set to zero, except for Time Slot 0, which carries eight ones. The signaling information (ABCD) is carried in the last four bits of a signaling bus time slot. The first four bits in each time slot are 0000.

The signaling bus is updated from the signaling buffer every frame. The signaling buffer is updated by the line every six frames. For 2 or 4-state signaling, the BCD or CD values are identical to the A or AB values. For these repeated values the most recent A or AB bits are presented from the signaling buffer.



Notes:
ABCD = Signaling bits for channel c (1-24).
Time Slots 0, 4, 8, 12, 16, 20, 24 and 28 do not carry signaling information and are equal to 0, except for Time Slot 0, which carries eight ones. Time slot 1, bit 1, carries the currently received M-bit.

Figure 32. Receive Highway - MVIP Mode

FRACTIONAL T1 MODE

In the Fractional T1 mode, the receive and transmit signaling (RSIGLn and TSIGLn) pins are reassigned to provide fractional T1 gapped clock signals RFT1GCn and TFT1GCn. The Fractional T1 Mode feature is only available in the Transmission Mode (i.e., when CONFIG1, pin 43, is low). The RSIGLn input lead becomes the RFT1GCn (Receive Fractional T1 Gapped Clock) output lead and the TSIGLn input lead becomes the TFT1GCn (Transmit Fractional T1 Gapped Clock) output lead.

A gapped clock for a receive fractional T1 channel is enabled by writing a 1 to the DS0 channels required in control bits RFD1 to RFD24 (registers X3AH-X3CH). The fractional T1 gapped clock will have the same phase as the RCLKn clock.

A gapped clock for a transmit fractional T1 channel is enabled by writing a 1 to the DS0 channels required in control bits TFD1 to TFD24 (registers X3DH-X3FH). The fractional T1 gapped clock will have the same phase as the TCLKn clock.

The Fractional T1 Mode is enabled when the control bit FT1M (bit 0 in register X02H) is set to a one.

PER DS0 INVERSION MODE

The same control pins and bits involved in the Fractional T1 Mode, i.e., CONFIG1 (pin 43), FT1M (bit 0 in register X02H), RFDc (c=1-24, in registers X3AH-X3CH) and TFDc (c=1-24, in registers X3DH-X3FH), combine to give the Per DS0 Inversion Mode, which operates in BOTH Transmission and MVIP Modes. With FT1M set to a zero, the bits RFDc, when set high, will invert the corresponding DS0 in RDATAn on the receive data highway, (after the Receive Slip Buffer) in either Transmission Mode or MVIP Mode, depending on the state of the CONFIG1 pin. Similarly, with the FT1M bit set to a zero, the bits TFDc, when set high, will invert the corresponding DS0 in TDATAn on the transmit data highway (before the data is clocked into the Transmit Slip Buffer), in either Transmission or MVIP Mode (depending on the state of CONFIG1).

The corresponding data streams on the Transmit/receive signaling highways are, however, NOT inverted. But, the corresponding signaling data bits (for the inverted DS0s) that are still carried in the RDATAn/TDATAn streams are inverted. Please also note that in the MVIP Mode, Time Slots 4n (n=0-7) cannot be inverted, since they are not assigned to DS0s. The actions are summarized in the following table:

FT1M Bit 0 X02H	CONFIG1 Pin 43	System Interface Mode	RSIGLn/ RFT1GCn	TSIGLn/ TFT1GCn	RFD1-RFD24	TFD1-TFD24	Mode
0	Low	1.544 Mbit/s Transmission	Signaling out	Signaling in	Invert Data on RDATAn DS0 1-24 if set to a 1.	Invert Data on TDATAn DS0 1-24 if set to a 1.	Normal
1	Low	1.544 Mbit/s Transmission	Gapped clock out	Gapped clock out	Control Rx gapped clock for DS0 1-24 if set to a 1.	Control Tx gapped clock for DS0 1-24 if set to a 1.	Fractional T1
0	High	2 Mbit/s MVIP	Signaling out	Signaling in	Invert Data on RDATAn DS0 1-24 if set to a 1.	Invert Data on TDATAn DS0 1-24 if set to a 1.	Normal
1	High	Illegal control state - do not use					

FRAMING

Frame Structure

Each of the four framers can select either the D4 SF (Superframe) or ESF (Extended Superframe) frame format for operations. The D4 SF frame format structure is shown in Figure 33. The SF format consists of 12 DS1 frames (or 2316 bits). Each DS1 frame consists of 193 bit positions. The first bit, the F bit, carries the pattern for frame alignment (Ft bits) and signaling phase alignment (Fs bits). The other 192 bits in the frame are used to carry 24 DS0 channels (eight bits per channel). Bit 2 in each DS0 channel is alternately assigned to carry a Yellow alarm indication when set to zero. The Japanese standard designates the Fs bit in frame 12 of the 12 frame superframe, which is normally is a 0, as the Yellow alarm indication. The Yellow alarm indicates that the distant end has detected a loss of signal or frame. The SF format carries either 2-state signaling or 4-state signaling by using bit 8 in the DS0 channels in frames 6 and 12 of the 12-frame superframe.

Frame #	1st Bit in frame	F-Bit		Bit Use for each time-slot			Signaling Options		
		Fs	Ft	Data	YA	Signaling	None	2-state	4-state
1	0	-	1	Bits 1-8	Bit 2	None	-	-	-
2	193	0	-	Bits 1-8	Bit 2	None	-	-	-
3	386	-	0	Bits 1-8	Bit 2	None	-	-	-
4	579	0	-	Bits 1-8	Bit 2	None	-	-	-
5	772	-	1	Bits 1-8	Bit 2	None	-	-	-
6	965	1	-	Bits 1-7	Bit 2	Bit 8	-	A	A
7	1158	-	0	Bits 1-8	Bit 2	None	-	-	-
8	1351	1	-	Bits 1-8	Bit 2	None	-	-	-
9	1544	-	1	Bits 1-8	Bit 2	None	-	-	-
10	1737	1	-	Bits 1-8	Bit 2	None	-	-	-
11	1930	-	0	Bits 1-8	Bit 2	None	-	-	-
12	2123	0 or YA	-	Bits 1-7	Bit 2	Bit 8	-	A	B

Figure 33. D4 SF Framing Structure

The ESF frame format structure consists of 24 DS1 frames, as shown in Figure 34. Each DS1 frame consists of 193 bit positions. The first bit, the F bit, carries the pattern for frame alignment (FPS bits), a 4 kbit/s HDLC link (D bits), and a CRC-6. The CRC-6 is used for performance monitoring purposes. The other 192 bits in the frame are used to carry 24 DS0 channels (eight bits per channel). The Yellow alarm is indicated by setting the HDLC link bits to a sequence of 8 ones followed by 8 zeros. The Yellow alarm indicates that the distant end has detected a loss of signal or frame. The ESF format carries either 2, 4 or 16-state signaling by using bit 8 in the DS0 channels in frame 6, 12, 18 and 24.

Frame #	1st Bit in frame	F-Bit			Bit Use for each time-slot		Robbed bit Signaling Options			
		FPS	DI	CRC	Data	Signaling	None	2-state	4-state	16-state
1	0	-	D	-	Bits 1-8	None	-	-	-	-
2	193	-		1	Bits 1-8	None	-	-	-	-
3	386	-	D	-	Bits 1-8	None	-	-	-	-
4	579	0		-	Bits 1-8	None	-	-	-	-
5	772	-	D	-	Bits 1-8	None	-	-	-	-
6	965	-		2	Bits 1-7	Bit 8	-	A	A	A
7	1158	-	D	-	Bits 1-8	None	-	-	-	-
8	1351	0		-	Bits 1-8	None	-	-	-	-
9	1544	-	D	-	Bits 1-8	None	-	-	-	-
10	1737	-		3	Bits 1-8	None	-	-	-	-
11	1930	-	D	-	Bits 1-8	None	-	-	-	-
12	2123	1		-	Bits 1-7	Bit 8	-	A	B	B
13	2316	-	D	-	Bits 1-8	None	-	-	-	-
14	2509	-		4	Bits 1-8	None	-	-	-	-
15	2702	-	D	-	Bits 1-8	None	-	-	-	-
16	2895	0		-	Bits 1-8	None	-	-	-	-
17	3088	-	D	-	Bits 1-8	None	-	-	-	-
18	3281	-		5	Bits 1-7	Bit 8	-	A	A	C
19	3474	-	D	-	Bits 1-8	None	-	-	-	-
20	3667	1		-	Bits 1-8	None	-	-	-	-
21	3860	-	D	-	Bits 1-8	None	-	-	-	-
22	4053	-		6	Bits 1-8	None	-	-	-	-
23	4246	-	D	-	Bits 1-8	None	-	-	-	-
24	4439	1		-	Bits 1-7	Bit 8	-	A	B	D

Figure 34. ESF Framing Structure

Frame Alignment

The selection of the bits for frame alignment is determined by the value written to control bits SYC1 and SYC0 (bits 4 and 3 in register X04H). The following table lists the options for selecting the F-bits that are used for frame alignment.

SYC1 X04H:4	SYC0 X04H:3	D4 SF	ESF
0	0	Not Used	Not Used
0	1	Fs Bits	FPS Bits
1	0	Ft Bits	Not Used
1	1	Fs and Ft Bits	FPS Bits and a valid CRC-6

Out Of Frame Alignment

An Out Of Frame (OOF) alarm is declared when a specified number of errored bits is detected in a specified number of consecutive framing bits. The framing bits that are used for alignment are determined by the value written to control bits SYC1 and SYC0. The out of frame alignment is programmable using control bits OOF1 and OOF0 (bits 7 and 6 in register 04H). The following table lists the options for declaring an Out Of Frame (OOF) alarm.

OOF1 X04H:7	OOF0 X04H:6	Out Of Frame Criteria
0	0	2 out of 4 framing bits in error
0	1	2 out of 5 framing bits in error
1	0	2 out of 6 framing bits in error
1	1	2 out of 4 framing bits in error

The QT1F-*Plus* device supports offline framing. It continues to send data to the terminal side output while the framer is in the process of determining whether it has lost frame synchronization. If the framer goes back to in-frame, and the framing bit positions are not changed, the framer will continue passing the individual DS0's through without affecting the data path.

In the unlikely event that the framing bit position has been changed, the DS0 data path will be affected and a CFA alarm will be declared via registers X10H and X11H.

Framing Pattern Mimic During PRBS Payloads

When PRBS patterns are carried in the DS1 payload, the pattern may simulate (mimic) the framing pattern to some extent, with the risk of causing false frame synchronization. In the case of using ESF with CRC6, any mimic captured by the framer synchronizer will be rejected due to the mismatch of the CRC6 calculation. Therefore, any mimic will not affect framing with the ESF format signal. When D4SF signal format is selected and a correct input signal framing format is applied, a mimic in the payload will not last longer than the framing pattern itself. Therefore, the correct framing position should be detected. However, when the incoming signal does not comply with the D4SF framing format, the receive framer might capture the mimic. Because the mimic will eventually run into mismatches, the framer will go Out of Frame again. In an experiment, sending an ESF signal to a QT1F-*Plus* programmed for D4SF with QRSS in the payload caused from 4 to 6 OOF events per second.

Transmit Framer

Each of the four transmit framers performs the following functions, unless the framer is configured for the transparent (unframed) mode of operation when the Transparent Mode only is selected.

When the SF format is selected:

- Generate the framing (terminal - Ft bits and signaling - Fs bits) pattern
- Set the Yellow alarm into bit 2 in all 24 DS0 channels or leave the bits for normal data
- Insert the 24 DS0 channels into the transmitted frame
- Insert the signaling states into bit 8 in all DS0 channels in frames 6 and 12 or leave the bits as is for clear channel operation

When the ESF format is selected:

- Generate the framing bit (FPS bits) pattern
- Insert the 4 kbit/s HDLC link bits (D bits) into the F-bits
- Insert the calculated CRC-6 value from the previous 24-frame superframe
- Insert the 24 DS0 channels into the transmitted frame
- Insert the signaling states into bit 8 in all DS0 channels in frames 6, 12, 18 and 24 or leave the bits as is for clear channel operation
- Calculate CRC-6 for next superframe insertion

Please note that when a framer is configured for the transparent mode of operation, all the channels in the frame are transmitted from the data bus transparently through the QT1F-*Plus*, bypassing the slip buffers.

The SF format is selected by writing control bits FMD1 (bit 2) and FMD0 (bit 1) in register X04H to 01. The ESF format is selected by writing control bits FMD1 (bit 2) and FMD0 (bit 1) in register X04H to 11. The selection is common to both the transmit and receive sides of a framer channel.

The Yellow alarm forces bit 2 to zero in all of the DS0 channels for the SF format (in place of data which can be either zero or one), while a repeating sequence of eight ones followed by eight zeros in the HDLC link is used in the ESF format. The microprocessor can write the state of the Yellow alarm indication. When the microprocessor writes a 1 to control bit YEL (bit 2) in register X07H, the Yellow alarm indication is transmitted for either the SF or ESF format. In addition, when control bit ENYEL (bit 4) in register 00H is written with a 1, the Yellow alarm indication from the signaling highway in the Transmission Mode only will result in a Yellow alarm indication being transmitted.

The transmitted path for the data link bits (D-bits) in the ESF format can be assigned from the signaling highway, HDLC link controller, or an internally generated 16-bit coded message. When control bit BFDL (bit 1) in register X01H is a 1, the bits are sent via the signaling highway. When control bit BFDL is 0, the bits are sent via the HDLC link controller. The selection of the D-bits from either signaling highway or the HDLC link controller can be overwritten by the Yellow alarm indication generation or when the 16-bit coded message is enabled.

The 16-bit coded message is generated for the ESF format only when control bit EBT (bit 0) in register X08H is written with a 1. The 16-bit message consists of eight ones followed by a 0, a six-bit code, and another 0 (11111111 0XXXXXX0). The six-bit code word is written to control bits TBCD5-TBCD0 in register X0BH.

Each framer has the capability of generating framing pattern errors, and also CRC-6 errors in the ESF format. When control bit FRME (bit 3) in register X07H is written with a 1, the framer will generate and transmit one bad framing bit. The bit that is detected in error depends on the framing pattern selected in the receiver. When control bit CRC (bit 4) in register X07H is written with a 1, the CRC bits are transmitted inverted for one superframe.

Each framer is capable of sending SF loop-up and loop-down codes per ANSI T1.403-1998. The specific loop-up code is provided by setting control bits LU6- LU0 (bits 6 - 0) in register 014H to the desired code and bits ULEN1 and ULEN0 (bits 4 and 3) in register 016H to the desired length. Setting control bit TXUP (bit 5) in register X05H will cause the loop-up code to be sent on the line continuously in place of normal data and framing. The specific loop-down code is provided by setting control bits LD6- LD0 (bits 6 - 0) in register 015H to the desired code and bits DLEN1 and DLEN0 (bits1 and 0) in register 016H to the desired length. Setting control bit TXDN (bit 4) in register X05H will cause the loop-down code to be sent on the line continuously in place of normal data and framing.

Channels 1-24

Channels 1-24 are inserted into the transmitted frame from the slip buffer when it is enabled, or directly from the data highway when it is bypassed (Transmission Mode only). The slip buffer locations are registers X90H - XA7H (frame 1) and XA8H - XBFH (frame 2). An individual time slot in the buffer can be frozen by writing a 0 to one or more control bits TDE1-TDE24 in registers XE4H - XE6H. This permits the microprocessor to write idle or service codes for one or more DS0s.

Fast Sync Mode

The QT1F-*Plus* provides a fast sync mode which may be used for testing purposes. The fast sync mode for the receiver side is selected when control bit RXFS (bit 1) in register X06H is written with a 1 in the NRZ mode. A pulse that is one clock cycle wide in bit position 192 of the last frame forces the framer into synchronization. It can occur repetitively at 3 ms intervals for the ESF format or at 1.5 ms intervals for the SF format, or it can be pulsed once provided the received framing sequence is valid afterwards.

The fast sync mode for the transmitter side is selected when control bit TXFS (bit 0) in register X06H is written with a 1 in the NRZ mode. The TFSn output in this mode is a one clock cycle wide pulse in bit position 192 of the last frame in the multiframe that occurs every 3 ms for the ESF format or every 1.5 ms for the SF format. This allows an external device to be synchronized to the QT1F-*Plus* framer.

Slip Buffers

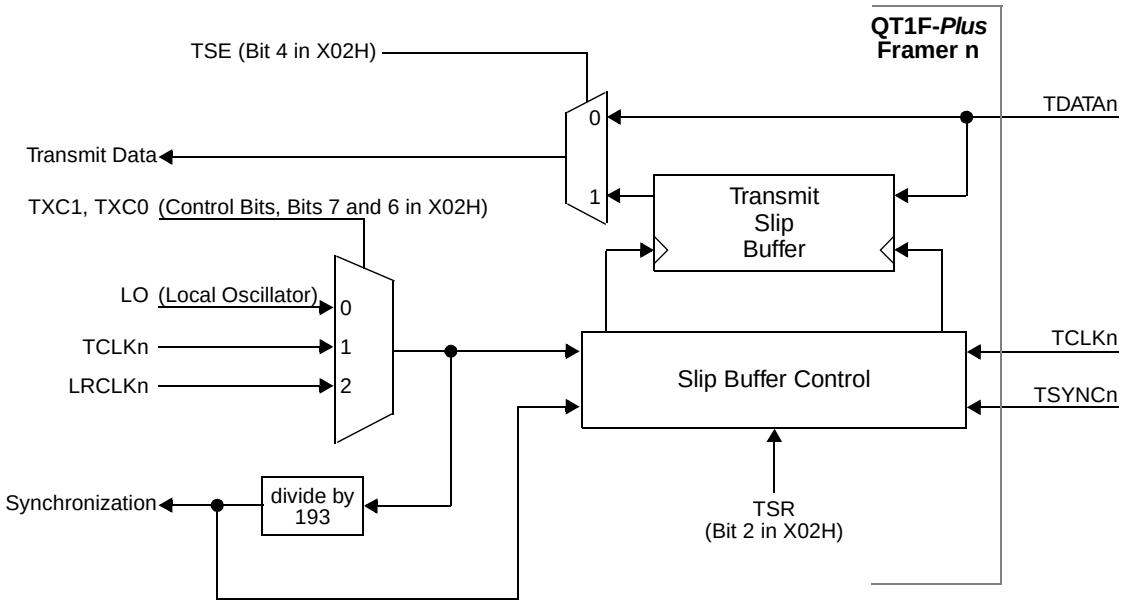
Each framer contains a two-frame slip buffer in both the transmit and receive data directions. Either of the slip buffers can be bypassed, if required, in the Transmission Mode only. The slip buffers must be enabled in the MVIP Mode. Only the transmit and receive data time slots (DS0 Channels 1-24) are passed through the slip buffers. The signaling states and framing bits are buffered in a separate memory location and are not subjected to slips. Each buffer is organized as a circular queue two frames in length. At this point, if data is arriving faster than it is being removed, the buffer will begin to fill. Before the buffer becomes totally full, a controlled slip will occur and one frame of data will discarded. This is accomplished by moving the write pointer back one frame and overwriting the previous frame that was written. If, after recentering, the data is being removed faster than it is arriving, the buffer will begin to empty. Before the buffer becomes completely empty, a controlled slip occurs in the opposite direction, and a frame of data is added to the buffer. This is accomplished by moving the read pointer back one frame and repeating the last frame sent. Each buffer may be manually recentered by setting the TSR or RSR control bits (bit 2 and 1) in the Framer Clock Control register X02H.

The transmit slip buffer is used to absorb low speed jitter in the transmit direction. The transmit slip buffer is enabled by writing a 1 to control bit TSE (bit 4) in the Framer Clock Control register X02H. When enabled, time slots are written into the transmit slip buffer by the system clock (TCLKn), and read out by the recovered receive clock (LRCLKn), the system clock (TCLKn), or the local oscillator (LO). Control bits TXC1 and TXC0 (bits 7 and 6) in register X02H select the clock source. The time slots (t = 1-24) from the transmit data bus are written into the slip buffer when their respective enable bits (TDEt) in registers XE4H, XE5H and XE6H are written with a 1.

If a phase shift between the two clocks is detected, a deletion or repetition of one frame of data (24 DS0s) occurs by the buffer reaching an almost full or almost empty threshold. A transmit slip error is indicated by status bit TXSLIP (bit 1) in register X10H, with a latched event LTXSLIP (bit 1) indicated in register X11H. The transmit slip buffer status is indicated by reading status bits TXS1 and TXS0 (bits 7 and 6) in register X14H which indicate if a slip has occurred and if it is a repetition or deletion.

Please note that the slip buffer alarms remain active when the slip buffer is disabled.

The individual DS0 channels in both frames can be accessed by the microprocessor, as well as written by the microprocessor in place of data. When a DS0 channel enable control bit in register location XE4-XE6H is written with a 0, the content of the two-frame slip buffer location is frozen. The microprocessor can write an idle or service code to be transmitted to the line. The transmit slip buffer data locations are X90H (Channel 1) to XA7H (Channel 24) for frame 1, and XA8H (Channel 1) to XBFH (Channel 24) for frame 2. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written with the service or idle code. A simplified schematic of the transmit slip buffer is shown in Figure 35.



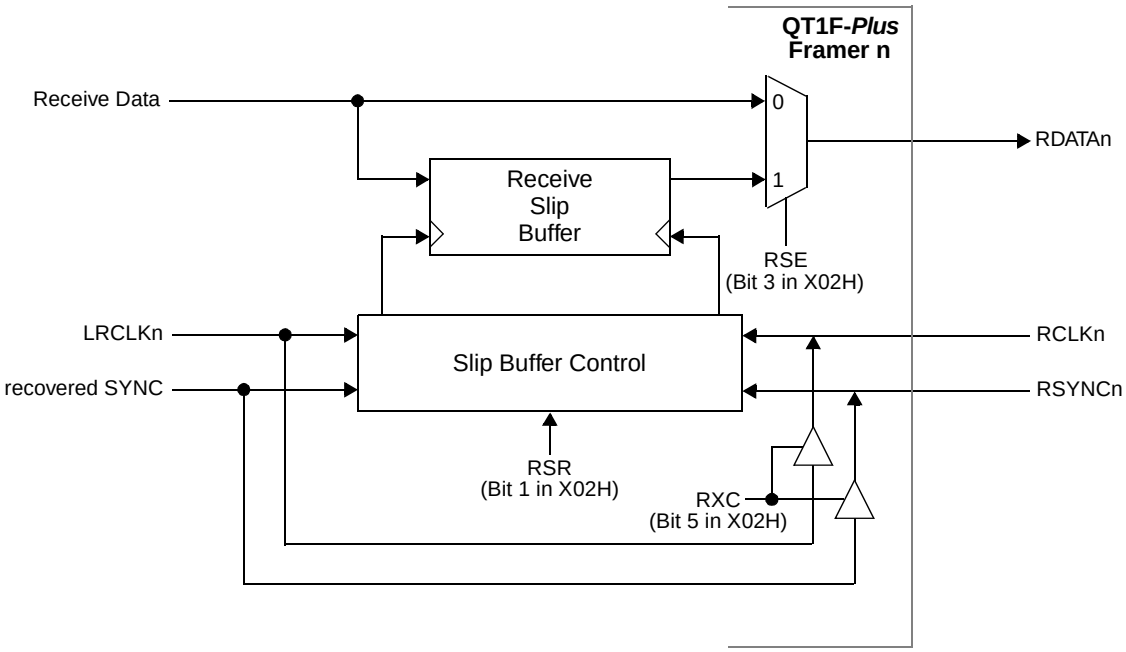
Note: n is the framer number (1, 2, 3, 4)

Figure 35. Transmit Slip Buffer

The receive slip buffer is used when the receive clock (RCLKn) is provided from an external source. The receive slip buffer controls the time slot access and retiming, providing a two-frame buffer that is optionally bypassable in the Transmission Mode only. The slip buffer must be enabled in MVIP Mode. Time slots from the line interface are written into the slip buffer by the recovered receive clock (LRCLKn), and read out by the system clock (RCLKn). If a phase shift between the two clocks is detected, a deletion or repetition of one frame of data (24 DS0s) occurs by the buffer reaching an almost full or almost empty threshold. The time slots from the receive line signal are written into the slip buffer when their respective enable bits (RDEn) in registers XE0H, XE1H and XE2H are written with a 1.

Individual DS0 channels can be accessed by the microprocessor, and they can be written by the microprocessor in place of data. When a DS0 enable control bit in register location XE0-XE2H is written with a 0, the content of the two-frame slip buffer location is frozen. The microprocessor can write an idle or service code in the location that will be transmitted to the receive data highway. The receive slip buffer data locations are X40H (Channel 1) to X57H (Channel 24) for frame 1, and X58H (Channel 1) to X6FH (Channel 24) for frame 2. Please note that both buffer locations (i.e., frame 1 and frame 2) must be written with the service or idle code. A simplified schematic of the receive slip buffer is shown in Figure 36.

A receive slip error is indicated by status bit RXSLIP (bit 0) in register X10H, with a latched event LRXSLIP (bit 0) indicated in register X11H. The receive slip buffer status is indicated by reading status bits RXS1 and RXS0 (bits 5 and 4) in register X14H which indicate if a slip has occurred and if it is a repetition or deletion.



Note: n is the framer number (1, 2, 3, 4)

Figure 36. Receive Slip Buffer

DELAY

Delay through the QT1F-*Plus* is a function mainly of the slip buffers, though other factors also influence the amount of delay. The table below gives the typical delay for different elements of the framer from line to system and from system to line. All numbers are in bit times for a clock rate of 1544 kHz. To estimate the total delay through a framer, add the system interface delay to the slip buffer delay (choose enabled or disabled value) and the codec delay (choose NRZ, AMI or B8ZS value), and then multiply by 648 ns.

Direction of Signal Flow	System Interface	Slip Buffer		Codec (select one)		
		Disabled	Enabled	NRZ	AMI	B8ZS
RPOSn/ RLDATn to RDATn	1	4	8 to 378 (Note 1)	1	1	8
TDATn to TPOSn/ TLDATn	1	4	8 to 378 (Note 2)	1	1	8

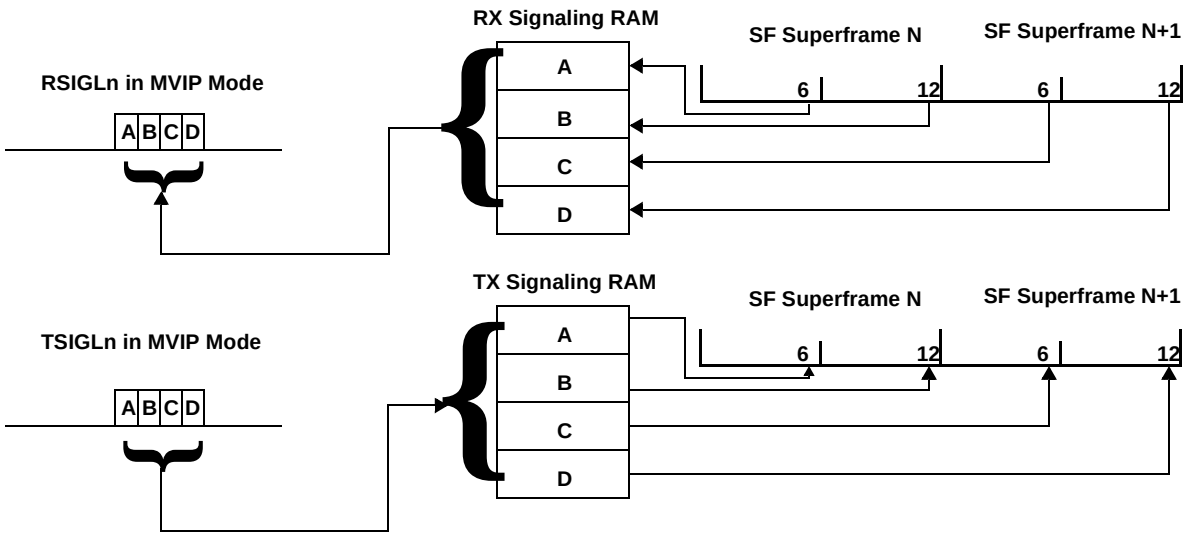
Note 1: When the framer is reset, the nominal delay is 96 bits through the slip buffer. Recenter (control bit RSR toggled) will cause a slip if the delay exceeds 289 bits to minimize the delay.

Note 2: When the framer is reset, the nominal delay is 96 bits through the slip buffer. Recenter (control bit TSR toggled) will cause a slip if the delay exceeds 289 bits to minimize the delay.

SIGNALING

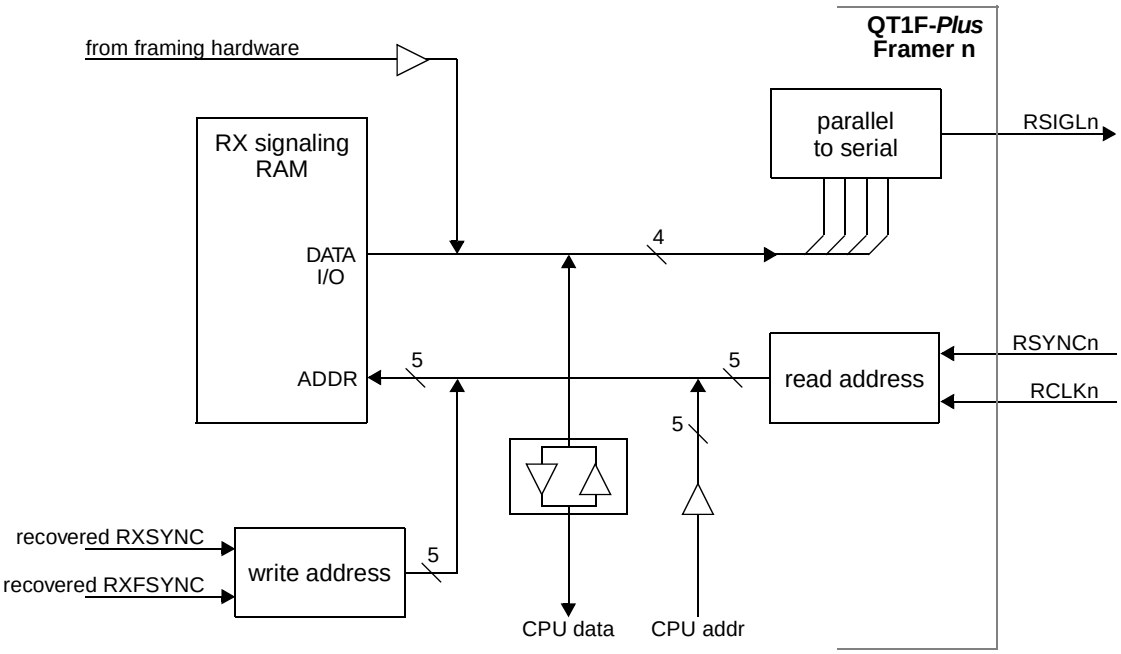
The signaling states are carried in bit 8 in the DS0 channels in frames 6 and 12 for the SF format and frames 6, 12, 18 and 24 for the ESF format. Control bits TYP1 (bit 7) and TYP0 (bit 6) in register 03H select the signaling format to be carried. Clear channel capability is also selectable by written these control bits with a 00.

The SF format carries 2-state, 4-state or 9-state signaling. 2-state signaling (A bits) is carried in frames 6 and 12. For 4-state and 9-state signaling, the A bit states are carried in frame 6, and the B bit states are carried in frame 12. The ESF format carries 2-state, 4-state or 16-state signaling. 2-state signaling (A bits) is carried in frames 6, 12, 16 and 24. For 4-state signaling, the A bit states are carried in frames 6 and 18, and the B states are carried in frames 12 and 24. For 16-state signaling (only for the ESF format), the A state is carried in frame 6, the B state in frame 12, the C state in frame 18, and the D state in frame 24. In the TXC-03103C, the transmit and receive signaling buffers can be used the same way for both AB signaling in SF and ABCD signaling in ESF modes, provided the framing mode is set to SF, and the signaling type is set to 16-state, under which condition all the ABCD sections of the 96-bit buffer are used to read out and write in signaling bits even for the SF framing mode, unlike the TXC-03103 device. In effect, the AB signaling bits from the 6th and 12th frame of the "m"th 12-frame SF are stored in the A,B sections of the buffer, while the AB signaling bits from the 6th and 12th frames of the "m+1"th 12-frame SF are stored in the C,D sections of the buffer. This allows monitoring and inserting of the A/B bits for toggle during every SF in the 9-state signaling scheme, as per the requirements of ANSI T1.403. **If the SF format 9-state signaling scheme is used, the control bits FMD1 and FMD0 (bits 2 and 1 in register X04H) will have to be set to 01, and the TYP1 and TYP0 bits (bits 7 and 6 in register X03H) will have to be set to 11.** The following diagram illustrates this



Signaling Buffers

The transmit and receive signaling buffers that are used to interface the QT1F-*Plus* to the system are 96 bits in length. In the receive direction, the signaling bits are extracted from the data stream and placed in the receive signaling buffer after the framing sequence is detected in the receive framer block. A simplified schematic of the receive signaling buffer is shown in Figure 37. In the Transmission Mode, four signaling bits are sent each frame, and all signaling states are sent over the 24 frames. Receive signaling bits are clocked out by the system clock (RCLKn), which is sourced by either the system or the QT1F-*Plus*. The signaling bits on RSIGLn are sent such that they will meet the system requirements for formatting a Virtual Tributary (VT) in a SONET format in the next multiframe. These bits can be extracted using the receive sync signal RSYNCn. In the MVIP Mode, all the signaling bits are sent for every DS0 channel every frame (125 microseconds) from the receive signaling buffer by using the system clock (RCLKn) and sync pulse (RSYNCn).



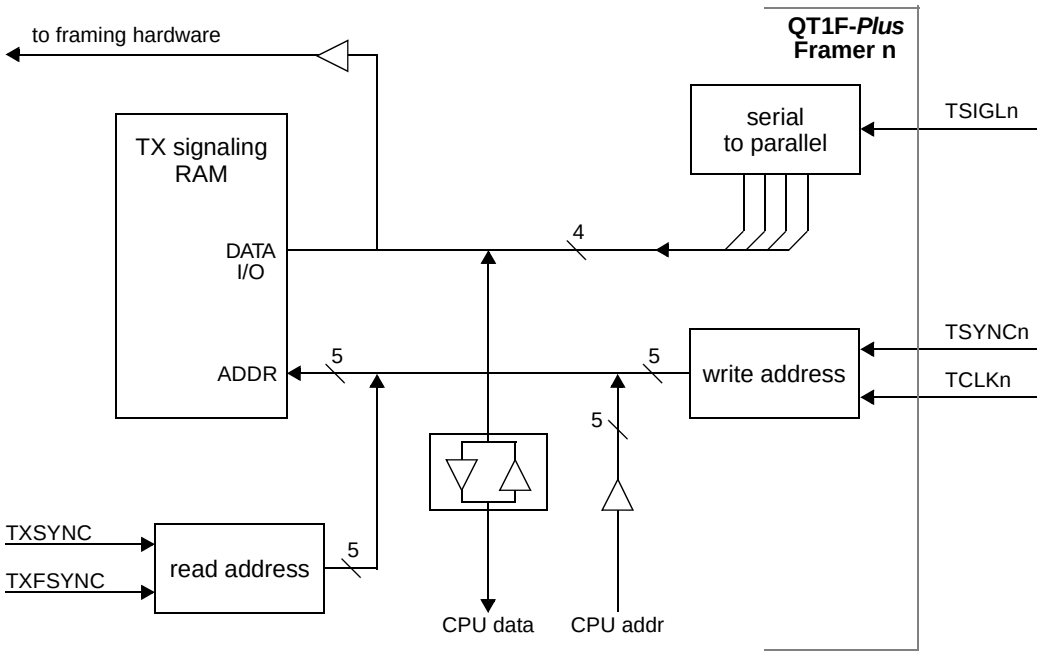
Note: n is the framer number (1, 2, 3, 4)

Figure 37. Receive Signaling Buffer

The received signaling bits are stored sequentially in the receive signaling buffer in the order they are received. The signaling bits in the receive signaling buffer (register locations X80H, X81H, X82H, X84H, X85H, X86H, X88H, X89H, X8AH, X8CH, X8DH and X8EH) may be read at any time by the microprocessor in order to monitor the signaling states, or written to modify the outgoing values. Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronized to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the corresponding (receive and transmit) signaling enable bits (SE1-SE24 bits) in register locations XE8H (channels 1 - 8), XE9H (channels 9 - 16), and XEAH (channels 17 - 24) are written with a 1, the signaling bits are sent on the signaling highway (and data highway). For example, a 1 written to control bit SE1 enables the signaling bits for DS0 channel 1 to be written into the signaling buffer. When a 0 is written into control bit SE1, the signaling buffer for channel 1 signaling is set to 0. The ABCD=0 states will be sent on the signaling highway until the SE1 bit is written with a 1. Please note that the action of the Receive Signaling Freeze control bit, RXF, that acts on all 24 DS0s (bit 5 in register X03H) is different. When RXF is set to 1, it freezes the Receive Signaling buffer, and the contents cannot be changed from the Receive line (but the microprocessor can write a new signaling value to the buffer) and the receive signaling highway gets the frozen signaling states in the buffer. When RXF is set to 0, the signaling highway updates with the values from the Receive line

The signaling bits in the receive direction are automatically frozen in their present states when loss of signal or loss of synchronization occurs. A signaling freeze may also be initiated manually by writing a 1 to control bit RXF (bit 5) in register X03H. A receive signaling freeze indication is given by status bit RXSF (bit 7) in register X15H.

A simplified schematic of the transmit signaling buffer is shown in Figure 38. Transmit signaling bits on the signaling pin TSIGLn are clocked into the transmit signaling buffer using the transmit system clock TCLKn and sync pulse TSYNCn. In the Transmission Mode, four signaling bits are provided each frame. In the MVIP Mode, all signaling bits are written to the TX signaling RAM for every channel every other frame (250 microseconds). However, signaling from the signaling highway must be provided every frame.



Note: n is the framer number (1, 2, 3, 4)

Figure 38. Transmit Signaling Buffer

The transmit signaling bits from the signaling highway are stored sequentially in the transmit signaling buffer in the order they are received. The signaling bits in the transmit signaling buffer (register locations XD0H, XD1H, XD2H, XD4H, XD5H, XD6H, XD8H, XD9H, XDAH, XDCH, XDDH and XDEH) may be read at any time by the microprocessor in order to monitor the signaling states, or written to modify the outgoing values. Since the buffer is accessed by multiple asynchronous processes, the read and write cycles for the signaling buffer are synchronized to the internal clocks. Simultaneous accesses are serviced sequentially. The priority of service depends on the amount of latency acceptable between when the request was received and when the data is required to be available. When the corresponding signaling enable bits (SE1-SE24 bits) in register locations XE8H (channels 1 - 8), XE9H (channels 9 - 16), and XEAH (channels 17 - 24) are written with a 1, the signaling bits are written into the transmit data stream in the corresponding robbed bit positions. For example, a 1 written to control bit SE1 enables the corresponding ABCD signaling bits from the transmit signaling buffer for channel 1 to be written into the LSB of DS0 1 in frame numbers 6, 12, 18 and 24. When a 0 is written into control bit SE1, the signaling buffer for channel 1 signaling is prevented from writing to the line, although the buffer updates from the transmit signaling highway. The action of the Transmit Signaling Freeze control bit, TXF (bit 4 in register X03H), that operates on all 24 DS0s, is different. When TXF=1, the transmit signal buffer becomes frozen to its current states, and continuously updates the line with the frozen signaling states. The frozen signaling states can be changed by the microprocessor, but they cannot be updated from the transmit signaling highway. When TXF=0, only then can the transmit signal buffer update from the highway.

A transmit signaling freeze indication occurs when control bit TXF (bit 4) in register X03H is written with a 1 (manual freeze), or when AIS is detected on the signaling highway (Transmission Mode only). A transmit signaling freeze indication is given by status bit TXSF (bit 6) in register X15H.

CLOCKING AND SYNCHRONIZATION

The clocking and synchronization portion of the QT1F-*Plus* includes the receive clock configuration, transmit clock synchronization, and the slip buffers for each of the framers. The following table provides a summary of the RCLKn clock operation in the receive direction.

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge Out	Comments
Transmission	1.544 MHz	Pos.	Neg.	Clock and sync pulse may be outputs* in which RCLKn clock is derived from the recovered received clock (LRCLKn).
MVIP	2.048 MHz	Pos.	Pos.	System clock and sync pulse must be inputs.

* Note: Control bit RXC (bit 5) in the Framer Clock Control Register X02H configures RCLKn as an input or output for each of the framers. In the MVIP Mode, the system clock must be an input.

In the transmit direction, the system clock TCLKn and sync pulse TSYNCn are always inputs to the QT1F-*Plus*. The transmit data TDATAn is clocked out of the slip buffer by either the transmit system clock (TCLKn), the local oscillator input (LO), or the recovered receive clock (LRCLKn). The clock selection for each framer is controlled by TXC1 (bit 7), and TXC0 (bit 6) in Framer Clock Control Register X02H. The local oscillator input (LO) has a nominal frequency of 1.544 MHz and should be accurate to $\pm$32 ppm. LO is the source for the RCLKn output when RXC = 1 and LOS is detected.

The following table provides a summary of the TCLKn clock operation in the transmit direction.

Interface Mode	Clock Rate	Sync Edge In	Data/Sig Edge In	Comments
Transmission	1.544 MHz	Pos.	Pos.	
MVIP	2.048 MHz	Pos.	Neg.	

Clock Reference

For system applications that require the recovered receive clock, the QT1F-*Plus* can provide two reference clocks derived from any of the four clock inputs (LRCLKn), when enabled. The recovered receive clock input LRCLKn that is used to derive the reference clock CLKREF1 (pin 46) is determined by the value written to control bits CR1S1 and CR1S0 (bits 1 and 0) in the Clock Reference Selection Register (019H). The recovered receive clock that is used to derive the reference clock CLKREF2 (pin 2) is determined by the value written to control bits CR2S1 and CR2S0 (bits 7 and 6) in the Clock Reference Selection Register (019H). The following table lists the various conditions for enabling/disabling the clock reference signal on the CLKREF1 pin. The ENREF1 and 1544KHZ control bits are located at bits 3 and 4 in the Clock Reference Selection Register (019H). The LIE control bit (bit 1) is located in the Frame Configuration Register (X00H). The LOS alarm status bit (bit 7) is located in the DS1 Status Register (X10H).

ENREF1 (Control)	LOS(n) (Alarm)	LIE(n) (Control)	1544KHZ (Control)	Action
0	X	X	X	CLKREF1 pin tristated.
1	0	0	0	8 kHz Reference provided on CLKREF1. The 8 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	0	0	1	1544 kHz Reference provided on CLKREF1. The 1544 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	1	X	X	CLKREF1 pin is forced low.
1	X	1	X	CLKREF1 pin is forced low when LINTn is in the active true state.

X can be either state.

The following table lists the various conditions for enabling/disabling the clock reference signal on the CLKREF2 pin. The ENREF2 and 1544KHZ control bits are located at bits 5 and 4 in the Clock Reference Selection Register (019H). The LIE control bit (bit 1) is located in the Frame Configuration Register (X00H). The LOS alarm status bit (bit 7) is located in the DS1 Status Register (X10H).

ENREF2 (Control)	LOS(n) (Alarm)	LIE(n) (Control)	1544KHZ (Control)	Action
0	X	X	X	CLKREF2 pin tristated.
1	0	0	0	8 kHz Reference provided on CLKREF2. The 8 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	0	0	1	1544 kHz Reference provided on CLKREF2. The 1544 kHz signal is derived from the recovered clock that is selected (LRCLKn).
1	1	X	X	CLKREF2 pin is forced low.
1	X	1	X	CLKREF2 pin is forced low when LINTn is in the active true state

X can be either state.

AIS DETECTION AND GENERATION

A line AIS is detected when the received line signal has 99.9% or more ones present in a period of 48 ms. Recovery occurs when fewer than 99.9% of ones occur in a 48 ms period. The status of line AIS is given by the AIS status bit (bit 0) in register X1BH.

AIS-CI Detector

To meet the latest ANSI T1.403 CORE requirements, the TXC-03103C detects the AIS-CI signature when AIS is present. The AIS-CI signature is a pattern whose length is 6176 bits, with all bits being logical ones except bit number 0, bit number 3088, bit number 3474 and bit number 5760, which are logical zeros. It may also be viewed as a pattern which recurs at 386-bit intervals that is 1111 1111 0011 1110 (from left to right) that is logically AND-gated with an all ones pattern. The actual AIS-CI code is a1.260 second period in which the AIS-CI signature is present for 150 milliseconds and a regular AIS is present for 1.110 seconds. Detection of the AIS-CI signature pattern twice in a row is sufficient to declare AIS-CI. A single bit error in the pattern, once the pattern is detected, is ignored. The output of the AIS-CI signature detector is logically AND-gated with the output of the AIS detector. This combined signal is logically OR-gated with the change of frame alignment alarm, CFA, register (bit 3 in register X110H). Mask MCFA, latched value LCFA, performance value PCFA and fault value FCFA are all bit 3 of registers X09H, X11H, X12H and X13H, respectively. These bits are shared with the AIS-CI signature function. Global mask and global events for CFA also apply to AIS-CI. Bit 3 of register 00AH (Global Status Indication Register) is a 1 when any of the four framer channels has detected a change in frame alignment or the AIS-CI signature. When bit 3 in register 00BH is set to a 1, a change in the frame alignment or AIS-CI indication in any framer channel (LCFA/LAISCI, registers X11H), is masked from providing an interrupt indication.

The QT1F-*Plus* also provides control bits and enable bits for alarms to generate AIS for the receive highway. When control bit SVTAIS (bit 6) in register X07H is written with 1, the AIS, OOF and LOS alarms, if enabled by their respective ENAIS (bit 2), ENOOF (bit 1), and ENLOS (bit 0) control bits in the Signaling and Time Slot Control register X03H, cause the generation of AIS according to the following table. The table reflects the AIS actions taken on Out Of Frame (OOF) alarm when enabled by ENOOF and SVTAIS. Control bits ENAIS for AIS and ENLOS for loss of signal function in the same manner. Please note that the microprocessor can force AIS to be generated for the receive data highway independent of the three control bits by writing a 1 to control bit SYSALL1 (bit 5) in register X07H.

Transmission Mode

ENOOF	SVTAIS	Action
0	0	Normal operation. No AIS generated on signaling or data highway.
0	1	Normal operation. No AIS generated on signaling or data highway.
1	0	AIS generated only on signaling highway when OOF alarm is detected. A-bits on the signaling highway are equal to 1.
1	1	AIS generated on signaling and data highways when OOF alarm is detected. A-bits on the signaling highway are equal to 1.

MVIP Mode

ENOOF	SVTAIS	Action
0	0	Normal operation. No AIS generated on data highway.
0	1	Normal operation. No AIS generated on data highway.
1	0	Normal operation. No AIS generated on data highway when OOF alarm is detected.
1	1	AIS generated on data highway when OOF alarm is detected.

In the transmit direction, from the transmit highway to the line, line AIS can be generated. When the microprocessor writes a 1 to control bit AISE (bit 1) in register X07H, the all ones AIS pattern is transmitted in all bits of the frame continuously until the control bit is written with a 0. When the microprocessor writes a 1 to control bit ENSAIS (bit 2) in register X00H, in the Transmission Mode only, the all ones AIS pattern is transmitted in all bits of the frame when the A-bits in the signaling highway are detected as ones. In addition, a status bit VTAIS (bit 3) in register X14H indicates when the A-bits are set to 1 in the Transmission Mode.

ANSI RAI - CI DETECTOR

In accordance with ANSI T1.403 CORE requirements, RAI-CI for the ESF format is transmitted using the FDL, by sequentially interleaving 0.99 s of the unscheduled message 1111 1111 0000 0000 (left to right; which represents RAI in the FDL), with 90 ms of the message 1111 1111 0111 1100 (left to right). RAI-CI for the SF format is detected if all 24 time slots consist of the pattern 1000 1011 (left to right). For SF format, if RAI/Yellow alarm is detected (bit 2 of all DS0s = 0, control bits FMD1 and FMD0 in register X04H = 01), SF RAI-CI (X0XXXXXX per DS0 for all 24 DS0s) may be detected by reading the Receive Slip Buffer contents (RDS0(1)-RDS0(24) for frames 1 and 2, at register locations X40H-X6FH).

HDLC CHANNEL

A HDLC message frame is composed of four parts: an opening flag, the message (which consists of multiple bytes), a two-byte CRC-16 frame check sequence, and a closing flag, as shown in Figure 39 below.

Bit	8	7	6	5	4	3	2	1
Opening Flag	0	1	1	1	1	1	1	0
Message	Address and Control Information							
CRC-16								
Closing Flag	0	1	1	1	1	1	1	0

Figure 39. HDLC Format

The opening and closing flags are represented by a single, unique 8-bit character defined as 01111110, which contains six contiguous ones. To avoid the occurrence of a false flag within the data stream, a zero is inserted (stuffed) after each string of five contiguous ones in the message or CRC-16. Reception of more than six contiguous ones is interpreted as a frame abort sequence. When an abort sequence is received, the remainder of the current frame is ignored and the received portion is discarded as an invalid frame. A two-byte CRC-16 frame check sequence is computed across the contents of the message (after the opening flag), and appended to the end of the message. The time between consecutive frames is filled with one or more flags. When two or more flags occur in sequence, they may share the boundary zero between them (011111101111110).

A 16-byte FIFO is provided in each direction for each framer, which permits short messages to be transmitted and received without having the microprocessor service the FIFOs. For long messages, interrupts and status information are provided to facilitate FIFO servicing by the microprocessor. For both short and long messages, the HDLC link controller performs the following functions:

- Zero bit stuffing/destuffing (11111 to 111110 / 111110 to 11111)
- ITU-T CRC-16 generation/checking (16-bit sequence)
- Flag generation/detection (01111110)
- Abort generation/detection (01111111...)
- Start of frame detection
- End of frame detection
- FIFO overflow and underflow

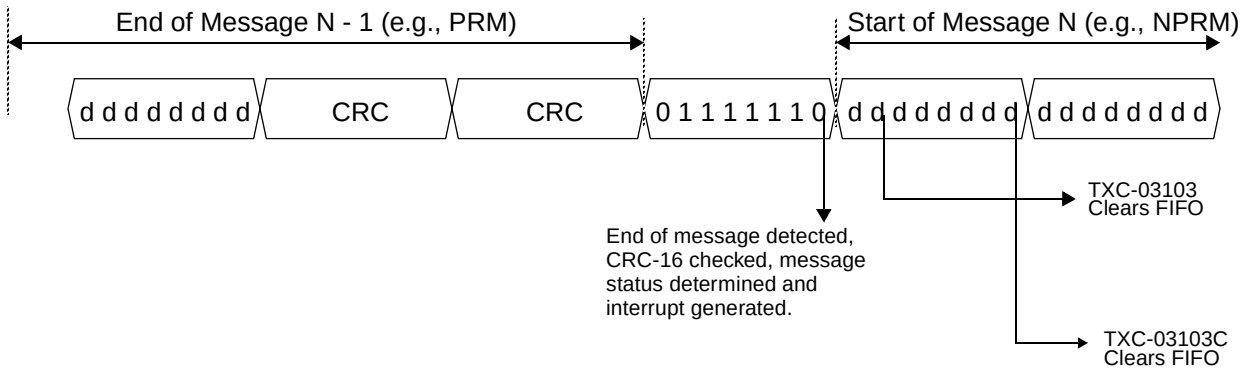
The HDLC receiver is enabled when a 1 is written to control bit EHR (bit 7) in the HDLC Link Control Register X08H. When enabled, the HDLC receiver will remove the stuffed zero bits, search for the opening flag and place the message contents in a 16-byte FIFO. The HDLC link controller will compute a CRC and compare it against the CRC that is received. The received CRC is not stored in the FIFO and is discarded after being received.

The receive FIFO is monitored for fill level, with maskable interrupts and latched indications provided. Bits RXFS1 and RXFS0 (bits 3 and 2) in the HDLC Link Status Register X16H indicate when the receive FIFO is less then half full, equal to or greater than half full, full and overflowed. An interrupt may also be set at the end of the message, or when the FIFO is half full, using the RHIE control bit (bit 3) in the HDLC Link Control Register X08H. Thus, when the messages are always expected to be shorter than the maximum FIFO depth of 16 bytes, the HDLC link controller will generate an interrupt on the completion of the message. When the messages are expected to exceed the maximum FIFO depth of 16 bytes, the controller will generate an interrupt when the FIFO is half filled.

Bits C4-C0 (bits 4-0) in the HDLC Link Receive Data Register (X18H) provide the number of bytes presently stored in the receive FIFO. Bits RHIS2-RHIS0 (bits 7-5) in the HDLC Link Status Register (X16H) provide message status and error indications, including when a bit code message is received. The HDLC link controller will generate a maskable interrupt for start of message detected, valid message received, CRC in error, and message aborted. The message bytes are read by the microprocessor at bits RHD7-RHD0 in register X17H for each framer. Bit 0 corresponds to the first bit received in a byte.

The latest ANSI T1.403 CORE requirements allow performance messages to share the facility data link with the minimum spacing between messages to be a single LAPD flag character. This is different from the previous design constraints of one message per second or command and response message traffic. The TXC-03103 design resets the receive FIFO when the start of a new message is detected. The TXC-03103C design waits until the first byte of the received non-flag character following one or more flag characters (01111110) is collected to reset the receive FDL FIFO.

The figure below describes the change as viewed from the 4 kbit/s data link. By delaying the FIFO reset the minimum time between the FDL interrupt and FIFO reset is extended from 2 bits on the FDL link (500 microseconds) to 8 bits on the FDL link (2.0 milliseconds). This provides enough time for the attached microprocessor to service the interrupt and read out the FDL FIFO prior to the receipt of a back-to-back follow-on message.



The HDLC transmitter is enabled when a 1 is written to control bit EHT (bit 6) in the HDLC Link Control Register X08H. When enabled, the HDLC link controller will transmit flags until data is placed in the transmit FIFO. Up to 16 bytes can be placed in the 16-byte FIFO. The message bytes are written into bits THD7-THD0 in the HDLC Link Transmit Data Register X0AH. Bit 0 corresponds to the first bit transmitted. The transmit bytes are read from the transmit FIFO and a 16-bit CRC is computed until the end of message is detected. When the last byte of the message is written into the FIFO, the microprocessor will set the end of message status bit EOM (bit 4) in the HDLC Link Control Register X08H. The computed 16-bit CRC will be appended to the end of the message followed by at least one flag before another message is transmitted. When the transmit FIFO is emptied without setting the EOM bit, the FIFO will set an underflow indication, and an abort character will be transmitted, thereby terminating the message.

The transmit HDLC link controller provides latched event bits and maskable interrupt bits related to the transmit FIFO status. Information such as underflow and fill status is provided by reading status bits TXFS1-TXFS0 (bits 1-0) in the HDLC Link Status Register X16H.

Transmit HDLC FIFO service interrupts may be programmed to occur when the transmit FIFO is half empty, or when the last byte is sent, by setting control bit THIE (bit 2) in register X08H. For short messages, the entire message may be written into the FIFO, and the controller will generate an interrupt, indicated by status bit THIS (bit 4) in register X16H, when the message has been sent. For longer messages, the controller will generate an interrupt when the FIFO is ready to accept more data.

There are four general types of message transfers, which are described below: transmitting long and short messages, and receiving long and short messages. The difference between the long and short messages is primarily in how the 16-bit FIFOs are serviced. With short messages, the entire message will fit into the FIFOs and interrupts will be generated when the end of the message occurs. With long messages, the message will not fit into the FIFO, and the message will have to be transmitted or received in several segments. Since long and short received messages are similar, their processing is described under the same heading.

Transmit Short Message

To transmit a short message, first configure the transmitter to generate an interrupt at the end of message by writing a 0 to control bit THIE (bit 2) in the HDLC Link Control Register X08H. Then write a 1 to control bit EHT (bit 6) in register X08H to enable the transmitter. The HDLC link controller will transmit flags until data is written into the transmit HDLC FIFO.

Write the message into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X0AH. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred automatically into the FIFO. After the last byte is written into the FIFO, the EOM (bit 4) in register X08H is written with a 1. The transmitter will then begin to send the message bytes until the FIFO is empty. Since the EOM bit was set, the completion of the message will generate an interrupt, if not masked, indicated by the latched THIS status bit ETHIS, (bit 4) in register X0EH. This latched status indication indicates that the message is complete or the FIFO is half full. After the CRC-16 is sent, the HDLC link controller will start to send flags.

Transmit Long Message

To transmit a long message, first configure the transmitter to generate an interrupt at the half full level of the FIFO by writing a 1 to control bit THIE (bit 2) in the HDLC Link Control Register X08H. Then write a 1 to control bit EHT (bit 6) in register X08H to enable the transmitter. The HDLC link controller will transmit flags until data is written into the transmit HDLC FIFO.

Write the first 16-byte message segment into the transmit FIFO by writing each byte in turn to THD7-THD0 in register X0AH. Bit 0 represents the first bit in the byte to be transmitted. The bytes written into THD7-THD0 are transferred automatically into the FIFO. The HDLC link controller will then start to send the message bytes. When the FIFO empties to the half full level, the ETHIS bit (bit 4) in register X0EH will be latched, and an interrupt generated, if the corresponding mask bit MTHIS (bit 4) in register X0FH is set to 0. This is an indication for the microprocessor to write another 8 bytes into the transmit HDLC FIFO. This process of sending and refilling is repeated, 8 bytes at a time, until the last byte in the message is written into the FIFO, when the EOM (bit 4) in register X08H is written with a 1. The transmitter continues to send the final message bytes until the FIFO is empty. When the last byte is transmitted and the FIFO is empty, the ETHIS bit will latch while EOM=1, indicating completion of the message. After the CRC-16 is sent, the HDLC link controller will start to send flags. The latched event register X0EH should be cleared before sending the next message to enable the reception of the status of the next transmitted message. Status bits TXFS1-TXFS0 (bits 1-0) in register X16H indicate the fill level of the transmit FIFO.

Receive Message

To receive a message, first configure the receiver to generate an interrupt at the half full level of the FIFO by writing a 0 to control bit RHIE (bit 3) in the HDLC Link Control Register X08H. Then enable the receiver by writing a 1 to control bit EHR (bit 7) in register X08H. Set mask bits MRHIS2-MRHIS0 (bits 7-5 in control register X01FH) to 001 and MRXFS1-MRXFS0 (bits 3-2 in control register X0FH) to 00.

The receiver will generate an interrupt (provided the corresponding mask bit is written with a 0), when the FIFO is half full or when an end of message is detected. Interrupts from RHIS2-RHIS0 will only be generated for an end of normal message, a received message error or bit code received. Interrupts from RXFS1-RXFS0 indicate FIFO service is needed. The receive message is read from the FIFO by reading the bytes RHD7-RHD0 in register X17H. Bit 0 represents the first bit in the byte to be received. The bytes in RHD7-RHD0 are transferred automatically from the receive FIFO. When the interrupt occurs, the RHIS2-RHIS0 status bits (bits 7 - 5) and RXFS1-RXFS0 (bits 3-2) in register X16H are also set in the ERHIS2-ERHIS0 bits (bits 7-5) and ERXFS1-ERXFS0 (bits 3-2) in the latched register X0EH, indicating the message status. If the message in progress status is set, the microprocessor should read the message bytes from RHD7-RHD0 using the FIFO Depth bits C4-C0 in register X18H to detect the number of bytes stored in the receive FIFO. Please note that the FIFO depth count is updated when the event indication is latched and interrupt generated, and will not be modified until it is read and cleared by the microprocessor. During long messages, the count is allowed to change after the half full indication. If the microprocessor fails to read out the FIFO in time, a second interrupt indication is generated, indicating a full or overflow condition. The reason for interrupt is indicated by status bits RXFS1-RXFS0 (bits 3-2) in register X16H. These control bits provide status information about the fill level of the receive FIFO. An end of message is also indicated by the RHIS2-RHIS0 status bits.

ALARMS

The following line level alarms for each of the four framers are detected in the QT1F-*Plus*: Loss Of Signal (LOS), Alarm Indication Signal (AIS), Out Of Frame (OOF), Yellow Alarm Indication (YEL), Change Of Frame Alignment (CFA), Severely Errored Frame (SEF), transmit slip (TXSLIP) and receive slip (RXSLIP). These alarms are provided by the DS1 Status and Mask Registers (registers X09H-X13H). In addition, the following HDLC link level alarms are supported by the QT1F-*Plus*: Receive HDLC event and status, Transmit HDLC event and status, Receive FIFO event and status, and Transmit FIFO event and status (registers X0EH and X16H). Each HDLC event bit can cause an interrupt when the corresponding mask bit is set to 0 in register X0FH. The latched status event indication (which can also be referred to as a software interrupt indication) for an alarm or condition is latched on either positive transitions, negative transitions, or both transitions. Control bits RISE (bit 6), and FALL (bit 5) in the Global Configuration register 006H determine the transitions that cause an event bit to latch for all four framers, as shown in the following table:

RISE (bit 6)	FALL (bit 5)	Action
0	0	Latched status bit indications in all registers disabled. Hardware and software interrupt indications disabled.
1	0	Latched status indication sets on positive alarm transition, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt status indication bit GIM (bit 7 in register 006H) are both 0.
0	1	Latched status indication sets on negative alarm transition, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt status indication bit GIM (bit 7 in register 006H) are both 0.
1	1	Latched status indication sets on both positive and negative alarm transitions, along with generating a hardware interrupt provided the corresponding mask bit and the global interrupt bit GIM (bit 7 in register 006H) are both 0.

The latched event is cleared by writing a 0 to the associated bit position in the latched status indication register. The QT1F-*Plus* also provides a Global Interrupt Mask (GIM) bit for the microprocessor interrupt pin (pin 125, INT/IRQ). When a 1 is written to control bit GIM (bit 7) in the Global Configuration Register 006H, this hardware interrupt indication pin is tristated when a latched indication (event) bit is set. When a 0 is written into the GIM bit, the hardware interrupt pin is enabled. When enabled, the polarity of the interrupt pin can be inverted by writing a 1 to control bit IPOL (bit 4) in the Global Configuration Register 006H.

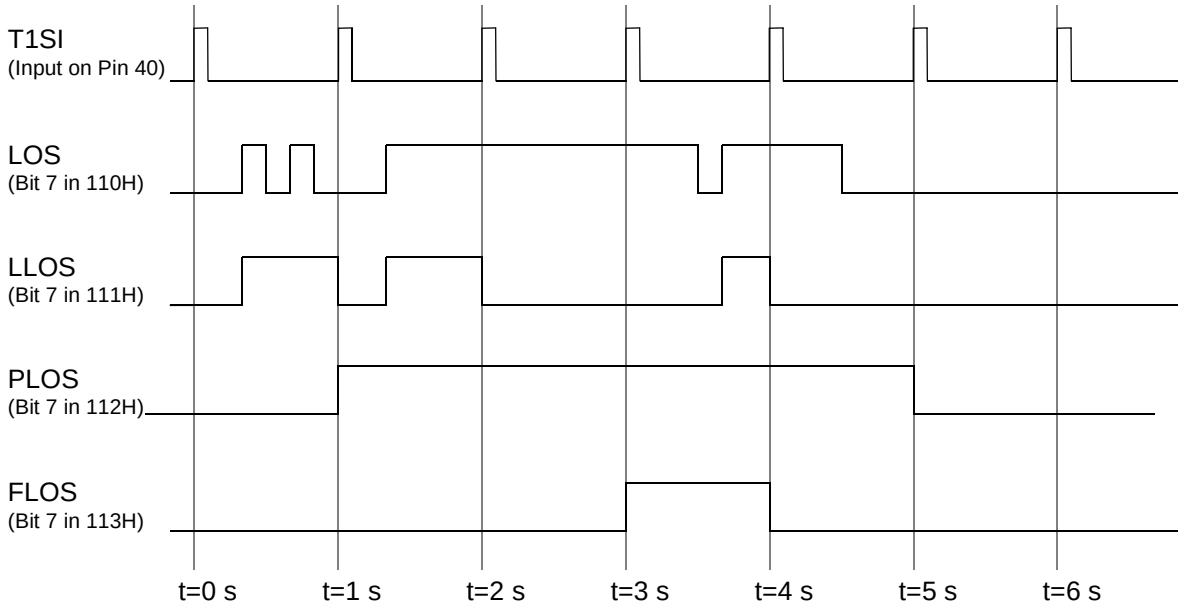
Besides providing individual unlatched and latched alarm status indications, and interrupt mask bits, on a per framer basis, the QT1F-*Plus* provides global interrupt status indication bits, as well as global interrupt mask bits and framer pointer bits in the Global Register segment (registers 00AH-00EH). A global interrupt status indication bit is set to 1 in register 00AH if the same type of alarm occurs in any of the four framers, provided that the corresponding global mask bit in register 00BH is not set to 1 and the QT1F-*Plus* is configured to latch on one of or both transitions of the alarm. Registers 00CH and 00EH provide pointers to the framer which caused the line event or HDLC link event that triggered the interrupt.

For example, assuming a loss of signal alarm occurred in framer 1 only, the LOS alarm will set the LOS bit (bit 7) in the unlatched register 110H. This alarm indication bit will be set to 1 for the duration of the alarm. Assuming that control bits RISE and FALL (bits 6 and 5) in the Global Configuration Register 006H are set to 10 (latched event set on a positive transition), the transition from 0 to 1 of the LOS alarm will cause the LLOS bit (bit 7) in register 111H to latch. A hardware interrupt will be generated on pin 125 if the interrupt mask bit MLOS (bit 7) in register 109H is a 0, and the global interrupt mask bit GIM (bit 7) in register 006H is a 0. If either of these bits is set to 1, the hardware interrupt will not occur. In addition, the latched LOS indication will also cause a Global LOS indication (bit 7) in register 00AH. The framer in which the loss of signal alarm was detected can be found by reading bits 3-0 in register 00CH. The interrupt will be reset by first reading the LLOS latched alarm bit position (bit 7) in register 111H and then writing a 0 into the bit position. This will also clear the global LOS indication bit. Reading the register confirms that the loss of signal alarm occurred in framer 1. If the LOS alarm persists, it will not cause the latched bit position to relatch. The alarm status can be determined by now reading repeatedly the unlatched status bit (bit 7) in register 110H, until it becomes 0, indicating that recovery has taken place.

Shadow Registers

The QT1F-*Plus* also provides shadow registers for the alarms of each of the four framers. The shadow register feature in the QT1F-*Plus* is enabled by writing a 1 to the Enable Performance Monitoring and Fault Monitoring control bit (ENPMFM), bit 3 in the Global Configuration register 006H. By applying a pulse at one second intervals to T1SI (pin 40), an indication bit will be set in register X12H if the corresponding alarm occurred at any time in the last one second interval. In addition, an indication bit will be set in register X13H if the alarm is active, but the transition to the active state did not occur in the last one second interval (i.e., the alarm has persisted for longer than one second). The rising edge of the T1SI pulse will also reset a latched event bit position in register X11H independent of the microprocessor.

Figure 40 illustrates the operation of the shadow registers for a loss of signal (LOS) alarm for framer 1. The behavior shown in the diagram also applies to the other line signal alarms in the same registers (AIS, OOF, YEL, CFA, SEF, TXSLIP, and RXSLIP). This figure assumes that control bits RISE and FALL (bits 6 and 5) in the Global Configuration Register 006H are set to 10 (latched event set on a positive transition). Please note that the LOS alarm causes a latched status indication LLOS (bit 7) in register 111H, and that the latched bit is reset by the rising edge of the T1SI pulse. The PLOS status bit (bit 7) in register 112H is a 1 whenever there is a transition to LOS during the last one second interval or LOS is present at the end of the last one second interval. The FLOS status bit (bit 7) in register 113H is a 1 if the LOS alarm is active but did not become active during the previous one-second interval.



Note 1: For this example, latched events are set only on positive event transitions.

Note 2: PLOS = LOS + LLOS evaluated at one second boundaries (where '+' is a logical or).

Note 3: FLOS = LOS & $\overline{\text{LLOS}}$ evaluated at one second boundaries (where '&' is a logical and, and $\overline{\text{X}}$ is a logical inversion).

Figure 40. Shadow Register Operation

In addition, shadow registers have been provided for monitoring the number of line errors that have occurred in one second intervals. When the Enable PM/FM control bit (ENPMFM), bit 3 in the Global Configuration register 006H, is a 1, the following shadow registers are updated with the count from the previous one-second interval on the rising edges of the one-second pulse provided at the T1SI pin: a 9-bit register for a CRC-6 error count, a 16-bit register for a coding violations count, and an 8-bit register for a framing bit error count. The rising edge of the one-second pulse also clears the counters that were holding the count for the transfer to the shadow registers.

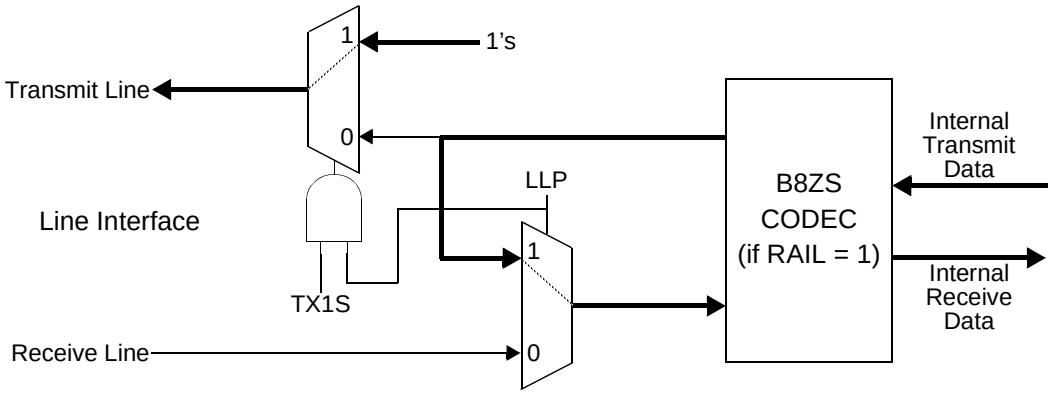
For example, the shadow register for monitoring frame bit errors in framer 1 works in the following way. The 8-bit framing bit error counter FBE7-FBE0 in register 1FCH counts the number of frame bit errors over a one-second interval, which is determined by the T1SI signal. At the rising edge of the pulse on the T1SI pin, the count in register 1FCH is transferred to the shadow register LFBE7-LFBE0 in location 1FAH. The frame bit error counter in register 1FCH is cleared at the same instant and it starts the error count for the next one-second interval. At the end of the next one-second interval, the shadow register is updated with the new count. A counter overflow bit FBEO is also provided (bit 7 in register 1FDH), with a corresponding shadow overflow bit LFBEO (bit 7) in register 1FBH. The microprocessor can also clear the counter in register 1FCH by writing 00H to it. The shadow register holds its count during a microprocessor read cycle.

MAINTENANCE

The QT1F-*Plus* provides three loopback modes. Local, remote line, and payload remote loopbacks are available for each of the four framers. These three loopbacks allow the user to section a network path and isolate a specific failure. In addition, a pseudo-random test generator and analyzer are provided. In-band loop-up and loop-down codes, per ANSI T1.403-1998, are supported in both SF and ESF modes.

Local Loopback

Local loopback for a framer is enabled when a 1 is written to control bit LLP (bit 0) in register X05H. Local loopback connects the transmit path with the receive path in the direction toward the line, as illustrated in Figure 41 below. The loopback is independent of the line interface selected, NRZ or dual unipolar (rail). When control bit TX1S (bit 2) in register X05H is written to 1, an AIS (all ones signal) is transmitted to the line instead of data. Please note that transmit line AIS can be enabled independent of the local loopback feature.

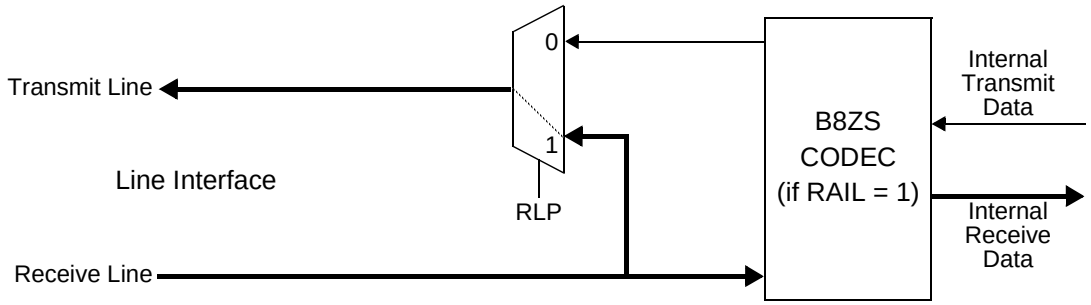


Note: Bold/dashed lines show paths used for TX1S=1 and LLP=1.

Figure 41. Local Loopback

Remote Line Loopback

Remote line loopback for a framer is enabled when a 1 is written to control bit RLP (bit 1) in register X05H. Remote line loopback connects the receive line data back to the transmitter, as illustrated in Figure 42 below. The loopback is performed before the B8ZS codec. The loopback is independent of the line interface selected, NRZ or dual unipolar (rail).



Note: Bold/dashed lines show paths used for RLP=1.

Figure 42. Remote Line Loopback

The remote line loopback can be activated or deactivated by the reception of loop-up or loop-down codes on the line. These codes are described in ANSI T1.403-1998 for the SF mode of operation. This feature is enabled by setting control bit ENPMFM (bit 3) in register 006H to a 1, setting control bit ALUP (bit 6) in register X05H to a 1 and providing a one second pulse on pin T1SI. The specific loop-up code is provided by setting control bits LU6-LU0 (bits 6 - 0) in register 014H to the desired code and bits ULEN1 and ULEN0 (bits 4 and 3) in register 016H to the desired length. If a matching pattern is received for 5 seconds the QT1F-*Plus* channel will automatically enter the remote line loopback state and remain there until a loop-down code is received. The local microprocessor can determine if a channel is in loopback by reading status bits UP (bit 2) and DOWN (bit 1) in register X15H. The specific loop-down code is provided by setting control bits LD6-LD0 (bits 6 - 0) in register 015H to the desired code and bits DLEN1 and DLEN0 (bits1 and 0) in register 016H to the desired length. If a matching pattern is received for 5 seconds the QT1F-*Plus* channel will automatically exit the remote line loopback state.

DS0 Channel Loopback

The DS0 channel loopback feature is enabled when a 1 is written to control bit ENDS0LB (bit 4 in register 0FFH). One or more DS0 channels can be looped back by writing a 1 to the corresponding control bit LBD24-LBD1 in registers X1EH, X1DH and X1CH.

The loopback takes place after the slip buffer and is provided whether the receive slip buffer is enabled or disenabled. Control bits ENDS0LB and LBD24-LBD1 are set to 0 upon a hardware reset. This function requires the presence of TCLKn to operate correctly.

Payload Remote Loopback

The QT1F-*Plus* device provides two payload remote loopback mechanisms; one that is identical to the QDS1F and one that is improved relative to the QDS1F. For the QDS1F style mechanism, setting control bit PAYL (bit 3) in register X05H provides this feature in a way that only the sequence integrity of the payload is kept. A small FIFO is provide between the receive and transmit sides of the framer as shown in Figure 43 below to account for skipping the receive frame bit and inserting the transmit frame bit. Therefore, the framing bit position of the outgoing bit stream is changed relative to the payload signals of the incoming bit stream from the line. This loopback is performed before the receive slip buffer.

In order to keep the framing bit and payload relation intact, the QT1F-*Plus* also provides a payload remote loopback by enabling all 24 DS0 loopbacks. This function requires the presence of TCLKn to operate correctly. In this way, the transmit data highway selects the data from the receive data payload through a buffer that permits received DS0c data to be mapped to transmit DS0c positions for c = 1 through 24, as shown in Figure 43 below.

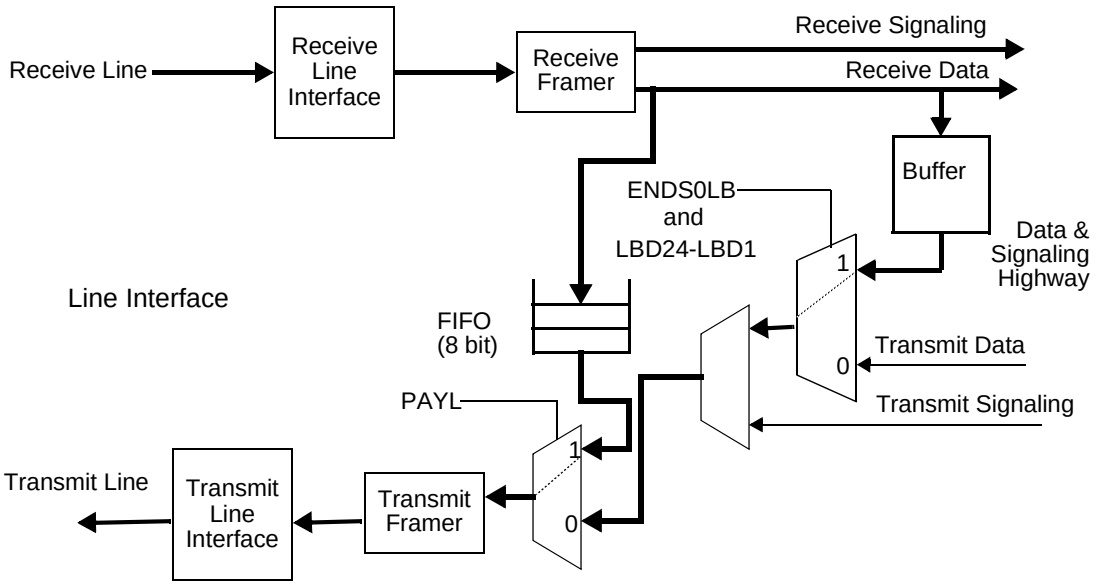


Figure 43. Payload Remote Loopback

BOUNDARY SCAN

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 44. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) input signals) and a Test Data Output (TDO) output signal.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{TRS}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the QT1F-*Plus* device's internal logic, as illustrated in Figure 44. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 20.

Boundary Scan Support

The maximum frequency the QT1F-*Plus* device will support for boundary scan is 10 MHz. The QT1F-*Plus* device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- IDCODE
- BYPASS

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the QT1F-*Plus* device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external QT1F-*Plus* input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the QT1F-*Plus* device remains fully operational. While in this test mode, QT1F-*Plus* input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the QT1F-*Plus* device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

The format of the IDCODE test instruction is "10".

Boundary Scan Reset

Specific control of the $\overline{\text{TRS}}$ pin is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This pin must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power up of the QT1F-*Plus*. If boundary scan testing is to be performed and the pin is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this pin high, but still meet the V_{IL} requirements listed in the "Input, Output and Input/Output Parameters" section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

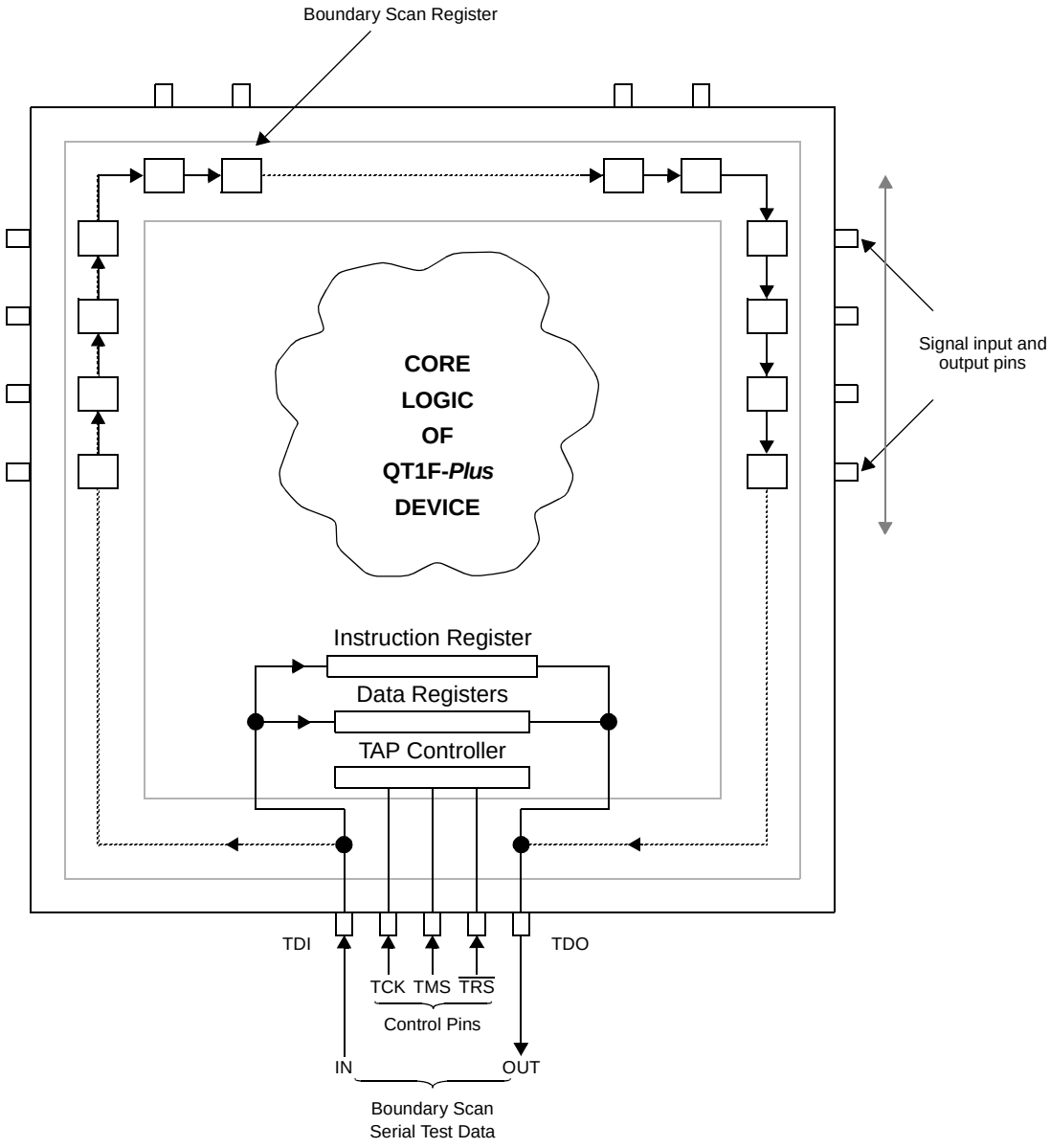


Figure 44. Boundary Scan Schematic

Boundary Scan Chain

A boundary Scan description Language (BSDL) file for the QT1F-*Plus* TXC-03103C device will be made available on the TranSwitch Internet Web site at www.transwitch.com. There are 141 scan cells in the QT1F-*Plus* boundary scan chain. Bidirectional device pins require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their functions. Cells that are not associated with a pin are marked "NA".

Scan Cell No.	I/O	Pin No.	Symbol	Comments
140	CONTROL	NA	XIOTRI_B	A '1' enables the outputs of I/O type OUTPUT3.
139	OUTPUT3	39	RDATA1_O39	
138	OUTPUT3	38	RSIGL1_O38	
137	CONTROL	NA	XRXC1_B	A '0' makes Pins 37, 36 to be OUTPUT.
136	BIDIR_IN	37	RCLK1_IO37	
135	BIDIR_OUT	37	RCLK1_IO37	
134	BIDIR_IN	36	RSYNC1_IO36	
133	BIDIR_OUT	36	RSYNC1_IO36	
132	INPUT	35	TDATA1_I35	
131	CONTROL	NA	XTFT4_ENB	A '0' makes Pin 34 to be OUTPUT.
130	BIDIR_IN	34	TSIGL1_IO34	
129	BIDIR_OUT	34	TSIGL1_IO34	
128	INPUT	33	TCLK1_I33	
127	INPUT	32	TSYNC1_I32	
126	OUTPUT3	31	RDATA2_O31	
125	OUTPUT3	29	RSIGL2_O29	
124	CONTROL	NA	XRXC2_B	A '0' makes Pins 28, 27 to be OUTPUT.
123	BIDIR_IN	28	RCLK2_IO28	
122	BIDIR_OUT	28	RCLK2_IO28	
121	BIDIR_IN	27	RSYNC2_IO27	
120	BIDIR_OUT	27	RSYNC2_IO27	
119	INPUT	26	TDATA2_I26	
118	CONTROL	NA	XTFT2_ENB	A '0' makes Pin 24 to be OUTPUT.
117	BIDIR_IN	24	TSIGL2_IO24	
116	BIDIR_OUT	24	TSIGL2_IO24	
115	INPUT	23	TCLK2_I23	
114	INPUT	22	TSYNC2_I22	
113	OUTPUT3	21	RDATA3_O21	
112	OUTPUT3	19	RSIGL3_O19	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
111	CONTROL	NA	XRXC3_B	A ‘0’ makes Pins 18, 17 to be OUTPUT.
110	BIDIR_IN	18	RCLK3_IO18	
109	BIDIR_OUT	18	RCLK3_IO18	
108	BIDIR_IN	17	RSYNC3_IO17	
107	BIDIR_OUT	17	RSYNC3_IO17	
106	INPUT	16	TDATA3_I16	
105	CONTROL	NA	XTFT3_ENB	A ‘0’ makes Pin 15 to be OUTPUT.
104	BIDIR_IN	15	TSIGL3_IO15	
103	BIDIR_OUT	15	TSIGL3_IO15	
102	INPUT	13	TCLK3_I13	
101	INPUT	12	TSYNC3_I12	
100	OUTPUT3	11	RDATA4_O11	
99	OUTPUT3	10	RSIGL4_O10	
98	CONTROL	NA	XRDY_ENB	A ‘0’ makes Pin 9 to be OUTPUT. A ‘1’ makes Pin 9 to be tristate.
97	OUTPUT3	9	RDY_O9	
96	CONTROL	NA	XRXC4_B	A ‘0’ makes Pins 8, 7 to be OUTPUT.
95	BIDIR_IN	8	RCLK4_IO8	
94	BIDIR_OUT	8	RCLK4_IO8	
93	BIDIR_IN	7	RSYNC4_IO7	
92	BIDIR_OUT	7	RSYNC4_IO7	
91	INPUT	6	TDATA4_I6	
90	CONTROL	NA	XTFT4_ENB	A ‘0’ makes Pin 5 to be OUTPUT.
89	BIDIR_IN	5	TSIGL4_IO5	
88	BIDIR_OUT	5	TSIGL4_IO5	
87	INPUT	4	TCLK4_I4	
86	INPUT	3	TSYNC4_I3	
85	CONTROL	NA	XREF_CLK_EN2_B	A ‘0’ makes Pin 2 to be OUTPUT enabled.
84	OUTPUT3	2	CLKREF2_O2	
83	INPUT	1	RESET_L_I1	
82	INPUT	128	WR_L_I128	
81	INPUT	127	SEL_L_I127	
80	INPUT	126	RD_L_I126	
79	OUTPUT3	125	INT_O125	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
78	CONTROL	NA	XDT_EN	A '0' makes Pins 123-114 to be OUTPUT.
77	BIDIR_IN	123	DAT7_IO123	
76	BIDIR_OUT	123	DAT7_IO123	
75	BIDIR_IN	122	DAT6_IO122	
74	BIDIR_OUT	122	DAT6_IO122	
73	BIDIR_IN	120	DAT5_IO120	
72	BIDIR_OUT	120	DAT5_IO120	
71	BIDIR_IN	119	DAT4_IO119	
70	BIDIR_OUT	119	DAT4_IO119	
69	BIDIR_IN	118	DAT3_IO118	
68	BIDIR_OUT	118	DAT3_IO118	
67	BIDIR_IN	117	DAT2_IO117	
66	BIDIR_OUT	117	DAT2_IO117	
65	BIDIR_IN	115	DAT1_IO115	
64	BIDIR_OUT	115	DAT1_IO115	
63	BIDIR_IN	114	DAT0_IO114	
62	BIDIR_OUT	114	DAT0_IO114	
61	INPUT	113	ADDR11_I113	
60	INPUT	112	ADDR10_I112	
59	INPUT	110	ADDR9_I110	
58	INPUT	109	ADDR8_I109	
57	INPUT	108	ADDR7_I108	
56	INPUT	107	ADDR6_I107	
55	INPUT	106	ADDR5_I106	
54	INPUT	105	ADDR4_I105	
53	INPUT	104	ADDR3_I104	
52	INPUT	103	ADDR2_I103	
51	INPUT	102	ADDR1_I102	
50	INPUT	101	ADDR0_I101	
49	INPUT	100	SYSCLK_I100	
48	INPUT	99	MOTO_I99	
47	OUTPUT3	98	LCS4_L_O98	
46	OUTPUT3	97	LTCLK4_O97	
45	OUTPUT3	96	TNEG4_O96	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
44	OUTPUT3	95	TPOS4_O95	
43	INPUT	93	LRCLK4_I93	
42	INPUT	92	RNEG4_I92	
41	INPUT	91	RPOS4_I91	
40	INPUT	90	LINT4_I90	
39	OUTPUT3	88	LCS3_L_O88	
38	OUTPUT3	87	LTCLK3_O87	
37	OUTPUT3	86	TNEG3_O86	
36	OUTPUT3	85	TPOS3_O85	
35	INPUT	83	LRCLK3_I83	
34	INPUT	82	RNEG3_I82	
33	INPUT	81	RPOS3_I81	
32	INPUT	80	LINT3_I80	
31	OUTPUT3	79	LCS2_L_O79	
30	OUTPUT3	77	LTCLK2_O77	
29	OUTPUT3	76	TNEG2_O76	
28	OUTPUT3	75	TPOS2_O75	
27	INPUT	74	LRCLK2_I74	
26	INPUT	72	RNEG2_I72	
25	INPUT	71	RPOS2_I71	
24	INPUT	70	LINT2_I70	
23	OUTPUT3	69	LCS1_L_O69	
22	OUTPUT3	68	LTCLK1_O68	
21	OUTPUT3	67	TNEG1_O67	
20	OUTPUT3	66	TPOS1_O66	
19	INPUT	65	LRCLK1_I65	
18	INPUT	64	RNEG1_I64	
17	INPUT	63	RPOS1_I63	
16	INPUT	62	LINT1_I62	
15	CONTROL	NA	XMON_ENB	A ‘0’ enables Pins 61, 60.
14	OUTPUT3	61	LSCLK_O61	
13	OUTPUT3	60	LSDO_O60	
12	CONTROL	NA	XFRM_ENB	A ‘0’ makes Pin 59 to be OUTPUT.
11	BIDIR_IN	59	LSDI_IO59	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
10	BIDIR_OUT	59	LSDI_IO59	
9	INPUT	51	SCAN_ENB	
8	INPUT	50	IOTRI_L_I50	
7	INPUT	49	CSO_L_I49	
6	OUTPUT3	48	PRBSOOL_O48	
5	CONTROL	NA	XREF_CLK_EN1_B	A '0' makes Pin 46 to be OUTPUT enabled.
4	OUTPUT3	46	CLKREF1_O46	
3	INPUT	43	CONFIG1_I43	
2	INPUT	42	CONFIG2_I42	
1	INPUT	41	LO_I41	
0	INPUT	40	T1SI_I40	

RESET PROCEDURE

After power-up the QT1F-*Plus* requires a hardware reset. This reset will reset all the per channel registers in the memory map below address X40H. It will also reset all of the global registers at addresses 004H through 0FFH. A low placed on the RESET pin for at least 10 cycles of SYSCLK after all clocks become stable will accomplish the hardware reset.

A global software reset is also available and should be applied at least 40 ms after power-up. This resets the performance counters, internal state machines, and the latched/shadow registers; it does not change the state of any of the control registers. Writing a 91H to control byte RESET in register 005H places the QT1F-*Plus* in a reset state. Writing a value other than 91H to control byte RESET will take the QT1F-*Plus* out of the reset state. The RESET register can be read to determine the reset state of the QT1F-*Plus*. A value of 01H in the RESET register indicates the QT1F-*Plus* is in a reset state; a value of 00H indicates the QT1F-*Plus* is not in reset. A per channel version of this function is available by writing a 1 to control bit SRST (bit 7) in register X05H followed by writing a 0 to control bit SRST. Note that all the memory locations at addresses X40H through XFFH are located in a per channel internal RAM and are not reset by either a hardware reset or a software reset.

Changing the mode of operation of a framer should be followed by a per channel software reset (SRST). The mode bits can be found in framer per channel registers X00H through X04H (RAIL, BE, ENZC, ENSAIS, ENSYEL, LIE, LPOL, TXCP, RXCP, TXNRZP, RXNRZP, PWRD, FDAT, FPOL, BFDL, TXC1, TXC0, RXC, TSE, RSE, TYP1, TYP0, ENAIS, ENOOF, ENLOS, OOF1, OOF0, ALT, SYC1, SYC0, FMD1 and FMD0). Not resetting the framer after changing most mode control bits will have minimal effect. However, if control bits FMD1 and FMD0 (bits 2 and 1) in register X04 are changed a per channel software reset procedure is required. Also, control bits located in per channel internal RAM (at addresses X40H through XFFH) need to be re-programmed after a change to FMD1 or FMD0.

If all four framer channels of the QT1F-*Plus* are not implemented in an application, the channels that are not used should be powered down (by setting control bit PWRD, bit 4 in register X01H to a 0) and all interrupts masked (by setting register X09H to FFH).

MEMORY MAP

The QT1F-*Plus* memory map contains registers and counters which may be accessed by the microprocessor. Addresses which are shown as spare, or which are not listed in the memory map, must not be accessed by the microprocessor. The status designation R indicates a read-only unlatched register location, R(L) a read-only latched register location, W a write-only register location and RW a read/write register location. R and R(L) register bit positions designated as Reserved (R) will read out an indeterminate value unless a 0 or 1 read value is indicated. Some RW Reserved (R) bit positions do not exist (i.e., they have no memory associated with them), so that any values written to these bits cannot be read. Those that do have associated memory should be written to 0, as indicated in the following tables. RW Reserved (R) bit positions should not be used for storage of any application information.

Device ID Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	1	1	1	1	0	0	0	0
002	R	1	1	0	0	0	0	0	1
003	R	0	0	0	0	0	0	0	0

Customer Notebook Register

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004	RW	User Defined Register							

Global Software Register

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005	RW	QT1F-*Plus* Software Reset (RESET byte)							

Global Configuration Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
006	RW	GIM	RISE	FALL	IPOL	ENPMFM	R (0)	R (0)	ENHWM
007		Spare							
008		Spare							
009		Spare							
01A-0FE		Spare							
0FF	RW	Reserved (Set to 0)			ENDS0LB	Reserved			R (0)

Global Status Indication, Interrupt Mask and Pointer Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A	R	GLOS	GAIS	GOOF	GYEL	GCFA/ GAISCI	QSEF	GTXSLIP	GRXSLIP
00B	RW	GMLOS	GMAIS	GMOOF	GMYEL	GMCFA/ GMAISCI	GMSEF	GMTXSLIP	GMRXSLIP
00C	R	Reserved				CHA4	CHA3	CHA2	CHA1
00D		Spare							
00E	R	Reserved				CHDL4	CHDL3	CHDL2	CHDL1
00F		Spare							

Line Interface Control and Monitoring Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010	RW	LCB7 - LCB0 (Command Byte)							
011	RW	LDO7 - LDO0 (Line Interface Data Output)							
012	R	LDI7 - LDI0 (Line Interface Data Input)							
013	RW	BDCST	PRBSFR	PRBSEN	ESP/ EMON	RXTX	ENMONFR	T1CHCS1	T1CHCS0

Loop-Up/Down Control Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
014	RW	R (0)	LU6-LU0 (Loop-Up Code)						
015	RW	R (0)	LD6-LD0 (Loop-Down Code)						
016	RW	Reserved			ULEN1	ULEN0	R (0)	DLEN1	DLEN0

Transmit And Receive Sync Delay Registers

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
017	RW	TSD7 - TSD0 (Transmit Sync Delay)							
018	RW	RSD7 - RSD0 (Receive Sync Delay)							

Clock Reference Selection Register

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
019	RW	CR2S1	CR2S0	ENREF2	1544KHZ	ENREF1	R	CR1S1	CR1S0

PER CHANNEL CONTROL AND STATUS INDICATION REGISTERS

The following registers configure, control or provide status information on a per channel basis. When an address location is written as XXXH, the first X indicates 1, 2, 3 or 4 to identify the associated channel, which corresponds to the like-numbered framer (n=1, 2, 3 or 4).

Framer Configuration and Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100 200 300 400	RW	RAIL	BE	ENZC	ENSYEL	FOD	ENSAIS	LIE	LPOL
101 201 301 401	RW	TXCP	RXCP	TXNRZP	PWRD	FDAT	FPOL	BFDL	RXNRZP
102 202 302 402	RW	TXC1	TXC0	RXC	TSE	RSE	TSR	RSR	FT1M
103 203 303 403	RW	TYP1	TYP0	RXF	TXF	OSE	ENAIS	ENOOF	ENLOS
104 204 304 404	RW	OOF1	OOF0	ALT	SYC1	SYC0	FMD1	FMD0	RSYC
13A 23A 33A 43A	RW	RFD8	RFD7	RFD6	RFD5	RFD4	RFD3	RFD2	RFD1
13B 23B 33B 43B	RW	RFD16	RFD15	RFD14	RFD13	RFD12	RFD11	RFD10	RFD9
13C 23C 33C 43C	RW	RFD24	RFD23	RFD22	RFD21	RFD20	RFD19	RFD18	RFD17
13D 23D 33D 43D	RW	TFD8	TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1
13E 23E 33E 43E	RW	TFD16	TFD15	TFD14	TFD13	TFD12	TFD11	TFD10	TFD9
13F 23F 33F 43F	RW	TFD24	TFD23	TFD22	TFD21	TFD20	TFD19	TFD18	TFD17

Software Reset and Loopback Control Register

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
105 205 305 405	RW	SRST	ALUP	TXUP	TXDN	PAYL	TX1S	RLP	LLP

System AIS and Test Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
106 206 306 406	RW	R (0)	R	R	R (0)	INSPRBS	SFZ	RXFS	TXFS
107 207 307 407	RW	R	SVTAIS	SYSALL1	CRC	FRME	YEL	AISE	BPV

DS1 Status and Mask Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
109 209 309 409	RW	MLOS	MAIS	MOOF	MYEL	MCFA/ MAISCI	MSEF	MTXSLIP	MRXSLIP
110 210 310 410	R	LOS	AIS	OOF	YEL	CFA/AISCI	SEF	TXSLIP	RXSLIP
111 211 311 411	RW	LLOS	LAIS	LOOF	LYEL	LCFA/ LAISCI	LSEF	LTXSLIP	LRXSLIP
112 212 312 412	RW	PLOS	PAIS	POOF	PYEL	PCFA/ PAISCI	PSEF	PTXSLIP	PRXSLIP
113 213 313 413	RW	FLOS	FAIS	FOOF	FYEL	FCFA/ FAISCI	FSEF	FTXSLIP	FRXSLIP

Counters and Counter Shadow Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1EC 2EC 3EC 4EC	R	Reserved							
1ED 2ED 3ED 4ED	R	Reserved							
1EE 2EE 3EE 4EE	R	Reserved							
1EF 2EF 3EF 4EF	R	Reserved							
1F0 2F0 3F0 4F0	RW	LCRC7 - LCRC0 (Latched CRC-6 Error Counter Shadow Register, 9 bits)							
1F1 2F1 3F1 4F1	RW	LCRCO	Reserved (Set to 0)						LCRC8
1F2 2F2 3F2 4F2	RW	CRC7 - CRC0 (CRC-6 Error Counter, 9 bits)							
1F3 2F3 3F3 4F3	RW	CRCO	Reserved (Set to 0)						CRC8
1F4 2F4 3F4 4F4	RW	LCV7 - LCV0 (Latched Coding Violation Counter Shadow Register, 16 bits)							
1F5 2F5 3F5 4F5	RW	LCV15 - LCV8 (Latched Coding Violation Counter Shadow Register, 16 bits)							
1F6 2F6 3F6 4F6	RW	LCVO	Reserved (Set to 0)						
1F7 2F7 3F7 4F7	RW	CV7 - CV0 (Coding Violation Counter, 16 bits)							
1F8 2F8 3F8 4F8	RW	CV15 - CV8 (Coding Violation Counter, 16 bits)							
1F9 2F9 3F9 4F9	RW	CVO	Reserved						
1FA 2FA 3FA 4FA	RW	LFBE7 - LFBE0 (Latched Framing Bit Error Counter Shadow Register, 8 bits)							
1FB 2FB 3FB 4FB	RW	LFBEO	Reserved (Set to 0)						
1FC 2FC 3FC 4FC	RW	FBE7 - FBE0 (Framing Bit Error Counter, 8 bits)							
1FD 2FD 3FD 4FD	RW	FBEO	Reserved (Set to 0)						
1FE 2FE 3FE 4FE	R	Reserved							
1FF 2FF 3FF 4FF	R	Reserved							

Operational Status Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
114 214 314 414	R	TXS1	TXS0	RXS1	RXS0	VTAIS	VTRDI	Reserved	
115 215 315 415	R	RXSF	TXSF	Reserved			UP	DOWN	LINT
11B 21B 31B 41B	R	Reserved							

Slip Buffer Pointer Status Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120 220 320 420	R	TWP7 - TWP0 (Transmit Slip Buffer Write Pointer)							
121 221 321 421	R	TRP7 - TRP0 (Transmit Slip Buffer Read Pointer)							
122 222 322 422	R	TWSBS	Reserved		TWPF4 - TWPF0 (Tx Write Pointer Frame)				
123 223 323 423	R	TRSBS	Reserved		TRPF4 - TRPF0 (Tx Read Pointer Frame)				
124 224 324 424	R	RWP7 - RWP0 (Receive Slip Buffer Write Pointer)							
125 225 325 425	R	RRP7 - RRP0 (Receive Slip Buffer Read Pointer)							
126 226 326 426	R	RWSBS	Reserved		RWPF4 - RWPF0 (Rx Write Pointer Frame)				
127 227 327 427	R	RRSBS	Reserved		RRPF4 - RRPF0 (Rx Read Pointer Frame)				
128 228 328 428	R	Reserved							
129 229 329 429	R	Reserved							

Receive Time Slot Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12A 22A 32A 42A	R	Reserved							
12B 22B 32B 42B	R	Reserved							
1E0 2E0 3E0 4E0	RW	RDE8 - RDE1 (Rx Time Slots 8-1 Selection)							
1E1 2E1 3E1 4E1	RW	RDE16 - RDE9 (Rx Time Slots 16-9 Selection)							
1E2 2E2 3E2 4E2	RW	RDE24 - RDE17 (Rx Time Slots 24-17 Selection)							
1E3 2E3 3E3 4E3	R	Reserved							

Receive Time Slot Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
140 - 157 Ch 1 240 - 257 Ch 2 340 - 357 Ch 3 440 - 457 Ch 4	RW	Frame 1 RDS0 (1) - RDS0 (24) Receive Time Slots TS1 - TS24 X40 - Time Slot 1 X57 - Time Slot 24							
158 - 16F Ch 1 258 - 26F Ch 2 358 - 36F Ch 3 458 - 46F Ch 4	RW	Frame 2 RDS0 (1) - RDS0 (24) Receive Time Slots TS1 - TS24 X58 - Time Slot 1 X6F - Time Slot 24							

Transmit Time Slot Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12C 22C 32C 42C	R	Reserved							
12D 22D 32D 42D	R	Reserved							
12E 22E 32E 42E	R	Reserved							
12F 22F 32F 42F	R	Reserved							
1E4 2E4 3E4 4E4	RW	TDE8 - TDE1 (Tx Time Slots 8-1 Selection)							
1E5 2E5 3E5 4E5	RW	TDE16 - TDE9 (Tx Time Slots 16-9 Selection)							
1E6 2E6 3E6 4E6	RW	TDE24 - TDE17 (Tx Time Slots 24-17 Selection)							
1E7 2E7 3E7 4E7	R	Reserved							

Transmit Time Slot Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
190 - 1A7 Ch 1 290 - 2A7 Ch 2 390 - 3A7 Ch 3 490 - 4A7 Ch 4	RW	Frame 1 TDS0 (1) - TDS0 (24) Transmit Time Slots TS1 - TS24 X90 - Time Slot 1 XA7 - Time Slot 24							
1A8 - 1BF Ch 1 2A8 - 2BF Ch 2 3A8 - 3BF Ch 3 4A8 - 4BF Ch 4	RW	Frame 2 TDS0 (1) - TDS0 (24) Transmit Time Slots TS1 - TS24 XA8 - Time Slot 1 XBF - Time Slot 24							

Signaling Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1E8 2E8 3E8 4E8	RW	SE8 - SE1 (Signaling Enable for Channels 8-1 Selection)							
1E9 2E9 3E9 4E9	RW	SE16 - SE9 (Signaling Enable for Channels 16-9 Selection)							
1EA 2EA 3EA 4EA	RW	SE24 - SE17 (Signaling Enable for Channels 24-17 Selection)							
1EB 2EB 3EB 4EB	R	Reserved							

Receive and Transmit Signaling Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
180 280 380 480	RW	Receive Signaling Bits A8-A1							
181 281 381 481	RW	Receive Signaling Bits A16-A9							
182 282 382 482	RW	Receive Signaling Bits A24-A17							
183 283 383 483	R	Reserved							
184 284 384 484	RW	Receive Signaling Bits B8-B1							
185 285 385 485	RW	Receive Signaling Bits B16-B9							
186 286 386 486	RW	Receive Signaling Bits B24-B17							
187 287 387 487	R	Reserved							
188 288 388 488	RW	Receive Signaling Bits C8-C1							
189 289 389 489	RW	Receive Signaling Bits C16-C9							
18A 28A 38A 48A	RW	Receive Signaling Bits C24-C17							
18B 28B 38B 48B	R	Reserved							
18C 28C 38C 48C	RW	Receive Signaling Bits D8-D1							
18D 28D 38D 48D	RW	Receive Signaling Bits D16-D9							
18E 28E 38E 48E	RW	Receive Signaling Bits D24-D17							
18F 28F 38F 48F	R	Reserved							
1D0 2D0 3D0 4D0	RW	Transmit Signaling Bits A8-A1							
1D1 2D1 3D1 4D1	RW	Transmit Signaling Bits A16-A9							
1D2 2D2 3D2 4D2	RW	Transmit Signaling Bits A24-A17							
1D3 2D3 3D3 4D3	R	Reserved							
1D4 2D4 3D4 4D4	RW	Transmit Signaling Bits B8-B1							
1D5 2D5 3D5 4D5	RW	Transmit Signaling Bits B16-B9							
1D6 2D6 3D6 4D6	RW	Transmit Signaling Bits B24-B17							
1D7 2D7 3D7 4D7	R	Reserved							
1D8 2D8 3D8 4D8	RW	Transmit Signaling Bits C8-C1							
1D9 2D9 3D9 4D9	RW	Transmit Signaling Bits C16-C9							
1DA 2DA 3DA 4DA	RW	Transmit Signaling Bits C24-C17							
1DB 2DB 3DB 4DB	R	Reserved							
1DC 2DC 3DC 4DC	RW	Transmit Signaling Bits D8-D1							
1DD 2DD 3DD 4DD	RW	Transmit Signaling Bits D16-D9							
1DE 2DE 3DE 4DE	RW	Transmit Signaling Bits D24-D17							
1DF 2DF 3DF 4DF	R	Reserved							

Receive Frame Bit Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
130 230 330 430	RW	Fe2/Fs4	DI/Ft4	CRC2/Fs3	DI/Ft3	Fe1/Fs2	DI/Ft2	CRC1/Fs1	DI/Ft1
131 231 331 431	RW	Fe4/X	DI/X	CRC4/X	DI/X	Fe3/Fs6	DI/Ft6	CRC3/Fs5	DI/Ft5
132 232 332 432	RW	Fe6/X	DI/X	CRC6/X	DI/X	Fe5/X	DI/X	CRC5/X	DI/X
133 233 333 433	RW	Fe2/Fs4	DI/Ft4	CRC2/Fs3	DI/Ft3	Fe1/Fs2	DI/Ft2	CRC1/Fs1	DI/Ft1
134 234 334 434	RW	Fe4/X	DI/X	CRC4/X	DI/X	Fe3/Fs6	DI/Ft6	CRC3/Fs5	DI/Ft5
135 235 335 435	RW	Fe6/X	DI/X	CRC6/X	DI/X	Fe5/X	DI/X	CRC5/X	DI/X

HDLC Link Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
108 208 308 408	RW	EHR	EHT	TAB	EOM	RHIE	THIE	EBRI	EBT
10C 20C 30C 40C	R	Reserved							

HDLC Link Transmit and Receive Data Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10A 20A 30A 40A	W	HDLC Transmit Data THD7 - THD0							
10B 20B 30B 40B	RW	Reserved		Transmit Bit Code Data TBCD5 - TBCD0					
117 217 317 417	R	HDLC Receive Data RHD7 - RHD0							
118 218 318 418	R	Reserved			C4 - C0 (HDLC Receive FIFO Depth)				
119 219 319 419	R	Reserved		Receive Bit Code Data RBCD5 - RBCD0					

HDLC Link Status Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10E 20E 30E 40E	RW	ERHIS2 - ERHIS0			ETHIS	ERXFS1 - ERXFS0		ETXFS1 - ETXFS0	
10F 20F 30F 40F	RW	MRHIS2 - MRHIS0			MTHIS	MRXFS1 - MRXFS0		MTXFS1 - MTXFS0	
116 216 316 416	R	RHIS2 - RHIS0			THIS	RXFS1 - RXFS0		TXFS1 - TXFS0	

DS0 Loopback Control Registers

Address CH 1, 2, 3, 4	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11C 21C 31C 41C	RW	LBD8	LBD7	LBD6	LBD5	LBD4	LBD3	LBD2	LBD1
11D 21D 31D 41D	RW	LBD16	LBD15	LBD14	LBD13	LBD12	LBD11	LBD10	LBD9
11E 21E 31E 41E	RW	LBD24	LBD23	LBD22	LBD21	LBD20	LBD19	LBD18	LBD17

Spare Registers

The following registers are designated as spare, where X = 1, 2, 3 or 4. These registers must not be accessed for read or write operations by the microprocessor:

007H, 008H, 009H, 00DH, 00FH, 01AH to 0FEH, X1AH, X1FH

Reserved and Test Registers

The following bit locations in read/write registers are designated as reserved and require zeros to be written into them as indicated in the first two tables below. Some of these bits are designated as internal test bits, etc. The per framer test registers X38 and X39 in the third table may be read but must not be written during normal operation.

Global Registers

Register	Bits	Comments
006	2 - 1	Write a 0 to these bit locations
014	7	Write a 0 to this bit location
015	7	Write a 0 to this bit location
016	2	Write a 0 to this bit location
0FF	7 - 5	Write a 0 to these bit locations
0FF	0	Write a 0 to this bit location

Per Framer Registers (X = 1, 2, 3, 4)

Register	Bits	Comments
X06	7, 4	Write a 0 to these bit locations
XF1	6 - 1	Write a 0 to these bit locations
XF3	6 - 1	Write a 0 to these bit locations
XF6	6 - 0	Write a 0 to these bit locations
XFB	6 - 0	Write a 0 to these bit locations
XFD	6 - 0	Write a 0 to these bit locations

Per Framer Test Registers (X = 1, 2, 3, 4)

Register	Bits	Comments
X38	7 - 0	Lower byte SF loopback code counter
X39	7 - 0	Upper byte SF loopback code counter

MEMORY MAP DESCRIPTIONS

GLOBAL REGISTERS

Device ID Registers

The manufacturer ID, part number code and version of the QT1F-*Plus* are implemented in registers 000H - 003H with read-only capability, as shown in the Memory Map section above. The manufacturer ID is 107 (decimal), and has been assigned for TranSwitch by the Joint Electron Device Engineering Council (JEDEC) of the Solid State Products Engineering Council. This field is 11 bits in length, and is assigned to bits 3 through 0 in register 001H, and bits 7 through 1 in register 000H. Bit 0 (LSB) in register 000H is fixed as a 1, so the value stored in the entire 12- bit field is 0D7H. The part number field is 16 bits long. The part number code used here for the QT1F-*Plus* is 03103 (decimal). The binary equivalent of 03103 (decimal) is assigned to bits 3-0 in register 003H, bits 7-0 in register 002H, and bits 7-4 (LSB) in register 001H (0C1FH). The Revision Level field at bits 7-4 in register 003H represents the version number of the device and is set to 0H, but this value may be changed as the device evolves.

Customer Notebook Register

The read/write bits in this register location are provided for use by the customer's application software.

Address	Bit	Symbol	Description
004	7-0	Notebook	**User Defined Register:** The bits in this read/write register are provided for use by the application software. The contents of this read/write register will have no direct effect on the operation of the QT1F-*Plus*.

Global Software Register

The control bits in this read/write register location are used for resetting the QT1F-*Plus*.

Address	Bit	Symbol	Description
005	7-0	RESET	**Software Reset:** Writing a 91H into this location will reset the QT1F-*Plus*. Writing a value other than 91H will remove the QT1F-*Plus* from the reset state. Reading this location provides a value of 00H if the QT1F-*Plus* is not in reset, and 01H if the QT1F-*Plus* is reset. The QT1F-*Plus* defaults to reset deactivation on an external hardware reset (e.g., power-up). At least 40 ms after power-up, a software reset should be applied to this register location in order to clear the QT1F-*Plus* prior to programming the register positions. The software reset resets the performance counters, internal state machines, and the latched/shadow registers. The control registers are not affected by this reset. In addition to this global reset byte, each of the four framers has an individual software reset bit, which is assigned to bit 7 (SRST) in register location X05H (where X corresponds to the framer's number, n).

Global Configuration Registers

The bits in these read/write registers control QT1F-*Plus* operations on a global basis for all four framers.

Address	Bit	Symbol	Description
006	7	GIM	**Global Interrupt Mask Bit:** A 1 disables (masks) the hardware interrupt pin (pin 125). When not masked (0), any latched status event (if not masked by the corresponding event mask bit) causes a hardware interrupt to occur.
	6	RISE	**Rising Edge Latched Status Event Bits Enable:** This bit works in conjunction with the FALL control bit (bit 5) to provide the following states for controlling the setting of the latched status event indication bits for the four framers. RISE / FALL / Action 0 / 0 / Latched status bit indications for all framers disabled. Hardware interrupt indication disabled. 0 / 1 / Latched status indication bits for all framers set on a negative status event bit indication transition. 1 / 0 / Latched status indication bits for all framers set on a positive status event bit indication transition. 1 / 1 / Latched status indication bits for all framers set on both a positive and a negative status event bit indication transition.
	5	FALL	**Falling Edge Latched Status Event Bits Enable:** Works in conjunction with the RISE control bit according to the table given above.
	4	IPOL	**Hardware Interrupt Polarity Sense:** When set to 1, the polarity of the hardware interrupt pin (pin 125) is inverted from active high to active low for the Intel microprocessor bus. When the Motorola microprocessor bus is selected, the polarity of the hardware interrupt pin (pin 125) is inverted from active low to active high.
	3	ENPMFM	**Enable Performance Monitoring and Fault Monitoring Feature:** When set to 1, the monitoring feature for the PM and FM shadow registers (X12H and X13H) is enabled and the latching of the shadowed performance counters (XF0, XF1, XF4, XF5, XF6, XFA and XFB) is enabled. The register bits set on the rising edges of the one second pulse, which must be present on the T1SI pin (pin 40). When set to 0, the monitoring feature is disabled.
	2-1	Reserved	**Reserved:** Set to 0.
	0	ENHWM	**Enable Hardware Mask Hierarchy:** When set to 1, the masking hierarchy for the alarms is enabled according to the table given below: Alarm Suppression Table (Shaded Columns indicate suppressed alarms) Direction: Line Port to System LOS: X Line AIS: X OOF: X YEL: SLIPS:

Address	Bit	Symbol	Description
0FF	7-5	Reserved	Set to zero.
	4	ENDS0LB	**Enable DS0 Loopback Feature:** A 1 enables the DS0 channel loopback feature for the four framers. DS0 channel loopbacks occur when the corresponding control bits LBD24-LBD1 are written with a 1. Clock TCLKn must be present for the DS0 loopback feature to function.
	3-1	Reserved	These bit locations do not exist.
	0	Reserved	Set to zero.

Global Status Indication, Mask and Pointer Registers

These registers are read-only, except for the mask register 00BH, which is read/write. The bits in the Global Status Indication Register 00AH indicate an alarm caused by a line event on a global basis (i.e., in any framer). If the corresponding mask bit is written with a 1 in the DS1 Mask Register (X09H) it prevents an interrupt generation, but the global indication will be present in register 00AH. Each event bit is formed by OR-gating the corresponding event bits in each of the four framer channels (registers X10H) to provide the individual status indication in register 00AH. A 1 written into a bit position in the Global Mask Register 00BH will mask the interrupt indication for the corresponding bit position in register 00AH. The bits in register locations 00CH and 00EH provide a pointer to the framer which caused the line or HDLC link latched event.

Global Status Indication Register

Address	Bit	Symbol	Description
00A	7	GLOS	**Global Loss Of Signal (LOS) Indication:** This bit is a 1 when any of the four framer channels has detected a loss of signal alarm.
	6	GAIS	**Global AIS Indication:** This bit is a 1 when any of the four framer channels has detected an AIS alarm.
	5	GOOF	**Global Out Of Frame (OOF) Indication:** This bit is a 1 when any of the four framer channels has detected an Out Of Frame alarm.
	4	GYEL	**Global Yellow Alarm (YEL) Indication:** This bit is a 1 when any of the four framers has detected a Yellow alarm.
	3	GCFA/GAISCI	**Global Change In Frame Alignment (CFA)/AIS-CI Indication:** This bit is a 1 when any of the four framer channels has detected a change in frame alignment or detected the AIS-CI signature.
	2	GSEF	**Global Severely Errored Frame (SEF) Indication:** This bit is a 1 when any of the framer channels has detected a Severely Errored Frame (SEF) alarm.
	1	GTXSLIP	**Global Transmit Slip Indication:** This bit is a 1 when any of the four framer channels has detected a transmit slip.
	0	GRXSLIP	**Global Receive Slip Indication:** This bit is a 1 when any of the four framer channels has detected a receive slip.

Global Interrupt Mask Register

Address	Bit	Symbol	Description
00B	7	GMLOS	**Global Loss Of Signal (LOS) Mask Bit:** When set to 1, a loss of signal alarm detected in any framer channel (LLOS, registers X11H) is masked from providing an interrupt indication.
	6	GMAIS	**Global AIS Mask Bit:** When set to 1, an AIS condition detected in any framer channel (LAIS, registers X11H) is masked from providing an interrupt indication.
	5	GMOOF	**Global Out Of Frame (OOF) Mask Bit:** When set to 1, an Out Of Frame alarm detected in any framer channel (LOOF, registers X11H) is masked from providing the global indication in register 00AH.
	4	GMYEL	**Global Yellow Alarm (YEL) Indication Mask Bit:** When set to 1, a Yellow alarm in any framer channel (LYEL, registers X11H) is masked from providing an interrupt indication.
	3	GMCFA/ GMAISCI	**Global Change In Frame Alignment (CFA)/AIS-CI Indication Mask Bit:** When set to 1, a change in frame alignment indication or AIS-CI indication in any framer channel (LCFA/LAISCI, registers X11H) is masked from providing an interrupt indication.
	2	GMSEF	**Global Severely Errored Frame (SEF) Mask Bit:** When set to 1, a Severely Errored Frame alarm detected in any framer channel (LSEF, registers X11H) is masked from providing an interrupt indication.
	1	GMTXSLIP	**Global Transmit Slip Indication Mask Bit:** When set to 1, a transmit slip detected in any framer channel (LTXSLIP, registers X11H) is masked from providing an interrupt indication.
	0	GMRXSLIP	**Global Receive Slip Indication Mask Bit:** When set to 1, a receive slip detected in any framer channel (LRXSLIP, registers X11H) is masked from providing an interrupt indication.

Global Pointer Registers

Address	Bit	Symbol	Description
00C	7-4	R	**Reserved:** Disregard these bits.
	3-0	CHA4-CHA1	**Channel Activity Line Events for Channels 4-1:** A 1 in a bit position points to (indicates) the framer channel that caused the global status indication because of a line event (e.g., loss of signal). For example, 0011 indicates that channels 2 and 1 have a latched line event.
00E	7-4	R	**Reserved**: Disregard these bits.
	3-0	CHDL4-CHDL1	**Channel Activity HDLC Link Event for Channels 4-1:** A 1 in a bit position points to (indicates) the framer channel that caused the global status indication because of a HDLC link event (e.g., receive FIFO event). For example, 1000 indicates that channel 4 has a latched data link event.

Line Interface Control and Monitoring Registers

These registers are read/write, except for register 012H, which is read-only unlatched. The control bits in these registers determine the Line Interface Control information flow between the QT1F-*Plus* and the external line interface transceivers, enable the pseudo-random generator and analyzer, and enable the monitor mode for the QT1F-*Plus*. The Line Interface Control feature is enabled by placing a low on the CONFIG1 pin (pin 43).

Address	Bit	Symbol	Description
010	7-0	LCB7-LCB0	**Line Interface Control Command Byte:** The bits in this register contain the command byte for the external line interface transceiver. The contents of the command byte written into this location depend on the transceiver selected. Please consult the transceiver data sheet for the appropriate codes. The command byte is transmitted via the Line Interface Control serial port output (LSDO). This byte is shifted out of this register starting with bit LCB0 first, and represents the first byte transmitted on the LSDO pin (pin 60).
011	7-0	LDO7-LDO0	**Line Interface Control Serial Data Output Byte:** The bits in this register contain the data byte which is written to the selected external line interface transceiver. The data byte is transmitted via the Line Interface Control serial port output (LSDO). This byte is shifted out of this register starting with bit LDO0 first, and represents the second byte transmitted on the LSDO pin.
012	7-0	LDI7-LDI0	**Line Interface Control Serial Data Input Byte:** The bits in this register contain the data byte which is read from the selected external line interface transceiver. The data byte is received via the Line Interface Control serial port input (LSDI). This byte is shifted into this register starting with bit LDI0 first.
013	7	BDCST	**Broadcast Command:** When this bit is set to 1, the two bytes in the Line Interface Control Command and Serial Data Output Byte registers are broadcasted to all external line interface transceivers. This is accomplished by forcing all line interface chip select signals ($\overline{\text{LCSn}}$) active low. This feature is disabled in the Internal DS1 Monitor Mode (CONFIG2 pin is high).
	6	PRBSFR	**PRBS Framed Mode**: When this bit is set to 1, the internal 2^{15}-1 PRBS generator and analyzer are configured to operate in the framed mode, which means that the channel's Transmit Framer block generates framing. When set to 0 for unframed mode, the internal 2^{15}-1 PRBS generator and analyzer are configured to operate on all of the bits in the transmit and receive data highways.
	5	PRBSEN	**PRBS Enable:** This bit is enabled in the Transmission Mode only. When this bit is set to 1, the internal 2^{15}-1 PRBS analyzer is enabled. The DS1 Channel Selection bits (bits 1 and 0) in this register select which channel's receive data highway is connected to the analyzer. The state of the analyzer is provided on pin PRBSOOL. A low on this pin indicates that the analyzer is locked, while a high indicates the unlocked state. The recovered line clock is the clock source for the Analyzer. If the receive slip buffer is enabled, its read clock source is the LRCLKn input pin. The LO input pin is the clock source for the generator. If the transmit slip buffer is enabled, then the input LO must be synchronous and in phase with TCLKn.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>013
(cont.)</td><td>4</td><td>ESP/EMON</td><td>Enable Serial Port: This feature is enabled when a low is placed on the CONFIG2 pin. When set to 1, a single transfer takes place between the external line interface transceiver and its associated QT1F-Plus framer via the Line Interface Control serial port. The external transceiver is accessed by an active low chip select signal (LCSn) for the transceiver selected by the DS1 selection bits, bits 1 and 0 in this register. This bit must be first set to 0 and then to 1 before another transfer is enabled.

Enable Monitor Port: The Internal DS1 Monitor mode is selected by placing a high on the CONFIG2 pin. The monitor mode has the following operating configurations, controlled by bits 4, 3 and 2 of this register:

<table>
<tr><th>RXTX</th><th>ESP/EMON</th><th>ENMONFR</th><th>Action</th></tr>
<tr><td>X</td><td>0</td><td>X</td><td>Tristate MONDTO and MONCLK leads.</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>Monitor Transmit Framer output via the MONCLK and MONDTO leads.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Receive framer input (NRZ) signal is monitored via the MONCLK and MONDTO leads.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Receive output framer signals are monitored via the MONCLK and MONDTO leads. In additions, the frame pulse is provided via the MONFRM lead. During the Loss of Signal condition, an all ones signal is placed on the MONDTO pin and the MONFRM pin will continue to send out frame pulses according to the prior framing bit position.</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>RXTX</td><td>RX or TX Monitor Selection: When the internal DS1 Monitor Mode is selected (a high is placed on the CONFIG2 pin), a 0 enables the transmit side to be monitored. A 1 enables the receive side to be monitored.</td></tr>
<tr><td></td><td>2</td><td>ENMONFR</td><td>Enable Frame Monitor: This bit operates in conjunction with the CONFIG2 pin and the RXTX and ESP/EMON control bits according to the table given above.</td></tr>
<tr><td></td><td>1-0</td><td>T1CHCS1-
T1CHCS0</td><td>DS1 Channel Selection: Selects the external line interface transceiver, the internal DS1(T1) channel (framer) for monitoring and the receive data highway channel for the internal 2^{15}-1 PRBS analyzer, according to the table given below:

<table>
<tr><th>Bit 1</th><th>Bit 0</th><th>Transceiver/DS1(T1) Monitored/Analyzer</th></tr>
<tr><td>0</td><td>0</td><td>Channel 1</td></tr>
<tr><td>0</td><td>1</td><td>Channel 2</td></tr>
<tr><td>1</td><td>0</td><td>Channel 3</td></tr>
<tr><td>1</td><td>1</td><td>Channel 4</td></tr>
</table></td></tr>
</table>

Loop Up/Down Control Registers

The values written to these registers are transmitted as up or down loop codes when enabled for a channel.

Address	Bit	Symbol	Description
014	7	R	**Reserved:** Set to 0.
	6-0	LU6-LU0	**Loop-Up Code:** The value written to this register represents a loop-up code. The number of bits in the code that are to be transmitted is determined by the value written to control bits ULEN1 and ULEN0 (bits 4 and 3 in register 016H). The loop-up code is transmitted continuously for a channel when control bit TXUP is set (bit 5 in register X05H). For CSU Loop-Up code (10000B), this must be done with 10H at register 014H and "01" at bits 4-3 of register 016H. For NI Loop-Up code (11000B), this must be done with 0CH or 06H or 11H at register 014H and "01" at bits 4-3 of register 016H. Do not set 18H or 03H at register 014H for this application. The value written in this register is used to control the automatic loop-up detection circuit (see control bit ALUP, bit 6 of register X05H).
015	7	R	**Reserved:** Set to 0.
	6-0	LD6-LD0	**Loop-Down Code:** The value written to this register represents a loop-down code. The number of bits in the code that are to be transmitted is determined by the value written to control bits DLEN1 and DLEN0 (bits 1 and 0 in register 016H). The loop-down code is transmitted continuously for a channel when control bit TXDN is set (bit 4 in register X05H). For CSU Loop-Down code (100100B), this must be done with 12H or 09H at register 015H and "10" at bits 1-0 of register 016H. Do not set 24H at register 015H for this application. For NI Loop-Down code (11100B), this must be done with 0EH or 13H at register 015H and "01" at bits 1-0 of register 016H. Do not set 1CH or 07H at register 015H for this application. The value written in this register is used to control the automatic loop-down detection circuit (see control bit ALUP, bit 6 of register X05H).
016	7-5	R	**Reserved:** These bit locations do not exist.
	4-3	ULEN1 ULEN0	**Loop-Up Length:** These two control bits set the number of loop-up bits which are transmitted by the value written into the loop-up code register (bits 6-0 in register 014H) according to the following table. ULEN1 (bit 4) / ULEN0 (bit 3) / Length of the Code 0 / 0 / 4 0 / 1 / 5 1 / 0 / 6 1 / 1 / 7 Note: The length of the loop-up code in register 014H is right justified. The value written in this register is used to control the automatic loop-up detection circuit (see control bit ALUP, bit 6 register X05H). For codes of length 3 or 2 use length 6 or 4 and repeat pattern.

Address	Bit	Symbol	Description
016 (cont.)	2	R	**Reserved:** Set to 0.
	1-0	DLEN1 DLEN0	**Loop-Down Length:** These two control bits set the number of loop-down bits which are transmitted by the value written into the loop-down code register (bits 6-0 in register 015H) according to the following table. DLEN1 (bit 1) — DLEN0 (bit 0) — Length of the Code 0 — 0 — 4 0 — 1 — 5 1 — 0 — 6 1 — 1 — 7 Note: The length of the loop-down code in register 015H is right justified. The value written in this register is used to control the automatic loop-down detection circuit (see control bit ALUP, bit 6 register X05H). For codes of length 3 or 2 use length 6 or 4 and repeat pattern.

Transmit and Receive Sync Delay Registers

The values written in these two read/write registers control the number of clock cycles the transmit sync pulse (TSYNCn) and receive system sync pulse (RSYNCn) may be delayed relative to the transmit system clock (TCLKn), and receive system clock (RCLKn), respectively.

Address	Bit	Symbol	Description
017	7-0	TSD7-TSD0	**Transmit Sync Delay:** The value written into this register location specifies the number of transmit clock cycles (TCLKn) that the transmit Sync signal (TSYNCn) is delayed internal to the QT1F-*Plus*, in increments of one bit time. The default value is 00 hex.
018	7-0	RSD7-RSD0	**Receive Sync Delay:** The value written into this register location specifies the number of receive clock cycles (RCLKn) that the receive Sync signal (RSYNCn) is delayed internal to the QT1F-*Plus*, in increments of one bit time. The default value is 00 hex. This function is only available when RCLKn and RSYNCn are inputs (control bit RXC is set to 0).

Clock Reference Selection Register

The control bits in this read/write register are used to control the clock references for the QT1F-*Plus*.

Address	Bit	Symbol	Description
019	7-6	CR2S1-CR2S0	**Reference Channel Clock 2 Selection:** Selects the channel from which the reference clock CLKREF2 (pin 2) is derived, according to the table given below: Bit 7 / Bit 6 / Reference clock derived from 0 / 0 / Channel 1 0 / 1 / Channel 2 1 / 0 / Channel 3 1 / 1 / Channel 4
	5	ENREF2	**Enable Reference Clock 2:** When set to 1, the reference clock on CLKREF2 (pin 2) is enabled. The reference clock is selected by the Reference Channel Clock 2 Selection control bits (bits 7 and 6), and is derived from receive clock (LRCLKn) for the selected channel. When set to 0, CLKREF2 (pin 2) is tristated. Please note that when set to 1, CLKREF2 will be forced low when a loss of signal (LOS) is detected either locally or from the external line interface transceiver when control bit LIE in bit 1 of Framer Configuration register X00H is a 1.
	4	1544KHZ	**1544 kHz Reference Clock Enable:** When set to 1, the 1544 kHz reference clock selected by the Reference Channel Clock 1 or 2 Selection control bits is provided on the pins CLKREF1 and/or CLKREF2, if enabled by control bits ENREF1, 2 in this register. When set to 0, a divide by 193 circuit is placed between the receive line clock (LRCLKn) and pins CLKREF1 and/or CLKREF2 so that 8 kHz reference signals are provided instead of 1544kHz if enabled by control bits ENREF1, 2 in this register.
	3	ENREF1	**Enable Reference Clock 1:** When set to 1, the reference clock on CLKREF1 (pin 46) is enabled. The reference clock is selected by the Reference Channel Clock 1 Selection control bits (bits 1 and 0), and is derived from receive clock (LRCLKn) for the selected channel. When set to 0, CLKREF1 (pin 46) is tristated. Please note that when set to 1, CLKREF1 will be forced low when a loss of signal (LOS) is detected either locally or from the external line interface transceiver when control bit LIE in bit 1 of Framer Configuration register X00H is a 1.
	2	R	**Reserved:** This bit location does not exist.
	1-0	CR1S1-CR1S0	**Reference Channel Clock 1 Selection:** Selects the channel from which the reference clock CLKREF1 (pin 46) is derived, according to the table given below: Bit 1 / Bit 0 / Reference clock derived from 0 / 0 / Channel 1 0 / 1 / Channel 2 1 / 0 / Channel 3 1 / 1 / Channel 4

PER CHANNEL REGISTERS

Framer Configuration and Control Registers

The control bits in the following read/write registers are used to configure the QT1F-*Plus* for the various modes of operation on a per channel basis. In the following table, n indicates the channel (framer) number 1-4.

Address	Bit	Symbol	Description
100 - Ch 1 200 - Ch 2 300 - Ch 3 400 - Ch 4	7	RAIL	**Dual Unipolar/NRZ Mode Selection:** When set to 1, the line interface for channel n is configured to operate in the dual unipolar mode (rail interface). When set to 0, the line interface for channel n is configured to operate in the NRZ mode.
	6	BE	**B8ZS Enable:** When set to 1 in the dual unipolar mode, the B8ZS CODEC is enabled. When set to 0, the interface CODEC is configured for AMI. In the NRZ mode, the state of this bit sets the TMODEn output bit value (e.g., to enable an external B8ZS codec) when the Fast Sync feature is not selected.
	5	ENZC	**Enable Excess Zeros Count:** When set to 1, the BPV counter will also count excess zeros. For a B8ZS line coding, 8 or more consecutive zeros will be counted as a single error, while for the AMI line code, 16 or more consecutive zeros will be counted as a single error.
	4	ENSYEL	**Enable Signaling Highway Yellow Alarm:** Enabled in the Transmission Mode. When set to 1, a Yellow alarm in the transmit signaling highway (TSIGLn) causes the Yellow Alarm to be propagated to the line for channel n.
	3	FOD	**Force Ones Density:** When set to 1 with AMI line coding selected (bit 6 in this register set to 0), a 1 causes a DS0 channel in the frame that contains all zeros to be transmitted with bit 7 changed to 1.
	2	ENSAIS	**Enable Signaling Highway AIS:** Enabled in the Transmission Mode. When set to 1, an AIS alarm detected in the transmit signaling highway (TSIGLn) causes the AIS condition to be propagated to the line for channel n.
	1	LIE	**General Purpose Interrupt Input Port (LINT) Enable:** When set to 1, the active true state present on the General Purpose Interrupt Input Port (LINTn pin) is logically OR-gated with the internal LOS signal to form the LOS event and interrupt for channel n. Control bit LPOL (bit 0 in this register) determines the active true sense. An active true signal also causes the clock reference pins CLKREF1 (pin 46) and/or CLKREF2 (pin 2), when enabled, to be held low.
	0	LPOL	**General Purpose Interrupt Input Port (LINT) Polarity Selection:** When set to 1, a low present on the General Purpose Interrupt Input Port for channel n (LINTn pin) is the active true state. When set to 0, a high present on the General Purpose Interrupt Input Port is the active true state.

Address	Bit	Symbol	Description
101 - Ch 1 201 - Ch 2 301 - Ch 3 401 - Ch 4	7	TXCP	**Transmit Clock Polarity Selection:** When set to 1, data for channel n is clocked out to the line on the rising edges of the transmit clock (LTCLKn). When set to 0, data is clocked out on the falling edges of the transmit clock (LTCLKn).
	6	RXCP	**Receive Clock Polarity Selection:** When set to 1, data for channel n is clocked in from the line on the rising edges of the receive clock (LRCLKn). When set to 0, data is clocked in on the falling edges of the receive clock (LRCLKn).
	5	TXNRZP	**Transmit NRZ Data Polarity Selection:** When set to 1, the polarity of the transmit NRZ data for channel n (TLDATn) is inverted.
	4	PWRD	**Power-Down Selection:** When reset to 0, the channel enters the inactivated low power state in both the transmit and receive directions. The transmit data value is determined by control bit FPOL when forcing is enabled by control bit FDAT. Please note that control bit FDAT must be set to 1 in the power-down mode, otherwise the transmit data output state will be indeterminate.
	3	FDAT	**Force Transmit Data Power-Down Mode:** This bit must be set to 0 for normal operation. When set to a 1, the transmit data is forced to the state specified by control bit FPOL. This bit must be set to 1 in the power-down mode.
	2	FPOL	**Force Transmit Data Polarity Power-Down Mode:** This control bit is enabled when the FDAT control bit is set to 1. When set to 1, transmit data output for channel n is set to 1 (AIS) in the power-down mode. When set to 0, transmit data is set to 0 in the power-down mode. Please note that the forcing function occurs prior to the selected line encoding function. The following table is a summary of the actions taken by control bits PWRD, FDAT and FPOL. PWRD / FDAT / FPOL / Action 1 / 0 / X / Normal Operation 1 / 1 / 0 / Power-up with transmit data set to 0 1 / 1 / 1 / Power-up with transmit data set to 1 0 / 0 / X / Power-down with indeterminate transmit data (do not use) 0 / 1 / 0 / Power-down, with transmit data set to 0 0 / 1 / 1 / Power-down, with transmit data set to 1
	1	BFDL	**Bypass HDLC Link Bits:** Enabled in the Transmission Mode. When set to 1, the FDL bits in the ESF format from the signaling highway (TSIGLn) are used in place of the HDLC data link in the transmit direction. When the SF format is selected, a 1 enables the Fs bit from the signaling highway to transmitted.
	0	RXNRZP	**Receive NRZ Data Polarity Selection:** When set to 1, the polarity of the received NRZ data for channel n (RLDATn) is inverted.

Address	Bit	Symbol	Description
102 - Ch 1 202 - Ch 2 302 - Ch 3 402 - Ch 4	7-6	TXC1-TXC0	**Transmit Clock Selection:** These two bits select the clock source for clocking out data from the transmit slip buffer to the line interface according to the following table: TXC1 TXC0 Transmit clock source 0 0 Local Oscillator (LO) 0 1 System Transmit Clock (TCLKn) -Transmission Mode* 1 0 Recovered Receive Clock (LRCLKn) 1 1 Invalid combination (do not use) * TXC1, TXC0 = 01 is not a valid selection in MVIP Mode as TCLKn is 2048 kHz and the required transmit line clock is 1544 kHz.
	5	RXC	**Receive Clock Select:** This bit works in conjunction with control bit RSE for selecting the clock (and sync) source for shifting data out of the receive slip buffer to the system. See bit 3 below.
	4	TSE	**Transmit Slip Buffer Enable:** When set to 1, the transmit slip buffer is enabled. When set to 0, the transmit slip buffer is disabled, and data bypasses the slip buffer.The transmit slip buffer must be enabled in the MVIP Mode.
	3	RSE	**Receive Slip Buffer Enable:** This bit works in conjunction with the RXC bit for enabling and disabling the receive slip buffer according to the following table. The receive slip buffer must be enabled in the MVIP Mode. RXC RSE Receive clock source/slip buffer/clock and sync 0 0 System Receive Clock (RCLKn) and Sync Pulse (RSYNCn); Slip buffer disabled. RSYNCn and RCLKn are inputs. Mode not recommended. 0 1 System Receive Clock (RCLKn) and Sync Pulse (RSYNCn); Slip buffer enabled. RSYNCn and RCLKn are inputs. Only valid mode for MVIP. 1 0 Recovered Receive Clock (LRCLKn) and internal sync pulse; Slip buffer disabled. RSYNCn and RCLKn are outputs. 1 1 Recovered Receive Clock (LRCLKn) and internal sync pulse; Slip buffer enabled. RSYNCn and RCLKn are outputs
	2	TSR	**Transmit Slip Buffer Recenter:** When set to 1, this bit forces the transmit slip buffer to recenter. Afterwards this bit should be written with a 0. While set to 0, the transmit slip buffer will recenter automatically to avoid the loss of data (programmed slip).
	1	RSR	**Receive Slip Buffer Recenter:** When set to 1, this bit forces the receive slip buffer to recenter. Afterwards this bit should be written with a 0. While set to 0, the receive slip buffer will recenter automatically to avoid the loss of data (programmed slip).
	0	FT1M	**Fractional T1 Mode:** A 1 written to this bit position enables the transmit and receive fractional T1 feature for the channel (n, X = 1, 2, 3 or 4). A gapped clock for the DS0 channel(s) selected is provided on the RFT1GCn and TFT1GCn leads. DS0 channels are selected by writing a 1 to or more control bits RFD1-RFD24 (X3AH-X3CH). Transmit DS0 channels are selected by writing a 1 to one or more control bits TFD1-TFD24 (X3DH-X3FH). A 0 written to this bit position, combined with a 1 in one or more of RFDc/TFDc, inverts the DS0c(s).

Address	Bit	Symbol	Description
103 - Ch 1 203 - Ch 2 303 - Ch 3 403 - Ch 4	7-6	TYP1-TYP0	**Signaling Type Selection:** The following table lists the signaling selection formats in the transmit and receive directions that are controlled by bits TYP1 and TYP0. TYP1 / TYP0 / Signaling Type 0 / 0 / Clear channel: no signaling. 0 / 1 / Two-state signaling: A bits in frames 6 and 12 for the SF format, and frames 6, 12, 18 and 24 for the ESF format. 1 / 0 / Four-state signaling: A bits in frame 6 for the SF format, and frames 6 and 18 for the ESF format. B bits in frame 12 for SF format and frames 12 and 24 for the ESF format. 1 / 1 / Sixteen-state signaling: ESF format only, A bits in frame 6, B bits in frame 12, C bits in frame 18 and D bits in frame 24. 1 / 1 / Nine-state signaling: SF format only, A bits - frame 6 B bits - frame 12 } Superframe N C bits - frame 6 D bits - frame 12 } Superframe N+1
	5	RXF	**Receive Signaling Freeze:** When set to one, received signaling bits from the DS1 line will not be written into the signaling buffer. The current contents of the signaling buffer will be used for the receive data path to the system.
	4	TXF	**Transmit Signaling Freeze:** When set to one, transmit signaling bits from the system will not be written into the signaling buffer. The current contents of the signaling buffer will be used for the transmit data path to the DS1 line interface port.
	3	OSE	**Ones Stuffing Enable:** When set to 1, the received signaling bit (bit 8) in the 24 DS0 channels is forced to 1 when the signaling bit is extracted. When set to 0, the received signaling bit will remain unchanged toward the system.
	2	ENAIS	**Enable AIS:** When set to 1, detection of a line AIS causes the A-bits in the receive signaling highway RSIGLn to be set to 1 in the Transmission Mode. The A-bits are present in Time Slots 3 through 24 in the signaling highway format. When ENAIS=1, AIS will also be inserted on the receive data highway when control bit SVTAIS (bit 6) in register X07H is a 1.
	1	ENOOF	**Enable OOF:** When set to 1, detection of an Out Of Frame Alarm will cause the A-bits in the receive signal highway bit RSIGLn to be set to 1 in the Transmission Mode. The A-bits are present in Time Slots 3 through 24 in the signaling highway format. When ENOOF=1, AIS will also be inserted on the receive data highway when control bit SVTAIS (bit 6) in register X07H is a 1.
	0	ENLOS	**Enable LOS:** When set to 1, detection of a Loss Of Signal will cause the A-bits in the receive signal highway bit RSIGLn to be set to 1 in the Transmission Mode. The A-bits are present in Time Slots 3 through 24 in the signaling highway format. When ENLOS=1, AIS will also be inserted on the receive data highway when control bit SVTAIS (bit 6) in register X07H is a 1.

Address	Bit	Symbol	Description
104 - Ch 1 204 - Ch 2 304 - Ch 3 404 - Ch 4	7-6	OOF1-OOF0	**Out Of Frame Detection Criteria:** The OOF bits determine the Out Of Frame detection criteria according to the following table: OOF1 OOF0 Out Of Frame Detection Criteria 0 0 2 out of 4 frame sync bits in error 0 1 2 out of 5 frame sync bits in error 1 0 2 out of 6 frame sync bits in error 1 1 2 out of 4 frame sync bits in error
	5	ALT	**Alternate Yellow Alarm:** When set to 1, the Fs-bit in frame 12 in SF frame format will be enabled for sending a Yellow alarm (Fs = 1). When this bit is set to 0, the Fs bit is transmitted as a 0. This feature is not available for the ESF framing format.
	4-3	SYC1 SYC0	**Frame Synchronization Bits:** These control bits determine which framing bits in the SF and ESF frame formats are to be used for frame synchronization (used for the out of frame criteria) according to the table given below. Please note that the Severely Errored Frame (SEF) criterion is not affected by the setting of these bits. SYC1 SYC0 D4 SF ESF 0 0 Not Used Not Used 0 1 Fs bits FPS bits 1 0 Ft bits Not Used 1 1 Fs and Ft bits FPS and CRC-6 bits In D4 SF mode, with frame sync using the Fs bits (SYC1=0, SYC0=1), the frame counter in register XFC will not report Ft bit errors. With frame sync using the Ft bits (SYC1=1, SYC0=0), the frame counter at register XFC will not report Fs bit errors.
	2-1	FMD1 FMD0	**Framing Mode Selection Bits:** These controls bits determine the framing mode according to the table give below: FMD1 FMD0 Framing Mode 0 0 Transparent (no framing) 0 1 D4 SF 1 0 Not Used 1 1 ESF Note: Control bits located in per channel internal RAM (at addresses X40H-XFFH) need to be re-programmed after a change to FMD1 or FMD0.
	0	RSYC	**Resync Enable:** A 1 causes the framer to reset the frame alignment circuit, and start the search for a new frame alignment pattern.

Address	Bit	Symbol	Description
13A - Ch 1 23A - Ch 2 33A - Ch 3 43A - Ch 4	7-0	RFD8-RFD1	**Receive Enable Fractional DS0 Channels 8-1:** The receive fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (RSIGL/RFT1GC) to be generated for the corresponding DS0 channels (8-1). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and this bit for the selected DS0 set to a one, the corresponding DS0 in RDATAn is inverted, in Transmission or MVIP Modes.
13B - Ch 1 23B - Ch 2 33B - Ch 3 43B - Ch 4	7-0	RFD16-RFD9	**Receive Enable Fractional DS0 Channels 16-9:** The receive fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (RSIGL/RFT1GC) to be generated for the corresponding DS0 channels (16-9). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and this bit for the selected DS0 set to a one, the corresponding DS0 in RDATAn is inverted, in Transmission or MVIP Modes.
13C - Ch 1 23C - Ch 2 33C - Ch 3 43C - Ch 4	7-0	RFD24-RFD17	**Receive Enable Fractional DS0 Channels 24-17:** The receive fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (RSIGL/RFT1GC) to be generated for the corresponding DS0 channels (24-17). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and this bit for the selected DS0 set to a one, the corresponding DS0 in RDATAn is inverted, in Transmission or MVIP Modes.
13D - Ch 1 23D - Ch 2 33D - Ch 3 43D - Ch 4	7-0	TFD8-TFD1	**Transmit Enable Fractional DS0 Channels 8-1:** The transmit fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (TSIGL/TFT1GC) to be generated for the corresponding DS0 channels (8-1). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and with this bit for the selected DS0 set to a one, the corresponding DS0 is inverted in TDATAn, in Transmission or MVIP Modes.
13E - Ch 1 23E - Ch 2 33E - Ch 3 43E - Ch 4	7-0	TFD16-TFD9	**Transmit Enable Fractional DS0 Channels 16-9:** The transmit fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (TSIGL/TFT1GC) to be generated for the corresponding DS0 channels (16-9). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and with this bit for the selected DS0 set to a one, the corresponding DS0 is inverted in TDATAn, in Transmission or MVIP Modes.
13F - Ch 1 23F - Ch 2 33F - Ch 3 43F - Ch 4	7-0	TFD24-TFD17	**Transmit Enable Fractional DS0 Channels 24-17:** The transmit fractional T1 mode is enabled when control bit FT1M is a 1 and the CONFIG1 pin is low (Transmission Mode). A 1 written to one or more bits enables a gapped clock (TSIGL/TFT1GC) to be generated for the corresponding DS0 channels (24-17). With the FT1M bit set to 0 in the relevant X02H, the CONFIG1 pin either low or high, and with this bit for the selected DS0 set to a one, the corresponding DS0 is inverted in TDATAn, in Transmission or MVIP Modes.

Software Reset and Loopback Control Register

The control bits in the following read/write register are used to reset each of the channels, and to configure each of the channels within the QT1F-*Plus* for the various loopback modes of operation.

Address	Bit	Symbol	Description
105 - Ch 1 205 - Ch 2 305 - Ch 3 405 - Ch 4	7	SRST	**Software Reset Channel n:** When set to 1, the channel is initialized and held in the reset state until a 0 is written into this bit position to permit commencement of channel operation.
	6	ALUP	**Automatic Loopback:** This control bit is enabled when control bit ENPMFM (bit 3 in register 006H) is a 1. When set to 1, a remote line loopback state is entered automatically when a loop-up code match is detected, and cleared automatically when the loop-down code match is detected. The loopback state is entered and cleared if the matches persist for 5 seconds or more. The UP and DOWN status bits in register X15H indicate the condition. The loop-up code is determined by control bits LU6 - LU0 (value in register 014H) whose length is defined by the code written to control bits ULEN1 and ULEN0 (bits 4 and 3 in register 016H). The loop-down code is determined by control bits LD6 - LD0 (value in register 015H) whose length is defined by the code written to control bits DLEN1 and DLEN0 (bits 1 and 0 in register 016H).
	5	TXUP	**Transmit Loop-Up Code Enable:** When set to 1, the loop-up code as determined by control bits LU6 - LU0 (value in register 014H) whose length is defined by the code written to control bits ULEN1 and ULEN0 (bits 4 and 3 in register 016H) is transmitted continuously. The loop-up code is released when this bit is set to 0.
	4	TXDN	**Transmit Loop-Down Code Enable:** When set to 1, the loop-down code as determined by control bits LD6 - LD0 (value in register 015H) whose length is defined by the code written to control bits DLEN1 and DLEN0 (bits 1 and 0 in register 016H) is transmitted continuously. The loop-down code is released when this bit is set to 0.
	3	PAYL	**Payload Loopback Enable:** When set to 1, a payload loopback will be enabled until this bit position is written with a 0. The data and signaling bits from all 24 received DS0s (192 bits per frame) are taken from before the receive slip buffer and are substituted for the data and signaling bits from the transmit slip buffer output and signaling buffer output on a first come first serve basis. Only receive bit ordering is maintained. DS0 bit and byte alignments to the frame bit position are lost.
	2	TX1S	**Transmit AIS (all ones):** When set to 1, an AIS (all ones) is transmitted instead of data during a local loopback. When set to 0, data is transmitted during a local loopback.
	1	RLP	**Remote Line Loopback Enable:** When set to 1, the remote line loopback feature is enabled until this bit position is written with a 0. Receive line data (prior to the B8ZS codec) is looped back as transmit line data when this loopback feature is enabled.
	0	LLP	**Local Loopback Enable:** When set to 1, the local loopback feature is enabled until this bit position is written with a 0. Transmit data (after the B8ZS codec) is looped back as received data when this loopback feature is enabled. When control bit TX1S (bit 2) is a 0 in register X05H, data is transmitted. When TX1S is a 1, AIS is transmitted. The AIS signal is defined as an all ones signal.

System AIS and Test Registers

The control bits in the following read/write registers are used to generate test conditions and to configure the system interface for AIS in channel (framer) n.

Address	Bit	Symbol	Description
106 - Ch 1 206 - Ch 2 306 - Ch 3 406 - Ch 4	7	R	**Reserved:** Set to 0.
	6-5	R	**Reserved:** These bit locations do not exist.
	4	R	**Reserved:** Set to 0.
	3	INSPRBS	**Insert Pseudo-Random Bit Sequence Enable:** When set to 1, PRBS is inserted for the terminal data on the transmit data highway. This feature is only available for Transmission Mode. To resume normal operation, this bit position must be written with a 0.
	2	SFZ	**System Freeze:** When set to 1, the output clocks LTCLKn and RCLKn are forced to zero. The input clocks LRCLKn and TCLKn are gated off. To resume normal operation, this bit position must be written with a 0.
	1	RXFS	**Receive Fast Sync Enable:** When set to 1, and the NRZ mode is selected, a pulse received on the RNEGn lead will force the synchronization of this pulse to be interpreted as bit position 192 of the last frame of a multiframe for either ESF or SF format. When set to 0, coding violations indicated on the RNEGn lead are counted.
	0	TXFS	**Transmit Fast Sync Enable:** When set to 1, and the NRZ mode is selected, a synchronization pulse will be transmitted on the TNEGn lead every three milliseconds in bit position 192 of frame 24 for the ESF format and every other frame 12 when the SF format is selected.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">107 - Ch 1
207 - Ch 2
307 - Ch 3
407 - Ch 4</td><td>7</td><td>R</td><td>Reserved: This bit location does not exist.</td></tr>
<tr><td>6</td><td>SVTAIS</td><td>System VTAIS: When set to 1, the AIS, OOF and LOS alarms, if enabled by setting to 1 their respective ENAIS (bit 2), ENOOF (bit 1), and ENLOS (bit 0) control bits in the Signaling and Time Slot Control register X03H, cause the generation of AIS on the data highway. The AIS is sent until the alarm has recovered, or the enable bit (e.g., ENAIS) is set to 0. The following table lists the operation of control bit ENOOF and this bit. Control bits ENAIS and ENLOS function in similar fashion.

Transmission Mode

<table>
<tr><th>ENOOF</th><th>SVTAIS</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>No AIS generated on signaling or data highway.</td></tr>
<tr><td>0</td><td>1</td><td>No AIS generated on signaling or data highway.</td></tr>
<tr><td>1</td><td>0</td><td>AIS generated only on signaling highway when OOF alarm is detected.</td></tr>
<tr><td>1</td><td>1</td><td>AIS generated on signaling and data highways when OOF alarm is detected.</td></tr>
</table>

MVIP Mode

<table>
<tr><th>ENOOF</th><th>SVTAIS</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>No AIS generated on data highway.</td></tr>
<tr><td>0</td><td>1</td><td>No AIS generated on data highway.</td></tr>
<tr><td>1</td><td>0</td><td>No AIS generated on data highway even when OOF alarm is detected.</td></tr>
<tr><td>1</td><td>1</td><td>AIS generated on data highway when OOF alarm is detected.</td></tr>
</table>

Please note that the microprocessor can cause AIS to be generated for the receive data highway independently of the two control bits by writing a 1 to control bit SYSALL1 (bit 5) in this register.</td></tr>
<tr><td>5</td><td>SYSALL1</td><td>Send System AIS: When set to 1, AIS (all ones) is sent on the receive data highway. AIS will be transmitted on the receive data highway until this bit is written with a 0.</td></tr>
<tr><td>4</td><td>CRC</td><td>Generate One CRC-6 Error: This feature is enabled when control bits FMD1 and FMD0 (bits 2 and 1) in register X04H are equal to 11 (ESF Format). When this bit is set to 1, the CRC-6 bits in the ESF format are transmitted in the inverted state once. To send another CRC-6 error, this bit must be first written with a 0, and then a 1.</td></tr>
<tr><td>3</td><td>FRME</td><td>Generate One Frame Error: When set to 1, the transmitter will send one frame bit (Fs, Ft or FPS) in error once. To transmit another framing error, this bit must be first written with a 0, and then a 1.</td></tr>
</table>

Address	Bit	Symbol	Description
107 - Ch 1 207 - Ch 2 307 - Ch 3 407 - Ch 4 (cont.)	2	YEL	**Generate Yellow Alarm Indication:** When set to 1, the Yellow Alarm Indication is transmitted as a 1 until the microprocessor writes a 0 into this bit position. The Yellow alarm is defined as bit 2 in each of 24 DS0 channels equal to 0 for the SF frame format, the Fs bit in frame 12 equal to 1 for the Japanese SF frame format, and a sequence of eight ones followed by eight zeros (1111111100000000) in the 4 kbit/s data channel for the ESF format.
	1	AISE	**Transmit Line AIS Enable:** When set to 1, a line AIS is transmitted. A line AIS is defined as all ones transmitted in the frame. Line AIS is transmitted until this bit is written with a 0.
	0	BPV	**Generate Bipolar Violation (BPV) Error:** When the dual unipolar mode is selected by bit 7 in register X00H, a 1 in this bit position causes a single BPV error to be sent. The microprocessor must write a 0 to this bit before another BPV error can be transmitted by setting it to 1.

DS1 Status and Mask Registers

These registers are read/write, except for registers X10H, which are read-only unlatched. The status bits in the X11H register represent the latched status indications generated by the channel alarms. The bits latch on either the rising edge, the falling edge, or both edges of the current status or interrupt request event bits as defined by the RISE/FALL control bits (bits 6 and 5) in the Global Configuration Register 006H. A latched bit will cause a hardware interrupt indication when the global interrupt mask bit GIM (bit 7) in register 006H and the corresponding mask bits in the mask registers 00BH and X09H are all written with a 0. The bits in register X10H represent the current (unlatched) alarm status. A latched status bit is reset by writing a 0 into the latched bit position, or by the rising edge of the T1SI pulse when the performance monitoring/fault monitoring feature is enabled. This feature activates the shadow registers X12H and X13H, and it is enabled by writing a 1 to control bit ENPMFM (bit 3) in the Global Configuration register 006H.

Address	Bit	Symbol	Description
109 - Ch 1 209 - Ch 2 309 - Ch 3 409 - Ch 4	7	MLOS	**Loss Of Signal (LOS) Mask Bit:** When set to 1, detection of a loss of signal alarm is masked from providing a hardware interrupt.
	6	MAIS	**AIS Mask Bit:** When set to 1, detection of an AIS condition is masked from providing a hardware interrupt.
	5	MOOF	**Out Of Frame (OOF) Mask Bit:** When set to 1, detection of an Out Of Frame alarm is masked from providing a hardware interrupt.
	4	MYEL	**Remote Yellow Alarm Mask Bit:** When set to 1, detection of a Yellow alarm indication is masked from providing a hardware interrupt.
	3	MCFA/ MAISCI	**Change In Frame Alignment (CFA)/AIS-CI Mask Bit:** When set to 1, detection of a change in frame alignment (CFA) or the AIS-CI signature indication is masked from providing a hardware interrupt.
	2	MSEF	**Severely Errored Frame Mask Bit:** When set to 1, detection of a severely errored frame alarm is masked from providing a hardware interrupt.
	1	MTXSLIP	**Transmit Slip Indication Mask Bit:** When set to 1, detection of a transmit slip is masked from providing a hardware interrupt.
	0	MRXSLIP	**Receive Slip Indication Mask Bit:** When set to 1, detection of a receive slip is masked from providing a hardware interrupt.

Address	Bit	Symbol	Description
110 - Ch 1 210 - Ch 2 310 - Ch 3 410 - Ch 4	7	LOS	**Loss Of Signal (LOS) Alarm (Unlatched):** A 1 indicates a loss of signal has been detected. A loss of signal alarm is detected when the incoming signal for the rail interface only has no transitions for 175 ± 75 consecutive pulse positions. The LOS alarm is cleared when an average pulse density of at least 12.5% has been received for 175 ± 75 contiguous pulse positions starting with a pulse. In addition, an external LOS indication from the external line transceiver (using the LINTn pin) can be OR-gated with this alarm by setting control bit LIE (bit 1) in register X00H to 1.
	6	AIS	**AIS Indication (Unlatched):** A 1 indicates that a line Alarm Indication Signal (AIS) has been detected. A line AIS is detected if 99.9% or more ones are present in the received signal in a period of 48 ms. Recovery occurs when the line signal has fewer than 99.9% of ones in a 48 ms period.
	5	OOF	**Out Of Frame (OOF) Alarm (Unlatched):** A 1 indicates that an Out Of Frame alarm has been detected. The alarm is programmed using the OOF1 and OOF0 control bits (bits 7 and 6) in register X04H. The selection of frame synchronization bits used for frame alignment is programmed using the SYC1 and SYC0 control bits (bits 4 and 3) in register 04H.
	4	YEL	**Yellow Alarm (YEL) Indication (Unlatched):** A 1 indicates the current state of the Yellow alarm. A Yellow alarm is detected within 32 ms for the ESF format and 335 ms for the SF format, with no line errors present. The alarm is detected within one second in the presence of line errors occurring at the rate of one error in 1000 bits.
	3	CFA/AISCI	**Change In Frame Alignment (CFA)/ AIS-CI Indication (Unlatched):** A 1 indicates that the frame alignment circuit has detected a change in the frame alignment pattern within the last 125 microseconds only after frame alignment has been detected. If AIS is true, this bit also indicates that the AIS-CI signature has been detected twice or more. The AIS-CI signature is an all ones pattern logically 'ANDed' with the code 1111 1111 0011 1110 (left to right), one bit of the code every 386 bits. This signature pattern typically repeats every 4 milliseconds for approximately 150 milliseconds, followed by 1.11 seconds of all ones, with the entire 1.26 second pattern repeating as long as the alarm persists.
	2	SEF	**Severely Errored Frame (SEF) Indication:** A 1 indicates a severely errored frame has been detected in the previous 125 microseconds. For the SF format, an SEF indication occurs if two or more frame bit errors (Ft bit only) are detected within a 0.75 ms period. For the ESF format, SEF is declared when two or more frame bit errors occur over a 3.0 ms period. Recovering occurs when fewer then two errors are detected for the periods indicated for the two frame formats (SF and ESF).
	1	TXSLIP	**Transmit Slip Indication (Unlatched):** This bit reflects the current status of the transmit slip buffer with respect to a slip being executed in the previous 125 microseconds.
	0	RXSLIP	**Receive Slip Indication (Unlatched):** This bit reflects the current status of the receive slip buffer with respect to a slip being executed in the previous 125 microseconds.

Address	Bit	Symbol	Description
111 - Ch 1 211 - Ch 2 311 - Ch 3 411 - Ch 4	7	LLOS	**Latched Loss Of Signal (LOS):** This bit is set to 1 on an active edge of LOS which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	6	LAIS	**Latched AIS:** This bit is set to 1 on an active edge of AIS which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	5	LOOF	**Latched Out Of Frame (OOF):** This bit is set to 1 on an active edge of OOF which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	4	LYEL	**Latched Yellow Alarm (YEL) Indication:** This bit is set to 1 on an active edge of YEL which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	3	LCFA/ LAISCI	**Latched Change In Frame Alignment (CFA)/AIS-CI Indication:** This bit is set to 1 on an active edge of CFA/AISCI which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	2	LSEF	**Latched Severely Errored Frame (SEF) Indication:** This bit is set to 1 on an active edge of SEF which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	1	LTXSLIP	**Latched Transmit Slip Indication:** This bit is set to 1 on an active edge of TXSLIP which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register, location 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.
	0	LRXSLIP	**Latched Receive Slip Indication:** This bit is set to 1 on an active edge of RXSLIP which is selected by the RISE (bit 6) and FALL (bit 5) bits in the Global Configuration Register 006H. If not masked by the corresponding mask bit in register X09H or the GIM bit in register 006H, an interrupt is generated. This bit is cleared by writing a 0 into this bit position.

Address	Bit	Symbol	Description
112 - Ch 1 212 - Ch 2 312 - Ch 3 412 - Ch 4	7	PLOS	**Loss Of Signal (LOS) One Second Error:** This bit is set to 1 if the LOS alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	6	PAIS	**AIS One Second Error:** This bit is set to 1 if the AIS indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	5	POOF	**Out Of Frame (OOF) One Second Error:** This bit is set to 1 if the OOF alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	4	PYEL	**Yellow Alarm (YEL) Indication One Second Error:** This bit is set to 1 if the YEL indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	3	PCFA/ PAISCI	**Change In Frame Alignment (CFA)/AIS-CI One Second Error:** This bit is set to 1 if the CFA/AISCI indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	2	PSEF	**Severely Errored Frame (SEF) Indication One Second Error:** This bit is set to 1 if the SEF alarm occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	1	PTXSLIP	**Transmit Slip Indication One Second Error:** This bit is set to 1 if the TXSLIP indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	0	PRXSLIP	**Receive Slip Indication One Second Error:** This bit is set to 1 if the RXSLIP indication occurred at any time in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.

Address	Bit	Symbol	Description
113 - Ch 1 213 - Ch 2 313 - Ch 3 413 - Ch 4	7	FLOS	**Loss Of Signal (LOS) Persistent Error:** This bit is set to 1 if the LOS alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	6	FAIS	**AIS Persistent Error:** This bit is set to 1 if the AIS indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	5	FOOF	**Out Of Frame (OOF) Persistent Error:** This bit is set to 1 if the OOF alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	4	FYEL	**Yellow Alarm (YEL) Indication Persistent Error:** This bit is set to 1 if the YEL indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	3	FCFA/ FAISCI	**Change In Frame Alignment (CFA) /AIS-CI Persistent Error:** This bit is set to 1 if the CFA/AISCI indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register X006H must be set to 1.
	2	FSEF	**Severely Errored Frame (SEF) Persistent Error:** This bit is set to 1 if the SEF alarm is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	1	FTXSLIP	**Transmit Slip Indication Persistent Error:** This bit is set to 1 if the TXSLIP indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.
	0	FRXSLIP	**Receive Slip Indication Persistent Error:** This bit is set to 1 if the RXSLIP indication is active but did not become active in the last one second interval. The T1SI signal must be present and control bit ENPMFM (bit 3) in the Global Configuration register 006H must be set to 1.

Counters and Counter Shadow Registers

The QT1F-*Plus* provides counter and counter shadow read/write registers for CRC-6 bit errors, coding violations (with or without excess zeros), and framing errors. The counter shadow registers provide the microprocessor with an error count for the previous one second interval. A counter and the corresponding counter shadow register (and their overflow bits) are cleared when the microprocessor writes 0 to their bits. When the shadow register feature is enabled by writing a 1 to control bit ENPMFM (bit 3) in the Global Configuration Register 006H, the rising edges of a one second interval pulse also clear the counters (and the overflow bits, if set). The shadow registers for the various counters are also updated at one second intervals by the rising edge of the pulse applied to the T1SI pin (pin 40).

Address	Bit	Symbol	Description
1F0 - Ch 1 2F0 - Ch 2 3F0 - Ch 3 4F0 - Ch 4	7-0	LCRC7-LCRC0	**Latched CRC-6 Error Counter Shadow Register:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This register contains the lower 8 bits of the 9-bit shadow register assigned for holding the CRC-6 error count that occurred in the previous one second interval. This location is updated from CRC7-CRC0 with a new count at one second intervals on the rising edges of the T1SI signal. Bit 0 is the LSB of the 9-bit count.
1F1 - Ch 1 2F1 - Ch 2 3F1 - Ch 3 4F1 - Ch 4	7	LCRCO	**Latched CRC-6 Error Counter Overflow Bit:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This bit contains the overflow indication associated with the 9-bit shadow register LCRC8-LCRC0 assigned for holding the CRC-6 error count that occurred in the previous one second interval. This location is updated from CRCO at one second intervals on the rising edges of the T1SI signal.
	6-1	R	**Reserved**: Set to 0.
	0	LCRC8	**Latched CRC-6 Error Counter Shadow Register:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This register contains the highest bit of the 9-bit shadow register assigned for holding the CRC-6 error count that occurred in the previous one second interval. This location is updated from CRC8 with a new count at one second intervals on the rising edges of the T1SI signal. Bit 0 is the MSB of the 9-bit count.
1F2 - Ch 1 2F2 - Ch 2 3F2 - Ch 3 4F2 - Ch 4	7-0	CRC7-CRC0	**CRC-6 Error Counter:** This register contains the lower 8 bits of the 9-bit CRC-6 error counter. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is cleared at one second intervals on the rising edges of the T1SI signal. Bit 0 is the LSB of the 9-bit count.
1F3 - Ch 1 2F3 - Ch 2 3F3 - Ch 3 4F3 - Ch 4	7	CRCO	**CRC-6 Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 9-bit CRC-6 counter CRC8-CRC0. This bit sets when the 9-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is also cleared at one second intervals on the rising edges of the T1SI signal.
	6-1	R	**Reserved**: Set to 0.
	0	CRC8	**CRC-6 Error Counter:** This register contains the highest bit of the 9-bit CRC-6 error counter. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is cleared at one second intervals on the rising edges of the T1SI signal. Bit 0 is the MSB of the 9-bit count.

Address	Bit	Symbol	Description
1F4 - Ch 1 2F4 - Ch 2 3F4 - Ch 3 4F4 - Ch 4	7-0	LCV7-LCV0	**Latched Coding Violation Counter Shadow Register:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This register contains the lower 8 bits of the 16-bit shadow register assigned for holding the B8ZS coding violation / excess zeros count that occurred in the previous one second interval. This location is updated from CV7-CV0 with a new count at one second intervals on the rising edges of the T1SI signal. Bit 0 is the LSB of the 16-bit count.
1F5 - Ch 1 2F5 - Ch 2 3F5 - Ch 3 4F5 - Ch 4	7-0	LCV15-LCV8	**Latched Coding Violation Counter Shadow Register:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This register contains the upper 8 bits of the 16-bit shadow register assigned for holding the B8ZS coding violation / excess zeros count that occurred in the previous one second interval. This location is updated from CV15-CV8 with a new count at one second intervals on the rising edges of the T1SI signal. Bit 7 is the MSB of the 16-bit count.
1F6 - Ch 1 2F6 - Ch 2 3F6 - Ch 3 4F6 - Ch 4	7	LCVO	**Latched Coding Violation Counter Overflow Bit:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This bit contains the overflow indication associated with the 16-bit shadow register LCV15-LCV0 assigned for holding the B8ZS coding violation / excess zeros count that occurred in the previous one second interval. This location is updated from CVO at one second intervals on the rising edges of the T1SI signal.
	6-0	R	**Reserved**: Set to 0.
1F7 - Ch 1 2F7 - Ch 2 3F7 - Ch 3 4F7 - Ch 4	7-0	CV7-CV0	**Coding Violation Counter:** This register contains the lower 8 bits of the 16-bit B8ZS coding violation / excess zeros counter. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is cleared at one second intervals on the rising edges of the T1SI signal. Bit 0 is the LSB of the 16-bit count.
1F8 - Ch 1 2F8 - Ch 2 3F8 - Ch 3 4F8 - Ch 4	7-0	CV15-CV8	**Coding Violation Counter:** This register contains the upper 8 bits of the 16-bit B8ZS coding violation / excess zeros counter. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is cleared at one second intervals on the rising edges of the T1SI signal. Bit 7 is the MSB of the 16-bit count.
1F9 - Ch 1 2F9 - Ch 2 3F9 - Ch 3 4F9 - Ch 4	7	CVO	**Coding Violation Counter Overflow Bit:** This bit contains the overflow indication associated with the 16-bit B8ZS coding violation / excess zeros counter CV15-CV0. This bit sets when the 16-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is also cleared at one second intervals on the rising edges of the T1SI signal.
	6-0	R	**Reserved**: These bit locations do not exist.
1FA - Ch 1 2FA - Ch 2 3FA - Ch 3 4FA - Ch 4	7-0	LFBE7-LFBE0	**Latched Framing Bit Error Counter Shadow Register:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This register contains the 8-bit count of the framing bit errors that occurred in the previous one second interval. This location is updated from FBE7-FBE0 with a new count at one second intervals on the rising edges of the T1SI signal.

Address	Bit	Symbol	Description
1FB - Ch 1 2FB - Ch 2 3FB - Ch 3 4FB - Ch 4	7	LFBEO	**Latched Framing Bit Error Counter Overflow Bit:** Enabled when control bit ENPMFM (bit 3) in register 006H is a 1, and a one second signal is applied to the T1SI pin. This bit contains the overflow indication associated with the 8-bit shadow register LFBE7-LFBE0 assigned for holding the framing bit error count that occurred in the previous one second interval. This location is updated from FBEO at one second intervals on the rising edges of the T1SI signal.
	6-0	R	**Reserved**: Set to 0.
1FC - Ch 1 2FC - Ch 2 3FC - Ch 3 4FC - Ch 4	7-0	FBE7-FBE0	**Framing Bit Error Counter:** This register contains the 8-bit framing bit error count. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is cleared at one second intervals on the rising edges of the T1SI signal.
1FD - Ch 1 2FD - Ch 2 3FD - Ch 3 4FD - Ch 4	7	FBEO	**Framing Bit Error Counter Overflow Bit:** This bit contains the overflow indication associated with the 8-bit framing bit error counter FBE7-FBE0. This bit sets when the 8-bit counter overflows. It will remain set until the microprocessor writes a 0 into this location. When control bit ENPMFM (bit 3) in register 006H is a 1, this location is also cleared at one second intervals on the rising edges of the T1SI signal.
	6-0	R	**Reserved**: Set to 0.

Operational Status Registers

The status bits in the following read-only unlatched registers indicate various status information associated with the transmit and receive two-frame slip buffers. The slip buffers are always enabled in the MVIP Mode (CONFIG1 pin is high - pin 43). The slip buffers are optional in the Transmission Mode (CONFIG1 pin is low - pin 43). The transmit slip buffer is enabled when a 1 is written into control bit TSE (bit 4) in register X02H. The receive slip buffer is enabled when a 1 is written into control bit RSE (bit 3) in register X02H.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">114 - Ch 1
214 - Ch 2
314 - Ch 3
414 - Ch 4</td><td>7-6</td><td>TXS1-TSX0</td><td>Transmit Slip Buffer Status: The following table indicates the direction of a transmit slip. A transmit slip indication (unlatched) is provided by status bit TXSLIP (bit 1) set to 1 in register X10H. A latched indication is given by LTXSLIP (bit 1) set to 1 in register X11H.

TXS1 TXSO Buffer Status
0 0 No slips have occurred.
0 1 Slip overflow. One frame dropped.
1 0 Slip underflow. One frame repeated.
1 1 Slip buffer error. Two slips in a row.</td></tr>
<tr><td>5-4</td><td>RXS1-RXS0</td><td>Receive Slip Buffer Status: The following table indicates the direction of a receive slip. A receive slip indication (unlatched) is provided by status bit RXSLIP (bit 0) set to 1 in register X10H. A latched indication is given by LRXSLIP (bit 0) set to 1 in register X11H.

RXS1 RXSO Buffer Status
0 0 No slips have occurred.
0 1 Slip overflow. One frame dropped.
1 0 Slip underflow. One frame repeated.
1 1 Slip buffer error. Two slips in a row.</td></tr>
<tr><td>3</td><td>VTAIS</td><td>VT AIS Received: This status bit is enabled in the Transmission Mode only. A 1 indicates that the (AIS) A-bits on the transmit signaling highway (TSIGLn) are set to 1. The response time and recovery times are immediate.</td></tr>
<tr><td>2</td><td>VTRDI</td><td>VT RDI Received: This status bit is enabled in the Transmission Mode only. A 1 indicates that the Remote Defect Indication (Y) bit on the transmit signaling highway (TSIGLn) is set to 1. The response time and recovery times are immediate.</td></tr>
<tr><td>1-0</td><td>R</td><td>Reserved: Disregard these bits.</td></tr>
</table>

Address	Bit	Symbol	Description
115 - Ch 1 215 - Ch 2 315 - Ch 3 415 - Ch 4	7	RXSF	**Receive Signaling Freeze Indication:** When set to 1, this status bit indicates that the receive signaling bits in the signaling buffer are frozen as a result of a loss of signal or out of frame alarm, or that control bit RXF (bit 5) in register X03H is a 1.
	6	TXSF	**Transmit Signaling Freeze Indication:** When set to 1, this status bit indicates that the transmit signaling bits in the signaling buffer are frozen as a result of receiving an AIS indication on the signaling highway in the Transmission Mode, or that control bit TXF (bit 4) in register X03H is a 1.
	5-3	R	**Reserved**: Disregard these bits.
	2	UP	**Receive Loop-Up Code Indication:** This feature is enabled by control bit ALUP (bit 6) in register X05H being set to a 1 as well as control bit ENPMFM (bit 3) in register 006H being set to a 1. When set to 1 this status bit indicates that a valid loop-up code, as defined by control bits LU6 - LU0 and ULEN1, ULEN0 in registers 014H and 016H, has been detected. The receipt of a valid loop-up code de-asserts the DOWN bit in this register. After receiving the loop-up code for 5 seconds, remote line loopback is entered.
	1	DOWN	**Receive Loop-Down Code Indication:** When set to 1, this status bit indicates that a valid loop-down code, as defined by control bits LD6 - LD0 and DLEN1, DLEN0 in registers 015H and 016H, has been detected. After receiving the loop-down code for 5 seconds, the remote line loopback condition is released. At initialization, this bit is set to 1, and after a loop-up code is received, the UP indication in this register is set and this bit is cleared.
	0	LINT	**General Purpose Input Status Indication:** The status of this bit reflects the state of the external input pin LINTn. The input polarity (i.e., active state) of this pin is determined by control bit LPOL (bit 0) in register X00H. The bit LINT is 1 when the pin is active.

Slip Buffer Pointer Status Registers

The following read-only unlatched register locations provide receive read and write pointer information, and transmit read and write pointer information, from the receive and transmit slip buffers respectively.

Please note that the sixteen register pairs X20H/X21H, X22H/X23H, X24H/X25H and X26H/X27H (where X=1, 2, 3 or 4) are constructed for 16-bit word read operations. Each pair must always be read in two consecutive read operations, with the even-numbered register being read first, e.g., 120H followed by 121H. If either register is read, the other will always be accessed for the next read operation, regardless of the address then selected. If the odd-numbered register is accessed first, data may be corrupted for both read operations. There is no such restriction on write operations.

Address	Bit	Symbol	Description
120 - Ch 1 220 - Ch 2 320 - Ch 3 420 - Ch 4	7-0	TWP7-TWP0	**Transmit Slip Buffer Write Pointer:** Bit 0 is the LSB. The value (between 0 and 192) is the current value of the transmit slip buffer write pointer.

Address	Bit	Symbol	Description
121 - Ch 1 221 - Ch 2 321 - Ch 3 421 - Ch 4	7-0	TRP7-TRP0	**Transmit Slip Buffer Read Pointer:** Bit 0 is the LSB. The value (between 0 and 192) is the current value of the transmit slip buffer read pointer.
122 - Ch 1 222 - Ch 2 322 - Ch 3 422 - Ch 4	7	TWSBS	**Transmit Slip Buffer Write Side:** A 1 indicates that the upper side of the transmit slip buffer is currently being written, A 0 indicates that the lower side of the transmit slip buffer is being written.
	6-5	R	**Reserved**: Disregard these bits.
	4-0	TWPF4-TWPF0	**Transmit Slip Buffer Write Pointer Frame:** The bits in these locations indicate for which frame the transmit slip buffer write pointer is being written. For the SF format the value will range between 0 and 11 and for the ESF format the value will range between 0 and 23. Bit 0 is the LSB.
123 - Ch 1 223 - Ch 2 323 - Ch 3 423 - Ch 4	7	TRSBS	**Transmit Slip Buffer Read Side:** A 1 indicates that the upper side of the transmit slip buffer is currently being read, A 0 indicates that the lower side of the transmit slip buffer is being read.
	6-5	R	**Reserved**: Disregard these bits.
	4-0	TRPF4-TRPF0	**Transmit Slip Buffer Read Pointer Frame:** The bits in these locations indicate for which frame the transmit slip buffer read pointer is being read. For the SF format the value will range between 0 and 11 and for the ESF format the value will range between 0 and 23. Bit 0 is the LSB.
124 - Ch 1 224 - Ch 2 324 - Ch 3 424 - Ch 4	7-0	RWP7-RWP0	**Receive Slip Buffer Write Pointer:** Bit 0 is the LSB. The value (between 0 and 192) is the current value of the receive slip buffer write pointer.
125 - Ch 1 225 - Ch 2 325 - Ch 3 425 - Ch 4	7-0	RRP7-RRP0	**Receive Slip Buffer Read Pointer:** Bit 0 is the LSB. The value (between 0 and 192) is the current value of the receive slip buffer read pointer.
126 - Ch 1 226 - Ch 2 326 - Ch 3 426 - Ch 4	7	RWSBS	**Receive Slip Buffer Write Side:** A 1 indicates that the upper side of the receive slip buffer is currently being written. A 0 indicates that the lower side of the receive slip buffer is being written.
	6-5	R	**Reserved**: Disregard these bits.
	4-0	RWPF4-RWPF0	**Receive Slip Buffer Write Pointer Frame:** The bits in these locations indicate for which frame the receive slip buffer write pointer is being written. For the SF format the value will range between 0 and 11 and for the ESF format the value will range between 0 and 23. Bit 0 is the LSB.
127 - Ch 1 227 - Ch 2 327 - Ch 3 427 - Ch 4	7	RRSBS	**Receive Slip Buffer Read Side:** A 1 indicates that the upper side of the receive slip buffer is currently being read, A 0 indicates that the lower side of the receive slip buffer is being read.
	6-5	R	**Reserved**: Disregard these bits.
	4-0	RRPF4-RRPF0	**Receive Slip Buffer Read Pointer Frame:** The bits in these locations indicate for which frame the receive slip buffer read pointer is being read. For the SF format the value will range between 0 and 11 and for the ESF format the value will range between 0 and 23. Bit 0 is the LSB.

Receive Time Slot Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the receive slip buffer locations for the system highway, and to allow the microprocessor to write in service codes and idle codes.

Address	Bit	Symbol	Description
1E0 - Ch 1 2E0 - Ch 2 3E0 - Ch 3 4E0 - Ch 4	7-0	RDE8-RDE1	**Receive DS0 Channel Enable for DS0 Channels 8-1:** When a bit in this register is set to 1, the corresponding received DS0 channel is written into the slip buffer. The DS0 channel is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding DS0 channel will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive DS0 channel 8. The slip buffers are located in registers X47H-X40H (frame 1) and X5FH-X58H (frame 2).
1E1 - Ch 1 2E1 - Ch 2 3E1 - Ch 3 4E1 - Ch 4	7-0	RDE16-RDE9	**Receive DS0 Channel Enable for DS0 Channels 16-9:** When a bit in this register is set to 1, the corresponding received DS0 channel is written into the slip buffer. The DS0 channel is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding DS0 channel will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive DS0 channel 16. The slip buffers are located in registers X4FH-X48H (frame 1) and X67H-X60H (frame 2).
1E2 - Ch 1 2E2 - Ch 2 3E2 - Ch 3 4E2 - Ch 4	7-0	RDE24-RDE17	**Receive DS0 Channel Enable for DS0 Channels 24-17:** When a bit in this register is set to 1, the corresponding received DS0 channel is written into the slip buffer. The DS0 channel is then read from the slip buffer for the receive data highway. When a bit in this register is written with a 0, the corresponding DS0 channel will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the receive data highway. Bit 7 is assigned to receive DS0 channel 24. The slip buffers are located in registers X57H-X50H (frame 1) and X6FH-X68H (frame 2).

Receive Time Slot Registers

The bits in these read/write registers are the receive time slots from the DS1 frame format (SF or ESF) that are present in the two-frame slip buffer, when enabled. Please note that, on loss of frame alignment, the states present in the slip buffer will be frozen to the states existing prior to the loss of frame alignment.

Address	Bit	Symbol	Description
140-157 - Ch 1 240-257 - Ch 2 340-357 - Ch 3 440-457 - Ch 4	7-0	RDS0(1)- RDS0(24)	**Receive DS0c:** Register locations X40H-X57H represent frame 1 in the two frame slip buffer for the data highway. The register locations for a DS0 channel are enabled when the corresponding receive DS0 channel enable bits (RDE1-RDE24) in registers XE0H, XE1H and XE2H are written with 1. When one or more control bits in registers XE0H-XE2H are written with a 0, the corresponding receive DS0 channel is disabled from being written into the buffer location, and the corresponding values in the two register locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both frame locations in the slip buffer must be written for a DS0 channel (see registers X90H - XA7H below).
158-16F - Ch 1 258-26F - Ch 2 358-36F - Ch 3 458-46F - Ch 4	7-0	RDS0(1)- RDS0(24)	**Receive DS0c:** Register locations X58H-X6FH represent frame 2 in the two frame slip buffer for the data highway. The register locations for a DS0 channel are enabled when the corresponding receive DS0 channel enable bits (RDE1-RDE24) in registers XE0H, XE1H and XE2H are written with 1. When one or more control bits in registers XE0H-XE2H are written with a 0, the corresponding receive DS0 channel is disabled from being written into the buffer location, and the corresponding values in the two register locations are frozen. The microprocessor can now write an idle or service code to the corresponding buffer location. Please note that both frame locations in the slip buffer must be written for a DS0 channel (see registers XA8H - XBFH below).

Transmit Time Slot Control Registers

The control bits in the following read/write registers are used to enable or disable (freeze) the transmit slip buffer locations for receiving input from the system highway, and to allow the microprocessor to write in service codes and idle codes.

Address	Bit	Symbol	Description
1E4 - Ch 1 2E4 - Ch 2 3E4 - Ch 3 4E4 - Ch 4	7-0	TDE8-TDE1	**Transmit DS0 Enable for DS0 Channels 8-1:** When a bit in this register is set to 1, the corresponding transmit DS0 channel from the transmit data highway is written into the slip buffer. The DS0 channel is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding DS0 channel from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit DS0 channel 8. The slip buffers are located in registers X97H-X90H (frame 1) and XAFH-XA8H (frame 2).
1E5 - Ch 1 2E5 - Ch 2 3E5 - Ch 3 4E5 - Ch 4	7-0	TDE16-TDE9	**Transmit DS0 Enable for DS0 Channels 16-9:** When a bit in this register is set to 1, the corresponding transmit DS0 channel from the transmit data highway is written into the slip buffer. The DS0 channel is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding DS0 channel from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit DS0 channel 16. The slip buffers are located in registers X9FH-X98H (frame 1) and XB7H-XB0H (frame 2).
1E6 - Ch 1 2E6 - Ch 2 3E6 - Ch 3 4E6 - Ch 4	7-0	TDE24-TDE17	**Transmit DS0 Enable for DS0 Channels 24-17:** When a bit in this register is set to 1, the corresponding transmit DS0 channel from the transmit data highway is written into the slip buffer. The DS0 channel is then read from the slip buffer for the transmit line. When a bit in this register is written with a 0, the corresponding DS0 channel from the data highway will not be written into the slip buffer. Instead, the microprocessor writes the value of the DS0 channel into the slip buffer and this value will be read from the slip buffer for the transmit line. Bit 7 is assigned to transmit DS0 channel 24. The slip buffers are located in registers XA7H-XA0H (frame 1) and XBFH-XB8H (frame 2).

Transmit Time Slot Registers

The bits in these read/write registers are the transmit time slots from the DS1 frame format that are present in the two-frame slip buffer, when enabled.

Address	Bit	Symbol	Description
190-1A7 - Ch 1 290-2A7 - Ch 2 390-3A7 - Ch 3 490-4A7 - Ch 4	7-0	TDS0(1)- TDS0(24)	**Transmit DS0c:** Register locations X90H-XA7H represent frame 1 in the two-frame slip buffer from the data highway. The register locations for a DS0 channel are enabled when the corresponding transmit DS0 channel enable bits (TDE1 - TDE24) in registers XE4H, XE5H and XE6H are written with 1. When one or more control bits in registers XE4H-XE6H are written with a 0, the corresponding transmit DS0 channel is disabled from being written into the buffer location, and the corresponding values in the register locations are frozen. The microprocessor can now write an idle or service code to the corresponding slip buffer location. Please note that both frame locations in the slip buffer must be written for a DS0 channel.
1A8-1BF - Ch 1 2A8-2BF - Ch 2 3A8-3BF - Ch 3 4A8-4BF - Ch 4	7-0	TDS0(1)- TDS0(24)	**Transmit DS0c:** Register locations XA8H-XBFH represent frame 2 in the two-frame slip buffer from the data highway. The register locations for a DS0 channel are enabled when the corresponding transmit DS0 channel enable bits (TDE1 - TDE24) in registers XE4H, XE5H and XE6H are written with 1. When one or more control bits in registers XE4H-XE6H are written with a 0, the corresponding transmit DS0 channel is disabled from being written into the buffer location, and the corresponding values in the register locations are frozen. The microprocessor can now write an idle or service code to the corresponding slip buffer location. Please note that both frame locations in the slip buffer must be written for a DS0 channel.

Signaling Control Registers

The bits in the following read/write registers control both the receive and transmit signaling buffer locations for DS0 channels 1 through 24.

Address	Bit	Symbol	Description
1E8 - Ch 1 2E8 - Ch 2 3E8 - Ch 3 4E8 - Ch 4	7-0	SE8-SE1	**Signaling Enable for DS0 Channels 8-1:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When SEc is set to 0, or changes from 1 to 0, the signaling states for the corresponding DS0c in the receive signaling buffers are set to 0. The abilities to internally write the signaling bits from the receive line into the receive signaling buffers, or to update the receive signaling buffer from the microprocessor, or to insert robbed bits into the transmit line DS0 channel, are disabled. Bit 7 is the enable bit for DS0 channel 8.
1E9 - Ch 1 2E9 - Ch 2 3E9 - Ch 3 4E9 - Ch 4	7-0	SE16-SE9	**Signaling Enable for DS0 Channels 16-9:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When SEc is set to 0, or changes from 1 to 0, the signaling states for the corresponding DS0c in the receive signaling buffers are set to 0. The abilities to internally write the signaling bits from the receive line into the receive signaling buffers, or to update the receive signaling buffer from the microprocessor, or to insert robbed bits into the transmit line DS0 channel, are disabled. Bit 7 is the enable bit for DS0 channel 16.
1EA - Ch 1 2EA - Ch 2 3EA - Ch 3 4EA - Ch 4	7-0	SE24-SE17	**Signaling Enable for DS0 Channels 24-17:** When a bit in this register is set to 1, the transmit and receive signaling bits for the corresponding telephone channel are enabled. The signaling bits are written into the transmit and receive signaling buffers from the transmit signaling highway and the receive line, and are inserted into the transmit line and receive signaling highway. When SEc is set to 0, or changes from 1 to 0, the signaling states for the corresponding DS0c in the receive signaling buffers are set to 0. The abilities to internally write the signaling bits from the receive line into the receive signaling buffers, or to update the receive signaling buffer from the microprocessor, or to insert robbed bits into the transmit line DS0 channel, are disabled. Bit 7 is the enable bit for DS0 channel 24.

Receive and Transmit Signaling Registers

The following read/write register locations contain the signaling states associated with each of the DS0 channels carried in the SF or ESF frame. When the signaling states for a channel are frozen, the microprocessor can write a new signaling state using the following registers.

Address	Bit	Symbol	Description
180 - Ch 1 280 - Ch 2 380 - Ch 3 480 - Ch 4	7-0	Received Signaling Bits A8-A1	**Receive A8-A1 Signaling Bits:** The signaling bits in this register are the states of the received A1 to A8 bits in the receive signaling buffer. Bit 7 is the A8 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1 (where c is the DS0 channel number, from 1 to 24). When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's A-signaling bits.
181 - Ch 1 281 - Ch 2 381 - Ch 3 481 - Ch 4	7-0	Received Signaling Bits A16-A9	**Receive A16-A9 Signaling Bits:** The signaling bits in this register are the states of the received A9-A16 bits in the receive signaling buffer. Bit 7 is the A16 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's A-signaling bits.
182 - Ch 1 282 - Ch 2 382 - Ch 3 482 - Ch 4	7-0	Received Signaling Bits A24-A17	**Receive A24-A17 Signaling Bits:** The signaling bits in this register are the states of the received A17-A24 bits in the receive signaling buffer. Bit 7 is the A24 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's A-signaling bits.
184 - Ch 1 284 - Ch 2 384 - Ch 3 484 - Ch 4	7-0	Received Signaling Bits B8-B1	**Receive B8-B1 Signaling Bits:** The signaling bits in this register are the states of the received B1 to B8 bits in the receive signaling buffer. Bit 7 is the B8 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's B-signaling bits.
185 - Ch 1 285 - Ch 2 385 - Ch 3 485 - Ch 4	7-0	Received Signaling Bits B16-B9	**Receive B16-B9 Signaling Bits:** The signaling bits in this register are the states of the received B9 to B16 bits in the receive signaling buffer. Bit 7 is the B16 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's B-signaling bits.
186 - Ch 1 286 - Ch 2 386 - Ch 3 486 - Ch 4	7-0	Received Signaling Bits B24-B17	**Receive B24-B17 Signaling Bits:** The signaling bits in this register are the states of the received B17 to B24 bits in the receive signaling buffer. Bit 7 is the B24 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's B-signaling bits.
188 - Ch 1 288 - Ch 2 388 - Ch 3 488 - Ch 4	7-0	Received Signaling Bits C8-C1	**Receive C8-C1 Signaling Bits:** The signaling bits in this register are the states of the received C1 to C8 bits in the receive signaling buffer. Bit 7 is the C8 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's C-signaling bits.

Address	Bit	Symbol	Description
189 - Ch 1 289 - Ch 2 389 - Ch 3 489 - Ch 4	7-0	Received Signaling Bits C16-C9	**Receive C16-C9 Signaling Bits:** The signaling bits in this register are the states of the received C9 to C16 bits in the receive signaling buffer. Bit 7 is the C16 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's C-signaling bits.
18A - Ch 1 28A - Ch 2 38A - Ch 3 48A - Ch 4	7-0	Received Signaling Bits C24-C17	**Receive C24-C17 Signaling Bits:** The signaling bits in this register are the states of the received C17 to C24 bits in the receive signaling buffer. Bit 7 is the C24 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's C-signaling bits.
18C - Ch 1 28C - Ch 2 38C - Ch 3 48C - Ch 4	7-0	Received Signaling Bits D8-D1	**Receive D8-D1 Signaling Bits:** The signaling bits in this register are the states of the received D1 to D8 bits in the receive signaling buffer. Bit 7 is the D8 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's D-signaling bits.
18D - Ch 1 28D - Ch 2 38D - Ch 3 48D - Ch 4	7-0	Received Signaling Bits D16-D9	**Receive D16-D9 Signaling Bits:** The signaling bits in this register are the states of the received D9 to D16 bits in the receive signaling buffer. Bit 7 is the D16 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's D-signaling bits.
18E - Ch 1 28E - Ch 2 38E - Ch 3 48E - Ch 4	7-0	Receive Signaling Bits D24-D17	**Received D24-D17 Signaling Bits:** The signaling bits in this register are the states of the received D17 to D24 in the receive signaling buffer. Bit 7 is the D24 signaling bit value. Please note that a receive signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit SEc is written with a 0, zeros are written into the buffer for the DS0's D-signaling bits.
1D0 - Ch 1 2D0 - Ch 2 3D0 - Ch 3 4D0 - Ch 4	7-0	Transmit Signaling Bits A8-A1	**Transmit A8-A1 Signaling Bits:** The signaling bits in this register are the A1 to A8 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the A8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1.When the corresponding DS0 channel enable bit SEc is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D1 - Ch 1 2D1 - Ch 2 3D1 - Ch 3 4D1 - Ch 4	7-0	Transmit Signaling Bits A16-A9	**Transmit A16-A9 Signaling Bits:** The signaling bits in this register are the A9 to A16 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the A16 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.

Address	Bit	Symbol	Description
1D2 - Ch 1 2D2 - Ch 2 3D2 - Ch 3 4D2 - Ch 4	7-0	Transmit Signaling Bits A24-A17	**Transmit A24-A17 Signaling Bits:** The signaling bits in this register are the A17 to A24 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the A24 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D4 - Ch 1 2D4 - Ch 2 3D4 - Ch 3 4D4 - Ch 4	7-0	Transmit Signaling Bits B8-B1	**Transmit B8-B1 Signaling Bits:** The signaling bits in this register are the B1 to B8 signaling bits written into the signaling buffer from the transmit signaling high-way. Bit 7 is the B8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D5 - Ch 1 2D5 - Ch 2 3D5 - Ch 3 4D5 - Ch 4	7-0	Transmit Signaling Bits B16-B9	**Transmit B16-B9 Signaling Bits:** The signaling bits in this register are the B9 to B16 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the B16 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D6 - Ch 1 2D6 - Ch 2 3D6 - Ch 3 4D6 - Ch 4	7-0	Transmit Signaling Bits B24-B17	**Transmit B24-B17 Signaling Bits:** The signaling bits in this register are the B17 to B24 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the B24 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D8 - Ch 1 2D8 - Ch 2 3D8 - Ch 3 4D8 - Ch 4	7-0	Transmit Signaling Bits C8-C1	**Transmit C8-C1 Signaling Bits:** The signaling bits in this register are the C1 to C8 signaling bits written into the signaling buffer from the transmit signaling high-way. Bit 7 is the C8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1D9 - Ch 1 2D9 - Ch 2 3D9 - Ch 3 4D9 - Ch 4	7-0	Transmit Signaling Bits C16-C9	**Transmit C16-C9 Signaling Bits:** The signaling bits in this register are the C9 to C16 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the C16 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.

Address	Bit	Symbol	Description
1DA - Ch 1 2DA - Ch 2 3DA - Ch 3 4DA - Ch 4	7-0	Transmit Signaling Bits C24-C17	**Transmit C24-C17 Signaling Bits:** The signaling bits in this register are the C17 to C24 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the C24 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1DC - Ch 1 2DC - Ch 2 3DC - Ch 3 4DC - Ch 4	7-0	Transmit Signaling Bits D8-D1	**Transmit D8-D1 Signaling Bits:** The signaling bits in this register are the D1 to D8 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the D8 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1DD - Ch 1 2DD - Ch 2 3DD - Ch 3 4DD - Ch 4	7-0	Transmit Signaling Bits D16-D9	**Transmit D16-D9 Signaling Bits:** The signaling bits in this register are the D9 to D16 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the D16 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.
1DE - Ch 1 2DE - Ch 2 3DE - Ch 3 4DE - Ch 4	7-0	Transmit Signaling Bits D24-D17	**Transmit D24-D17 Signaling Bits:** The signaling bits in this register are the D17 to D24 signaling bits written into the signaling buffer from the transmit signaling highway. Bit 7 is the D24 signaling bit value. Please note that a transmit signaling state is written into the signaling buffer when the corresponding DS0 channel enable bit SEc is written with a 1. When the corresponding DS0 channel enable bit is written with a 0, the ability to insert transmit line robbed bit signaling bits from the transmit signaling buffer for the DS0 is disabled.

Frame Bits

The bits in the following read/write registers are the frame bits from the ESF frame or the SF frame.

Address	Bit	Symbol	Description
130 - Ch 1 230 - Ch 2 330 - Ch 3 430 - Ch 4	7	Fe2/Fs4	**Received Frame Bit:** This bit position is the received Fe2 bit in the ESF frame or the Fs4 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/Ft4	**Received Frame bit:** This bit position is the received FDL bit in the ESF frame or the Ft4 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC2/Fs3	**Received Frame Bit:** This bit position is the received CRC2 bit (in frame 6) in the ESF frame or the Fs3 in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/Ft3	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame or the Ft3 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe1/Fs2	**Received Frame Bit:** This bit position is the received Fe1 bit in the ESF frame or the Fs2 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/Ft2	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame or the Ft2 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC1/Fs1	**Received Frame Bit:** This bit position is the received CRC1 bit (in frame 2) in the ESF frame or the Fs1 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/Ft1	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame or the Ft1 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

Address	Bit	Symbol	Description
131 - Ch 1 231 - Ch 2 331 - Ch 3 431 - Ch 4	7	Fe4/X	**Received Frame Bit:** This bit position is the received Fe4 bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC4/X	**Received Frame Bit:** This bit position is the received CRC4 bit (in frame 14) in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe3/Fs6	**Received Frame Bit:** This bit position is the received Fe3 bit in the ESF frame, or the Fs6 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/Ft6	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft6 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC3/Fs5	**Received Frame Bit:** This bit position is the received CRC3 bit (in frame 10) in the ESF frame, or the Fs5 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/Ft5	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft5 bit in the SF frame, and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

Address	Bit	Symbol	Description
132 - Ch 1 232 - Ch 2 332 - Ch 3 432 - Ch 4	7	Fe6/X	**Received Frame Bit:** This bit position is the received Fe6 bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC6/X	**Received Frame Bit:** This bit position is the received CRC6 bit (in frame 22) in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe5/X	**Received Frame Bit:** This bit position is the received Fe5 bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC5/X	**Received Frame Bit:** This bit position is the received CRC5 bit (in frame 18) in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 1 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

Address	Bit	Symbol	Description
133 - Ch 1 233 - Ch 2 333 - Ch 3 433 - Ch 4	7	Fe2/Fs4	**Received Frame Bit:** This bit position is the received Fe2 bit in the ESF frame, or the Fs4 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/Ft4	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft4 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC2/Fs3	**Received Frame Bit:** This bit position is the received CRC2 bit (in frame 6) in the ESF frame, or the Fs3 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/Ft3	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft3 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe1/Fs2	**Received Frame Bit:** This bit position is the received Fe1 bit in the ESF frame, or the Fs2 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/Ft2	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft2 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC1/Fs1	**Received Frame Bit:** This bit position is the received CRC1 bit (in frame 2) in the ESF frame, or the Fs1 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/Ft1	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft1 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

Address	Bit	Symbol	Description
134 - Ch 1 234 - Ch 2 334 - Ch 3 434 - Ch 4	7	Fe4/X	**Received Frame Bit:** This bit position is the received Fe4 bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC4/X	**Received Frame Bit:** This bit position is the received CRC4 bit (in frame 14) in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe3/Fs6	**Received Frame Bit:** This bit position is the received Fe3 bit in the ESF frame, or the Fs6 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/Ft6	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft6 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC3/Fs5	**Received Frame Bit:** This bit position is the received CRC3 bit (in frame 10) in the ESF frame, or the Fs5 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/Ft5	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, or the Ft5 bit in the SF frame, and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

Address	Bit	Symbol	Description
135 - Ch 1 235 - Ch 2 335 - Ch 3 435 - Ch 4	7	Fe6/X	**Received Frame Bit:** This bit position is the received Fe6 bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	6	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	5	CRC6/X	**Received Frame Bit:** This bit position is the received CRC6 bit (in frame 22) in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	4	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	3	Fe5/X	**Received Frame Bit:** This bit position is the received Fe5 bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	2	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	1	CRC5/X	**Received Frame Bit:** This bit position is the received CRC5 bit (in frame 18) in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.
	0	DI/X	**Received Frame Bit:** This bit position is the received FDL bit in the ESF frame, but is unused in the SF format and represents frame 2 that is written into the slip buffer. The bit is mapped onto the data highway with a delay of one frame and is not subject to a slip.

HDLC Link Control Registers

The bits in the following read/write registers control the transmit and receive HDLC link that is carried in 4 D-bits, using the F- bits in the ESF format.

Address	Bit	Symbol	Description
108 - Ch 1 208 - Ch 2 308 - Ch 3 408 - Ch 4	7	EHR	**Enable HDLC Receiver:** A 1 enables the HDLC receiver. After flag detection and zero bit destuffing the bytes are written into the receive HDLC FIFO. A 0 disables the HDLC link controller, clears the FIFO, and disables the HDLC receive interrupts.
	6	EHT	**Enable HDLC Transmitter:** A 1 enables the HDLC transmitter. The transmitter will send flags when the transmit HDLC FIFO is empty. The bytes are formatted into the message when the FIFO has bytes present. A 0 disables the HDLC link controller, clears the FIFO, and disables the HDLC transmit interrupts.
	5	TAB	**Transmit Abort:** When set to 1, the transmit HDLC link controller will transmit the abort sequence (a zero followed by seven ones) after the next data byte. This is followed by clearing the transmit HDLC FIFO, and sending continuous flags.
	4	EOM	**Transmit End Of Message Flag:** When set to 1, the transmit HDLC FIFO contains the last byte in the message. When the FIFO has emptied, the 16-bit CRC is transmitted, and this followed by an interrupt.
	3	RHIE	**Receiver Half Full Interrupt Enable:** This bit controls the receive HDLC status interrupt entry conditions for status bits RHIS2-RHIS0 (bits 7-5) in register X16H and event bits ERHIS2-ERHIS0 (bits 7-5) in register X0EH. When set to 1, the receive HDLC link controller generates an interrupt when the receive HDLC FIFO is half full, or at the end of the message. When set to 0, the HDLC link controller generates an interrupt request only at the end of the message or when the FIFO has overflowed.
	2	THIE	**Transmit Half Full Interrupt Enable:** This bit controls the transmit HDLC status interrupt entry condition for status bit THIS (bit 4) in register X16H and event bit ETHIS (bit 4) in register X0EH. When set to 1, the transmit HDLC link controller generates an interrupt when the transmit HDLC FIFO is half full, or at the end of the message. When set to 0, the HDLC link controller generates an interrupt request only at the end of the message or when the FIFO has underflowed.
	1	EBRI	**Enable Bit Code Receiver Interrupt:** When the ESF format is selected and this bit is set to 1, the bit code receive interrupt is enabled.
	0	EBT	**Enable Bit Code Transmitter:** When the ESF format is selected and this bit is set to 1, the bit code transmitter is enabled. The bit code defined in register X0BH is formatted into a 16-bit message that is transmitted continuously on the HDLC Link as 1111111100000000.

HDLC Link Transmit and Receive Data Registers

Two registers are used for writing the transmit bytes into the 16-byte transmit FIFO, and for reading the receive bytes from the receive FIFO, for the HDLC message. Register X18H indicates the number of bytes in the receive FIFO. All registers are read/write.

Address	Bit	Symbol	Description
10A - Ch 1 20A - Ch 2 30A - Ch 3 40A - Ch 4	7-0	THD7-THD0	**HDLC Transmit Data:** The byte written to this location is written to the transmit FIFO. Bit 0 corresponds to the first bit transmitted in the HDLC message byte.
10B - Ch 1 20B - Ch 2 30B - Ch 3 40B - Ch 4	7-6	R	**Reserved:** These bit locations do not exist.
	5-0	TBCD5-TBCD0	**Transmit Bit Code Data:** The value written into this register will be formatted into a 16-bit message. The 16-bit message is transmitted continuously when control bit EBT is written with a 1 (bit 0 in register X08H) TBCD5 is the MSB and the first bit in the code word transmitted (i.e., the six X bits in the 16-bit sequence 111111110XXXXXX0).
117 - Ch 1 217 - Ch 2 317 - Ch 3 417 - Ch 4	7-0	RHD7-RHD0	**HDLC Receive Data:** A read cycle transfers one byte from the receive FIFO into this location. Bit 0 corresponds to the first bit received in the HDLC message byte.
118 - Ch 1 218 - Ch 2 318 - Ch 3 418 - Ch 4	7-5	R	**Reserved:** Disregard these bits.
	4-0	C4-C0	**HDLC Receive FIFO Depth**: This register indicates the number of data bytes currently present in the HDLC receive FIFO. The value read is in binary. Bit 0 is the LSB value. For example, the value 00000 indicates that the FIFO is empty, and the value 01111 indicates that there are 15 bytes present in the receive FIFO.
119 - Ch 1 219 - Ch 2 319 - Ch 3 419 - Ch 4	7-6	R	**Reserved:** Disregard these bits.
	5-0	RBCD5-RBCD0	**Receive Bit Code Data**: These bits are set to the bit code when a new bit code is received 8 out of 10 consecutive times. Otherwise, these six bits are set to all ones. RBCD5 is the MSB.

HDLC Link Status Registers

These registers are all read/write. The status bits in the X0E registers represent the latched status and interrupt request indications generated by the receive and transmit HDLC link controllers and the FIFOs. The latched event bits are a result of a receive or transmit status indication or interrupt request in the HDLC Link Status register X16H. The bits latch on either the positive transitions, the negative transitions, or both positive and negative transitions of the current status or interrupt request event bits as defined by the RISE/FALL control bits (bits 6 and 5) in the Global Configuration Register 006H. A latched bit causes a hardware interrupt indication when the corresponding mask bit in the HDLC Link Mask Register X0FH is written with a 0. The status bits in register X16H represent the current (unlatched) status and interrupt request indications generated by the receive and transmit HDLC link controllers and FIFOs.

Address	Bit	Symbol	Description
10E - Ch 1 20E - Ch 2 30E - Ch 3 40E - Ch 4	7-5	ERHIS2- ERHIS0	**Latched Receive HDLC Interrupt Events:** These latched status bits will change to indicate a corresponding change in RHIS (2-0), bits 7-5 of register X16, except when RHIS (2-0) changes to all zeros when these latched status bits will retain the previously latched value. These bits are cleared by writing a 0 to any bit position that is set. A hardware interrupt is generated when any of these bits latches and the corresponding mask bit position in register X0FH is written with a 0.
	4	ETHIS	**Latched Transmit HDLC Interrupt Event:** The latched bit in this location corresponds to a transmit HDLC interrupt status indication in bit 4 in register X16H. This bit is cleared by writing a 0 to it. A hardware interrupt is generated when this bit latches and the corresponding mask bit position in register X0FH is written with a 0.
	3-2	ERXFS1- ERXFS0	**Latched Receive HDLC FIFO Status Events:** These latched status bits will change to indicate a corresponding change in RXFS (1-0), bits 3-2 of register X16, except when RXFS (1-0) changes to all zeros when these latched status bits will retain the previously latched value. These bits are cleared by writing a 0 to any bit position that is set. If not masked by the corresponding mask bit position in register X0FH, a hardware interrupt is generated when any of these bits latches.
	1-0	ETXFS1- ETXFS0	**Latched Transmit HDLC FIFO Status Events:** These latched status bits will change to indicate a corresponding change in TXFS (1-0), bits 1-0 of register X16, except when TXFS (1-0) changes to all zeros when these latched status bits will retain the previously latched value. These bits are cleared by writing a 0 to any bit position that is set. A hardware interrupt is generated when this bit latches and the corresponding mask bit position in register X0FH is written with a 0.

Address	Bit	Symbol	Description
10F - Ch 1 20F - Ch 2 30F - Ch 3 40F - Ch 4	7-5	MRHIS2-MRHIS0	**Receive HDLC Interrupt Mask:** When one or more bits are set to a 1, the latched receive HDLC interrupt event indications in corresponding bits 7-5 in register X0EH are masked from causing a hardware interrupt. For example, if 001 is written into this location, a start of message indication is masked from causing a hardware interrupt (see RHIS2-RHIS0 below).
	4	MTHIS	**Transmit HDLC Interrupt Mask:** When set to 1, the latched transmit HDLC interrupt event indication corresponding to bit 4 in register X0EH is masked from causing a hardware interrupt.
	3-2	MRXFS1-MRXFS0	**Receive HDLC FIFO Status Interrupt Mask:** When one or more bits are set to a 1, a latched receive HDLC FIFO event indication in corresponding bits 3-2 in register X0EH is masked from causing a hardware interrupt. For example, if a 01 is written into this location, a half full or more than half full indication is masked from causing a hardware interrupt (see RXFS1 - RXFS0 below).
	1-0	MTXFS1-MTXFS0	**Transmit HDLC FIFO Status Interrupt Mask:** When one or more bits are set to a 1, a latched transmit HDLC FIFO event that has taken place in corresponding bits 1-0 in register X0EH is masked from causing a hardware interrupt. For example, if a 01 is written into this location, a half full or less than half full indication is masked from causing a hardware interrupt (see TXFS1 - TXFS0 below).

Address	Bit	Symbol	Description
116 - Ch 1 216 - Ch 2 316 - Ch 3 416 - Ch 4	7-5	RHIS2-RHIS0	**Receive HDLC Interrupt Status:** The following table lists the various interrupt status indications for the receive HDLC message. See control bit RHIE (bit 3) in register X08H. RHIS2 RHIS1 RHIS0 RHIE Condition 0 0 0 X Idle Condition. 0 0 1 X Start of message indication. 0 1 0 0 Valid message received (CRC checked OK, message is 16 bytes or less), or FIFO overflow. 0 1 0 1 FIFO needs servicing (short message, receive half full control bit set) or valid message received. 0 1 1 X Message received with CRC error. 1 0 X X Abort message detected. 1 1 X X Bit code received (FIFO automatically cleared). X represents either value may be indicated.
	4	THIS	**Transmit HDLC Interrupt Status:** A 1 indicates that the transmit FIFO needs servicing, either because the message is completed, or because the FIFO is equal to or less than half full. See control bit THIE (bit 2) in register X08H.
	3-2	RXFS1-RXFS0	**Receive FIFO Status:** The following table lists the various receive FIFO status indications for the receive HDLC message. RXFS1 RXFS0 Condition 0 0 Normal. FIFO less than half full. 0 1 FIFO equal to or more than half full. 1 0 FIFO full. 1 1 FIFO overflowed.
	1-0	TXFS1-TXFS0	**Transmit FIFO Status:** The following table lists the various transmit FIFO status indications for the transmit HDLC message. TXFS1 TXFS0 Condition 0 0 Normal. FIFO equal to or greater than half full. 0 1 FIFO less than half full. 1 0 FIFO overwritten (attempt to write to a full FIFO). 1 1 FIFO underflowed (attempt to read an empty FIFO).

DS0 Loopback Control Registers

These registers are all read/write. The control bits in the three registers are enabled when control bit ENDS0LB (bit 4 in register 0FFH) is written with a 1. Writing a 1 to any one or more control bits in the following registers causes the corresponding DS0 channel(s) to be looped back from the receive path to the transmit path. The LBD24-LBD1 control bits are reset to 0 upon a hardware reset.

Address	Bit	Symbol	Description
11C - Ch 1 21C - Ch 2 31C - Ch 3 41C - Ch 4	7-0	LBD8-LBD1	**Loopback DS0 Channels 8-1:** A 1 in one or more control bits causes the corresponding DS0 channel(s) to be looped back.
11D - Ch 1 21D - Ch 2 31D - Ch 3 41D - Ch 4	7-0	LBD16-LBD9	**Loopback DS0 Channels 16-9:** A 1 in one or more control bits causes the corresponding DS0 channel(s) to be looped back.
11E - Ch 1 21E - Ch 2 31E - Ch 3 41E - Ch 4	7-0	LBD24-LBD17	**Loopback DS0 Channels 24-17:** A 1 in one or more control bits causes the corresponding DS0 channel(s) to be looped back.

APPLICATION DIAGRAM

The diagram in Figure 45 illustrates the use of the QT1F-*Plus* device to provide framing and DS0 access for a variety of DS1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided. Note that these applications require operating the QT1F-*Plus* at V_{DD} = +5.0 volts to comply with the +5.0 volt parts connected to the QT1F-*Plus*.

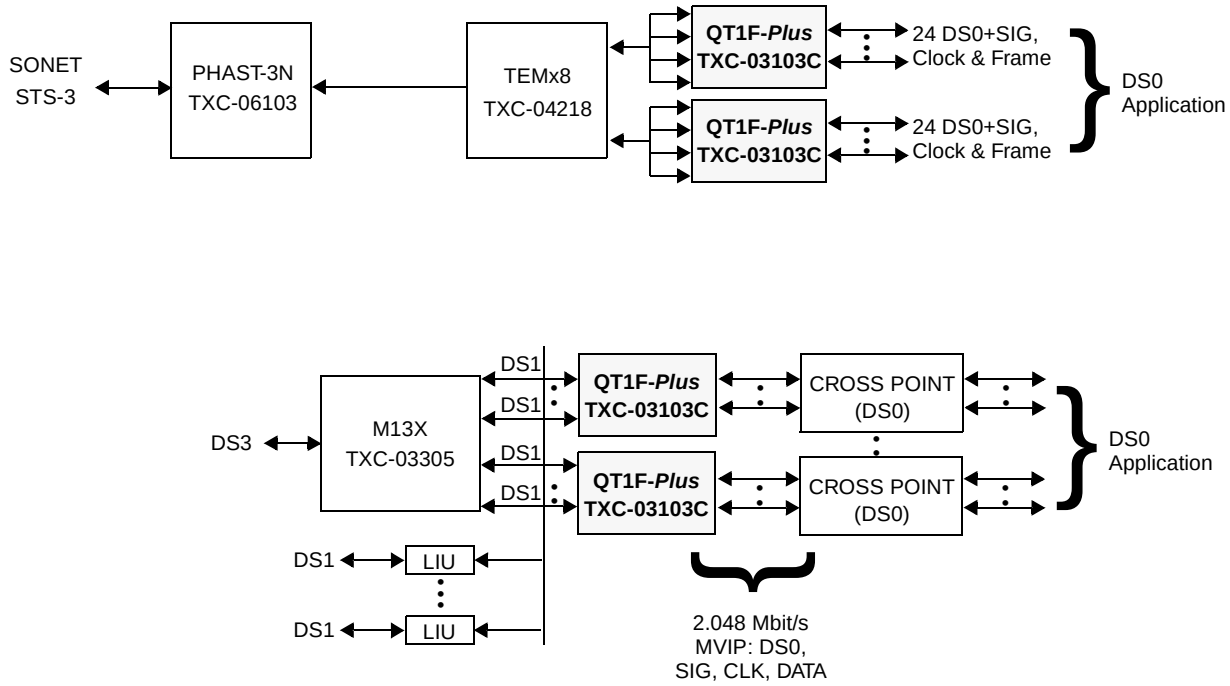


Figure 45. QT1F-*Plus* TXC-03103C Application

PACKAGE INFORMATION

The QT1F-*Plus* device is packaged in a 128-pin low profile plastic quad flat package suitable for surface mounting, as illustrated in Figure 46a.

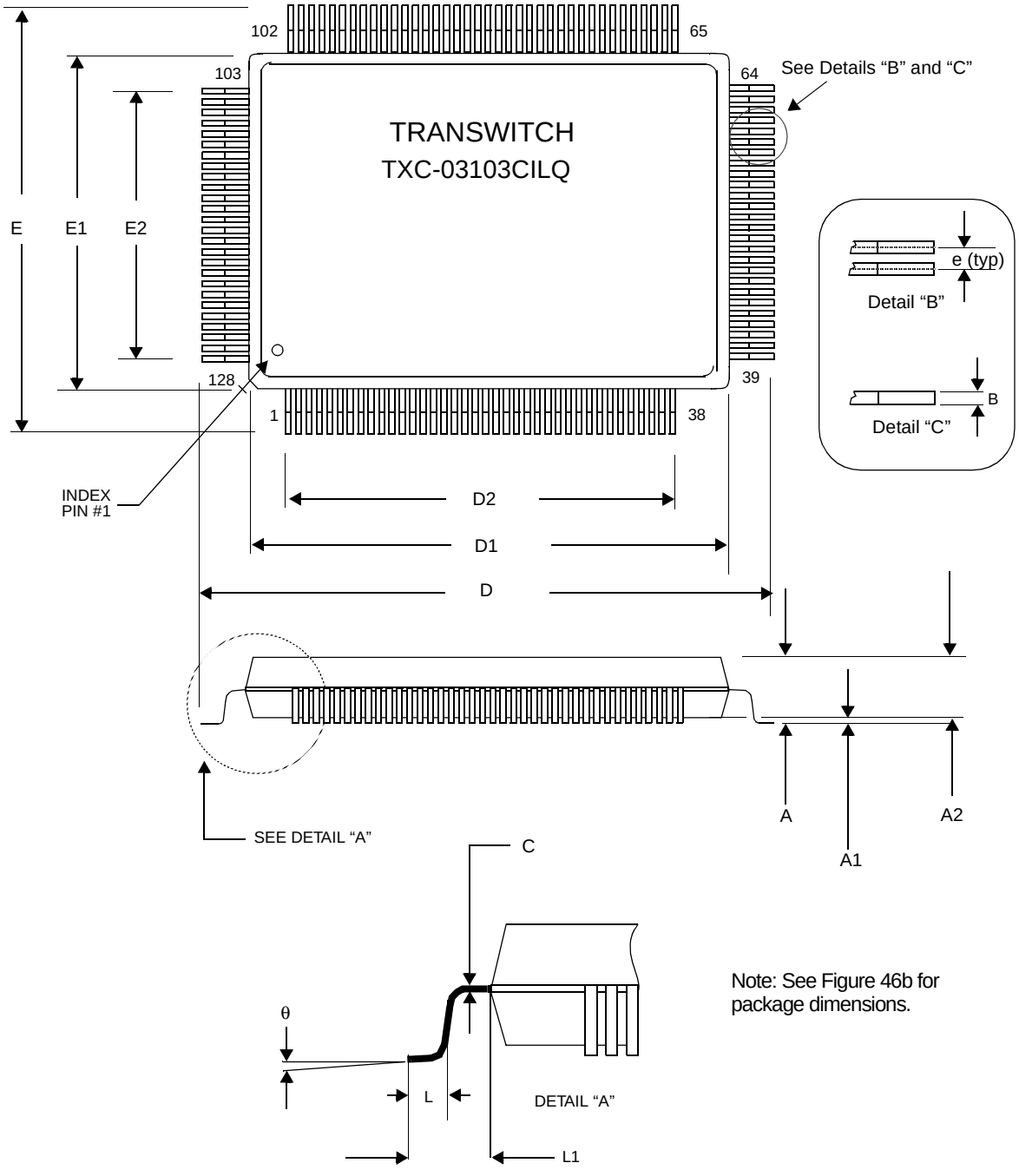


Figure 46a. QT1F-*Plus* TXC-03103C 128-Pin Package Diagram

Symbol	Minimum	Nominal	Maximum	Note
				1
A	-	-	1.60	
A1	0.05	-	0.15	
A2	1.35	1.40	1.45	
B	0.18	0.22	0.27	2, 3
C	0.10	-	0.20	2, 3
D	21.90	22.00	22.10	
D1	19.90	20.00	20.10	4
D2	-	18.50 REF	-	5
e	0.50 BCS			
E	15.90	16.00	16.10	
E1	13.90	14.00	14.10	4
E2	-	12.50 REF	-	5
L	0.45	0.60	0.75	
L1	1.00 REF			
q	0 °	-	7 °	

Notes:

1. Linear dimension: millimeter. Angular dimension: degree.
2. Dimensions B and C do not include dambar protrusion. Dambar cannot be located on the lower radius or the foot.
3. Plating thickness included. Plating thickness to be 0.005 mm minimum, 0.020 mm maximum.
4. Dimensions D1 and E1 do not include mold protrusion or mold mismatch.
5. Measured between centers of outer pins.

Figure 46b. QT1F-*Plus* TXC-03103C 128-Pin Package Dimensions

ORDERING INFORMATION

Part Number: TXC-03103CILQ 128-pin Low Profile Plastic Quad Flat Package

RELATED PRODUCTS

TXC-03305, M13X Device (DS3/DS1 Mux/Demux). Has built-in PMDL controller for a DS3 Data Link when in C-bit Parity Mode, integrated DS3/DS2/DS1 Demultiplexing De-Jitter Buffers as additional features when compared to the M13E. Can also operate in the M13E mode, when none of the additional features will be available.

TXC-04218, TEMx8 Device (8 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 8 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04222, TEMx28® Device (28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04251, QT1M Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-05427, COBRA Device (Constant Bit Rate ATM Adaptation Layer 1). Provides ATM AAL1 Structured and Unstructured service for four T1, E1 or n x 64k constant bit rate interfaces.

TXC-05870, PacketTrunk-4 Device (TDMoIP/MPLS Gateway). The PacketTrunk-4 device is a single-chip solution for implementing cost-effective, standards-compliant TDMoIP/MPLS interfaces and systems. PacketTrunk-4 provides all of the necessary interface, encapsulation, clock recovery, and QoS functionality for enabling transport of unstructured or structured TDM signals over a packet-switched network (PSN).

TXC-06103, PHAST®-3N Device (SONET STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator with Telecom Bus interface). This device provides the combined functionality of the SOT-3 and SYN155C VLSI devices, with a Telecom Bus Interface.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007
Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated QT1F-*Plus* TXC-03103C Data Sheet that have significant differences relative to the previous and now superseded QT1F-*Plus* TXC-03103C Data Sheet:

Updated QT1F-*Plus* TXC-03103C Data Sheet: *PRELIMINARY* Ed. 3, October 2004

Previous QT1F-*Plus* TXC-03103C Data Sheet: *PRELIMINARY* Ed. 2, March 2001

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Added Patent No. 6,456,595. Updated trademark information.
20	Changed Conditions for Parameter Moisture Exposure level and changed Note 4 for "Absolute Maximum Ratings and Environmental Limitations" table.
102	Changed last sentence of Description for Symbol BDCST.
148	Updated "Application Diagram" section.
151	Updated "Related Products" section.
152	Updated "Standards Documentation Sources" section.
154	Changed "List of Data Sheet Changes" Changes section.

- NOTES -


TRANSWITCH
Engines for Global Connectivity