L4M Device
Level 4 Mapper
TXC-03456

DATA SHEET

FEATURES

- Maps an asynchronous 139.264 Mbit/s tributary into an AU-4/VC-4 STS-3c/SPE.
- Nibble or byte 139.264 Mbit/s line interface
  - G.751 receive and transmit performance monitoring (frame alignment, distant alarm indication)
- SDH/SONET bus access
  - Drop/add byte buses
  - Optional drop bus AU-4 pointer tracking with framing delay compensation
- SDH/SONET timing mode
  - Drop bus timing
  - Add bus timing
  - External timing with framing delay compensation
- Microprocessor access
  - Intel I/O with separate address/data buses
  - Motorola I/O with separate address/data buses
  - Motorola I/O with multiplexed bus
  - Interrupt capability with individual mask bits
- POH byte processing
- Enhanced desynchronizer access
- Testing features
  - Line loopback
  - SDH/SONET loopback
  - 2^{23}-1 test generator and analyzer
- Boundary scan capability (IEEE 1149.1)
- 144-pin plastic quad flat package

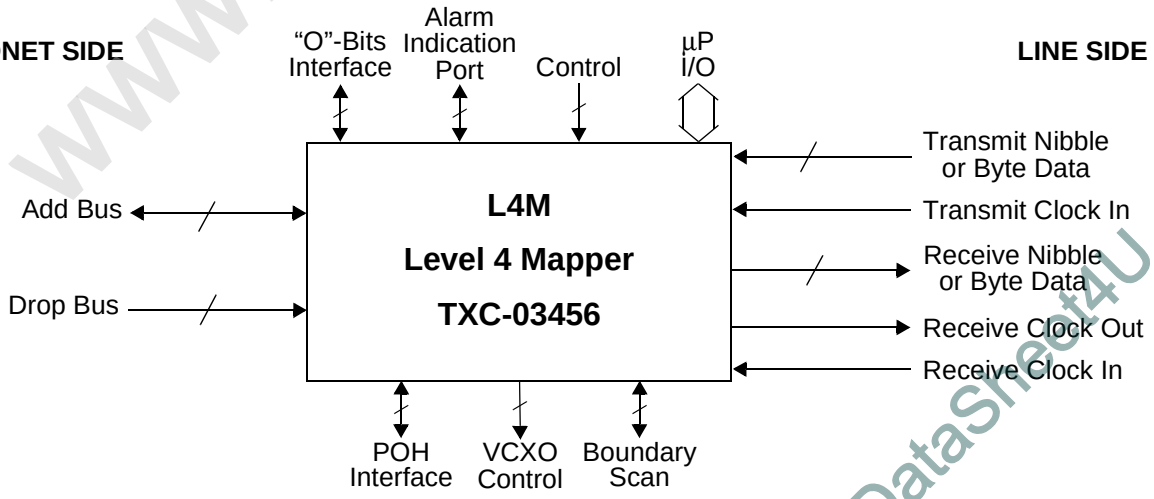
DESCRIPTION

The L4M device maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SDH/SONET signal is transmitted via the add bus with timing derived from the drop bus, add bus, or external clock source. The L4M can compensate for up to a frame offset when using external timing and an external C1 pulse. An option is provided to generate TOH bytes, such as the A1 and A2 framing bytes, a C1 byte, and the H1 and H2 pointer bytes only in drop bus and external timing modes. The VC-4/SPE can be fixed to a known J1 reference when add bus timing is selected, or it can be positioned with a pointer value of 0 or 522 when drop bus or external timing is selected.

In the drop direction, an optional pointer tracking machine is provided. In this mode, the L4M can compensate for up to a frame in offset. External access is provided for the POH bytes, in addition to internal processing capability. Serial access is provided for the overhead communications bits in the format. An alarm indication port is provided for ring configuration applications.

APPLICATIONS

- Add/drop multiplexers
- Digital cross-connect systems
- Broadband switching systems
- Transmission equipment



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BLOCK DIAGRAM

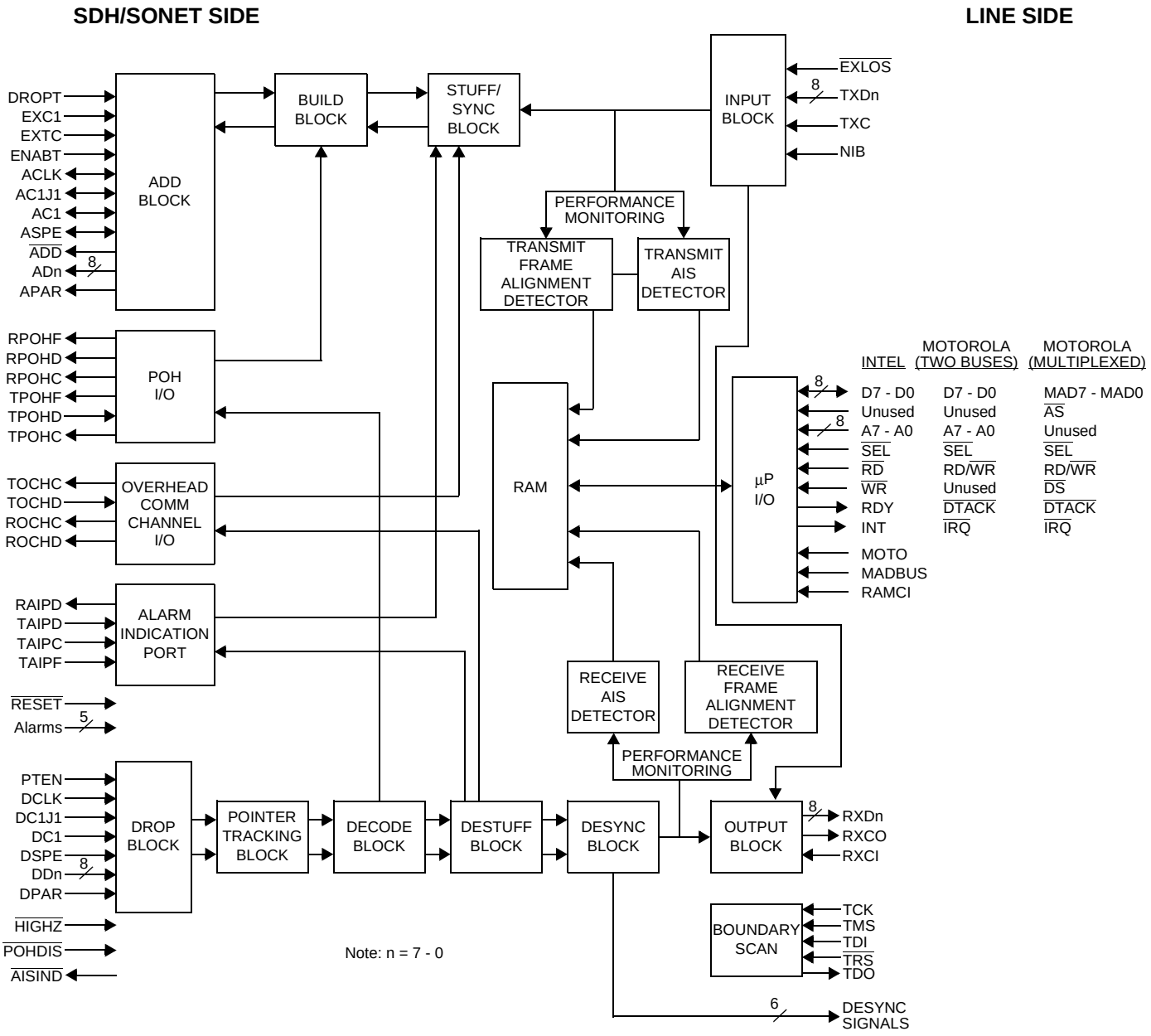


Figure 1. L4M TXC-03456 Block Diagram

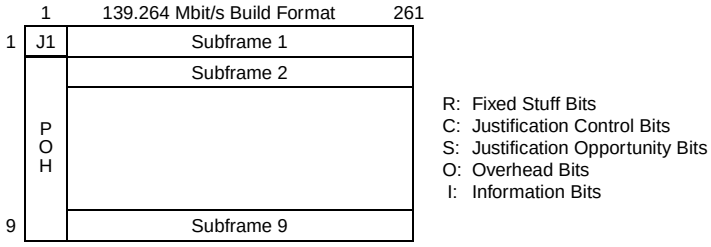
BLOCK DIAGRAM DESCRIPTION

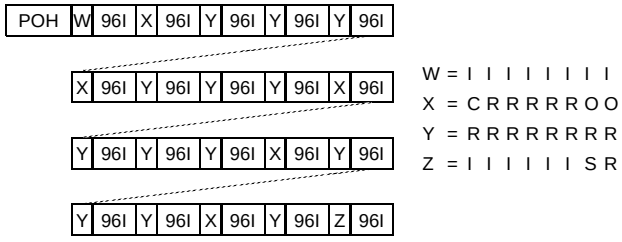
A simplified block diagram of the L4M device is shown in Figure 1. A byte-wide or nibble-wide 139.264 Mbit/s signal (TXDn) is connected to the Input Block. The nibble interface is selected by placing a high on the lead designated as NIB. Data is clocked into the L4M on positive transitions of the clock signal TXC. A control bit is provided which enables data to be clocked into the L4M on negative transitions of the clock. The L4M Input Block also terminates an external loss of signal ($\overline{\text{EXLOS}}$) indication. A low placed on this lead indicates that an external line interface device, such as a CMI interface device, has detected a loss of signal. This signal is reported as an alarm within the L4M for the microprocessor, and can generate an interrupt and a 140 Mbit/s AIS when enabled.

The 140 Mbit/s transmit line signal is monitored by the two Transmit Performance Monitoring Blocks for ITU-T G.751 frame alignment and a Distant Alarm Status. A Distant Alarm is defined as a 1 in bit 13 of the G.751 frame format. This alarm can generate an interrupt indication when enabled. When frame alignment is established, framing errors are counted in a 16-bit performance counter. The 140 Mbit/s line signal is also monitored for an Alarm Indication Signal (AIS). The AIS detection circuit can be enabled to work in conjunction with the frame alignment circuit. An AIS condition is reported as an alarm, and can generate an interrupt when enabled.

The Stuff/Sync Block contains a FIFO and is controlled by write timing from the Input Block, and by read timing from the Build Block. The FIFO accommodates input and timing jitter as specified in ITU-T Recommendation G.823. The FIFO is protected against overflow and underflow conditions by reporting a FIFO error alarm, and will automatically recenter when a FIFO underflow or overflow alarm has been detected. The reset is held for approximately one frame before the FIFO is released for operation. Upon power-up, or on applying a reset, the transmit FIFO is also recentered. The stuffing algorithm uses one set of five control bits (C-bits) with one stuff opportunity bit (S-bit) per subframe (nine subframes) for frequency justification.

The Build Block, with timing signals exchanged with the Stuff/Sync Block, constructs the VC-4 format as illustrated below.





The L4M can build the 261 column by 9 row VC-4 format without or with path overhead bytes, and "O"-bits, depending on the features selected. The addition of POH bytes to the VC-4 format is disabled by applying a low to the pin designated $\overline{\text{POHDIS}}$ (also applying a low to $\overline{\text{POHDIS}}$ disables receive VC-4 POH processing). The starting position of the VC-4 J1 bytes can be synchronized to the add bus J1 pulse, when add bus timing is selected, or have a starting location of 0 or 522, when drop bus or the external timing modes are selected.

The L4M can also generate an unequipped or supervisory unequipped VC-4. An unequipped VC-4 is defined as all zeros for the POH and payload bytes, while a supervisory unequipped VC-4 is defined as having valid POH bytes, but the payload bytes equal to zero. The Build Block is also responsible for multiplexing individual

POH bytes from the Path Overhead interface, or from RAM locations written to by the microprocessor, into the add bus data stream. The RDI state and FEBE count may be provided from a mate L4M for path-protected ring configurations.

The Add Block uses drop bus timing signals, add bus timing signals, or external timing signals for outputting the SDH/STS-3c data signal and parity to the add bus. A feature is also provided that generates the A1, A2, C1 and H1/H2 Transport (SDH Section) Overhead bytes, depending upon the timing mode selected. The C1 byte value may be a fixed or a microprocessor-written value. The SS-bits in the transmitted pointer may be fixed or written by the microprocessor. Unused Transport Overhead bytes can be selected to be three-stated or forced to zero. In the add bus timing mode, the clock and C1J1 signals are monitored for operation. In the external timing mode, an option is provided which can compensate up to a frame for the position of the C1 byte framing pulse (EXC1).

The Add Block interface for the add bus timing mode consists of an input clock (ACLK), input C1 and J1 indicator (AC1J1), a separate C1 input (AC1) when enabled, an input SPE indicator (ASPE), output byte data (AD7-AD0), output parity indication (APAR), and an output add data to bus indicator ($\overline{\text{ADD}}$). When the L4M is configured to operate in the external timing mode, the add bus signals consist of: external reference input clock (EXTC) and framing signal (EXC1) (optional), an output clock (ACLK), output C1 and J1 indicator (AC1J1), an output SPE indicator (ASPE), output byte data (AD7-AD0), output parity indication (APAR), and an output add data to bus indicator ($\overline{\text{ADD}}$). When the L4M is configured to operate in the drop bus timing mode, the add bus signals consist of: an output clock (ACLK), output C1 and J1 indicator (AC1J1), an output SPE indicator (ASPE), output byte data (AD7-AD0), output parity indication (APAR), and an output add data to bus indicator ($\overline{\text{ADD}}$). Odd parity may be calculated over all add bus signals (except the add indicator), or data only.

The Drop Block terminates the drop bus signals. The drop bus signals consists of an input clock (DCLK), input C1 and J1 indicator (DC1J1), an input SPE indicator (DSPE), input byte data (DD7-DD0), input parity indication (DPAR), and an optional framing pulse (DC1). When the pointer tracking machine feature is enabled, the J1 signal in the C1J1 signal must not be present. Odd parity may be checked over all of the drop bus signals, or for the data byte only. When the pointer tracking machine is enabled, the relative position of C1 can be compensated up to one frame.

The Pointer Tracking Block is enabled by placing a high on the lead designated as PTEN. The pointer tracking machine meets the pointer tracking requirements specified in ETSI 1015. The Pointer Tracking Block determines the starting location of the J1 byte in the VC-4 format. The S-bit transition check in the H1 pointer byte may be disabled in the Pointer Tracking Block. When enabled, the S-bit check can be a fixed value or a value written by the microprocessor. In addition, the AIS to LOP transition can be disabled to have the Pointer Tracking state machine conform to Bellcore standards. The Pointer Tracking Block monitors the pointer bytes for a path AIS and LOP alarm. Positive, negative and NDF occurrences are counted in 8-bit performance counters.

Having established the starting location of the VC-4, the Decode Block performs Path Overhead byte processing. The POH bytes are written into RAM locations for a microprocessor read cycle in addition to being provided at a POH interface for external access. Capability is also provided in the L4M for performing the path trace message comparison for the J1 byte. B3 BIP-8 parity errors and the input FEBE count in the G1 byte are counted as bit or block errors. The status of the RDI bit is also checked, and an alarm indication provided. The FEBE count is also provided, along with an RDI indication (as a result of local alarms) to an Alarm Indication Port for path-protected ring operation. A bit stuffing AIS feature is also provided in addition to using an external AIS clock to generate line AIS as a result of receive alarms.

The Desynchronizer Block is based on a proprietary TranSwitch design. The Desynchronizer Block removes the effect on the output signal of systemic jitter due to signal mapping and pointer movements, and consists of two FIFOs. The FIFOs are monitored for overflow and underflow alarms, and reset automatically when an alarm is detected. A 15-bit pointer leak register is provided for a microprocessor-written value. The following six desynchronizer signals are provided: Positive and negative phase detector outputs (CTRL and $\overline{\text{CTRL}}$), a stuff indicator (STUFF) that provides the status of the stuff (justification) on a per-subframe basis, positive and negative justification indicator bits (PJ and NJ), and a pointer leak counter equal to zero indication (PLEQ0). In

addition, the desynchronizer pointer offset counter (9 bits plus sign value) is provided in the memory map for a microprocessor read, if required.

The output of the Desynchronizer Block is connected to the L4M Output Block, Receive Frame Alignment Detector Block and Receive AIS Detector Block. The 140 Mbit/s receive line signal is monitored by the Receive Frame Alignment Detector Block for ITU-T G.751 frame alignment and the Distant Alarm Status. A Distant alarm is defined as a 1 in bit 13 of the G.751 frame format. This alarm can generate an interrupt indication when enabled. When frame alignment is established, framing errors are counted in a 16-bit performance counter.

The 140 Mbit/s line signal is also monitored for an Alarm Indication Signal (AIS). The AIS detection circuit can be enabled to work in conjunction with the frame alignment circuit. An AIS condition is reported as an alarm, and can generate an interrupt when enabled. The Receive Frame Alignment Detector and Receive AIS Detector Blocks are disabled when the bit stuffing approach for generating 140 Mbit/s AIS is enabled and when the L4M generates a receive line AIS. AIS using a bit stuffing approach is implemented in the Decode Block prior to the Desynchronizer Block.

A byte-wide or nibble-wide 139.264 Mbit/s signal (RXDn) is provided as an output from the Output Block. A nibble interface is selected by placing a high on the lead designated as NIB. Data is normally clocked out of the L4M on negative transitions of the clock signal RXCO. A control bit is provided which enables data to be clocked out of the L4M on positive transitions of the clock.

External access to the Path Overhead bytes is provided by the POH I/O Block. The nine receive POH bytes present in the serial data channel (RPOHD) are clocked out on negative transitions of the gapped clock (RPOHC). A framing pulse (RPOHF), one clock cycle wide, identifies the starting location of the POH bytes, with bit 1 in the J1 byte. In the transmit direction, a gapped clock (TPOHC), and framing pulse (TPOHF) are provided. Serial data containing the POH bytes is clocked into the L4M on positive transitions of the clock. The B3 byte is present in the serial bit stream, but it is ignored by the L4M, and is recalculated. The framing pulse is one clock cycle wide and identifies the starting location of the POH bytes, with bit 1 in the J1 byte.

An external AIS input is provided for generating a received 140 Mbit/s AIS and an RDI indication, if the POH bytes are processed externally.

The Overhead Communications Channel I/O block provides an asynchronous interface for the 90 "O"-bits found in the SDH/SONET format. Serial data (ROCHD) which contains the "O"-bits, is clocked out of the L4M on negative transitions of the gapped clock (ROCHC). The received "O"-bits are not synchronized with the starting location of the frame. In the transmit direction, the "O"-bits (TOCHD) are clocked into the L4M by the gapped output clock (TOCHC).

The Alarm Indication Port data output signal (RAIPD), consisting of the FEBE count and RDI indication, is clocked out of the L4M on negative transitions of the receive POH clock (RPOHC). The serial data consists of nine bytes each frame. The first four bits correspond to the FEBE count, which has been derived from the B3 BIP-8 parity check. The next bit, bit 5, corresponds to the RDI indication. Bits 6 and 7 are set to 0, while bit 8 is set to a 1. The received POH framing pulse (RPOHF) identifies the starting location of bit 1 in the first byte. In the transmit direction, the received serial data, framing pulse, and clock from the mate L4M become the data input (TAIPD), framing pulse input (TAIPF), and clock input (TAIPC). When the ring mode is selected, the mate L4M FEBE count and RDI indication are transmitted in the G1 byte.

An upstream AIS indication may be inputted into the L4M using the E1 byte in the Transport (Section) Overhead bytes, or the external ISTAT, PAIS, and STAI pins. The upstream AIS indication can generate a 140 Mbit/s AIS, and a transmit RDI indication.

The L4M supports three types of microprocessor interfaces: Intel microprocessor with separate address and data buses, Motorola microprocessor with separate address and data buses, and a Motorola microprocessor with a multiplexed address/data bus interface.

The Boundary Scan block provides a mechanism for external access to the input and output pins of the device, so that they may be observed and tested. The structure and operation of this block are described in the Operation section.

PIN DIAGRAM

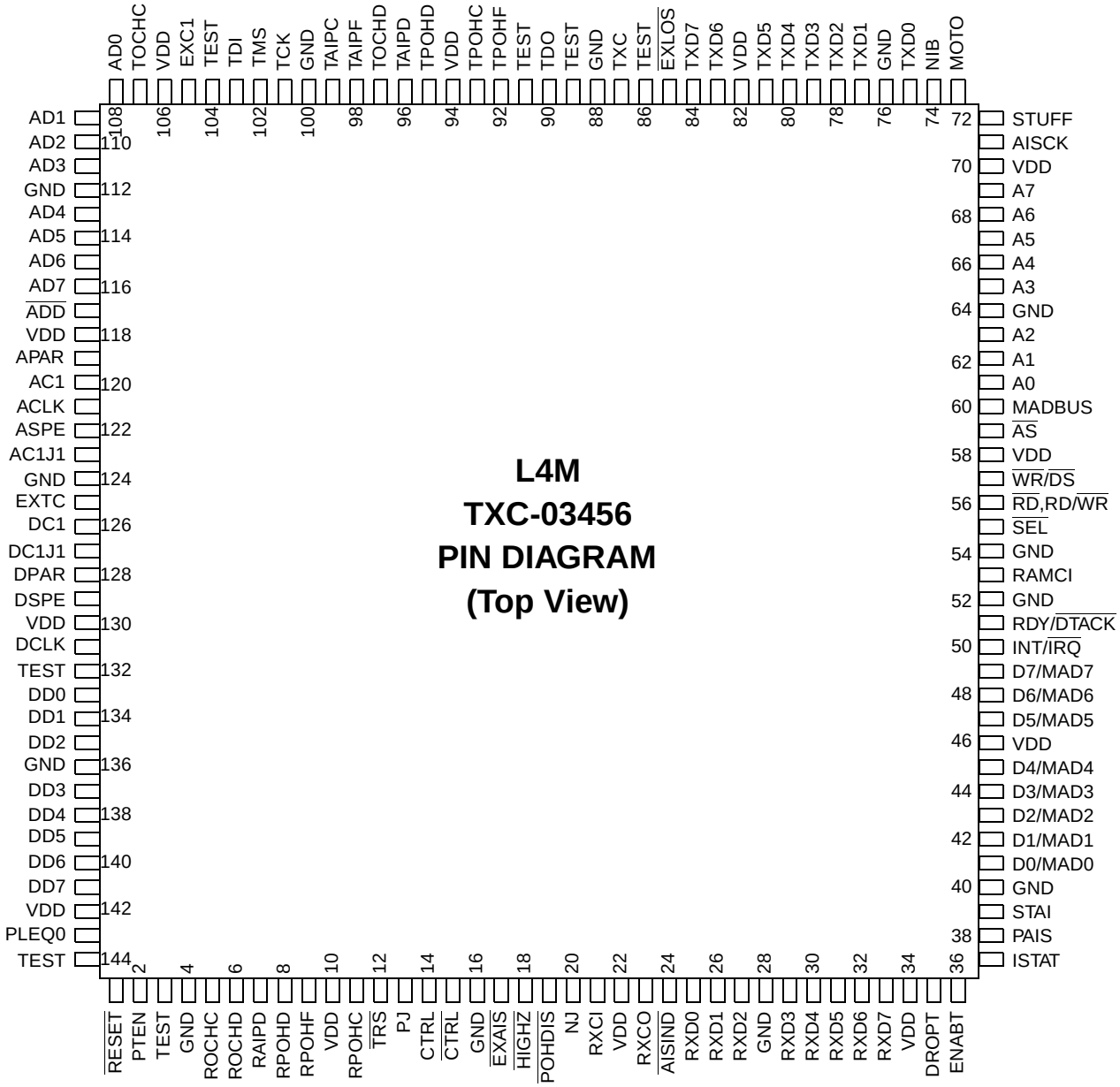


Figure 2. L4M TXC-03456 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	10, 22, 34, 46, 58, 70, 82, 94, 106, 118, 130, 142	P		**VDD:** +5 volt supply voltage, ± 5%
GND	4, 16, 28, 40, 52, 54, 64, 76, 88, 100, 112, 124, 136	P		**Ground:** 0 volt reference.

*Note: I = Input; O = Output; P = Power

140 MBIT/S LINE INTERFACE

Symbol	Pin No.	I/O/P	Type*	Name/Function
TXC	87	I	TTL	**Transmit 140 Mbit/s Line Clock:** The clock rate is 34.816 MHz (nibble rate), or 17.408 MHz (byte rate). Byte or nibble-wide line data is clocked into the L4M on positive transitions of this clock when control bit TINVC is a 0**.** Data is clocked in on negative transitions of this clock when control bit TINVC is a 1.
TXDn (n=7-0)	84, 83, 81-77, 75	I	TTL	**Transmit 140 Mbit/s Line Data:** TXD7 (pin 84) is defined as the MSB for the byte interface, and is the first bit transmitted. For the nibble interface, TXD3 (pin 79) is defined as the MSB. TXD0 (pin 75) is the LSB for both the byte and nibble interfaces.
$\overline{\text{EXLOS}}$	85	I	TTLp	**External 140 Mbit/s Loss of Signal:** An optional low input signal to report an external transmit 140 Mbit/s line loss of signal. If this lead is not used it must be connected to VDD.
RXDn (n=7-0)	33-29 27-25	O	TTL4mA	**Receive 140 Mbit/s Line Data:** RXD7 (pin 33) is defined as the MSB for the byte interface, and is the first bit received. For the nibble interface, RXD3 (pin 29) is defined as the MSB. RXD0 (pin 25) is the LSB for both the byte and nibble interfaces.
RXCO	23	O	TTL4mA	**Receive 140 Mbit/s Line Output Clock:** The clock rate is 34.816 MHz (nibble rate), or 17.408 MHz (byte rate). Byte or nibble-wide line data is clocked out of the L4M on negative transitions of this clock when control bit RINVC is a 0**.** Data is clocked out on positive transitions of this clock when control bit RINVC is a 1. This clock is derived from the receive line input clock (RXCI).
RXCI	21	I	TTL	**Receive 140 Mbit/s Line Input Clock:** Byte (17.408 MHz) or nibble (34.816 MHz) clock used by the internal desynchronizer for sourcing data. This clock is used to derive the receive line output clock (RXCO).
NIB	74	I	TTL	**Nibble/Byte Data Selection:** Common control lead for both the transmit and receive 140 Mbit/s interfaces. A high selects the interfaces as nibble, while a low selects the interfaces as byte.

*Note: See Input, Output and I/O Parameters section for Type definitions.

SDH/SONET DROP BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
DCLK	131	I	TTL	**Drop Bus Clock:** Byte-wide data (DD7-DD0), parity (DPAR), payload indicator (DSPE), and the C1 and J1 pulses (DC1J1) are clocked into the L4M on negative transitions of this clock, which has a rate of 19.44 MHz. The clock signal is used for receive timing, and is monitored for loss of clock.
DPAR	128	I	TTL	**Drop Bus Parity Bit:** This input represents an odd parity calculation for each data byte, the DSPE signal, and the DC1J1 signal. When the internal pointer tracking feature is enabled, parity is calculated for data and the C1 pulse only. When a 1 is written to control bit PARDO, parity is calculated for the data byte only.
DC1J1	127	I	TTL	**Drop Bus C1J1 Indicator:** The C1 pulse is an active high, one clock cycle wide timing pulse, that indicates the starting location of the first C1 byte time slot in the STM-1 or STS-3c frame when DSPE is low. When the pointer tracking feature is disabled, a J1 pulse, also one clock cycle wide, must be present to identify the starting location of the J1 byte in the AU-4 VC-4, or in the STS-3c SPE signal when DSPE is high. If the J1 pulse is not present, the pointer tracking feature must be enabled. The C1 pulse must be provided on this signal lead, or on the DC1 signal lead. Up to a frame in offset delay for the C1 byte can be compensated for when the pointer tracking mode is enabled**.** The receive offset delay is controlled by bit RC1DC in the memory map.
DSPE	129	I	TTL	**Drop Bus SPE Indicator:** A signal that is active high during the AU-4/STS-3c SPE time when the pointer tracking feature is disabled. This signal is not required when the pointer tracking feature is enabled.
DDn (n=7-0)	141-137 135-133	I	TTL	**Drop Bus Byte:** Byte-wide data that corresponds to the AU-4/STS-3c signal from the drop bus. The first bit dropped corresponds to DD7 (pin 141).
DC1	126	I	TTL	**Drop Bus C1 Pulse:** An external positive C1 pulse that may be provided on this pin instead of in the DC1J1 signal. This signal is or-gated internally with the DC1J1 signal to form a composite C1J1. When this signal lead is not used, it must be grounded.

SDH/SONET ADD BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
ACLK	121	I/O	TTL4mA	**Add Bus Clock:** The add clock is used for build timing, transmit FIFO, and for sourcing the add bus byte-wide data (AD7-AD0) and parity (APAR), when add bus timing is selected. When external timing or drop timing mode is selected, this signal becomes an output. The add bus clock rate is 19.44 MHz.
AC1J1	123	I/O	TTL4mA	**Add Bus C1J1 Indicator:** The C1 pulse is an active high, one clock cycle wide, timing pulse that identifies the starting location of the first C1 byte time slot in the STM-1 or STS-3c frame. The C1 pulse may be provided on a separate lead (AC1) when the add bus timing mode is selected. A J1 pulse, also one clock cycle wide, identifies the starting location of the J1 byte in the AU-4 VC-4 or STS-3c SPE signal when the POH bytes are used. When the POH feature is disabled, the J1 pulse is not required. When external timing or drop timing is enabled this signal becomes an output. The C1J1 pulses correspond to the C1 and J1 bytes present on AD(7-0). When a 1 is written to control bit AC1EN, the C1 pulse may be provided on a separate lead (AC1) instead of in the AC1J1 signal.
APAR	119	O	TTL4mA	**Add Bus Parity Bit:** This output bit represents the odd parity calculation for each data byte (and SPE and C1J1, including AC1, when they are outputs). When a 1 is written to control bit PARDO, parity is calculated for the data byte only. APAR is not calculated over the unused TOH Byte times.
ASPE	122	I/O	TTL4mA	**Add Bus SPE Indicator:** An input signal in add timing mode that is high during the AU-4/STS-3c SPE time. When the external timing or drop timing modes are enabled, this signal becomes an output.
ADn (n=7-0)	116-113 111-108	O	TTL4mA	**Add Data Byte:** Byte-wide data that corresponds to the AU-4/STS-3c signal to be placed on the add bus. The first bit transmitted corresponds to AD7 (pin 116). Data is three-stated during periods of no activity (e.g., during unused TOH times).
$\overline{\text{ADD}}$	117	O	TTL4mA	**Add Indicator:** An active low signal that identifies the time slots corresponding to the output data (AD7-AD0).
AC1	120	I/O	TTL4mA	**Add Bus C1 Pulse:** This lead provides the C1 pulse as an output when the drop bus timing or external timing modes are enabled, and when the AC1EN control signal is a 1. The AC1J1 signal will contain the C1 pulse. When the add bus timing mode is enabled, this lead may be used as the C1 input, independent of the AC1EN control bit. This signal is or-gated internally with the AC1J1 signal in the add bus timing mode to form a composite C1J1signal. If this signal lead is not used in the add bus timing mode, it must be grounded.

RECEIVE AND TRANSMIT PATH OVERHEAD BYTE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RPOHF	9	O	TTL4mA	**Receive Path Overhead Framing:** A positive, one clock cycle wide, framing pulse that is synchronous with bit 1 in the J1 byte in the POH interface data.
RPOHD	8	O	TTL4mA	**Receive Path Overhead Data:** The serial output for the nine Path Overhead bytes: J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5 bytes. The bytes are clocked out, starting with bit 1 in J1, on negative transitions of the clock signal (RPOHC) when the POH feature is enabled.
RPOHC	11	O	TTL4mA	**Receive Path Overhead Clock:** The nine POH bytes and RAIPD data are clocked out on negative transitions of this clock signal (RPOHC).
TPOHF	92	O	TTL4mA	**Transmit Path Overhead Framing:** A positive, one clock cycle wide, framing pulse that is synchronous with bit 1 in the J1 byte in the POH interface data.
TPOHD	95	I	TTL	**Transmit Path Overhead Data:** A serial input for the Path Overhead bytes: J1, C2, G1, F2, H4, Z3, Z4, and Z5 bytes. The B3 byte time slot must be provided, but the contents are ignored by the L4M. The bytes are clocked in, starting with bit 1 in J1, on positive transitions of the clock signal (TPOHC). 8 bits are clocked in during the B3 Byte time, but they are ignored by the L4M device. The L4M recalculates the B3 byte parity value. The POH bytes are ignored when a low is placed on the $\overline{\text{POHDIS}}$ lead (pin 19).
TPOHC	93	O	TTL	**Transmit Path Overhead Clock:** The transmit clock used for clocking in the Path Overhead bytes. Data is clocked in on positive transitions of the clock.

RECEIVE AND TRANSMIT OVERHEAD COMM CHANNEL INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TOCHC	107	O	TTL4mA	**Transmit Overhead Comm Channel Clock:** An output clock provided for sourcing the transmit overhead communications channel data ("O"-bits). This clock has an effective data transfer rate of 720 kHz (8 kHz per bit, times 90 bits).
TOCHD	97	I	TTL	**Transmit Overhead Comm Channel Data:** Data is clocked in on positive transitions of the clock signal (TOCHC). The data is unaligned in relationship to the overhead communications channel data bit placement in the SDH/SONET format.
ROCHC	5	O	TTL4mA	**Receive Overhead Comm Channel Clock:** A clock provided for outputting the transmit overhead communications channel data. This clock has an effective data transfer rate of 720 kHz (8 kHz per bit, times 90 bits).
ROCHD	6	O	TTL4mA	**Receive Overhead Comm Channel Data:** Data is clocked out on negative transitions of the clock signal (ROCHC). The data output for the overhead communications channel from the format is unaligned in relationship with the SDH/SONET frame.

EXTERNAL TIMING FOR ADD BUS

Symbol	Pin No.	I/O/P	Type	Name/Function
EXTC	125	I	TTL	**External Clock Input:** Enabled by placing a high on the ENABT lead (pin 36). Used for deriving output timing for the add bus. A clock rate of 19.44 MHz is required for AU-4/ STS-3c operation. This clock input is monitored for loss of clock.
EXC1	105	I	TTL	**External C1 Input:** Enabled by placing a high on the ENABT lead (pin 36). An optional C1 input signal that can be used for frame alignment. In addition, an option is provided for the pointer tracking feature which can compensate up to a frame in offset delay. If this pin is not used, it should be grounded.

RECEIVE DESYNCHRONIZER

Symbol	Pin No.	I/O/P	Type	Name/Function
CTRL	14	O	CMOS4mA	**Phase Detector Output Positive:** Normally connected to low pass filter as part of the desynchronizer phase-locked loop. See Figure 25.
$\overline{\text{CTRL}}$	15	O	CMOS4mA	**Phase Detector Output Negative:** Normally connected to low pass filter as part of the desynchronizer phase-locked loop. See Figure 25.
STUFF	72	O	TTL4mA	**Stuff (Justification) Opportunity Indication:** This lead provides a status of the stuff (justification) S-bit in the Z byte for each row in the nine subframes in the 140 Mbit/s SDH/SONET format. The pin is high for one SONET/SDH row when there is a stuff indication, and low when this bit is information. The output on this pin is updated each row based on majority voting of the five c-bits.
PJ	13	O	TTL4mA	**Positive Justification Indication:** This lead provides a positive pulse when a positive pointer movement is detected. The pulse width is one DCLK cycle wide.
NJ	20	O	TTL4mA	**Negative Justification Indication:** This lead provides a positive pulse when a negative pointer movement is detected. The pulse width is one DCLK cycle wide.
PLEQ0	143	O	TTL4mA	**Pointer Leak Counter Equal to Zero Indication:** This lead provides a positive indication when the internal pointer leak counter is equal to zero. This signal is reset to zero when the internal counter is preset. A positive pulse, one DCLK cycle wide, is then output for each time a bit is leaked out of the L4M's Desynchronizer. The last bit leaked out is represented by the last rising edge of the PLEQ0 signal lead.

RECEIVE AND TRANSMIT ALARM INDICATION PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
RAIPD	7	O	TTL4mA	**Receive Alarm Indication Port Data:** A serial output that provides the four-bit FEBE count (received B3 BIP-8 parity errors, bits 1-4), and Path RDI alarm indication (bit 5) for ring operation. Bits 6, 7, and 8 are set to 0, 0, 1, respectively. This lead is normally connected to the TAIPD lead at the mate 140 Mbit/s Mapper for ring operation. The RPOHC signal is used to clock out this signal. The RPOHF signal is used to provide the frame reference signal. The data output is disabled (forced to 0) when an active low is placed on the $\overline{\text{POHDIS}}$ lead.
TAIPD	96	I	TTL	**Transmit Alarm Indication Port Data:** This serial input lead is normally connected to the RAIPD lead at the mate L4M for ring operation. Provides an input for the four-bit FEBE count (received B3 BIP-8 parity errors), and Path RDI alarm indication from the mate L4M. The data input is disabled when an active low is placed on the $\overline{\text{POHDIS}}$ lead.
TAIPC	99	I	TTL	**Transmit Alarm Indication Port Clock:** This clock input is normally connected to the RPOHC clock lead at the mate L4M for ring operation. Transmit alarm data (TAIPD) is clocked into the L4M on positive transitions of the clock. This clock input is monitored for loss of clock.
TAIPF	98	I	TTL	**Transmit Alarm Indication Port Framing Pulse:** Normally connected to RPOHF lead at the mate L4M for ring operation. Used to indicate the start of the external alarm indications for ring operation.

BOUNDARY SCAN

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	101	I	TTL	**Test Boundary Scan Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on positive transitions.
TDI	103	I	TTLp	**Test Boundary Data Input:** Serial data input for boundary scan test messages.
TDO	90	O 3-state	TTL4mA	**Test Boundary Data Output:** Serial data output whose information is clocked out on negative transitions of TCK. This pin requires a 4.7 kΩ pull-up resistor if it is used.
TMS	102	I	TTLp	**Test Boundary Mode Select:** The signal present on this lead is used to control test operations.
$\overline{\text{TRS}}$	12	I	TTLp	**Test Boundary Scan Reset:** An active low asynchronous reset signal. This lead should be held low if the boundary scan is not being used.

OTHER PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
ENABT	36	I	TTL	**Enable Add Bus Timing:** Works in conjunction with the DROPT lead. The following table is the definition of the timing modes: ENABT / DROPT / Action 1 / X / External timing. Add bus timing derived from the external clock (EXTC) and the external framing pulse (EXC1). The ASPE, AC1J1, ACLK and AC1 signal leads become output leads. 0 / 0 / Add bus timing. Data derived from the add bus clock, ASPE, and AC1J1 input signals. Note: ASPE, AC1J1, AC1 and ACLK are inputs. 0 / 1 / Drop bus timing. Data, ASPE, AC1J1, and ACLK output signals are derived from the drop bus clock (DCLK) and C1 pulse in the drop bus DC1J1 signal.
DROPT	35	I	TTL	**Drop Timing Mode Enabled:** Works in conjunction with the ENABT lead. See table above.
ISTAT	37	I	TTL	**External STS Alarm Indication:** The purpose of this lead is to provide an upstream AIS indication for the L4M. This pin is enabled by writing a 1 to the EAPE control bit. A high on this lead generates AIS, and path RDI, when enabled.
PAIS	38	I	TTL	**External Path AIS Indication:** The purpose of this lead is to provide an upstream AIS indication for the L4M. This pin is enabled by writing a 1 to the EAPE control bit. A high generates line AIS, and path RDI, when enabled.
STAI	39	I	TTL	**STS Network Alarm Indication:** This pin is enabled by writing a 1 to the XRDIEN control bit. A high generates a path RDI, when enabled.
AISCK	71	I	CMOS	**AIS Clock Input:** Enabled when control bit BSAISE is a 0. This clock is used to generate transmit and receive 140 Mbit/s AIS on defined alarms. The clock frequency must be 34.816 MHz +/- 15 ppm for a nibble interface, and 17.408 MHz +/- 15 ppm for a byte interface. If AIS bit stuffing is used to generate AIS (control bit BSAISE is written with a 0), this clock is not required.
$\overline{\text{EXAIS}}$	17	I	TTLp	**External AIS Alarm Input:** A low causes a receive 140 Mbit/s AIS when enabled, and a path RDI to be generated. May be used when processing received POH bytes via external circuitry (e.g., C2 byte).

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{POHDIS}}$	19	I	TTLp	**Path Overhead Byte Processing Disabled:** A low disables the insertion of the POH bytes (they are tri-stated) into the SPE from either the memory map RAM or the POH interface. It also disables the processing of the POH bytes in the receive direction and their subsequent actions.
$\overline{\text{AISIND}}$	24	O	TTL	**Receive AIS Indication Output:** A low indicates that 140 Mbit/s AIS is being generated in the receive path. This pin is disabled when the BSAISE control bit=1 and the RLAISD alarm=1. However, when the L4M generates a receive line AIS, this pin will go low even if BSAISE=1 and RLAISD=1.
$\overline{\text{HIGHZ}}$	18	I	TTLp	**High Impedance Enable:** A low causes all output and bi-directional pins to three-state for test purposes.
PTEN	2	I	TTL	**Pointer Tracking Enable:** A high enables the internal pointer tracking feature. The pointer tracking feature determines the starting location of J1 in the dropped signal. The C1 pulse must be provided as the DC1, or DC1J1 signal. The J1 pulse must not be provided. The DSPE lead is ignored when the pointer tracking machine feature is enabled. A low requires the DC1J1 and DSPE signals to be provided as inputs.
$\overline{\text{RESET}}$	1	I	TTLp	**Hardware Reset:** A low clears all performance counters, and presets the internal FIFOs and counters. All control bits (10H-1FH) are preset to 0 except for bit 3 of register 13H and bit 0 of registers 1AH and 1BH. These 3 bits are preset to 1. This pulse must be present for a minimum of 200 nanoseconds. Note: The L4M requires approximately 1 microsecond upon power-up for stabilization before a low can be applied to this pin.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-0)	69-65 63-61	I	TTL	**Address Bus (Motorola/Intel Buses):** These are address line inputs that are used for accessing a RAM location for a read/write cycle. A0 is the least significant bit. High is logic 1.
$\overline{\text{AS}}$	59	I	TTL	**Address Select (Multiplex Bus):** A low is used for address select when the multiplex bus mode is selected.
D(7-0) MAD(7-0)	49-47 45-41	I/O	TTL8mA	**Data Bus:** Bi-directional data lines used for transferring data. D0 is the least significant bit. Can also be used as multiplexed address and data bus with Motorola interface. High is logic 1.
$\overline{\text{SEL}}$	55	I	TTLp	**Select:** A low will enable data transfers between the processor and the L4M RAM during a read/write cycle.
$\overline{\text{RD}}$ RD/$\overline{\text{WR}}$	56	I	TTL	**Read (Intel mode) or Read/Write (Motorola mode):** Intel Mode - An active low signal generated by the microprocessor for reading the L4M RAM locations. Motorola and multiplex Mode - An active high signal generated by the microprocessor for reading the L4M RAM locations. An active low signal is used to write to L4M RAM locations.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{WR}$ / $\overline{DS}$	57	I	TTL	**Write (Intel mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the Mapper RAM locations. Motorola Mode - Not used. For the multiplex mode, this lead is used for the Data Select control.
RDY/ $\overline{DTACK}$	51	O	TTL8mA 3-state	**Ready (Intel mode) or Data Transfer Acknowledge (Motorola modes):** This lead is three-stated. Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates that the L4M cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola and multiplex Mode - During a read bus cycle, a low signal indicates that the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INT/ $\overline{IRQ}$	50	O	TTL4mA	**Interrupt:** Intel Mode - A high on this output pin signals an interrupt request to the microprocessor. Motorola Mode - A low on this output pin signals an interrupt request to the microprocessor.
MOTO	73	I	TTL	**Motorola/Intel Microprocessor Select:** This lead works in conjunction with the MADBUS lead. A high selects a Motorola microprocessor compatible bus interface. A low selects the Intel microprocessor compatible bus interface. The following table summarizes the microprocessor selection. MOTO / MADBUS / Action 0 / X / Intel Microprocessor Interface, separate address/data buses. 1 / 0 / Motorola Microprocessor Interface, separate address/data buses. 1 / 1 / Motorola Microprocessor Interface, multiplexed address/data buses.
MADBUS	60	I	TTL	**Multiplexed Address/Data Bus:** When the MOTO lead is high, a high on this lead selects a Multiplexed Address/Data Bus interface, while a low selects separate Address/Data buses. This lead is disabled when MOTO is low.
RAMCI	53	I	CMOS	**RAM Clock Input:** Asynchronous clock input used for the internal L4M RAM operation. This clock must be connected to the microprocessor clock that has an operating rate of between 12 and 25 MHz with a duty cycle of 50 $\pm$ 10%. This clock is also used as an internal time base for the loss of signal detectors.

MANUFACTURE TEST PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
TEST	144	I	TTLp	**Test Pin for Manufacture Testing:** For normal operation this pin must be grounded.
TEST	89	I	TTLp	**Test Pin for Manufacture Testing.** For normal operation this pin must be grounded.
TEST	91	O	TTL4mA	**Test Pin for Manufacture Testing:** For normal operation this pin must be left unconnected.
TEST	104	I	TTLp	**Test Pin for Manufacture Testing:** For normal operation this pin must be grounded.
TEST	86	I	TTLp	**Test Pin for Manufacture Testing:** For normal operation this pin must be grounded.
TEST	132	I	TTLp	**Test Pin for Manufacture Testing:** For normal operation this pin must be grounded.
TEST	3	I	TTLp	**Test Pin for Manufacture Testing:** For normal operation this pin must be grounded.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Ambient operating temperature	T_A	-40	85	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			23.0	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.00	5.25	V	
I_{DD}		251	320	mA	
P_{DD}		1.27	1.68	W	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			1.65	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		3.5		pF	

Note: Input has a 9k (nominal) internal pull-up resistor.

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	$C_{LOAD} = 15pF$
t_{FALL}	2.0	3.9	8.0	ns	$C_{LOAD} = 15pF$

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	C_{LOAD} = 15pF
t_{FALL}	1.0	2.0	4.0	ns	C_{LOAD} = 15pF

Input/Output Parameters For TTL8mA

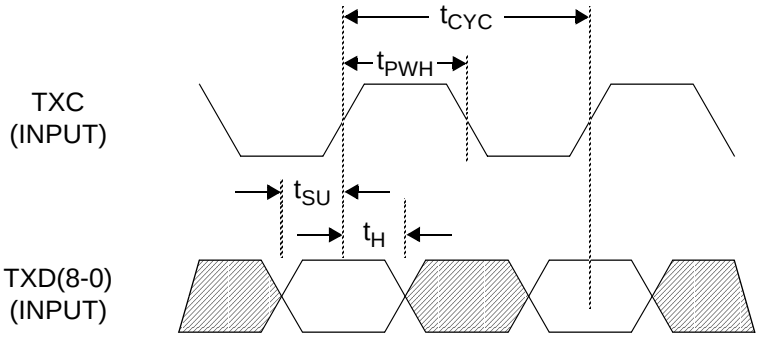
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	mA	V_{DD} = 5.25
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.9	4.5	8.0	ns	C_{LOAD} = 25pF
t_{FALL}	0.8	1.5	3.1	ns	C_{LOAD} = 25pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the L4M device are illustrated in Figures 3 through 21, with values of the timing parameters following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ as applicable.

Please note that all of the timing parameters in this document are subject to change contingent on the results of characterization.

Figure 3. Transmit Line Interface Timing

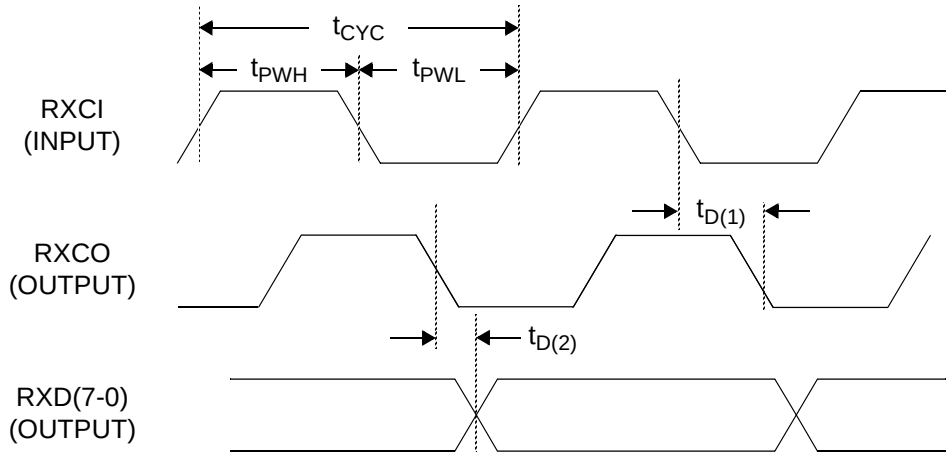


Note: Shown for TINVC equal to 0. Data is clocked in on negative transitions when control bit TINVC is equal to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TXC clock period	t_{CYC}		*		ns
TXC duty cycle, t_{PWH}/t_{CYC}		40		60	%
Data input set up time for TXC↑	t_{SU}	5.0			ns
Data input hold time after TXC↑	t_H	10.0			ns

* Nibble Interface: 28.7224 ns, Byte interface: 57.4449 ns.

Figure 4. Receive Line Interface Timing

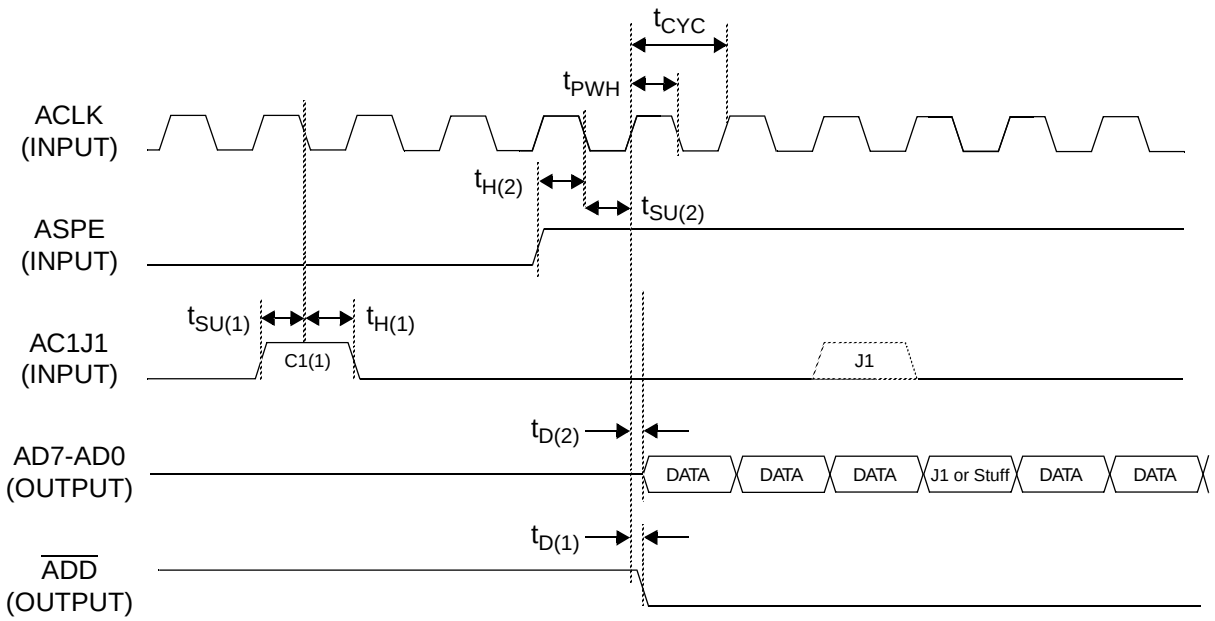


Note: Shown for RINVC equal to 0. Data is clocked out on positive transitions when control bit RINVC is equal to 1.

Parameter	Symbol	Min	Typ	Max	Unit
RXCI clock period	t_{CYC}		*		ns
RXCI duty cycle t_{PWH}/t_{CYC}		40		60	%
RXCO↓ delay after RXCI↓	$t_{D(1)}$			23.0	ns
Data output delay after RXCO↓	$t_{D(2)}$	-2.0		9.5	ns

* Nibble Interface: 28.7224 ns, Byte interface: 57.4449 ns.

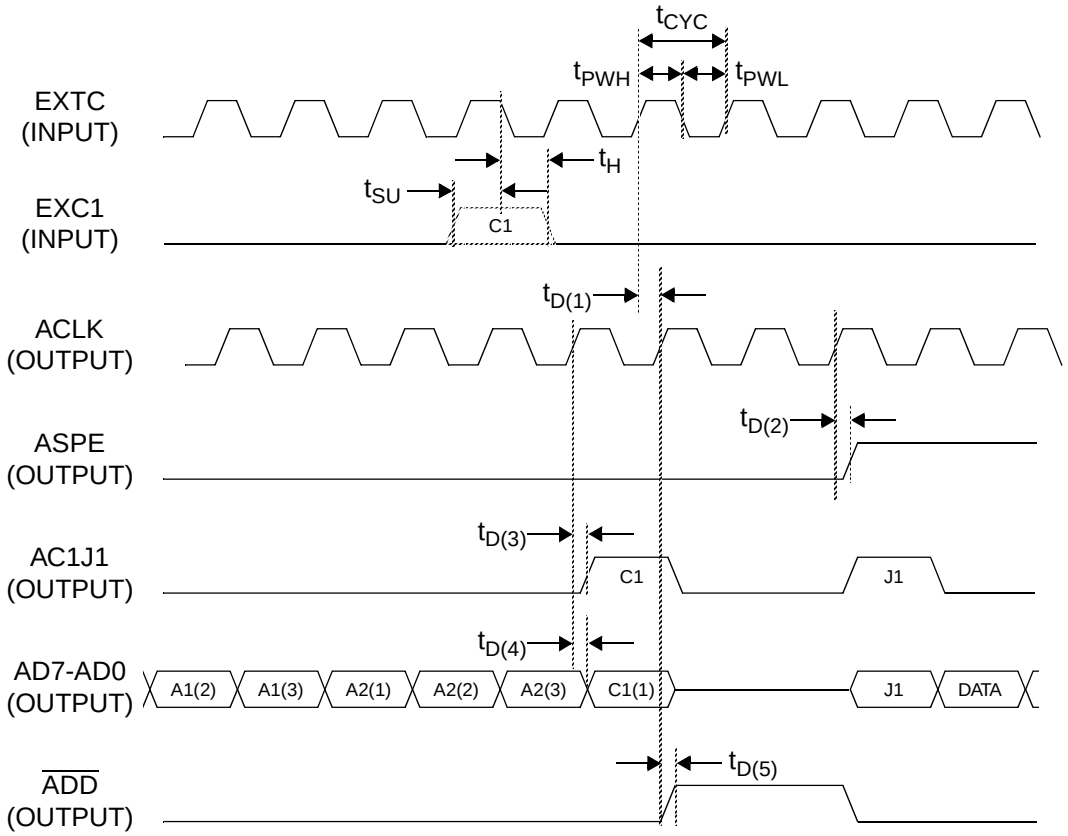
Figure 5. Add Bus Interface Timing (Add Bus)



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. The APAR signal is not shown.

Parameter	Symbol	Min	Typ	Max	Unit
Add clock period	t_{CYC}		51.44		ns
Add clock duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
AC1J1 set-up time to ACLK↓	$t_{SU(1)}$	3.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	7.0			ns
ASPE set-up time to ACLK↓	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
$\overline{ADD}$ low output delay from ACLK↑	$t_{D(1)}$	7.5		33.0	ns
Data output delay from ACLK↑	$t_{D(2)}$	7.0		28.0	ns
APAR output delay from ACLK↑	$t_{D(3)}$ (not shown)	10.0		37.0	ns

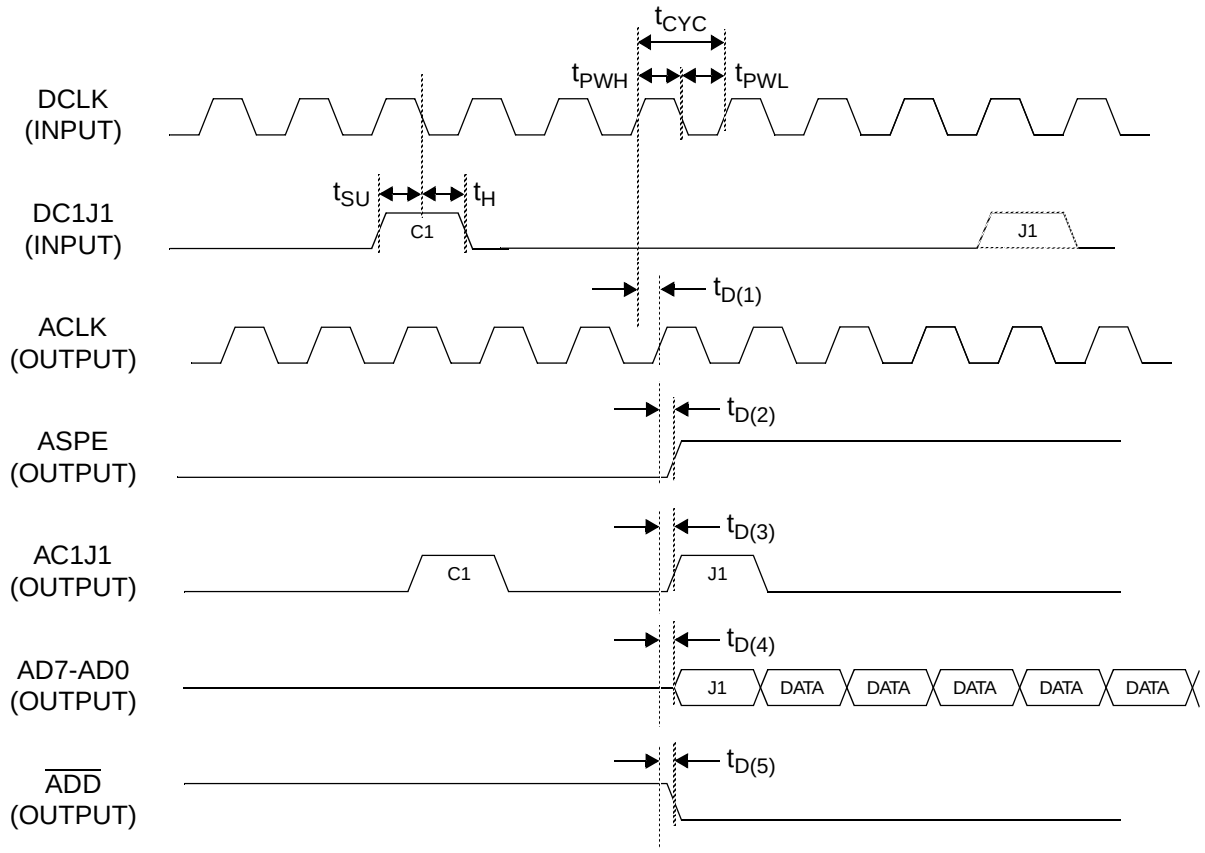
Figure 6. Add Bus Interface Timing (External Clock)



Note: Shown for the TOHOUT control bit equal to 1 and the relationship to an optional external C1 pulse. The APAR signal is not shown.

Parameter	Symbol	Min	Typ	Max	Unit
External clock period	t_{CYC}		51.44		ns
Duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
Set up time for EXC1 for EXTC↓	t_{SU}	4.0			ns
Hold time for EXC1 after EXTC↓	t_H	7.0			ns
Delay ACLK↑ from EXTC↑	$t_{D(1)}$	12.0		28.0	ns
Delay ASPE from ACLK↑	$t_{D(2)}$	-6.0		6.0	ns
Delay AC1J1 from ACLK↑	$t_{D(3)}$	-6.0		6.0	ns
Delay, data from ACLK↑	$t_{D(4)}$	-6.0		6.0	ns
Delay, $\overline{ADD}$ from ACLK↑	$t_{D(5)}$	-6.0		6.0	ns
Delay, APAR from ACLK↑	$t_{D(6)}$ (not shown)	-6.0		11	ns

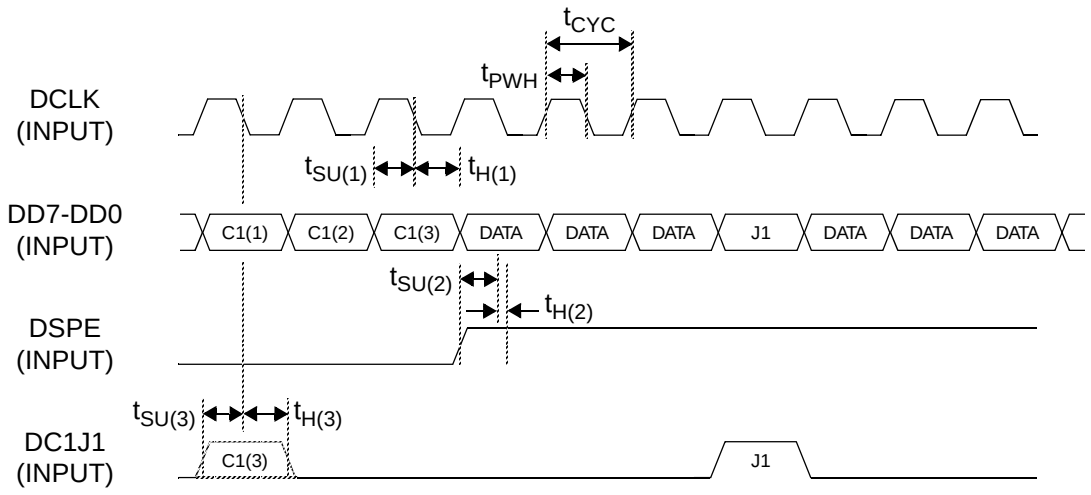
Figure 7. Add Bus Interface Timing (Drop Bus Clock and C1)



Note: The C1 and J1 pulses must be present in the DC1J1 signal if the pointer tracking state machine is turned off. The add bus J1 pulse is shown for the SVC4H control bit set to 0. The APAR signal is not shown.

Parameter	Symbol	Min	Typ	Max	Unit
Drop clock period	t_{CYC}		51.44		ns
Duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
Set-up time for DC1J1 to DCLK↓	t_{SU}	3.0			ns
Hold time for DC1J1 after DCLK↓	t_H	7.0			ns
Delay ACLK↑ from DCLK↑	$t_{D(1)}$	12.0		28.0	ns
Delay ASPE from ACLK↑	$t_{D(2)}$	-6.0		6.0	ns
Delay AC1J1 from ACLK↑	$t_{D(3)}$	-6.0		6.0	ns
Delay, data from ACLK↑	$t_{D(4)}$	-6.0		6.0	ns
Delay, $\overline{ADD}$ from ACLK↑	$t_{D(5)}$	-6.0		6.0	ns
Delay, APAR from ACLK↑	$t_{D(6)}$ (not shown)	-6.0		11	ns

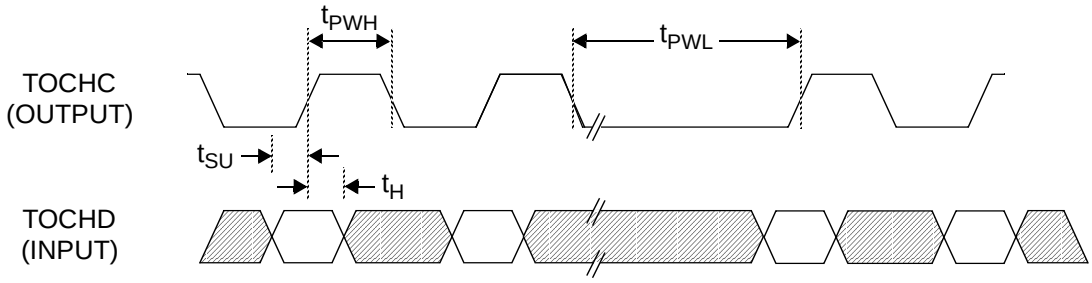
Figure 8. Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the AU-4/STS-3c format there will be one J1 pulse, which indicates the start of the VC-4 that carries the 140 Mbit/s POH bytes and payload. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used it must be grounded. When the pointer tracking machine is selected, the J1 pulse and SPE signal are not required. The DPAR signal is not shown.

Parameter	Symbol	Min	Typ	Max	Unit
Drop clock period	t_{CYC}		51.44		ns
Duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
Data set up time for DCLK↓	$t_{SU(1)}$	4.0			ns
Data hold time after DCLK↓	$t_{H(1)}$	7.0			ns
DSPE set up time for DCLK↓	$t_{SU(2)}$	15.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	4.0			ns
DPAR set up time for DCLK↓	$t_{SU(4)}$ not shown	3.0			ns
DPAR hold time after DCLK↓	$t_{SU(4)}$ not shown	7.0			ns
DC1J1 set up time for DCLK↓	$t_{SU(3)}$	4.0			ns
DC1J1 hold time after DCLK↓	$t_{H(3)}$	7.0			ns

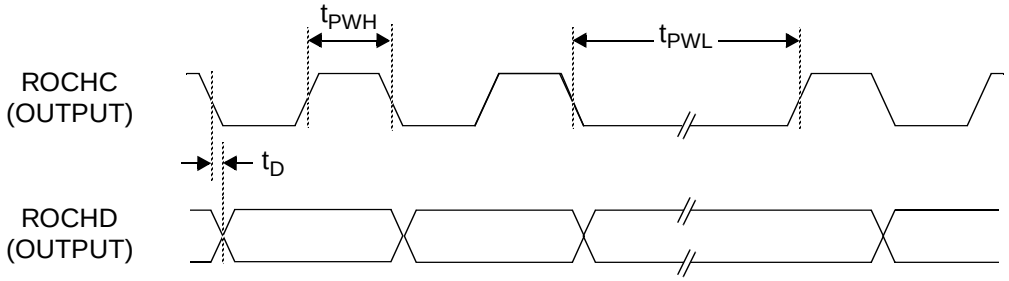
Figure 9. Transmit Overhead Comm Channel Timing



Note: The clock will be non-symmetrical.

Parameter	Symbol	Min	Typ	Max	Unit
TOCHC clock low time	t_{PWL}	668.7		1183.1	ns
TOCHC clock high time	t_{PWH}		668.7		ns
TOCHD data set up time for TOCHC↑	t_{SU}	10.0			ns
TOCHD data hold time after TOCHC↑	t_H	7.0			ns

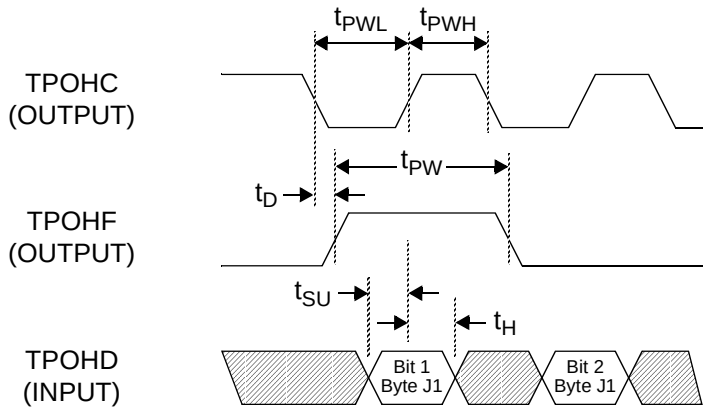
Figure 10. Receive Overhead Comm Channel Timing



Note: The clock will be non-symmetrical.

Parameter	Symbol	Min	Typ	Max	Unit
ROCHC clock low time	t_{PWL}	668.7		1183.1	ns
ROCHC clock high time	t_{PWH}		668.7		ns
ROCHD data output delay from ROCHC↓	t_D	-4.0		5.0	ns

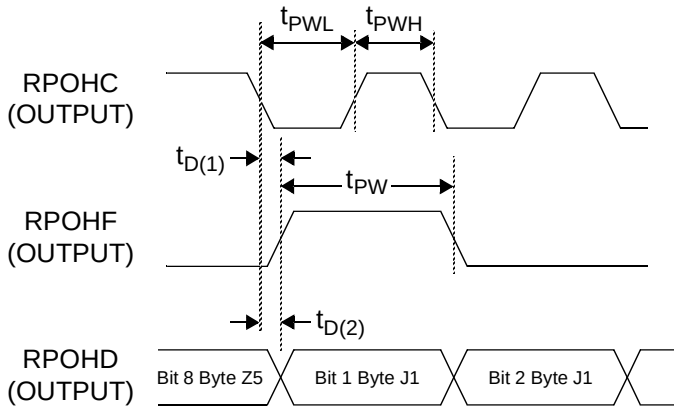
Figure 11. Transmit Path Overhead Interface Timing



Note: The clock will be non-symmetrical.

Parameter	Symbol	Min	Typ	Max	Unit
TPOHC clock high time	t_{PWH}	668.7		1337.4	ns
TPOHC clock low time	t_{PWL}	668.7		1337.4	ns
TPOHF framing pulse output delay for TPOHC↓	t_D	-2.0		5.0	ns
TPOHD data in set up time for TPOHC↑	t_{SU}	10.0			ns
TPOHD data in hold time after TPOHC↑	t_H	7.0			ns
TPOHF pulse width	t_{PW}		1388.8		ns

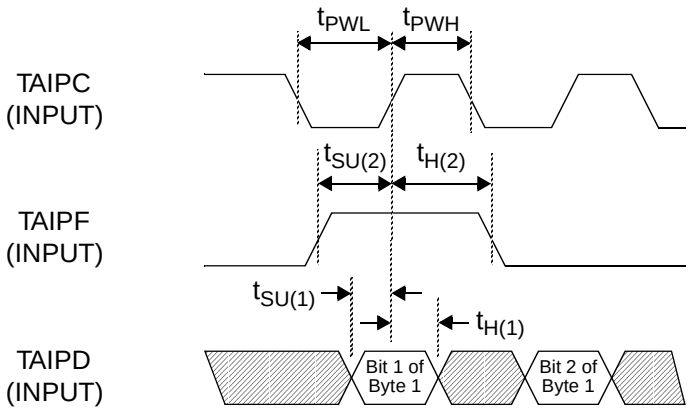
Figure 12. Receive Path Overhead Interface Timing



Note: The clock will be non-symmetrical.

Parameter	Symbol	Min	Typ	Max	Unit
RPOHC clock high time	t_{PWH}	668.7		1337.4	ns
RPOHC clock low time	t_{PWL}	668.7		1337.4	ns
RPOHF framing pulse output delay from RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RPOHD data output delay from RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.8		ns

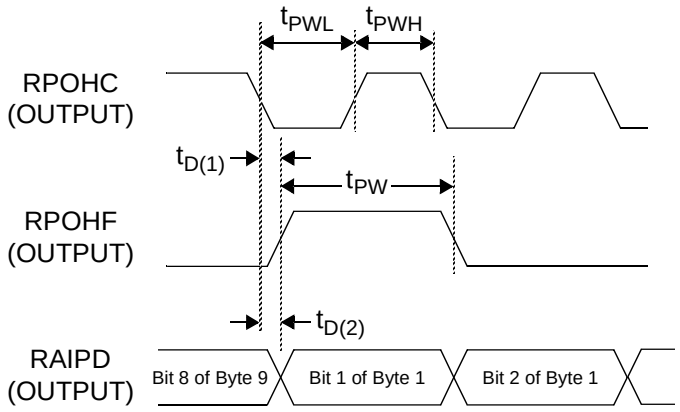
Figure 13. Transmit Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits repeated, nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits 1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TAIPC clock high time	t_{PWH}	617.3		1388.8	ns
TAIPC clock low time	t_{PWL}		771.6		ns
TAIPD data set up time for TAIPC↑	$t_{SU(1)}$	3.0			ns
TAIPD data hold time after TAIPC↑	$t_{H(1)}$	7.0			ns
TAIPF framing pulse set up time for TAIPC↑	$t_{SU(2)}$	3.0			ns
TAIPF framing pulse hold time after TAIPC↑	$t_{H(2)}$	7.0			ns

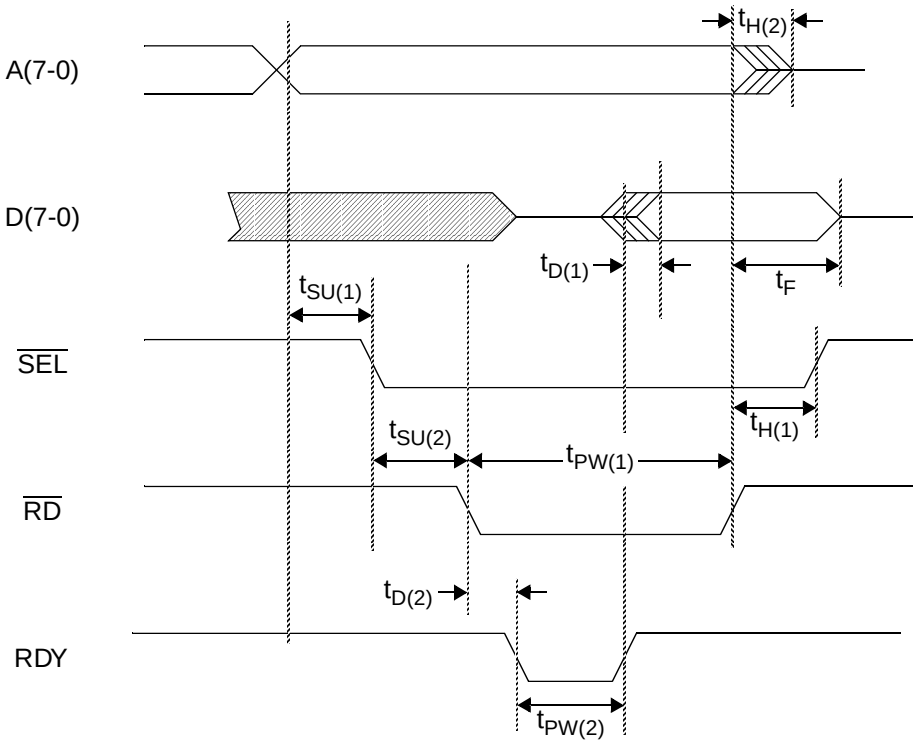
Figure 14. Receive Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits repeated, nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits 1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

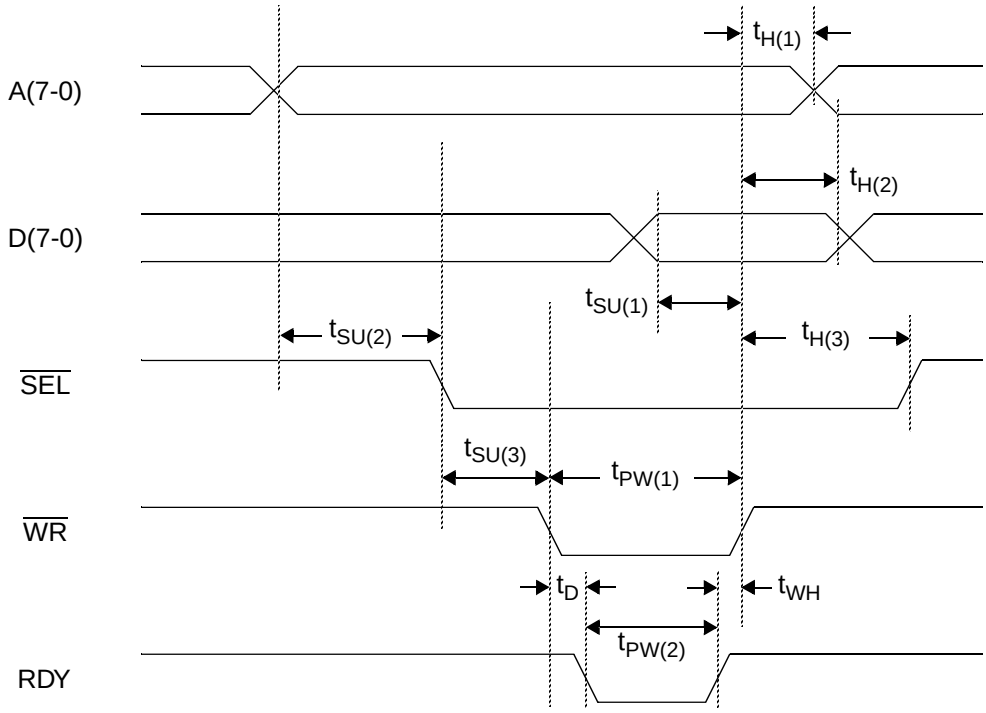
Parameter	Symbol	Min	Typ	Max	Unit
RPOHC clock high time	t_{PWH}	617.3		1388.8	ns
RPOHC clock low time	t_{PWL}		771.6		ns
RPOHF framing pulse output delay from RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RAIPD data output delay from RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.8		ns

Figure 15. Microprocessor Timing Read Cycle - Intel



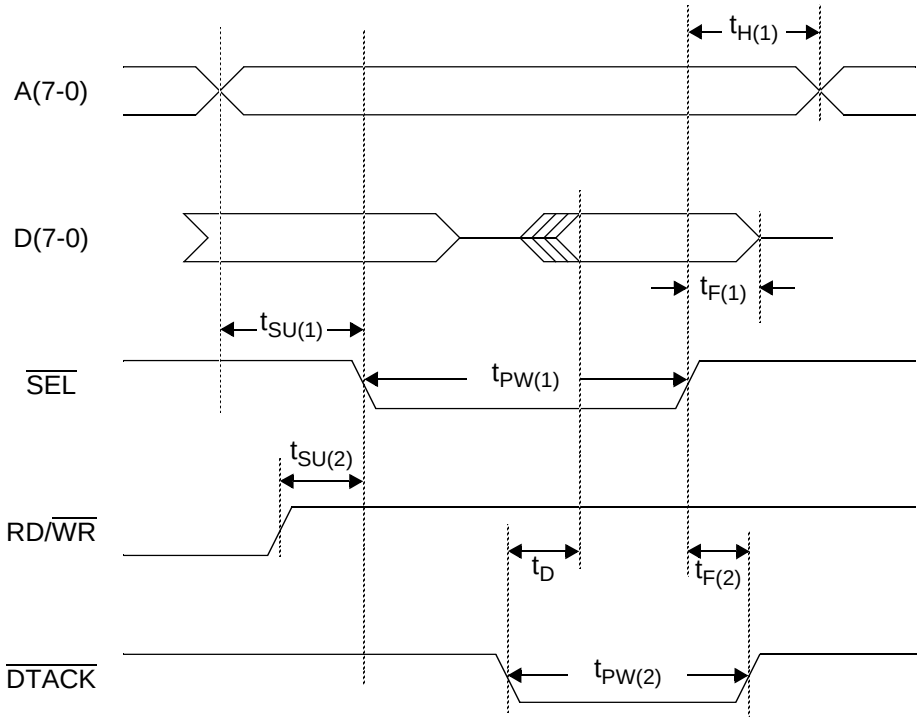
Parameter	Symbol	Min	Typ	Max	Unit
Address set up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
Data valid delay after RDY$\uparrow$	$t_{D(1)}$			5.0	ns
Data float time after $\overline{RD}\uparrow$	t_F	0.0		11.0	ns
$\overline{SEL}$ set up time for $\overline{RD}\downarrow$	$t_{SU(2)}$	0.0			ns
RD pulse width	$t_{PW(1)}$	40.0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0.0			ns
RDY delay after $\overline{RD}\downarrow$	$t_{D(2)}$	0.0		30.0	ns
RDY pulse width	$t_{PW(2)}$	0.0		4.0	µs
Address hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	5.0			ns

Figure 16. Microprocessor Timing Write Cycle - Intel



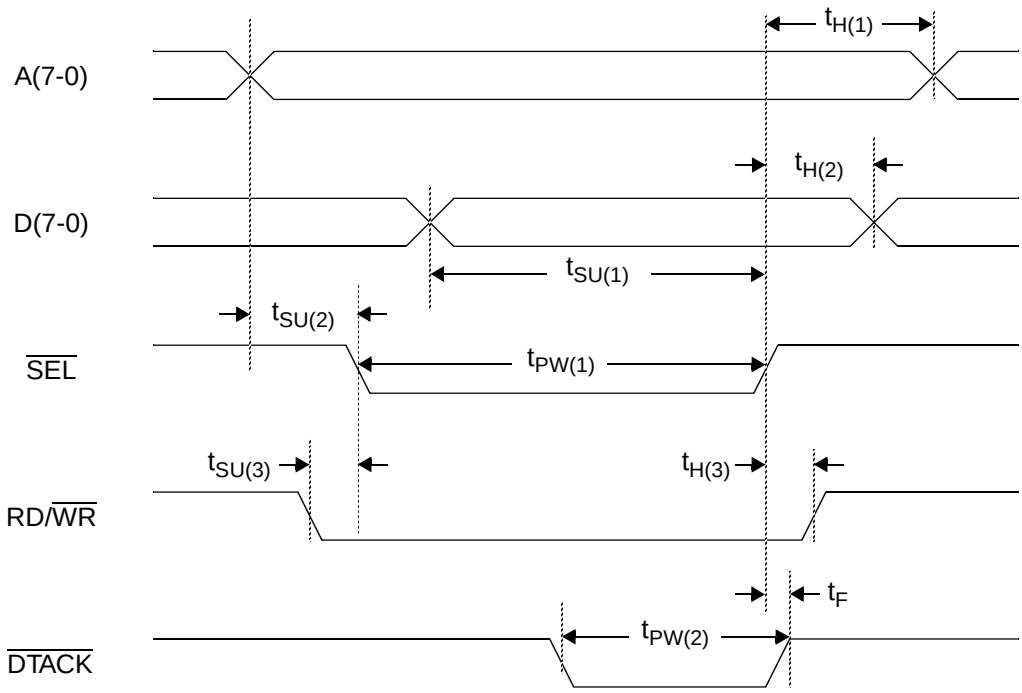
Parameter	Symbol	Min	Typ	Max	Unit
Address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	0.0			
Data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5.0			ns
Data valid set up time to $\overline{WR}\uparrow$	$t_{SU(1)}$	20.0			ns
Address valid set up time for $\overline{SEL}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{SEL}$ set up time for $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40.0			ns
RDY delay after $\overline{WR}\downarrow$	t_D	0.0		30.0	ns
RDY pulse width	$t_{PW(2)}$	0.0		4	us
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	3.0			ns
RDY$\uparrow$ to $\overline{WR}\uparrow$	t_{WH}	0.0			ns

Figure 17. Microprocessor Timing Read Cycle - Motorola



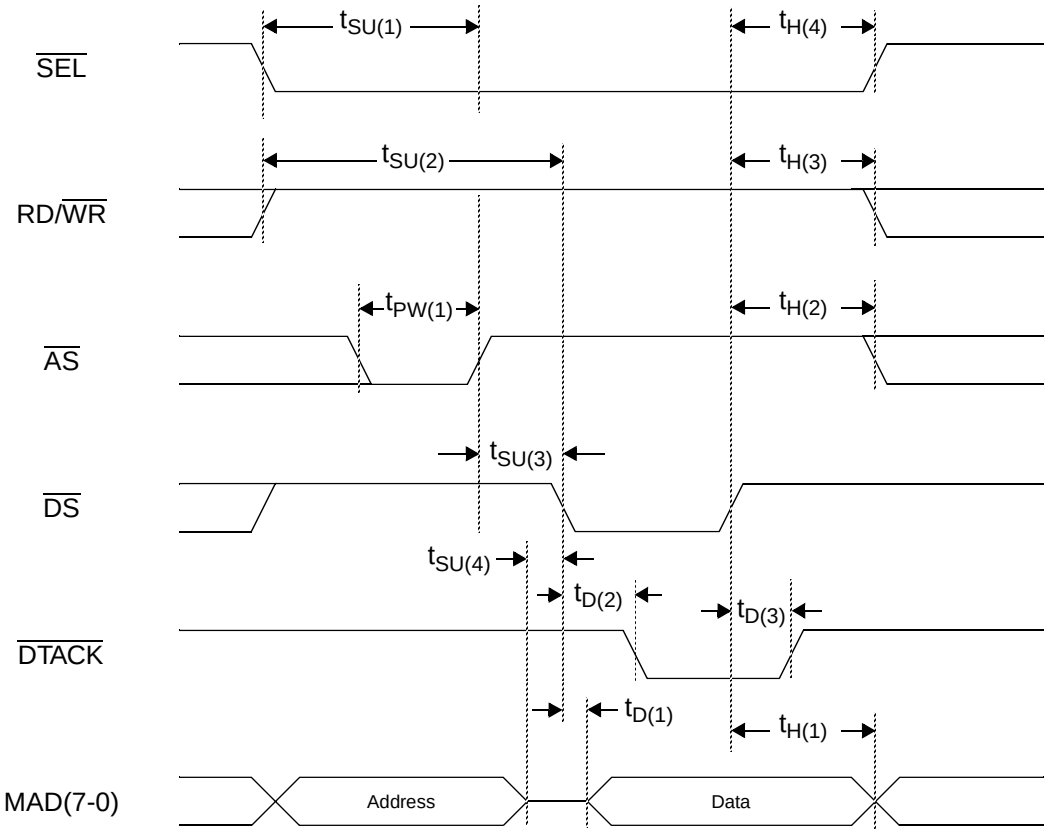
Parameter	Symbol	Min	Typ	Max	Unit
Address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	5.0			
Data float time after $\overline{SEL}\uparrow$	$t_{F(1)}$	0.0		13.0	ns
Address valid set up time for $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
Read set up time for $\overline{SEL}\downarrow$	$t_{SU(2)}$	5.0			ns
Select pulse width	$t_{PW(1)}$	40.0			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		4	us
Data output delay after $\overline{DTACK}\downarrow$	t_D			0.0	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(2)}$	0.0		10.0	ns

Figure 18. Microprocessor Timing Write Cycle - Motorola



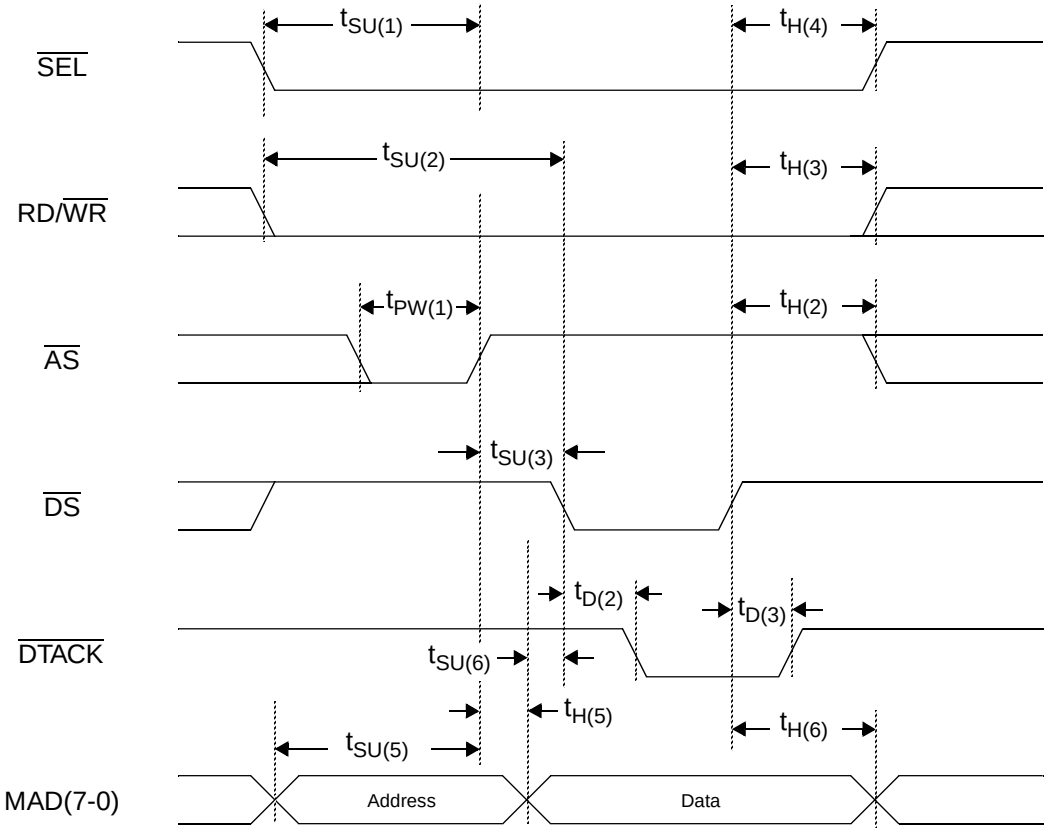
Parameter	Symbol	Min	Typ	Max	Unit
Address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	5.0			ns
Data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	3.0			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
Data valid set up time for $\overline{SEL}\uparrow$	$t_{SU(1)}$	20.0			ns
Address valid set up time for $\overline{SEL}\downarrow$	$t_{SU(2)}$	10.0			ns
Write set up time for $\overline{SEL}\downarrow$	$t_{SU(3)}$	5.0			ns
Select pulse width	$t_{PW(1)}$	40.0			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		4	us
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	0.0		10.0	ns

Figure 19. Microprocessor Timing Read Cycle Multiplex Bus - Motorola



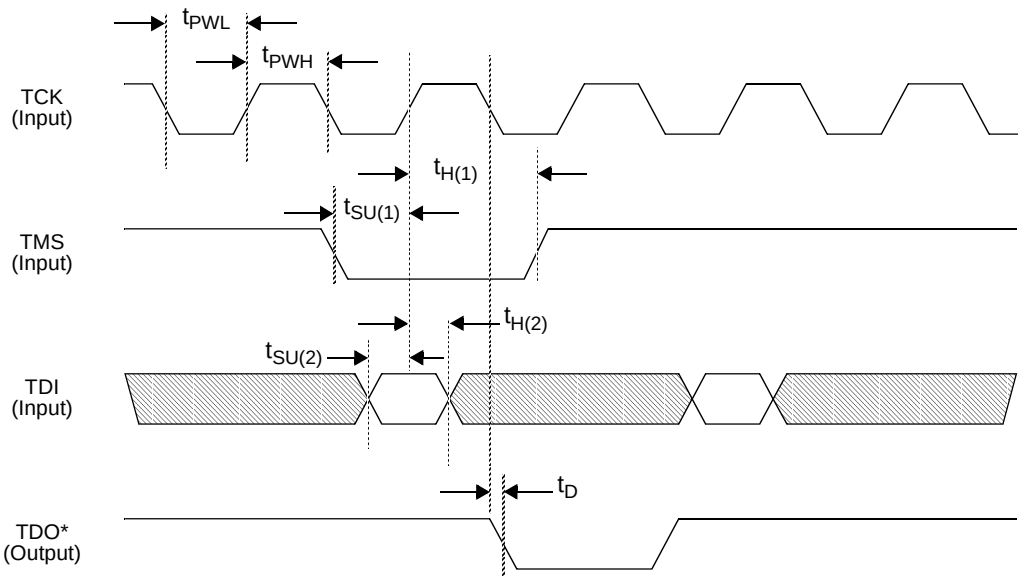
Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}\downarrow$ to $\overline{AS}\uparrow$, setup time	$t_{SU(1)}$	20.0			ns
RD/$\overline{WR}\uparrow$ (read) to $\overline{DS}\downarrow$, setup time	$t_{SU(2)}$	20.0			ns
$\overline{AS}\downarrow$ time	$t_{PW(1)}$	20.0			ns
$\overline{AS}\uparrow$ to $\overline{DS}\downarrow$, setup time	$t_{SU(3)}$	20.0			ns
MAD(7-0) three-state to $\overline{DS}\downarrow$ setup time	$t_{SU(4)}$	20.0			ns
Data out delay from $\overline{DS}\downarrow$	$t_{D(1)}$			250.0	ns
$\overline{DTACK}$ active out delay from $\overline{DS}\downarrow$	$t_{D(2)}$			330.0	ns
$\overline{DTACK}$ inactive out delay from $\overline{DS}\uparrow$	$t_{D(3)}$			20.0	ns
Data out hold time after $\overline{DS}\uparrow$	$t_{H(1)}$			20.0	ns
$\overline{AS}$ hold time after $\overline{DS}\uparrow$	$t_{H(2)}$	0.0			ns
RD/$\overline{WR}$ (read) hold time after $\overline{DS}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{DS}\uparrow$	$t_{H(4)}$	0.0			ns

Figure 20. Microprocessor Timing Write Cycle Multiplex Bus - Motorola



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}\downarrow$ to $\overline{AS}\uparrow$, setup time	$t_{SU(1)}$	20.0			ns
RD/$\overline{WR}\downarrow$ (write) to $\overline{DS}\downarrow$, setup time	$t_{SU(2)}$	20.0			ns
$\overline{AS}\downarrow$ time	$t_{PW(1)}$	20.0			ns
$\overline{AS}\uparrow$ to $\overline{DS}\downarrow$, setup time	$t_{SU(3)}$	20.0			ns
$\overline{DTACK}$ active out delay from $\overline{DS}\downarrow$	$t_{D(2)}$			330.0	ns
$\overline{DTACK}$ inactive out delay from $\overline{DS}\uparrow$	$t_{D(3)}$			20.0	ns
Data in valid setup time for $\overline{DS}\downarrow$	$t_{SU(6)}$	20.0			ns
Data in hold time after $\overline{DS}\uparrow$	$t_{H(6)}$	0.0			ns
$\overline{AS}$ hold time after $\overline{DS}\uparrow$	$t_{H(2)}$	0.0			ns
RD/$\overline{WR}$ (read) hold time after $\overline{DS}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{DS}\uparrow$	$t_{H(4)}$	0.0			ns
Address valid setup time for $\overline{AS}\uparrow$	$t_{SU(5)}$	20.0			ns
Address hold time after $\overline{AS}\uparrow$	$t_{H(5)}$	0.0			ns

Figure 21. Boundary Scan Timing



*Note: TDO is a three-state output. If this pin is used, it should be connected via a 4.7 kΩ resistor to the +5 volt supply.

Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓	t_D	-	7.0	ns

OPERATION

The operations section is divided into two major sections: Internal Device Operation, and External Device Interfaces.

INTERNAL DEVICE OPERATION

Timing Modes

The L4M supports the following timing modes: drop bus, add bus, and external timing modes. In the drop bus timing mode, the drop bus clock (DCLK) and the C1 pulse (DC1J1 or DC1) before or after framing reference compensation, provide the time base for deriving the add bus signals which consist of clock (ACLK), data (AD(7-0)), C1 and J1 indicator (AC1J1 and AC1), SPE indicator (ASPE), add indicator ($\overline{\text{ADD}}$), and parity (APAR). The add side J1 pulse is derived internally. The add bus starting location for the SPE may have a pointer value equal to 0 or 522.

In the add bus timing mode, add bus timing signals are independent of the drop bus signals. Add bus timing is derived from add bus input signals which consists of a clock (ACLK), C1 and J1 indicator ($\overline{\text{AC1J1}}$ and AC1), and SPE indicator (ASPE). The output signals consists of data (AD(7-0)), add indicator ($\overline{\text{ADD}}$), and parity (APAR). The starting location of the SPE (J1 byte) is determined by the input J1 pulse (AC1J1), and SPE indicator (ASPE).

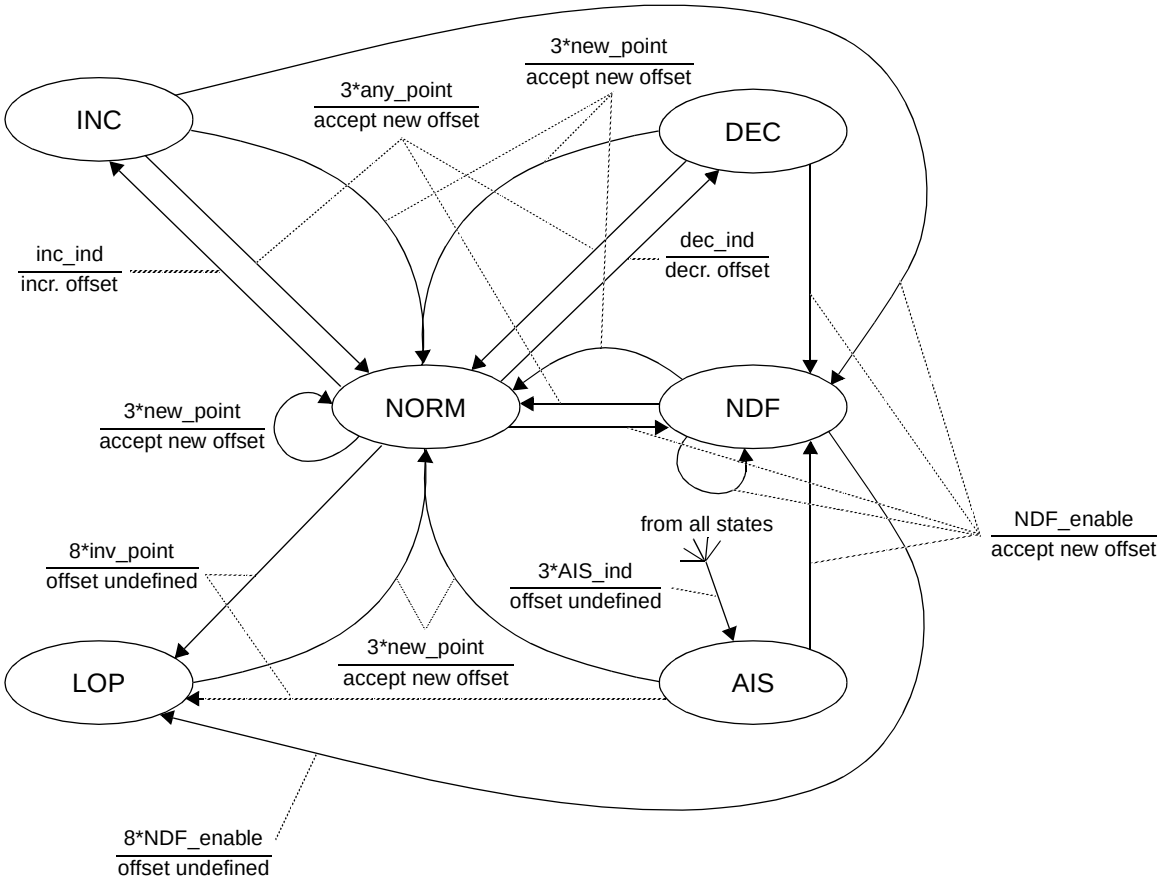
In the external timing mode, the external timing signals are independent of the drop bus timing. The external timing signals consist of an external clock (EXTC) and optional frame reference pulse (EXC1). The L4M can also compensate for up to one frame of offset delay for the external C1 pulse. Add bus output timing is derived from the two external signals and consists of a clock (ACLK), C1 and J1 indicator (AC1J1 and AC1), SPE indicator (ASPE), data (AD(7-0)), add indicator ($\overline{\text{ADD}}$), and parity (APAR). The add bus starting location for the SPE may have a pointer value equal to 0 or 522.

The three timing modes are selected using two control pins, designated as DROPT (pin 35) and ENABT (pin 36). The following table lists the control lead states for selecting the timing mode.

DROPT pin	ENABT pin	Timing Mode
Low	Low	Add Bus Timing
X	High	External Timing
High	Low	Drop Bus Timing

Receive C1 Reference Delay

When the pointer tracking feature is enabled by placing a high on the PTEN lead (pin 2), and control bit RC1DC (bit 3 in 18H) is written with a 1, a 12-bit register location (19H and 18H) is enabled which can compensate for up to 2429 positions (270 columns x 9 rows) for a dropped C1 reference pulse. For example, if a binary 0 is written into the 12-bit register by the microprocessor, the C1 pulse (in DC1J1 or DC1) must be in the C11 time slot (the correct time slot). When the binary value of 1 is written into the 12-bit register, it is assumed that the C1 pulse is shifted one time slot (one clock cycle) into the time slot that corresponds to the C12 byte. This means that the starting point for the frame reference should be one byte earlier. Values written into the 12-bit register greater than 2429 will be counted as a delay equal to 0.



Note: The AIS to LOP transition is not specified for North American applications, and can be disabled by setting the PADS control bit to a 1.

Figure 22. Pointer Interpretation State Diagram

Pointer Tracking Feature

The pointer tracking feature is enabled by placing a high on the PTEN lead (pin 2). The AU-4 pointer is carried in the H1 and H2 bytes. The starting location for the frame is determined by the C1 pulse present in the DC1J1 or DC1 signal lead. When the pointer tracking feature is enabled, the J1 pulse in the DC1J1 signal must not be present, nor is the DSPE signal required. The pointer tracking machine derives the starting location of the J1 byte and the other VC-4 bytes. The pointer tracking state machine is compliant with the ETSI state machine specified in the ETSI 1015 document. A logic diagram of the state machine is shown in Figure 22. No additional states or transitions have been added to the pointer state machine.

For North American applications, a control bit is provided for disabling the AIS to LOP transition, which is shown as a dotted line in Figure 22. This transition is disabled by writing a 1 to control bit PADS (bit 1 in 18H). In addition, control bits are provided which permit the value of the S-bits (H1 byte) in the pointer tracking machine to be disabled, equal to 10, or to a microprocessor-written value.

The following table lists the control states associated with the SS-bits.

RPSDS	RPSSEL	Action
0	0	Pointer tracking machine uses 10 as the SS-bit value in the state machine.
0	1	Pointer tracking machine uses microprocessor-written value for SS-bit check in state machine.
1	X	SS-bit check in pointer tracking machine disabled. Pointer tracking machine ignores the SS-bits in the transition state definitions.

Path AIS and loss of pointer alarms are provided. In addition, pointer increments, decrements, and NDFs are counted in 8-bit performance counters.

Upstream Receive AIS Indication

An upstream AIS indication can be provided for the L4M in one of two ways: using the E1 byte in the Transport Overhead bytes, or control lead indications. The upstream AIS indication can generate a 140 Mbit/s line AIS and transmit path RDI, when enabled. Writing a 0 to control bit EAPE enables using the E1 byte for the upstream AIS indication. For example, the TranSwitch SOT-3 generates an AIS signal (all ones) in the E1 byte when a loss of frame, loss of signal, loss of pointer, or line or path AIS are detected. The L4M uses majority logic (five out eight ones) to determine if the E1 byte has an AIS indication (E1AIS alarm). The first and subsequent indications indicate the alarm condition. Recovery occurs on the first indication that the E1 byte does not have an all ones (AIS) state. This indication is to be used by the L4M to generate a receive AIS indication and path RDI, when enabled.

When a 1 is written to the EAPE control bit it disables the detection of all ones in the E1 byte, and enables the ISTAT and PAIS leads. An active high on the ISTAT or PAIS lead causes the XISTAT and XPAIS alarms, and a 140 Mbit/s line AIS and path RDI when enabled.

Receive Path Overhead Byte Processing

The Path Overhead bytes consist of the J1, B3, C2, G1, F2, H4, Z3, Z4, and the Z5 bytes. All POH bytes are provided at the external POH interface, including the B3 byte. The POH bytes are also written into the L4M memory map for a microprocessor read cycle.

Path Overhead Byte Processing is inhibited (and functions reset) when an active low is placed on the $\overline{\text{POHDIS}}$ lead (pin 19). POH processing (for C2 and J1) is also inhibited when any of the following alarms are detected:

- Drop Bus of the J1 pulse (DBLOJ1) when the PTEN pin is low
- Drop Bus loss of clock (DBLOC)
- E1AIS detected (E1AIS) when EAPE control bit is 0
- PAIS Alarm pin equal to 1 (XPAIS alarm) when EAPE control bit is 1
- ISTAT Alarm pin equal to 1 (XISTAT alarm) when EAPE control bit is 1
- Receive loss of pointer (RLOP) when PTEN pin is high
- Receive path AIS (RPAIS) when PTEN pin is high

Receive J1 Byte Processing

There are two possible received J1 message sizes, 16 bytes (ITU-T), or 64 bytes (ANSI). The L4M is capable of dimensioning the transmit (and receive) RAM memory segment to the two sizes (16-Byte or 64-Byte). In addition, two modes of operation are provided for the 16-byte (ITU-T) format: a microprocessor read mode, and a compare read mode. The following table lists the various control states associated with J1 processing.

CCITT	J1COM	Action
0	X	Transmit and receive J1 segments are configured for the 64-byte J1 message size. No relationship is required between the memory segment and the message written for transmission or for the message received.
1	0	Transmit and receive J1 segments are configured for the 16-byte J1 message size. No relationship is required between the memory segment and the message written for transmission or the message received.
1	1	Transmit and receive J1 segments are configured for the 16-byte J1 message size. No relationship is required between the memory segment and the message written for transmission. For the receive J1 bytes, a 16-byte microprocessor message is written into a 16-byte segment for comparison against the received message. The written message must start with the multiframe indicator written into the starting location of the segment. The L4M does not perform the CRC check in the 16-byte message.

The ITU-T defined 16-byte message consists of an alignment signal of (10000000 00000000) in the most significant bit (bit 1) of the message. The remaining 7 bits in each frame consists of a data message, as illustrated below.

Bit	1	2	3	4	5	6	7	8
	1	16-Byte J1 Message						
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							

ITU-T 16-Byte J1 Message Format

The J1 16-byte message comparison works according to the following steps:

1. Assume that the L4M J1 detector is out of lock, and there is no mismatch alarm.
2. A 16-byte reference message is written into the memory map by the microprocessor.
3. The incoming message is received, and the J1 comparison circuit searches for the multiframe pattern (1000...0 pattern).
4. Multiframe is found.
5. The incoming (received) 16-byte message is then checked for three consecutive 16-byte message repeats.
6. If an error occurs before step 5 is completed, the sequence repeats, starting at step 3.
7. If the incoming 16-byte message repeats three times in row (after the multiframe is detected) without an error, the internal memory map segment is updated. This is an in-lock condition, and the J1 Loss of Lock alarm is reset.
8. This stable message is compared against the microprocessor-written message, byte for byte for 16-bytes (the length of the multiframe message). If they compare, a match is declared. No mismatch alarm. If they do not compare a mismatch alarm is declared. A J1 mismatch alarm results in RDI and AIS being sent continuously, when enabled. There is no out-of-lock alarm because the received message is stable.
9. If the microprocessor-writes a new byte, a J1 Trace Identifier Mismatch (J1TIM) alarm will also occur because the receive message is stable but there is mismatch between the two locations. A mismatch alarm is declared, and RDI and AIS are sent continuously, when enabled. There is no out-of-lock alarm because the received message is stable.
10. If the receive message changes for three consecutive 16-byte messages, an out of lock alarm occurs. However, the mismatch alarm resets.
11. The sequence repeats.

When the J1 is not in lock (J1 lock equal to 0), a J1 loss of lock alignment alarm (J1LOL) is declared. This process is inhibited and reset during an incoming AIS condition.

Receive C2 Byte

The L4M provides C2 signal label mismatch detection between the received C2 byte, and a microprocessor-written value and also a fixed 01H value in hardware, when enabled. When control bit C2FVD is written with a 1, the detection of the 01 value is disabled, and detection depends solely on the register value written by the microprocessor. Five or more consecutive mismatched signal labels in the C2 byte from the microprocessor-written value or a label not equal to the 01H (when C2FVD=0) results in a path signal label error (PSLERR) alarm. The alarm state is exited when five or more consecutive matches, or the 01H value (when C2FVD=0) are received correctly.

The L4M also provides an unequipped indication (C2EQ0) when the incoming C2 byte matches an internal 00H value for five consecutive frames. The alarm is exited when the C2 byte does not equal a 00H value for five or more consecutive frames. Please note that if the accepted path signal label value is all zeros (C2 unequipped), or an 01 (if C2FVD=0), a mismatch alarm (PSLERR) is not declared.

The C2 mismatch detection and unequipped indication are disabled when any of the following alarms are detected.

- Loss of Drop Bus J1 Pulse (DBLOJ1) when the PTEN pin is low
- E1 AIS (E1AIS) (from the Drop bus) when EAPE is 0
- ISTAT is a 1 when EAPE is 1
- PAIS is a 1 when EAPE is 1
- Receive loss of pointer (RLOP) when the PTEN pin is high
- Receive path AIS (RPAIS) when the PTEN pin is high

Receive G1 Byte

The received states of the G1 byte are provided for a microprocessor read cycle, and are also provided at the path overhead byte interface, for external processing as required.

Bits 1 through 4 in the G1 byte convey a FEBE count. There are nine possible valid FEBE values, 0 through 8. Other values are detected as a zero count. The FEBE value received is the count of interleaved bit blocks that have been detected in error in the received Path BIP-8 code at the far end. A 16-bit counter is provided for counting the number of FEBE bits or blocks received in error. Up to eight errors per frame may be counted.

Bit 5 is the defined as the Path Far End Receive Defect Indication alarm (Path RDI) indication. A receive path RDI alarm indication (RRDI) occurs when the L4M detects a one for five or ten consecutive frames. Recovery occurs when the L4M detects a zero for five or ten consecutive frames. Writing a 1 to control bit RDI10 selects the detect and recovery value of 10 consecutive events.

Bits 6, 7, and 8 in the G1 byte are unassigned and are normally received as 0s. They are provided for both a microprocessor read cycle and at the external POH interface.

Receive Desynchronizer

The rate at which the pointer leak buffer is to be leaked is written to the 15-bit pointer leak rate register.

If enhanced desynchronizer operation is required, the following additional signals are provided: a stuff indication lead, positive and negative justification indications, and a pointer leak counter equal to zero indication lead. For controls, a LOADEN control bit and a 9-bit (plus sign bit) pointer offset counter are provided, in addition to the 15-bit pointer leak rate register.

Receive 140 Mbit/s Line AIS Generation

The L4M provides two techniques for generation of line AIS. The first approach uses an external clock, and the second approach uses a bit stuffing technique. The use of an external stable clock for AIS permits the receive performance monitoring circuit to be used (i.e., Receive AIS Detector and Receive Frame Alignment Detector), while the bit stuffing AIS approach disables the receive performance monitoring circuit when the L4M is generating a receive line AIS. Line AIS is defined as all ones in the data signal. In addition, in the receive direction, when BSAISE=1 line AIS cannot be generated when the drop bus clock is lost, since this clock is required for generating line AIS. When the bit stuffing AIS approach is not used and the L4M generates an RXAIS signal, the external PLL will lose lock. In this case the AISIND pin can be used with some external logic to cause the external 139.264 MHz VCXO to lock onto the AIS clock to maintain proper synchronization of the 139.264 MHz VCXO clock.

Using an external clock for AIS generation is enabled by writing a 0 to control bit BSAISE (bit 0 in 1CH). Please note that control bit BSAISE is 0 upon power-up. The AIS clock is either 17.408 MHz for byte operation, or 34.816 MHz for nibble operation. The AIS clock is monitored for operation and an alarm indication (LAISC) provided when this clock is not functioning. Loss of AIS clock also prevents the L4M from generating a line AIS in either the transmit or receive directions. When the L4M is required to generate either a transmit or receive line AIS the external AISCK clock input is used as the timebase.

The bit stuffing approach does not require an external clock. The capability to generate line AIS on alarm indications is enabled by writing a 1 to control bit BSAISE. In the transmit direction, line AIS is generated by bit stuffing 7/9 of the time using an all ones pattern for data. The actual technique consists of performing stuffing for the first four rows of the 9 subframes (CCCCC=1, and the S-bit is 0). Frequency justification is performed for row 5, bit stuffing for rows 6, 7, and 8, followed by frequency justification for row 9. In the receive direction, the approach is the same, bit stuffing is multiplexed into the format prior to the desynchronizer.

In the transmit direction, line AIS cannot be transmitted when the drop clock is lost in the drop bus timing modes, in the add bus timing mode when the add bus clock is lost, or when the external clock is lost in the external timing mode.

Receive and Transmit Performance Monitoring

The L4M provides 139.264 Mbit/s receive and transmit performance monitoring. Performance monitoring includes frame alignment, providing the status of the remote indication alarm bit, counting framing errors and, when enabled, works in conjunction with the AIS detector circuits.

The L4M monitors the receive and transmit data for frame alignment as specified in ITU-T Recommendation G.751. The frame structure consists of 2928 bits, starting with bit 1. The frame alignment pattern is carried in bits 1 through 12, and has the following frame alignment pattern: 111110100000. After frame alignment, a 16-bit performance counter counts the number of errored frames (one or more bits in the frame alignment pattern is in error) in both the transmit and receive directions. In addition, the status of the distant alarm indication (bit 13 in the format) is provided. A 1 causes a TDAI alarm (bit 5 in 28/29H), or a RDAI alarm (bit 4 in 28/29H), and an interrupt if the mask bit is enabled, and the hardware interrupt is enabled. No other action is taken upon detection of Distant Alarm Indication. An enable bit (LFAISE) is provided to generate a 140 Mbit/s AIS, when loss of frame alignment is detected. The frame alignment detection can be coupled with the AIS recovery circuit by setting the FDAEN control bit to 1.

In the receive direction, the performance monitoring circuit (i.e., Receive AIS Detector and Receive Frame Alignment Detector) is disabled when the bit stuffing AIS feature is enabled and the L4M is generating a receive line AIS; also, the receive frame error counter is inhibited on a RLOF alarm or DBLOC alarm and the transmit frame error counter is inhibited on a TLOF alarm.

Transmit Unequipped Channel Generation

The L4M provides the capability of generating an unequipped channel or a supervisory unequipped channel. The following table lists the control bit states for generating the two types of unequipped channels and the priority associated with path AIS.

TUNEQ	POHEUQ	PAISG	Action
0	X	0	Normal Operation
1	0	0	Transmit Unequipped channel. POH bytes and payload bytes are equal to zero.
1	1	0	Transmit supervisory unequipped channel. POH are transmitted (if enabled). Payload bytes are transmitted as zero.
X	X	1	Transmit path AIS. POH (when enabled) and payload bytes transmitted as 1.

Transmit POH Bytes

The insertion of the transmit POH bytes is enabled by placing a high on the signal lead labeled $\overline{\text{POHDIS}}$ (pin 19). This signal lead has priority over the control bits such as the POH enable control bit for unequipped status (POHEUQ). When an active low is placed on this pin, the insertion of POH bytes into the SPE is disabled. However, the POH RAM locations may still be written to by the microprocessor. The starting location of the payload (without the POH bytes) will be still determined by the J1 pulse (add bus timing), or at the 0 or 522 location (drop bus or external timing modes), determined by the SVC4H control bit.

When enabled ($\overline{\text{POHDIS}}$ is high), the L4M has the capability of inserting the Path Overhead bytes from RAM locations, or from an external POH interface (except the B3 byte). The individual RAM locations are allowed to be updated during operation.

The L4M is also equipped with a control bit (POHRAM) that permits the Path Overhead bytes (except the B3 byte) from the transmit POH interface (when selected) to be written into common RAM locations (or microprocessor-written values) in addition to being transmitted. The following are the control states associated with the POHRAM and EXbn control bits.

POHRAM	EXbn	Action
1	1	The external interface POH byte that is selected is transmitted and is also written into RAM. For example, when EXF2 is a 1, the external interface F2 byte is transmitted and written into the RAM each frame.
0	1	The external POH byte that is selected is transmitted. The microprocessor can write a value to RAM as required. For example, when EXF2 is a 1, the external interface F2 byte is transmitted each frame, but is not written to the RAM location.
X	0	Microprocessor-written POH byte is transmitted, except B3 and G1 bytes. See RING, FEBEEN and RDIEN control bits for more information.

This feature allows the microprocessor to read selected transmitted POH interface bytes prior to transmission for test purposes. In addition, this feature permits the user to switch back and forth between a selected POH I/O byte and the RAM location, without having to reinitialize the RAM POH byte locations during switch-over.

Transport (Section) Overhead Bytes

The L4M provides an option in the drop bus and external timing modes to provide selected Transport (Section) Overhead Bytes. This feature is selected by writing a 1 to control bit TOHOUT (bit 5 in 14H). The selected TOH bytes are the six A1 and A2 framing bytes, C1 byte, and the H1 and H2 pointer bytes (including Y and 1s pointer bytes). The A11, A12, and A13 bytes are equal to F6H, while A21, A22, and A23 are equal to 28H. When control bit UPC1 is a 0, the value 01H is transmitted as the C1 byte. When UPC1 is a 1, the microprocessor-written value in 17H is transmitted as the C1 byte.

The pointer values H1 and H2 correspond to H11 and H21 in the AU-4 pointer (H11, H12, H13, H21, H22, H23), as illustrated below. The H11 and H21 bytes carry the pointer value that corresponds to 522 or 0, depending on the state of the SVC4H control bit. The H12 and H13 bytes carry the value 1001ss11. The H22, and H23 bytes are specified as all ones.

H11	H12	H13	H21	H22	H23
NNNNSSID	1001ss11	1001ss11	IDIDIDID	11111111	11111111

Note: NNNN is equal to 0110.

When control bit TPSSEL is a 0, the SS-bits are transmitted as a 10, while the SS-bits in H12 and H13 are undefined and are transmitted as 00. When a 1 is written into the transmit pointer S-bit select control bit TPSSEL, the microprocessor is able to program the SS and ss bits. Register 1DH has the following structure:

Bit	7	6	5	4	3	2	1	0
	TS	TS	Ts	Ts	Ts	Ts	RS	RS
	Transmit H11		Transmit H12		Transmit H13		Receive H11	

Transmit C1 Reference Delay (External Timing Mode Only)

When the external timing mode is selected, and control bit TC1DC (bit 3 in 16H) is written with a 1, a 12-bit register location (19H and 18H) is enabled which can compensate for up to 2429 positions (270 columns x 9 rows) for the external C1 reference pulse. For example, if a binary 0 is written into the 12-bit register by the microprocessor, the external C1 pulse (in EXC1) is in the C11 time slot (the correct time slot). When the binary value of 1 is written into the 12-bit register, it is assumed that the C1 pulse is shifted one time slot (one clock cycle) into the time slot that corresponds to C12 byte. This means that the starting point for the transmit frame reference should be one byte earlier. Values written into the 12-bit register other than 2429 will be counted with a delay equal to 0.

Add Bus C1 Input/Output Pulse

When control bit AC1EN is a 1, in the drop timing mode and external timing modes, the C1 indicator pulse is provided as a separate output lead (AC1) instead of being in the C1J1 signal. In this mode, the C1J1 signal will carry the J1 pulse only. In the add bus timing mode, the AC1 lead is or-gated with the AC1J1 signal to form a composite internal C1J1 signal. The AC1 option is selected using the states defined in the table below:

AC1EN	AC1 pin	Action
0	Low	Normal operation. Pin is grounded. C1 is provided in the AC1J1 signal.
1	C1 pulse	In the drop timing and external timing modes, C1 is provided as a separate output signal. The AC1J1 signal contains the J1 signal only. In the add bus timing mode, the C1 signal may be provided in the AC1J1 signal or as a separate signal.

Test Generator and Analyzer

The L4M is equipped with a transmit test generator and receive analyzer. A simplified block diagram of the test generator and analyzer is shown in Figure 23 below. The transmit clock (TXC) must be present in order for the 2^{23}-1 test generator to function. The test generator sequence is specified in ITU-T recommendation O.151. The test generator is enabled by writing a 1 to control bit TGEN (bit 2 in 14H). The byte or nibble transmit input is disabled and the test sequence is enabled. The test generator can be also be enabled when the L4M is in line loopback. The 2^{23}-1 test analyzer samples the receive data for operation. The test analyzer is enabled by writing a 1 to control bit ANAEN (bit 1 in 14H). The test analyzer monitors the incoming test sequence for lock, using consecutive 1000-bit blocks (not a sliding window). An out of lock alarm (ANOOL) is detected when 30 bits in a 1000-bit sequence are detected in error. Recovery occurs when the first 24 bits in the test sequence match. Errors are counted in a 16-bit performance counter (locations 44 and 45H). The counter is inhibited when out of lock or when the analyzer is disabled.

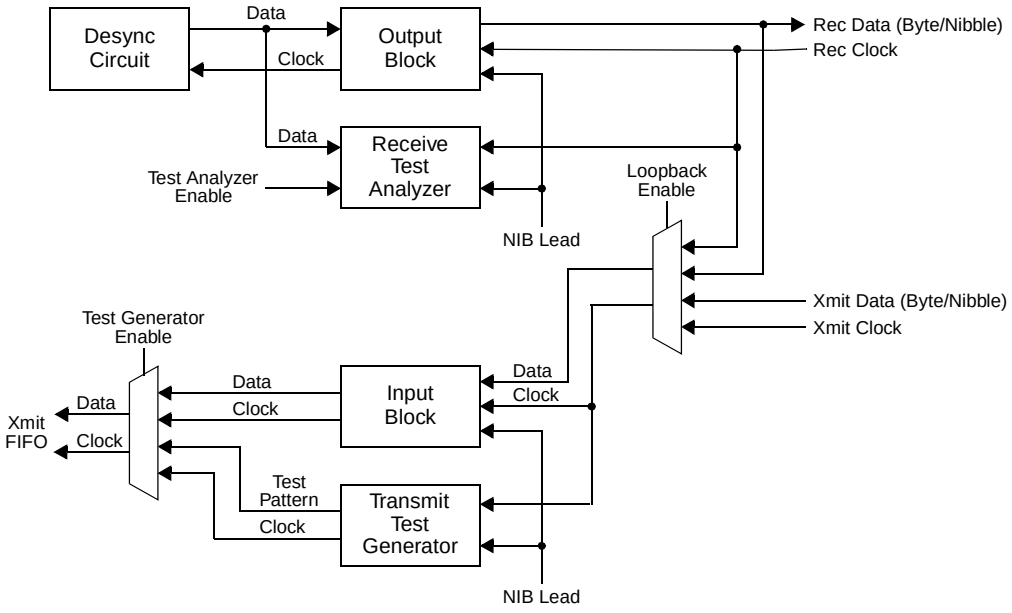


Figure 23. Test Generator, Analyzer and Loopback

Performance Counters

All 16-bit performance counters have a special 16-bit read operation which allows uninterrupted access, without the danger of one byte changing while the other byte is read. To perform a 16-bit read operation, the low order byte is read first. The read operation freezes the count in the high order byte. The high order byte should be read next.

All the performance counters can also be configured to be either saturating or non-saturating. When a 0 is written to control bit COR (bit 0 in 13H), the performance counters are configured to be saturating, with the counters stopping at their maximum count. An 8-bit or 16-bit counter is reset on a microprocessor read cycle. Counts that occur during the read cycle are held, and the counter updated afterwards. When a 1 is written to control bit COR, the performance counters are configured to be non-saturating, and roll over after the maximum count in the counter is reached. In this mode, the counters do not clear on a microprocessor read cycle, but continue to count.

All the performance counters can be reset simultaneously by writing a 1 to control bit RSETC (bit 7 in 1CH). This bit is self clearing, and does not require the microprocessor to write a 0 into this location afterwards. In addition, a performance counter can also be cleared by writing the value of 00H to the low byte, immediately followed by writing a 00H to address n+1. The n+1 address location contains the high order byte of the 16-bit performance counter.

All performance counters (except the Receive Framing Error counter and the Transmit Framing Error counter) are inhibited when any of the following alarms occur, and released for operation after the last alarm clears.

- Loss of Drop Bus J1 pulse (DBLOJ1) when PTEN pin is low.
- Receive loss of pointer alarm (RLOP) when PTEN pin is high.
- Receive path AIS alarm (RPAIS) when PTEN pin is high.
- Loss of Drop Bus Clock (DBLOC).
- E1 byte AIS Detected (E1AIS) when external alarm enable (EAPE) control bit is 0.
- External alarm ISTAT pin is high (XISTAT) when external alarm enable (EAPE) control bit is 1.
- External alarm PAIS pin is high (XPAIS) when external alarm enable (EAPE) control bit is 1.
- J1 loss of lock (J1LOL) alarm and control bit J1LEN is a 1 (and $\overline{\text{POHDIS}}$ is a 1).
- J1 trace identifier mismatch (J1TIM) alarm and control bit J1TEN is a 1 (and $\overline{\text{POHDIS}}$ is a 1).
- Received active low on the external AIS lead (XAIS alarm).
- Path Signal Label Enable control bit (PSLER) is a 1, and either a PSLERR or C2EQ0 alarm occurs.

The receive framing counters and transmit framing counters are inhibited on loss of frame alignment.

Boundary Scan

Introduction

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the L4M device's interface pins. The Boundary Scan Block consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan path bordering the input and output pins. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) and a Test Data Output (TDO) output signal.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the L4M device's internal logic, as illustrated in Figure 24. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 21.

Boundary Scan Support

The maximum frequency the L4M device will support for boundary scan is 10 MHz. The L4M device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the L4M device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external L4M input and output leads.

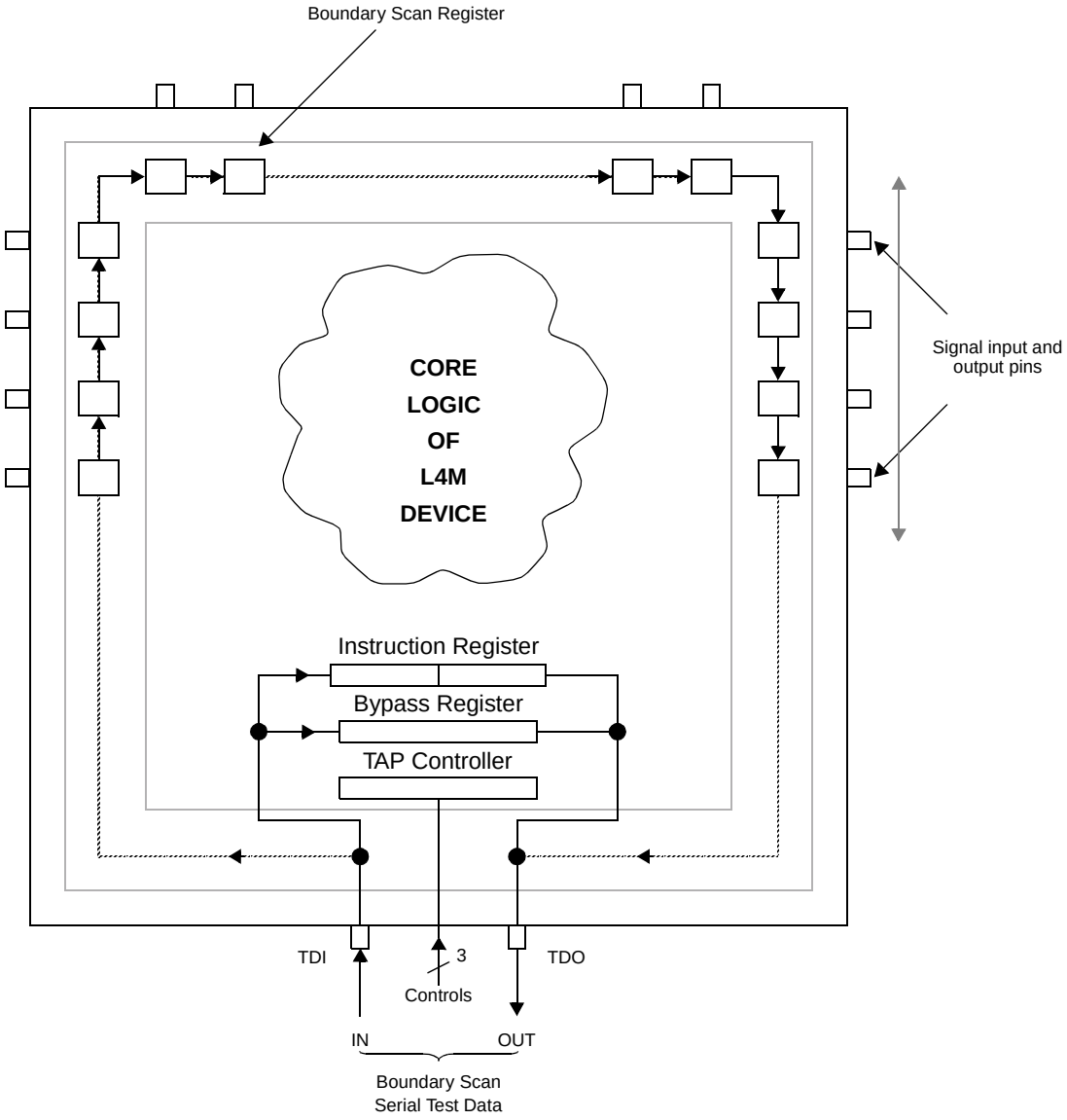
SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the L4M device remains fully operational. While in this test mode, L4M input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the L4M device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

Figure 24. Boundary Scan Schematic



Boundary Scan Chain

There are 124 scan cells in the L4M boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
1	Input	104	TEST	Should be set to 0.
2	Input	105	EXC1	
3	Output	107	TOCHC	
4	Output	108	AD0	
5	Output	109	AD1	
6	Output	110	AD2	
7	Output	111	AD3	
8			$\overline{\text{GZADB}}$	Output enable for AD0...AD7
9	Output	113	AD4	
10	Output	114	AD5	
11	Output	115	AD6	
12	Output	116	AD7	
13	Output	117	$\overline{\text{ADD}}$	
14	Output	119	APAR	
15			$\overline{\text{GZBIDA}}$	Output enable for AC1, ACLK, ASPE, and AC1J1. 0=Output, 1=Input
16	Bidirectional	120	AC1	
17	Bidirectional	121	ACLK	
18	Bidirectional	122	ASPE	
19	Bidirectional	123	AC1J1	
20	Input	125	EXTC	
21	Input	126	DC1	
22	Input	127	DC1J1	
23	Input	128	DPAR	
24	Input	129	DSPE	
25	Input	131	DCLK	
26	Input	132	TEST	Should be set to 0.
27	Input	133	DD0	
28	Input	134	DD1	
29	Input	135	DD2	
30	Input	137	DD3	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
31	Input	138	DD4	
32	Input	139	DD5	
33	Input	140	DD6	
34	Input	141	DD7	
35	Output	143	PLEQ0	
36	Input	144	TEST	
37	Input	1	$\overline{\text{RESET}}$	
38	Input	2	PTEN	
39	Input	3	TEST	Should be set to 0.
40	Output	5	ROCHC	
41	Output	6	ROCHD	
42	Output	7	RAIPD	
43	Output	8	RPOHD	
44	Output	9	RPOHF	
45	Output	11	RPOHC	
46			HIGHZE	HI-Z enable. set to 0 to not tri-state.
47			$\overline{\text{GZOSHARED}}$	Output enable for PJ. 0=Output, 1=Input
48	Output	13	PJ	
49	Output	14	CTRL	
50	Output	15	$\overline{\text{CTRL}}$	
51	Input	17	$\overline{\text{EXAIS}}$	
52	Input	18	$\overline{\text{HIGHZ}}$	
53	Input	19	$\overline{\text{POHDIS}}$	
54			$\overline{\text{GZBDSHARED}}$	Output enable for NJ. 0=Output, 1=Input
55	Bidirectional	20	NJ	
56	Input	21	RXCI	
57			$\overline{\text{GZRXCO}}$	Output enable for RXCO.
58	Output	23	RXCO	
59	Output	24	$\overline{\text{AISIND}}$	
60	Output	25	RXD0	
61	Output	26	RXD1	
62	Output	27	RXD2	
63	Output	29	RXD3	
64			$\overline{\text{GZRXDC}}$	Output enable for RXD0...RXD1

Scan Cell No.	I/O	Pin No.	Symbol	Comments
65	Output	30	RXD4	
66	Output	31	RXD5	
67	Output	32	RXD6	
68	Output	33	RXD7	
69	Input	35	DROPT	
70	Input	36	ENABT	
71	Input	37	ISTAT	
72	Input	38	PAIS	
73	Input	39	STAI	
74	Bidirectional	41	D0	
75	Bidirectional	42	D1	
76	Bidirectional	43	D2	
77	Bidirectional	44	D3	
78			$\overline{\text{GZDUP}}$	Output enable for D0...D7. 0=Ouput, 1=Input.
79	Bidirectional	45	D4	
80	Bidirectional	47	D5	
81	Bidirectional	48	D6	
82	Bidirectional	49	D7	
83	Output	50	INT/$\overline{\text{IRQ}}$	
84			$\overline{\text{GZRDY}}$	Output enable for RDY/$\overline{\text{DTACK}}$
85	Output	51	RDY/$\overline{\text{DTACK}}$	
86	Input	53	RAMCI	
87	Input	55	$\overline{\text{SEL}}$	
88	Input	56	$\overline{\text{RD}}$	
89	Input	57	$\overline{\text{WR}}$	
90	Input	59	$\overline{\text{AS}}$	
91	Input	60	MADBUS	
92	Input	61	A0	
93	Input	62	A1	
94	Input	63	A2	
95	Input	65	A3	
96	Input	66	A4	
97	Input	67	A5	
98	Input	68	A6	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
99	Input	69	A7	
100	Input	71	AISCK	
101	Output	72	STUFF	
102	Input	73	MOTO	
103	Input	74	NIB	
104	Input	75	TXD0	
105	Input	77	TXD1	
106	Input	78	TXD2	
107	Input	79	TXD3	
108	Input	80	TXD4	
109	Input	81	TXD5	
110	Input	83	TXD6	
111	Input	84	TXD7	
112	Input	85	$\overline{\text{EXLOS}}$	
113	Input	86	TEST	Should be set to 0.
114	Input	87	TXC	
115	Input	89	TEST	Should be set to 0.
116			$\overline{\text{GZSCAN}}$	Output enable for TESTS.
117	Output	91	TEST	Should be set to 0.
118	Output	92	TPOHF	
119	Output	93	TPOHC	
120	Input	95	TPOHD	
121	Input	96	TAIPD	
122	Input	97	TOCHD	
123	Input	98	TAIPF	
124	Input	99	TAIPC	

EXTERNAL DEVICE OPERATION

Phase-Locked Loop

The phase-locked loop (PLL) circuit for the L4M is shown in Figure 25. The bandwidth (BW Hz) of the PLL is given by the following equation.

$$BW = K_d K_o K_h / 2\pi$$

where,

$Ko = (30ppm/v) \times (139.264\ Hz/ppm) \times (2\pi)$

$Kd = 5v/[(2\pi) \times (256)]$

$Kh = 39/[2 \times (15 + 36/2)] = 0.591$

The bandwidth of the PLL is equal to 7.7 Hz.

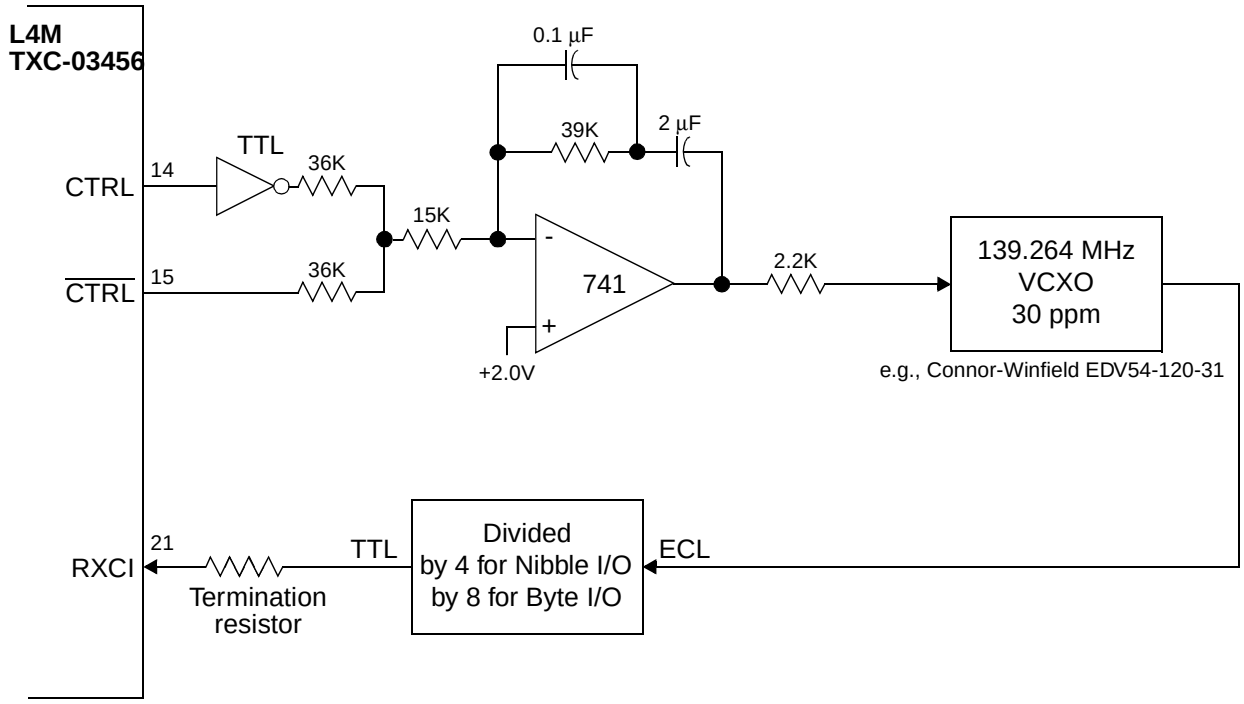


Figure 25. Phase-Locked Loop

To ensure that the L4M meets the jitter performance outlined in the ETS1015 document, an adaptive FIFO leak rate algorithm must be employed to dynamically adjust the value written to the FLR register (1AH). An application note on this subject entitled “Jitter Test results for the L4M device - Application Note”, document number TXC-03456-0001-AN, Edition 1.0, February 7, 1995 is available upon request.

140 Mbit/s Line Interface

Figure 26 is a simplified view of the 140 Mbit/s line interface. The NIB control lead selects whether the receive and transmit line interface is nibble- or byte-wide. The AIS clock (AISCK) should be connected to a stable 34.816 MHz frequency source for nibble interface operation, or to a 17.408 MHz frequency source for byte interface operation. The AIS indication lead ($\overline{\text{AISIND}}$) provides an external indication when AIS is generated.

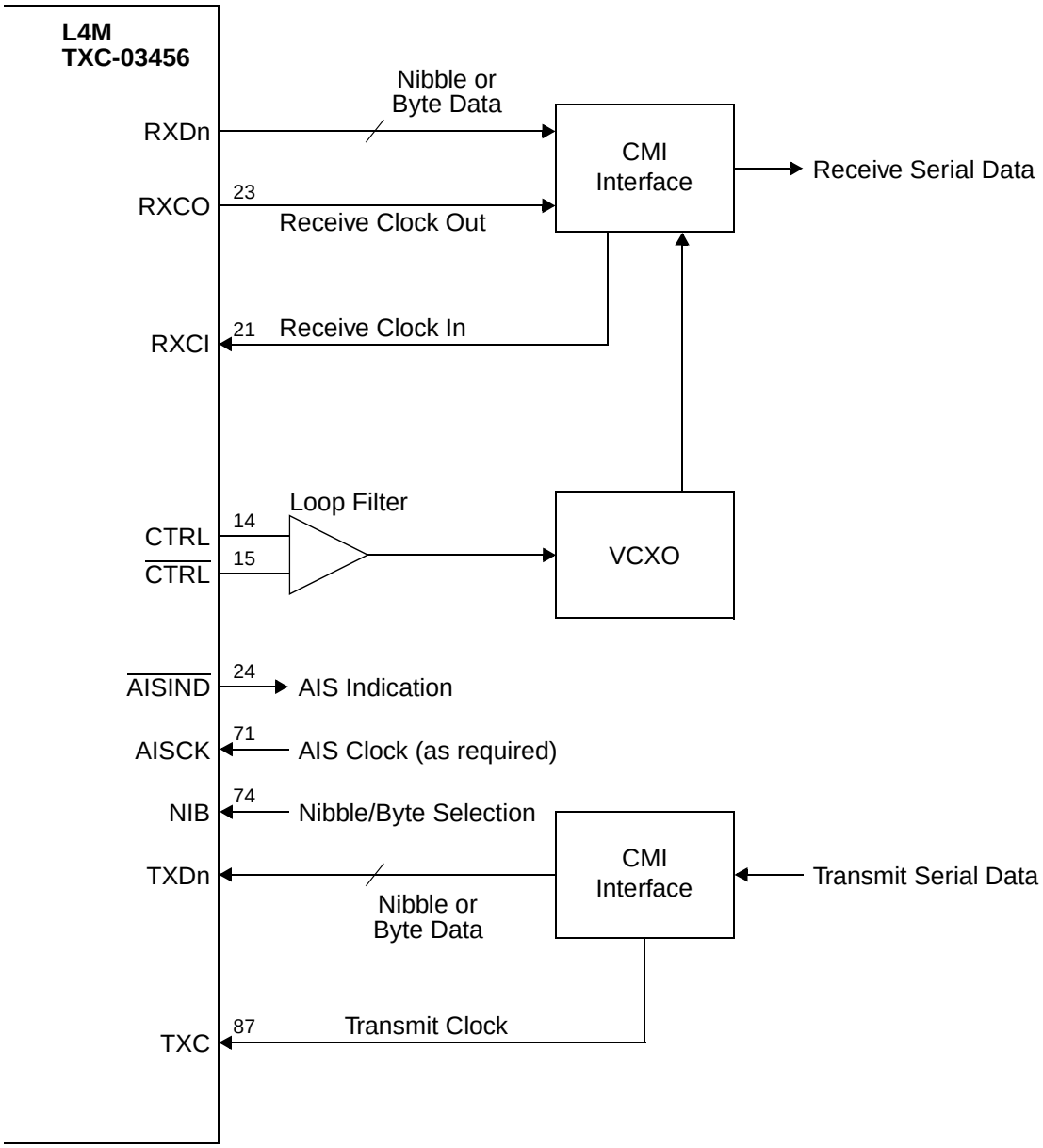


Figure 26. L4M 140 Mbit/s Line Interface

Ring Configuration

Figure 27 shows two L4M devices arranged in a ring configuration. The two L4Ms exchange path FEBE and RDI information using the alarm indication port. The receive alarm indication port clock and framing pulse are shared with the receive POH byte interface clock and framing pulse signals. This feature is disabled when an active low is placed on the $\overline{\text{POHDIS}}$ lead. Data (RAIPD), as a repetitive byte, is clocked out of the L4M using the path overhead interface clock (RPOHC). The path overhead frame pulse RPOHF indicates the start of the repetitive data byte (RAIPD).

In normal operation, receive alarm indication port data (RAIPD) is connected to its mate transmit alarm indication port (TAIPD). The receive clock (RPOHC) is connected to transmit clock TAIPC at its mate, and the receive framing pulse RPOHF is connected to the transmit frame pulse input (TAIPF). Likewise, the mate L4M's receive data is connected to the transmit alarm interface port. The clock present at TAIPC is monitored for operation. An alarm indication port loss of clock alarm causes the FEBE count to be transmitted as 0, and RDI to be transmitted as 0. Writing a 1 to the RING control bit selects the ring mode of operation.

The alarm indication byte is sent in the following way:

Bits 1-4	Bit 5	Bit 8		
B3 Count	Path RDI	0	0	1

The byte is repeated nine times.

The information sent via the alarm indication port is:

- FEBE count
- Path RDI/FERF Indication whose value is set by:
    - Received active low on the external AIS lead (XAIS alarm).
    - Received E1 byte indication (E1AIS), and control bit EAPE is a 0.
    - External ISTAT Pin (XISTAT) alarm, when control bit EAPE is a 1.
    - External PAIS Pin (XPAIS) alarm, when control bit EAPE is a 1.
    - Drop bus loss of J1 (DBLOJ1) when PTEN is low.
    - Receive loss of pointer (RLOP) alarm when PTEN is high.
    - Receive path AIS (RPAIS) alarm when PTEN is high.
    - Path Signal Label Enable control bit (PSLEN) is a 1, and either a PSLERR or C2EQ0 alarm occurs.
    - Control bit J1TEN is a 1, and a J1TIM alarm occurs.
    - Control bit J1LEN is a 1, and a J1LOL alarm occurs.

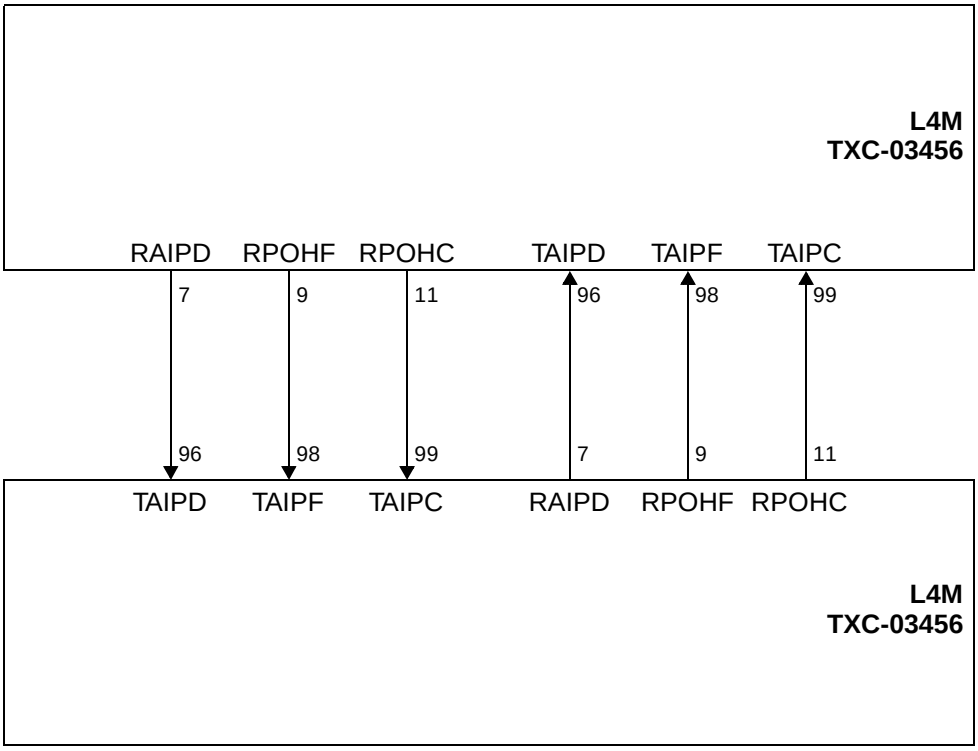


Figure 27. Use of Two L4M Devices in Ring Configuration

Overhead Communication Channel Interface

The 139.264 Mbit/s format has ten overhead communication channel bits ("O"-bits) per subframe or 90 bits per frame. The "O"-bit receive and transmit interfaces are treated as an asynchronous serial data communications channel.

In the transmit direction, the "O"-bit interface consists of an output clock (TOCHC) and data input lead (TOCHD). Data is clocked into the 140 Mbit/s Mapper on positive transitions of the clock. The clock is non-symmetrical.

In the receive direction, the interface consists of an output clock (ROCHC) and data output signal (ROCHD). Data is clocked out of the L4M on negative transitions of the clock. The clock is non-symmetrical.

Path Overhead Interface

In the transmit direction, timing is provided for clocking in the nine POH bytes. The insertion of POH data from the POH interface is disabled when an active low is placed on the $\overline{\text{POHDIS}}$ lead. When enabled, the transmit POH interface B3 byte position is masked out by the L4M. A B3 test byte may be written by the microprocessor into the L4M RAM and transmitted in place of the calculated B3 byte, or it may function as a B3 error mask. A transmit non-symmetrical clock (TPOHC) and framing pulse (TPOHF) are provided for sourcing the Path Overhead bytes (TPOHD) from the external circuitry. The framing pulse is one clock cycle wide and occurs in the first bit time of the J1 byte.

In the receive direction all nine Path Overhead bytes are clocked out at the POH interface. The receive timing is asynchronous in relationship to transmit timing. A receive clock (RPOHC) and framing pulse (RPOHF) are provided for outputting the Path Overhead bytes (RPOHD) for external circuitry. The framing pulse is one clock cycle wide and occurs in the first bit time of the J1 byte.

MEMORY MAP

The following definitions are used for the microprocessor access modes of the memory address locations in the tables below: R/W (read/write), R (read only), R(L) (read latched bit position).

CONTROL BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	R/W	TINVC	TLAIS	RING	EXOB	TESTB3	XRDIEN	POHEUQ	ADDZ
11	R/W	PSLEN	RDIEN	TRDI	FEBEEN	EAPE	RAISEN	RAISG	RINVC
12	R/W	EXZ5	EXZ4	EXZ3	EXH4	EXF2	EXG1	EXC2	EXJ1
13	R/W	J1COM	CCITT	TUNEQ	POHRAM	LHZ	LLBK	SLBK	COR
14	R/W	EAISEN	TCAISEN	TOHOUT	J1LEN	J1TEN	TGEN	ANAEN	SVC4H
15	R/W	LFAISE	FDAEN	TPSSEL	RPSDS	RPSSEL	FBTOZ	C2FVD	UPC1
16	R/W	Transmit C1 Offset 2048	1024	512	256	TC1DC			PAISG
17	R/W	Transmit C1 Offset 128	64	32	16	8	4	2	1
18	R/W	Receive C1 Offset 2048	1024	512	256	RC1DC	RDI10	PADS	FEBEBC
19	R/W	Receive C1 Offset 128	64	32	16	8	4	2	1
1A	R/W	FIFO Leak Rate Register							
1B	R/W	FIFO Leak Rate Register							LOADEN
1C	R/W	RESETC	RESETD	RESETS			PARDO	AC1EN	BSAISE
1D	R/W	TS	TS	Ts	Ts	Ts	Ts	RS	RS
1E	R/W	Bit 1----------Transmit C1 Value----------Bit 7							
1F	R/W								PLDINV

STATUS BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	R	ANOOL	TLAISD	TFIFOE	ABLOJ1	LAISC	XAIS	DBLOJ1	E1AIS
21	R(L)	ANOOL	TLAISD	TFIFOE	ABLOJ1	LAISC	XAIS	DBLOJ1	E1AIS
22	R	BUSERR	RFIFOE	RRDI	PSLERR	C2EQ0	J1LOL	J1TIM	RLAISD
23	R(L)	BUSERR	RFIFOE	RRDI	PSLERR	C2EQ0	J1LOL	J1TIM	RLAISD
24	R	TLOC	ABLOC	DBLOC	RLOC	1SFOU	XSTAI	XISTAT	XPAIS
25	R(L)	TLOC	ABLOC	DBLOC	RLOC	1SFOU	XSTAI	XISTAT	XPAIS
26	R	SINT	EXTLOS	AIPLOC			NEW		
27	R(L)		EXTLOS	AIPLOC			NEW		
28	R	TLOF	RLOF	TDAI	RDAI	RLOP	RPAIS		
29	R(L)	TLOF	RLOF	TDAI	RDAI	RLOP	RPAIS		

INTERRUPT MASK BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30	R/W	ANOOL	TLAISD	TFIFOE	ABLOJ1	LAISC	XAIS	DBLOJ1	E1AIS
31	R/W	BUSERR	RFIFOE	RRDI	PSLERR	C2EQ0	J1LOL	J1TIM	RLAISD
32	R/W	TLOC	ABLOC	DBLOC	RLOC		XSTAI	XISTAT	XPAIS
33	R/W	HINT	EXTLOS	AIPLOC			NEW		
34	R/W	TLOF	RLOF	TDAI	RDAI	RLOP	RPAIS		

TRANSMIT PATH OVERHEAD BYTES

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
68	R/W	B3 Test Mask and Test Byte Bit 1----------Bit 8							
69	R/W	C2 Signal Label (microprocessor or POH Interface) Bit 1----------Bit 8							
6A	R/W	Transmit FEBE Count (G1 Byte) Bit 1----------Bit 4				Transmit RDI	Unassigned Bit 6----------Bit 8		
6B	R/W	F2 byte (microprocessor or POH interface)							
6C	R/W	H4 byte (microprocessor or POH interface)							
6D	R/W	Z3 byte (microprocessor or POH interface)							
6E	R/W	Z4 byte (microprocessor or POH interface)							
6F	R/W	Z5 byte (microprocessor or POH interface)							
80 to BF	R/W	J1 Byte (64 or 16 bytes of RAM) Microprocessor or POH interface							

RECEIVE PATH OVERHEAD BYTES

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
75	R/W	C2 Microprocessor-Written Value for Mismatch Bit 1----------Bit 8							
78	R	B3 Received byte Bit 1----------Bit 8							
79	R	C2 Received byte Bit 1----------Bit 8							
7A	R	Received FEBE Count (G1 Byte) Bit 1----------Bit 4				Receive RDI/FERF	Unassigned Bit 6----------Bit 8		
7B	R	F2 byte (microprocessor read)							
7C	R	H4 byte (microprocessor read)							
7D	R	Z3 byte (microprocessor read)							
7E	R	Z4 byte (microprocessor read)							
7F	R	Z5 byte (microprocessor read)							
C0 to FF or C0 to CF	R	J1 Byte 64 bytes (or 16 bytes) Received Message Bit 1----------Bit 8							
F0 to FF	R/W	J1 Byte (16 bytes of RAM) J1 Microprocessor Written Value for Mismatch Bit 1----------Bit 8							

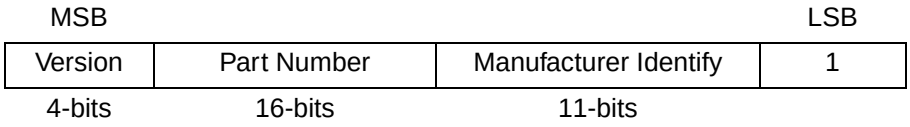
PERFORMANCE COUNTERS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40	R/W	B3 counter (low byte)							
41	R/W	B3 counter (high byte)							
42	R/W	FEBE counter (low byte)							
43	R/W	FEBE counter (high byte)							
44	R/W	Receive analyzer counter (low byte)							
45	R/W	Receive analyzer counter (high byte)							
46	R/W	Transmit framing pattern error counter (low byte)							
47	R/W	Transmit framing pattern error counter (high byte)							
48	R/W	Receive framing pattern error counter (low byte)							
49	R/W	Receive framing pattern error counter (high byte)							
4A	R/W	B3 Block Errors (8-bits)							
4B	R/W	Positive Justification Counter (8-bits)							
4C	R/W	Negative Justification Counter (8-bits)							
4D	R/W	NDF Counter							
4E	R	Desynchronizer Pointer Offset Counter (PLBOC)							
4F	R	Not Used						PLBOC Sign Bit	PLBOC Bit 9

MEMORY MAP DESCRIPTIONS

DEVICE IDENTIFIER

The device identifier (ID) is based on the manufacturer ID found in IEEE standard 1149.1 on Boundary Scan, and the ID assigned by the Solid State Products Engineering Council (JEDEC). The serial format for this ID is shown below:



The device identifier is not currently provided as a boundary scan message. However, the manufacturer ID and part number are implemented with read-only capability for microprocessor read access. The manufacturer ID given for all TranSwitch chips is 107 (06B hex.). The part number of the L4M device is 03456 (0D80 hex.) in binary. In addition, the read-only segment is expanded to include a 4-bit mask level field and a 4-bit future growth field as shown below:

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004	R	Mask Level				Growth			
003	R	Revision (Version) Level				0	0	0	0
002	R	1	1	0	1	1	0	0	0
001	R	0	0	0	0	0	0	0	0
000	R	1	1	0	1	0	1	1	1

CONTROL REGISTER BIT DESCRIPTIONS

Address	Bit	Symbol	Description
10	7	TINVC	**Transmit Invert Line Clock:** A 0 enables byte- or nibble-wide data (TXDn) to be clocked into the L4M on positive transitions of the clock (TXC). A 1 enables byte- or nibble-wide data to be clocked in on negative transitions of the clock.
	6	TLAIS	**Transmit Line AIS:** A 1 enables the L4M to generate and insert an all ones line signal (140 Mbit/s AIS) in the transmit direction, independent of the state of the enable AIS bits and alarms. Transmit line AIS is generated under the following conditions: - External loss of signal alarm (EXTLOS) when EAISEN is a 1, - Loss of transmit clock alarm (TLOC) when TCAISEN is a 1, - Loss of 140 Mbit/s frame alignment when LFAISE is a 1, - Microprocessor writes a 1 to this bit position.
	5	RING	**Path Protected Ring Mode:** The L4M must be connected to a mate L4M for this mode. A 1 enables the Transmit Alarm Indication Port to control the FEBE (when FEBEEN=1) and RDI (when RDIEN=1) that are transmitted in the G1 byte.
	4	EXOB	**External "O"-bit Interface:** A 1 enables the Overhead Communication Channel data interface for transmitting the 90 overhead communication channel bits ("O"-bits) specified in the 140 Mbit/s SDH/SONET format. The interface bits are inserted asynchronously into the SDH/SONET format with respect to the nine subframes. A 0 causes zeros to be transmitted for all of the "O"-bits.
	3	TESTB3	**Test B3 Byte:** A 1 enables a microprocessor-written byte (location 68H) to be the transmitted B3 byte. A 0 enables the microprocessor-written byte in location 68H to work as a B3 error mask. A 1 written into one or more bit positions will cause that bit position to be transmitted inverted from its calculated value, until the bit position is written with a 0.
	2	XRDIEN	**External RDI Enable:** A 1 in this bit and the RDIEN bit enables a path RDI (bit 5 in G1) to be generated and transmitted when a high is placed on the STAI pin. A 0 disables the logic level placed on the STAI pin from controlling the state of path RDI.
	1	POHEUQ	**POH Bytes Enabled During Unequipped Status:** This bit works in conjunction with control bit TUNEQ for generating an unequipped channel. The Path Overhead Byte enable feature must be enabled ($\overline{\text{POHDIS}}$ lead is high). TUNEQ / POHEUQ / Action 0 / X / Normal Operation 1 / 0 / Unequipped Channel. POH and payload bytes are transmitted as 0. 1 / 1 / Supervisory Unequipped Channel. POH enabled. Payload bytes transmitted as 0.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>10</td><td>0</td><td>ADDZ</td><td>
Add Bus Force High Impedance State: Works in conjunction with the control bit FBTOZ for controlling the add bus signal states. Assuming that there is no drop or add bus alarms, the following states are possible:

ADDZ FBTOZ Action
0 0 Normal operation. Unused bytes (TOH and POH bytes when disabled) are transmitted in the high impedance state.
0 1 Normal operation. Unused bytes (TOH and POH bytes when disabled) are transmitted as 0s. $\overline{ADD}$ is forced to 0.
1 0 All add bus bytes (time slots) forced to the high impedance state. Note: when add bus timing is selected, data only will be forced to the high impedance state. The C1J1 and SPE signals are inputs. In the other two timing modes, add bus and external timing modes, the add bus clock (ACLK), SPE indicator, C1J1 will be forced to 0. $\overline{ADD}$ is forced to 1.
1 1 All add bus Bytes (time slots) forced to the zero state. Note: when add bus timing is selected, data only will be forced to the zero state. The C1J1 and SPE signals are inputs. In the other two timing modes, add and external, the add bus clock, SPE, C1J1 will be forced to 0. $\overline{ADD}$ is forced to 0.

When there is an alarm for the clock that sources the add bus data, the operation in the table below occurs:

<table>
<tr><th rowspan="2">ADDZ</th><th rowspan="2">FBTOZ</th><th colspan="3">Action for Timing Modes</th></tr>
<tr><th>ADD Bus</th><th>DROP Bus</th><th>External</th></tr>
<tr><td>0</td><td>0</td><td>Add Bus data forced to Hi-Z state. $\overline{ADD}$=1.</td><td>Add Bus data is forced to its Hi-Z state. ASPE, ACLK, AC1J1 forced to 0. $\overline{ADD}$=1.</td><td>Add Bus data is forced to its Hi-Z state. ASPE, ACLK, AC1J1 forced to 0. $\overline{ADD}$=1.</td></tr>
<tr><td>0</td><td>1</td><td>Add Bus data forced to 0 state. $\overline{ADD}$=0.</td><td>Add Bus data is forced to 0 state. ASPE, AC1J1, ACLK, $\overline{ADD}$ are forced to 0 state.</td><td>Add Bus data is forced to 0 state. ASPE, AC1J1, ACLK, $\overline{ADD}$ are forced to 0 state.</td></tr>
<tr><td>1</td><td>0</td><td>Add Bus data is forced to Hi-Z state. $\overline{ADD}$=1.</td><td>Add Bus data is forced to Hi-Z state. ASPE, ACLK, AC1J1 forced to 0. $\overline{ADD}$=1.</td><td>Add Bus data is forced to Hi-Z state. ASPE, ACLK, AC1J1 forced to 0. $\overline{ADD}$=1.</td></tr>
<tr><td>1</td><td>1</td><td>Add Bus data and $\overline{ADD}$ are forced to the 0 state.</td><td>Add Bus data is forced to 0 state. ACLK, ASPE, AC1J1, and $\overline{ADD}$ are forced to 0.</td><td>Add Bus data is forced to 0 state. ACLK, ASPE, AC1J1, and $\overline{ADD}$ are forced to 0.</td></tr>
</table>
</td></tr>
</table>

Address	Bit	Symbol	Description
11	7	PSLEN	**Path Signal Label Alarm Enable:** A 1 enables a 140 Mbit/s receive line AIS, and path RDI to be generated and sent when a C2 mismatch alarm (PLSERR) or unequipped (C2EQ0) alarm occurs.

	6	RDIEN	**Far End Receive Failure Enable:** A 1 enables the internal alarms to determine the state of the transmitted RDI bit, while a 0 disables the internal alarms from controlling the state of the RDI bit. When written with a 0, the microprocessor must write the state of the RDI bit by writing a 1 or 0 to control bit TRDI or bit 3 in the G1 POH byte register location 7AH. The following table is a summary of the various conditions that generates an RDI.
			
			- External G1 byte, when EXG1 is a 1
			- RDIEN is a 1 and RING and EXG1 are 0:
			  - DBLOC alarm=1 and DROPT pin is low
			  - Low on $\overline{\text{EXAIS}}$ (pin 17)
			  - E1 byte AIS indication, when EAPE is a 0
			  - High on ISTAT (pin 37), when EAPE is a 1
			  - High on PAIS (pin 38), when EAPE is a 1
			  - High on STAI (pin 39), when XRDIEN is a 1
			  - Drop bus loss of J1 alarm (DBLOJ1) when PTEN (pin 2) is low
			  - Path signal label mismatch (PSLERR), when PSLEN is a 1
			  - Unequipped status (C2EQ0), when PSLEN is a 1
			  - J1 loss of lock (J1LOL), when J1LEN is a 1
			  - J1 trace message mismatch (J1TIM), when J1TEN is a 1
			  - Loss of pointer (RLOP), when PTEN (pin 2) is high
			  - Path AIS (RPAIS), when PTEN (pin 2) is high.
			- RING and RDIEN are a 1, and EXG1 is 0:
			  - RDI status via Alarm Indication Port (no AIPLOC alarm).
			- RDIEN and EXG1 are 0:
			  - Bit 3 in 6AH is a 1 (transmit G1 byte in RAM).
			  - TRDI is a 1.

	5	TRDI	**Transmit RDI:** A 1 generates an RDI (Bit 5 in the transmit G1 byte is set to 1) when control bit RDIEN bit is 0. This bit is orred with the microprocessor-written RAM G1 value for RDI (bit 3) in location 6AH.
	4	FEBEEN	**Far End Block Error Enable:** A 1 enables the received B3 value to generate the transmitted FEBE count. A 0 enables a microprocessor-written value (bits 7 - 4 in register location 6AH) to be transmitted as the FEBE count. The FEBE count is sent under the following conditions: - Via external G1 byte, when EXG1 is a 1. - Microprocessor-written value in bits 7-4 in 6AH, when FEBEEN is a 0. - Received B3 BIP-8 errors, when FEBEEN is a 1, and RING and EXG1 are 0. - Received B3 BIP-8 errors via Alarm Indication Port, when FEBEEN and RING are 1, and EXG1 is 0.

Address	Bit	Symbol	Description
11	3	EAPE	**External Alarm Pin Enable:** A 1 enables the external ISTAT (pin 37) and PAIS (38) pins to function in place of the E1 byte AIS detection circuit (out of band AIS indication). A 0 disables the external alarm pins and enables the E1 byte AIS detection circuit (in band AIS indication). The E1 byte may be used to carry an in band upstream AIS indication. The E1 byte AIS detection circuitry uses majority logic to determine if the byte is carrying an AIS indication.

	2	RAISEN	**Receive Line AIS Enable:** A 1 enables internal (and external) alarms to generate a receive 140 Mbit/s line AIS. A 0 disables the ability of the internal alarms to generate a 140 Mbit/s line AIS. The following table is a summary of the various conditions that generates a 140 Mbit/s line AIS, and provides an AIS indication (pin 24).
			
			- RAISEN is a 1:
			  - Low on $\overline{\text{EXAIS}}$ (pin 17)
			  - E1 byte AIS indication, when EAPE is a 0
			  - High on ISTAT (pin 37), when EAPE is a 1
			  - High on PAIS (pin 38), when EAPE is a 1
			  - Drop bus loss of J1 alarm (DBLOJ1) when PTEN (pin 2) is low
			  - Drop bus loss of clock (DBLOC), when BSAISE is a 0
			  - Path signal label mismatch (PSLERR), when PSLEN is a 1
			  - Unequipped status (C2EQ0), when PSLEN is a 1
			  - J1 loss of lock (J1LOL), when J1LEN is a 1
			  - J1 trace message mismatch (J1TIM), when J1TEN is a 1
			  - Loss of pointer (RLOP), when PTEN (pin 2) is high
			  - Path AIS (RPAIS), when PTEN (pin 2) is high.
			- RAISEN is a 0:
			  - The microprocessor writes a 1 to RAISG.
			  Note. The microprocessor may write to control bit RAISG at any time to generate a line AIS. However, writing a 0 to RAISEN prevents contention between the internal alarms and the microprocessor for generation of line AIS.
			- Receive loss of line frame alignment (RLOF), when LFAISE is a 1 and BSAISE is a 0.

	1	RAISG	**Generate Receive AIS:** A 1 causes a receive 140 Mbit/s line AIS to be generated independent of the internal alarms. Note: The microprocessor may write to control bit RAISG at any time for generating a line AIS. However, writing a 0 to RAISEN prevents contention between the internal alarms and the microprocessor for generation of line AIS.
	0	RINVC	**Receive Invert Line Clock:** Byte- or nibble-wide data is clocked out of the L4M on negative transitions of the clock (RXCO) when this bit is a 0. A 1 enables the byte or nibble line signal to be clocked out of the L4M on positive transitions of the clock.

Address	Bit	Symbol	Description
12	7	EXZ5	**Transmit External Z5 Byte:** A 1 enables the Z5 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 6FH to be transmitted.
	6	EXZ4	**Transmit External Z4 Byte:** A 1 enables the Z4 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 6EH to be transmitted.
	5	EXZ3	**Transmit External Z3 Byte:** A 1 enables the Z3 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 6DH to be transmitted.
	4	EXH4	**Transmit External H4 Byte:** A 1 enables the H4 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 6CH to be transmitted.
	3	EXF2	**Transmit External F2 Byte:** A 1 enables the F2 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 6BH to be transmitted.
	2	EXG1	**Transmit External G1 Byte:** A 1 enables the G1 byte from the external POH interface to be transmitted. A 0 selects the states of the G1 byte to be written by internal logic, or by the microprocessor, as enabled.
	1	EXC2	**Transmit External C2 Byte:** A 1 enables the C2 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value in register location 69H to be transmitted.
	0	EXJ1	**Transmit External J1 Byte:** A 1enables the J1 byte from the external POH interface to be transmitted. A 0 enables the microprocessor-written value to be transmitted.
13	7	J1COM	**J1 Message Comparison Mode:** Works in conjunction with the CCITT control bit according to the following table: CCITT / J1COM / Action 0 / X / Transmit and receive J1 memory segments are configured for 64 bytes. Incoming messages are written in a rotating fashion with no defined starting address. 1 / 0 / Transmit and receive J1 memory segments are configured for 16 bytes. Incoming messages are written in a rotating fashion with no defined starting address. 1 / 1 / Transmit and receive J1 memory segments are configured for 16 bytes. J1 incoming message comparison feature enabled. The microprocessor writes the expected 16-byte message into RAM. After multiframe alignment is established, the J1 bytes in the message are compared against the microprocessor-written bytes, located in register location F0 to FFH.
	6	CCITT	**J1 Memory Size:** A 1 dimensions the transmit and receive memory segment size to 16 bytes, while a 0 dimensions the memory segment to 64 bytes.

Address	Bit	Symbol	Description
13	5	TUNEQ	**Transmit Unequipped Status:** This bit works in conjunction with control bit POHEUQ for generating an unequipped channel. The Path Overhead Byte enable feature must be enabled ($\overline{\text{POHDIS}}$ lead is high). TUNEQ / POHEUQ / Action 0 / X / Normal Operation 1 / 0 / Unequipped Channel. POH and payload bytes are transmitted as 0. 1 / 1 / Supervisory Unequipped Channel. POH bytes enabled. Payload bytes transmitted as 0.
	4	POHRAM	**Path Overhead Bytes to RAM**: A 1 enables the transmit POH bytes (e.g. EXH4 is equal to 1) from the external POH interface to be written into RAM prior to transmission. A 0 still enables selected external interface POH bytes to be transmitted, but the RAM locations are not written with the value of the external POH byte. Instead, the RAM locations will hold the microprocessor-written values.
	3	LHZ	**Force Receive Line to High Impedance:** A 1 forces the receive byte or nibble data (RXDn), and line output clock (RXCO) to a high impedance state, until this bit is written with a 0. This bit is set to 1 after a device reset.
	2	LLBK	**Line Loopback:** A 1 written into this location enables the received line signal to be looped back as the transmit line signal. The received data and clock are provided at either the byte or nibble receive line interfaces.
	1	SLBK	**SDH/SONET Loopback:** A 1 written into this location enables a VC-4/SPE loopback. This feature is not valid when the PTEN pin is set to 1.
	0	COR	**Non-Saturating Performance Counters Enable:** A 1 enables the performance counters to be non-saturating with roll over capability. A 0 causes all performance counters to be saturating, stopping at their maximum value, with clear on read capability.
14	7	EAISEN	**External Loss Of Signal AIS Enable:** A 1 enables a 140 Mbit/s AIS to be transmitted when a low is applied to $\overline{\text{EXLOS}}$ (pin 85). A 0 disables an external loss of signal indication from transmitting an AIS.
	6	TCAISEN	**Transmit Loss of Clock AIS Enable:** A 1 enables the L4M to send a 140 Mbit/s AIS when a transmit loss of clock alarm (TLOC) is detected. A 0 disables a transmit loss of clock alarm (TLOC) from transmitting an AIS.

Address	Bit	Symbol	Description
14	5	TOHOUT	**Transport Overhead Bytes Output Enabled:** A 1 enables the L4M to generate the three A1 and A2 framing bytes, the C1 byte, and the H1 and H2 bytes, according to the following table. This feature in enabled in the drop bus and external timing modes only. TOHOUT / UPC1 / SVC4H / Action 0 / X / 0 — No TOH bytes. The SPE starting location (starting with J1) equals 522 when drop or the external timing mode is selected. For add bus timing, the starting location is determined by the J1 pulse (AC1J1). 0 / X / 1 — No TOH bytes. The SPE starting location (starting with J1) equals 0 when drop or the external timing mode is selected. For add bus timing, the starting location is determined by the J1 pulse (AC1J1). 1 / 0 / 0 — A1, A2, C11, and H1/H2 byte generated. The C11 byte (first C1 byte) is fixed as 01H. The pointer value is equal to 522, the starting location of the SPE. The generation of the TOH bytes is disabled in the add bus timing mode. 1 / 0 / 1 — A1, A2, C11, and H1/H2 byte generated. The C11 byte (first C1 byte) is fixed as 01H. The pointer value is equal to 0, the starting location of the SPE. The generation of the TOH bytes is disabled in the add bus timing mode. 1 / 1 / 0 — A1, A2, C11, and H1/H2 byte generated. The C11 byte (first C1 byte) is the microprocessor-written value (location 1EH). The pointer value is equal to 522, the starting location of the SPE. The generation of the TOH bytes is disabled in the add bus timing mode. 1 / 1 / 1 — A1, A2, C11, and H1/H2 byte generated. The C11 byte (first C1 byte) is the microprocessor-written value (location 1EH). The pointer value is equal to 0, the starting location of the SPE. The generation of the TOH bytes is disabled in the add bus timing mode.
	4	J1LEN	**J1 Loss Of Lock Alarm Action Enable:** A 1 enables the L4M to generate a receive 140 Mbit/s AIS (when AIS is enabled; RAISEN is a 1), and path RDI is enabled and the L4M is not in a path protection ring configuration (when RDIEN is a 1 and RING is 0) when a J1 loss of lock is detected.

Address	Bit	Symbol	Description
14	3	J1TEN	**J1 Trace Identifier Mismatch Alarm Action Enable:** A 1 enables the L4M to generate a receive 140 Mbit/s AIS (when AIS is enabled; RAISEN is a 1), and path RDI is enabled and the L4M is not in a path protection ring configuration (when RDIEN is a 1 and RING is 0) when a J1 a trace identifier mismatch is detected.
	2	TGEN	**Transmit Test Generator Enable:** A 1 enables the transmit 2^{23}-1 test pseudo random generator. The transmit clock signal (TXC) must be present. Byte or nibble interface data is disabled.
	1	ANAEN	**Test Analyzer Enable:** A 1 enables the 2^{23}-1 pseudo random test analyzer. The test analyzer samples the receive data. Errors are counted in a 16-bit performance counter after alignment is established.
	0	SVC4H	**Start Transmit VC-4 after H3 Byte:** This feature is operational in the drop timing and external timing modes only. A 1 enables the VC-4 (starting with the J1 byte) to start after the H3 byte. The H1/H2 pointer value is set to 0 when the TOH feature is enabled (TOHOUT is a 1). A 0 enables the VC-4 to start after the C1 byte with a pointer value equal to 522. In the add bus timing mode, an add bus J1 pulse (in AC1J1) determines the starting location of the SPE.
15	7	LFAISE	**Loss Of Frame AIS Enable:** A common control bit for both the receive and transmit performance monitoring circuits. A 1 enables a receive or transmit loss of frame alarm to generate a receive or transmit 140 Mbit/s AIS. The generation of AIS in the receive direction is disabled when the bit stuffing AIS feature is enabled (BSAISE is a 1). A 0 disables a loss of frame alarm from generating AIS.
	6	FDAEN	**Frame Alignment AIS Enable:** A 1 enables frame alignment to work in conjunction with the AIS detector. The AIS detection occurs when AIS is detected and loss of frame has occurred. AIS recovery occurs when frame alignment occurs or the AIS condition goes away. A 0 disables the frame alignment from working with the AIS detection circuit, that is, AIS can be declared even if a loss of frame condition is not present.
	5	TPSSEL	**Transmit Pointer S-bit Select:** Enabled when control bit TOHOUT is a 1 in the drop bus and external timing modes. A 1 permits the microprocessor to write the value of the transmit S-bits in the H11, H12, and H13 bytes. A 0, forces the S-bits in H11 to be sent as 10, and the S-bits in H12 and H13 to be sent as 00. See register 1DH.
	4	RPSDS	**Receive Pointer S-bit Disabled:** Enabled when PTEN (pin 2) is high enabling the pointer tracking machine. This bit also works in conjunction with the RPSSEL bit according to the following table. RPSDS / RPSSEL / Action 0 / 0 / Pointer byte H11 S-bits are checked in pointer tracking machine against the value 10. 0 / 1 / Pointer byte H11 S-bits are checked in pointer tracking machine against a microprocessor-written value in bits 1 and 0 in 1DH. 1 / X / The S-bit check is disabled in the pointer tracking machine.

Address	Bit	Symbol	Description
15	3	RPSSEL	**Receive Pointer S-Bit Select:** Enabled when PTEN (pin 2) is high enabling the pointer tracking machine. This bit works in conjunction with the RPSDS bit according to the table given above.
	2	FBTOZ	**Force Unused Bytes To Zero:** A 1 forces the unused TOH bytes and POH bytes (when disabled) to 0. A 0 forces the unused bytes to a high impedance state.
	1	C2FVD	**C2 Fixed Value Disabled:** A 1 disables the comparison of the received C2 byte against the fixed hardware value of 01H in the C2 mismatch detection circuit. The C2 mismatch comparison is performed against the microprocessor-written value only.
	0	UPC1	**Microprocessor Writes C1 Value:** Enabled when control bit TOHOUT is a 1 in the drop bus and external timing modes. A 1 enables the microprocessor to write the value of the transmitted C1 byte. A 0 generates the value of 01H for the transmitted C1 byte.
16 17	7-4 7-0	Transmit C1 Offset	**Transmit C1 Offset Register:** Enabled in the external timing mode only, when a high is placed on ENABT (pin 36), and when control bit TC1DC is a 1. The 12-bit register location compensates for the position of the C1 pulse in the EXC1 signal (pin 105). The LSB is bit 0 in 17H, and the MSB is bit 7 in 16H. The register compensates for up to 2429 (270 columns X 9 rows - 1). For example, if the C1 pulse is in the correct position, zeros are written to the register. The correct position of the framing reference is when C1 corresponds to the C11 position in the SDH/SONET format. When a binary 1 is written to the register (bit 0 in 17H is a 1), it is assumed that the position of the C1 pulse present in the EXC1 signal is shifted in time one byte and the input pulse corresponds to the C12 byte position in the SDH/SONET frame. This means that the starting point for the frame should be one byte earlier. Values written into the register greater than a binary value of 2429 will be counted as zero delay.
16	3	TC1DC	**Transmit C1 Delay Control:** Enabled in the external timing mode only, when a high is placed on ENABT (pin 36). A 1 enables the transmit 12-bit C1 offset register in locations 16H and 17H to compensate for a C1 offset delay in the transmit direction.
	0	PAISG	**Path AIS Generator Enable:** A 1 causes path AIS to be generated in the transmit direction. The transmitted payload and POH bytes are forced to the 1 state (if $\overline{\text{POHDIS}}$=1), in addition to the TOH bytes (when enabled).

Address	Bit	Symbol	Description
18 19	7-4 7-0	Receive C1 Offset	**Receive C1 Offset Register:** Enabled when a high is placed on the pointer tracking machine control lead PTEN (pin 2), and when control bit RC1DC is a 1. The 12-bit register location compensates the position of the C1 pulse in the DC1J1 or DC1 signal (pin 127, 126). The LSB is bit 0 in 19H, and the MSB is bit 7 in 18H. The register compensates for up to 2429 (270 columns X 9 rows - 1). For example, if the C1 pulse is in the correct position, zeros are written to the register. The correct position of the framing reference is when C1 corresponds to the C11 position in the SDH/SONET format. When a binary 1 is written to the register (bit 0 in 19H is a 1), it is assumed that the position of the C1 pulse present in the DC1 signal is shifted in time one byte and the input pulse corresponds to the C12 byte position in the SDH/SONET frame. This means that the starting point for the frame should be one byte earlier. Values written into the register greater than a binary value of 2429 will be counted as zero delay.
18	3	RC1DC	**Receive C1 Delay Control:** Enabled when the pointer tacking machine is selected, when a high is placed on PTEN (pin 2). A 1 enables the receive 12-bit register in locations 18 and 19H to compensate for a C1 offset delay in the receive direction.
	2	RDI10	**RDI/FERF Recovery/Detection 10 Consecutive Enable:** A 1 selects 10 consecutive events as the value for detection and recovery. A 0 selects 5 consecutive events as the value for detection and recovery.
	1	PADS	**Pointer Tracking Machine AIS to LOP Transition Disabled:** A 1 disables the AIS to LOP transition in the pointer tracking state machine. A 0 enables the AIS to LOP transition in the pointer tracking machine.
	0	FEBEBC	**FEBE Block Count Enable:** A 1 enables the FEBE counter to be configured to count FEBE blocks instead of FEBES. A valid count (between 1 and 8) will increment the 16-bit counter once. A 0 configures the FEBE counter to count FEBES.
1A 1B	7-0 7-1	Pointer Leak Rate Register	**FIFO Leak Rate Register:** The 15-bit value written into registers 1A and 1BH is used for presetting the internal pointer leak counter. The value written into this register is based on the rate of occurrence of pointer movements from the number of counts read from positive/negative stuff counters, and the NJ/PJ indication pins. This count will represent the average leak rate. A count of 1 will decrement the pointer leak counter every three rows. Thus the minimum time to leak out one pointer movement is 8 frames or 1 millisecond, since each pointer movement is 24 bits. Bit 7 in register 1BH is assigned as the MSB, and represents bit 15 in the string, as shown below: | Register 1B | Register 1A | Bit 7 6 5 4 3 2 1 7 6 5 4 3 2 1 0 A pin (PLEQ0) is provided that will give a positive indication when the pointer leak counter is equal to zero. This indication is reset to zero when the pointer leak counter is preset. Register 1AH is preset to 01H after a device reset.

Address	Bit	Symbol	Description
1B	0	LOADEN	**Load Enable:** Used for desynchronizer operation. The internal pointer leak counter shall be preset with the 15-bit leak rate value using the following steps: 1. Write the value to the seven upper bits (with 7 being the MSB), and a 0 to this bit. 2. Write the 8-bit value into the lower register (1A). 3. Write a 1 to this bit, or write the seven upper bits in this register, along with a 1 to this bit. The internal counter will preset with the 15-bit value on the 0 to 1 transition. This bit is set to 1 after a device reset.
1C	7	RESETC	**Reset Counters**: A 1 causes the performance counters to reset. When the reset is completed, this bit is self clearing and this bit position becomes a 0.
	6	RESETD	**Reset Mapper:** A 1 resets the Mapper. The Mapper will remain reset until the processor writes a 0 into this location.
	5	RESETS	**Reset Desynchronizer:** A 1 resets the two FIFOs in the desynchronizer to mid-range values.
	2	PARDO	**Parity Data Byte Only:** A common bit for both the drop and add buses, and valid for all timing modes. A 1 enables parity to be calculated for data bytes only. A 0 enables parity to be calculated for the add bus output signals, and drop bus input signals.
	1	AC1EN	**Add Bus C1 Pulse Enable:** A 1 enables the C1 pulse to be transmitted as a separate signal instead of in the AC1J1 signal in the external and drop timing modes. A 0 enables the AC1J1 signal to carry both the C1 and J1 signals. In the add bus timing mode, the C1 signal can be applied on the AC1 pin instead of in the C1J1 signal independent of the state of this bit.
	0	BSAISE	**Bit Stuffing AIS Enable:** A 1 causes an internal bit stuffing implementation to be used for the transmit and receive 140 Mbit/s line AIS generation instead of using the external AIS clock. This bit is set to 0 upon power-up (selecting the external AIS clock). When the bit stuffing AIS feature is selected, the receive performance monitor circuit and AIS detection circuits are disabled when receive AIS is generated automatically by the L4M. Please note that the loss of the drop bus clock will disable the generation of receive AIS based on bit stuffing.

Address	Bit	Symbol	Description
1D	7-0	S-Bits µP Control	**Pointer S-bit Microprocessor-Written Values:** The bits in this location are the microprocessor-written S-bits in the transmit pointer bytes, and the S-bits used in the receive pointer tracking machine. The transmit S-bits in this location are enabled when control bits TPSSEL and TOHOUT are 1. In the receive direction, the S-bits in this location are enabled when control bit RPSSEL is 1 and RPSDS is 0. The bits are defined as: Bit 7 is the S-bit state in bit 5 in the transmitted H11 byte. Bit 6 is the S-bit state in bit 6 in the transmitted H11 byte. Bit 5 is the S-bit state in bit 5 in the transmitted H12 byte. Bit 4 is the S-bit state in bit 6 in the transmitted H12 byte. Bit 3 is the S-bit state in bit 5 in the transmitted H13 byte. Bit 2 is the S-bit state in bit 6 in the transmitted H13 byte. Bit 1 is the S-bit state used to compare bit 5 in the received H11 byte in the pointer state machine. Bit 0 is the S-bit state used to compare bit 6 in the received H11 byte in the pointer state machine.
1E	7-0	C1	**C1 Microprocessor-Written Value:** When control bits TOHOUT and UPC1 are equal to 1, the transmitted C1 value is the value written into this location by the microprocessor. When control bit TOHOUT is a 1 and UPC1 is a 0, a fixed value of 01H is transmitted, and this register location is disabled.
1F	0	PLDINV	**Phase-Locked Loop Detector Invert Control Bit:** A 1 inverts the sense of one of the phase-locked loop internal phase detector's inputs. This bit should be set to 1 for normal operation.

STATUS REGISTER BIT DESCRIPTIONS

The unlatched alarms are allocated to even numbered hexadecimal address locations, while the latched alarm bit positions are allocated to odd numbered register locations. A latched bit sets on the positive level of the alarm. A latched bit position clears on a microprocessor read cycle. If the alarm is active after the read cycle, the bit position will relatch.

Address	Bit	Symbol	Description
20 21	7	ANOOL	**Analyzer Out Of Lock:** When enabled, an alarm occurs when the 2^{23}-1 analyzer is out of lock. An out of lock alarm occurs when 30 bits in a 1000 bits are received in error. In lock occurs when the first 24 bits in the pattern are received correctly. An out of lock disables the analyzer error 16-bit counter. This bit is forced to 0 when the ANAEN control bit is set to 0.
	6	TLAISD	**Transmit Line AIS Detected:** An alarm occurs when a 140 Mbit/s AIS has been detected (all ones in the transmit bit stream). When control bit FDAEN is a 0, an AIS is detected when the incoming signal has five or less zeros in each of two consecutive frame periods (2928 bits per frame). Recovery occurs when if each of two consecutive frame periods contains six or more zeros. When control bit FDAEN is a 1, AIS is detected when the incoming signal has five or less zeros in each of two consecutive frame periods, and a loss of frame alignment has been detected. Recovery occurs when each of two consecutive frame periods contains six or more zeros, or frame alignment has occurred. Other than reporting the alarm, no action is taken.
	5	TFIFOE	**Transmit FIFO Error Detected:** An alarm occurs when an overflow or underflow condition has taken place in the transmit FIFO. The FIFO recenters automatically after the FIFO error. Other than reporting the alarm, and recentering the FIFO, no action is taken.
	4	ABLOJ1	**Add Bus Loss of J1**: An alarm occurs when, in add bus timing mode, the J1 pulse in the AC1J1 signal is missing for 8 consecutive frames. Recovery occurs when the J1 pulse in the AC1J1 signal is present for 8 consecutive frames.
	3	LAISC	**Loss of AIS Clock:** An alarm occurs when the AIS input clock (AISCK) is stuck high or low for 12-34 consecutive clock cycles of the RAM clock (RAMCI). Recovery occurs on the first clock transition. This clock is used to generate the 140 Mbit/s line AIS when control bit BSAISE is a 0.
	2	XAIS	**External AIS Indication:** An indication occurs when an active low is present on the EXAIS pin. When control bit RAISEN is a 1, a receive 140 Mbit/s AIS is generated, and a path RDI is generated when RDIEN=1.
	1	DBLOJ1	**Drop Bus Loss of J1:** An alarm occurs when the J1 pulse in the DC1J1 signal is missing for 8 consecutive frames. Recovery occurs when the J1 pulse in the DC1J1 pulse is present for 8 consecutive frames. When the pointer tracking feature is enabled (PTEN is high), the detection of this alarm is disabled.
	0	E1AIS	**AIS Detected in the E1 Byte:** An alarm occurs when a majority of all ones (5 out of 8 bits are a 1) has been detected in the incoming E1 byte once. Recovery occurs when a majority of ones is not detected once. This provides a means of signaling the 140 Mbit/s Mapper that an upstream SDH/SONET Loss Of Frame and other alarms have occurred.

Address	Bit	Symbol	Description
22 23	7	BUSERR	**Received Parity Error Detected:** An alarm indicates that a parity error has been detected in the drop bus signals. The drop bus data, SPE signal and composite C1J1 pulse are calculated for odd parity and compared against the parity bit input for parity errors when the pointer tracking feature is disabled (PTEN lead is low). The drop bus data, and C1 pulse is calculated for odd parity and compared against the parity bit input for parity errors when the pointer tracking feature is enabled (PTEN lead is high). When a 1 is written to control bit PARDO, the parity calculation and comparison is for the data byte only regardless of the state of the PTEN lead. No other action is taken, other than the alarm indication.
	6	RFIFOE	**Receive FIFO Error:** An alarm occurs when the receive second stage FIFO in the desynchronizer has either underflowed or overflowed. The FIFO is recentered automatically. No other action is taken.
	5	RRDI	**Receive RDI Alarm Detected:** An alarm occurs when a path RDI alarm has been detected in bit 5 of the received G1 byte. Control bit RDI10 determines whether the consecutive event requirement for detection and recovery is 5 or 10.
	4	PSLERR	**Path Signal Label Mismatch Detected:** An alarm indicates that the received C2 byte did not match the microprocessor-written value in location 75H, nor did it match the internal 01H value (when control bit C2FVD is a 0) for 5 consecutive frames. Recovery occurs when a match occurs in the C2 comparison byte (75H) or internal 01H value (when enabled), for 5 consecutive frames. When control bit C2FVD is a 1, the comparison against the internal 01H value is disabled. This alarm is disabled if a C2 unequipped alarm occurs.
	3	C2EQ0	**C2 Byte Equal to Zero:** An alarm occurs when the received C2 byte is all zeros for 5 consecutive frames, indicating that the VC-4/SPE is carrying an unequipped channel status (POH bytes and payload bytes are equal to zero). Recovery occurs when the received C2 byte is not all zeros for 5 consecutive frames.
	2	J1LOL	**J1 Loss of Lock Alarm:** An alarm occurs when the alignment of the J1 trace identifier label (message) has not been established. The J1 detection circuit is enabled when control bits J1COM and CCITT are a 1. The J1LOL alarm will become momentarily active when the following alarms are exited: DBLOJ1 when PTEN pin is low; E1AIS when EAPE bit is 0; XPAIS or XISTAT when EAPE bit is 1; RLOP or RPAIS when PTEN pin is high.
	1	J1TIM	**J1 Trace Identifier Mismatch:** An alarm indicates that the received stable 16-byte message did not match for one message time. Recovery from this alarm occurs when the J1 state machine losses lock (J1LOL) and then acquires lock with a 16-byte stable J1 message that matches the J1 comparison message in registers F0H to FFH.

Address	Bit	Symbol	Description
22 23	0	RLAISD	**Receive Line AIS Detected:** The alarm detection is enabled when control bit BSAISE is a 0 (bit stuffing AIS disabled), or when BSAISE=1 and the L4M is not generating a receive AIS based upon received alarms. When control bit FDAEN is a 0, a 140 Mbit/s line AIS is detected when the receive line signal (after the desynchronizer) has five or less zeros in two consecutive frame periods. Recovery occurs if each of the two consecutive frame periods has six or more zeros. When control bit FDAEN is a 1, an alarm occurs when the receive line signal has five or less zeros in two consecutive periods, and loss of frame has occurred. Recovery occurs if each of two consecutive frame periods has six or more zeros, or frame alignment has been detected.
24 25	7	TLOC	**Transmit Loss Of Clock:** An alarm occurs when the transmit line clock (TXC) is stuck high or low for 13-34 or more consecutive clock cycles of the RAM clock (RAMCI). Recovery occurs on the first clock transition.
	6	ABLOC	**Add Bus Loss Of Clock:** An alarm occurs when the add bus input clock (ACLK) in the add bus timing mode is stuck high or low for 13-34 or more consecutive clock cycles of the RAM clock (RAMCI). Recovery occurs on the first clock transition.
	5	DBLOC	**Drop Bus Loss Of Clock:** An alarm occurs when the drop bus input clock (DCLK) is stuck high or low for 13-34 or more consecutive clock cycles of the RAM clock (RAMCI). Recovery occurs on the first clock transition.
	4	RLOC	**Receive Line Loss Of Clock:** An alarm occurs when the receive line input clock (RXCI) is stuck high or low for 12-35 or more consecutive clock cycles of the RAM clock (RAMCI). Recovery occurs on the first clock transition.
	3	1SFOU	**First Stage FIFO Overflow or Underflow:** An alarm occurs when the 1st stage receive FIFO in the desynchronizer has either underflowed or overflowed. The FIFO is recentered automatically. No other action is taken. The 1st stage FIFO will overflow or underflow if the value in register 1AH and 1BH is too large, such that the pointer movements are not leaked out as fast as they are arriving.
	2	XSTAI	**SDH/SONET Network Alarm Indication:** An indication occurs when an active high is present on the STAI pin. When control bits XRDIEN and RDIEN are set to 1, a path RDI is transmitted for the duration of the alarm.
	1	XISTAT	**External SDH/SONET Alarm:** An indication occurs when an active high is present on the ISTAT pin. When control bit EAPE is a 1, path RDI is transmitted and a receive AIS is generated for the duration of the alarm.
	0	XPAIS	**External Path AIS Alarm:** An indication occurs when an active high is present on the PAIS pin. When control bit EAPE is a 1, path RDI is transmitted and a receive AIS is generated for the duration of the alarm.

Address	Bit	Symbol	Description
26	7	SINT	**Software Interrupt:** A software interrupt indication occurs when one or more interrupt mask bit positions are written with a 1, and the corresponding alarms for those interrupt mask bits occur. The SINT state is exited when the latched alarm causing the interrupt is cleared or the alarm's corresponding interrupt mask bit is written with a 0.
26 27	6	EXTLOS	**External Transmit Loss Of Signal Alarm:** An alarm occurs when a low is present on the $\overline{\text{EXLOS}}$ pin. When control bit EAISEN is a 1, a transmit line AIS is generated.
	5	AIPLOC	**Alarm Indication Port Loss Of Clock:** An alarm occurs when the TAIPC clock (which is connected to the mate L4M) has been stuck high or low for 113-764 or more consecutive RAM clock (RAMCI) periods. FEBE and RDI are transmitted as 0 in the G1 byte. Recovery occurs on the first clock transition.
	2	NEW	**New Alarm:** When the pointer tracking feature is disabled (PTEN pin is low), this alarm indicates that the J1 pulse has jumped more than three byte positions or has made an illegal increment or decrement. When the pointer tracking feature is enabled (PTEN pin is high), this alarm indicates that 3 x new pointers has been detected.
28 29	7	TLOF	**Transmit 140 Mbit/s Loss Of Frame Alarm:** An alarm occurs when four consecutive errored frame alignment patterns (based on G.751) are detected. Recovery occurs when three consecutive frame alignment patterns without errors are detected.
	6	RLOF	**Receive 140 Mbit/s Loss Of Frame Alarm:** An alarm occurs when four consecutive frame alignment patterns (based on G.751) are detected incorrectly. Recovery occurs when three consecutive frame alignment patterns are detected correctly.
	5	TDAI	**Transmit Distant Alarm Indication:** A 1 indicates that bit 13 in the transmitted 140 Mbit/s G.751 format is a 1. This alarm is inhibited when loss of frame alignment (**TLOF**), or when a transmit 140 Mbit/s AIS is detected, or when an errored transmit frame is detected (only for that particular errored frame).
	4	RDAI	**Receive Distant Alarm Indication:** A 1 indicates that bit 13 in the received 140 Mbit/s G.751 format is a 1. This alarm is inhibited on a loss of frame alignment (RLOF), or when a receive 140 Mbit/s AIS is detected, or when an errored receive frame is detected (only for that particular errored frame).
	3	RLOP	**Receive Loss Of Pointer Alarm:** Enabled when the pointer tracking feature is enabled (PTEN lead is high). An alarm occurs when loss of pointer has been detected in the pointer tracking machine.
	2	RPAIS	**Receive Path AIS Alarm:** Enabled when the pointer tracking feature is enabled (PTEN lead is high). An alarm occurs when path AIS has been detected in the H1 and H2 bytes.

INTERRUPT MASK BIT DEFINITIONS

The interrupt mask bits work in conjunction with the latched bit positions to provide a hardware and global software interrupt indication. Writing a 1 to one or more mask bits, when the corresponding alarm occurs, will cause the global software interrupt (SINT, Address 26H, bit 7) to occur, and will cause a hardware interrupt to occur by setting the HINT control bit (Address 33H, bit 7) to 1. The hardware interrupt pin will be turned off when the latched alarm bit causing the interrupt is cleared, or when the corresponding interrupt mask bit is set to 0, or the HINT bit is set to 0. The bit positions in the mask bit segment locations correspond to the bit positions in the status register segment locations.

Address	Bit	Symbol	Description
30	7	ANOOL	Analyzer Out Of Lock
	6	TLAISD	Transmit line 140 Mbit/s AIS Detected
	5	TFIFOE	Transmit FIFO error (underflowed or overflowed)
	4	ABLOJ1	Add bus loss of J1
	3	LAISC	Loss of AIS clock
	2	XAIS	External AIS generate signal on EXAIS pin
	1	DBLOJ1	Drop bus loss of J1
	0	E1AIS	AIS detected in the E1 byte (Transport Overhead)
31	7	BUSERR	Drop bus parity error
	6	RFIFOE	Receive FIFO error (underflowed or overflowed)
	5	RRDI	Receive RDI/FERF (bit 5 in G1)
	4	PSLERR	Path Signal Label error
	3	C2EQ0	Unequipped C2 status (00H)
	2	J1LOL	J1 loss of lock (alignment unstable)
	1	J1TIM	J1 Trace identifier mismatch
	0	RLAISD	Receive Line AIS Detected
32	7	TLOC	Transmit Line Loss Of Clock
	6	ABLOC	Add bus loss of clock
	5	DBLOC	Drop bus loss of clock
	4	RLOC	Receive line loss of clock
	2	XSTAI	External network alarm
	1	XISTAT	External STS alarm
	0	XPAIS	External Path AIS alarm
33	7	HINT	Hardware interrupt enable
	6	EXTLOS	External Loss Of Signal alarm
	5	AIPLOC	Alarm Indication Port Loss of clock alarm
	2	NEW	3 consecutive new pointers received

Address	Bit	Symbol	Description
34	7	TLOF	Transmit 140 Mbit/s Loss Of Frame alarm
	6	RLOF	Receive 140 Mbit/s Loss Of Frame alarm
	5	TDAI	Transmit 140 Mbit/s Distant Alarm Indication
	4	RDAI	Receive 140 Mbit/s Distant Alarm Indication
	3	RLOP	Receive Loss Of Pointer
	2	RPAIS	Receive Path AIS

TRANSMIT POH REGISTER DESCRIPTIONS

The transmission of the POH byte in the add direction, and the processing of the POH bytes in the drop direction are enabled when a high is placed on the $\overline{\text{POHDIS}}$ lead.

Address	Bit	Symbol	Description
68	7-0	B3 Error Mask	**B3 Error Mask and Test Byte:** When control bit TESTB3 is written with a 0, a 1 written to any of the bit locations will generate a continuous bit error in the corresponding B3 bit position. Internally, this RAM location is exclusive-or gated with the calculated B3 byte prior to transmission. The B3 errors are transmitted until this location is rewritten with a 00H. Bit 7 in this location corresponds to bit 1 in the transmitted B3 byte. When control bit TESTB3 is written with a 1, the bits written into this location are transmitted as the B3 byte.
69	7-0	C2 Signal Label	**C2 Signal Label Byte:** When control bit EXC2 is a 0, the bits written into this location are transmitted as the C2 byte. When control bits EXC2 and POHRAM are a 1, the external POH interface C2 byte is written into this location, and is also transmitted. When control bit EXC2 is a 1, and POHRAM is a 0, the external POH interface C2 byte is transmitted and this location holds the microprocessor-written C2 value. Bit 7 in this location corresponds to bit 1 in the transmitted C2 byte.
6A	7-0	Transmit G1 Byte	**Transmit G1 Byte:** Bits 7-0 provide the states of the external POH byte or microprocessor-written values, according to the following: 1 2 3 4 5 6 7 8 G1 Byte 7 6 5 4 3 2 1 0 This location FEBE RDI Unassigned When control bits EXG1, RDIEN, and FEBEEN are 0, the microprocessor writes the transmitted FEBE state and path RDI state. The unassigned bits are always written by the microprocessor unless EXG1 is a 1. When control bits EXG1 and POHRAM are a 1, the external POH interface G1 byte is written into this location, and is also transmitted. When control bit EXG1 is a 1, and POHRAM is a 0, the external POH interface G1 byte is transmitted and this location holds the microprocessor-written G1 value. The unassigned bits for transmission must always be written into bits 2 through 0 in this location, otherwise the transmitted states of these bits are undetermined. See also FEBEEN, RDIEN and RING control bits.

Address	Bit	Symbol	Description
6B	7-0	F2	**User Channel:** When control bit EXF2 is a 0, the bits written into this location are transmitted as the F2 byte. When control bits EXF2 and POHRAM are a 1, the external POH interface F2 byte is written into this location, and is also transmitted. When control bit EXF2 is a 1, and POHRAM is a 0, the external POH interface F2 byte is transmitted and this location holds the microprocessor-written F2 value. Bit 7 in this location corresponds to bit 1 in the transmitted F2 byte.
6C	7-0	H4	**H4 Byte:** When control bit EXH4 is a 0, the bits written into this location are transmitted as the H4 byte. When control bits EXH4 and POHRAM are a 1, the external POH interface H4 byte is written into this location, and is also transmitted. When control bit EXH4 is a 1, and POHRAM is a 0, the external POH interface H4 byte is transmitted and this location holds the microprocessor-written H4 value. Bit 7 in this location corresponds to bit 1 in the transmitted H4 byte.
6D	7-0	Z3	**Z3 Byte:** When control bit EXZ3 is a 0, the bits written into this location are transmitted as the Z3 byte. When control bits EXZ3 and POHRAM are a 1, the external POH interface Z3 byte is written into this location, and is also transmitted. When control bit EXZ3 is a 1, and POHRAM is a 0, the external POH interface Z3 byte is transmitted and this location holds the microprocessor-written Z3 value. Bit 7 in this location corresponds to bit 1 in the transmitted Z3 byte.
6E	7-0	Z4	**Z4 Byte:** When control bit EXZ4 is a 0, the bits written into this location are transmitted as the Z4 byte. When control bits EXZ4 and POHRAM are a 1, the external POH interface Z4 byte is written into this location, and is also transmitted. When control bit EXZ4 is a 1, and POHRAM is a 0, the external POH interface Z4 byte is transmitted and this location holds the microprocessor-written Z4 value. Bit 7 in this location corresponds to bit 1 in the transmitted Z4 byte.
6F	7-0	Z5	**Z5 Byte:** When control bit EXZ5 is a 0, the bits written into this location are transmitted as the Z5 byte. When control bits EXZ5 and POHRAM are a 1, the external POH interface Z5 byte is written into this location, and is also transmitted. When control bit EXZ5 is a 1, and POHRAM is a 0, the external POH interface Z5 byte is transmitted and this location holds the microprocessor-written Z5 value. Bit 7 in this location corresponds to bit 1 in the transmitted Z5 byte.
80 to BF	7-0	J1	**Path Trace Message:** The bytes written into this memory segment (16 or 64 bytes determined by the CCITT control bit) will provide a repetitive 64-or 16-byte fixed length message for transmission. The 16-byte message is allocated to the 80 to 8FH segment. The remaining segment 90 to BFH is not used. The starting address is not set for transmission. The message is transmitted in a rotating fashion. When control bit EXJ1 is a 0, the bits written into these locations are transmitted as the J1 byte stream. When control bits EXJ1 and POHRAM are a 1, the external POH interface J1 bytes are written into these locations, and are also transmitted. When control bit EXJ1 is a 1, and POHRAM is a 0, the external POH interface J1 bytes are transmitted and this location holds the microprocessor-written J1 values. Bit 7 in this location corresponds to bit 1 in the transmitted J1 byte.

RECEIVE POH REGISTER DESCRIPTIONS

The transmission of the POH byte in the add direction, and the processing of the POH bytes in the drop direction is enabled when a high is placed on the $\overline{\text{POHDIS}}$ lead.

Address	Bit	Symbol	Description
75	7-0	C2 Compare Byte	**C2 Path Signal Label Compare Byte:** The bits in this location are written by the microprocessor and are compared against the received C2 value for path signal label mismatch detection. Bit 7 in this location corresponds to bit 1 in the C2 byte.
78	7-0	B3 Byte	**B3 Received Byte:** This location contains the received B3 parity byte value received each frame. Bit errors are counted in a 16-bit counter located at 40H (low order byte) and 41H (high order byte). Block errors (one or more parity errors) are counted in an 8-bit counter located at 4AH. Bit 7 in this location corresponds to bit 1 in the B3 byte.
79	7-0	C2 Received Signal Label	**C2 Received Signal Label Byte:** This location is the received C2 byte value received each frame. The received C2 byte is compared against the microprocessor-written value in location 75H. Bit 7 in this location corresponds to bit 1 in the C2 byte.
7A	7-0	Received G1 Byte	**Received G1 Byte:** This location is the received G1 byte value received each frame. The bit relationship is the following. 1 2 3 4 5 6 7 8 G1 Byte 7 6 5 4 3 2 1 0 This location FEBE RDI Unassigned
7B	7-0	F2	**F2 Received Byte:** This location is the received F2 byte value received each frame. Bit 7 in this location corresponds to bit 1 in the F2 byte.
7C	7-0	H4	**H4 Received Byte:** This location is the received H4 byte value received each frame. Bit 7 in this location corresponds to bit 1 in the H4 byte.
7D	7-0	Z3	**Z3 Received Byte:** This location is the received Z3 byte value received each frame. Bit 7 in this location corresponds to bit 1 in the Z3 byte.
7E	7-0	Z4	**Z4 Received Byte:** This location is the received Z4 byte value received each frame. Bit 7 in this location corresponds to bit 1 in the Z4 byte.
7F	7-0	Z5	**Z5 Received Byte:** This location is the received Z5 byte value received each frame. Bit 7 in this location corresponds to bit 1 in the Z5 byte.
C0 to FF	7-0	Received J1 Message	**Path Trace Message Microprocessor Read feature:** The received J1 message bytes are stored into this memory segment. The 16-byte message is allocated to the C0H to CFH memory segment, when control bit CCITT is a 1. When CCITT is 0, the memory segment is configured for 64 bytes. The incoming message is written in with no specific starting address, and in a rotating fashion, and any incoming J1 byte is written into the next sequential RAM location. However, when CCITT and J1COM are both set to 1 and the received 16-byte J1 message has a valid multiframe alignment pattern and is stable (J1LOL=0), the bits written into C0H-CFH will be aligned such that the J1 Byte with the start of multiframe indication will be in location C0H. The values in C0H to CFH will be the “debounced” stable message.

Address	Bit	Symbol	Description
F0 to FF	7-0	Compare J1 Message	**Path Trace Message Compare feature:** The microprocessor writes into this 16-byte memory segment the expected J1 message (multiframe bits and CRC as required) when CCITT is 1 and J1COM is 1. This message is then compared against the received J1 byte for the correct message. The starting address of the message must be written to location F0H (multiframe value of 1). The L4M performs the alignment of the incoming message against this message segment.

PERFORMANCE COUNTERS DESCRIPTIONS

All performance counters globally can be configured to be either saturating or non-saturating with a roll over in count. Writing a 1 to control bit COR (bit 0 in register location 13H) conditions all counters to be non-saturating. Reading a non-saturating counter will not clear the counter. When the counters are configured to be saturating, the counter will clear on a microprocessor read cycle. All performance counters are cleared simultaneously when a 1 is written to control bit RSETC. This bit is self clearing and does not require a 0 to be written to it. When reading a 16-bit counter, the low order byte must be read first.

Address	Bit	Symbol	Description
40 41	7-0	B3 Counter	**B3 Byte Parity Error 16-bit counter**: Counts the number of B3 BIP-8 parity error indications that have been detected between the received B3 value and the calculated value. The low order counter value is held in location 40H. The high order counter value is in held in location 41H. Bit 0 in 40H is the LSB.
42 43	7-0	FEBE Counter	**Far End Block Error 16-bit Counter:** When control bit FEBEBC is a 0, this counter counts the number of FEBE error count indications received in bits 1 through 4 of the G1 byte. The maximum number of errors counted per frame is 8. Values other than between 1 thru 8 are counted as 0 errors. The low order counter value is held in location 42H. The high order counter value is in held in location 43H. When control bit FEBEBC is a 1, the number of FEBE blocks in error are counted instead of the FEBE count. Bit 0 in 42H is the LSB.
44 45	7-0	Analyzer Counter	**Analyzer 16-bit Error Counter:** Enabled when control bit ANAEN is a 1, and when the analyzer is in lock. Counts the number of errors received in the received 2^{23}-1 PRBS pattern. The low order counter value is held in location 44H. The high order counter value is in held in location 45H. Bit 0 in 44H is the LSB.
46 47	7-0	Transmit Framing Error Counter	**Transmit 140 Mbit/s Framing Pattern 16-bit Error Counter:** After frame alignment, this counter counts the number of transmit errored framing patterns in the G.751 signal. The low order counter value is held in location 46H. The high order counter value is in held in location 47H. Bit 0 in 46H is the LSB.
48 49	7-0	Receive Framing Error Counter	**Receive 140 Mbit/s Framing Pattern 16-bit Error Counter:** Enabled when control bit BSAISE is a 0 or when BSAISE is 1 and the L4M is not generating a receive AIS. After frame alignment, this counter counts the number of received errored framing patterns in the G.751 signal. The low order counter value is held in location 48H. The high order counter value is in held in location 47H. Bit 0 in 48H is the LSB.

Address	Bit	Symbol	Description
4A	7-0	B3 Block Counter	**B3 8-bit Block Error Counter:** Counts the number of B3 blocks that are received in error. Bit 0 is the LSB.
4B	7-0	Positive Justification Counter	**Positive Justification 8-bit Counter:** Counts the number of positive justifications based on the incoming J1 pulse. When the pointer tracking feature is enabled, counts the number of pointer increments. Bit 0 is the LSB.
4C	7-0	Negative Justification Counter	**Negative Justification 8-bit Counter:** Counts the number of negative justifications based on the incoming J1 pulse. When the pointer tracking feature is enabled, counts the number of pointer decrements. Bit 0 is the LSB.
4D	7-0	NDF Counter	**New Data Flag 8-bit Counter.** Enabled when a high is placed on PTEN (pin2), the pointer tracking feature. Counts the number of received NDF (1001, 0001, 1101, 1011, and 1000) detected in bits 1-4 of H11. This counter does not count the NDF in the AIS to NDF state transition of the pointer tracking state machine.
4E 4F	7-0 1-0	Desyn Pointer Offset Counter	**Desynchronizer Pointer Offset Counter:** A 9-bit counter, plus a sign bit, that provides the count of the internal pointer offset counter (i.e., pointer leak buffer offset counter, which is the number of bits that have to be leaked out if the sign bit is 0, or the number of leak times not to leak out a bit if the sign bit is 1) for a microprocessor read cycle, when required. The MSB bit is located in bit 0 in 4FH, followed by bit 7 in 4EH. The sign bit is located in bit 1 in 4FH. The value provided is in the 2's complement form, with a zero value equal to 0. This counter can be used in setting the FLR registers. Further information on this subject is provided in a TranSwitch Application Note, document number TXC-03456-0001-AN, Ed. 1, February 7, 1995.

PACKAGE INFORMATION

The L4M device is packaged in a 144-pin plastic quad flat package (PQFP) suitable for socket or surface mounting, as illustrated in Figure 28.

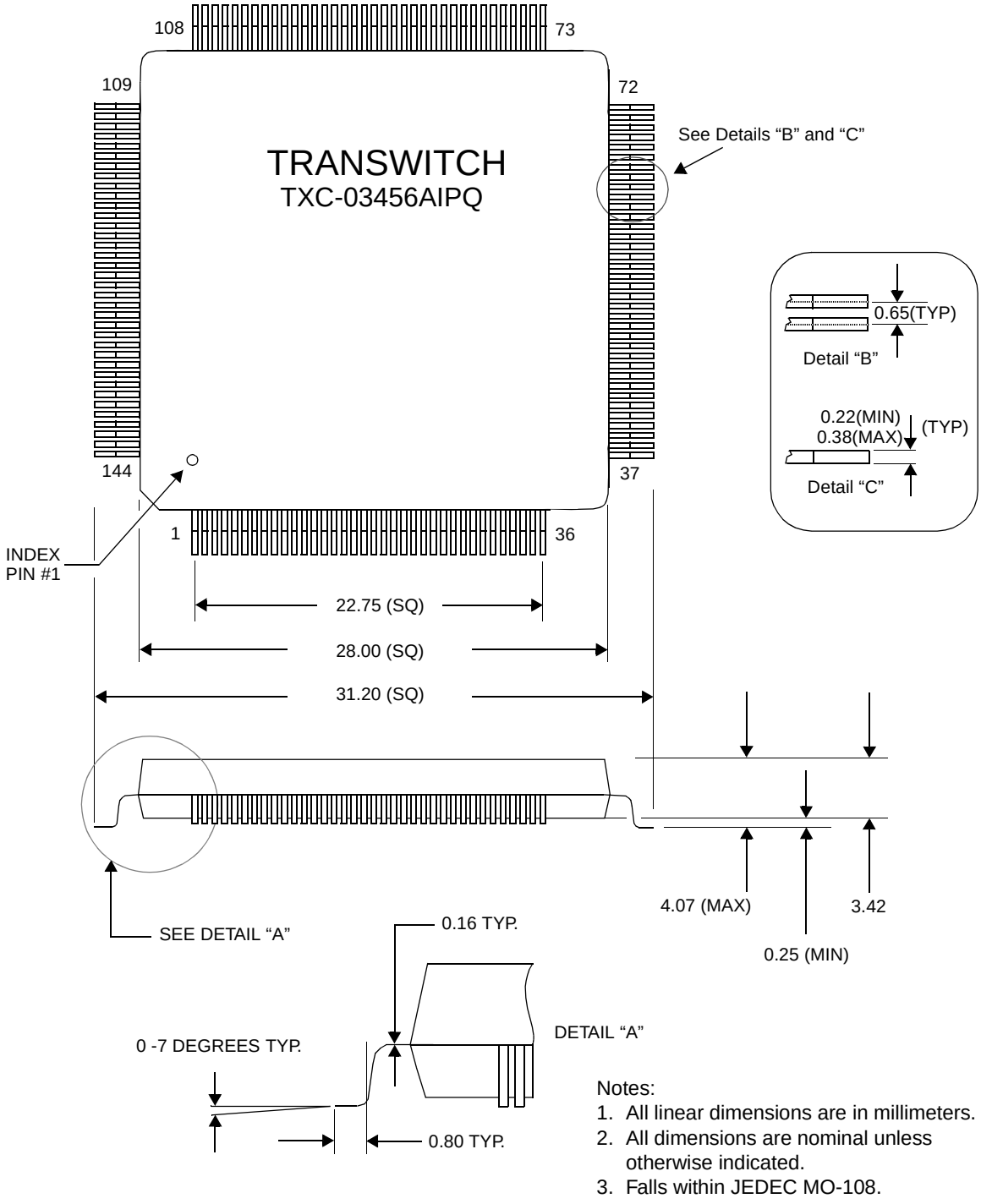


Figure 28. L4M TXC-03456 144-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number:	TXC-03456AIPQ	144-Pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web: www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: 800-669-6857 (within U.S.A.)
Tel: 903-769-3717 (outside U.S.A.)
Fax: 508-650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: 215-697-2179
Fax: 215-697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: 800-433-5177 (within U.S.A.)
Tel: 503-693-6232 (outside U.S.A.)
Fax: 503-693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (within U.S.A.)
Tel: 908-699-5800 (outside U.S.A.)
Fax: 908-336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated L4M Data Sheet that have significant differences relative to the previous, and now superseded, L4M Data Sheet:

Updated L4M Data Sheet:	Edition 1A, January 2000.
Previous L4M Data Sheet:	*PRELIMINARY* Edition 1, June 1995.

The page numbers indicated below of this updated data sheet include changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
All	Removed *PRELIMINARY* document status markings (and associated explanatory text on pages 1 and 93).
2	Updated Table of Contents.
19	Deleted third and fifth row of first table. Changed Max value and deleted Typ value in second table.
89	Added part number to diagram for Figure 28.
90	Changed content of “Related Products” section.
91	Changed content of “Standards Documentation Sources” section.
93	Added “List of Data Sheet Changes” section.
95	Changed content of “Documentation Update Registration Form” section.

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