E2/E3F Device
8-, 34-Mbit/s Framer
TXC-03701B

DATA SHEET

FEATURES

- Framer for ITU-TSS Recommendations:
  - G.742 (8448 kbit/s)
  - G.745 (8448 kbit/s)
  - G.751 (34368 kbit/s)
  - G.753 (34368 kbit/s)
- Line side interface:
  - Rail or NRZ
- HDB3 codec for rail I/O
- Terminal side interface:
  - Nibble-parallel
  - Bit-serial
- Transmit reference generator for serial I/O
- Microprocessor or control leads
- Service bit I/O port
- Pin-selectable transmit line clock polarity
- 68-pin plastic leaded chip carrier

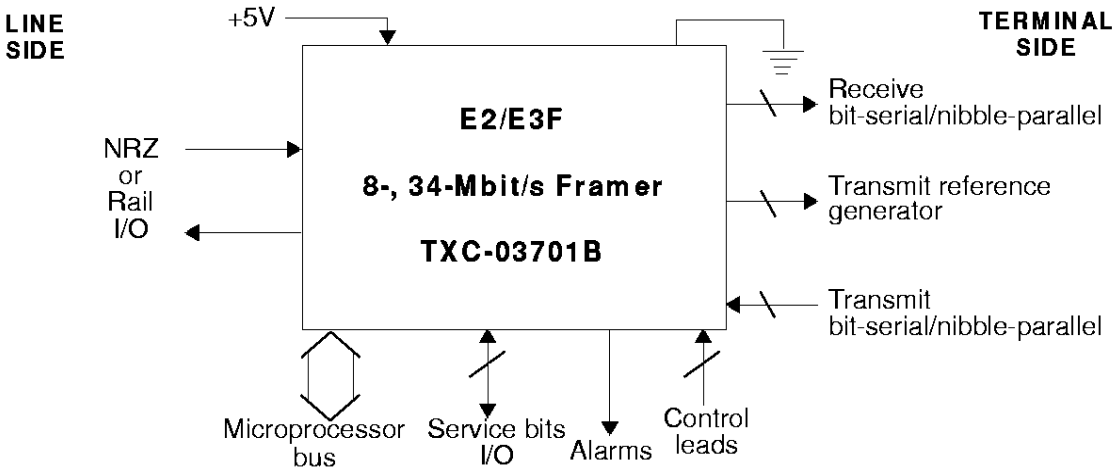
DESCRIPTION

The E2/E3 Framer (E2/E3F) is a CMOS VLSI device that provides the functions needed to frame a wideband payload to one of four ITU-TSS Recommendations: G.742, G.745, G.751, or G.753. The E2/E3F interfaces to line circuitry with either rail or NRZ signals. On the terminal side, the interface can be either nibble-parallel or bit-serial. The nibble interface clocks are gapped for the service bits, framing bits and the BIP-4 option, if selected. For the serial interface, a transmit reference generator is provided.

The E2/E3F can be operated with or without a microprocessor. When interfaced with a microprocessor, the E2/E3F provides an 8-byte memory map for control, performance counters and alarm status. The E2/E3F provides a transmit and receive interface port for accessing the overhead bits from each of the four recommendations. The overhead bits can also be accessed by the microprocessor via the memory map.

APPLICATIONS

- Line terminals
- Wideband data or video transport
- Test equipment
- Multiplexer systems



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TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 • USA • Tel: 203-929-8810 • Fax: 203-926-9453

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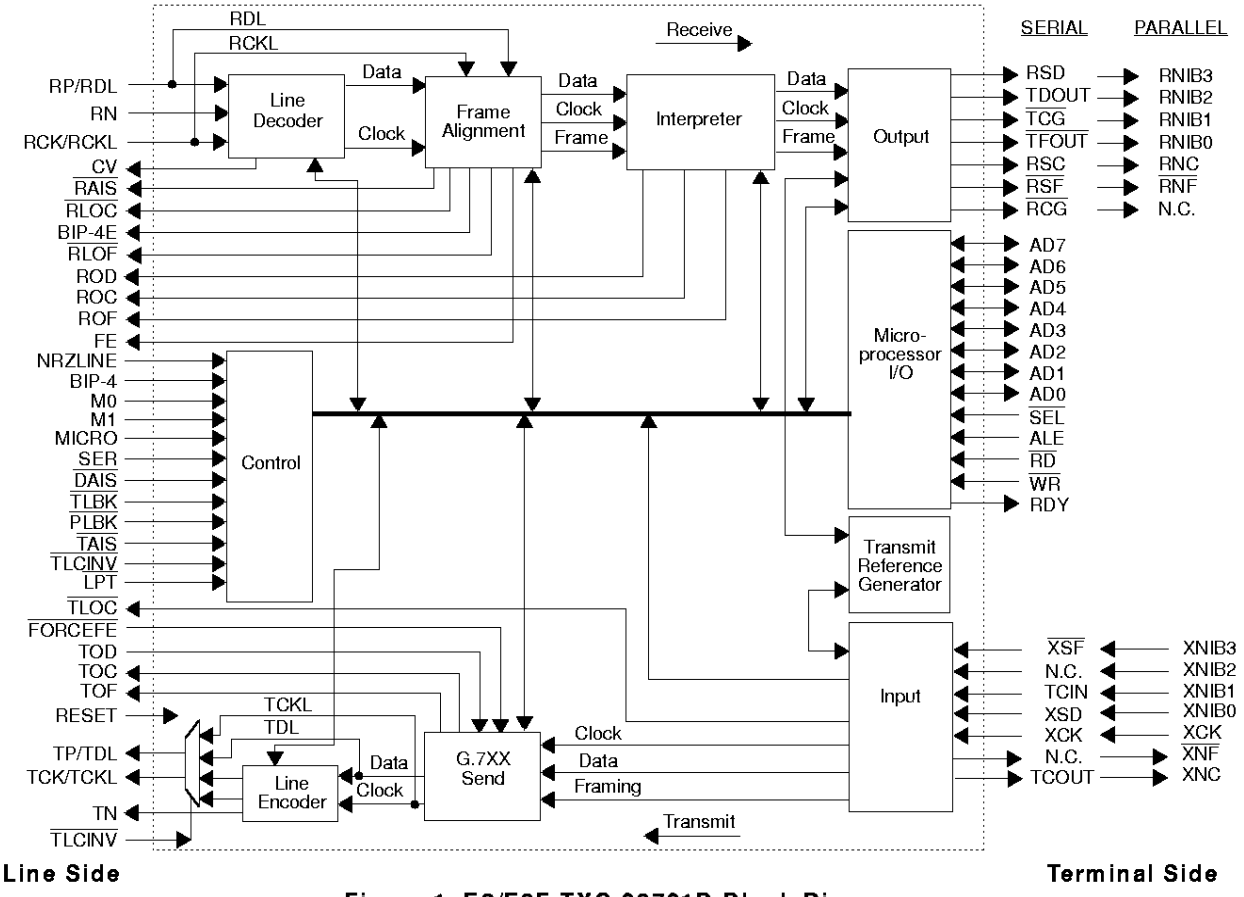


Figure 1. E2/E3F TXC-03701B Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram for the E2/E3F is shown in Figure 1. The E2/E3F receives a line side NRZ data signal (RDL) and clock signal (RCKL), or a positive (RP) and negative (RN) rail signal and clock signal (RCK), from a TranSwitch MRT, or from another line interface circuit. The selection of the line interface, rail or NRZ, is controlled by the external lead labeled NRZLINE. Indications of HDB3 coding violation errors are detected in the Line Decoder Block and are provided on an external signal lead (CV) as pulses. Coding violation errors are also counted in an 8-bit saturating counter accessed by the microprocessor through the memory map. A coding violation is not part of the standard HDB3 zero-substitution code, and occurs because of noise or other impairments on the line.

The selection of one of the four G.7XX framing formats (G.742, G.745, G.751, and G.753), which are supported by the E2/E3F, is determined by external control leads (M1 and M0), or states written into the memory map by the microprocessor. The Frame Alignment Block performs frame alignment and alarm detection. It detects Loss of Frame ($\overline{\text{RLOF}}$), Loss of Clock ($\overline{\text{RLOC}}$), and performs AIS detection ($\overline{\text{RAIS}}$) and BIP-4 (Bit Interleaved Parity-4) detection (BIP-4E) when this feature is enabled in the nibble-parallel mode. Loss of clock is detected whether the clock is stuck high or low. A framing error (FE) output is also provided to indicate when any of the framing bits in the G. 7XX frame are in error. Loss of the receive clock or framing normally causes AIS to be inserted into the terminal side data stream. However, for some applications, receive data is required on the terminal side regardless of frame alignment. The disable AIS ($\overline{\text{DAIS}}$) control lead permits the E2/E3F to provide receive data in the presence of loss of frame. The external alarm indications (latched and unlatched states) are provided in the memory map, and unlatched alarm indications are provided at signal leads.

The service bits are defined as bits 11 and 12 for G.742 and G.751, as listed in Figure 2. The service bits for G.745 and G.753 are defined as bits 5 through 8 in sets II and III. The receive service bit interface consists of the following signals: data output signal (ROD), clock output signal (ROC), and framing pulse (ROF). The clock signal (ROC) is gapped and is provided for clocking out the service bits. The service bit states are also written by the Interpreter Block into E2/E3F memory locations, which can be read by the microprocessor if the signaling rate is low.

G.742

1	11	12	212(Set I)	424(II)	636(III)	844	848(IV)
1111010000	s	s	DATA	DATA	DATA	DATA	BIP-4 if selected

G.745

1	264(I)	268	272	528(II)	532	536	792(III)	1052	1056(IV)
11100110	DATA	jc	s	DATA	jc	s	DATA	DATA	BIP-4 if selected

G.751

1	11	12	384(Set I)	768(II)	1152(III)	1532	1536(IV)
1111010000	s	s	DATA	DATA	DATA	DATA	BIP-4 if selected

G.753

1	716(I)	720	724	1432(II)	1436	1440	2144	2148(III)
111110100000	DATA	jc	s	DATA	jc	s	DATA	BIP-4 if selected

Note:
1. The leading segment of the frame (starting at bit 1) is the frame alignment signal pattern.
2. s indicates the service bits.
3. jc indicates four justification control bits. In sets where DATA is not preceded by service bits, the first 4 or 8 bits of DATA may be associated with justification.

Specifications	Service Bits	No. of Bits in Frame	Frame Alignment Signal Pattern	Bit Rate (kbit/s)
G.742	11,12	848	1111010000	8448
G.745	5-8 Set II (269-272) 5-8 Set III (533-536)	1056	11100110	8448
G.751	11,12	1536	1111010000	34368
G.753	5-8 Set II (721-724) 5-8 Set III (1437-1440)	2148	111110100000	34368

Figure 2. G.7XX Frame Contents Summary

The E2/E3F terminal side Output Block provides either a bit-serial or a nibble-parallel interface. The interface is selected by an external control lead (SER) or by setting a control bit in the memory map. The bit-serial interface consists of the following signals: a data output signal (RSD), a clock output signal (RSC), a receive clock gapped output signal ($\overline{\text{RCG}}$), and a framing pulse ($\overline{\text{RSF}}$). The receive clock gapped signal ($\overline{\text{RCG}}$) is active low during the framing and service bit times. The nibble-parallel interface consists of the following signals: a data output signal having a nibble format (RNIB3 through RNIB0), a clock output signal (RNC), and a framing pulse ($\overline{\text{RNF}}$). Signal leads are shared for the two interfaces (RSD and RNIB3, RSC and RNC, $\overline{\text{RSF}}$ and $\overline{\text{RNF}}$) and with the transmit reference generator, which is used in the serial mode only. The RNIB3 bit corresponds to the first bit received in a four-bit bit-serial stream segment. In the nibble mode, the framing pattern, service bits and BIP-4 nibble are not provided at the interface. The receive nibble clock (RNC) is gapped during framing pattern, service bit and BIP-4 times.

The transmitter operates independently of the receiver, unless the loop timing feature is selected. When the loop timing feature is selected, the receive clock becomes the transmitted clock. In the transmit direction, the terminal side bit-serial interface consists of the following signals: a data input signal (XSD), a clock input signal (XCK), and a framing pulse ($\overline{XSF}$). The nibble-parallel interface consists of the following signals: a data input signal having a nibble format (XNIB3 - XNIB0), a clock input signal (XCK), a framing output pulse ($\overline{XNF}$), and a nibble output clock signal (XNC). The leads are shared between the two interfaces and with the E2/E3F transmit reference generator in order to minimize the pin count. The XNIB3 bit corresponds to the first bit transmitted in a four-bit bit-serial stream segment. The transmit nibble clock (XNC) is stretched to accommodate the framing pattern, service bit and BIP-4 times. The E2/E3F also detects loss of clock ($\overline{TLOC}$) whether the input clock is stuck high or low.

The transmitter has control leads for BIP-4 generation (BIP-4) and inserting AIS ($\overline{TAIS}$). When the E2/E3F is operating with a microprocessor, the BIP-4 and AIS functions are controlled by the microprocessor. When the BIP-4 option is selected, the BIP-4 is transmitted as the last nibble in the frame format, as shown in Figures 2 and 3.

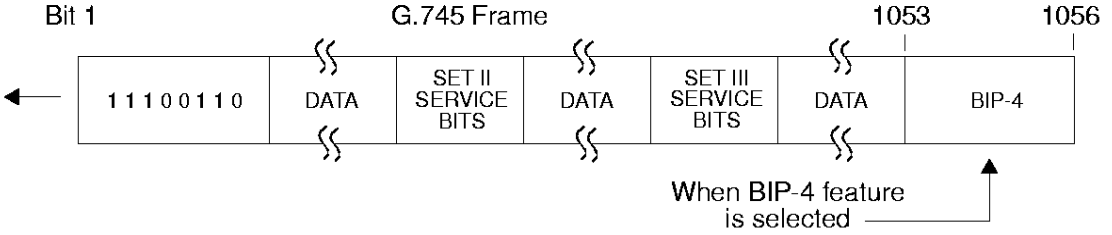


Figure 3. G.745 BIP-4 Location

The transmitted service bits are inserted into the frame format from either an external interface or from memory map locations. The transmit service bit interface consists of the following signals: a data in signal (TOD), a clock output signal (TOC), and a framing pulse (TOF).

To facilitate transmit side multiplexing while operating in the bit-serial mode, the E2/E3F provides a transmit frame reference generator. The transmit frame reference generator accepts an external 8.448 or 34.368 MHz clock signal (TCIN) and produces a clock out signal (TCOUT), a framing pulse ($\overline{TFOUT}$), a clock gap signal ($\overline{TCG}$), and a data signal (TDOUT). The data signal consists of G.7XX framing bits and zeros elsewhere. The purpose of the transmit reference signals is to fix the transmit time-base for the terminal payload multiplexer circuitry.

The selection of the transmit line interface, rail or NRZ, is controlled by the state present on the NRZLINE control lead, which also controls the receive interface selection. When the internal HDB3 Encoder Block is bypassed, the transmit line interface consists of a data signal (TDL) and a clock signal (TCKL). When the HDB3 encoder is enabled, the transmit line interface consists of positive (TP) and negative (TN) rail signals and a clock signal (TCK). The TCK/TCKL clock may be inverted by setting $\overline{TLCINV}$ low.

Input pins are provided for activating terminal loopback ($\overline{TLBK}$) and payload loopback ($\overline{PLBK}$).

A high placed on the microprocessor control lead (MICRO) selects the microprocessor interface. All the external control leads, except the loop timing ($\overline{LPT}$), receive AIS disable ($\overline{DAIS}$), and the line interface (NRZLINE) control leads are disabled when the microprocessor interface is selected. The E2/E3F provides pull-up resistors for the active low control leads.

The microprocessor interface consists of eight bidirectional data and address leads (AD7 - AD0), along with four microprocessor control input leads and a ready (RDY) output signal.

PIN DIAGRAM

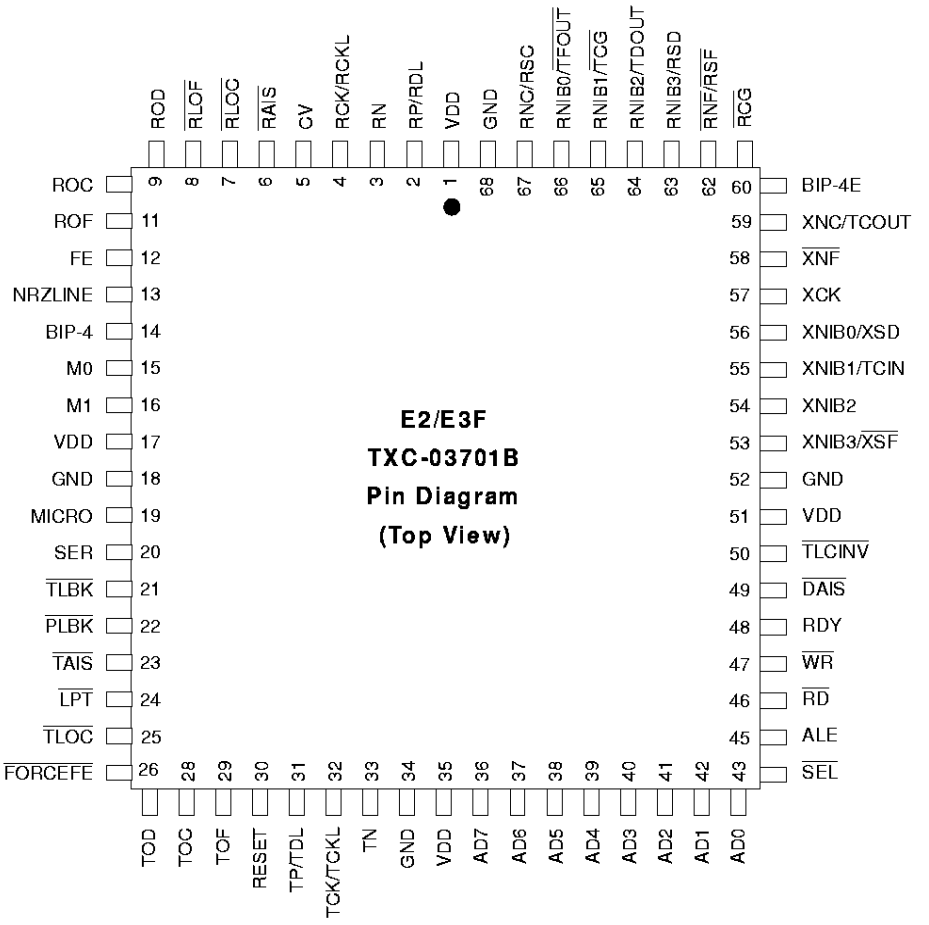


Figure 4. E2/E3F TXC-03701B Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1,17,35,51	P		**VDD:** +5-volt supply voltage, +/- 5%
GND	18,34,52,68	P		**Ground:** 0 volts reference.

*Note: I = Input; O = Output; P = Power

LINE SIDE RECEIVE SIGNALS

Symbol	Pin No.	I/O/P	Type *	Name/Function
RP/RDL	2	I	TTLp	**Receive Positive Rail/Receive NRZ Data:** Positive rail input data is clocked into the E2/E3F on negative transitions of the clock signal RCK/RCKL. The HDB3 codec for rail operation is enabled by applying a low to the NRZLINE signal lead. Receive NRZ data is clocked into the E2/E3F on positive transitions of the clock signal RCK/RCKL. The NRZ mode is enabled by applying a high to the NRZLINE signal lead.
RN	3	I	TTLp	**Receive Negative Rail Data:** Negative rail input data is clocked into the E2/E3F on negative transitions of the clock signal RCK/RCKL. The HDB3 codec for rail operation is enabled by applying a low to the NRZ-LINE signal lead.
RCK/RCKL	4	I	TTLp	**Receive Clock Rail/NRZ:** The receive clock is used for clocking in the rail/NRZ data signals and is used as the time base for receiver operation.

LINE SIDE TRANSMIT SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TP/TDL	31	O	TTL8mA	**Transmit Positive Rail/Transmit NRZ Data:** Positive rail data is clocked out of the E2/E3F on positive transitions of the clock signal TCK/TCKL when pin 50 is high and on negative transitions of the clock when pin 50 is low. The HDB3 codec for rail operation is enabled by applying a low to the NRZLINE signal lead. Transmit NRZ data is clocked out of the E2/E3F on negative transitions of the clock signal TCK/TCKL. The NRZ mode is enabled by applying a high to the NRZLINE signal lead.
TCK/TCKL	32	O	TTL8mA	**Transmit Clock Rail/NRZ:** The transmit clock is used for clocking out the rail/NRZ data signals. The TCK/TCKL clock signal is derived from the XCK clock. Note: When XCK is removed, the framer then uses TCIN to generate TCK/TCKL (in serial mode only). If both XCK and TCIN are removed, TCK/TCKL is derived from RCK/RCKL. This clock may be inverted by using control pin 50 (TLCINV).
TN	33	O	TTL8mA	**Transmit Negative Rail Data:** Negative rail output data is clocked out of the E2/E3F on positive transitions of the clock signal TCK/TCKL when pin 50 is high and on negative transitions of the clock when pin 50 is low. The HDB3 codec for rail operation is enabled by applying a low to the NRZLINE signal lead.

* Note: See Input, Output and I/O Parameters section for Type definitions.

TERMINAL INTERFACE SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RCG}}$	61	O	TTL4mA	**Receive Clock Gapped:** An active low signal which indicates the receive framing and service bit locations. The $\overline{\text{RCG}}$ signal is provided in the serial mode only.
$\overline{\text{RNF}}/\overline{\text{RSF}}$	62	O	TTL4mA	**Receive Framing Pulse:** This active low framing pulse is synchronous with the last data nibble RNIB(3-0) for the terminal side nibble-parallel interface, and with the first bit in the frame for the bit-serial interface.
RNIB3/RSD	63	O	TTL4mA	**Receive Nibble Bit 3/Receive Serial Data:** Bit 3 is the most significant bit in the nibble and corresponds to the first bit received in the nibble. The framing pattern, service bits, and BIP-4 nibble are not provided as parallel data. In the serial mode, all bits, including the framing pattern and service bits, are provided.
RNIB2/ TDOUT	64	O	TTL4mA	**Receive Nibble Bit 2/Transmit Reference Generator Data Output:** Bit 2 in nibble mode. The reference generator is enabled in the serial mode. The output data signal consists of all ones in place of the framing bits and zeros elsewhere in the frame. The TDOUT signal is generated from the input clock (TCIN).
RNIB1/$\overline{\text{TCG}}$	65	O	TTL4mA	**Receive Nibble Bit 1/Transmit Reference Generator Clock Gap Signal:** Bit 1 in nibble mode. The reference generator is enabled in the serial mode. The active low $\overline{\text{TCG}}$ signal indicates the location of the framing pattern and the service bits in the frame. The $\overline{\text{TCG}}$ signal is generated from the input clock (TCIN).
RNIB0/ $\overline{\text{TFOUT}}$	66	O	TTL4mA	**Receive Nibble Bit 0/Transmit Reference Generator Framing Pulse:** Bit 0 is the least significant bit in the nibble and is the last bit received. The reference generator is enabled in the serial mode. The active low $\overline{\text{TFOUT}}$ signal is one clock cycle (TCOUT) wide, and is synchronous with the first bit in the frame.
RNC/RSC	67	O	TTL4mA	**Receive Nibble Clock/Receive Serial Clock:** The nibble and serial clocks are derived from the line side rail/NRZ clock signal (RCK/RCKL). A received nibble is clocked out on positive transitions of RNC. RNC is gapped during framing pattern, service bit and BIP-4 bit times. Serial data is clocked out on positive transitions of RSC.

Symbol	Pin No.	I/O/P	Type	Name/Function
XNIB3/$\overline{XSF}$	53	I	TTLp	**Transmit Nibble Bit 3/Transmit Serial Framing Pulse:** For the terminal side parallel interface, bit 3 in the transmitted nibble is the most significant bit and corresponds to the first bit transmitted in the nibble. When the terminal interface is serial, the negative framing pulse is synchronous with the first bit in the frame. It is recommended that the framing pulse ($\overline{TFOUT}$) and other signals generated by the transmit reference generator be used as the transmit framing pulse, and for multiplexing the data into the frame.
XNIB2	54	I	TTLp	**Transmit Nibble Bit 2:** Bit 2 in the transmit nibble.
XNIB1/TCIN	55	I	TTLp	**Transmit Nibble Bit 1/Transmit Reference Generator Clock In:** Bit 1 in the transmit nibble. For a serial interface, the reference clock (TCIN) is used to derive the clock out (TCOUT), data signal (TDOUT), framing pulse ($\overline{TFOUT}$), and gapped clock signal ($\overline{TCG}$). The reference generator signals are provided for multiplexing the external payload data into the serial frame. The E2/E3F requires a transmit clock having a frequency of 8448 kHz with a stability of +/- 30 ppm to meet the clock tolerance specified in ITU-TSS Recommendations G.742 and G.745. For Recommendations G.751 and G.753, the required clock frequency is 34368 kHz with a stability of +/- 20 ppm.
XNIB0/XSD	56	I	TTLp	**Transmit Nibble Bit 0/Transmit Serial Data:** For the terminal side parallel interface, bit 0 is the least significant bit in the nibble and the last bit from the nibble that is transmitted. For a serial interface, the input must consist of all the bits in the frame. The E2/E3F inserts a new framing pattern and the service bits (from the external interface or the memory map) into the transmit data stream determined by the location of the framing pulse ($\overline{XSF}$).
XCK	57	I	TTLp	**Transmit Clock:** For the terminal side parallel interface, the transmit clock is used for all transmit timing functions, including deriving the nibble output clock (XNC) and framing pulse ($\overline{XNF}$). The E2/E3F requires a transmit clock having a frequency of 8448 kHz with a stability of +/- 30 ppm to meet the clock tolerance specified in ITU-TSS Recommendations G.742 and G.745. For Recommendations G.751 and G.753, the required clock frequency is 34368 kHz with a stability of +/- 20 ppm. For the serial interface, this clock may be derived from the transmit reference generator clock output (TCOUT). The duty cycle must be 50 ± 5%.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{XNF}$	58	O	TTL4mA	**Transmit Nibble Framing Pulse:** The nibble framing pulse and clock signal (XNC) are provided for multiplexing nibble data into the E2/E3F from external circuitry. The negative framing pulse identifies the first bit in the frame.
XNC/TCOUT	59	O	TTL8mA	**Transmit Nibble Clock/Transmit Reference Generator Clock Out:** The nibble clock is derived from the transmit clock (XCK) and is used as a time base for clocking data out of the external multiplexer and into the E2/E3F. XNC is gapped during the framing pattern, service bit and BIP-4 bit times. Data is clocked in on positive transitions. TCOUT is derived from the input clock (TCIN), and has the same duty cycle.

SERVICE BIT INTERFACE SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
ROD	9	O	TTL8mA	**Receive Service Data Bits:** The service bits for the G.742 and G.751 recommendations are defined as bits 11 and 12. For the G.745 and G.753 recommendations, the service bits are defined as 5 through 8 in Sets II and III.
ROC	10	O	TTL8mA	**Receive Service Bits Clock:** A gapped clock that clocks out the service bits on positive transitions.
ROF	11	O	TTL8mA	**Receive Service Bits Framing Pulse:** A positive framing pulse that is synchronous with the first bit in the frame.
TOD	27	I	TTLp	**Transmit Service Data Bits:** The service bits for G.742 and G.751 are bits 11 and 12. For G.745 and G.753, the service bits are 5 through 8 in Sets II and III. When the E2/E3F is configured to work with a microprocessor, bit 0 (OHI/O) in location 00H must be written with a one to enable TOD.
TOC	28	O	TTL8mA	**Transmit Service Bits Clock:** A gapped clock that clocks in the service bits on positive transitions. The clock is active only for clocking in the transmit service data bits (TOD).
TOF	29	O	TTL8mA	**Transmit Service Bits Framing Pulse:** A positive framing pulse that is synchronous with the first bit in the frame.

MICROPROCESSOR INTERFACE SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
AD(7-0)	36-43	I/O	TTL I/O	**Address/Data Bus:** These leads constitute the time-multiplexed address and data bus for accessing the registers which reside in the E2/E3F. Only AD(2-0) are required for address input.
$\overline{SEL}$	44	I	TTLp	**Select:** A low enables the microprocessor to access the E2/E3F memory map for control, status, and alarm information (Note 1).
ALE	45	I	TTLp	**Address Latch Enable:** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle (Note 1).
$\overline{RD}$	46	I	TTLp	**Read:** An active low signal generated by the microprocessor for reading the registers which reside in the memory map. The E2/E3F memory map is selected by placing a low on the select lead (Note 1).
$\overline{WR}$	47	I	TTLp	**Write:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The E2/E3F memory map is selected by placing a low on the select lead (Note 1).
RDY	48	O	TTL Open Drain	**Ready:** An active high is an E2/E3F acknowledgment to the microprocessor that the addressed memory map location can complete the data transfer.

*Note 1: When MICRO (pin 19) is tied low, the microprocessor interface is disabled. This microprocessor interface input pin has an internal pull-up resistor and can be left open.

CONTROL SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
NRZLINE	13	I	TTLp	**Non-Return to Zero Line Selection:** A high enables an NRZ line interface (RP/TP), and causes the HDB3 decoder/encoder to be bypassed. An active low enables the rail interface (RP/RN, and TP/TN) and the HDB3 decoder/encoder.
BIP-4	14	I	TTLp	**Bit Interleaved Parity - 4:** A high enables the BIP-4 function. In the transmit direction, the BIP-4 is calculated for data nibbles only, and is sent as the last nibble in the frame format. In the receive direction, the BIP-4 is calculated for the data bits only and compared against the received value which is present in the last four bits of the frame. An output indication (BIP-4E) occurs when one or more columns do not match. A BIP-4 error mask is provided in the memory map which permits up to four errors to be transmitted. At the terminal interface, the transmit and receive nibble clocks are gapped to accommodate the time that corresponds to the BIP-4 nibble.

Symbol	Pin No.	I/O/P	Type	Name/Function
M1 M0	16 15	I	TTLp	**Mode Control:** The two controls select the operating rate of the E2/E3F according to the table shown below: **M1** / **M0** / **Recommendation** / **Rate (kbit/s)** low / low / G.745 / 8448 low / high / G.742 / 8448 high / low / G.753 / 34368 high / high / G.751 / 34368
MICRO	19	I	TTLp	**Microprocessor Mode:** A high enables the microprocessor interface. When the microprocessor is enabled, the following hardware control leads are disabled: BIP-4, Mode (M0 and M1), Serial I/O (SER), and transmit AIS ($\overline{\text{TAIS}}$). Bits are provided in Address 00H of the memory map for controlling these functions. These bits are inactive when MICRO is low.
SER	20	I	TTLp	**Serial Interface:** A high selects the bit-serial interface for the terminal side interface. A low selects the nibble-parallel interface.
$\overline{\text{TLBK}}$	21	I	TTLp	**Terminal Loopback:** A low enables a transmit-to-receive loopback at the line side.
$\overline{\text{PLBK}}$	22	I	TTLp	**Payload Loopback:** A low enables a receive-to-transmit loopback at the terminal side in the serial mode of operation only.
$\overline{\text{TAIS}}$	23	I	TTLp	**Transmit Alarm Indication Signal:** A low causes an all ones signal (AIS) to be sent in place of a G.7XX frame format.
$\overline{\text{LPT}}$	24	I	TTLp	**Loop Timing:** A low enables the loop timing feature. Loop timing disables the transmit clock and enables the receive clock to be used as the transmit clock.
$\overline{\text{FORCEFE}}$	26	I	TTLp	**Force Framing Error:** An errored framing bit is inserted into the transmit framing pattern upon a high to low transition.
RESET	30	I	TTLp	**Reset:** A positive pulse having a duration of at least 10 transmit clock cycles (XCK) applied to this pin resets the internal counters, logic circuits, and the performance counters and control bits in the memory map to zero. The reset pulse is applied after the power becomes stable.
$\overline{\text{DAIS}}$	49	I	TTLp	**Disable AIS:** A low disables the automatic insertion of AIS into the terminal side receive nibble/serial bit stream.
$\overline{\text{TLCINV}}$	50	I	TTLp	**Transmit Line Clock Invert:** A low inverts the output clock TCK/TCKL when operating in the P and N rail mode.

STATUS AND ALARM SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
CV	5	O	TTL8mA	**Coding Violation:** A positive pulse, one clock cycle wide, is generated when an illegal coding violation is detected. A coding violation is not part of the HDB3 zero-substitution code. A CV occurs because of noise or other impairments occurring on the line. This output is only valid in the P and N rail mode of operation.
$\overline{\text{RAIS}}$	6	O	TTL8mA	**Receive Alarm Indication Signal:** An active low alarm occurs within one millisecond after the E2/E3F detects an all ones condition, including in the presence of a 10^{-5} bit error rate. An incoming signal with a framing pattern and all ones in the data field is not mistaken as an AIS.
$\overline{\text{RLOC}}$	7	O	TTL8mA	**Receive Loss of Clock:** An active low alarm occurs when there are no transitions in the received clock (RCK/RCKL) for 10 clock cycles. Recovery occurs on the first clock transition.
$\overline{\text{RLOF}}$	8	O	TTL8mA	**Receive Loss of Frame:** An active low alarm occurs when frame cannot be detected in the following modes and conditions: **G.742:** Four consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000 (10-bit pattern). **G.745:** Five consecutive frames lost. Recovery occurs when two consecutive frames are detected. The framing pattern is 11100110 (8-bit pattern). **G.751:** Four consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000 (10-bit pattern). **G.753:** Three consecutive frames lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 111110100000 (12-bit pattern).
FE	12	O	TTL8mA	**Framing Error:** An active high alarm occurs when one or more framing bits are in error. The framing error alarm occurs at the end of the framing pattern and remains high until an error-free framing pattern is received or a loss of frame occurs.
$\overline{\text{TLOC}}$	25	O	TTL8mA	**Transmit Loss of Clock:** An active low alarm occurs when there are no transitions in the transmit clock (TCK) for 10 clock cycles. Recovery occurs on the first clock transition.
BIP-4E	60	O	TTL8mA	**BIP-4E:** A positive pulse occurs when the comparison between the received BIP-4 value and the calculated value does not match in a column.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		1	Watts
Ambient operating temperature	T_A	-40	+85	°C
Operating junction temperature	T_J		150	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		46	48	°C/W	0 ft/min linear airflow
Thermal resistance - junction to case			12	°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			125	mA	
P_{DD}			675	mW	Inputs switching

THROUGHPUT DELAYS

E2

Path	Delay (bit times)
Rx line input to Rx terminal output	TBD
Tx terminal input to Tx line output	TBD

E3

Path	Delay (bit times)
Rx line input to Rx terminal output	TBD
Tx terminal input to Tx line output	TBD

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	
Input capacitance		4.0		pF	

Note: Input has a 72k (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = 4.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = -4.0$
I_{OL}			-4.0	mA	
I_{OH}			4.0	mA	
t_{RISE}		1.2		ns	$C_{LOAD} = 15$ pF
t_{FALL}		1.7		ns	$C_{LOAD} = 15$ pF

OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = 8.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = -8.0$
I_{OL}			-8.0	mA	
I_{OH}			8.0	mA	
t_{RISE}		2.0		ns	$C_{LOAD} = 15$ pF
t_{FALL}		1.9		ns	$C_{LOAD} = 15$ pF

OUTPUT PARAMETERS FOR TTL OPEN DRAIN

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = -8.0$
I_{OL}			-8.0	mA	
t_{FALL}		11.0		ns	$C_{LOAD} = 15$ pF

Note: V_{OH}, I_{OH} and t_{RISE} will depend on external resistance and capacitance.

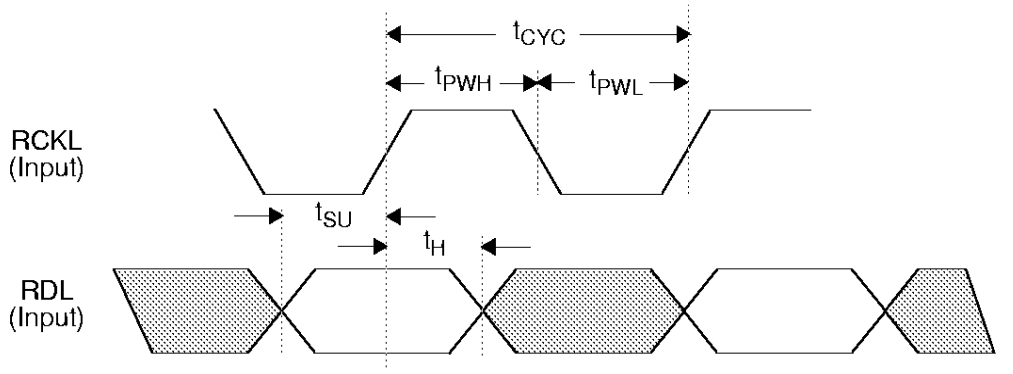
INPUT/OUTPUT PARAMETERS FOR TTL I/O

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	
Input capacitance		7.1		pF	
V_{OH}	2.4	--		V	$V_{DD} = 4.75$; $I_{OH} = 8.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = -8.0$
I_{OL}			-8.0	mA	
I_{OH}		--	8.0	mA	
t_{RISE}		3.3		ns	$C_{LOAD} = 15$ pF
t_{FALL}		7.9		ns	$C_{LOAD} = 15$ pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the E2/E3F are illustrated in Figures 5 through 20, with values of the timing intervals tabulated below the diagrams. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 5. Line Side Receive NRZ Timing



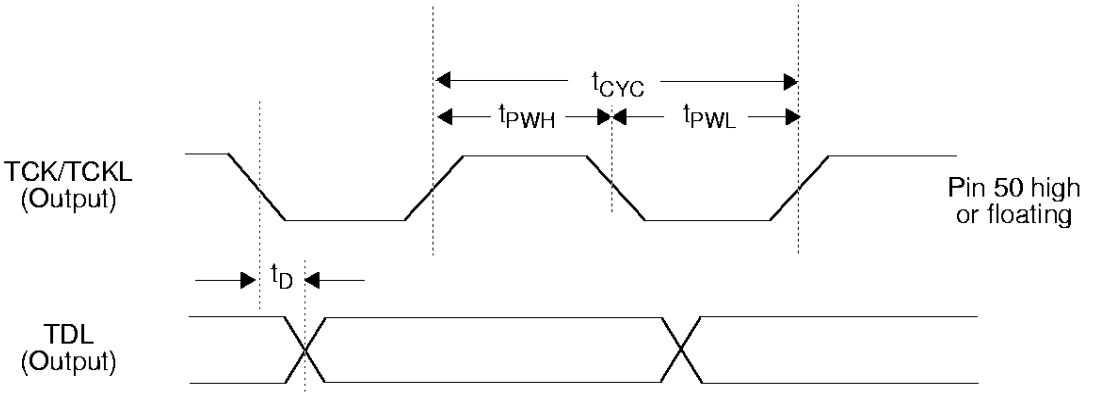
E3

Parameter	Symbol	Min	Typ	Max	Unit
RCKL clock period	t_{CYC}	29.0			ns
RCKL high time	t_{PWH}	12.1	14.6		ns
RCKL low time	t_{PWL}	12.1	14.6		ns
RDL set-up time to RCKL↑	t_{SU}	4.0			ns
RDL hold time after RCKL↑	t_H	4.0			ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
RCKL clock period	t_{CYC}	116.0			ns
RCKL high time	t_{PWH}	46.0	59.2		ns
RCKL low time	t_{PWL}	46.0	59.2		ns
RDL set-up time to RCKL↑	t_{SU}	4.0			ns
RDL hold time after RCKL↑	t_H	4.0			ns

Figure 6. Line Side Transmit NRZ Timing



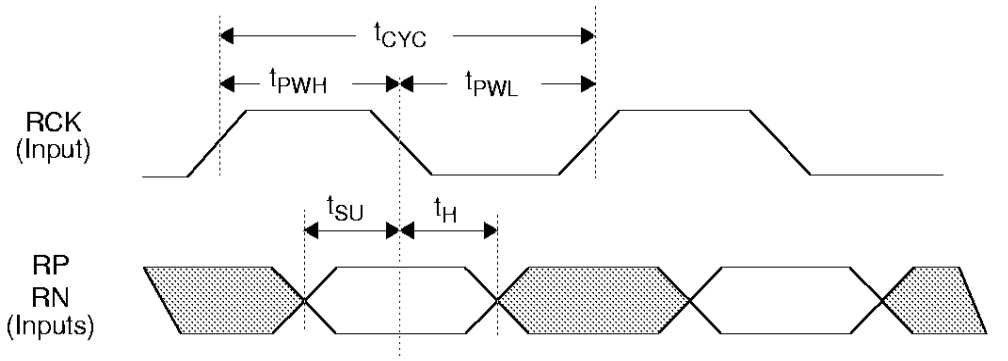
E3

Parameter	Symbol	Min	Typ	Max	Unit
TCKL clock period	t_{CYC}	29.1	29.1		ns
TCKL high time	t_{PWH}	13.1			ns
TCKL low time	t_{PWL}	13.1			ns
TDL delay after TCKL↓	t_D			7.0	ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
TCKL clock period	t_{CYC}	118.4	118.4		ns
TCKL high time	t_{PWH}	53.3			ns
TCKL low time	t_{PWL}	53.3			ns
TDL delay after TCKL↓	t_D			7.0	ns

Figure 7. Line Side Receive Rail Timing



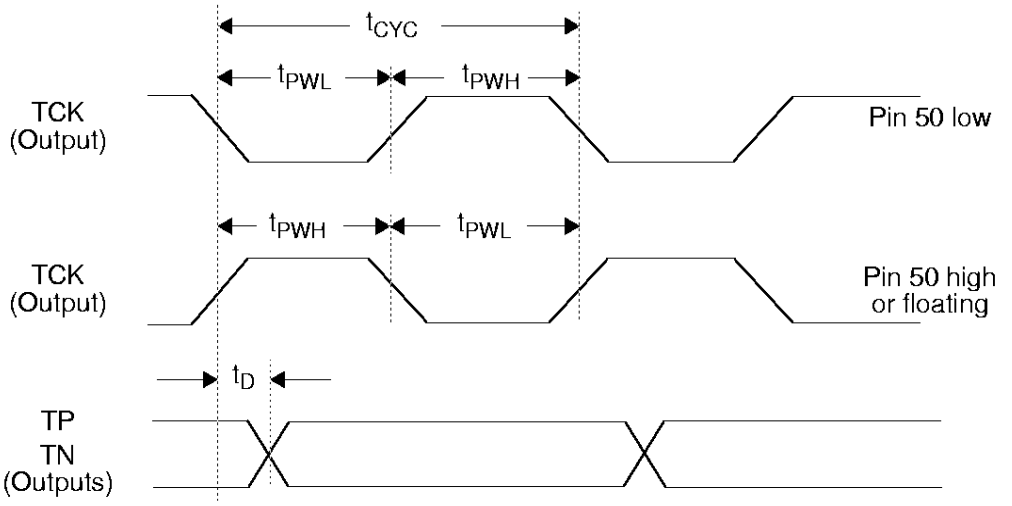
E3

Parameter	Symbol	Min	Typ	Max	Unit
RCK clock period	t_{CYC}	29.0			ns
RCK high time	t_{PWH}	12.1	14.6		ns
RCK low time	t_{PWL}	12.1	14.6		ns
RP/RN set-up time to RCK↓	t_{SU}	4.0			ns
RP/RN hold time after RCK↓	t_H	4.0			ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
RCK clock period	t_{CYC}	116.0			ns
RCK high time	t_{PWH}	46.0	59.2		ns
RCK low time	t_{PWL}	46.0	59.2		ns
RP/RN set-up time to RCK↓	t_{SU}	4.0			ns
RP/RN hold time after RCK↓	t_H	4.0			ns

Figure 8. Line Side Transmit Rail Timing



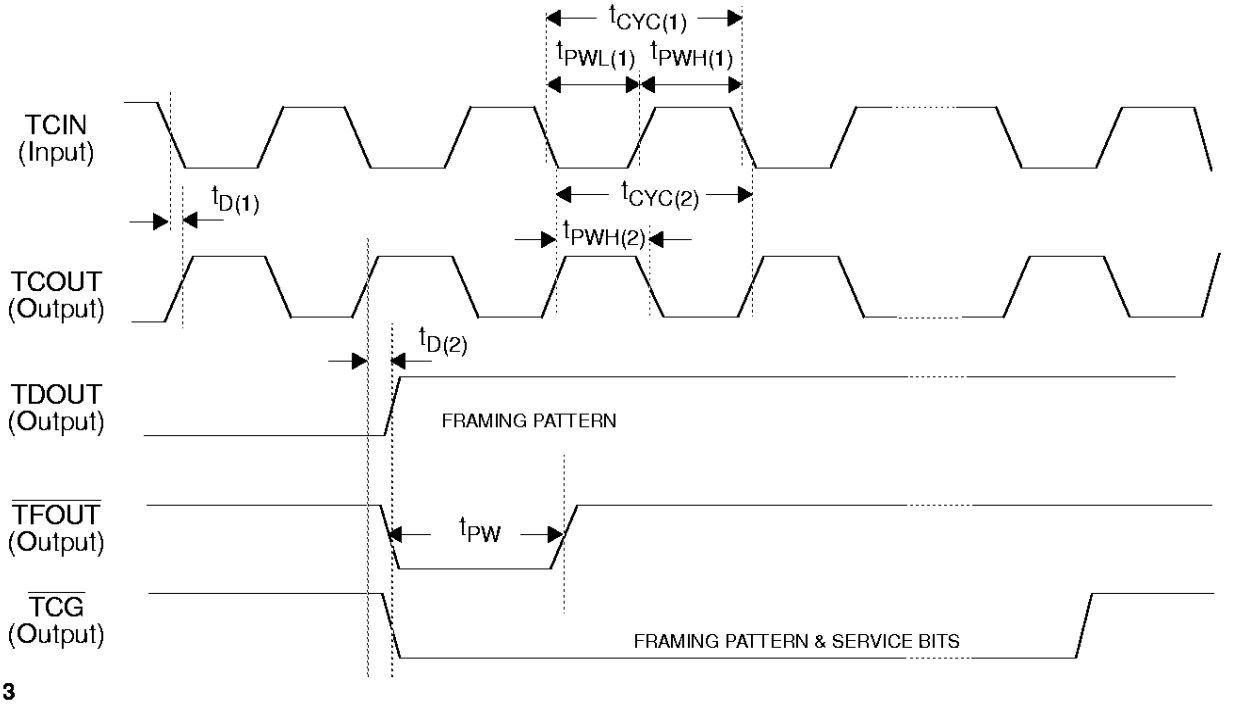
E3

Parameter	Symbol	Min	Typ	Max	Unit
TCK clock period	t_{CYC}	29.1	29.1		ns
TCK high time	t_{PWH}	13.1		16.0	ns
TCK low time	t_{PWL}	13.1		16.0	ns
TP/TN delay after TCK active edge	t_D			7.0	ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
TCK clock period	t_{CYC}	118.4	118.4		ns
TCK high time	t_{PWH}	53.3		65.1	ns
TCK low time	t_{PWL}	53.3		65.1	ns
TP/TN delay after TCK active edge	t_D			7.0	ns

Figure 9. Transmit Reference Generator Timing



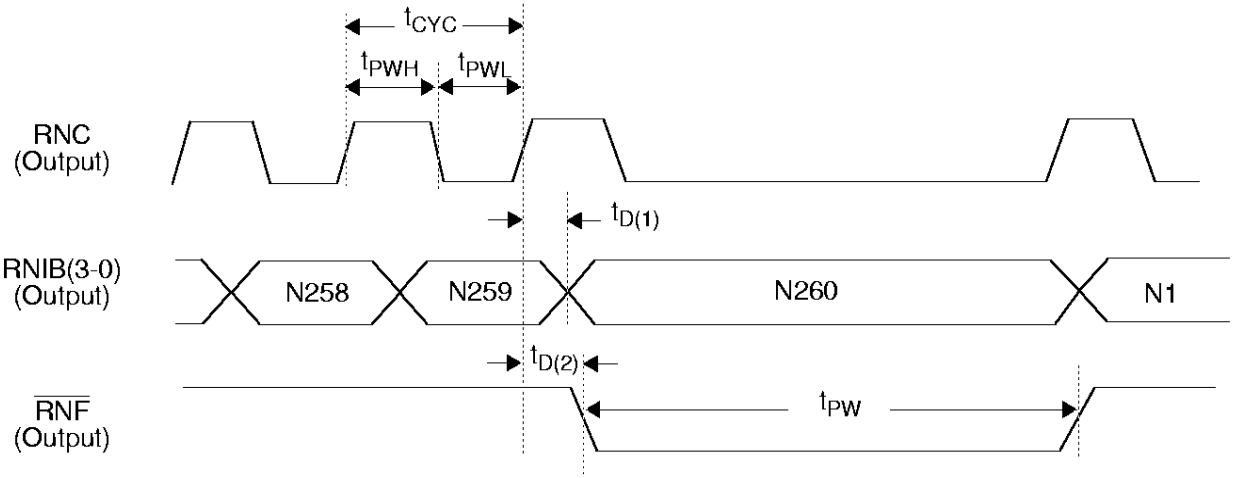
E3

Parameter	Symbol	Min	Typ	Max	Unit
TCIN clock period	$t_{CYC(1)}$	29.1			ns
TCIN high time	$t_{PWH(1)}$	13.1			ns
TCIN low time	$t_{PWL(1)}$	13.1			ns
TCOUT clock period	$t_{CYC(2)}$	29.1			ns
TCOUT high time	$t_{PWH(2)}$	13.1			ns
TCOUT↑ delay after TCIN↓	$t_{D(1)}$			15.0	ns
TDOUT, $\overline{\text{TFOUT}}$, $\overline{\text{TCG}}$ delay after TCOUT↑	$t_{D(2)}$			7.0	ns
$\overline{\text{TFOUT}}$ pulse width	t_{PW}		1 $t_{CYC(1)}$		ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
TCIN clock period	$t_{CYC(1)}$	118.4	118.4		ns
TCIN high time	$t_{PWH(1)}$	53.3			ns
TCIN low time	$t_{PWL(1)}$	53.3			ns
TCOUT clock period	$t_{CYC(2)}$	118.4			ns
TCOUT high time	$t_{PWH(2)}$	53.3			ns
TCOUT↑ delay after TCIN↓	$t_{D(1)}$			15.0	ns
TDOUT, $\overline{\text{TFOUT}}$, $\overline{\text{TCG}}$ delay after TCOUT↑	$t_{D(2)}$			7.0	ns
$\overline{\text{TFOUT}}$ pulse width	t_{PW}		1 $t_{CYC(1)}$		ns

Figure 10. Terminal Side Receive Nibble Timing



This waveform diagram shows a G.745 frame with the BIP-4 feature off. The gapped clock period corresponds to the 8-bit (two nibbles) framing pattern.

E2

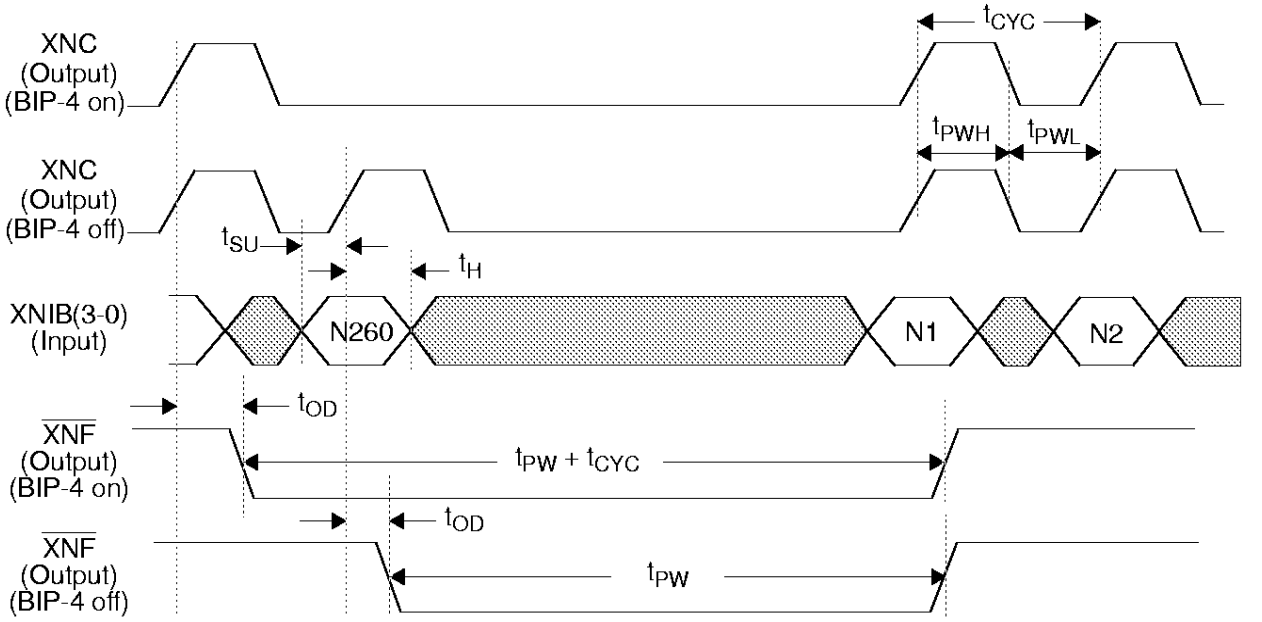
Parameter	Symbol	Min	Typ	Max	Unit
RNC clock period	t_{CYC}	473.0			ns
RNC high time	t_{PWH}	213.0			ns
RNC low time	t_{PWL}	213.0			ns
RNIB delay after RNC↑	$t_{D(1)}$			7.0	ns
$\overline{RNF}$ delay after RNC↑	$t_{D(2)}$			7.0	ns
$\overline{RNF}$ pulse width (G.745)	t_{PW}	947.0			ns
$\overline{RNF}$ pulse width (G.742)	t_{PW}	1184.0			ns

Recommendation	BIP-4 On Number of Nibbles	Bip-4 Off Number of Nibbles	Nibble Rate k nibbles/s
G.742	208	209	2112
G.745	259	260	2112
G.751	380	381	8592
G.753	531	532	8592

E3

Parameter	Symbol	Min	Typ	Max	Unit
RNC clock period	t_{CYC}	116.4			ns
RNC high time	t_{PWH}	52.4			ns
RNC low time	t_{PWL}	52.4			ns
RNIB delay after RNC↑	$t_{D(1)}$			7.0	ns
$\overline{RNF}$ delay after RNC↑	$t_{D(2)}$			7.0	ns
$\overline{RNF}$ pulse width (G.753)	t_{PW}	349.0			ns
$\overline{RNF}$ pulse width (G.751)	t_{PW}	291.0			ns

Figure 11. Terminal Side Transmit Nibble Timing



This waveform diagram shows a G.745 frame with the BIP-4 feature on and off. The gapped clock period corresponds to the 8-bit (two nibbles) framing pattern.

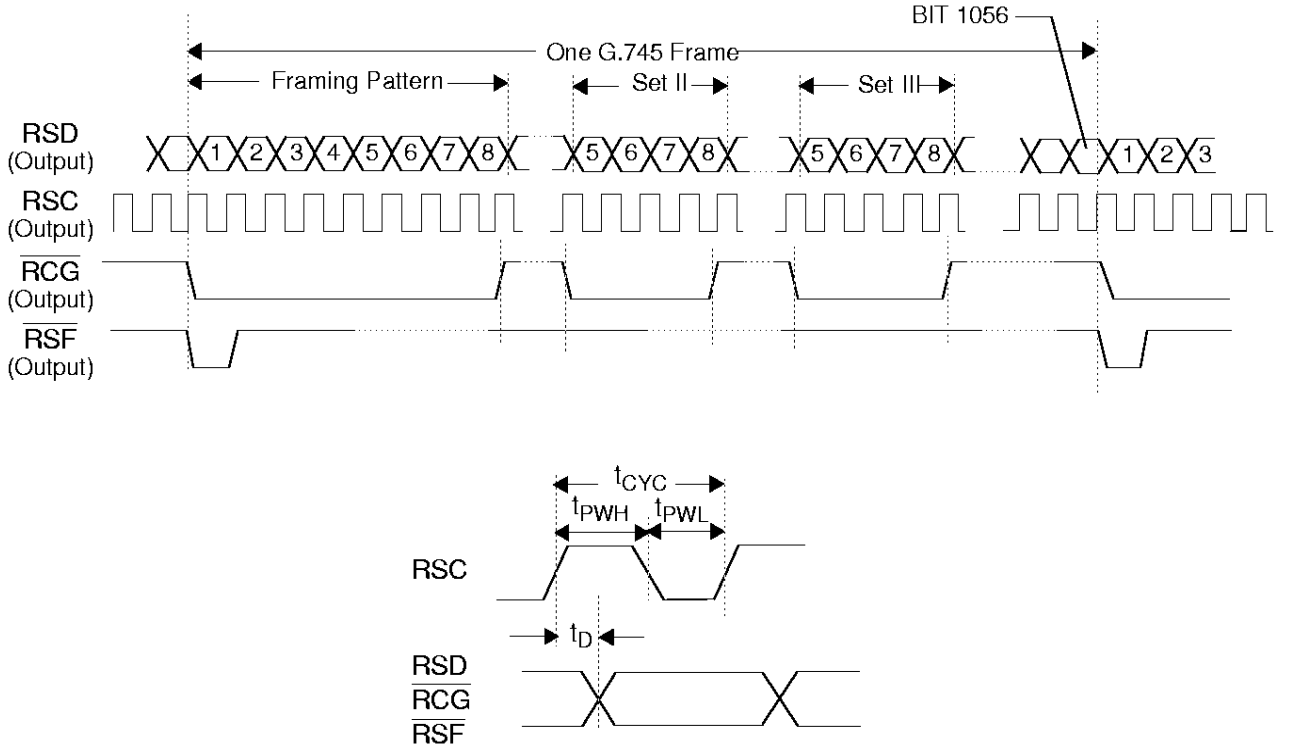
E2

Parameter	Symbol	Min	Typ	Max	Unit
XNC clock period	t_{CYC}	473.0			ns
XNC high time	t_{PWH}	213.0			ns
XNC low time	t_{PWL}	213.0			ns
XNIB set-up time to XNC↑	t_{SU}	4.0			ns
XNIB hold time after XNC↑	t_H	4.0			ns
$\overline{XNF}$ output delay after XNC↑	t_{OD}	4.0			ns
$\overline{XNF}$ pulse width (BIP-4 off, G.745)	t_{PW}	947.0			ns
$\overline{XNF}$ pulse width (BIP-4 off, G.742)	t_{PW}	1184.0			ns

E3

Parameter	Symbol	Min	Typ	Max	Unit
XNC clock period	t_{CYC}	116.4			ns
XNC high time	t_{PWH}	52.4			ns
XNC low time	t_{PWL}	52.4			ns
XNIB set-up time to XNC↑	t_{SU}	4.0			ns
XNIB hold time after XNC↑	t_H	4.0			ns
$\overline{XNF}$ output delay after XNC↑	t_{OD}	4.0			ns
$\overline{XNF}$ pulse width (BIP-4 off, G.753)	t_{PW}	349.0			ns
$\overline{XNF}$ pulse width (BIP-4 off, G.751)	t_{PW}	291.0			ns

Figure 12. Terminal Side Receive Serial Timing



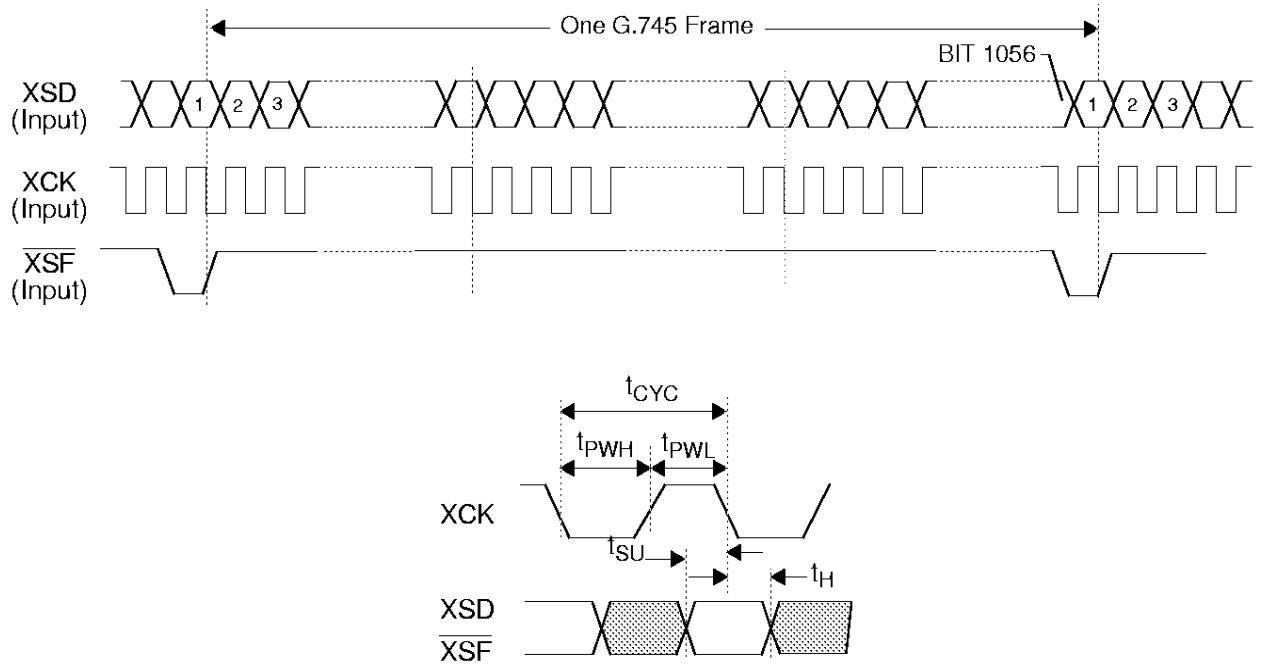
E3

Parameter	Symbol	Min	Typ	Max	Unit
RSC clock period	t_{CYC}	29.0	29.1		ns
RSC high time	t_{PWH}	11.5			ns
RSC low time	t_{PWL}	11.5			ns
RSD, $\overline{RCG}$, $\overline{RSF}$ delay after RSC↑	t_D			7.0	ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
RSC clock period	t_{CYC}	116.0	118.4		ns
RSC high time	t_{PWH}	46.0			ns
RSC low time	t_{PWL}	46.0			ns
RSD, $\overline{RCG}$, $\overline{RSF}$ delay after RSC↑	t_D			7.0	ns

Figure 13. Terminal Side Transmit Serial Timing



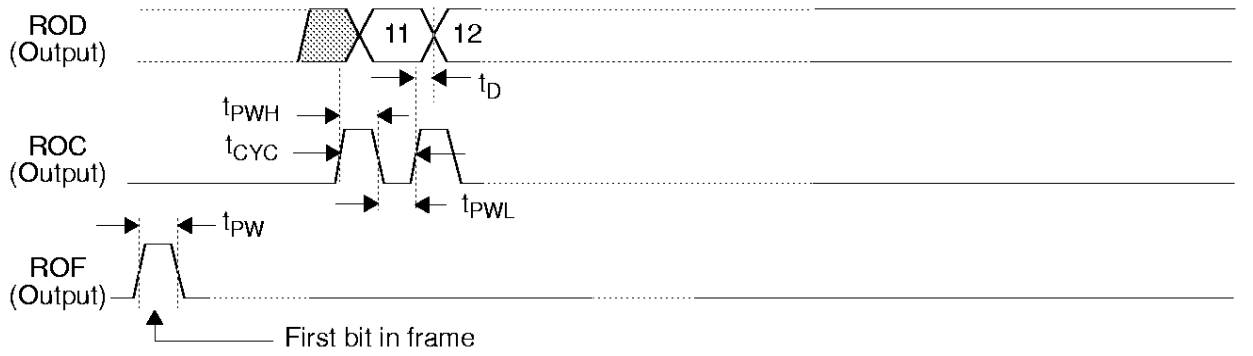
E3

Parameter	Symbol	Min	Typ	Max	Unit
XCK clock period	t_{CYC}	29.1			ns
XCK high time	t_{PWH}	13.1			ns
XCK low time	t_{PWL}	13.1			ns
XSD, $\overline{XSF}$ set-up time to XCK↓	t_{SU}	4.0			ns
XSD, $\overline{XSF}$ hold time after XCK↓	t_H	4.0			ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
XCK clock period	t_{CYC}	118.4			ns
XCK high time	t_{PWH}	53.3			ns
XCK low time	t_{PWL}	53.3			ns
XSD, $\overline{XSF}$ set-up time to XCK↓	t_{SU}	4.0			ns
XSD, $\overline{XSF}$ hold time after XCK↓	t_H	4.0			ns

Figure 14. G.742/G.751 Service Bit Receive Timing



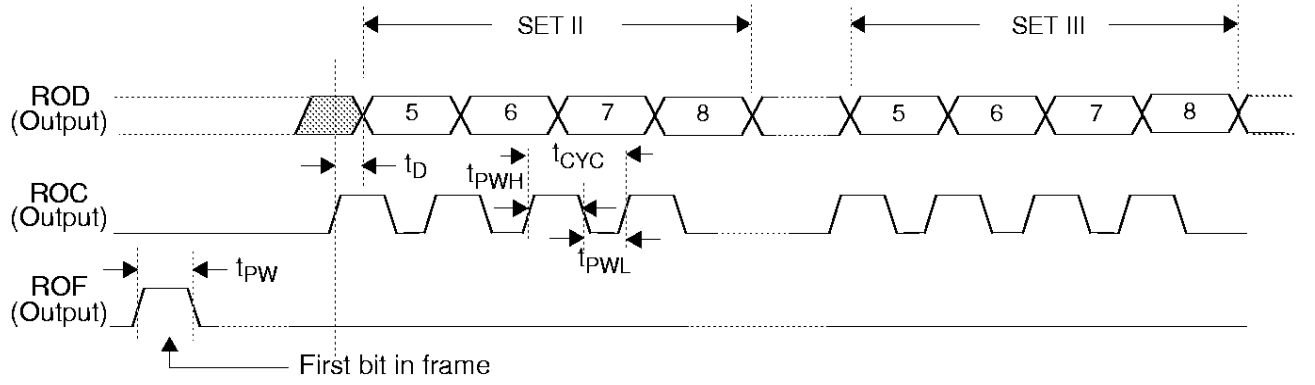
G.751 (E3)

Parameter	Symbol	Min	Typ	Max	Unit
ROC clock period	t_{CYC}	29.0	29.1		ns
ROC high time	t_{PWH}	11.0			ns
ROC low time	t_{PWL}	11.0			ns
ROF pulse width	t_{PW}	11.0			ns
ROD delay after ROC↑	t_D			7.0	ns

G.742 (E2)

Parameter	Symbol	Min	Typ	Max	Unit
ROC clock period	t_{CYC}	116.0	118.4		ns
ROC high time	t_{PWH}	46.0			ns
ROC low time	t_{PWL}	46.0			ns
ROF pulse width	t_{PW}	46.0			ns
ROD delay after ROC↑	t_D			7.0	ns

Figure 15. G.745/G.753 Service Bit Receive Timing



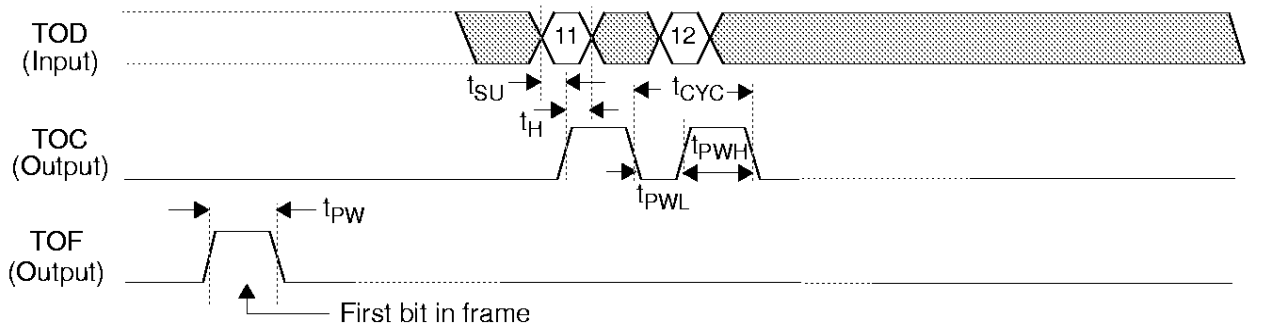
G.753 (E3)

Parameter	Symbol	Min	Typ	Max	Unit
ROC clock period	t_{CYC}	29.0	29.1		ns
ROC high time	t_{PWH}	11.0			ns
ROC low time	t_{PWL}	11.0			ns
ROF pulse width	t_{PW}	11.0			ns
ROD delay after ROC↑	t_D			7.0	ns

G.745 (E2)

Parameter	Symbol	Min	Typ	Max	Unit
ROC clock period	t_{CYC}	116.0	118.4		ns
ROC high time	t_{PWH}	46.0			ns
ROC low time	t_{PWL}	46.0			ns
ROF pulse width	t_{PW}	46.0			ns
ROD delay after ROC↑	t_D			7.0	ns

Figure 16. G.742/G.751 Service Bit Transmit Timing



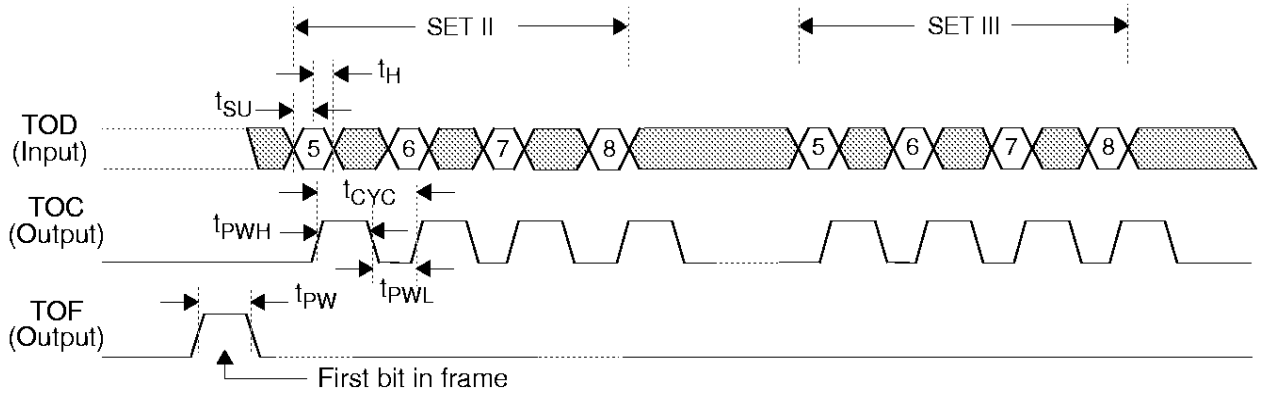
G.751 (E3)

Parameter	Symbol	Min	Typ	Max	Unit
TOC clock period	t_{CYC}	29.1			ns
TOC high time	t_{PWH}	13.1			ns
TOC low time	t_{PWL}	13.1			ns
TOF pulse width	t_{PW}	11.0			ns
TOD set-up time to TOC↑	t_{SU}	4.0			ns
TOD hold time after TOC↑	t_H	4.0			ns

G.742 (E2)

Parameter	Symbol	Min	Typ	Max	Unit
TOC clock period	t_{CYC}	118.4			ns
TOC high time	t_{PWH}	53.3			ns
TOC low time	t_{PWL}	53.3			ns
TOF pulse width	t_{PW}	46.0			ns
TOD set-up time to TOC↑	t_{SU}	4.0			ns
TOD hold time after TOC↑	t_H	4.0			ns

Figure 17. G.745/G.753 Service Bit Transmit Timing



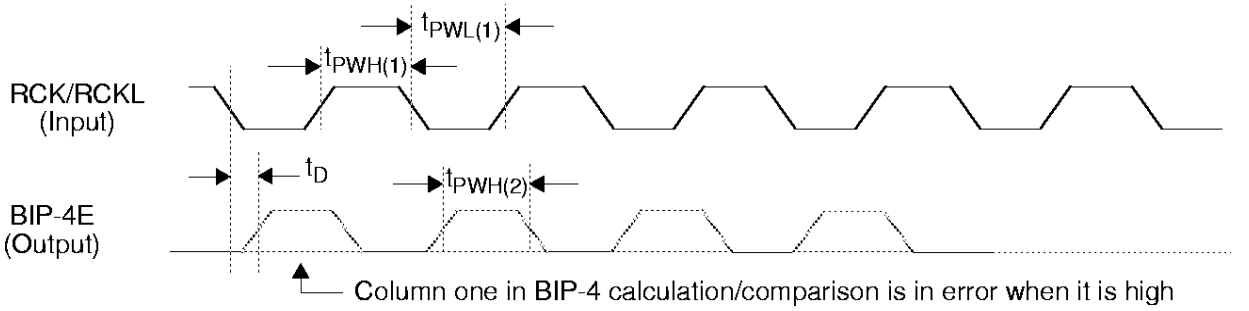
G.753 (E3)

Parameter	Symbol	Min	Typ	Max	Unit
TOC clock period	t_{CYC}	29.1			ns
TOC high time	t_{PWH}	13.1			ns
TOC low time	t_{PWL}	13.1			ns
TOF pulse width	t_{PW}	11.0			ns
TOD set-up time after TOC↑	t_{SU}	4.0			ns
TOD hold time to TOC↑	t_H	4.0			ns

G.745 (E2)

Parameter	Symbol	Min	Typ	Max	Unit
TOC clock period	t_{CYC}	118.4			ns
TOC high time	t_{PWH}	53.3			ns
TOC low time	t_{PWL}	53.3			ns
TOF pulse width	t_{PW}	46.0			ns
TOD set-up time after TOC↑	t_{SU}	4.0			ns
TOD hold time to TOC↑	t_H	4.0			ns

Figure 18. BIP-4 Error Timing



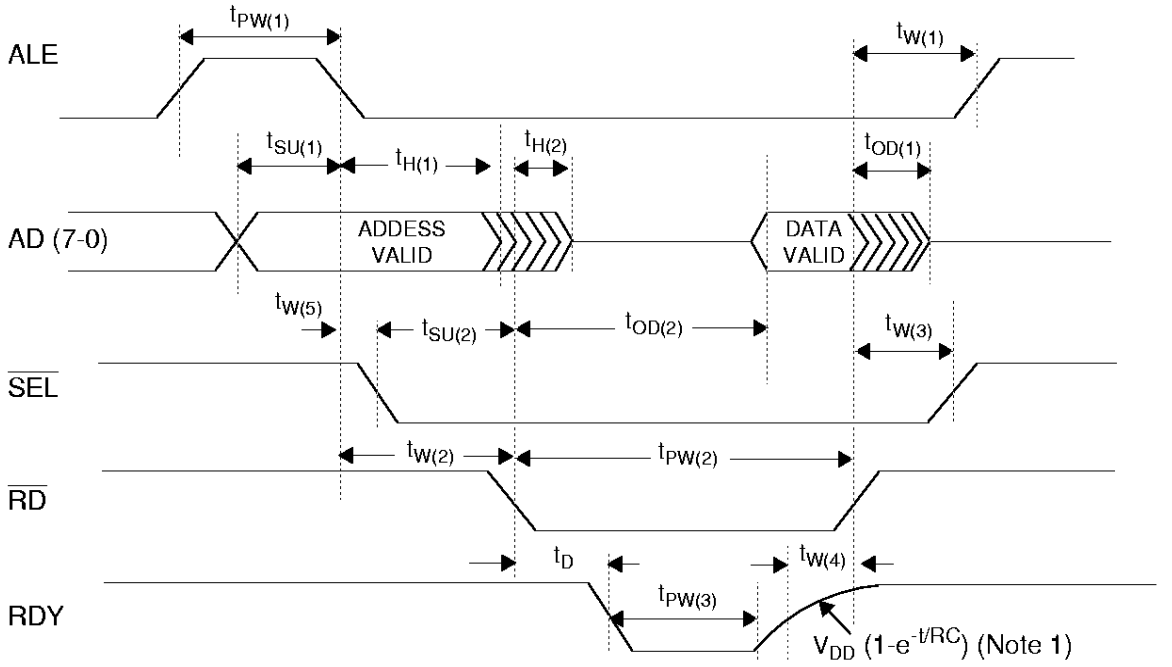
E3

Parameter	Symbol	Min	Typ	Max	Unit
RCK/RCKL high time	$t_{PWH(1)}$	12.1	14.6		ns
RCK/RCKL low time	$t_{PWL(1)}$	12.1	14.6		ns
BIP-4E delay after RCK/RCKL↓	t_D			7.0	ns
BIP-4E high time	$t_{PWH(2)}$	11.0			ns

E2

Parameter	Symbol	Min	Typ	Max	Unit
RCK/RCKL high time	$t_{PWH(1)}$	46.0	59.2		ns
RCK/RCKL low time	$t_{PWL(1)}$	46.0	59.2		ns
BIP-4E delay after RCK/RCKL↓	t_D			7.0	ns
BIP-4E high time	$t_{PWH(2)}$	46.0			ns

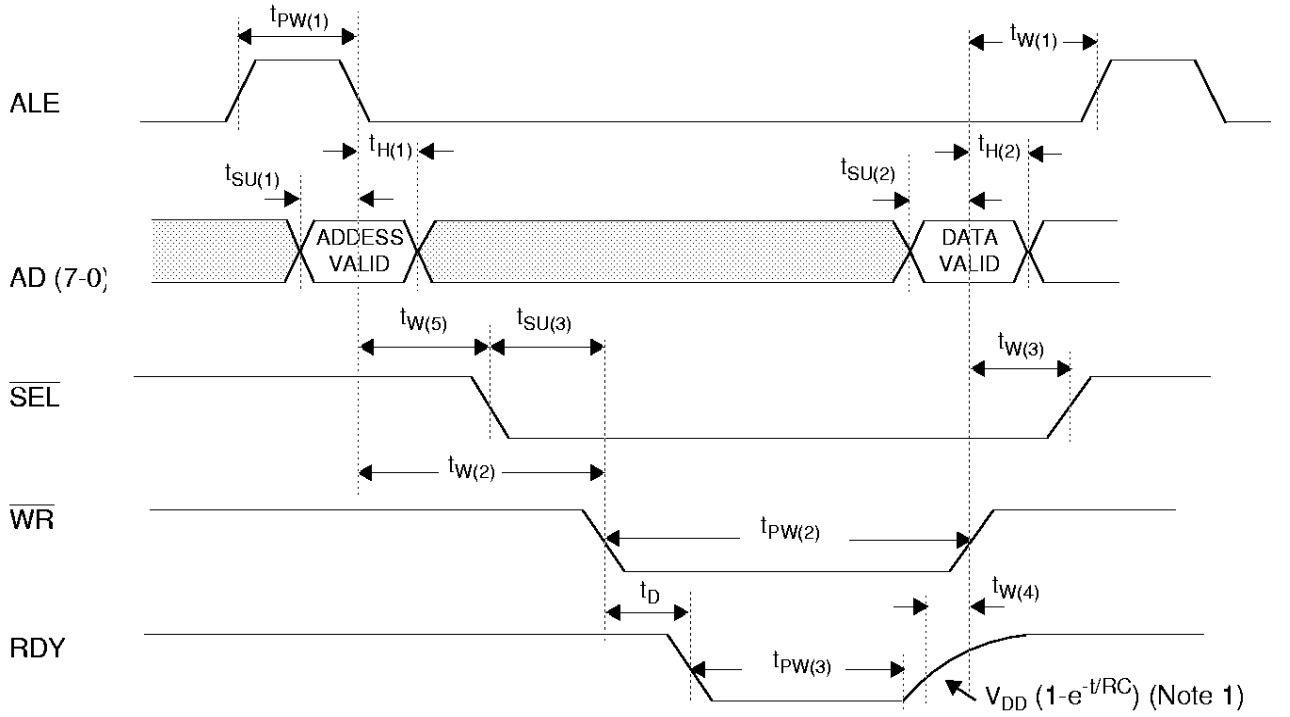
Figure 19. Microprocessor Read Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20.0			ns
ALE wait time after $\overline{RD}$↑	$t_{W(1)}$	25.0			ns
Address set-up time to ALE↓	$t_{SU(1)}$	10.0			ns
Address hold time after ALE↓	$t_{H(1)}$	10.0			ns
Address hold time after $\overline{RD}$↓	$t_{H(2)}$	0.0			ns
Data output delay (to tristate) after $\overline{RD}$↑	$t_{OD(1)}$	10.0		90.0	ns
Data output delay after $\overline{RD}$↓ (Notes 2, 4)	$t_{OD(2)}$			$2 * t_{CYC} + 20.0$	ns
$\overline{SEL}$ set-up time to $\overline{RD}$↓	$t_{SU(2)}$	20.0			ns
$\overline{RD}$ pulse width (Notes 2, 3)	$t_{PW(2)}$	$2 * t_{CYC} + 3.0$			ns
$\overline{RD}$ wait time after ALE↓	$t_{W(2)}$	20.0			ns
$\overline{SEL}$ wait time after $\overline{RD}$↑	$t_{W(3)}$	5.0			ns
RDY delay after $\overline{RD}$↓ (Note 2)	t_D	3.0		t_{CYC} +12	ns
RDY pulse width (Notes 2, 4)	$t_{PW(3)}$	$2 * t_{CYC}$		$3 * t_{CYC}$	ns
$\overline{RD}$ wait time after RDY↑	$t_{W(4)}$	0.0			ns
$\overline{SEL}$ wait time after ALE↓	$t_{W(5)}$	10.0			ns

Note 1: Open drain rise time is dependent upon external load resistance (R) and capacitance (C).
Note 2: t_{CYC} is the period of the line interface clock used (E2 or E3).
Note 3: At least 10 clock cycles of XCK must occur after reset before a read cycle is valid.
Note 4: Output data is valid when RDY is released from low level at end of $t_{PW(3)}$.

Figure 20. Microprocessor Write Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20.0			ns
ALE wait time after $\overline{WR}$↑	$t_{W(1)}$	25.0			ns
Address set-up time to ALE↓	$t_{SU(1)}$	10.0			ns
Address hold time after ALE↓	$t_{H(1)}$	10.0			ns
Data set-up time to $\overline{WR}$↑	$t_{SU(2)}$	10.0			ns
Data hold time after $\overline{WR}$↑	$t_{H(2)}$	10.0			ns
$\overline{WR}$ pulse width (Notes 2, 3)	$t_{PW(2)}$	2 * t_{CYC} + 3.0			ns
$\overline{WR}$ wait time after ALE↓	$t_{W(2)}$	20.0			ns
$\overline{SEL}$ set-up time to $\overline{WR}$↓	$t_{SU(3)}$	20.00			ns
$\overline{SEL}$ wait time after $\overline{WR}$↑	$t_{W(3)}$	5.0			ns
RDY delay time after $\overline{WR}$↓ (Note 2)	t_D	3.0		t_{CYC} +12	ns
RDY pulse width (Note 2)	$t_{PW(3)}$	2 * t_{CYC}		3 * t_{CYC}	ns
$\overline{WR}$ wait time after RDY↑	$t_{W(4)}$	0.0			ns
$\overline{SEL}$ wait time after ALE↓	$t_{W(5)}$	10.0			ns

Note 1: Open drain rise time is dependent upon external load resistance (R) and capacitance (C).
Note 2: t_{CYC} is the period of the line interface clock used (E2 or E3).
Note 3: At least 10 clock cycles of XCK must occur after reset before a write cycle is valid.

OPERATION

POWER SUPPLY CONNECTIONS

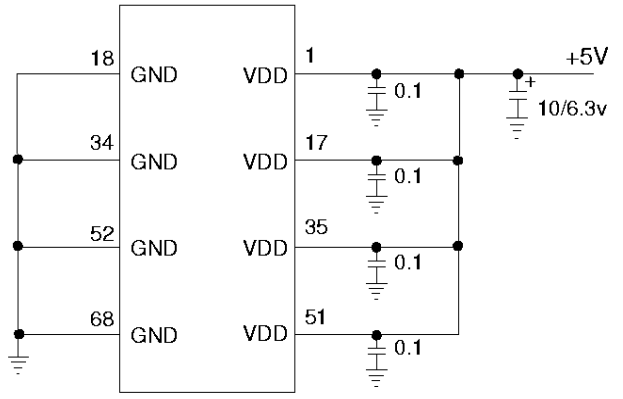


Figure 21. Power Supply Connections

The E2/E3F has four supply pins that provide internal power distribution. A VDD pin must be connected to a single +5 volt power supply, as shown in Figure 21. It is recommended that 0.1 microfarad ceramic disk capacitors be used for decoupling each of the supply pins, and that the decoupling capacitors be connected in close proximity to the E2/E3F. In addition, a 10 microfarad 6.3v tantalum capacitor should be connected between +5 volt and ground.

MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	R/W	M1	M0	SER	TAIS	BIP-4	TLBK	PLBK	OHI/O
1	R	CODING VIOLATION COUNTER							
2	R	RLOF	RLOC	RAIS	TLOC	--	--	--	--
3	R	BIP-4 ERROR COUNTER							
4	R/W	BIP-4 ERROR MASK				--	--	--	FRSRCH
5	R	ROH5/11	ROH6/12	ROH7	ROH8	ROH5	ROH6	ROH7	ROH8
6	R/W	TOH5/11	TOH6/12	TOH7	TOH8	TOH5	TOH6	TOH7	TOH8
7	R(L)	RLOF	RLOC	RAIS	TLOC	--	--	--	--

*R/W: Read/write; R: Read only; R(L): Read only - latched register. Unused bit positions in R/W addresses should be written to 0.

MEMORY MAP DESCRIPTIONS

CONTROL REGISTERS

Address*	Bit	Symbol	Description
0	7 6	M1 M0	**Mode Control:** The two controls select the operating rate of the E2/E3F according to the table given below: M1 M0 Recommendation Rate (kbit/s) 0 0 G.745 8448 0 1 G.742 8448 1 0 G.753 34368 1 1 G.751 34368
	5	SER	**Serial Interface:** A one written into this bit location selects the bit-serial interface for the terminal side I/O. A zero selects the nibble-parallel interface.
	4	TAIS	**Transmit Alarm Indication Signal:** A one written into this bit location causes an all ones signal (AIS) to be sent in place of a G.7XX frame format.
	3	BIP-4	**Bit Interleaved Parity-4 Alarm:** A one written into this location enables the BIP-4 function. In the transmit direction, the BIP-4 is calculated for data nibbles only, and is sent as the last four bits in the transmitted frame format. In the receive direction, the BIP-4 is calculated for the data bits only and compared against the last four bits of the frame (BIP-4). An output indication (BIP-4E) occurs when one or more columns do not match. At the terminal interface, the transmit and receive nibble clocks are gapped during the BIP-4 time.
	2	TLBK	**Terminal Loopback:** A one written into this location disables the receive line side input and causes the transmit line output to be looped back as the receive line input. To avoid contention between the loopback control lead, which is not disabled in the microprocessor mode, and the memory map control bit, the following truth table is used. $\overline{\text{TLBK}}$ Control Lead — TLBK Control Bit — Terminal Loopback low — Don't Care — On high — 1 — On high — 0 — Off
	1	PLBK	**Payload Loopback:** PLBK is valid only in the serial mode. A one written into this location disables the terminal side transmit data input, and causes the terminal receive data output to be looped back as the transmit terminal data input in the serial mode only. To avoid contention between the loopback control lead, which is not disabled in the microprocessor mode, and the memory map control bit, the following truth table is used. A payload loopback is also known as a line loopback. $\overline{\text{PLBK}}$ Control Lead — PLBK Control Bit — Payload Loopback low — Don't Care — On high — 1 — On high — 0 — Off
	0	OHI/O	**Service (Overhead) Bit I/O Selection:** A one written into this location enables the external service bit interface (TOD). A zero written into this location disables the external service bit interface (TOD), and enables service bits written into Address 6H as the transmitted service bits.

* All Addresses are hexadecimal.

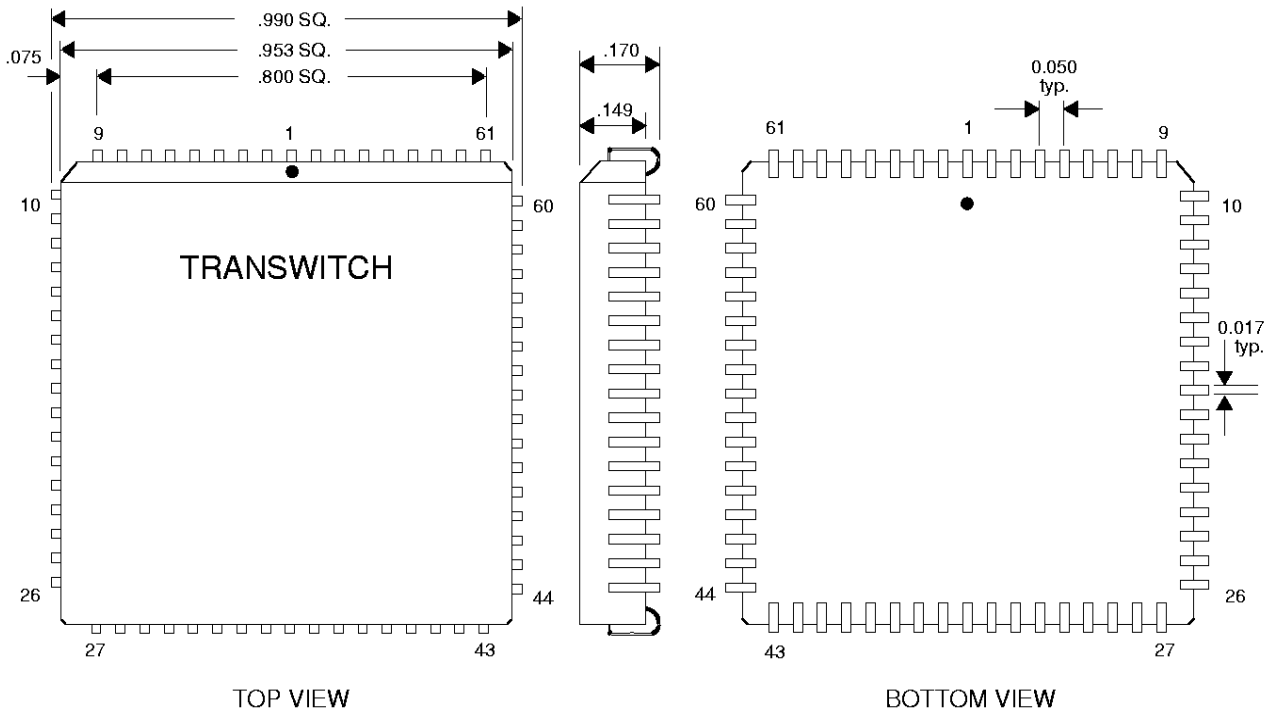
COUNTERS, STATUS BITS AND SERVICE BITS

Address	Bit	Symbol	Description
1	7-0		**Coding Violation Counter:** This saturating counter counts the number of illegal coding violations. Its count is valid only when operating in the P and N rail mode. Bit 7 is the most significant bit. The counter resets to zero upon completion of a microprocessor read cycle.
2	7	RLOF	**Receive Loss of Frame (Unlatched):** For G.742, RLOF occurs when four consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is: 1111010000. For G.745, RLOF occurs when five consecutive frames are lost. Recovery occurs when two consecutive frames are detected. The framing pattern is 11100110. For G.751, RLOF occurs when four consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is 1111010000. For G.753, RLOF occurs when three consecutive frames are lost. Recovery occurs when three consecutive frames are detected. The framing pattern is: 111110100000.
	6	RLOC	**Receive Loss of Clock (Unlatched):** An alarm occurs when no transitions are detected in the received clock (RCK/RCKL) for 10 clock cycles. Recovery occurs on the first clock transition.
	5	RAIS	**Receive Alarm Indication Signal (Unlatched):** An alarm occurs when an all ones condition is detected in the receive data, including in the presence of a 10^{-5} error rate.
	4	TLOC	**Transmit Loss of Clock (Unlatched):** An alarm occurs when no transitions are detected in the transmit clock (XCK) for 10 clock cycles. Recovery occurs on the first clock transition.
3	7-0		**BIP-4 Error Counter:** This saturating counter counts the number of BIP-4 errors that have occurred in the comparison between the received BIP-4 value and the calculated value. Bit 7 is the most significant bit. The counter resets to zero upon completion of a microprocessor read cycle.
4	7-4		**BIP-4 Error Mask:** A one written to one or more bits causes those BIP-4 values to be inverted from their calculated value, and transmitted continuously. Bit 7 represents the first BIP-4 value transmitted in the frame, while bit 4 represents the last BIP-4 value transmitted in the frame. To stop the transmission of errors, the microprocessor must write zeros to the appropriate mask positions again.
	0	FRSRCH	**Frame Search:** A one written to this control bit causes one clock slip in the framer detection circuit, which forces the framer out of frame intentionally and forces the framer to search for a new valid frame. A zero must be written to this location before a subsequent frame search is issued.
5	7-0	ROHn	**Receive Overhead (Service Bits):** ROH5/11 and ROH6/12 in bits 7 and 6 are the received bits which correspond to bits 11 and 12 in received G.742 and G.751 frame formats. ROH5/11 - ROH8 in bits 7-4 correspond to bits 5-8 in Set II in the G.745 and G.753 frame formats. ROH5-ROH8 in bits 3-0 correspond to bits 5-8 in Set III in the G.745 and G.753 frame formats.

Address	Bit	Symbol	Description
6	7-0	TOHn	**Transmit Overhead (Service) Bits:** TOH5/11 and TOH6/12 in bits 7 and 6 correspond to bits 11 and 12 in the G.742 and G.751 frame formats. TOH5/11-TOH8 in bits 7-4 correspond to bits 5-8 in Set II in the G.745 and G.753 frame formats. TOH5-TOH8 in bits 3-0 correspond to bits 5-8 in Set III in the G.745 and G.753 frame formats. The transmission of the service bits in this location is enabled by writing a zero to bit 0 (OHI/O) in Address 0H.
7	7-4		**Latched Alarm Bits:** The bits in this location correspond to the bits in location 02H, except that the bits are latched on with an alarm. A microprocessor read cycle clears the latched bit positions. If an alarm remains active during a read cycle, the bit re-latches.

PACKAGE INFORMATION

The E2/E3F is available in a 68-pin plastic leaded chip carrier suitable for surface or socket mounting, as shown in Figure 22.



Note: All dimensions are in inches and are nominal unless otherwise indicated.

Figure 22. E2/E3F TXC-03701B 68-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-03701-BIPL	68-pin plastic leaded chip carrier

RELATED PRODUCTS

TXC-02050, MRT Multi-Rate Line Interface device. The MRT directly interfaces with the E2/E3F and provides the functions for terminating ITU-TSS-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU-TSS line rates.

TXC-05101C, HDLC VLSI Device (HDLC Controller). Provides an interface to packet. Performs flag generation/detection, zero insertion/deletion, abort detection and byte framing.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells using AAL3/4/5.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets using AAL3/4/5.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

TXC-21037, E2/E3F-MRT Evaluation Board. A complete ready-to-use single board that demonstrates the functions and features of the E2/E3F and MRT Line Interface VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the E2/E3F VLSI device for control and monitoring.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331

Tel: 800-701-4333 (In U.S.A.)
Tel: 908-981-0060
Fax: 908-981-9667

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

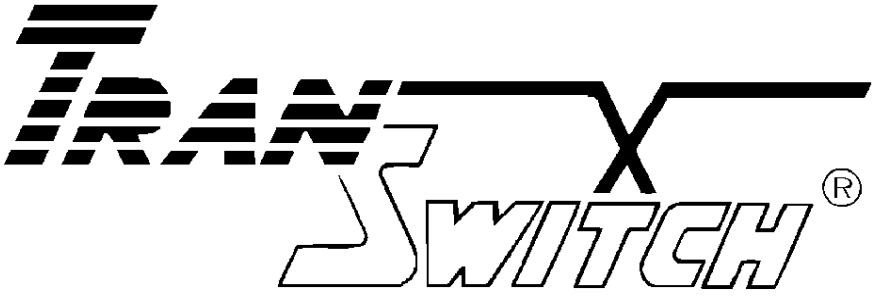
TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

- NOTES -

- NOTES -



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