EtherMap™-12 Device
Ethernet into STS-12/STM-4 SONET/SDH Mapper
TXC-04212

DATA SHEET
PRODUCT PREVIEW

FEATURES

- Eight 10/100 Mbit/s Ethernet ports, each using a SMII interface
- Single 1000 Mbit/s Ethernet port, using a parallel GMII interface (lead shared with SMII interfaces)
- Ethernet Management interface for control and configuration of externally connected PHYs
- GMII Mux-mode allowing multiple concatenation groups from one GMII
- Supports IEEE 802.3 flow control (Half and Full-duplex) and management statistics (RMON) on 10/100/1000 Mbit/s Ethernet ports (100 Mbps full-duplex only)
- Ethernet frame encapsulation/decapsulation protocols:
  - ITU-T G.7041, Generic Framing Procedure (GFP)
  - ITU-T X.86/X.85, Link Access Procedure SDH (LAPS)
  - ITU-T Q.922, Link Access Procedure Frame Mode (LAPF)
  - IETF RFC2878, Point-to-Point Protocol (PPP) with Bridging Control Protocol (BCP) support
  - Transparent HDLC processing
  - Performs mapping/demapping of encapsulated Ethernet frames into/from Low Order Virtual Concatenated
- Payloads and High Order virtual and contiguous concatenated payloads
- Dynamic bandwidth allocation using LCAS (ITU-T G.7042) for Low and High Order Virtual Concatenated payloads
- Glueless memory interface to external SDRAMs (up to 256 Mb)
- Low Order POH and Pointer processing for 336/252 VT/TUs
- High Order POH and Pointer processing for STS-1/VC-3/STS-3c/VC-4, STS-6c, STS-9c and STS-12c/VC4-4c
- Byte-wide 77.76MHz Add /Drop Line Telecom Bus interfaces
- Per-port Ethernet side and SONET/SDH system side loopback for system level diagnostics
- 16-bit wide microprocessor interface, selectable between Motorola or Intel
- API based driver provided (comparable with EtherMap-3)
- Boundary scan (IEEE 1149.1 standard)
- + 3.3V and +1.2V power supplies, 5V tolerant I/O leads
- 580-lead Plastic Ball Grid Array Package (PBGA)

DESCRIPTION

The EtherMap™-12 is a highly integrated, STS-12/STM-4 rate SONET/SDH device that provides mapping of 10/100/1000 Mbps Ethernet traffic into SONET/SDH Transport structures.

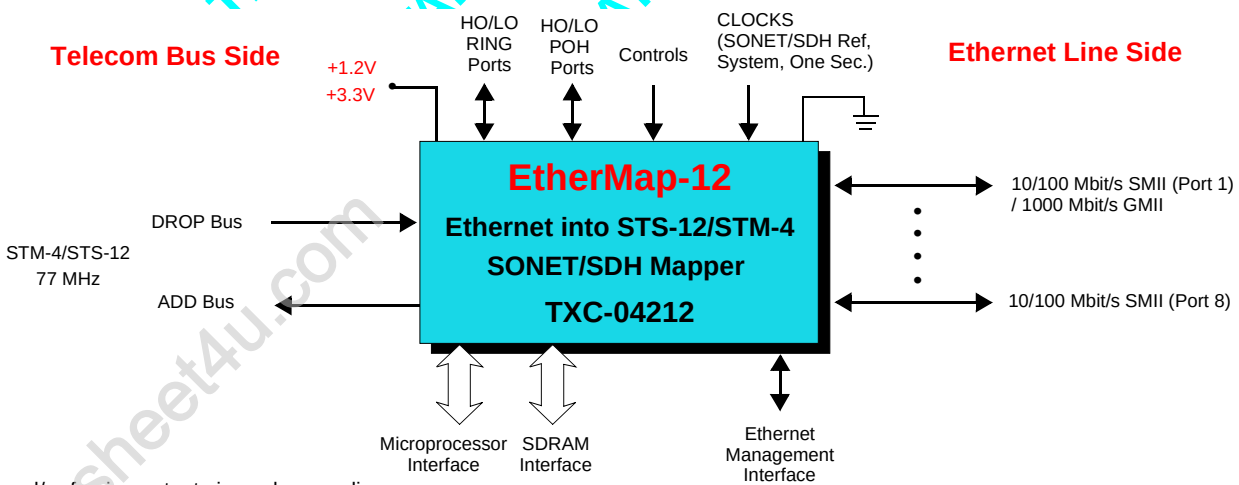
The EtherMap-12 has on the Ethernet side, either Eight 10/100 Mbps SMII MAC interfaces or One independent 1000 Mbps GMII MAC interface. Over-subscription is allowed for example in mapping One Gigabit Ethernet stream into either a single VC-4-4c/STS12c SPE, multiple VC-4/STS-3c SPEs, or multiple VC-3s/STS-1 SPEs is supported via configuration and built-in flow control mechanisms.

The STS-12/STM-4 front-end of the device is a standard byte wide 77.76 MHz Telecom Bus interface SONET processing includes Low and High Order pointer tracking and retiming, Low and High Order POH processing and performance monitoring along with complete High Order and Low Order Virtual Concatenation with LCAS. Both VT/TU and STS-1/VC-3 level non-blocking cross connects are available for flexible data path grooming and switching. The device operates from a 1.2V core and 3.3V/IO power supplies.

A fully functional Device Driver is available through TranSwitch Applications Engineering.

APPLICATIONS

- SONET/SDH add/drop and terminal multiplexers
- Multi-service access platforms
- IP DSLAMS
- CPE access platforms
- Wireless backhaul multiplexors



Document Number:
PRODUCT PREVIEW TXC-04212-MB, Ed. 2
November 2003

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

PRODUCT PREVIEW

TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

PRODUCT PREVIEW

TABLE OF CONTENTS (cont.)

Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

PRODUCT PREVIEW

LIST OF FIGURES (cont.)

LIST OF TABLES

FEATURES

The EtherMap-12 supports the following features. Please note that the convention used in the transmit (or ADD) direction is from the Ethernet line signal (SMII/GMII) to the SDH/SONET format (Telecom Bus), while the receive (or DROP) direction is from the SDH/SONET format to the Ethernet line.

GENERAL DEVICE LEVEL

- External SDRAM Memory Interface for:
  - Receive Frame buffering for Virtual Concatenation delay compensation and Ethernet flow control.
  - Transmit frame buffering with Ethernet flow control.
- Standard 16-bit wide microprocessor (lead selectable between Motorola or Intel Mode).
- One second Performance and Fault Monitoring registers/counters, with Alarm and Performance Statistics generation.
- On-chip Ethernet RMON statistics capability; as per RFC 2819.
- High and Low Order tributary POH interface.
- High and Low Order Alarm Indication Port.
- SMII/GMII Ethernet interface for connection to PHY's/MAC's.
- Ethernet Management Interface.
- Byte wide ADD/DROP Telecom Bus interface (77.76 MHz).
- Power-up to a default configuration (with disabled Telecom Bus Interface).

SONET/SDH MAPPINGS:

The Mapper and Demapper blocks provide the following rates and format mappings:

- STS-12c SPE
- STS-12 / STS-9c SPE
- STS-12 / STS-6c SPE
- STS-12 / STS-3c SPE
- STS-12 / STS-1 SPE
- STS-12 / STS-1 / VT1.5 SPE
- STM-4 / AUG-4 / AU-4-4c / VC-4-4c
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12s / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11s / VC-11
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11

All supported mappings can be mixed according to the [G.707] multiplexing structure up to a total payload rate equivalent to one STM-4/STS-12 signal.

The Mapper and Demapper blocks provide mapping/demapping of GFP/LAPS/LAPF/PPP/Transparent HDLC frames into/from the following SONET/SDH structures:

- For Low Order SDH applications[1], the frames are carried in, extracted from, VC-12s or VC-11s in the VC-4 structure using a TUG-3 mapping scheme, or in the VC-3 structure using a TUG-2 mapping scheme. Complete Low Order POH will be generated resp. terminated. The K4/Z7 byte is used for Low Order Virtual Concatenation.
- For Low Order SONET applications, the frames are carried in, extracted from, VT1.5s or VT2s in a STS-1 that is carried in a STS-12 structure. Complete Low Order POH will be generated resp. terminated. The K4/Z7 byte is used for Low Order Virtual Concatenation.
- For High Order SDH applications, the frames are carried in, extracted from, VC-3s[1] using TUG-3s with TU-3s, or in VC-4s or in a single VC-4-4c structure. Complete High Order POH will be generated resp. terminated.The H4 byte is used for High Order Virtual Concatenation.
- For High Order SONET applications, the frames are directly carried in, extracted from, STS-1 SPEs, or in STS-3c SPEs, or in a single STS-6c SPE, or in a single STS-9c SPE, or in a single STS-12c SPE. Complete High Order POH will be generated resp. terminated.The H4 byte is used for High Order Virtual Concatenation.

SONET/SDH Tx Mapper

High Order Path[1]

The Mapper complies to the latest ITU/ETSI/ANSI standards and features regarding the generation of the High Order Path Overhead bytes. These features include:

- J1 Byte: 16 or 64 Byte Trail Trace Identifier.
- B3 Byte: BIP-8 calculation and insertion.
- C2 Byte: signal label insertion.
- G1 Byte:
  - REI insertion (remote information from receive side).
  - RDI insertion (remote information from receive side): Single or Three bit.
  - Optionally RDI generation for a minimum of 20 Multiframes.
- H4 Byte:
  - Optionally Low Order V1/V2 multiframe generation.
  - Optionally Virtual Concatenation multiframe generation.
  - Optionally LCAS source state machine and control word generation.
- Unequipped Generation.
- Supervisory Unequipped Generation.
- AIS Generation.
- Tandem Connection Monitoring application is not supported.

1. Note: in ITU-T SDH a VC-3 can either be high order (AU-3/STS-1) or low order (TU-3). In the remainder of the Ether-Map-12 data sheet high order and low order refers to the type of path overhead bytes rather than the order of the path in the multiplexing hierarchy. Though both low and high order VC-3 mapping is supported, VC-3 operation will be covered in the high order path sections.

Low Order Path

The Mapper complies to the latest ITU/ETSI/ANSI standards and features regarding the generation of the Low Order TU/VT Path Overhead bytes. These features include:

- J2 Byte: 16 Byte Trail Trace Identifier.
- V5 and K4/Z7 Byte:
  - REI insertion (remote information from receive side).
  - RFI insertion: Microprocessor control.
  - BIP-2 calculation and insertion.
  - RDI insertion (remote information from receive side): Single or Three bit.
  - Optionally RDI generation for a minimum of 20 multiframes.
  - (Extended) signal label insertion.
  - 32-bit Virtual Concatenation multiframe generation.
  - Optionally LCAS source state machine and control word generation.
  - Unequipped Generation.
- Supervisory Unequipped Generation.
- AIS Generation.
- Tandem Connection Monitoring application is not supported.

SONET/SDH Rx Demapper

High Order Path

The Rx Demapper complies to the latest ITU/ETSI/ANSI standards and features regarding the processing of the High Order Path Overhead bytes. These features include:

- J1 Byte: 16 or 64 Byte Trail Trace Identifier.
- B3 Byte: BIP-8 Bit/Block error counter option.
- C2 Byte: Signal Label Mismatch, Unequipped, and VC AIS detection.
- G1 Byte:
  - RDI detection, Single or Three bit.
  - REI error counter.
- H4 Byte:
  - Optionally Low Order V1/V2 multiframe monitoring.
  - Optionally Virtual Concatenation multiframe monitoring.
  - Optionally LCAS sink state machine and control word retrieval.

Low Order Path

The Rx DeMapper complies to the latest ITU/ETSI/ANSI standards and features regarding the processing of the Low Order Path Overhead bytes. These features include:

- J2 Byte: 16 Byte Trail Trace Identifier.
- V5 and K4/Z7 Byte:
  - RDI detection, Single or Three bit.
  - REI error counter.
  - RFI detection.
  - BIP-2 Bit/Block error counter option.
  - Signal Label Mismatch, Unequipped, and VC AIS detection.
  - 32-bit Virtual Concatenation multiframe monitoring.
  - Optionally LCAS sink state machine and control word retrieval.
- Tandem Connection Monitoring application is not supported.

VIRTUAL CONCATENATION

A maximum differential delay of 64 ms is supported using an external SDRAM Memory Module. In addition, support for LCAS (Link Capacity Adjustment Scheme) is provided, based on the ANSI T1.105-2001 and G.7042/Y.1305 documents. The H4 and K4/Z7 processing includes the Virtual Concatenation Multiframe processing, along with the LCAS control words to achieve hitless capacity adjustment.

Note on the LCAS processing: There are configuration options that will make the H4 and K4/Z7 byte processing compatible with non-LCAS Virtual Concatenation systems.

TX AND RX EOS PROCESSORS

The transmit and receive EoS (Ethernet over SONET/SDH) processor blocks support the following encapsulation standards:

- Generic Framing Procedure (GFP).
  - Framed Mode GFP, that will assume the following type of clients: 10/100/1000 Mbps Ethernet.
- Link Access Procedure SDH (LAPS).
  - Ethernet over LAPS, ITU-T X.86 (02/2001): For extension of LANs (10/100/1000 Mbps Ethernet) over WAN within a private and/or public network.
- Link Access Procedure Frame Relay (LAPF)
- Point-to-Point Protocol (PPP) with Bridging Control Protocol (BCP) and Link Control Protocol (LCP) support.
- Transparent HDLC processing (t.HDLC)

Each Ethernet port allows the use of only one encapsulation standard at a time. However, the device can support simultaneous operation of all encapsulation standards across the Ethernet ports.

ETHERNET PORTS

The EtherMap-12 provides the following Ethernet Port features:

- Eight independent SMII (Serial Medial Independent Interfaces) for 10/100 Mbit/s Ethernet
  - Global 125 MHz reference clock
  - Global Synchronization signal
  - Lead selects PHY or Switch connection to external client

- Single GMII (Gigabit MII) for 1000 Mbit/s Ethernet
    - Lead shared with the SMII ports
- Selection of GMII or SMII is selected through a lead
- Ethernet Management Interface
- PHY or Switch Selection

10/100/1000 MBPS ETHERNET MAC BLOCKS

- Compliant to IEEE 802.3, 802.3u, 802.3x, 802.3z, and 802.3ac
- Full Duplex Operation in 10/100/1000 Mbit/s
- Half Duplex Operation in 10/100 Mbit/s
- MAC control sub layer provides support for control frames including PAUSE frames
- Provides support for statistics gathering based on RMON MIB Group 1, RMON MIB Group 2, RMON MIB Group 3, RMON MIB Group 9, RMON MIB 2, and the dot 3 Ethernet MIB
- GMII Mux Mode

SDRAM INTERFACES

- Glueless interface to external 256 Mbits SDRAM devices
- 32 Data, 13 Address, 1 Chip Select, 1 Clock, 1 Clock Enable, 1 Row Address Strobe, 1 Column Address Strobe, 1 Write Enable Strobe, 1 Data Bus Mask, and 2 Bank Address leads
- Buffers TX/RX data transfers
- Clock frequency of 125 MHz
- Programmable Refresh Period
- CAS latency of 3 supported
- Refresh operation is transparent to the user (i.e. auto-refresh)

MICROPROCESSOR INTERFACE

- 17-bit Address
- 16-bit Data bus
- Motorola or Intel style split bus supported
- Interrupt request lead
- Interrupt mask bits for controlling generation of hardware interrupt requests

JTAG INTERFACE

- IEEE 1149.1 compliant TAP is provided for board level testing.

DEVICE DRIVER

- Device configuration
- Fault monitoring
- Performance monitoring

PRODUCT PREVIEW

BLOCK DIAGRAM

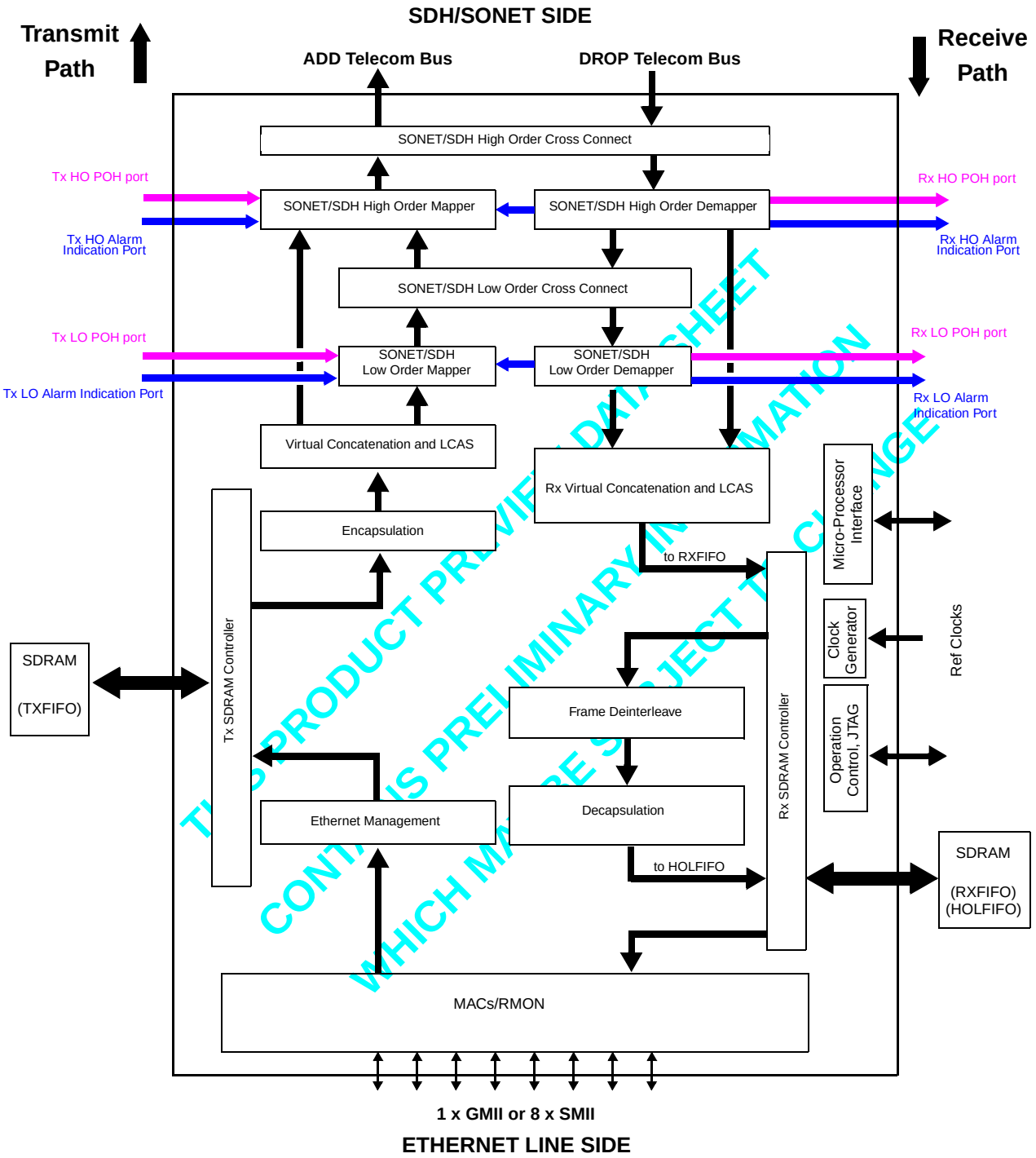


Figure 1. Functional Block Diagram of the EtherMap-12

BLOCK DIAGRAM DESCRIPTION

The EtherMap-12 provides functionality for mapping and demapping of Ethernet frames to and from SONET/SDH Virtual Concatenated tributary structures in both LCAS/non-LCAS mode. On the SONET/SDH side, the EtherMap-12 supports a STM-4/STS-12/STS-12c like structure using a single TranSwitch defined Telecom Bus operating at 77.76 MHz. On the Ethernet Line side, the EtherMap-12 supports either up to eight 10/100 Mbps Ethernet ports, or one 1000 Mbps (Gigabit) Ethernet port. The eight 10/100 Mpbs Ethernet ports each support the industry standard SMII interface. The single Gigabit Ethernet port supports the industry standard GMII interface.

In the transmit direction (Ethernet-to-SONET/SDH), the EtherMap-12 terminates the 10/100/1000 Mbps Ethernet traffic. The Ethernet frames from configured port(s) are extracted and buffered in the TXFIFO, which resides in external SDRAM memory. The TXFIFO is primarily used for implementing flow control when the Ethernet line side bandwidth is greater than the allocated bandwidth on the SONET/SDH side (i.e., an over-subscription situation). Based on system configuration, Ethernet frames from each of the Ethernet ports are encapsulated using one of the supported link layer protocols: LAPS, GFP, PPP, LAPF or Transparent HDLC. The encapsulated Ethernet frames are byte interleaved over preselected SONET/SDH containers and transported using Virtual Concatenation. The EtherMap-12 provides complete High and Low Order Path Overhead generation for the SONET/SDH containers. The bandwidth of SONET/SDH containers using Virtual Concatenation, are allowed to increase or decrease in a hitless fashion using the Link Capacity Adjustment Scheme (LCAS). The SONET/SDH containers carrying Ethernet frames are then be transmitted to an upstream SONET/SDH (Line/Section) Overhead Terminator device using a parallel Telecom Bus.

In the receive direction (SONET/SDH-to-Ethernet), the EtherMap-12 terminates a parallel Telecom Bus with SONET/SDH containers carrying Ethernet frames. The EtherMap-12 provides complete High and Low Order Path Overhead processing for the SONET/SDH tributaries. The SONET/SDH containers are extracted and buffered in the RXFIFO which resides in external SDRAM memory. The TXFIFO is used primarily for providing alignment and differential delay compensation for the selected SONET/SDH containers which form part of the Virtual Concatenation group. Once alignment and delay compensation has been achieved, the Ethernet frames are byte de-interleaved from the SONET/SDH containers to form their original frame structure on a per port basis. Next, Ethernet frames are extracted from the encapsulation frame (LAPS, GFP, PPP, LAPF or Transparent HDLC) and are buffered in the HOL (head-of-line) FIFO, which is in external SDRAM. The HOL FIFO buffers Ethernet frames when periods of congestion are seen at the Ethernet outputs. When congestion clears, frames are retrieved from the HOL FIFO and passed onto the Ethernet port for transmission to the external client(s).

The Multiple EtherMap software driver supports the EtherMap-12 device and has the same architecture as other TranSwitch device drivers, and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the EtherMap-12 device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction.

ETHERMAP-12 DEVICE INTERFACES

The EtherMap-12 provides the following main external interfaces.

10/100 MBPS ETHERNET SMII

This interface is used to allow the EtherMap-12 to connect to an external 10/100 Mbps Ethernet client (PHY/Switch). The EtherMap-12 device supports Eight independent SMII interfaces. The SMII interfaces are lead-shared with the GMII interface. The configuration choice is made during initialization/reset phase through a package signal lead. The SMII interface is comprised of two signals per port, a global synchronous pulse signal and a global 125 MHz reference clock. All signals are synchronous to the clock.

During initialization/reset phase, a package signal lead is used to allow selection between SMII and GMII interfaces. Furthermore, when using SMII interface, another package signal lead is used to select the type of SMII connection to external client: PHY or Switch. The state of the package leads will have a continuous effect on the selections.

1000 MBPS ETHERNET GMII

This interface is used to allow the mapper to connect to an external 1000 Mbps Ethernet client (PHY/Switch). The EtherMap-12 device supports a single GMII interface. The GMII interface is lead-shared with the SMII interfaces. The configuration choice is made on power-up/initialization through a package signal lead. The GMII interface is comprised of two independent Rx and Tx 8-bit data paths, two control signals per data path direction, two network status signals and a clock per data path direction. All signals are synchronous to their respective clocks.

ETHERNET MANAGEMENT INTERFACE

This interface is used to connect an external Ethernet PHY to the EtherMap-12 in order to configure and control its operation. The EtherMap-12 device supports a single Ethernet Management interface. This interface is used by all of the Eight 10/100 Mbps ports or the single 1000 Mbps port. The Ethernet Management interface is comprised of an output Management Data clock signal and a bidirectional Management Data signal that allows serial data to be clocked in and out of the external PHY device. All data transfers are synchronous to the clock signal. This interface provides support for up to 32 PHYs.

MICROPROCESSOR INTERFACE

This interface is used to allow the EtherMap-12 to communicate with to an external microprocessor. The interface provides support for a standard Motorola 68360/MPC860/MPC8260 or Intel split address/data bus interface that allows access to the EtherMap-12 memory map register locations. The mode of operation is configurable via external hardware signal leads.

SDRAM MEMORY INTERFACES

These interfaces are used to allow the mapper to connect to two external SDRAM Memory Modules. The external SDRAM Memory Modules are used for buffering of Ethernet traffic in both directions and also provides SONET/SDH frame storage for differential delay compensation. The SDRAM memory interface comprises of a 32-bit data bus, 13-bit address bus, bank address bus, 3-bit command bus, Input/Output Mask bus, system clock (up to 125 MHz) and control enable signals. This interface provides a "glueless" interface to the 256 Mbits SDRAM memory modules.

PARALLEL LINE SIDE TELECOM BUS INTERFACE

This interface is used to allow the EtherMap-12 to connect to an upstream SONET/SDH Line Overhead Terminator using a parallel Telecom Bus interface. This interface is collectively comprised of a single DROP and a single ADD bus.

The DROP bus is composed of a 8-bit wide input data bus, a byte clock input (77.76 MHz), a payload timing input signal, a payload active input signal and a parity indication input signal.

The ADD bus is composed of a 8-bit wide output data bus, a byte clock input/output (77.76 MHz), a payload timing input/output signal, a payload active input/output signal, a parity indication output signal and an add bus active indicator output signal.

The EtherMap-12 provides support for ADD bus timing modes.

HIGH & LOW ORDER POH PORT INTERFACE

The POH byte interface provides an alternative access to all of the SONET/SDH Low Order and High Order tributary POH bytes for external processing. There are two separate POH byte interfaces, one for Low Order (VT1.5/VC-12) POH, and one for High Order (STS-1/VC-3, STS-3c/VC-4, STS-6c, STS-9c, and STS-12c/VC-4-4c) POH.

Individual POH byes except J1/J2, C2/V5/K4 Signal label and BIP-2/BIP-8 fields are inserted into the POH from the transmit POH byte interface.

All POH bytes are provided at the receive POH byte interface for external processing.

HIGH & LOW ORDER ALARM INDICATION PORT INTERFACE

The Alarm Indication Port is provided to transport the remote information signal from a mate POH monitor to the POH generator. The remote information includes REI, RDI and various extended RDI indications. There are two separate Alarm Indication Ports, one for Low Order (VT1.5/VC-12) remote information, and one for High Order (STS-1/VC-3, STS-3c/VC-4, STS-6c, STS-9c, and STS-12c/VC-4-4c) remote information.

JTAG INTERFACE

This interface provides a five signal Boundary Scan capability that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test. In addition to the TAP, a lead is provided to place the output buffers in a high impedance state for systems that do not support the IEEE 1149.1 standard.

PRODUCT PREVIEW

ETHERNET OVER SONET SDH MAPPING

The EtherMap-12 device supports mapping of Ethernet frames over SONET/SDH containers using the mappings shown in Figure 2.

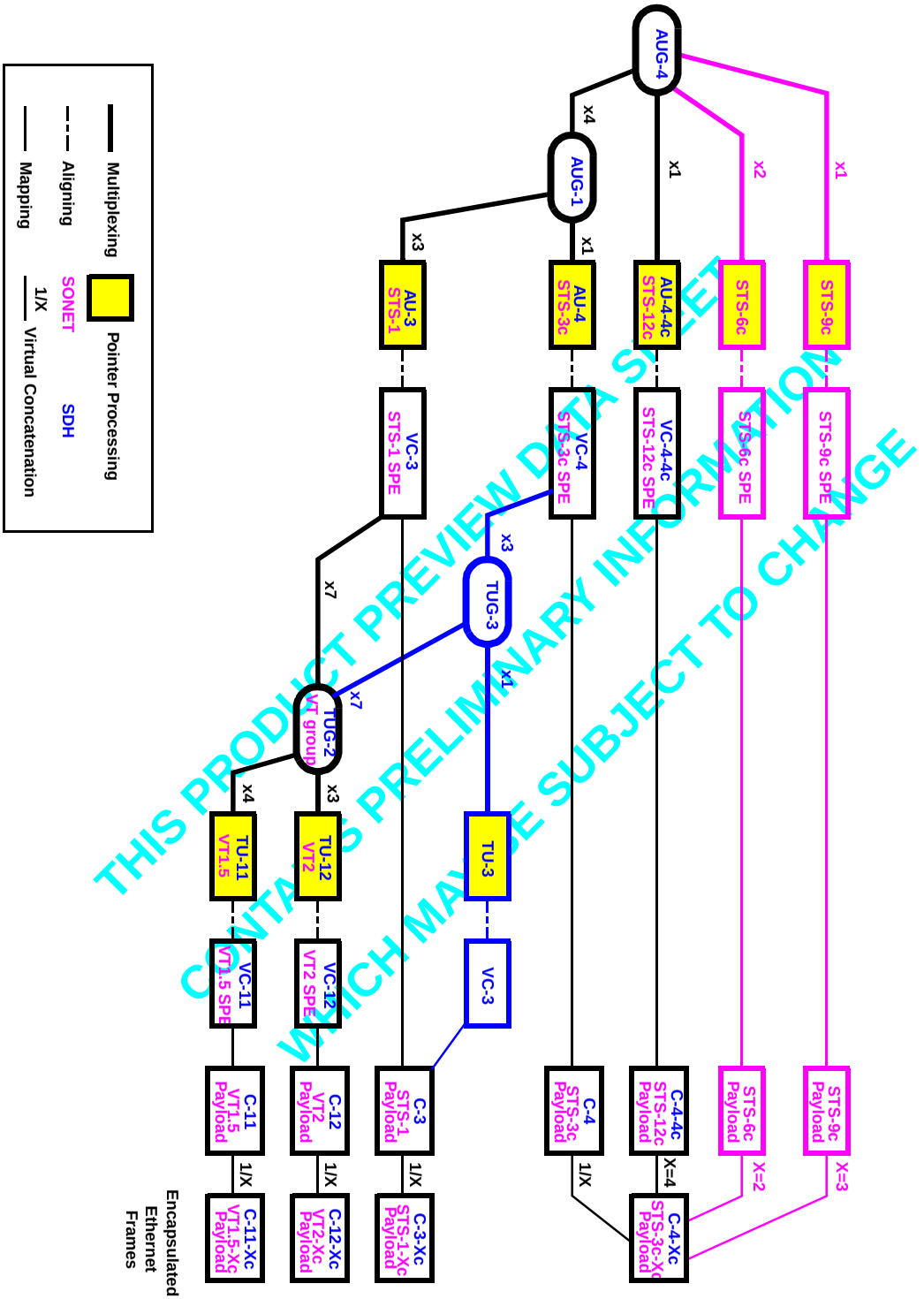


Figure 2. Mapping of Ethernet Frames Over SONET/SDH

DATA PROCESSING/FLOW

The EtherMap-12 provides functionality for mapping and demapping of Ethernet frames to and from SONET/SDH Virtual Concatenated tributary structures. Figures 3 and 4 represent the virtual tributary structures that are supported by the EtherMap-12 device.

Figure 3 shows the VC-11-Xv/VC-12Xv/VT1.5-Xv/VT2-Xv structure. The VCG provides a payload area of X times the payload capacity of the corresponding Low Order path container. The payload is mapped in the payload area of X individual Low Order path containers which form the members of the VCG. Each Low Order path container has its own POH.

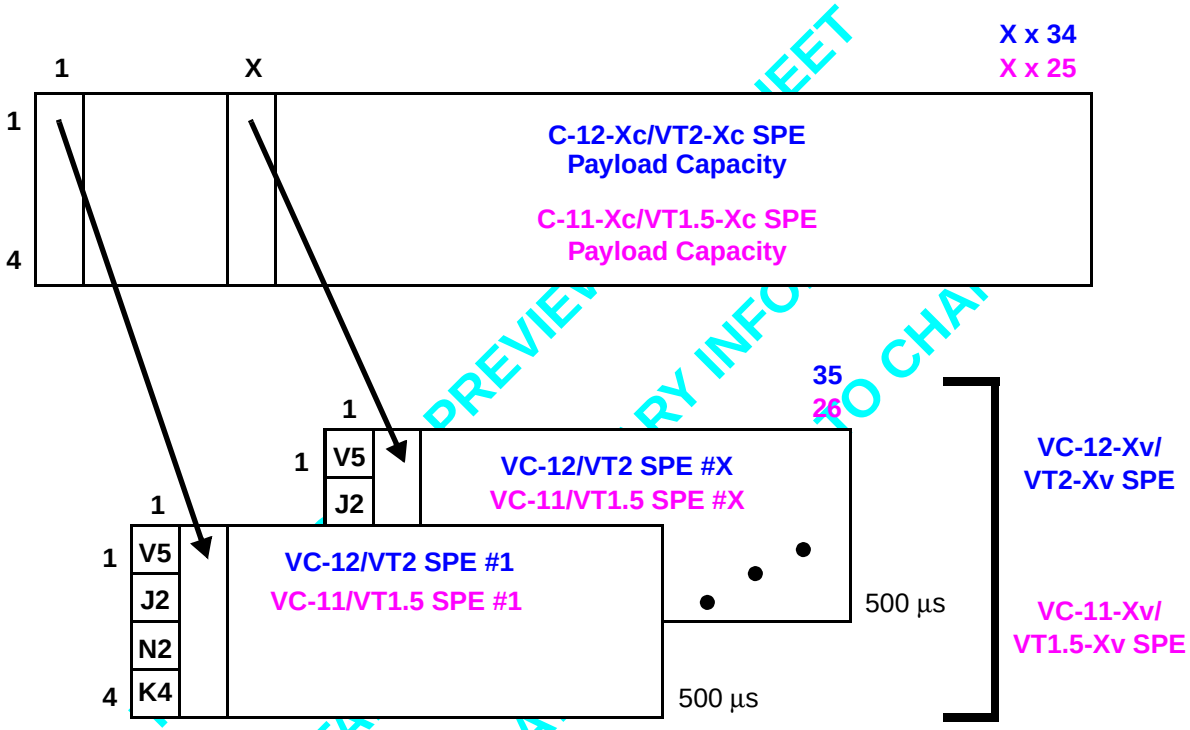


Figure 3. Low Order Virtual Concatenation Structure for SONET

Figure 4 shows the VC-3-Xv/VC-4-Xv/STS-1-Xv/STS-3c-Xv structure. The VCG provides a payload area of X times the payload capacity of the corresponding High Order path container. The payload is mapped in the payload area of X individual High Order path containers which form the members of the VCG. Each High Order path container has its own POH.

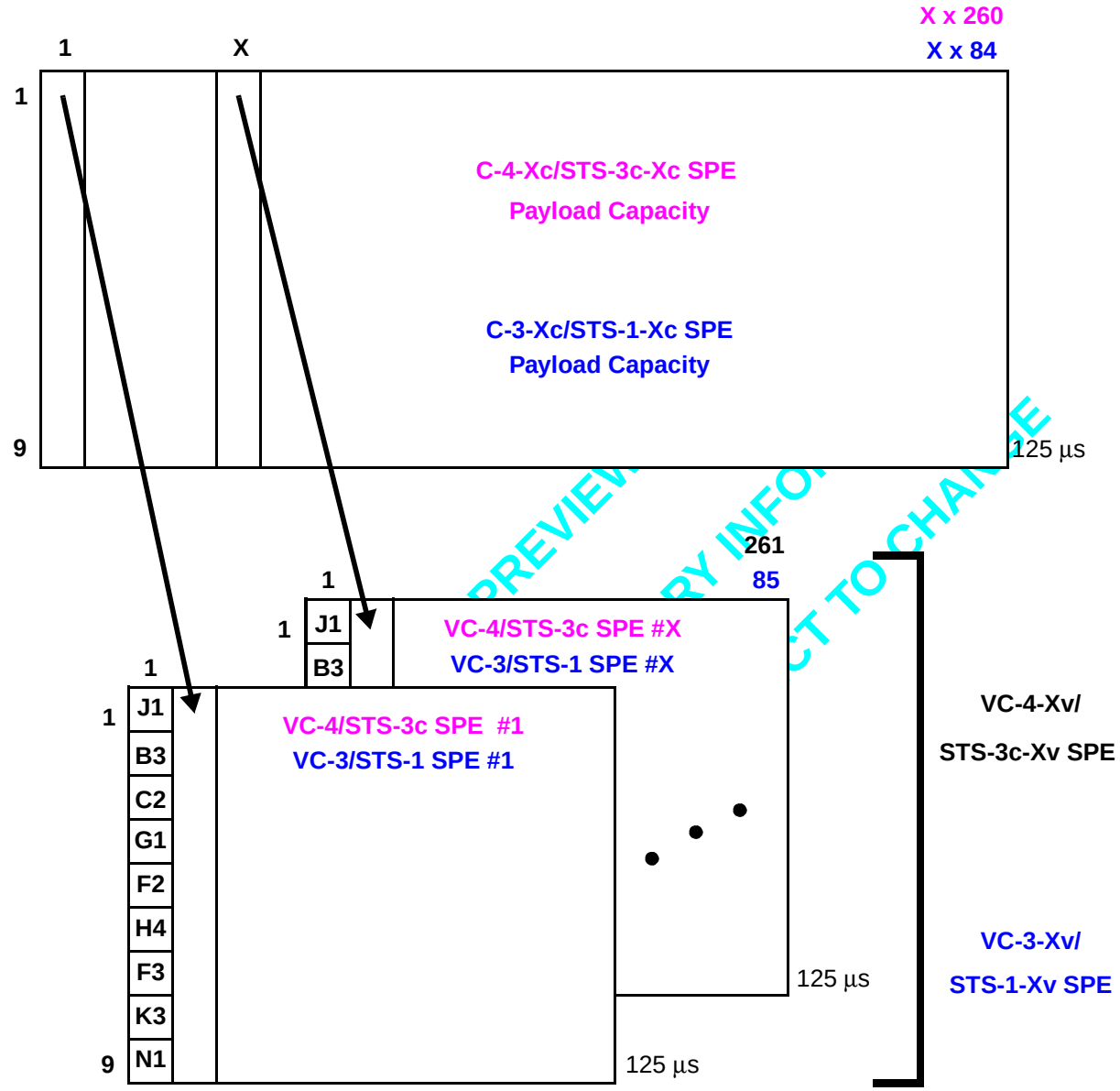


Figure 4. High Order Virtual Concatenation Structure for SONET/SDH

Figure 5 shows the VC-4-Xc/STS-Nc (N = 3X) contiguous concatenated structure. The contiguous concatenated container provides a single POH column, (X-1) stuff columns, and a payload area of X times the payload capacity of the VC-4/STS-3c High Order path container.

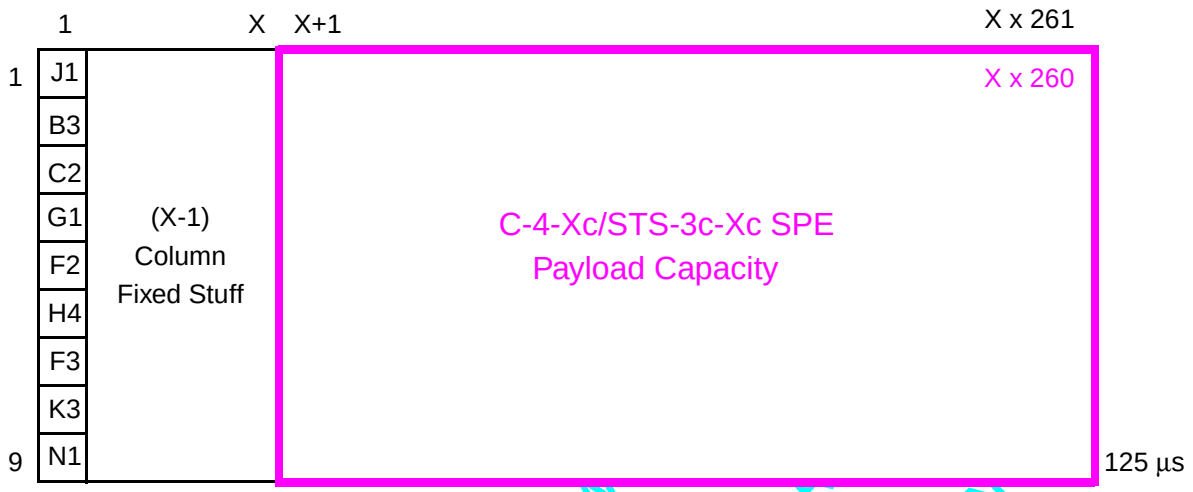
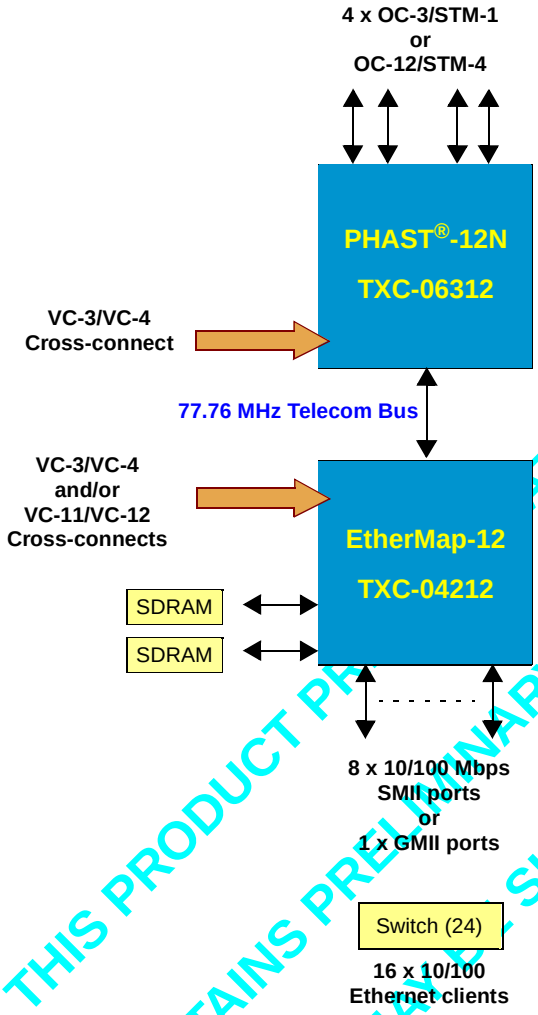


Figure 5. VC-4-Xc/STS-Nc (N = 3X) Contiguous Concatenation Structure for SONET/SDH

APPLICATION EXAMPLES



LEAD DIAGRAM

BOTTOM VIEW

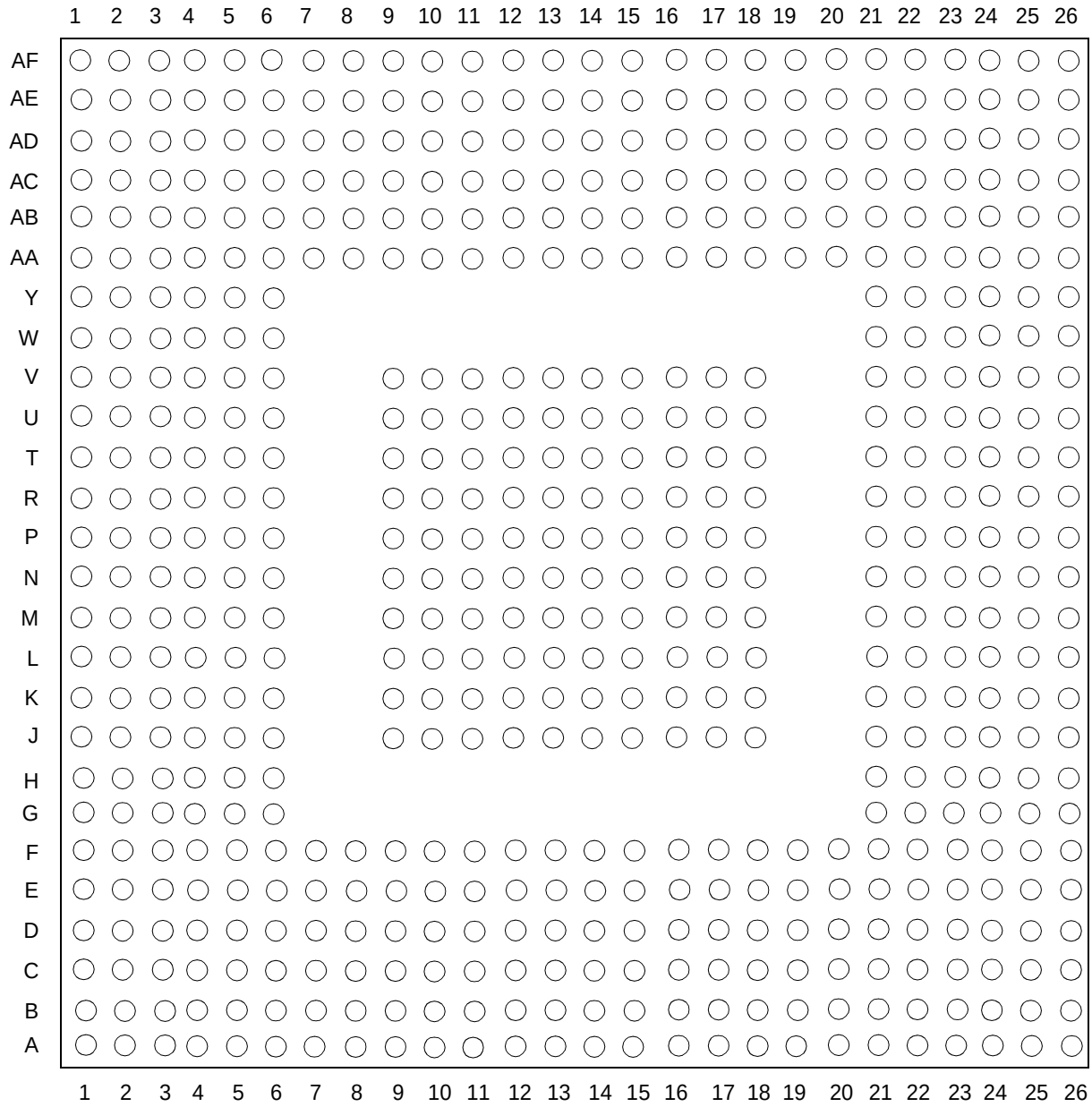


Figure 6. EtherMap-12 TXC-04212 Lead Diagram

PRODUCT PREVIEW

PRODUCT PREVIEW

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND, AND NO CONNECT LEADS

Symbol	Lead No.	I/O/P*	Name/Function
VDD33	D4, D23, E5, E13, E14, E22, F6, F9, F10, F13, F14, F17, F18, F21, J6, J21, K6, K21, N5, N6, N21, N22, P5, P6, P21, P22, U6, U21, V6, V21, AA6, AA9, AA10, AA13, AA14, AA17, AA18, AA21, AB5, AB13, AB14, AB22, AC4, AC23	P	**VDD33:** +3.3 volt power supply, ±5%.
VDD12	F7, F8, F11, F12, F15, F16, F19, F20, G6, G21, H6, H21, L6, L21, M6, M21, R6, R21, T6, T21, W6, W21, Y6, Y21, AA7, AA8, AA11, AA12, AA15, AA16, AA19, AA20	P	**VDD12:** +1.2 volt power supply, ±5%.
VSS	A1, A2, A3, A24, A25, A26, B1, B2, B3, B24, B25, B26, C1, C2, C3, C24, C25, C26, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, AD1, AD2, AD3, AD24, AD25, AD26, AE1, AE2, AE3, AE24, AE25, AE26, AF1, AF2, AF3, AF24, AF25, AF26	P	**Ground:** 0 (zero) Volts reference.
VDDP12	AC24	P	**VDDP12:** +1.2 volt digital power supply for the PLL, ±5%.
VDDP33	AB24	P	**VDDP33:** +3.3 volt digital power supply for the PLL, ±5%.
VDDPA12	Y22	P	**VDDPA12:** +1.2 volt analog power supply for the PLL, ±5%.
VSSP12	AB23	P	**VSSP12:** digital ground for the PLL.
VSSP33	AC25	P	**VDDP33:** +3.3 volt digital power supply for the PLL, ±5%
VSSPA12	AA23	P	**VSSPA12:** analog ground for the PLL.
NC	A11, A14, A19, A22, B7, B15, B17, C9, D6, D22, E6, E7, E10, E12, E16, E19, E21, E23, F5, F26, G4, G5, H23, J3, J5, J26, K3, K5, K24, M1, N24, N25, R5, T22, U24, W1, W4, W5, W22, Y3, AA2, AA5, AA22, AB6, AB26, AC5, AC17, AC22, AD7, AD10, AE7, AE13, AE18, AF4, AF6, AF9, AF13		**No Connect:** These leads are not to be connected, not even to another no connect lead, and must be left floating. Connection of an NC lead may impair performance or cause damage to the device. NC leads that are currently unused may be assigned functions in a future version of the device, affecting its usability in applications which have not left them floating.

* Note: I = Input; O = Output; OD=Open Drain Output; P = Power; T = Tristate:

LINE SIDE DROP TELECOM BUS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TBDD7 TBDD6 TBDD5 TBDD4 TBDD3 TBDD2 TBDD1 TBDD0	C15 D15 E15 A16 B16 C16 D16 A17	I	LVTTL-5	**Drop Bus Data In:** Byte wide data corresponding to the STM-4/STS-12 rate signal from the Drop bus. The first bit received (dropped) corresponds to bit 7.
TBDCLK	A15	I	LVTTL-5	**Drop Bus Clock:** This clock operates at 77.76 MHz for STM-4/STS-12 operation and is used to clock data and other signals into the EtherMap-12. Drop bus byte wide data, the parity bit, SPE indication, and the C1J1V1 signals are clocked into the EtherMap-12 on negative transitions of this clock.
TBDC1J1V1	D14	I	LVTTL-5	**Drop Bus SPE Indicator/Multiframe Pulse:** An active high timing signal that carries frame and SPE information. This signal works in conjunction with the TBDSPE signal. The single C1 pulse identifies the location of the first C1 byte when TBDSPE signal is low. One J1 pulse per STS/AU identifies the starting location of the J1 bytes in the STM-4/STS-12 signal when TBDSPE is high. One V1 pulse per substructured STS/AU identifies the V1/V2 multiframe. The J1 pulse is optional in the TBDC1J1V1 signal. The EtherMap-12 provides pointer tracking. The V1 pulse is optional in the TBDC1J1V1 signal. The EtherMap-12 also provides H4 detectors to determine the location of the V1/V2 bytes in place of using the V1 pulse.
TBDSPE	C14	I	LVTTL-5	**Drop Bus SPE Indicator:** A signal that is active high during each byte of the STM-4/STS-12 POH and payload bytes, and low during Transport Overhead byte times.
TBDPAR	B14	I	LVTTL-5	**Drop Bus Parity Bit:** Parity bit input signal that represents the parity calculation for each data byte, SPE, and C1J1V1 signal from the bus. Even or odd parity may be detected, and an option for the data byte only is provided. A parity error has no effect of the operation of the EtherMap-12. A control bit is provided that allows even or odd parity to be detected.

PRODUCT PREVIEW

LINE SIDE ADD TELECOM BUS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TBAD7 TBAD6 TBAD5 TBAD4 TBAD3 TBAD2 TBAD1 TBAD0	D11 C11 B11 D12 C12 B12 A12 D13	O(T)	LVCMOS 16 mA	**Add Bus Data Byte Out:** Byte wide data that corresponds to the selected TU/VT/VC. The first bit transmitted (added) corresponds to bit 7.
TBAC1J1V1	B10	I/O*	LVTTL-5/ LVCMOS 16 mA	**Add Bus SPE Indicator/Multiframe Pulse:** Composite active high input timing signal that carries STM-4 or STS-12 starting frame, and J1 byte location information. This timing signal functions in conjunction with the **TBASPE** signal. The C1(J0) pulse identifies the location of the first C1(J0) byte in the SONET/SDH frame when TBASPE is low. A J1 pulse identifies the starting location of each J1 byte in the constituent VC-4 signal or three J1 pulses identify the starting location of the twelve J1 bytes for the STS-1 signals in the STS-12 signal when TBASPE is high. One or more V1 pulses may be present for asynchronous VT/TU mappings to determine the starting location of the V1 byte. This signal is active high during each byte of the STM-4/STS-12 payload, and low during Transport Overhead times.
TBASPE	E11	I/O*	LVTTL-5/ LVCMOS 16 mA	**Add Bus SPE Indicator:** This signal is active high during each byte of the POH and payload bytes, and low during Transport Overhead times.
TBAPAR	C10	O(T)	LVCMOS 16 mA	**Add Bus Parity Signal:** An odd or even parity output signal which is calculated over the byte wide add data. This 3-state lead is only active when there is data being added to the Add bus. A control bit is provided that allows even or odd parity to be calculated.
$\overline{\text{TBADD}}$	A9	O	LVCMOS 16 mA	**Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the Add bus is valid. It identifies the location of all of the TU/VT time slots being selected. A control bit is provided that allows this bit to be active high.

* When TBMASTER =0 and TBMODE =1, these signals are output by the device for source timing, in all other cases these signals must be input for ADD bus timing.

ETHERNET GMII/ 8xSMII INTERFACES

The control lead, GMII/$\overline{\text{SMII}}$, when LOW, selects the group of eight SMII Ethernet interfaces, and when HIGH, selects the single GMII interface. The GMII interface is described in the section below, and also how the leads are shared with the SMII interface leads.

Each SMII interface is comprised of a 125 MHz Serial Transmit Data Output (SMII_DOn) and Serial Receive Data Input (SMII_DIn); where n = 1 to 8.

Symbol	Lead No.	I/O/P	Type	Name/Function
ETNTXGCLK	AC8	O	LVCMOS 12 mA	**Gigabit Ethernet Transmit Clock Output:** In GMII mode, this lead is used to output a 125MHz clock (i.e., to a PHY device). The **ETNTXD[7-0]**, **ETNTXEN** and **ETNTXER** signals are synchronously driven with this clock. In SMII mode, this clock should not be used.
ETNTXCLK	AF7	I	LVTTL-5	**GMII Transmit Clock:** In GMII mode, this lead is used, alternatively, to input a 125MHz clock (i.e., either from a PHY device or an external system clock source), to be used for the GMII transmit side datapath signals such as **ETNTXD[7-0]**, **ETNTXEN** and **ETNTXER.** In SMII mode, this input is not used.
ETNTXEN	AE8	I/O	LVTTL-5/ LVCMOS 12 mA	**GMII Transmit Enable/Global SMII SYNC:** In GMII mode, this lead is used to output a control signal to indicate valid data is being presented on the **ETNTXD[7-0]**. In SMII mode and when connected to a PHY device (or a switch), this lead is used to output a global SYNC signal (i.e., common for all eight SMII interfaces). In SMII mode and when connected to a switch device (i.e., a MAC-MAC connection), this lead is used to input a global SYNC signal (i.e., common for all eight SMII interfaces).
ETNTXER	AB9	O	LVCMOS 8 mA	**GMII Transmit Error:** In GMII mode, this lead is used to output a control signal to indicate that a coding violation was received on the input data stream. In SMII mode, this input lead is not used.
ETNTXD7 ETNTXD6 ETNTXD5 ETNTXD4 ETNTXD3 ETNTXD2 ETNTXD1 ETNTXD0	AE10 AF8 AE9 AB10 AC10 AD9 AD8 AC9	O	LVCMOS 12 mA	**GMII/SMII Transmit Data Out:** In GMII mode, these leads are used to output the byte wide data (i.e., to a PHY device). In SMII mode, each of the eight leads is used to output an independent serial data stream for the corresponding SMII interface.
ETNRXD7 ETNRXD6 ETNRXD5 ETNRXD4 ETNRXD3 ETNRXD2 ETNRXD1 ETNRXD0	AC12 AB12 AD12 AF11 AD11 AC11 AB11 AF10	I	LVTTL-5	**GMII/SMII Receive Data In:** In GMII mode, these leads are used to input the byte wide data (i.e., from a PHY device). In SMII mode, each of the eight leads is used to input an independent serial data stream for the corresponding SMII interface.

Symbol	Lead No.	I/O/P	Type	Name/Function
ETNRXDV	AE11	I	LVTTL-5	**GMI Receive Data Valid:** In GMII mode, this lead is used as an input to indicate valid data is present on the **ETNRXD[7-0]**. In SMII mode, this lead is not used.
ETNRXER	AE12	I	LVTTL-5	**GMII Receive Data Error:** In GMII mode, this lead is used to input a control signal to indicate that a frame has been received in error. In SMII mode, this lead is not used.
ETNRXCLK	AF12	I	LVTTL	**GMII/SMII Receive Clock:** In GMII mode, this lead is used to input a 125MHz clock (i.e., from a PHY device), to be used for the GMII receive side datapath signals such as **ETNRXD[7-0]**, **ETNRXDV** and **ETNRXER.** In SMII mode, this lead is used to input a global 125MHz clock signal (i.e., common for all eight SMII interfaces).
ETNMDIO	AC13	I/O	LVTTL-5 /LVCMOS 8 mA	**MII Management Data I/O:** This is a bidirectional lead that is used for serial data to be clocked in or out of an external PHY device. Serial data is clocked out synchronously with the clock **ETNMDC** lead. (Data input/output for the IEEE 802.3u compliant Management and Status.) This lead is used in both GMII and SMII modes.
ETNMDC	AD13	O	LVCMOS 8 mA	**MII Management Data Interface Clock:** This lead will output a clock of 2.5MHz used to synchronously transfer data in and out of an external PHY device using the **ETNMDIO** lead.

SDRAM INTERFACE 1

Symbol	Lead No.	I/O/P	Type	Name/Function
SD1D31 SD1D30 SD1D29 SD1D28 SD1D27 SD1D26 SD1D25 SD1D24 SD1D23 SD1D22 SD1D21 SD1D20 SD1D19 SD1D18 SD1D17 SD1D16 SD1D15 SD1D14 SD1D13 SD1D12 SD1D11 SD1D10 SD1D09 SD1D08 SD1D07 SD1D06 SD1D05 SD1D04 SD1D03 SD1D02 SD1D01 SD1D00	T4 U3 U1 U2 T2 R4 T3 T1 R2 R3 R1 P3 P4 N2 P1 P2 N4 N1 N3 M5 M4 M2 M3 L1 L4 L2 K1 L3 L5 K2 K4 J1	I/O(T)	LVTTL/LV3 CMOS 16 mA	**SDRAM Data bus:** 32 bits wide Data bus; byte wise tri-stateable.
SD1A12 SD1A11 SD1A10 SD1A09 SD1A08 SD1A07 SD1A06 SD1A05 SD1A04 SD1A03 SD1A02 SD1A01 SD1A00	Y4 AA3 V4 AA1 V5 W3 Y1 W2 Y2 V3 U5 U4 V2	O	LV3CMOS 16 mA	**SDRAM Address Bus:** 13 bits wide Address bus.

Symbol	Lead No.	I/O/P	Type	Name/Function
SD1BA1 SD1BA0	Y5 AB1	O	LV3CMOS 16 mA	**Bank Select:** These signals are used to select the banks of a standard SDRAM device.
$\overline{\text{SD1RAS}}$	AB2	O	LV3CMOS 16 mA	**Row Address Strobe:** For control of external SDRAM. This signal along with $\overline{\text{SD1CAS}}$ and $\overline{\text{SD1WE}}$ define the command being given to the external SDRAM.
$\overline{\text{SD1CAS}}$	AA4	O	LV3CMOS 16 mA	**Column Address Strobe:** For control of external SDRAM. his signal along with $\overline{\text{SD1WE}}$ and $\overline{\text{SD1RAS}}$ define the command being given to the external SDRAM. Refer to the table in the $\overline{\text{SD1RAS}}$ lead description.
$\overline{\text{SD1WE}}$	AB4	O	LV3CMOS 16 mA	**Write Enable:** For control of external SDRAM. This signal along with $\overline{\text{SD1CAS}}$ and $\overline{\text{SD1RAS}}$ define the command being given to the external SDRAM. Refer to the table in the $\overline{\text{SD1RAS}}$ lead description.
$\overline{\text{SD1CS2}}$ $\overline{\text{SD1CS1}}$	AC1 AB3	O	LV3CMOS 16 mA	**Chip Select:** For control of external SDRAM. Used to select and deselect external SDRAM.
SD1MASK	AC2	O	LVCMOS 16 mA	**Mask Bits:** This control output is used to mask out the standard 32 bit wide SDRAM memory interface. It is used to tristate the SDRAM data bus during a READ cycle and to mask the SDRAM data bus during a WRITE cycle.
SD1CLKA	V1	O	LV3CMOS 16 mA	**Interface Clock:** For control of external SDRAM. All SDRAM interface signals are sampled/output on the rising edge of this clock, which runs at 125 MHz.

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Function
1	1	1	**NOP: No operation**
0	1	1	**ACTIVE:** Used to activate a row in a particular bank. The SD1BA(1-0) selects the bank, and SD1A(12-0) selects the row.
1	0	1	**READ:** Used to initialize the SDRAM for a burst read.
1	0	0	**WRITE:** Used to initialize the SDRAM for a burst write.
0	1	0	**PRECHARGE:** Deactivate open row in a bank or banks.
0	0	1	**AUTO REFRESH:** This command is performed every 1240 SYSCLK period, to ensure that all of the SDRAM rows are refreshed. This default setting can be changed by SDRARP at register address TBD.
0	0	0	**LOAD MODE REGISTER:** This command is issued at the end of the configuration step, to configure the internal mode register of the SDRAM. It is the last command before the SDRAM to be ready for read/write accesses.

Symbol	Lead No.	I/O/P	Type	Name/Function
SD1CLKB	T5	I	LVTTL-5	**Interface Clock Input:** For control of external SDRAM. This input must be connected externally to SD2CLKA output.
SD1CLKE	AC3	O	LV3CMOS 16 mA	**Interface Clock Enable:** For control of external SDRAM. High is intended to activate the clock, low is intended to deactivate the clock.

SDRAM INTERFACE 2

Symbol	Lead No.	I/O/P	Type	Name/Function
SD2D31	N26	I/O(T)	LVTTL/LV CMOS 16 mA	**SDRAM Data Bus:** 32 bits wide Data bus; byte wise tri-stateable.
SD2D30	P26			
SD2D29	P25			
SD2D28	P24			
SD2D27	P23			
SD2D26	R26			
SD2D25	R25			
SD2D24	R24			
SD2D23	R23			
SD2D22	R22			
SD2D21	T26			
SD2D20	T25			
SD2D19	T24			
SD2D18	T23			
SD2D17	U26			
SD2D16	U25			
SD2D15	V26			
SD2D14	U23			
SD2D13	V25			
SD2D12	U22			
SD2D11	V24			
SD2D10	W26			
SD2D09	W25			
SD2D08	V23			
SD2D07	Y26			
SD2D06	W24			
SD2D05	V22			
SD2D04	Y25			
SD2D03	AA26			
SD2D02	W23			
SD2D01	Y24			
SD2D00	AA25			

Symbol	Lead No.	I/O/P	Type	Name/Function
SD2A12 SD2A11 SD2A10 SD2A09 SD2A08 SD2A07 SD2A06 SD2A05 SD2A04 SD2A03 SD2A02 SD2A01 SD2A00	K25 H25 L23 J25 L22 M22 M23 L24 K26 L25 M24 N23 L26	O	LVCMOS 16 mA	**SDRAM Address Bus:** 13 bits wide Address bus.
SD2BA1 SD2BA0	K23 K22	O	LVCMOS 16 mA	**Bank Select:** These signals are used to select the banks of a standard SDRAM device.
$\overline{\text{SD2RAS}}$	J24	O	LVCMOS 16 mA	**Row Address Strobe:** For control of external SDRAM. This signal along with $\overline{\text{SD2CAS}}$ and $\overline{\text{SD2WE}}$ define the command being given to the external SDRAM.
$\overline{\text{SD2CAS}}$	H24	O	LVCMOS 16 mA	**Column Address Strobe:** For control of external SDRAM. his signal along with $\overline{\text{SD2WE}}$ and $\overline{\text{SD2RAS}}$ define the command being given to the external SDRAM. Refer to the table in the $\overline{\text{SD2RAS}}$ lead description.

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Function
1	1	1	**NOP: No operation**
0	1	1	**ACTIVE:** Used to activate a row in a particular bank. The SD2BA(1-0) selects the bank, and SD2A(12-0) selects the row.
1	0	1	**READ:** Used to initialize the SDRAM for a burst read.
1	0	0	**WRITE:** Used to initialize the SDRAM for a burst write.
0	1	0	**PRECHARGE:** Deactivate open row in a bank or banks.
0	0	1	**AUTO REFRESH:** This command is performed every 1240 SYSCLK period, to ensure that all of the SDRAM rows are refreshed. This default setting can be changed by SDRARP at register address TBD.
0	0	0	**LOAD MODE REGISTER:** This command is issued at the end of the configuration step, to configure the internal mode register of the SDRAM. It is the last command before the SDRAM to be ready for read/write accesses.

Symbol	Lead No.	I/O/P	Type	Name/Function
SD2WE	J22	O	LVCMOS 16 mA	**Write Enable:** For control of external SDRAM. This signal along with SD2CAS and SD2RAS define the command being given to the external SDRAM. Refer to the table in the SD2RAS lead description.
SD2CS2 SD2CS1	H26 J23	O	LVCMOS 16 mA	**Chip Select:** For control of external SDRAM. Used to select and deselect external SDRAM.
SD2MASK	G26	O	LVCMOS 16 mA	**Mask Bits:** This control output is used to mask out the standard 32 bit wide SDRAM memory interface. It is used to tristate the SDRAM data bus during a READ cycle and to mask the SDRAM data bus during a WRITE cycle.
SD2CLKA	M25	O	LVCMOS 16 mA	**Interface Clock:** For control of external SDRAM. All SDRAM interface signals are sampled/output on the rising edge of this clock, which runs at 125 MHz.
SD2CLKB	M26	I	LVTTL	**Interface Clock input:** For control of external SDRAM. This input must be connected externally to SD2CLKA output.
SD2CLKE	G25	O	LVCMOS 16 mA	**Interface Clock Enable:** For control of external SDRAM. High is intended to activate the clock, low is intended to deactivate the clock.

RECEIVE HO PATH OVERHEAD (HOPOH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHRXCLK	B21	O	LVCMOS 12 mA	**Receive HOPOH Interface Clock:** The receive HOPOH address (POHRXPADD), address latch enable (POHRXALE), data (POHRXDAT), and data latch enable (POHRXDLE) signals are clocked out on falling edges of this clock (77.76 MHz).
POHRXALE	C20	O	LVCMOS 8 mA	**Receive HOPOH Interface Address Latch Enable:** A positive 8 (POHRXCLK) clock cycle-wide pulse that indicates a valid address (eight consecutive bits) present on POHRXADD.
POHRXADD	A21	O	LVCMOS 8 mA	**Receive HOPOH Interface Address:** The states present on these leads during address latch enable time indicate the output HOPOH byte and the SDH/SONET format. Eight consecutive bits make up a valid address.
POHRXDLE	D19	O	LVCMOS 8 mA	**Receive HOPOH Interface Data Latch Enable:** A positive 8 (POHRXCLK) clock cycle-wide pulse that indicates valid data present on POHRXDAT.
POHRXDAT	B20	O	LVCMOS 8 mA	**Receive HOPOH Interface Data:** The states present on these leads over eight consecutive bits, during data latch enable time constitute the output byte data selected by the address.

PRODUCT PREVIEW

TRANSMIT HO PATH OVERHEAD (HOPOH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHTXCLK	D8	O	LVCMOS 12 mA	**Transmit HOPOH Interface Clock:** The transmit POH address (POHTXADD), address latch enable (POHTXALE), and data latch enable (POHTXDLE) signals are clocked out on falling edge of POHTXCLK (77.76 MHz). Data (POHTXDAT), is clocked in.
POHTXALE	A6	O	LVCMOS 8 mA	**Transmit HOPOH Interface Address Latch Enable:** A positive 8 (POHTXCLK) clock cycle-wide pulse that indicates a valid address (Eight consecutive bits) present on POHTXADD.
POHTXADD	C7	O	LVCMOS 8 mA	**Transmit HOPOH Interface Address:** The states present on this lead during address latch enable time indicate the output POH byte and the SDH/SONET format. Eight consecutive bits make up a valid address.
POHTXDLE	B6	O	LVCMOS 8 mA	**Transmit HOPOH Interface Data Latch Enable:** A positive 8 (POHTXCLK) clock cycle-wide pulse that indicates valid data present on POHTXDAT
POHTXDAT	E8	I	LVTTL-5	**Transmit HOPOH Interface Data:** The states present on these leads over eight consecutive bits, during data latch enable time, constitute the input byte data selected by the address.

RECEIVE LOWER ORDER PATH OVERHEAD (LOPOH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHRXCLK1	E18	O	LVCMOS 12 mA	**Receive LOPOH Interface Clock:** The receive LOPOH address (POHRXADD1), address latch enable (POHRXALE1), data (POHRXDAT1), and data latch enable (POHRXDLE1) signals are clocked out on falling edges of this clock (77.76 MHz).
POHRXALE1	C19	O	LVCMOS 8 mA	**Receive LOPOH Interface Address Latch Enable:** A positive 12 (POHRXCLK1) clock cycle-wide pulse that indicates a valid address (twelve consecutive bits) present on POHRXADD1.
POHRXADD1	A20	O	LVCMOS 8 mA	**Receive LOPOH Interface Address:** The states present on these leads during address latch enable time indicate the output LOPOH byte and the SONET/SDH format. Twelve consecutive bits make up a valid address.
POHRXDLE1	B19	O	LVCMOS 8 mA	**Receive LOPOH Interface Data Latch Enable:** A positive 8 (POHRXCLK1) clock cycle-wide pulse that indicates valid data present on RPDAT1.
POHRXDAT1	D18	O	LVCMOS 8 mA	**Receive LOPOH Interface Data:** The states present on these leads over eight consecutive bits, during data latch enable time constitute the output byte data selected by the address.

TRANSMIT LOWER ORDER PATH OVERHEAD (LOPOH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHTXCLK1	A5	O	LVCMOS 12 mA	**Transmit LOPOH Interface Clock:** The transmit LOPOH address (POHTXADD1), address latch enable (POHTXALE1), and data latch enable (POHTXDLE1) signals are clocked out on falling edge of POHTXCLK1 (77.76 MHz). Data (POHTXDAT1), is clocked in.
POHTXALE1	C6	O	LVCMOS 8 mA	**Transmit LOPOH Interface Address Latch Enable:** A positive 12 (POHTXCLK1) clock cycle-wide pulse that indicates a valid address (twelve consecutive bits) present on POHTXADD1.
POHTXADD1	D7	O	LVCMOS 8 mA	**Transmit LOPOH Interface Address:** The states present on this lead during address latch enable time indicate the output LOPOH byte and the SONET/SDH format. Twelve consecutive bits make up a valid address.
POHTXDLE1	B5	O	LVCMOS 8 mA	**Transmit LOPOH Interface Data Latch Enable:** A positive 8 (POHTXCLK1) clock cycle-wide pulse that indicates valid data present on POHTXDAT1.
POHTXDAT1	A4	I	LVTTL-5	**Transmit LOPOH Interface Data:** The states present on these leads over eight consecutive bits, during data latch enable time, constitute the input byte data selected by the address.

RECEIVE (HO) HIGH ORDER ALARM INDICATION PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
RINGRXIPF	C18	O	LVCMOS 8 mA	**Receive HO Alarm Indication Port Frame Pulse:** A active high one (RINGRXIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream.
RINGRXIPC	E17	O	LVCMOS 8 mA	**Receive HO Alarm Indication Port Clock:** A 77.76 MHz output clock used for clocking the frame pulse (RINGRXIPF) and the serial data (RINGRXIPD).
RINGRXIPD	B18	O	LVCMOS 8 mA	**Receive HO Alarm Indication Port Data:** A serial frame that contains the REI count and RDI alarm states for the High Order paths. The REI count is converted to a four bit count. One byte per channel (24 channels) are needed.

TRANSMIT (HO) HIGH ORDER ALARM INDICATION PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
RINGTXIPF	A8	I	LVTTL-5	**Transmit HO Alarm Indication Port Frame Pulse:** A active high one (RINGTXIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream.
RINGTXIPC	B8	I	LVTTL-5	**Transmit HO Alarm Indication Port Clock:** A 77.76 MHz output clock used for clocking in the frame pulse (RINGTXIPF) and the serial data (RINGTXIPD).

Symbol	Lead No.	I/O/P	Type	Name/Function
RINGTXIPD	D9	I	LVTTL-5	**Transmit HO Alarm Indication Port Data:** A serial frame that contains the REI count, RDI alarm states, and the Tandem Connection monitoring and alarm states for the individual High Order paths.

RECEIVE LO ORDER ALARM INDICATION PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
RINGRXIPF1	D17	O	LVCMOS 8 mA	**Receive LO Alarm Indication Port Frame Pulse:** A active high one (RINGRXIPC1=19.44) clock cycle-wide frame pulse that identifies bit 1 in the data stream.
RINGRXIPC1	A18	O	LVCMOS 8 mA	**Receive LO Alarm Indication Port Clock:** A 77.76 MHz output clock used for clocking in the frame pulse (RINGRXIPF1) and the serial data (RINGRXIPD1).
RINGRXIPD1	C17		LVCMOS 8 mA	**Receive LO Alarm Indication Port Data:** A serial frame that contains the REI count, RDI alarm states for the VT/TUs.

TRANSMIT LOW ORDER ALARM INDICATION PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
RINGTXIPF1	A7	I	LVTTL-5	**Transmit LO Alarm Indication Port Frame Pulse:** A active high one (RINGTXIPC1) clock cycle-wide frame pulse that identifies bit 1 in the data stream.
RINGTXIPC1	C8	I	LVTTL-5	**Transmit LO Alarm Indication Port Clock:** A 77.76 MHz output clock used for clocking in the frame pulse (RINGTXIPF1) and the serial data (RINGTXIPD1).
RINGTXIPD1	E9	I	LVTTL-5	**Transmit LO Alarm Indication Port Data:** A serial frame that contains the REI count, RDI alarm states, and the Tandem Connection monitoring and alarm states for the individual LO VT/TU Paths.

CONTROLS

Symbol	Lead No.	I/O/P	Type	Name/Function
GMII/$\overline{\text{SMII}}$	AD6	I	LVTTL-5p	**GMII/SMII Interface Select:** When low, the eight SMII interfaces are selected. When high, the single GMII interface is selected. This lead must be held in the steady state during initialization/reset phase. This lead has an internal pull-up resistor.
$\overline{\text{DEVHIZ}}$	AC7	I	LVTTL-5p	**High Impedance Select:** A low forces all output leads, except for the boundary scan data output TBDO, to the high impedance state for testing purposes. This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{RESET}}$	AB8	I	LVTTL-5p	**Reset:** An active low signal used for resetting the internal cores/blocks and performance counters within the EtherMap-12 to preset values. The reset must be applied only after power is applied and stable, and the clocks are also stable. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor.
PHY/$\overline{\text{MAC}}$	AE6	I	LVTTL-5p	**PHY/MAC Interface Select:** In SMII mode and when low, the EtherMap-12 device is connected to a MAC (i.e., a switch). In SMII mode and when high, the EtherMap-12 device is connected to a PHY device. In GMII mode and when high, the EtherMap-12 device will use the GMII RX_CLK (of 125MHz) to drive the GMII transmit side and output onto GTX_CLK (ENTRXCLK lead) lead (i.e., ETNTXGCLK lead). In GMII mode and when low, the EtherMap-12 device will use the TX_CLK (ETNTXCLK lead) to drive the GMII transmit side and output onto GTX_CLK lead. This lead has an internal pull-up resistor.
ETNSYNCDIR	AF14	I	LVTTL-5p	**SMII Global SYNC Direction Select:** In SMII mode and when low, the SMII_GSYNC signal (ETNTXEN lead) is an input. In SMII mode and when high, the SMII_GSYNC signal will be an output. In GMII mode, this lead is not used. This lead has an internal pull-up resistor.
TBMODE	B9	I	LVTTL-5	**TBMODE:** Selection of the mode of the line Telecom Bus. 0 means add slave, 1 means add master.
TBMASTER	D10	I	LVTTL-5d	**TBMASTER:** Selection of the mode of the line Telecom Bus. 0 means selection of the mode with TBMODE. 1 means add master with TBAC1J1V1 and TBASPE in tristate (independently from the value of TBMODE).

CLOCK INTERFACES

Symbol	Lead No.	I/O/P	Type	Name/Function
RTCLK	A10	I	LVTTL-5d	**SONET/SDH Reference Clock:** This clock is a 77.76 MHz +/- 20 ppm reference clock used by the SONET/SDH blocks.
RTFS	A13	I	LVTTL-5d	**SONET/SDH Reference Frame Sync:** A 8 kHz reference frame sync pulse synchronous to RTCLK.
RTMFS	C13	I	LVTTL-5d	**SONET/SDH Reference Multiframe Sync:** A 2kHz reference frame sync pulse synchronous to RTCLK (and RTFS, if present).
SYSCLK	AB21	I	CMOS	**System Reference Clock:** A 50 MHz input clock for all blocks except the SONET/SDH blocks.
ONESEC	B13	I	LVTTL-5d	**One Second Performance Measurement Clock:** A 1.0 Hz +/- 32 ppm clock used for the one second shadow counters, and PM/FM alarm registers.

PRODUCT PREVIEW

HOST PROCESSOR INTERFACE SELECTION

Symbol	Lead No.	I/O/P	Type	Name/Function
MPMODE1 MPMODE0	AE23 AD22	I	LVTTL	**Microprocessor Interface Select:** These leads select the Host Processor interface mode:

MPMODE1	MPMODE0	Interface
0	0	Generic Intel
0	1	Generic Motorola
1	0	Motorola MPC860
1	1	Motorola MPC8260 Local Bus

Note: All host processor interface modes share the same leads.

GENERIC INTEL - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	AD23	I	LVTTL	**Microprocessor Interface Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Intel notation: CLK**
MPA16 MPA15 MPA14 MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	AF18 AD17 AE17 AB16 AF17 AC16 AD16 AE16 AF16 AB15 AC15 AD15 AE15 AF15 AC14 AD14 AE14	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the EtherMap-12 for a read or write cycle. MPA16 is the most significant bit in the location's address. **Intel notation: A[ ]**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	AC20 AF22 AB19 AE21 AD20 AF21 AC19 AE20 AB18 AD19 AF20 AC18 AE19 AF19 AD18 AB17	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the EtherMap-12 and the host processor. MPD15 is the most significant bit. **Intel notation: D[ ]**
MPSEL	AD21	I	LVTTL	**EtherMap-12 Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the EtherMap-12 through a read or write cycle. **Intel notation: CS**
MPTS	AE22	I	LVTTL	**Read Strobe (Active low):** This active low lead initiates a read transfer between the host processor and the EtherMap-12. **Intel notation: RD**
MPWR	AF23	I	LVTTL	**Write Strobe (Active Low):** This active low lead initiates a write transfer between the host processor and the EtherMap-12. **Intel notation: WR**
MPACK	AB20	O(T)	LVCMOS 24mA	**Ready (Active low):** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. **Intel notation: RDY**
MPINTR	AC21	O	LVCMOS 8mA	**Interrupt (Active high):** This lead signals an interrupt request to the host processor.

GENERIC MOTOROLA - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	AD23	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola notation: CLK**

PRODUCT PREVIEW

Symbol	Lead No.	I/O/P	Type	Name/Function
MPA16 MPA15 MPA14 MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	AF18 AD17 AE17 AB16 AF17 AC16 AD16 AE16 AF16 AB15 AC15 AD15 AE15 AF15 AC14 AD14 AE14	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the EtherMap-12 for a read or write cycle. MPA16 is the most significant bit in the location's address. **Motorola notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	AC20 AF22 AB19 AE21 AD20 AF21 AC19 AE20 AB18 AD19 AF20 AC18 AE19 AF19 AD18 AB17	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the EtherMap-12 and the host processor. MPD15 is the most significant bit. **Motorola notation: D[ ]**
MPSEL	AD21	I	LVTTL	**EtherMap-12 Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the EtherMap-12 through a read or write cycle. **Motorola notation: $\overline{CS}$**
MPTS	AE22	I	LVTTL	**Data Strobe (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the EtherMap-12. **Motorola notation: $\overline{DS}$**
MPWR	AF23	I	LVTTL	**Read/$\overline{\text{Write}}$ (Active Low):** This active low lead indicates that the actual transfer between the host processor and the EtherMap-12 is a write transfer. **Motorola notation: R/$\overline{W}$**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPACK	AB20	O(T)	LVCMOS 24mA	**Data Transfer Acknowledge (Active low):** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola notation: DSACK**
MPINTR	AC21	O	LVCMOS 8mA	**Interrupt Request (Active low):** This lead signals an interrupt request to the host processor.

MOTOROLA MPC860 - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	AD23	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC860 notation: CLK**
MPA16 MPA15 MPA14 MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	AF18 AD17 AE17 AB16 AF17 AC16 AD16 AE16 AF16 AB15 AC15 AD15 AE15 AF15 AC14 AD14 AE14	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the EtherMap-12 for a read or write cycle. MPA16 is the most significant bit in the location's address. **Motorola MPC860 notation: A[ ]**

PRODUCT PREVIEW

Symbol	Lead No.	I/O/P	Type	Name/Function
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	AC20 AF22 AB19 AE21 AD20 AF21 AC19 AE20 AB18 AD19 AF20 AC18 AE19 AF19 AD18 AB17	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the EtherMap-12 and the host processor. MPD15 is the most significant bit. **Motorola MPC860 notation: D[ ]**
MPSEL	AD21	I	LVTTL	**EtherMap-12 Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the EtherMap-12 through a read or write cycle. **Motorola MPC860 notation: CS**
MPTS	AE22	I	LVTTL	**Transfer Start (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the EtherMap-12. It is active low only during the first cycle of the access. **Motorola MPC860 notation: TS**
MPWR	AF23	I	LVTTL	**Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the EtherMap-12 is a write transfer. **Motorola MPC860 notation: RD/WR**
MPACK	AB20	O(T)	LVCMOS 24mA	**Transfer Acknowledge (Active Low):** This active low lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC860 notation: TA**
MPINTR	AC21	O	LVCMOS 8mA	**Interrupt Request (Active low):** This lead signals an interrupt request to the host processor.

MOTOROLA MPC8260 LOCAL BUS - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	AD23	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC8260 Notation: CLK**
MPA16 MPA15 MPA14 MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	AF18 AD17 AE17 AB16 AF17 AC16 AD16 AE16 AF16 AB15 AC15 AD15 AE15 AF15 AC14 AD14 AE14	I	LVTTL	**Local Address Bus:** These leads are the address bus used by the host processor for accessing the EtherMap-12 for a read or write cycle. MPA16 is the most significant bit in the location's address. **Motorola MPC8260 Notation: L_A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	AC20 AF22 AB19 AE21 AD20 AF21 AC19 AE20 AB18 AD19 AF20 AC18 AE19 AF19 AD18 AB17	I/O(T)	LVTTL/ LVCMOS 8mA	**Local Data Bus:** These leads are the bidirectional data bus used for transferring data between the EtherMap-12 and the host processor. MPD15 is the most significant bit. **Motorola MPC8260 Notation: LCL_D[ ]**
MPSEL	AD21	I	LVTTL	**EtherMap-12 Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the EtherMap-12 through a read or write cycle. **Motorola MPC8260 notation: CS**
MPTS	AE22	I	LVTTL	**Not Applicable Input:** This lead must be tied to VSS.

Symbol	Lead No.	I/O/P	Type	Name/Function
MPWR	AF23	I	LVTTL	**Local Bus Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the EtherMap-12 is a write transfer. **Motorola MPC8260 notation: LWR**
MPACK	AB20	O(T)	LVCMOS 24mA	**Local Bus GPCM Transfer Acknowledge (Active Low):** This lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle and then de-asserted during 3 MPCLK cycles before going in tristate. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC8260 notation: LGTA**
MPINTR	AC21	O	LVCMOS 8mA	**Interrupt Request (Active low):** This lead signals an interrupt request to the host processor.

BOUNDARY SCAN (IEEE STANDARD 1149.1)

Symbol	Lead No.	I/O/P	Type	Name/Function
TCK	F2	I	LVTTL-5	**Test Boundary Scan Clock:** This signal is used to shift data into TDI on its rising edge and out of TDO on its falling edge. The maximum clock frequency is 10 MHz.
TDI	D1	I	LVTTL-5p	**Test Boundary Scan Data Input:** Serial test instructions and data are clocked into this lead on the rising edge of TCK. This lead has an internal pull-up resistor.
TDO	E2	O	LVCMOS 8 mA	**Test Boundary Scan Data Output:** Serial data test instructions and data are clocked out of this lead on the falling edge of TCK. When inactive, this lead goes to a high impedance state.
TMS	F3	I	LVTTL-5p	**Test Boundary Scan Mode Select:** This input lead is sampled on the rising edge of TCK. It is used to place the Test Access Port controller into various states, as defined in IEEE 1149.1. An internal pull-up holds this lead high during normal operation. This lead has an internal pull-up resistor.
$\overline{\text{TRST}}$	E1	I	LVTTL-5p	**Test Boundary Scan Reset:** An active low signal that asynchronously resets the Test Access Port controller. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor.

TEST

Symbol	Lead No.	I/O/P	Type	Name/Function
SCANEN	AB25	I	LVTTL-5d	**Scan Enable:** This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low.
SCANMODE	AF5	I	LVTTL-5d	**Scan Mode:** This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low.
TESTIN8	AE5	I	LVTTL-5d	**Test Input:** This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low.
PLLBYPASS	AA24	I	LVTTL-5d	**PLL Bypass:** This lead is used for TranSwitch Testing purposes only. This lead should be held low for correct operation. PLLBYPASS has an internal pull-down to VSS.
PLLOUT	Y23	O	LVCMOS 4mA	**PLL Output:** This lead is used for TranSwitch Testing purposes only. This lead should be left open (floating).
MBISTMODE	AC26	I	LVTTL-5d	**Memory Bist:** This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low.
TESTIN7 TESTIN6 TESTIN5 TESTIN4 TESTIN3 TESTIN2 TESTIN1 TESTIN0	H2 G1 G2 H4 H3 G3 F1 H5	I	LVTTL-5p	**Test Input:** These leads are used for TranSwitch Testing purposes only. These leads have internal pull-ups to VDD and should be held high.
TESTOUT7 TESTOUT6 TESTOUT5 TESTOUT4 TESTOUT3 TESTOUT2 TESTOUT1 TESTOUT0	AB7 AC6 AD5 AE4 AD4 H1 J2 J4	O	LVCMOS 4mA	**Test Output:** These leads are used for TranSwitch Testing purposes only. These leads should be left open (floating).

Symbol	Lead No.	I/O/P	Type	Name/Function
SCANIN39	G24	I	LVTTL-5	**Test Input:** These leads are used for TranSwitch Testing purposes only. These leads should be held low.
SCANIN38	F25			
SCANIN37	H22			
SCANIN36	E26			
SCANIN35	G23			
SCANIN34	F24			
SCANIN33	E25			
SCANIN32	D26			
SCANIN31	G22			
SCANIN30	F23			
SCANIN29	E24			
SCANIN28	D25			
SCANIN27	D24			
SCANIN26	F22			
SCANIN25	C23			
SCANIN24	B23			
SCANIN23	C22			
SCANIN22	D21			
SCANIN21	E20			
SCANIN20	A23			
SCANIN19	B22			
SCANIN18	C21			
SCANIN17	D20			
SCANIN16	C5			
SCANIN15	B4			
SCANIN14	C4			
SCANIN13	D5			
SCANIN12	E4			
SCANIN11	D3			
SCANIN10	D2			
SCANIN9	E3			
SCANIN8	F4			

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS (REFERENCED TO VSS)

Parameter	Symbol	Min	Max	Unit	Conditions
I/O Supply voltage (3.3V)	V_{DD33}	-0.3	3.9	V	Note 1, 4
Core Supply voltage (1.2V)	V_{DD12}	-0.3	1.4	V	Note 1, 4
DC input voltage LVTTL input voltage LVTTL-5 input voltage	V_{IN}	 0 -0.5	 3.3 5.5	V	Note 1, 4
Storage temperature range	T_S	-55	+150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	+85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		2	kV	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883E, Method 3015.7.
4. Device core is 1.2 V only. All input signals leads accept 5V signals except for SMII/GMII and SDRAM memory interface signals which accept only 3.3V signals.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient		16		$^oC/W$	Test performed with package assembled on JEDEC standard Multi-layer test board with 0 ft/min linear airflow.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD33}	3.135	3.30	3.465	V	
I_{DD33}		TBD		mA	
V_{DD12}	1.14	1.20	1.26	V	
I_{DD12}		TBD		mA	
Power Dissipation, $P_{DDTOTAL}$		TBD		W	

Note:

1. This is an approximate value.

PRODUCT PREVIEW

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR LVTTL-5 (5 VOLT TOLERANT)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.0	V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15 µA	µA	V_{DD33} = 3.45, Vin = V_{DD} or GND
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTL-5p (5 VOLT TOLERANT, with PULL-UP RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.0	V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			100	µA	V_{DD33} =3.45; Input = 0 volts
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTL-5d (5 VOLT TOLERANT, with PULL-DOWN RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.0	V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			-100	µA	V_{DD33} = 3.45; Input = 3.45 volts
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTL (3.3 VOLT TOLERANT)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	V_{DD33} = 3.45, Vin = V_{DD} or GND
Input capacitance		5		pF	

OUTPUT PARAMETERS FOR LVCMOS 24mA (Open Drain)

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		**TBD**		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -24.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 24.0
I_{OL}	24			mA	
I_{OH}	-24			mA	
t_{RISE}	1.23		2.74	ns	C_{LOAD} = 30 pF
t_{FALL}	1.07		2.72	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD33}.

OUTPUT PARAMETERS FOR LVCMOS 12mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		**TBD**		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -12.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 12.0
I_{OL}	12			mA	
I_{OH}	-12			mA	
t_{RISE}	1.58		3.38	ns	C_{LOAD} = 30 pF
t_{FALL}	1.38		3.47	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

OUTPUT PARAMETERS FOR LVCMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		**TBD**		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 8.0
I_{OL}	8			mA	
I_{OH}	-8			mA	
t_{RISE}	1.87		3.90	ns	C_{LOAD} = 30 pF
t_{FALL}	1.80		4.42	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

OUTPUT PARAMETERS FOR LVCMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 4.0
I_{OL}	4			mA	
I_{OH}	-4			mA	
t_{RISE}	2.81		6.02	ns	C_{LOAD} = 30 pF
t_{FALL}	3.15		7.34	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input
Output capacitance		5		pF	

INPUT/OUTPUT PARAMETERS FOR LVTTL-5 INPUT AND LVCMOS OUTPUT 12mA (5 VOLT TOLERANT Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	0 to 3.3 V input
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -12.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 12.0
I_{OL}	12			mA	
I_{OH}	-12			mA	
t_{RISE}	1.58		3.38	ns	C_{LOAD} = 30 pF
t_{FALL}	1.38		3.47	ns	C_{LOAD} = 30 pF

INPUT/OUTPUT PARAMETERS FOR LVTTL-5 INPUT AND LVCMOS OUTPUT 8mA (5 VOLT TOLERANT Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	0 to 3.3 V input
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 8.0
I_{OL}	8			mA	
I_{OH}	-8			mA	
t_{RISE}	1.87		3.91	ns	C_{LOAD} = 30 pF
t_{FALL}	1.80		4.43	ns	C_{LOAD} = 30 pF

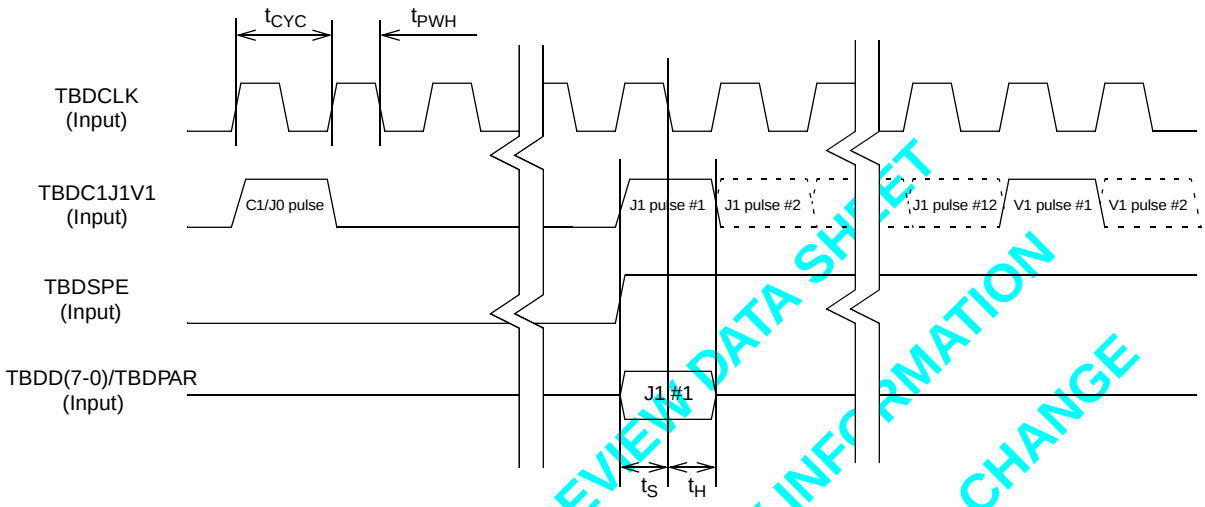
INPUT/OUTPUT PARAMETERS FOR LVTTL INPUT AND LV3CMOS OUTPUT 16mA (5V VOLT TOLERANT Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	0 to 3.3 V input
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -16.0
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 16.0
I_{OL}	16			mA	
I_{OH}	-16			mA	
t_{RISE}	1.32		2.90	ns	C_{LOAD} = 30 pF
t_{FALL}	1.19		3.07	ns	C_{LOAD} = 30 pF

TIMING CHARACTERISTICS

This section presents the detailed timing characteristics for the EtherMap-12 in Figures 7 through 35 with values of the timing parameters tabulated below each waveform diagram. All outputs are measured with a maximum load capacitance of 50 pF unless otherwise stated. Timing parameters are measured at the voltage levels of $(V_{OH} + V_{OL})/2$ for output signals and $(V_{IH} + V_{IL})/2$ for input signals.

Figure 7. Drop Bus Timing



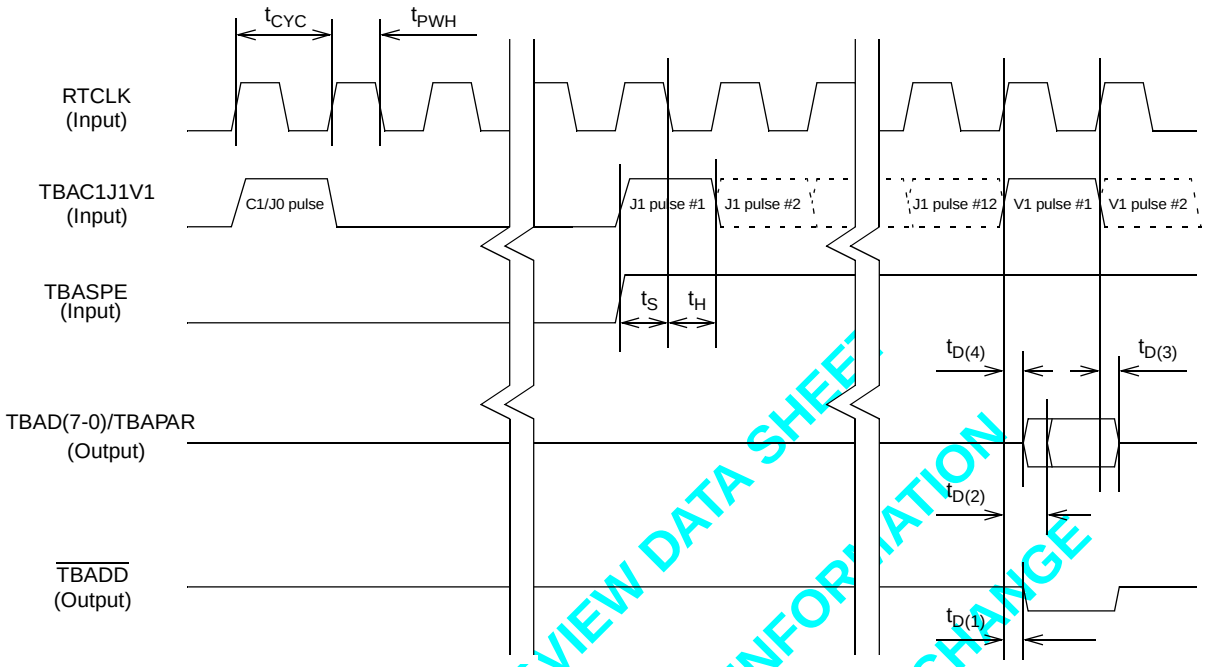
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
TBDCLK clock period	t_{CYC}		12.86		ns
TBDCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
TBDC1J1V1/TBDSPE/TBDD(7-0)/TBDPAR setup time to TBDCLK↓	t_S	3			ns
TBDC1J1V1/TBDSPE/TBDD(7-0)/TBDPAR hold time after TBDCLK↓	t_H	0			ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The active TBDCLK clock edge on which the data/parity and timing signals are clocked out can be selected, see "Drop Bus Interface" on page 176. The waveforms shown correspond to the negative clock edge selection.
3. An additional delay of 0 up to 15 extra TBDCLK clock cycles can be inserted between the Drop bus timing and the Drop bus data/parity signals, TBDC1J1V1 and TBDSPE, see "Drop Bus Interface" on page 176. The waveforms shown correspond to a delay of 0 clock cycles.

Figure 8. ADD Bus Timing (Timing signals are inputs)



50 pF Load

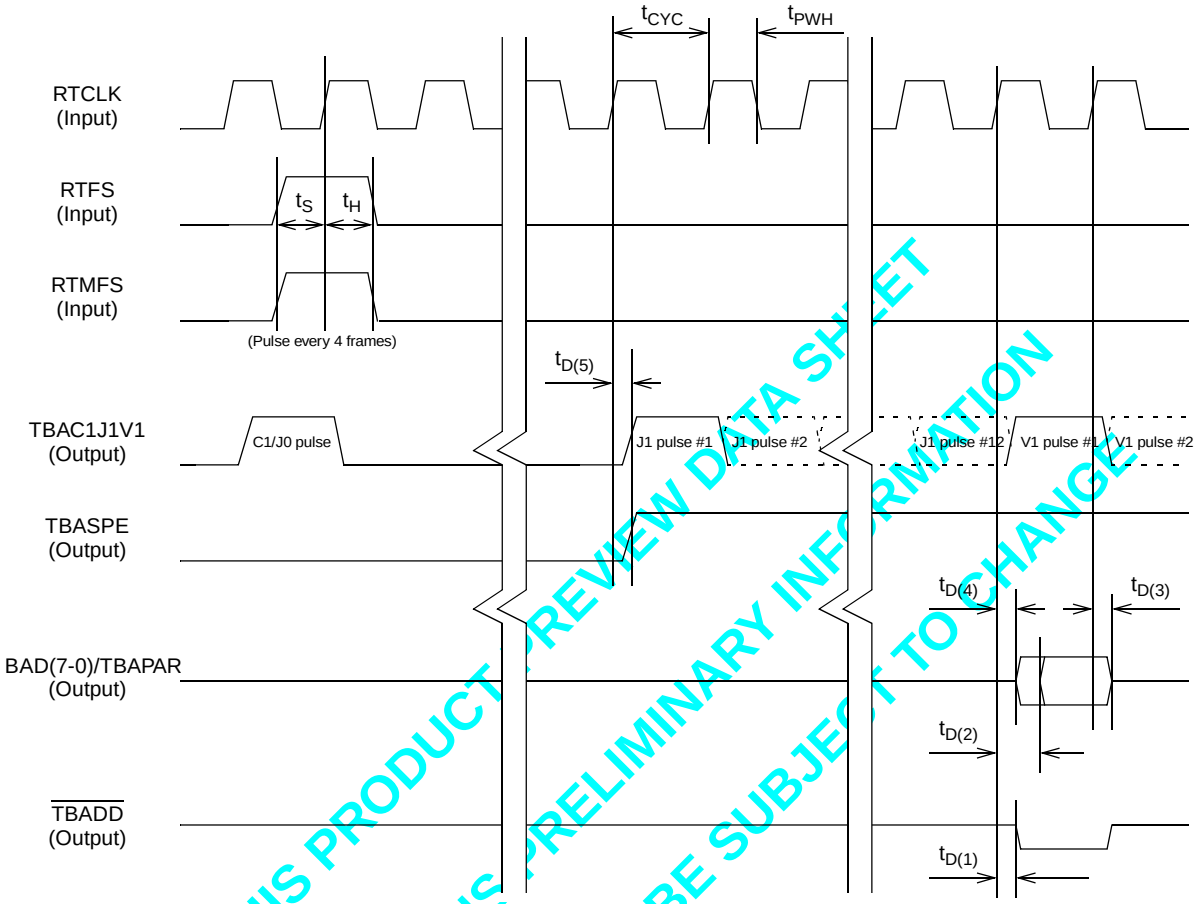
Parameter	Symbol	Min	Typ	Max	Unit
RTCLK clock period	t_{CYC}		12.86		ns
RTCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
TBAC1J1V1/ASPE setup time before RTCLK↓	t_S	3			ns
TBAC1J1V1/ASPE hold time after RTCLK↓	t_H	0			ns
$\overline{\text{TBADD}}$ add indicator delayed from RTCL	$t_{D(1)}$	1		6	ns
TBAD(7-0)/APAR out valid delay from RTCLK↑	$t_{D(2)}$	1		6	ns
TBAD(7-0)/APAR to tristate delay from RTCLK↑	$t_{D(3)}$	1		6	ns
TBAD(7-0)/APAR out tristate to driven delay from RTCLK↑	$t_{D(4)}$	1		6	ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The active RTCLK clock edge on which the data/parity signals are clocked out can be selected, see "Add Bus Interface" on page 177. The waveforms shown correspond to the positive clock edge selection.
3. The active RTCLK clock edge on which the timing signals are sampled can be selected, see "Add Bus Interface" on page 177. The waveforms shown correspond to the negative clock edge selection.
4. An additional delay of 0 up to 15 extra RTCLK clock cycles can be inserted between the Add bus timing and the Add bus data/parity signals, TBAC1J1V1 and TBASPE, see "Add Bus Interface" on page 177. The waveforms shown correspond to a delay of 0 clock cycles.

PRODUCT PREVIEW

Figure 9. ADD Bus Timing (Timing signals are outputs)



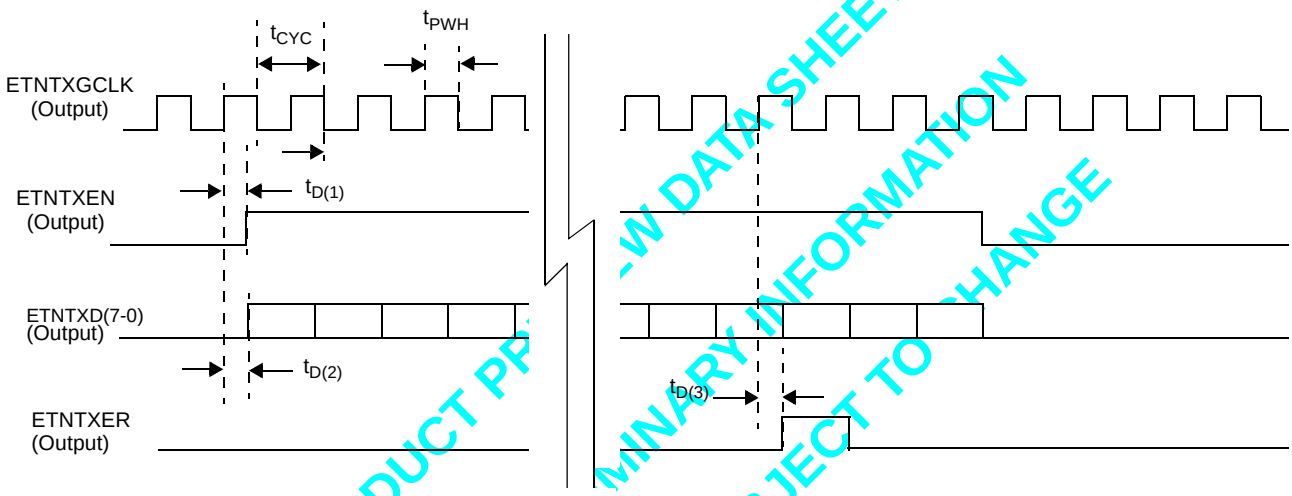
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
RTCLK clock period	t_{CYC}		12.86		ns
RTCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
RTFS/RTMFS setup time to RTCLK↑	t_S	3			ns
RTFS/RTMFS hold time after RTCLK↑	t_H	0			ns
$\overline{\text{TBADD}}$ add indicator delayed from RTCLK↑	$t_{D(1)}$	1		6	ns
TBAD(7-0)/TBAPAR out valid delay from RTCLK↑	$t_{D(2)}$	1		6	ns
TBAD(7-0)/TBAPAR to tristate delay from RTCLK↑	$t_{D(3)}$	1		6	ns
TBAD(7-0)/TBAPAR out tristate to driven delay from RTCLK↑	$t_{D(4)}$	1		6	ns
TBAC1J1V/TBASPE out valid delay from RTCLK↑	$t_{D(5)}$	1		6	ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The active RTCLK clock edge on which the data/parity and timing signals are clocked out can be selected, see "Add Bus Interface" on page 177. The waveforms shown correspond to the positive clock edge selection.
3. The active RTCLK clock edge on which the RTFS/RTMFS signals are sampled can be selected, see "Add Bus Interface" on page 177. The waveforms shown correspond to the positive clock edge selection.
4. An additional delay of 0 up to 15 extra RTCLK clock cycles can be inserted between the Add bus timing and the Add bus data/parity signals, TBAC1J1V1 and TBASPE, see "Add Bus Interface" on page 177. The waveforms shown correspond to a delay of 0 clock cycles.

Figure 10. Tx GMII Ethernet Interface

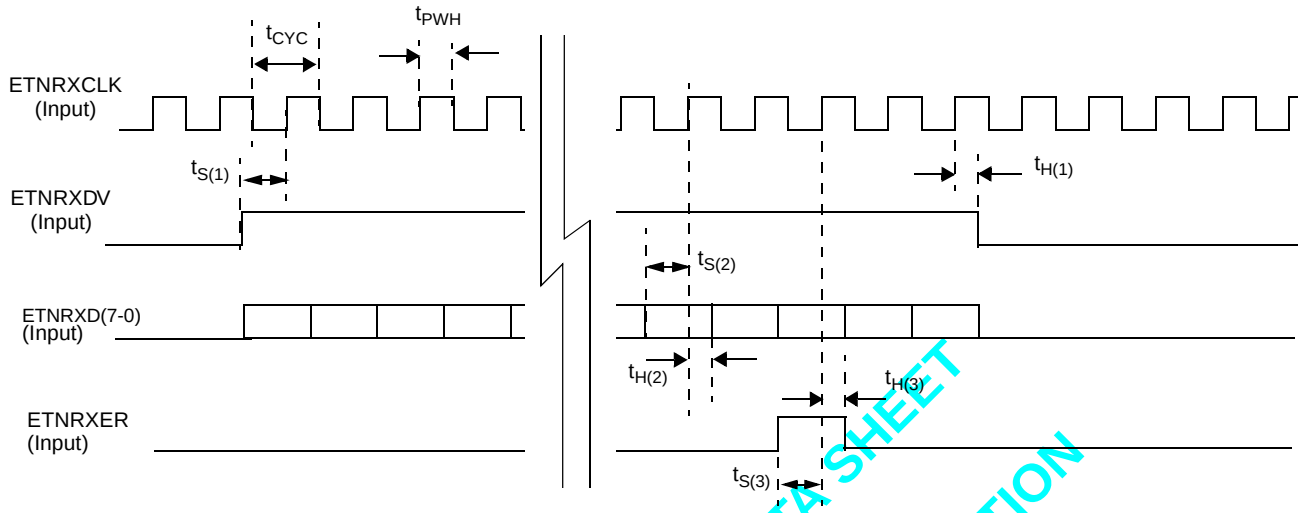


5 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
ETNTXGCLK clock period	t_{CYC}		8		ns
ETNTXGCLK duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	40		60	ns
ETNTXEN out valid delay from ETNTXGCLK↑	$t_{D(1)}$	1.5		4.5	ns
ETNTXD(7-0) out valid delay from ETNTXGCLK↑	$t_{D(2)}$	1.5		4.5	ns
ETNTXER out valid delay from ETNTXGCLK↑	$t_{D(3)}$	1.5		4.5	ns

PRODUCT PREVIEW

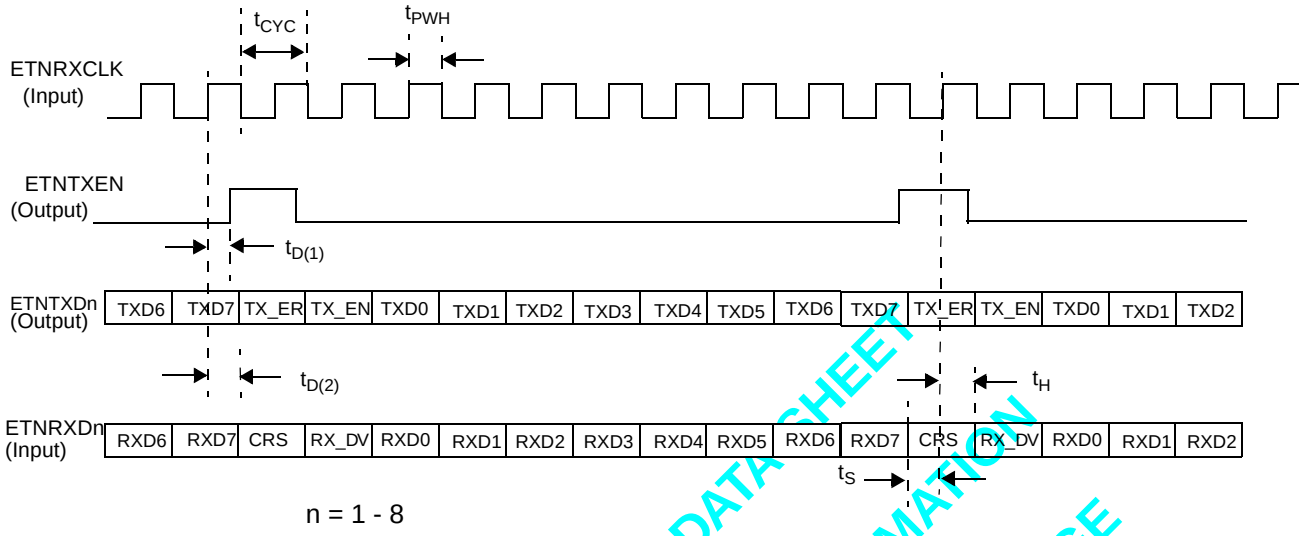
Figure 11. RX GMII Ethernet Interface



10 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
ETNRXCLK clock period	t_{CYC}		8		ns
ETNRXCLK duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	45		55	%
ETNRXDV setup time before ETNRXCLK↑	$t_{S(1)}$	2			ns
ETNRXDV hold time after ETNRXCLK↑	$t_{H(1)}$	0			ns
ETNRXD(7-0) setup time before ETNRXCLK↑	$t_{S(2)}$	2			ns
ETNRXD(7-0) hold time after ETNRXCLK↑	$t_{H(2)}$	0			ns
ETNRXER setup time before ETNRXCLK↑	$t_{S(3)}$	2			ns
ETNRXER hold time after ETNRXCLK↑	$t_{H(3)}$	0			ns

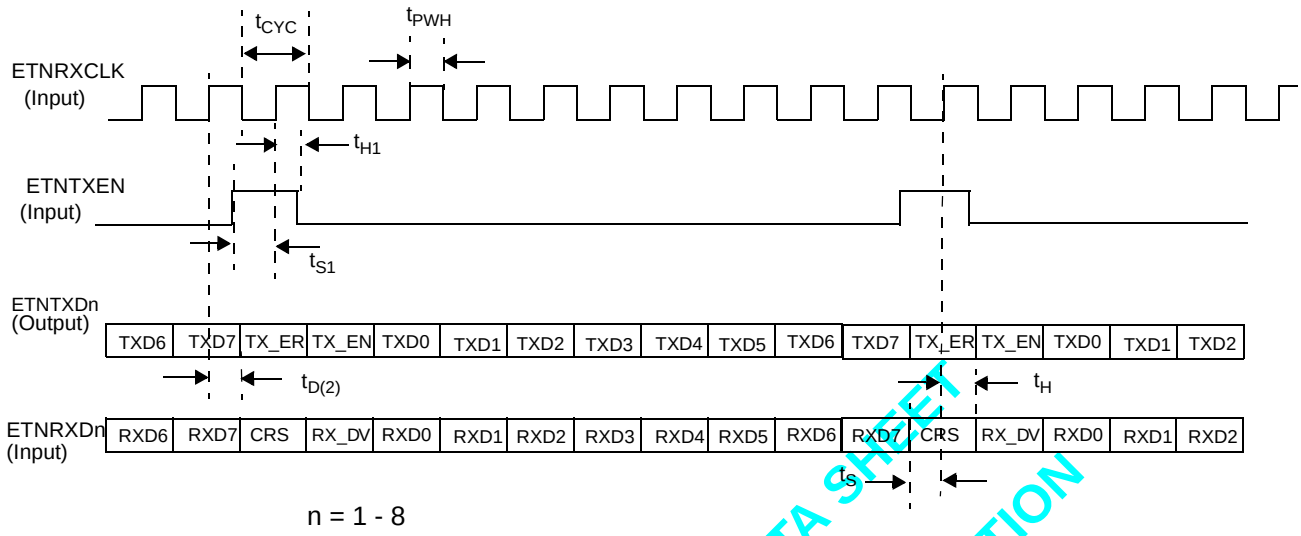
Figure 12. TX/Rx SMII Ethernet Interface (with SYNC as output)



10 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
ETNRXCLK clock period	t_{CYC}		8		ns
ETNRXCLK duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	40		60	%
ETNTXEN out valid delay from ETNRXCLK↑	$t_{D(1)}$	1.5		4.5	ns
ETNTXDn out valid delay from ETNRXCLK↑	$t_{D(2)}$	1.5		4.5	ns
ETNRXDn setup time before ETNRXCLK↑	t_S	1.5			ns
ETNRXDn hold time after ETNRXCLK↑	t_H	1			ns

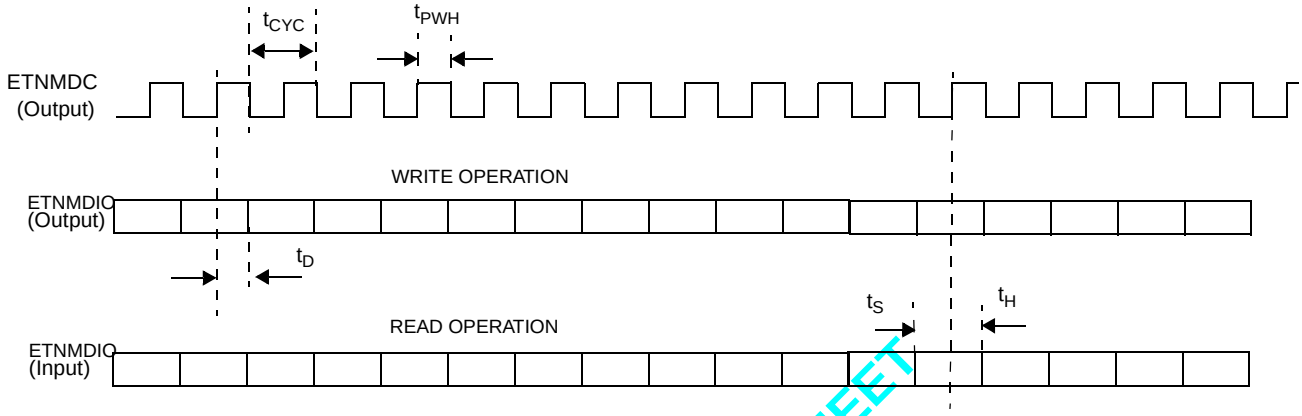
Figure 13. TX/Rx SMII Ethernet Interface (with SYNC as input)



10 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
ETNRXCLK clock period	t_{CYC}		8		ns
ETNRXCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
ETNTXEN setup time before ETNRXCLK ↑	t_{S1}	1.5			ns
ETNTXEN hold time after ETNRXCLK ↑	t_{H1}	1			
ETNTXDn out valid delay from ETNRXCLK ↑	$t_{D(2)}$	1.5		4.5	ns
ETNRXDn setup time before ETNRXCLK ↑	t_S	1.5			ns
ETNRXDn hold time after ETNRXCLK ↑	t_H	1			ns

Figure 14. Ethernet Management Interface

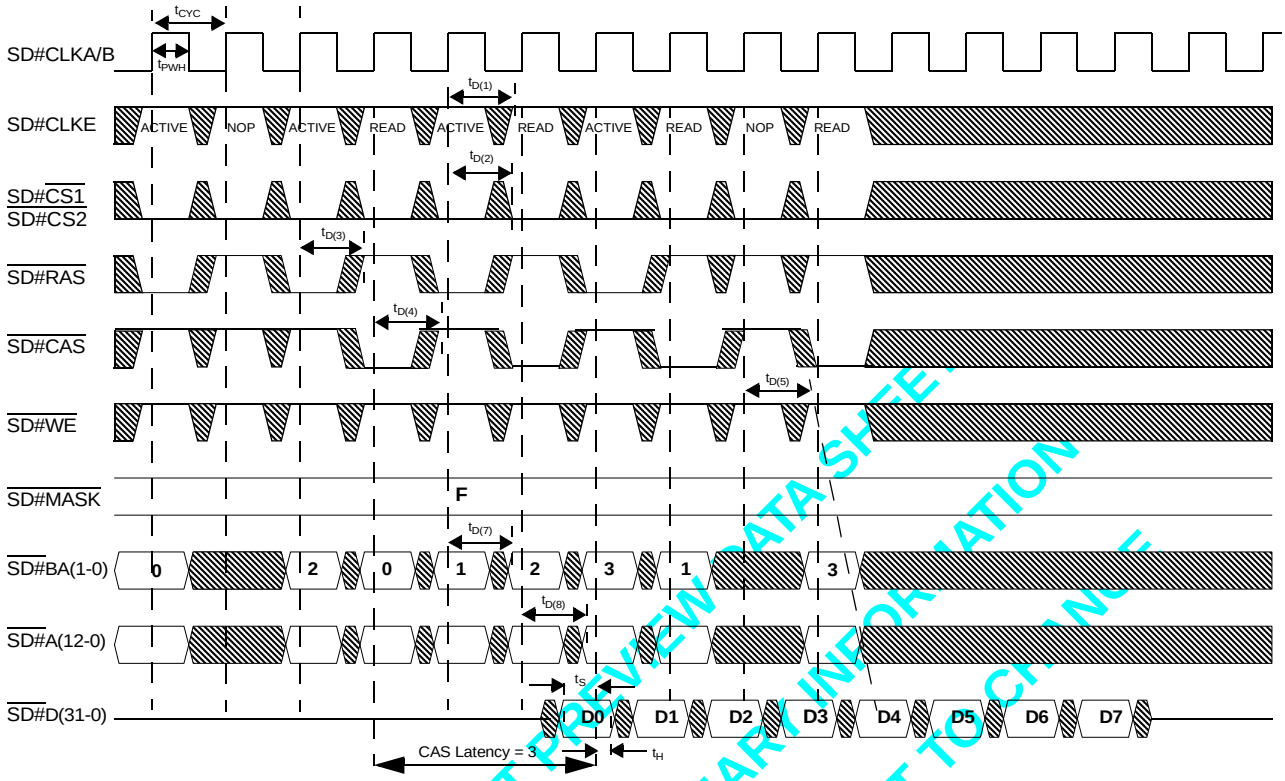


10 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
ETNMDC clock period	t_{CYC}		**TBD**		ns
ETNMDC duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	**TBD**		**TBD**	ns
ETNMDIO out valid delay from ETNMDC↑	t_D	15		30	ns
ETNMDIO setup time before ETNMDC↑	t_S	5			ns
ETNMDIO hold time after ETNMDC↑	t_H	5			ns

PRODUCT PREVIEW

Figure 15. SDRAM Interface - Single Word Read

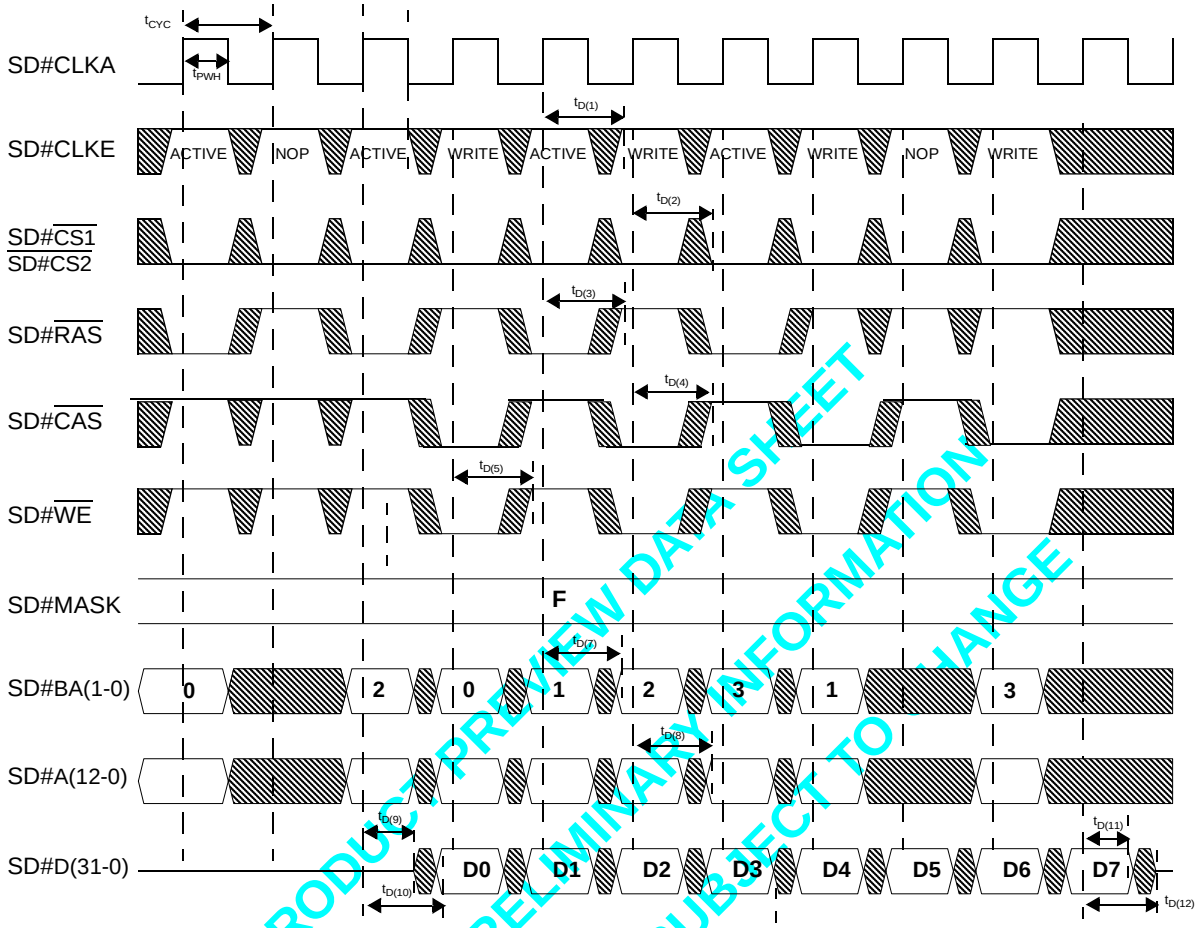


30 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
SD#CLKA/B clock period	t_{CYC}		8		ns
SD#CLKA/B duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	45		55	%
SD#CLKE valid delay from SD#CLK↑	$t_{D(1)}$	2		5	ns
SD#$\overline{CS}$ valid delay from SD#CLK↑	$t_{D(2)}$	2		5	ns
SD#$\overline{RAS}$ valid delay from SD#CLK↑	$t_{D(3)}$	2		5	ns
SD#$\overline{CAS}$ valid delay from SD#CLK↑	$t_{D(4)}$	2		5	ns
SD#$\overline{WE}$ valid delay from SD#CLK↑	$t_{D(5)}$	2		5	ns
SD#BA(1-0) valid delay from SD#CLK↑	$t_{D(7)}$	2		5	ns
SD#A(12-0) valid delay from SD#CLK↑	$t_{D(8)}$	2		5	ns
SD#D(31-0) setup time to SD#CLKB↑	t_S	1			ns
SD#D(31-0) hold time from SD#CLKB↑	t_H	1			ns

Note: # means 1 or 2 depending on the number of the SDRAM.

Figure 16. SDRAM Interface - Single Word Write



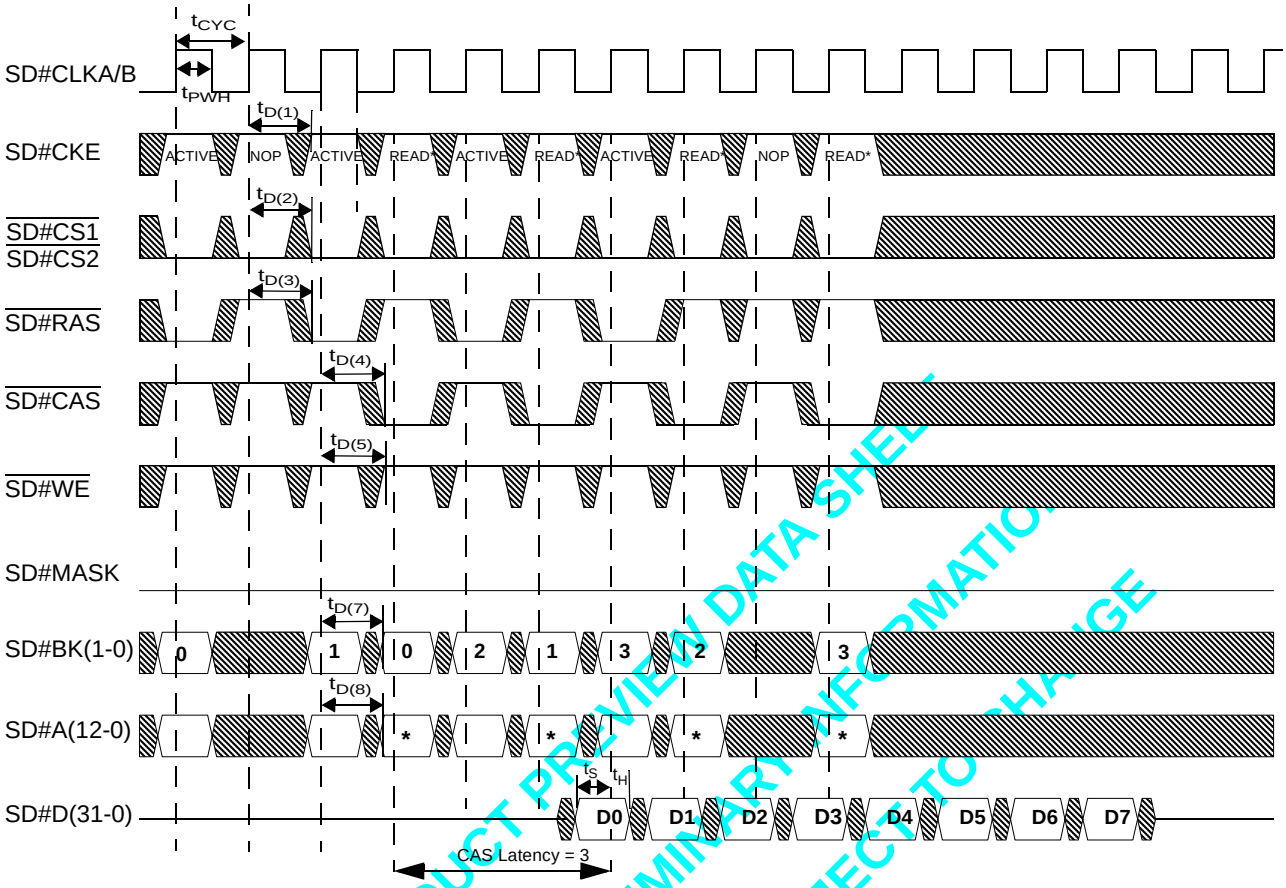
30 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
SD#CLKA clock period	t_{CYC}		8		ns
SD#CLKA duty cycle, t_{PWH}/t_{CYC}	t_{PWH}	45		55	%
SD#CLKE valid delay from SD#CLKA↑	$t_{D(1)}$	2		5	ns
SD#$\overline{CS}$ valid delay from SD#CLKA↑	$t_{D(2)}$	2		5	ns
SD#$\overline{RAS}$ valid delay from SD#CLKA↑	$t_{D(3)}$	2		5	ns
SD#$\overline{CAS}$ valid delay from SD#CLKA↑	$t_{D(4)}$	2		5	ns
SD#$\overline{WE}$ valid delay from SD#CLKA↑	$t_{D(5)}$	2		5	ns
SD#MASK valid delay from SD#CLKA↑	$t_{D(6)}$	2		5	ns
SD#BA(1-0) valid delay from SD#CLKA↑	$t_{D(7)}$	2		5	ns
SD#A(12-0) valid delay from SD#CLKA↑	$t_{D(8)}$	2		5	ns
SD#D(31-0) tristate to driven from SD#CLKA↑	$t_{D(9)}$	2		5	ns
SD#D(31-0) valid delay from SD#CLKA↑	$t_{D(10)}$	2		5	ns
SD#D(31-0) valid hold from SD#CLKA↑	$t_{D(11)}$	2		5	ns
SD#D(31-0) driven to tristate from SD#CLKA↑	$t_{D(12)}$	2		5	ns

Note:1 For burst accesses $t_{D(10)}$ and $t_{D(11)}$ apply as the delay parameters between successive data bytes.

PRODUCT PREVIEW

Figure 17. SDRAM Interface - Burst Read

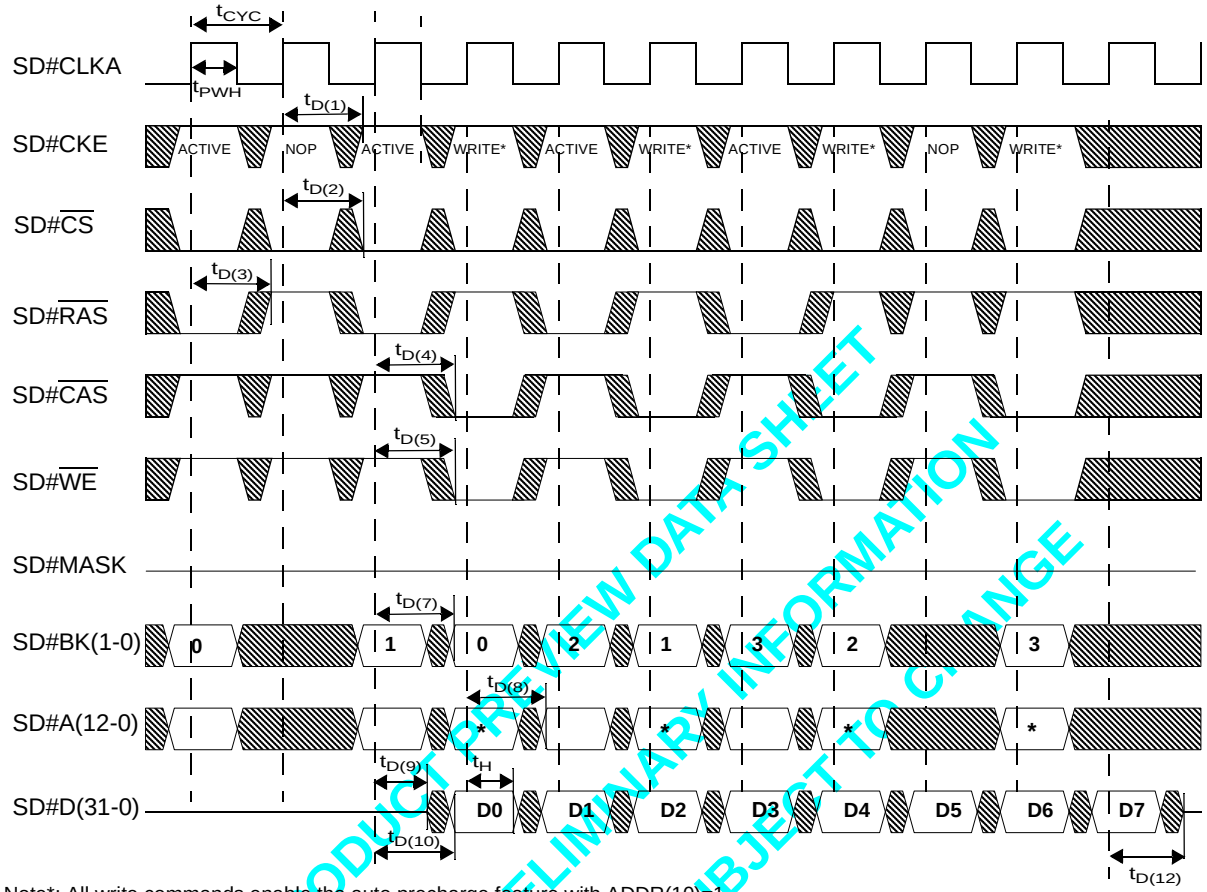


Note*: All read commands enable the auto precharge feature with ADDR(10)=1
means SDRAM 1 or SDRAM 2

30 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
SD#CLKA/B clock period	t_{CYC}		8		ns
SD#CLKA/B duty cycle, t_{PWH}/t_{CYC}		45		55	%
SD#CLKE valid delay from SD#CLKA↑	$t_{D(1)}$	2		5	ns
$\overline{\text{SD\#CS}}$ valid delay from SD#CLKA↑	$t_{D(2)}$	2		5	ns
$\overline{\text{SD\#RAS}}$ valid delay from SD#CLKA↑	$t_{D(3)}$	2		5	ns
$\overline{\text{SD\#CAS}}$ valid delay from SD#CLKA↑	$t_{D(4)}$	2		5	ns
$\overline{\text{SD\#WE}}$ valid delay from SD#CLKA↑	$t_{D(5)}$	2		5	ns
$\overline{\text{SD\#BA}}$(1-0) valid delay from SD#CLKA↑	$t_{D(7)}$	2		5	ns
$\overline{\text{SD\#A}}$(12-0) valid delay from SD#CLKA↑	$t_{D(8)}$	2		5	ns
$\overline{\text{SD\#D}}$(31-0) setup time to SD#CLKB↑	t_S	1			ns
$\overline{\text{SD\#D}}$(31-0) hold time from SD#CLKB↑	t_H	1			ns

Figure 18. SDRAM Interface - Burst Write



Note*: All write commands enable the auto precharge feature with ADDR(10)=1
means SDRAM1 and SDRAM2

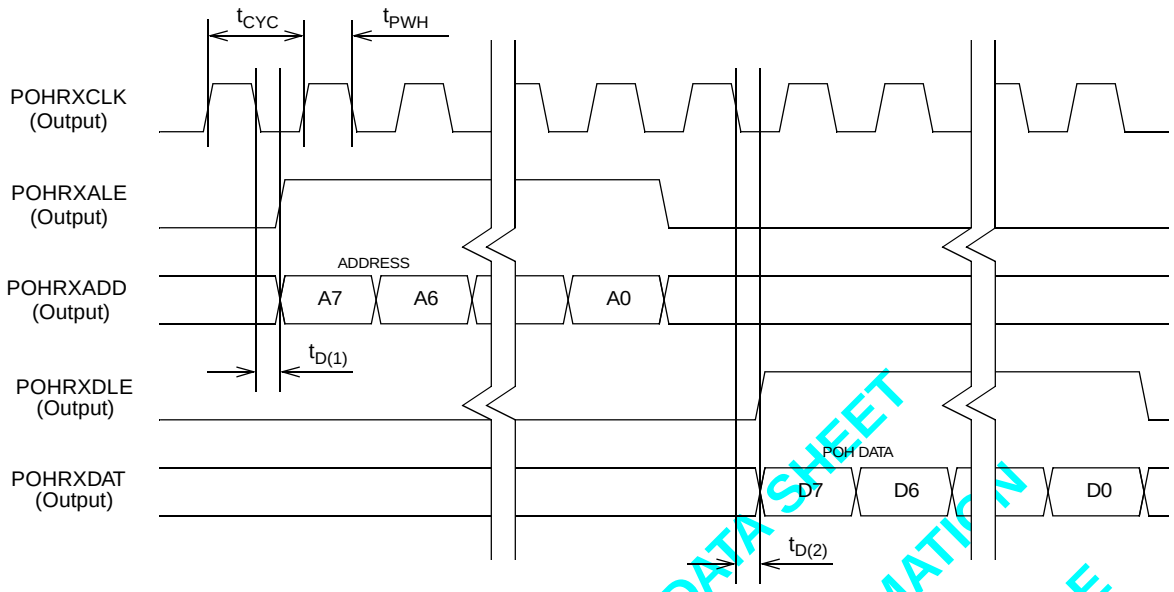
30 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
SD#CLKA clock period	t_{CYC}		8		ns
SD#CLKA duty cycle, t_{PWH}/t_{CYC}		45		55	%
SD#CLKE valid delay from SD#CLKA↑	$t_{D(1)}$	2		5	ns
SD#$\overline{CS}$ valid delay from SD#CLKA↑	$t_{D(2)}$	2		5	ns
SD#$\overline{RAS}$ valid delay from SD#CLKA↑	$t_{D(3)}$	2		5	ns
SD#$\overline{CAS}$ valid delay from SD#CLKA↑	$t_{D(4)}$	2		5	ns
SD#$\overline{WE}$ valid delay from SD#CLKA↑	$t_{D(5)}$	2		5	ns
SD#BA(1-0) valid delay from SD#CLKA↑	$t_{D(7)}$	2		5	ns
SD#A(12-0) valid delay from SD#CLKA↑	$t_{D(8)}$	2		5	ns
SD#D(31-0) tristate to driven from SD#CLKA↑	$t_{D(9)}$	2		5	ns
SD#D(31-0) valid delay from SD#CLKA↑	$t_{D(10)}$	2		5	ns
SD#D(31-0) valid hold from SD#CLKA↑	t_H	2		5	ns
SD#D(31-0) driven to tristate from SD#CLKA↑	$t_{D(12)}$	2		5	ns

Note: For burst accesses $t_{D(10)}$ and t_H apply as the delay and hold parameters between successive data bytes.

PRODUCT PREVIEW

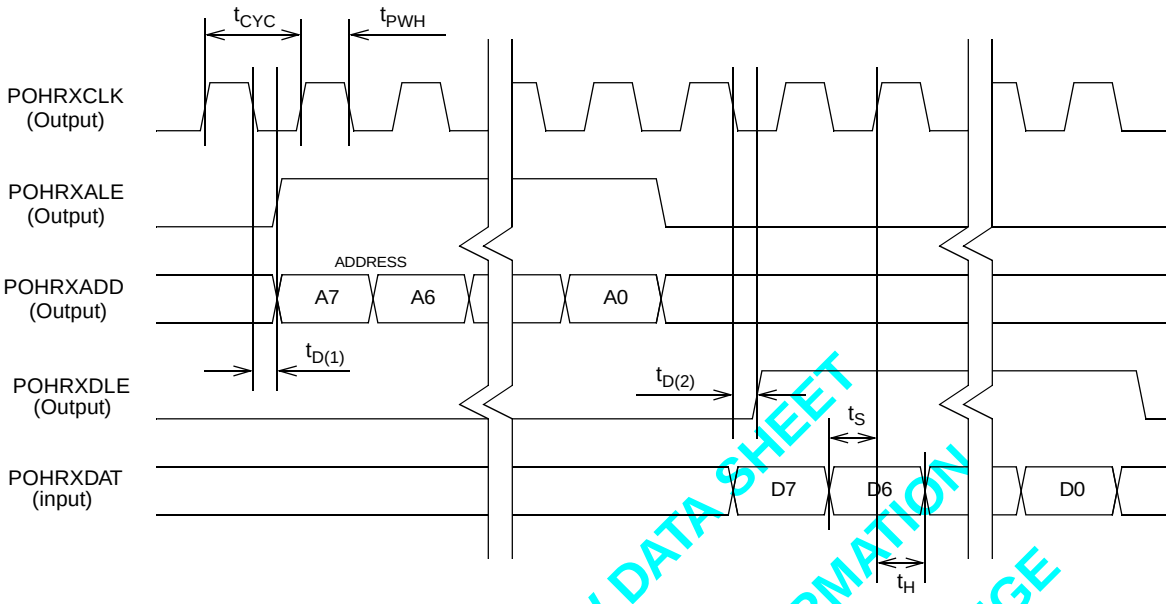
Figure 19. RX High Order POH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHRXCLK clock period	t_{CYC}		12.86		ns
POHRXCLK clock pulse width	t_{PWH}	40	50	60	%t_{CYC}
POHRXALE/POHRXADD out valid delay from POHRXCLK↓	$t_{D(1)}$	1		4	ns
POHRXDLE/POHRXDAT out valid delay from POHRXCLK↓	$t_{D(2)}$	1		4	ns

Figure 20. TX High Order POH Byte Interface

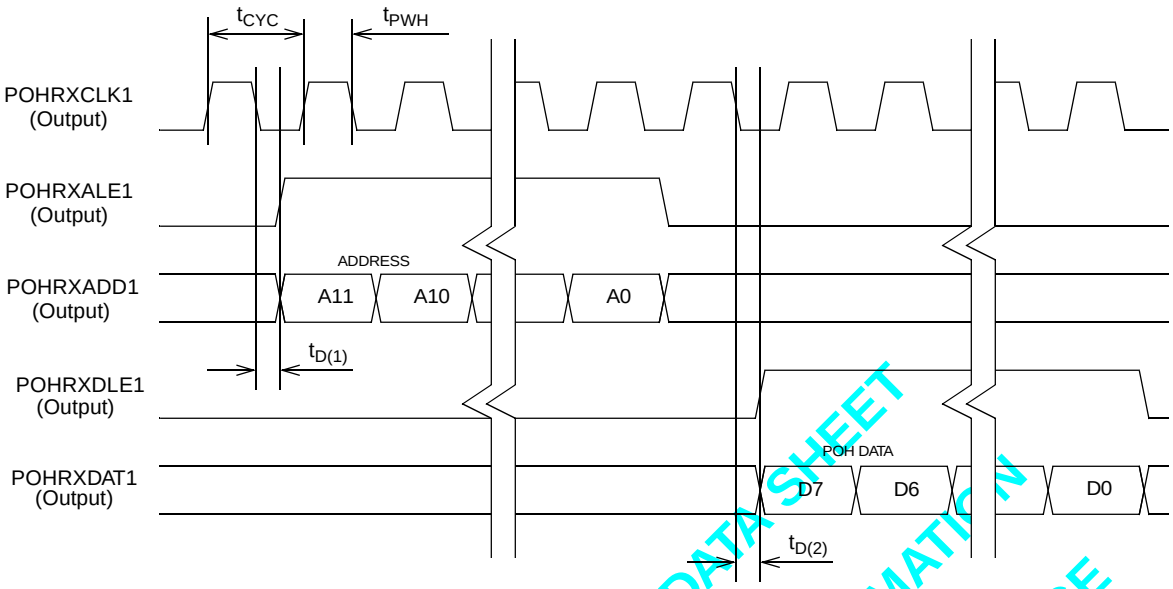


50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHTXCLK clock period	t_{CYC}		12.86		ns
POHTXCLK clock pulse width		40	50	60	$\%t_{CYC}$
POHTXALE/POHTXADD out valid delay from POHTXCLK↓	$t_{D(1)}$	1		4	ns
POHTXDLE out valid delay from POHTXCLK↓	$t_{D(2)}$	1		4	ns
POHTXDAT setup time before POHTXCLK↑	t_S	3			ns
POHTXDAT hold time after POHTXCLK↑	t_H	0			ns

PRODUCT PREVIEW

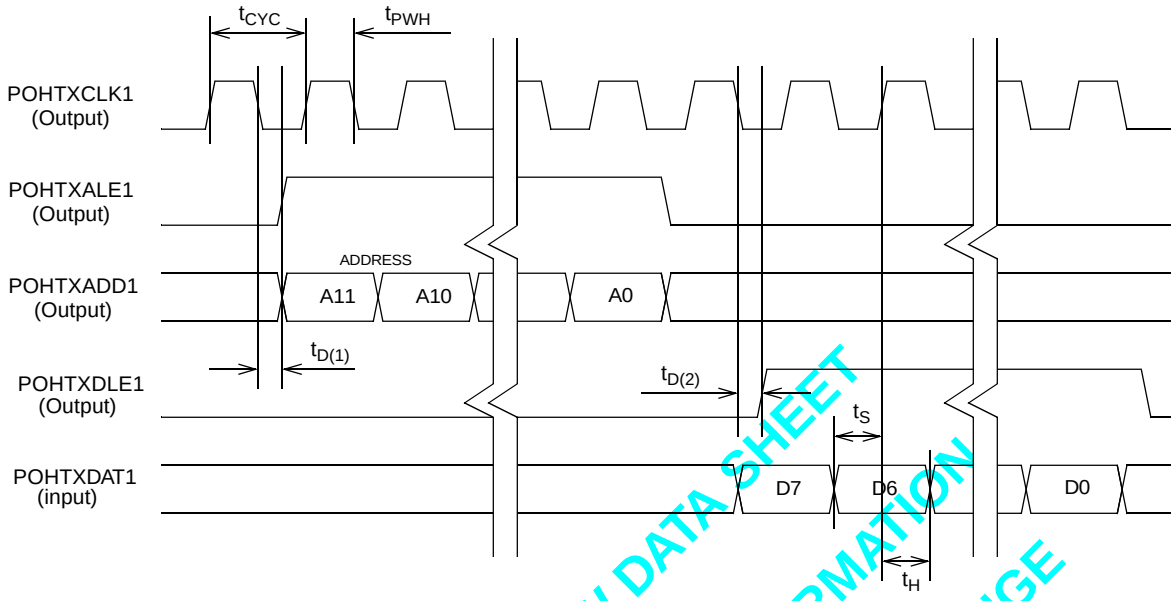
Figure 21. RX Low Order POH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHRXCLK1 clock period	t_{CYC}		12.86		ns
POHRXCLK1 clock pulse width	t_{PWH}	40	50	60	%t_{CYC}
POHRXALE1/POHRXADD1 out valid delay from POHRXCLK1↓	$t_{D(1)}$	1		4	ns
POHRXDLE1/POHRXDAT1 out valid delay from POHRXCLK1↓	$t_{D(2)}$	1		4	ns

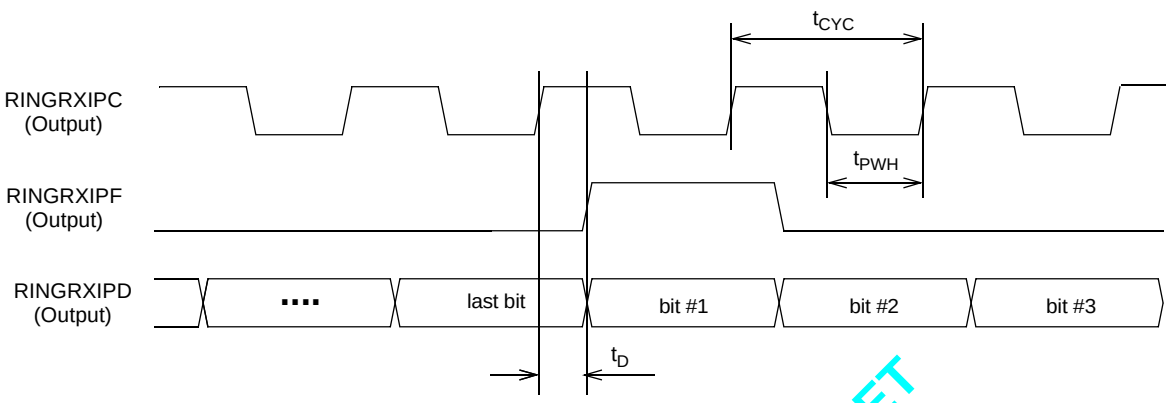
Figure 22. TX Low Order POH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHTXCLK1 clock period	t_{CYC}		12.86		ns
POHTXCLK1 clock pulse width		40	50	60	%t_{CYC}
POHTXALE1/POHTXADD1 out valid delay from POHTXCLK1↓	$t_{D(1)}$	1		4	ns
POHTXDLE1 out valid delay from POHTXCLK1↓	$t_{D(2)}$	1		4	ns
POHTXDAT1 setup time before POHTXCLK1↑	t_S	3			ns
POHTXDAT1 hold time after POHTXCLK1↑	t_H	0			ns

Figure 23. RX High Order Alarm Indication Port Interface



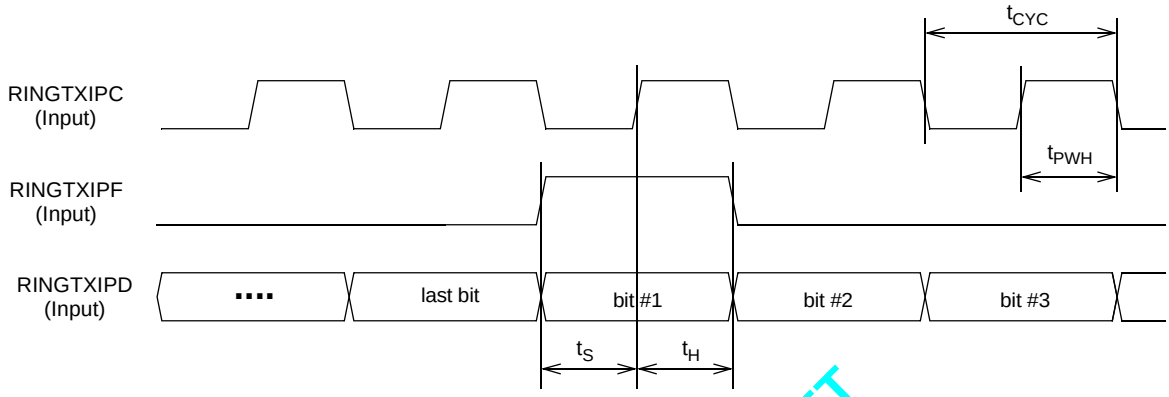
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
RINGRXIPC clock period	t_{CYC}		51.44		ns
RINGRXIPC clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
RINGRXIPF/RINGRXIPD out valid delay from RINGRXIPC↓	t_D	1		6	ns

Notes:

1. All the output signals are synchronous of the rising edge of internal clock SYSCLK(RTCLK=77.76MHz).
2. The minimum value of T_D (1 ns) is maintained because the data and framing pulse are placed on the output when the rising edge of the RINGRXIPC is placed on the output. The maximum value of T_D is maintained also.

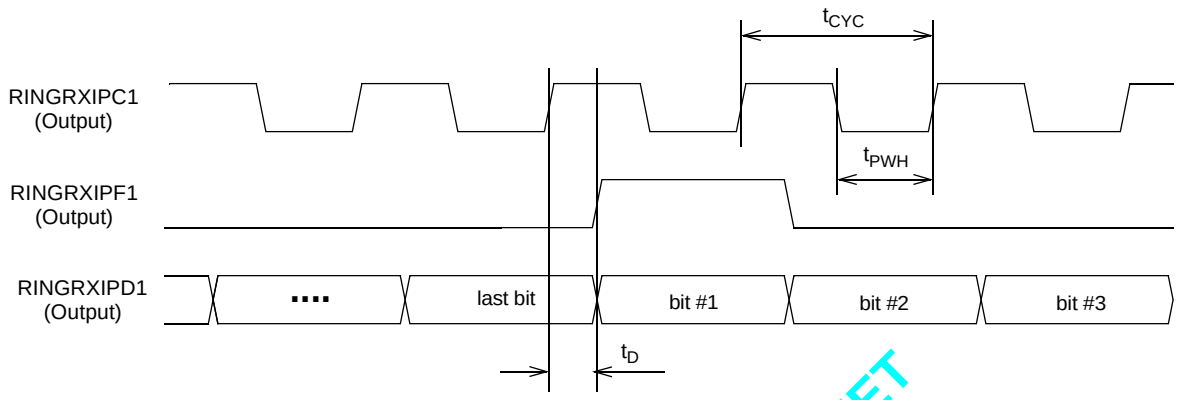
Figure 24. TX High Order Alarm Indication Port Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
RINGTXIPC clock period	t_{CYC}		51.44		ns
RINGTXIPC clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
RINGTXIPF/RINGTXIPD setup time before RINGTXIPC↑	t_S	30			ns
RINGTXIPF/RINGTXIPD hold time after RINGTXIPC↑	t_H	0			ns

Figure 25. RX Low Order Alarm Indication Port Interface



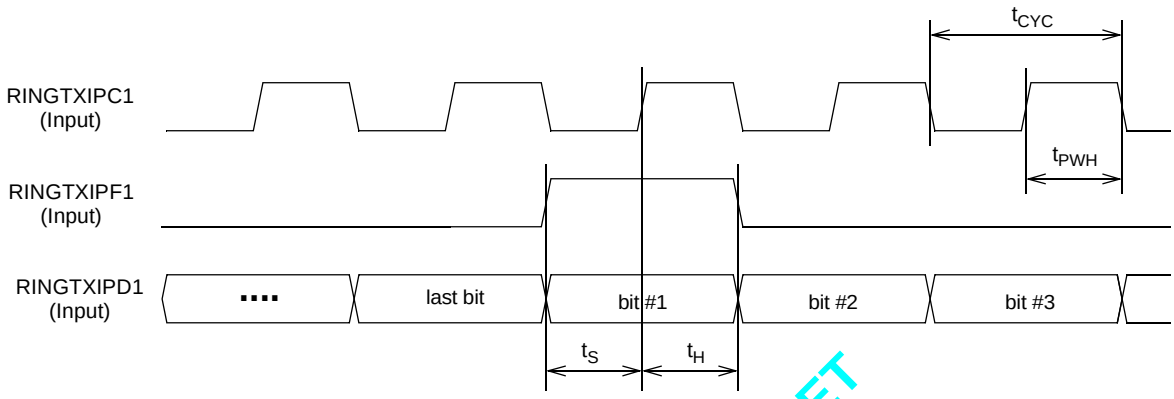
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
RINGRXIPC1 clock period	t_{CYC}		51.44		ns
RINGRXIPC1 clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
RINGRXIPF/RINGRXIPD out valid delay from RINGRXIPC1↓	t_D	1		6	ns

Notes:

1. All the output signals are synchronous of the rising edge of internal clock SYSCLK(RTCLK=77.76MHz).
2. The minimum value of T_D (1 ns) is maintained because the data and framing pulse are placed on the output when the rising edge of the RINGRXIPC1 is placed on the output. The maximum value of T_D is maintained also.

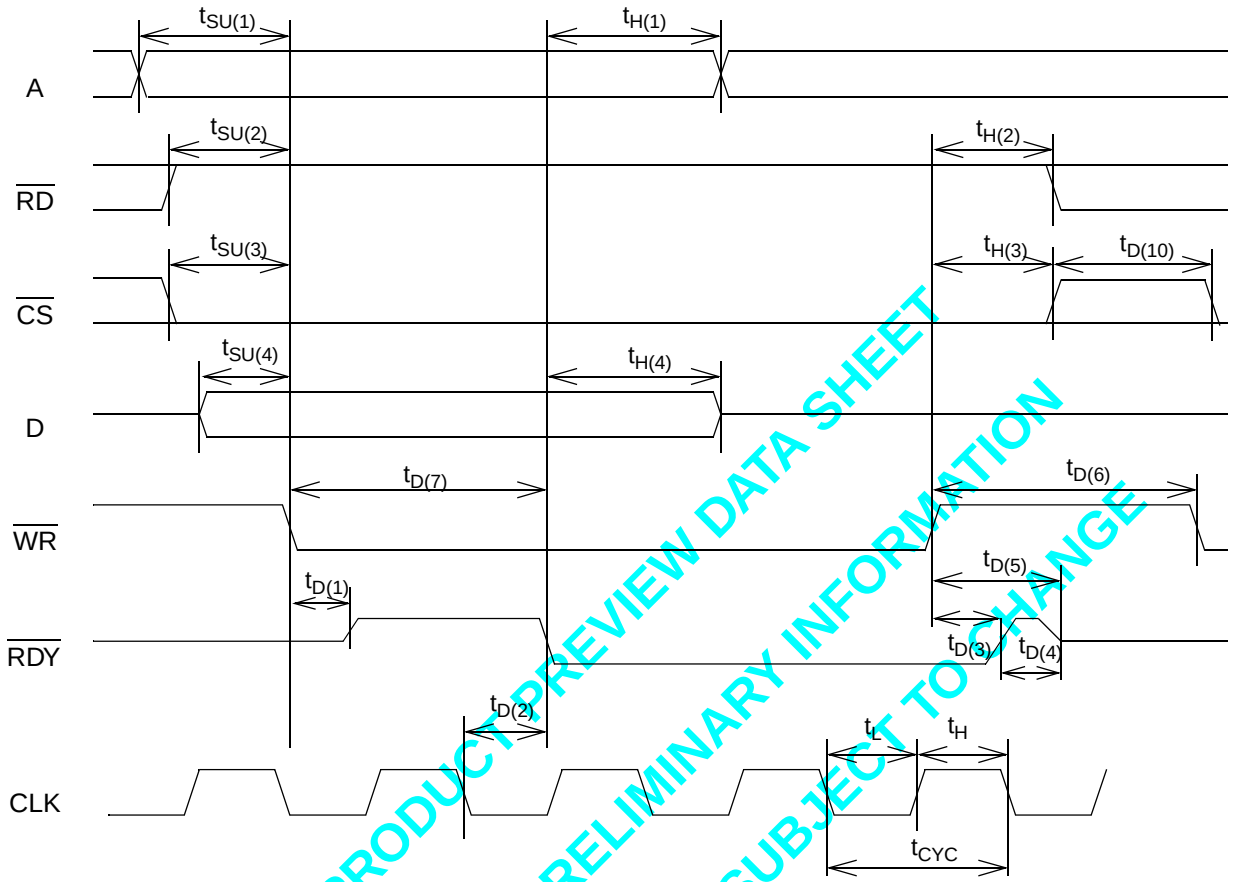
Figure 26. TX Low Order Alarm Indication Port Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
RINGTXIPC1 clock period	t_{CYC}		51.44		ns
RINGTXIPC1 clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
RINGTXIPF1/RINGTXIPD1 setup time before RINGTXIPC1↑	t_S	30			ns
RINGTXIPF1/RINGTXIPD1 hold time after RINGTXIPC1↑	t_H	0			ns

Figure 27. Microprocessor Interface: Generic Intel Mode Write Cycle[1]



1. See the Lead Description table on GENERIC INTEL - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
A setup time before $\overline{WR}\downarrow$	$t_{SU(1)}$	-0.9*t_{CYC}		-	
$\overline{RD}$ setup time before $\overline{WR}\downarrow$	$t_{SU(2)}$ [a]	0		-	ns
$\overline{CS}$ setup time before $\overline{WR}\downarrow$	$t_{SU(3)}$ [b]	0		-	ns
D setup time before $\overline{WR}\downarrow$	$t_{SU(4)}$	-0.9*t_{CYC}		-	
Hold time of A to active edge $\overline{RDY}$	$t_{H(1)}$	0		-	ns
$\overline{RD}$ hold time after $\overline{WR}\uparrow$	t_{H2} [c]	t_{CYC}		-	
$\overline{CS}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$ [b, d]	-		-	
Hold time of D to active edge $\overline{RDY}$	$t_{H(4)}$	0		-	ns
Delay from $\overline{WR}\downarrow$ to $\overline{RDY}$ driving	$t_{D(1)}$	0		20	ns
Delay from CLK$\downarrow$ to active edge $\overline{RDY}$	$t_{D(2)}$	0		8	ns
Delay from $\overline{WR}\uparrow$ to inactive edge $\overline{RDY}$	$t_{D(3)}$	0		7	ns
Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate	$t_{D(4)}$	5		-	ns
Delay from $\overline{WR}\uparrow$ to $\overline{RDY}$ going in tristate	$t_{D(5)}$	-		20	ns
$\overline{WR}$ inactive pulse width	$t_{D(6)}$	t_{CYC}		-	
Response latency	$t_{D(7)}$	TBD		TBD	
$\overline{CS}$ inactive pulse width	$t_{D(10)}$ [e]	t_{CYC}		-	

a. Only applies if a write access is preceded by a read access.

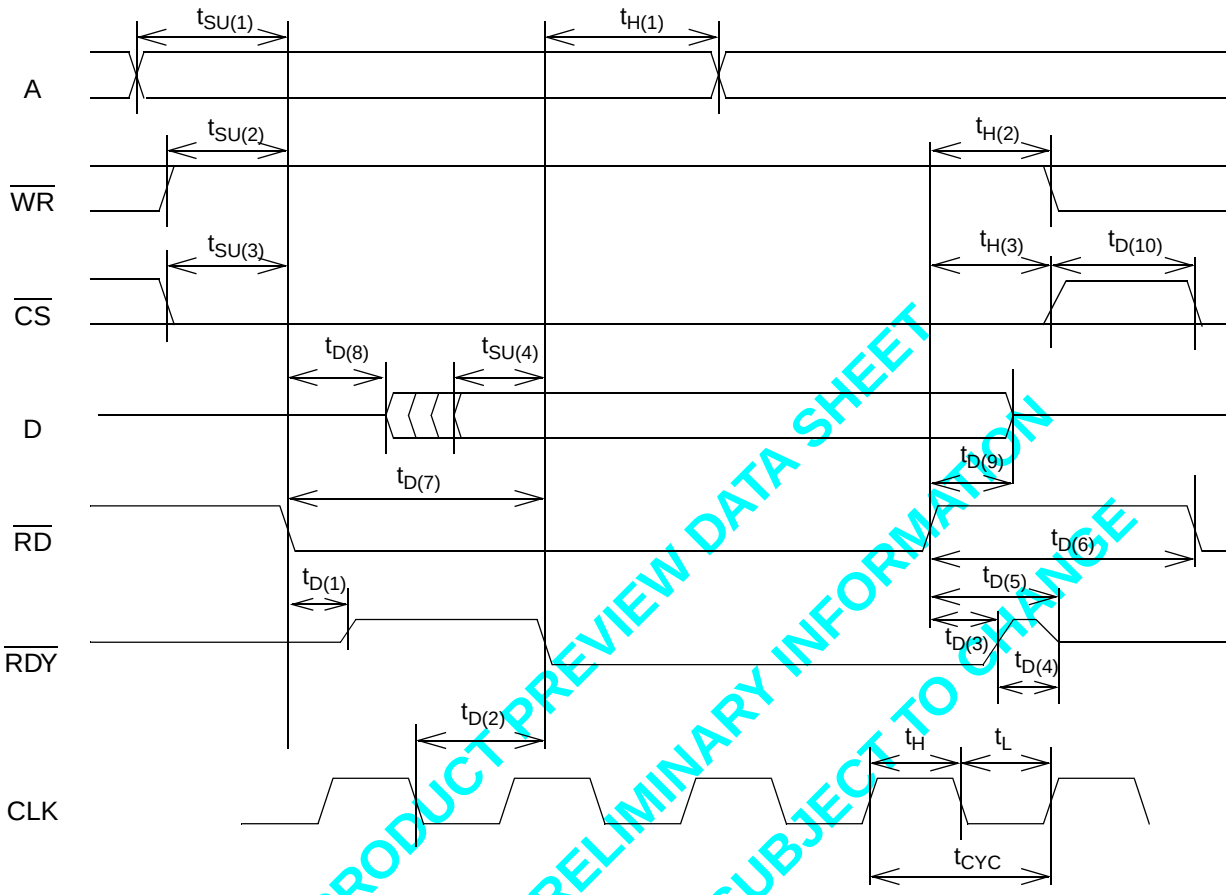
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.

c. Only applies if a write access is followed by a read access.

d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{WR}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.

e. Between accesses to different peripherals.

Figure 28. Microprocessor Interface: Generic Intel Mode Read Cycle[1]



1. See the Lead Description table on GENERIC INTEL - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
A setup time before $\overline{RD}\downarrow$	$t_{SU(1)}$	-0.9*t_{CYC}		-	
$\overline{WR}$ setup time before $\overline{RD}\downarrow$	$t_{SU(2)}$ [a]	0		-	ns
$\overline{CS}$ setup time before $\overline{RD}\downarrow$	$t_{SU(3)}$ [b]	0		-	ns
D setup time before $\overline{RDY}$	$t_{SU(4)}$	0.7*t_{CYC}		-	
A hold time after active edge $\overline{RDY}$	$t_{H(1)}$	0		-	ns
$\overline{WR}$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$ [c]	t_{CYC}		-	
$\overline{CS}$ hold time after $\overline{RD}\uparrow$	$t_{H(3)}$ [b, d]	-		-	
Delay from $\overline{RD}\downarrow$ to $\overline{RDY}$ driving	$t_{D(1)}$	0		20	ns
Delay from CLK$\downarrow$ to active edge $\overline{RDY}$	$t_{D(2)}$	0		8	ns
Delay from $\overline{RD}\uparrow$ to inactive edge $\overline{RDY}$	$t_{D(3)}$	0		7	ns
Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate	$t_{D(4)}$	5		-	ns
Delay from $\overline{RD}\uparrow$ to $\overline{RDY}$ going in tristate	$t_{D(5)}$	-		20	ns
$\overline{RD}$ inactive pulse width	$t_{D(6)}$	t_{CYC}		-	
Response latency	$t_{D(7)}$	TBD		TBD	
Delay from $\overline{RD}\downarrow$ to D driving	$t_{D(8)}$	0		12	ns
Delay from $\overline{RD}\uparrow$ to D going in tristate	$t_{D(9)}$	0		12	ns
$\overline{CS}$ inactive pulse width	$t_{D(10)}$ [e]	t_{CYC}		-	

a. Only applies if a read access is preceded by a write access.

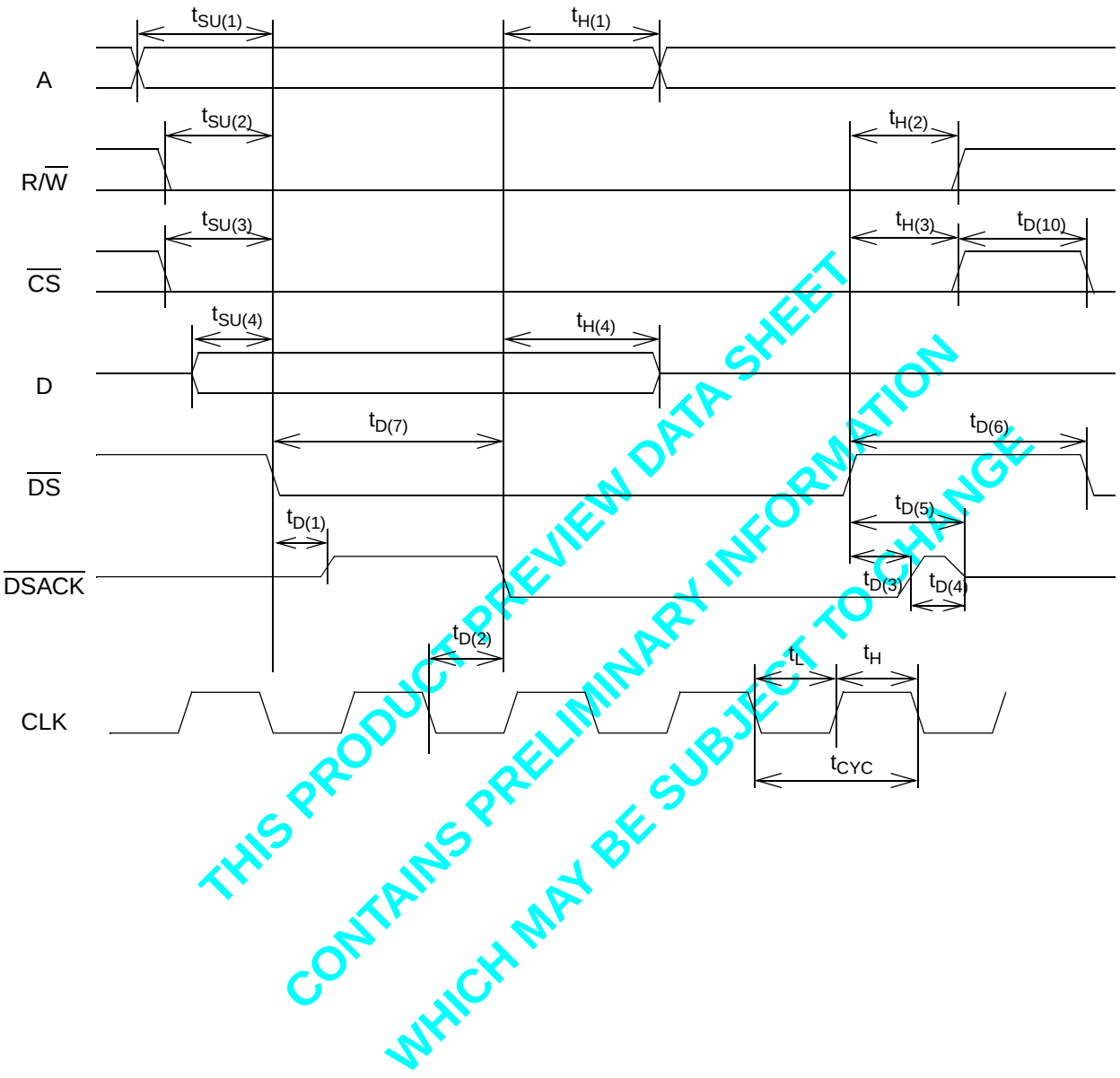
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.

c. Only applies if a read access is followed by a write access.

d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{RD}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.

e. Between accesses to different peripherals

Figure 29. Microprocessor Interface: Generic Motorola Mode Write Cycle[1]



1. See the Lead Description table on GENERIC MOTOROLA - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	$0.4*t_{CYC}$		-	
CLK clock high phase pulse width	t_H	$0.4*t_{CYC}$		-	
A setup time before $\overline{DS}\downarrow$	$t_{SU(1)}$	$-0.9*t_{CYC}$		-	
R/$\overline{W}$ setup time before $\overline{DS}\downarrow$	$t_{SU(2)}$ [a]	0		-	ns
$\overline{CS}$ setup time before $\overline{DS}\downarrow$	$t_{SU(3)}$ [b]	0		-	ns
D setup time before $\overline{DS}\downarrow$	$t_{SU(4)}$	$-0.9*t_{CYC}$		-	
A hold time after $\overline{DSACK}$	$t_{H(1)}$	0		-	ns
R/$\overline{W}$ hold time after $\overline{DS}\uparrow$	$t_{H(2)}$ [c]	0		-	ns
$\overline{CS}$ hold time after $\overline{DS}\uparrow$	$t_{H(3)}$ [b, d]	-		-	
D hold time after active edge $\overline{DSACK}$	$t_{H(4)}$	0		-	ns
Delay from $\overline{DS}\downarrow$ to $\overline{DSACK}$ driving	$t_{D(1)}$	0		20	ns
Delay from CLK$\downarrow$ to active edge $\overline{DSACK}$	$t_{D(2)}$	0		8	ns
Delay from $\overline{DS}\uparrow$ to inactive edge $\overline{DSACK}$	$t_{D(3)}$	0		7	ns
Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate	$t_{D(4)}$	5		-	ns
Delay from $\overline{DS}\uparrow$ to $\overline{DSACK}$ going in tristate	$t_{D(5)}$	-		20	ns
$\overline{DS}$ inactive pulse width	$t_{D(6)}$	t_{CYC}		-	
Response latency	$t_{D(7)}$	TBD		TBD	
$\overline{CS}$ inactive pulse width	$t_{D(10)}$ [e]	t_{CYC}		-	

a. Only applies if a write access is preceded by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.

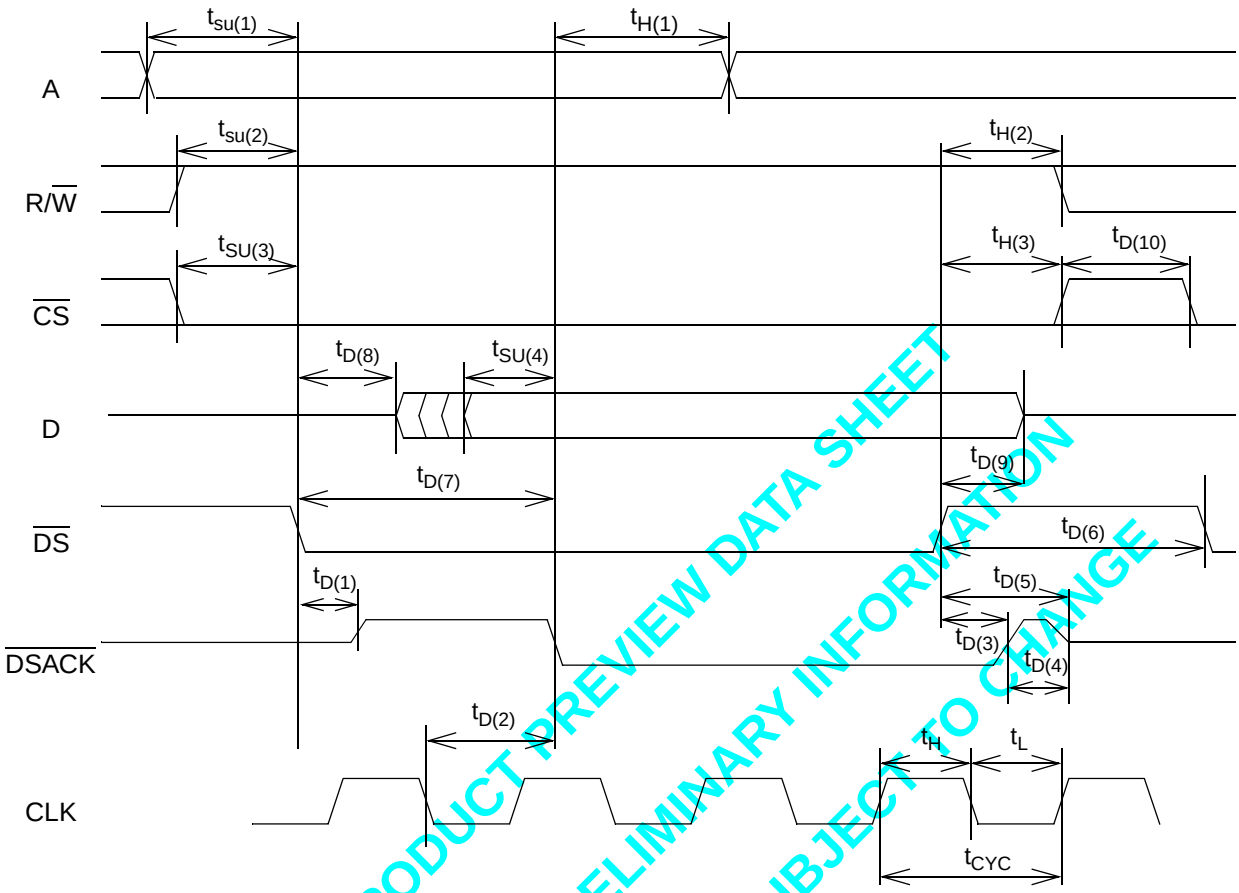
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.

c. Only applies if a write access is followed by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.

d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.

e. Between accesses to different peripherals

Figure 30. Microprocessor Interface: Generic Motorola Mode Read Cycle[1]



1. See the Lead Description table on GENERIC MOTOROLA - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
A setup time before $\overline{DS}\downarrow$	$t_{SU(1)}$	-0.9*t_{CYC}		-	
R/$\overline{W}$ setup time before $\overline{DS}\downarrow$	$t_{SU(2)}$ [a]	0		-	ns
$\overline{CS}$ setup time before $\overline{DS}\downarrow$	$t_{SU(3)}$ [b]	0		-	ns
D setup time to active edge $\overline{DSACK}$	$t_{SU(4)}$	0.7*t_{CYC}		-	
A hold time to active edge $\overline{DSACK}$	$t_{H(1)}$	0		-	ns
R/$\overline{W}$ hold time after $\overline{DS}\uparrow$	$t_{H(2)}$ [c]	0		-	ns
$\overline{CS}$ hold time after $\overline{DS}\uparrow$	$t_{H(3)}$ [b, d]	-		-	
Delay from $\overline{DS}\downarrow$ to $\overline{DSACK}$ driving	$t_{D(1)}$	0		20	ns
Delay from CLK$\downarrow$ to active edge $\overline{DSACK}$	$t_{D(2)}$	0		8	ns
Delay from $\overline{DS}\uparrow$ to inactive edge $\overline{DSACK}$	$t_{D(3)}$	0		7	ns
Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate	$t_{D(4)}$	5		-	
Delay from $\overline{DS}\uparrow$ to $\overline{DSACK}$ going in tristate	$t_{D(5)}$	-		20	ns
$\overline{DS}$ inactive pulse width	$t_{D(6)}$	t_{CYC}		-	
Response latency	$t_{D(7)}$	TBD		TBD	
Delay from $\overline{DS}\downarrow$ to D driving	$t_{D(8)}$	0		12	ns
Delay from $\overline{DS}\uparrow$ to D going in tristate	$t_{D(9)}$	0		12	ns
$\overline{CS}$ inactive pulse width	$t_{D(10)}$ [e]	t_{CYC}		-	

a. Only applies if a read access is preceded by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.

b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.

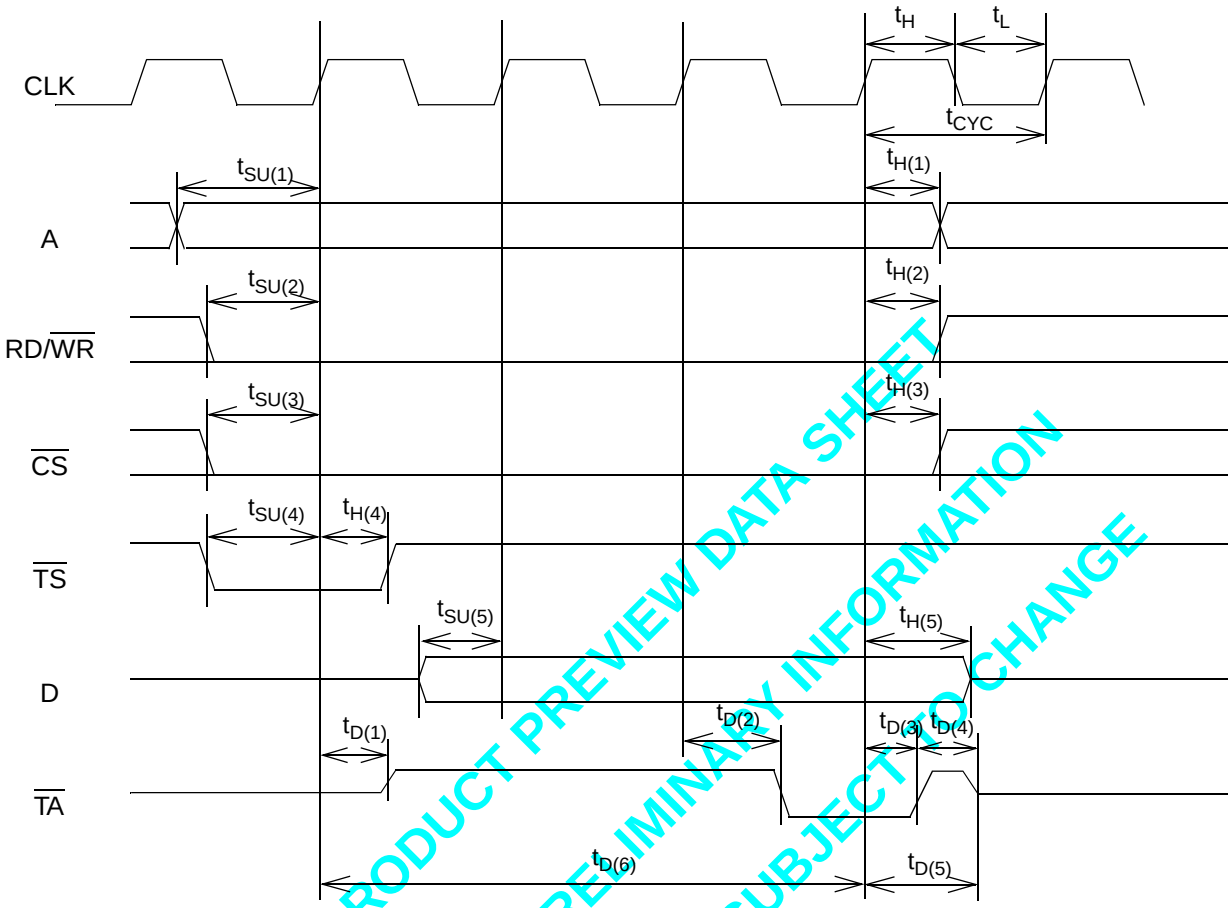
c. Only applies if a read access is followed by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.

d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.

e. Between accesses to different peripherals

PRODUCT PREVIEW

Figure 31. Microprocessor Interface: Motorola MPC860 Mode Write Cycle[1]



1. See the Lead Description table on MOTOROLA MPC860 - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
A setup time before CLK↑	$t_{SU(1)}$ [a]	0		-	ns
RD/$\overline{WR}$ setup time before CLK↑	$t_{SU(2)}$ [a, b]	0		-	ns
$\overline{CS}$ setup time before CLK↑	$t_{SU(3)}$ [a, c]	6		-	ns
$\overline{TS}$↓ setup time before CLK↑	$t_{SU(4)}$	6		-	ns
D setup time before CLK↑	$t_{SU(5)}$ [d]	0		-	ns
A hold time after CLK↑	$t_{H(1)}$ [e]	0		-	ns
RD/$\overline{WR}$ hold time after CLK↑	$t_{H(2)}$ [e, f]	0		-	ns
$\overline{CS}$ hold time after CLK↑	$t_{H(3)}$ [e, c]	0		-	ns
$\overline{TS}$ hold time after CLK↑	$t_{H(4)}$	4		-	ns
D hold time after CLK↑	$t_{H(5)}$ [e]	0		-	ns
Delay from CLK↑ to $\overline{TA}$ driving	$t_{D(1)}$ [a]	0		20	ns
Delay from CLK↑ to active edge $\overline{TA}$	$t_{D(2)}$ [g]	1		7	ns
Delay from CLK↑ to inactive edge $\overline{TA}$	$t_{D(3)}$ [e]	1		7	ns
Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate	$t_{D(4)}$	5		-	ns
Delay from CLK↑ to $\overline{TA}$ going in tristate	$t_{D(5)}$ [e]	-		20	ns
Maximum response latency	$t_{D(6)}$	TBD		TBD	

a. Timing is relative to the rising edge of CLK during which $\overline{TS}$ is asserted.

b. Only applies if a write access is preceded by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.

c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.

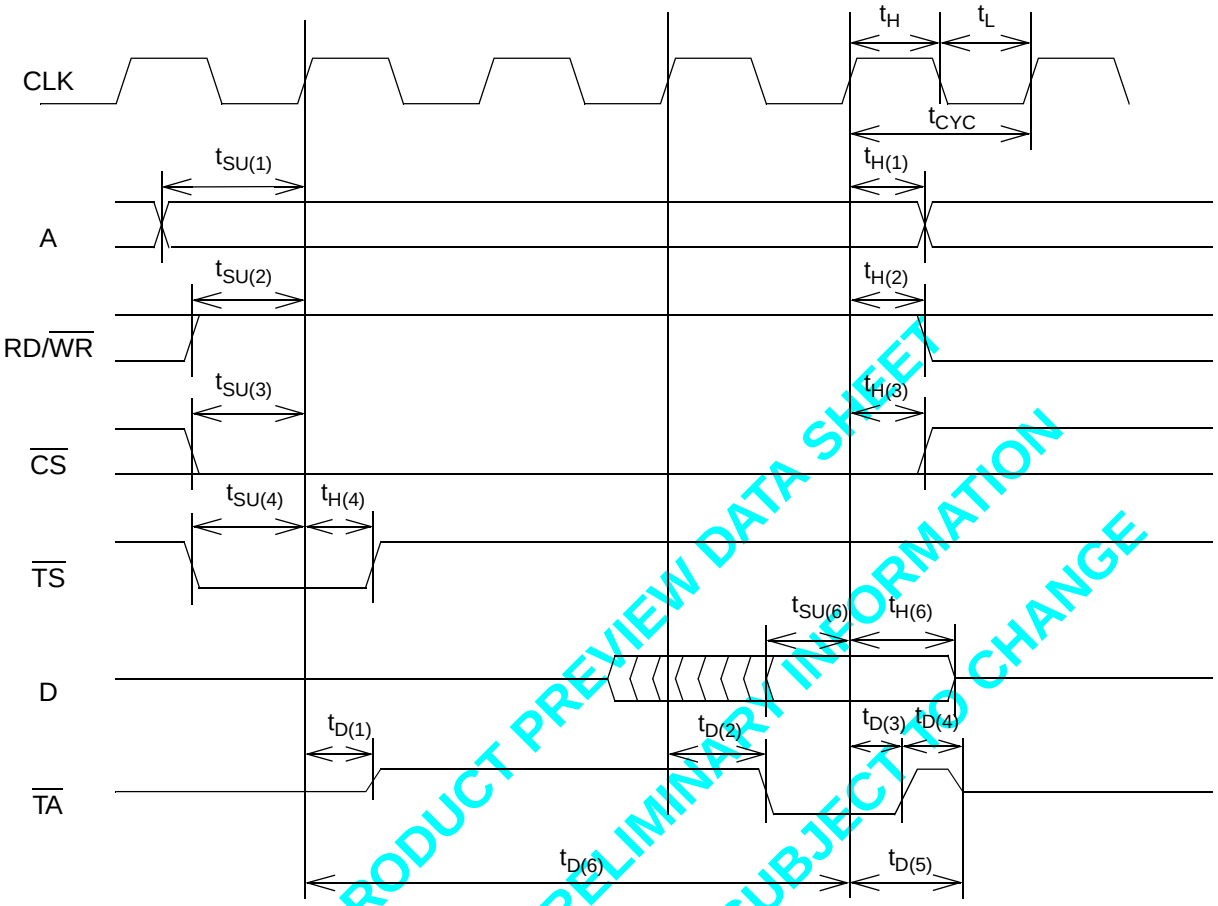
d. Timing is relative to next rising edge after the one during which $\overline{TS}$ is asserted.

e. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.

f. Only applies if a write access is followed by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.

g. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

Figure 32. Microprocessor Interface: Motorola MPC860 Mode Read Cycle[1]



1. See the Lead Description table on MOTOROLA MPC860 - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
A setup time before CLK↑	$t_{SU(1)}$ [a]	0		-	ns
RD/$\overline{WR}$ setup time before CLK↑	$t_{SU(2)}$ [a, b]	0		-	ns
$\overline{CS}$ setup time before CLK↑	$t_{SU(3)}$ [a, c]	6		-	ns
$\overline{TS}$↓ setup time before CLK↑	$t_{SU(4)}$	6		-	ns
A hold time after CLK↑	$t_{H(1)}$ [d]	0		-	ns
RD/$\overline{WR}$ hold time after CLK↑	$t_{H(2)}$ [d, e]	0		-	ns
$\overline{CS}$ hold time after CLK↑	$t_{H(3)}$ [c, d]	0		-	ns
$\overline{TS}$ hold time after CLK↑	$t_{H(4)}$	4		-	ns
Delay from CLK↑ to $\overline{TA}$ driving	$t_{D(1)}$ [a]	0		20	ns
Delay from CLK↑ to active edge $\overline{TA}$	$t_{D(2)}$ [f]	1		7	ns
Delay from CLK↑ to inactive edge $\overline{TA}$	$t_{D(3)}$ [d]	1		7	ns
Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate	$t_{D(4)}$	5		-	ns
Delay from CLK↑ to $\overline{TA}$ going in tristate	$t_{D(5)}$ [d]	-		20	ns
Maximum response latency	$t_{D(6)}$	TBD		TBD	
D setup time before CLK↑	$t_{SU(6)}$ [d]	t_{CYC}		-	
Hold time of D going in tristate to CLK↑	$t_{H(6)}$ [d]	1		12	ns

a. Timing is relative to the rising edge of CLK during which $\overline{TS}$ is asserted.

b. Only applies if a read access is preceded by a write access. RD/WR may stay high between 2 successive read accesses to the same peripheral.

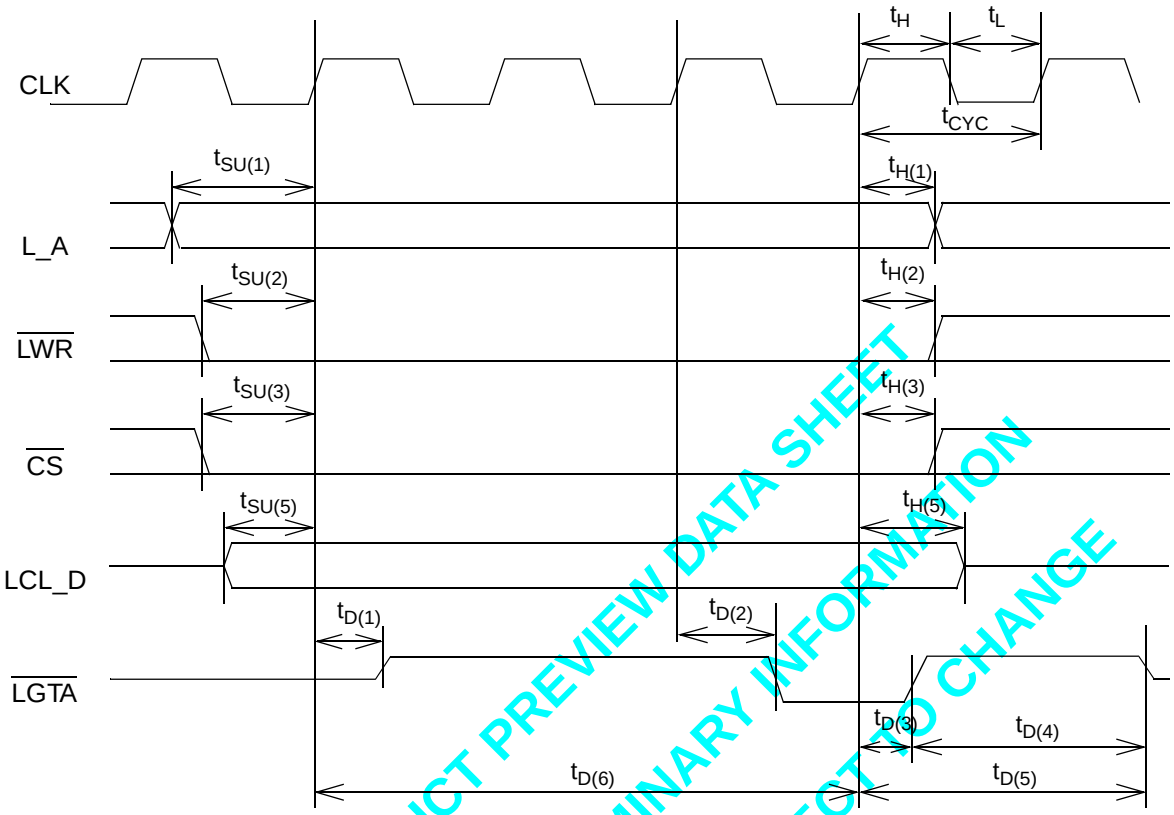
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.

d. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.

e. Only applies if a read access is followed by a write access. RD/$\overline{WR}$ may stay high between 2 successive read accesses to the same peripheral.

f. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

Figure 33. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Write Cycle[1]



1. See the Lead Description table on MOTOROLA MPC8260 LOCAL BUS - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
L_A setup time before CLK↑	$t_{SU(1)}$ [a]	0		-	ns
$\overline{LWR}$ setup time before CLK↑	$t_{SU(2)}$ [a, b]	0		-	ns
$\overline{CS}$ setup time before CLK↑	$t_{SU(3)}$ [c]	6		-	ns
LCL_D setup time before CLK↑	$t_{SU(5)}$ [a]	0		-	ns
L_A hold time after CLK↑	$t_{H(1)}$ [d]	0		-	ns
$\overline{LWR}$ hold time after CLK↑	$t_{H(2)}$ [d, e]	0		-	ns
$\overline{CS}$ hold time after CLK↑	$t_{H(3)}$ [c, d]	0		-	ns
LCL_D hold time after CLK↑	$t_{H(5)}$ [d]	0		-	ns
Delay from CLK↑ to $\overline{LGTA}$ driving	$t_{D(1)}$ [a]	0		20	ns
Delay from CLK↑ to active edge $\overline{LGTA}$	$t_{D(2)}$ [f]	1		7	ns
Delay from CLK↑ to inactive edge $\overline{LGTA}$	$t_{D(3)}$ [d]	1		7	ns
Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate	$t_{D(4)}$	3*t_{CYC} + 5		-	ns
Delay from CLK↑ to $\overline{LGTA}$ going in tristate	$t_{D(5)}$ [d]	3*t_{CYC}		3*t_{CYC} + 20	ns
Maximum response latency	$t_{D(6)}$	TBD		TBD	

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.

b. Only applies if a write access is preceded by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.

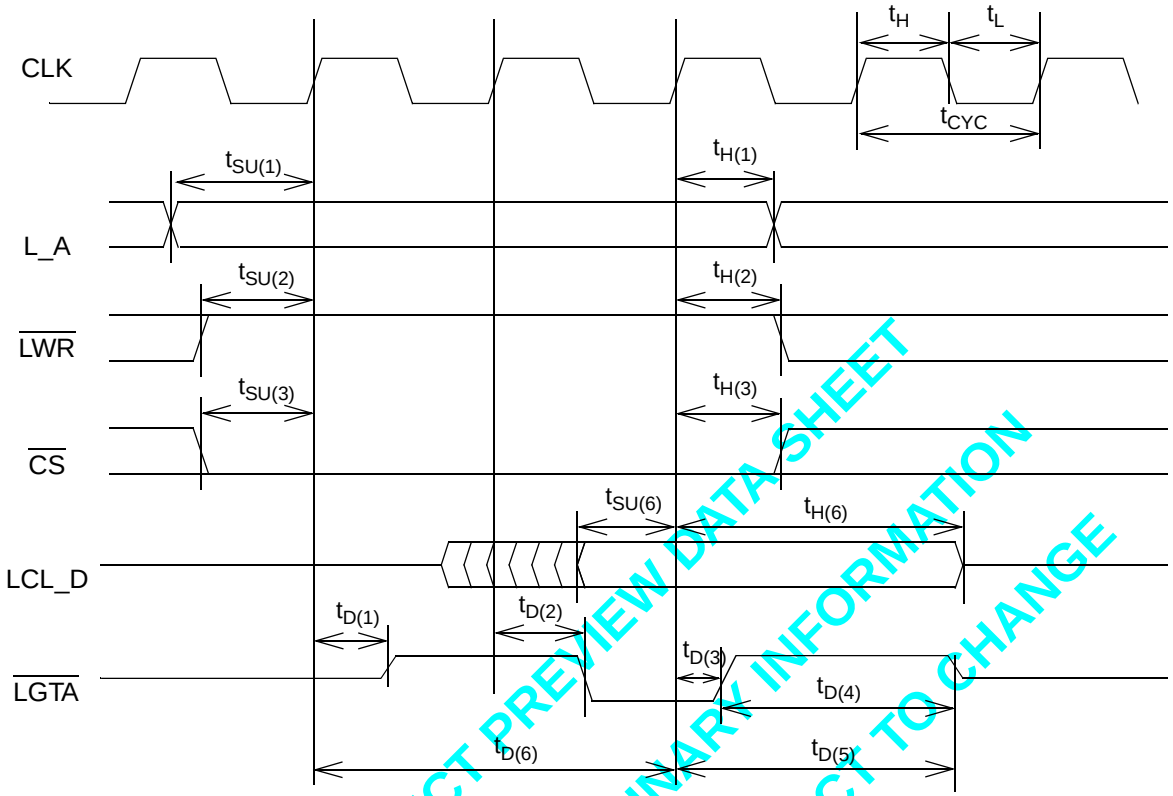
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.

d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.

e. Only applies if a write access is followed by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.

f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

Figure 34. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Read Cycle[1]



1. See the Lead Description table on MOTOROLA MPC8260 LOCAL BUS - HOST PROCESSOR INTERFACE for the mapping to I/O leads.

Parameter	Symbol	Min	Typ	Max	Unit
CLK clock period	t_{CYC}	20		-	ns
CLK clock low phase pulse width	t_L	0.4*t_{CYC}		-	
CLK clock high phase pulse width	t_H	0.4*t_{CYC}		-	
L_A setup time before CLK↑	$t_{SU(1)}$ [a]	0		-	ns
$\overline{LWR}$ setup time before CLK↑	$t_{SU(2)}$ [a, b]	0		-	ns
$\overline{CS}$ setup time before CLK↑	$t_{SU(3)}$ [c]	6		-	ns
L_A hold time after CLK↑	t_{H1} [d]	0		-	ns
$\overline{LWR}$ hold time after CLK↑	$t_{H(2)}$ [d, e]	0		-	ns
$\overline{CS}$ hold time after CLK↑	$t_{H(3)}$ [c, d]	0		-	ns
Delay from CLK↑ to $\overline{LGTA}$ driving	$t_{D(1)}$ [a]	0		20	ns
Delay from CLK↑ to active edge $\overline{LGTA}$	$t_{D(2)}$ [f]	1		7	ns
Delay from CLK↑ to inactive edge $\overline{LGTA}$	$t_{D(3)}$ [d]	1		7	ns
Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate	$t_{D(4)}$	3*t_{CYC} + 5		-	ns
Delay from CLK↑ to $\overline{LGTA}$ going in tristate	$t_{D(5)}$ [d]	3*t_{CYC}		3*t_{CYC} + 20	ns
Maximum response latency	$t_{D(6)}$	TBD		TBD	
D setup time before CLK↑	$t_{SU(6)}$ [d]	T		-	
Hold time of D going in tristate to CLK↑	$t_{H(6)}$ [d]	3*t_{CYC} + 1		3*t_{CYC} + 12	ns

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.

b. Only applies if a read access is preceded by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.

c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.

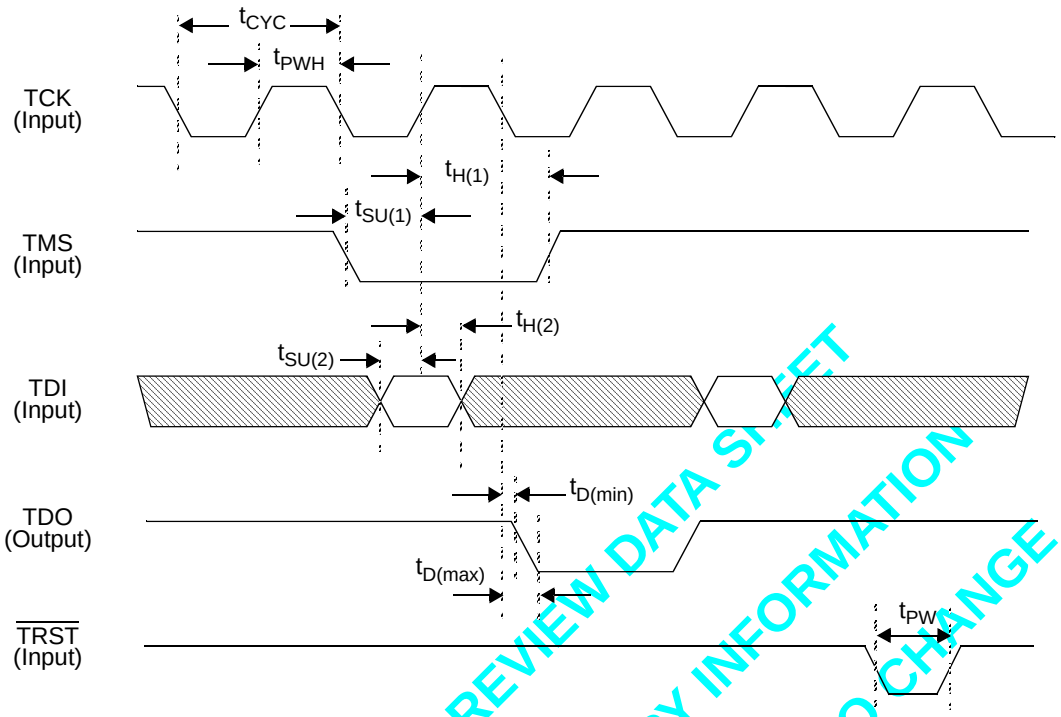
d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.

e. Only applies if a read access is followed by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.

f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

PRODUCT PREVIEW

Figure 35. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock period	t_{CYC}	50		ns
TCK clock duty cycle t_{PWH}/t_{CYC}		40	60	ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	15		ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	15		ns
TDO delay from TCK↓	t_D	4.0	20	ns
$\overline{TRST}$ pulse width	t_{PW}	50		ns

OPERATION

SONET/SDH PROCESSING

General

The Mapper and Demapper blocks provide the SONET/SDH processing of the EtherMap-12. The Mapper maps and multiplexes a Virtual Concatenated payload into a VC-4/STS-3c/VC-3/STS-1 structure on the ADD Telecom Bus. Conversely, the Demapper demaps and demultiplexes a VC-4/STS-3c/VC-3/STS-1 structure from the DROP Telecom Bus into a Virtual Concatenated payload. Figure 36 shows a functional block diagram of the Mapper and Demapper blocks.

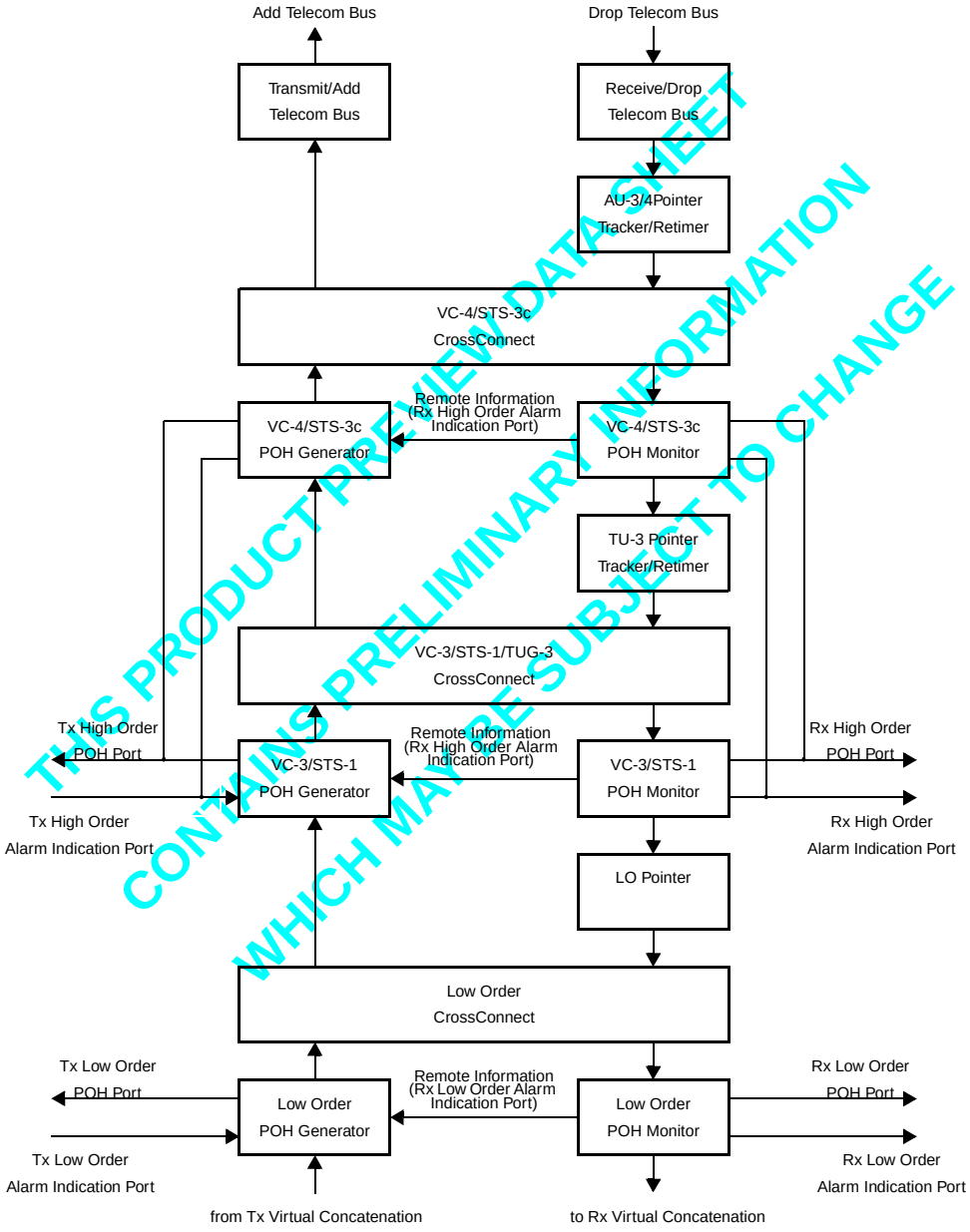


Figure 36. Functional Block Diagram of the Mapper/Demapper

Figure 37 presents a bi-directional functional model according to ITU-T G.783 of the functionality made available through the Mapper and Demapper blocks (see ITU-T G.806 for the terminology used). The Telecom Bus is represented as server layer to the S3/S4 High Order path layers.

.

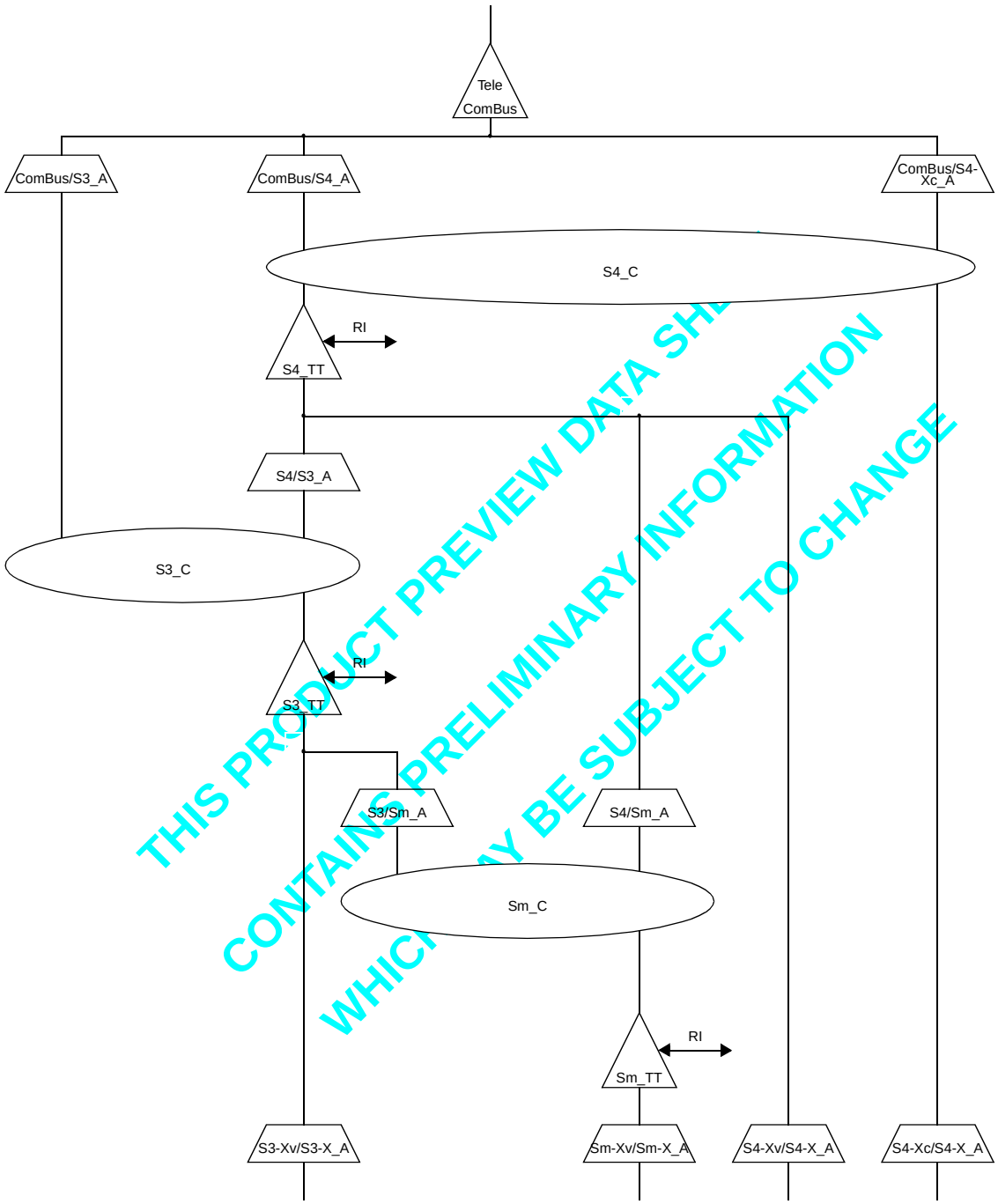


Figure 37. Functional Model of the Mapper/Demapper

MAPPER BLOCK

This block provides mapping and multiplexing for Low Order and High Order tributaries (carrying Ethernet framed data) into STM-4/STS-12 structures transmitted on the Add side Telecom Bus. A vast assemblage of SONET/SDH rates and format mappings are supported as indicated below:

- STS-12c SPE
- STS-12 / STS-9c SPE
- STS-12 / STS-6c SPE
- STS-12 / STS-3c SPE
- STS-12 / STS-1 SPE
- STS-12 / STS-1 / VT1.5 SPE
- STM-4 / AUG-4 / AU-4-4c / VC-4-Xc
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12s / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11s / VC-11
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11

All supported mappings can be mixed according to the [G.707] multiplexing structure up to a total payload rate equivalent to one STM-4/STS-12 signal.

HIGH ORDER PATH

The Tx Mapper formats the VCs/SPEs into a STM-4/STS-12 structure. The pointer value carried in the H1 and H2 bytes is transmitted with a fixed value 0 or 522. The microprocessor writes the signal label, and the 16 or 64-byte value of the J1 message. The device provides either single-bit or three-bit RDI. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Remote Error Indication (REI) is inserted from the BIP-8 errors detected on the receive side, and BIP-8 parity is generated for the B3 byte. Control bits are provided to generate unequipped, supervisory unequipped and AIS maintenance signals. Control bits are also provided to insert REI and BIP-8 errors in the G1/ B3 bytes for test purposes.

The Mapper complies with the latest ITU/ETSI/ANSI standards and features regarding the generation of the High Order Path Overhead bytes. These features include:

- J1 Byte: 16 or 64 Byte Trail Trace Identifier.
- B3 Byte: BIP-8 calculation and insertion.
- C2 Byte: signal label insertion.
- G1 Byte:
  - REI insertion (remote information from receive side).
  - RDI insertion (remote information from receive side): Single or Three bit.
  - Optionally RDI generation for a minimum of 20 Multiframes.
- H4 Byte:
  - Optionally Low Order V1/V2 multiframe generation.
  - Optionally Virtual Concatenation multiframe generation.
  - Optionally LCAS source state machine and control word generation.
- Unequipped Generation.
- Supervisory Unequipped Generation.
- AIS Generation.

- Tandem Connection Monitoring application is not supported.

LOW ORDER PATH

Low Order VC/VT tributaries are formatted into an STM-4/STS-12 structure. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 78 for VT1.5 and 105 for TU-12. The microprocessor writes the signal label, and the value of the J2 message as a 16-byte message. The device provides either single-bit or three bit RDI using the V5 and K4 bytes. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Remote Error Indication (REI) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated for the V5 byte. Control bits are provided for generating unequipped, supervisory unequipped and AIS maintenance signals. Control bits are also provided to insert REI and BIP-2 errors in the V5 byte for test purposes. A list of the VT/TU Overhead byte generation functions is listed below:

- J2 Byte
  - 16 Byte Trail Trace Identifier.
- V5 and K4 (Z7) Byte
  - REI Insertion (remote information from receive side).
  - RFI Insertion
    - Microprocessor control.
  - BIP-2 calculation and Insertion.
  - RDI Insertion (remote information from receive side): Single or Three bit.
  - Optionally RDI generation for a minimum of 20 Multiframes.
  - (Extended) signal label insertion.
  - 32-bit Virtual Concatenation Multiframe generation.
  - Optionally LCAS source state machine and control generation.
- Unequipped Channel Generation.
- Supervisory Equipped Generation.
- AIS Generation.
- Tandem Connection Monitoring application is not supported.

DEMAPPER BLOCK

The Demapper Block provides the demapping and demultiplexing of the Low Order and High Order tributaries from STM-4/STS-12 structures received on the Drop side Telecom Bus. The same vast assemblage of formats that are supported by the Mapper Block are also supported by the Demapper Block as shown below:

- STS-12c SPE
- STS-12 / STS-9c SPE
- STS-12 / STS-6c SPE
- STS-12 / STS-3c SPE
- STS-12 / STS-1 SPE
- STS-12 / STS-1 / VT1.5 SPE
- STM-4 / AUG-4 / AU-4-4c / VC-4-Xc
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12s / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11s / VC-11
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12
- STM-4 / AUG-4 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11

All supported mappings can be mixed according to the [G.707] multiplexing structure up to a total payload rate equivalent to one STM-4/STS-12 signal.

HIGH ORDER PATH

The Rx Demapper block performs High Order (AU-3/4/4-Xc and TU-3) pointer processing and retiming. The pointer tracking process is based on ETSI/ITU-T standards, which also meets ANSI requirements. Pointer increments and decrements are counted.

The High Order POH bytes are processed and monitored for trail trace identifier mismatch, signal label mismatch, unequipped status, VC AIS, BIP-8 parity error detection and error counter, REI error counting, single-bit or three-bit Remote Defect Indications (RDI), and loss of Virtual Concatenation or Low Order pointer multiframe. The received signal label can be retrieved, as well as the trail trace identifier of a selected channel.

The Rx Demapper complies to the latest ITU/ETSI/ANSI standards and features regarding the processing of the High Order Path Overhead bytes. These features include:

- J1 Byte: 16 or 64 Byte Trail Trace Identifier.
- B3 Byte: BIP-8 Bit/Block error counter option.
- C2 Byte: Signal Label Mismatch, Unequipped, and VC AIS detection.
- G1 Byte:
  - RDI detection, Single or Three bit.
  - REI error counter.
- H4 Byte:
  - Optionally Low Order V1/V2 multiframe monitoring.
  - Optionally Virtual Concatenation multiframe monitoring.
  - Optionally LCAS sink state machine and control word retrieval.
  - Tandem Connection Monitoring application is not supported.

LOW ORDER PATH

The Rx Demapper block performs Low Order pointer processing and retiming. The pointer tracking process is based on ETSI/ITU-T standards, which also meets ANSI requirements. Pointer increments and decrements are also counted, and the size bits are monitored for the correct value.

The Low Order POH bytes are processed and monitored for trail trace identifier mismatch, signal label mismatch, unequipped status, VC AIS, BIP-2 parity error detection and error counter, REI error counting, single-bit or three-bit Remote Defect Indications (RDI), and loss of Virtual Concatenation multiframe. The received (extended) signal label can be retrieved, as well as the trail trace identifier of a selected channel.

The Rx DeMapper complies to the latest ITU/ETSI/ANSI standards and features regarding the processing of the Low Order Path Overhead bytes. These features include:

- J2 Byte: 16 Byte Trail Trace Identifier.
- V5 and K4/Z7 Byte:
  - RDI detection, Single or Three bit.
  - REI error counter.
  - RFI detection.
  - BIP-2 Bit/Block error counter option.
  - Signal Label Mismatch, Unequipped, and VC AIS detection.
  - 32-bit Virtual Concatenation multiframe monitoring.
  - Optionally LCAS sink state machine and control word retrieval.
- Tandem Connection Monitoring application is not supported.

TRANSMIT HIGH ORDER PATH TERMINATION (VC-3/VC-4/VC-4-Xc/STS-1/STS-Nc POH Generator)

General

The EtherMap-12 optionally provides transmit High Order path termination functions for one STS-12c SPE/VC-4-4c, one STS-9c SPE/VC-4-3c, two STS-6c SPE/VC-4-2cs, four STS-3c-SPE/VC-4s and twelve STS-1 SPE/VC-3s.

J1

The transmitted J1 path trace message can be written by the microprocessor for transmission into the uP_J1MessageBytes RAM at address (TBD). The device supports 16 or 64 byte long repeating messages. The length can be selected via the J1_Length64 register, i.e., bit (TBD) at address (TBD).

B3

The B3 is calculated and transmitted for each SPE/VC.

For test purposes the EtherMap-12 supports a B3 error mask in the POH RAM, at address (TBD). When the B3_Masking register, bit (TBD) at address (TBD) is set, the calculated B3 is exor'ed with the B3 error mask before being inserted into the signal.

C2

The C2 signal label can be written by the microprocessor for transmission into the C2 position of the POH RAM at address (TBD).

The EtherMap-12 also has the option to source an unequipped signal by setting the ForceUneq register (bit TBD at address TBD) or a supervisory unequipped SPE/VC by setting the ForceSupUneq register (bit TBD at address TBD).

G1

The received B3 errors are automatically inserted into the G1 byte as path REI.

The EtherMap-12 has on option to transmit either a single bit path RDI or an enhanced 3-bit path RDI. Selection is made via the OneBitRDI register (bit TBD at address TBD).

The transmitted G1 bytes can be generated from local alarm conditions or derived from the Alarm Indication Port Interface. The selection is made per High Order path timeslot on the High Order Alarm Indication Port interface via the SelectInterface register at address (TBD). See the High Order Alarm Indication Port Interface section for the time slot assignment.

TBD	SelectInterface
0	RDI and REI generated from local alarm conditions.
1	RDI and REI derived from High Order Alarm Indication Port interface.

When the unidirectional option is active by setting the G1_UniDirectional register (bit TBD at address TBD), all transmitted remote information is set to zero.

H4

The H4 byte can be written by the microprocessor into the POH RAM at address (TBD), or by the High Order POH port interface for transmission, or it can be selected to carry the V1/V2 multiframe in case the SPE/VC is substructured into Low Order TU/VTs. It can also be selected to carry the Virtual Concatenation multiframe and control packets in case High Order Virtual Concatenation is active for this SPE/VC. This selection is made via the H4_Control register, bits (TBD) at address (TBD):

bit TBD	bit TBD	H4_Control
0	0	Insert H4 from the POH RAM, e.g. for an unstructured, non-Virtual Concatenated VC-4/STS-3c.
0	1	Insert H4 from the High Order POH port.
1	0	Pass the multiframe and control word for a Virtual Concatenated VC-3/STS-1.
1	1	Generate the V1/V2 multiframe for VC-3/VC-4/STS-1 SPE substructured into LO TU/VT's.

F2, F3, K3, and N1

The F2, F3, K3, and N1 bytes can be written by the microprocessor into the POH RAM, at address (TBD), or by the High Order POH port interface for transmission. These values are static and are not acted upon by the EtherMap-12 transmit logic.

The source can be selected via the F2_Control, F3_Control, K3_Control and N1_Control registers (bits TBD at address TBD): a value of 0 selects the POH RAM, a value of 1 selects the POH port.

RECEIVE HIGH ORDER PATH TERMINATION (VC-3/VC-4/VC-4-Xc/STS-1/STS-Nc POH Monitor)

General

The EtherMap-12 optionally provides receive High Order path termination functions for one STS-12c SPE/VC-4-4c, one STS-9c SPE/VC-4-3c, two STS-6c SPE/VC-4-2cs, four STS-3c-SPE/VC-4s and twelve STS-1 SPE/VC-3s.

The received POH bytes are always forwarded to the receive High Order POH Port interface and written to the receive High Order POH RAM at address (TBD).

J1

Both 16 and 64 byte messages can be received. The expected J1 path trace message can be configured at address (TBD). The received J1 path trace is compared with the microprocessor written expected J1 path trace. If a mismatch occurs between received and expected J1 path trace, a trace identifier mismatch defect (dTIM) is declared. An all-zero path trace is also reported to allow detection of an unequipped signal versus a supervisory unequipped signal.

The microprocessor can retrieve the value of the received J1 path trace of one VC-4/STS-3c and of one VC-3/STS-1 path termination at a time.

Address	Register	Description
TBD		Accepted 64 byte Trace Message
TBD	J1_Report_Enable	Enable reporting of the accepted J1 trace message for the J1_Report_Channel.

Address	Register	Description
TBD	J1_Report_Channel	Select the VC-4/STS-3c SPE resp VC-3/STS-1 SPE channel for which the J1 accepted trace message is retrieved.
TBD	J1_Stable_1	A constantly repeating single J1 byte has been detected.
TBD	J1_Stable_16	A 16-byte J1 trace message has been detected.
TBD	J1_Stable_64	A 64-byte J1 trace message has been detected.

The number of trace message multiframes to set or reset the TIM Defect is configurable via registers J1_NrOfFramesToSetTim (bits TBD at address TBD) and J1_NrOfFramesToResetTim (bits TBD at address TBD).

B3

Performance monitor counters are provided for the B3 errors and B3 block errors.

Optionally, the burst error degraded signal defect can be detected. The threshold values and interval times are configurable per High Order path via registers B3_SetThresHold, B3_ClearThreshold, B3_SetNrOfIntervals and B3_ClearNrOfIntervals at address (TBD).

C2

Unequipped detection (dUNEQ) and VC AIS detection (dAIS) is performed on the incoming C2 byte. The expected C2 signal label can be written by the microprocessor at address (TBD). If a mismatch occurs between the received C2 and the expected C2, a payload mismatch defect (dPLM) is declared.

The accepted C2 value is written to the on-chip RAM for retrieval by the microprocessor at address (TBD).

G1

A performance monitoring counter is provided for the path REI.

The G1 byte is monitored for the presence of single bit or enhanced path RDI.

H4

The H4 byte is written to the on-chip RAM for retrieval by the microprocessor. It can be optionally monitored for the V1/V2 multiframe in case the SPE/VC is substructured into Low Order TU/VTs, or the Virtual Concatenation multiframe in case High Order Virtual Concatenation is active for this SPE/VC. The selection is made per High Order path via the H4_MultiFrameType register (bits TBD at address TBD).

H4_MultiFrameType	
00	Disable monitoring of H4.
01	Monitor the V1/V2 multiframe for a VC-3/VC-4/STS-1 SPE substructured into Low Order TU/VTs.
10	Monitor the Virtual Concatenation multiframe.
11	Reserved.

F2, F3, K3, and N1

The F2, F3, K3, and N1 are written to the on-chip High Order POH RAM for retrieval by the microprocessor.

HIGH ORDER POH PORT INTERFACE

All received High Order POH bytes are output on the receive High Order POH port interface.

The transmit High Order POH port interface allows inserting most High Order POH byte into the High Order POH. J1 and C2 cannot be selected from the transmit High Order POH port interface, while the B3 BIP-8 is used as error mask on the calculated BIP-8 for test purposes.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is a 8-bit word with following format:

A7-A4	A3	A2	A1	A0	
Channel Number	0	0	0	0	J1
	0	0	0	1	B3
	0	0	1	0	C2
	0	0	1	1	G1
	0	1	0	0	F2
	0	1	0	1	H4
	0	1	1	0	F3
	0	1	1	1	K3
	1	0	0	0	N1

HIGH ORDER ALARM INDICATION PORT INTERFACE

The High Order Alarm Indication Port Interface transports the Remote Information (RI) from the High Order POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to insert by the POH generator.

The High Order POH monitor blocks multicast the Remote Information of all High Order path channels to the High Order POH generator blocks and the Receive High Order Alarm Indication Port Interface.

The High Order POH generator blocks can select per High Order path channel if the Remote Information is taken from the Transmit High Order Alarm Indication Port Interface, or the internal Remote Information provided by the High Order POH monitor blocks.

Each interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the High Order Alarm Indication Port data frame.

Each High Order Alarm Indication Port data frame consists of 16 timeslots of 32 bits per timeslot:

Frame	X																X+1
TimeSlot	0					1					...	15					...
Bit Number	31	30	...	1	0	31	30	...	1	0	...	31	30	...	1	0	...

The first 12 time slots are assigned to VC-3/STS-1 Remote Information, the last 4 time slots to VC-4/STS-3c Remote Information:

TimeSlot	Assigned to
0	VC3/STS-1 #1
1	VC3/STS-1 #2
2	VC3/STS-1 #3
3	VC3/STS-1 #4
4	VC3/STS-1 #5
5	VC3/STS-1 #6
6	VC3/STS-1 #7
7	VC3/STS-1 #8
8	VC3/STS-1 #9
9	VC3/STS-1 #10
10	VC3/STS-1 #11
11	VC3/STS-1 #12
12	VC-4/STS-3c #1
13	VC-4/STS-3c #2
14	VC-4/STS-3c #3
15	VC-4/STS-3c #4

Each 32-bit timeslot has a field for the REI and RDI. A valid flag indicates if the value in a field is valid and needs to be processed. Invalid values are ignored.

Bit Number	Name	Description
31	REI-valid	REI value in bits 30..27 is valid.
30..27	REI	REI value
26	reserved	
25	RDI-valid	RDI values in bits 24..22 are valid
24	RDI-S	Enhanced RDI Server failure, contributes to single bit RDI
23	RDI-C	Enhanced RDI Connectivity failure, contributes to single bit RDI
22	RDI-P	Enhanced RDI Path failure
21..4	reserved	
3..0	CRC-4	CRC-4 over bits 31..4

STS-1/AU-3/AU-4 POINTER GENERATION

In Add Bus master mode, the pointer value can be configured to be any value from 0 to 782.

TU-3 POINTER GENERATION

The TU-3 pointer has a fixed value of 0.

TU-3 POINTER TRACKING

The incoming negative and positive TU-3 pointer adjustments are counted for performance monitoring.

The LOP and Pointer AIS defects are detected.

VC-3/STS-1/TUG-3 CROSS CONNECT

The VC-3/STS-1/TUG-3 timeslots can be interchanged. Each TSI output VC-3/STS-1/TUG-3 timeslot can be configured to connect to any TSI input timeslot (SourceSlot) or to send an unequipped (ForceUneq) or AIS (ForceAIS) signal.

TU/VT POINTER TRACKING

The incoming negative and positive pointer adjustments are counted for performance monitoring.

The LOP and Pointer AIS defects are detected.

The V1, V2, and V4 bytes are written to the on-chip RAM for retrieval by the microprocessor (V1 RAM at TBD).

TU/VT POINTER GENERATION

The VT1.5/TU-11 pointer of the added VT1.5/VC-11s has a fixed value equal to 78.

The VT2/TU-12 pointer of the added VT2/VC-12s has a fixed value equal to 105.

LOW ORDER CROSS CONNECT

The Low Order timeslots can be interchanged. Each Low Order TSI output timeslot can be configured to connect to any TSI input timeslot or to send an unequipped (ForceUneq) or AIS (ForceAIS) signal.

Cross connects are made by writing the appropriate value into the MAPRAM_data cross connect map. This array of 336 elements is indexed by the output channel number, and its value represents the input channel number to be connected to this output channel.

The cross connect map consists of two banks of 336 elements. The cross connect hardware reads the information from the active bank, while the software can only write to the inactive bank. When a new configuration is written to the inactive bank, both banks can be swapped.

Software can select which of the banks is visible for reading.

TRANSMIT LOW ORDER PATH TERMINATION (Low Order POH Generator)

General

The EtherMap-12 provides transmit Low Order path termination functions for up to 336 VT1.5-SPE/VC-11s or 252 VT2-SPE/VC-12s. The Low Order POH generators are numbered according to the (B, 0) klm numbering: Channel = (B-1)*84+(k-1)*28+(l-1)*4+(m-1)

Channel	VC-4/STS-3c #	Assigned to Low Order #klm
0	0	VT1.5/VC-12 #111
1		VT1.5/VC-12 #112
2		VT1.5/VC-12 #113
3		VT1.5 #114
4		VT/VC-12 #121
...		...
82		VT1.5/VC-12 #373
83		VT1.5 #374
84	1	VT1.5/VC-12 #111
...		
334	3	VT1.5/VC-12 #373
335		VT1.5 #374

J2

The J2 path trace can be written by the microprocessor for transmission as a 16 byte long repeating message in the Transmit Low Order POH RAM at address (TBD).

BIP-2

The V5 BIP-2 is calculated and transmitted for each VT/VC.

For test purposes, the EtherMap-12 supports a BIP-2 error mask in the Transmit Low Order POH RAM, at address (TBD). When the BIP2_Error register, bit (TBD) at address (TBD), is set, the calculated BIP-2 is exor'ed with the BIP-2 error mask before being inserted into the V5 byte.

Signal Label

Both the V5 signal label (in the transmit Low Order POH RAM at address TBD) and the K4 extended signal label (Ext_SignalLabel register at address TBD) can be written by the microprocessor for transmission.

The V5 signal label must be set to '101' to activate the generation of the K4 bit 1 MFAS and Extended Signal Label.

The EtherMap-12 also has the option to source an unequipped signal or a supervisory unequipped VT/VC through the SendUneq and UneqSelect registers at address (TBD).

SendUneq bit TBD	UneqSelect bit TBD	
0	X	Source an equipped VC/VT.
1	0	Source an unequipped VC/VT.
1	1	Source a supervisory unequipped VC/VT

REI/RDI

The received V5 BIP-2 errors are automatically inserted into the V5 path REI. The EtherMap-12 has an option to transmit either a single bit V5 path RDI, or an enhanced 4-bit V5/K4 path RDI. The transmitted REI/RDI can be generated from local alarm conditions or derived from the Alarm Indication Port Interface. When the unidirectional option is active, all transmitted remote information is set to zero.

K4 Bit 2

The K4 bit 2 can be written by the microprocessor or by the High Order POH port interface for transmission, or it can be selected to carry the Virtual Concatenation multiframe and control packets in case Low Order Virtual Concatenation is active for this VT/VC. In the latter case, the extended signal label in K4 bit 1 has to be activated to generate the MFAS word (see "Signal Label" on page 100).

The source for the K4 bit 2 can be selected per Low Order channel through register LO_VC_Source, bits (TBD) at address (TBD).

bit (TBD)	bit (TBD)	LO_VC_Source
0	0	Insert K4 bit 2 from the POH RAM.
0	1	Insert K4 bit 2 from the High Order POH port.
1	0	Reserved
1	1	Pass the multiframe and control word for a Virtual Concatenated VC-12/VT1.5 SPE.

V5 RFI, and N2

The V5 RFI bit, N2 byte can be written by the microprocessor or by the Low Order POH port interface for transmission. This value is static and is not acted upon by the EtherMap-12 transmit logic.

RECEIVE LOW ORDER PATH TERMINATION (Low Order POH Monitor)

General

The EtherMap-12 provides receive Low Order path termination functions for up to 84 VT1.5-SPEs or 63 VC-12s for each STS-3-SPE or VC-4. Like the Low Order POH generators, the Low Order POH monitors are numbered according to the (B,0) klm numbering:

Channel = (B-1)*84+ (k-1)*28+(l-1)*4+(m-1)

The received POH bytes are always forwarded to the receive Low Order POH Port interface and written to the receive Low Order POH RAM at address (TBD).

J2

The EtherMap-12 supports 16 byte J2 trace messages. The received J2 path trace message can be compared with a microprocessor written expected J2 path trace at address (TBD). If a mismatch occurs between received and expected J2 path trace, a trace identifier mismatch defect (dTIM) is declared. An all-zero path trace is also reported to allow detection of an unequipped signal versus a supervisory unequipped signal.

The microprocessor can retrieve the value of the received J2 path trace of one Low Order path termination at a time.

Address	Register	Description
(TBD)		Accepted 16 byte Trace Message
(TBD), bit TBD	J2_Report_Enable	Enable reporting of the accepted J2 trace message for the J2_Report_Channel.
(TBD), bits TBD	J2_Report_Channel	Select the VT/VC channel for which the J2 accepted trace message is retrieved.
(TBD), bit TBD	J2_Stable_1	A constantly repeating single J2 byte has been detected.
(TBD), bit TBD	J2_Stable_16	A 16-byte J2 trace message has been detected.

The number of trace message multiframes to set or reset the TIM Defect is configurable via registers J2_NrOfFramesToSetTim (bits TBD at address TBD) and J2_NrOfFramesToResetTim (bits TBD at address TBD).

BIP-2

Performance monitor counters are provided for the V5 BIP-2 errors and V5 BIP-2 block errors.

Optionally the burst error degraded signal defect can be detected. The threshold values and interval times are configurable per Low Order path via registers BIP2_DEG_SetThresHold, BIP2_DEG_ClearThreshold, BIP2_DEG_SetNrOfIntervals and BIP2_DEG_ClearNrOfIntervals at address (TBD).

Signal Label

Unequipped detection (dUNEQ) and VC AIS detection (dAIS) is performed on the incoming V5 signal label. The expected V5 signal label and the expected K4 extended signal label can be written by the microprocessor. If a mismatch occurs between the received and the expected (extended) signal label, a payload mismatch defect (dPLM) is declared.

The accepted V5 signal label and K4 extended signal label values are written to the on-chip RAM for retrieval by the microprocessor.

Address	Register	Description
	TSL_Accepted	Accepted V5 trail signal label.
	ETSL_Accepted	Accepted K4 extended trail signal label.
	TSL_Expected	Expected V5 trail signal label.
	ETSL_Expected	Expected K4 extended trail signal label.

The number of (multi-)frames to accept a TSL or Extended TSL value is configurable via registers TSL_NrOfIntervals (bits TBD at address TBD) and ETSL_NrOfIntervals (bits TBD at address TBD).

REI/RDI/RFI

A performance monitoring counter is provided for the path REI.

The V5/K4 bytes are monitored for the presence of single bit or enhanced path RDI.

The V5 byte is monitored for the presence of RFI

K4 Bit 2

The K4 bit 2 can be optionally monitored for the Virtual Concatenation multiframe in case lower Order Virtual Concatenation is active for this SPE/VC.

N2

The N2 byte is written to the on-chip RAM for retrieval by the microprocessor.

LOW ORDER POH PORT INTERFACE

All received Low Order POH bytes of all 63/84 timeslots are output on the receive Low Order POH port interface.

The transmit Low Order POH port interface allows inserting most Low Order POH byte into the Low Order POH. J2 and the V5/K4 signal label cannot be selected from the transmit LO POH port interface, while the V5 BIP-2 field is used as error mask on the calculated BIP-2 for test purposes.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is a 12-bit word with following format:

A11	A10-A2	A1	A0	
0 (reserved)	TimeSlot Number (range 0..335)	0	0	V5
		0	1	J2
		1	0	N2/Z6
		1	1	K4/Z7

The Low Order time slots are numbered according to the (B,0) klm numbering:
TimeSlot = (B-1)*84+(k-1)*28+(l-1)*4+(m-1)

Channel	VC-4/STS-3c #(B,0)	Assigned to Low Order #klm
0	0	VT1.5/VC-12 #111
1		VT1.5/VC-12 #112
2		VT1.5/VC-12 #113
3		VT1.5 #114
4		VT/VC-12 #121
...		...
82		VT1.5/VC-12 #373
83		VT1.5 #374
84	1	VT1.5/VC-12 #111
...		
334	3	VT1.5/VC-12 #373
335		VT1.5 #374

LOW ORDER ALARM INDICATION PORT INTERFACE

The Low Order Alarm Indication Port Interface transports the Remote Information (RI) from the Low Order POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to insert by the POH generator.

The Low Order POH monitor blocks multicast the Remote Information of all Low Order channels to the Low Order POH generator blocks and the Receive Low Order Alarm Indication Port Interface.

The Low Order POH generator blocks can select per Low Order channel if the Remote Information is taken from the Transmit Low Order Alarm Indication Port Interface or the internal Remote Information provided by the Low Order POH monitor blocks.

Each interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the Low Order Alarm Indication Port data frame.

Each Low Order Alarm Indication Port data frame consists of 336 timeslots of 16 bits per timeslot:

Frame	X																X+1
TimeSlot	0					1					...	335					...
Bit Number	15	14	...	1	0	15	14	...	1	0	...	15	14	...	1	0	...

The Low Order time slots are numbered according to the (B,0) klm numbering:
TimeSlot = (B-1)*84+ (k-1)*28+(l-1)*4+(m-1)

Channel	VC-4/STS-3c #(B,0)	Assigned to Low Order #klm
0	0	VT1.5/VC-12 #111
1		VT1.5/VC-12 #112
2		VT1.5/VC-12 #113
3		VT1.5 #114
4		VT/VC-12 #121
...		...
82		VT1.5/VC-12 #373
83		VT1.5 #374
84	1	VT1.5/VC-12 #111
...		
334	3	VT1.5/VC-12 #373
335		VT1.5 #374

Each 16-bit timeslot has a field for the REI and RDI. A valid flag indicates if the value in a field is valid and needs to be processed. Invalid values are ignored.

Bit Number	Name	Description
15	REI-valid	REI value in bits 30..27 is valid.
14	REI	REI value
13	RDI-valid	RDI values in bits 24..22 are valid
12	RDI-S	Enhanced RDI Server failure, contributes to single bit RDI
11	RDI-C	Enhanced RDI Connectivity failure, contributes to single bit RDI
10	RDI-P	Enhanced RDI Path failure
9..4	reserved	
3..0	CRC-4	CRC-4 over bits 15..4

VIRTUAL CONCATENATION AND LCAS

The EtherMap-12 device takes a contiguous piece of Ethernet bandwidth and breaks it up into a number of individual SPE/VC which travel independently through the SONET/SDH network and are reassembled at their destination back into the contiguous piece of Ethernet bandwidth. The EtherMap-12 also performs the converse, by taking the SPE/VC that it has received from a sending device and reassembling it back into a contiguous piece of Ethernet bandwidth.

Two tremendous advantages are immediately obvious:

1) Since the Ethernet traffic is traveling through the network in a standard size SPE/VC, only the equipment at the end points needs to be changed.

2) Granularity of bandwidth used can be variable and in increments of the SPE/VC that is used. This is useful for the transport of payloads, such as Ethernet, which do not efficiently fit into one of the standard SPE/VC.

The EtherMap-12 device also supports LCAS (Link Capacity Adjustment Scheme). This is a mechanism where the allocated bandwidth for an Ethernet link can be dynamically reconfigured without causing any hits on to the existing traffic flow.

The sections below will describe in greater detail how the EtherMap-12 performs virtual concatenation.

LOW ORDER VIRTUAL CONCATENATION WITHOUT LCAS[1]

In SONET mode Ethernet traffic is transported in VT1.5-Xv-SPE as follows:

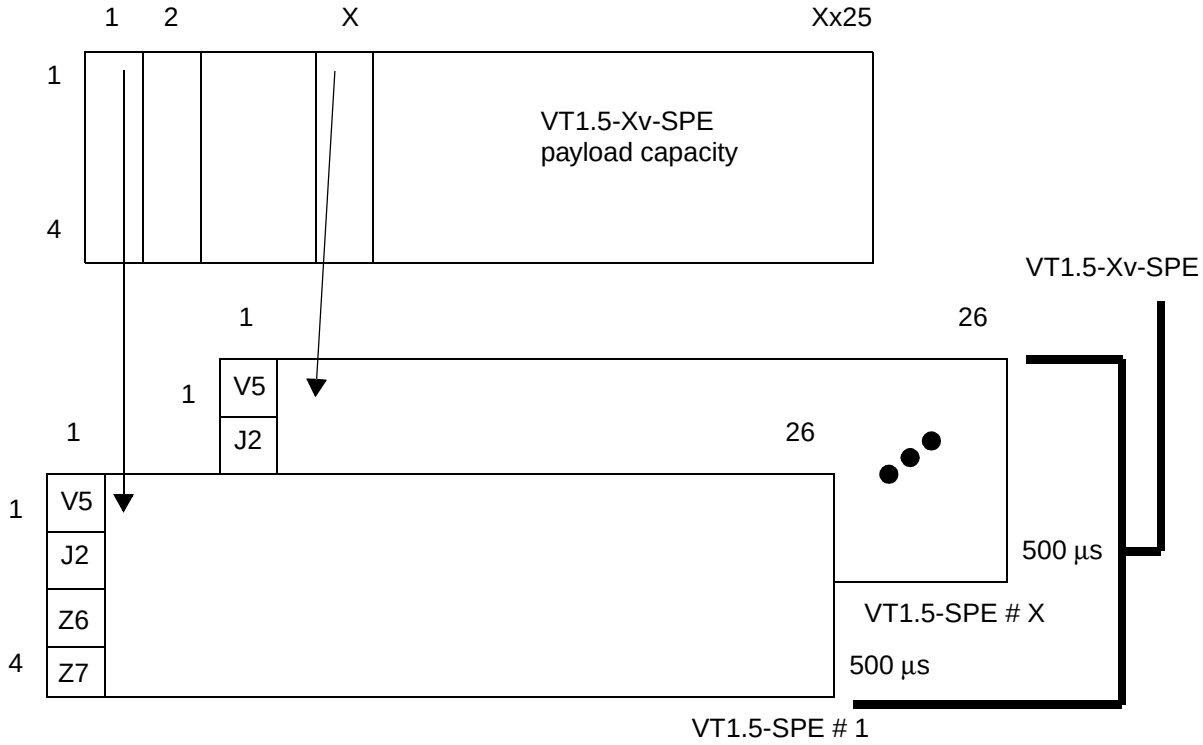


Figure 38. VT1.5-Xv-SPE Structure

The VT1.5-Xv-SPE payload capacity consists of Ethernet traffic which has been encapsulated in one of five ways: GFP, LAPS, LAPF, PPP or transparent HDLC. More will be said about these encapsulation methods in following sections.

In SDH mode, Ethernet traffic is transported in VC-12-Xv as shown below or in a VC-3-Xv as shown in Figure 45. Note, a VC-3 is considered high order if carried in an AU-3, and low order if carried in a TUG-3; in this case the VC-3s are mapped to a TUG-3 as shown in Figure 40. Also note that the EtherMap-12 has the capability to map the VC-3s to either a TUG-3 or AU-3 Just like for the VT1.5-Xv-SPE case, the VC-12Xv payload capacity consists of Ethernet traffic which has been encapsulated using GFP, LAPS, LAPF, PPP or transparent HDLC.

1. Note: in ITU-T SDH a VC-3 can either be high order (AU-3/STS-1) or low order (TU-3). In the EtherMap-12 data sheet high order and low order refers to the type of path overhead bytes rather than the order of the path in the multiplexing hierarchy. Though both low and high order VC-3 mapping is supported, VC-3 operation will be covered in the high order path sections (H4), while the low order sections only cover VC-11/VT1.5 and VC-12/VT2 (K4/Z7).

.

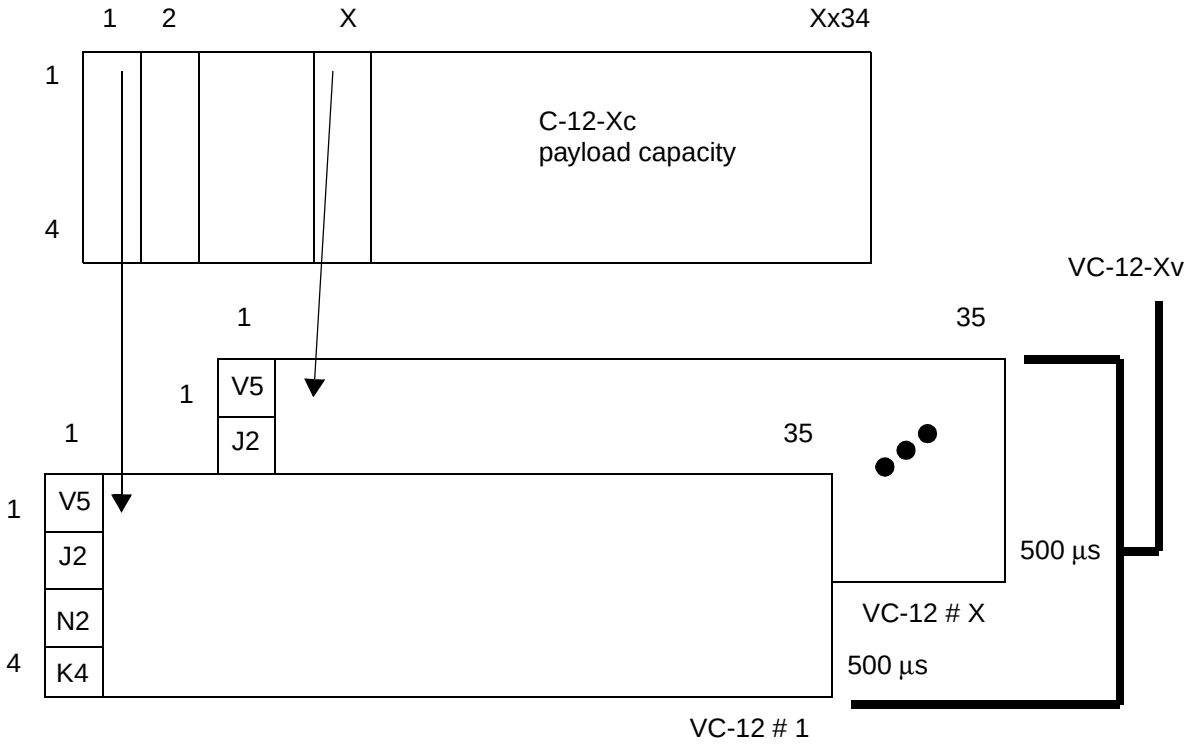


Figure 39. VC-11-Xv Structure

Once the EtherMap-12 has broken up the Ethernet payload into VC-12 or VT1.5-SPE they are then multiplexed into their respective SDH or SONET frame structures as shown below.

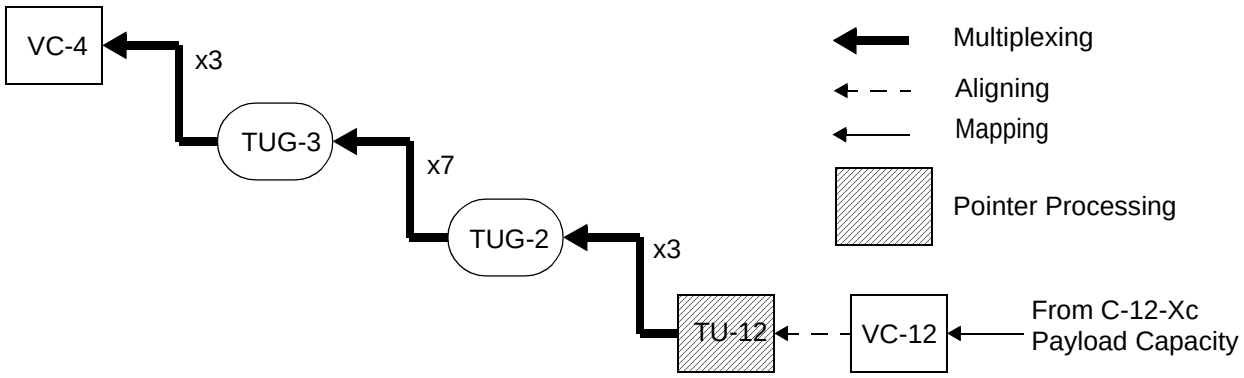


Figure 40. LO SDH Multiplexing Structure 1 Supported by the EtherMap-12

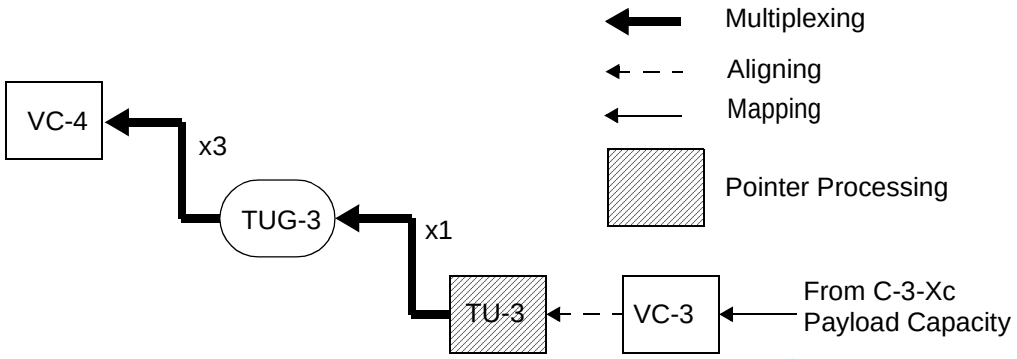


Figure 41. LO SDH Multiplexing Structure 3 Supported by the EtherMap-12

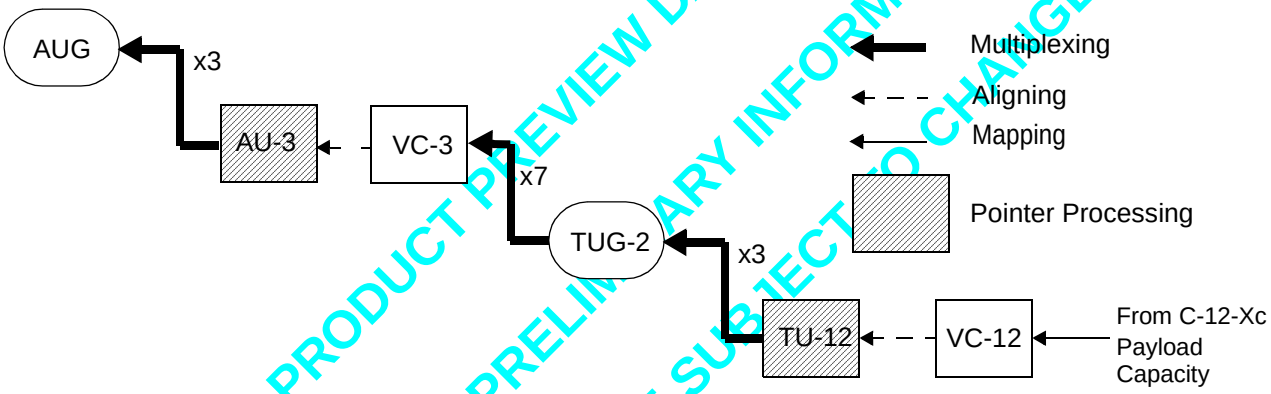


Figure 42. LO SDH Multiplexing Structure 2 Supported by the EtherMap-12

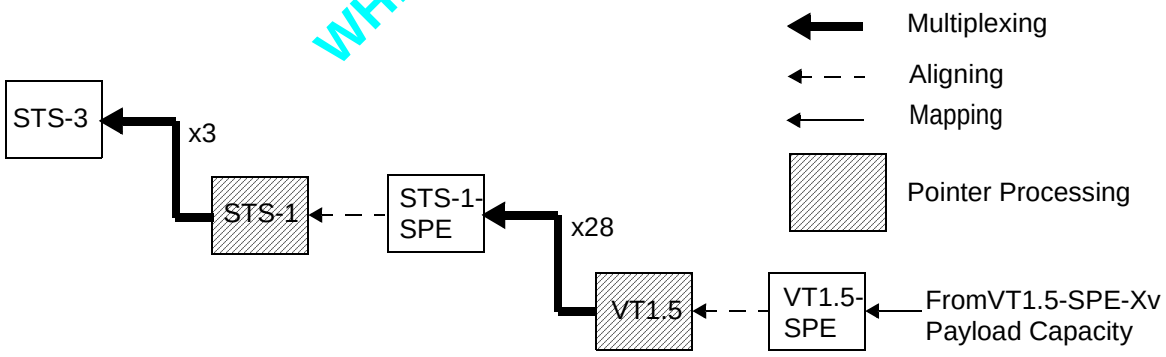


Figure 43. LO SONET Multiplexing Structure Supported by the EtherMap-12

LOW ORDER VIRTUAL CONCATENATION WITH LCAS

When using low order virtual concatenation in SONET/SDH mode, every low order virtual concatenation group (VCG) can be independently configured to optionally operate in LCAS mode. Low order virtual concatenation can be used without LCAS, but LCAS requires low/high order virtual concatenation. The low order virtual concatenation LCAS Control packet definition and format is specified in the ITU-T G.707/Y.1322 standard. The LCAS protocol is specified in the ITU-T G.7042/Y.1305 standard.

For SONET mode, the LCAS Control packet is resident in the Z7 [Bit 2] POH byte. For SDH mode, the LCAS Control packet is resident in the K4 [Bit 2] POH byte.

During initialization/normal operation, the EtherMap-12 device provides support for management and re-allocation of member resources between LCAS and non-LCAS modes for use by multiple low order VCGs. In addition, general add and remove operations are supported using single high level messages.

In the transmit direction, for every member of a low order VCG operating in LCAS mode, the EtherMap-12 device provides individual source side LCAS hardware-based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- PRBS generation for the Group Identification (GID) bit field.
- CRC-3 generation.
- LCAS Sequence Indicator (SQ) field generation.
- LCAS Control (CTRL) field generation.
- Inter-member messages during add/remove operations.
- For each transmit low order VCG in LCAS mode, selection of a low order member, in the receive direction, that is carrying the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Termination of MST and RS-Ack information from respective sink side LCAS state machine.
- Configurable low order per-member and per-VCG time-out counters for detection of failure during add and remove operations.
- Alarm generation to indicate LCAS source side state machine status.

In the receive direction, for every member of a low order VCG operating in LCAS mode, the EtherMap-12 device provides for individual sink side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- Group Identification (GID) field mismatch detection.
- CRC-3 check.
- LCAS Sequence Indicator (SQ) field processing.
- LCAS Control (CTRL) field processing.
- Generation of MST and RS-Ack status information.
- Detection and processing of Trail Signal Fail (TSF) conditions.
- For each receive low order VCG in LCAS mode, selection of a transmit side low order VCG that is used to transport the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Alarm generation to indicate LCAS sink side state machine status.

HIGH ORDER VIRTUAL CONCATENATION WITHOUT LCAS

In SONET mode Ethernet traffic is transported in STS-1-Xv-SPE or in a STS-3c-SPE. The STS-1-Xv-SPE structure is shown in the Figure 44. The STS-1-Xv-SPE payload capacity or the STS-3c-SPE data consists of Ethernet traffic which has been encapsulated in one of five ways: GFP, LAPS, LAPF, PPP or transparent HDLC.

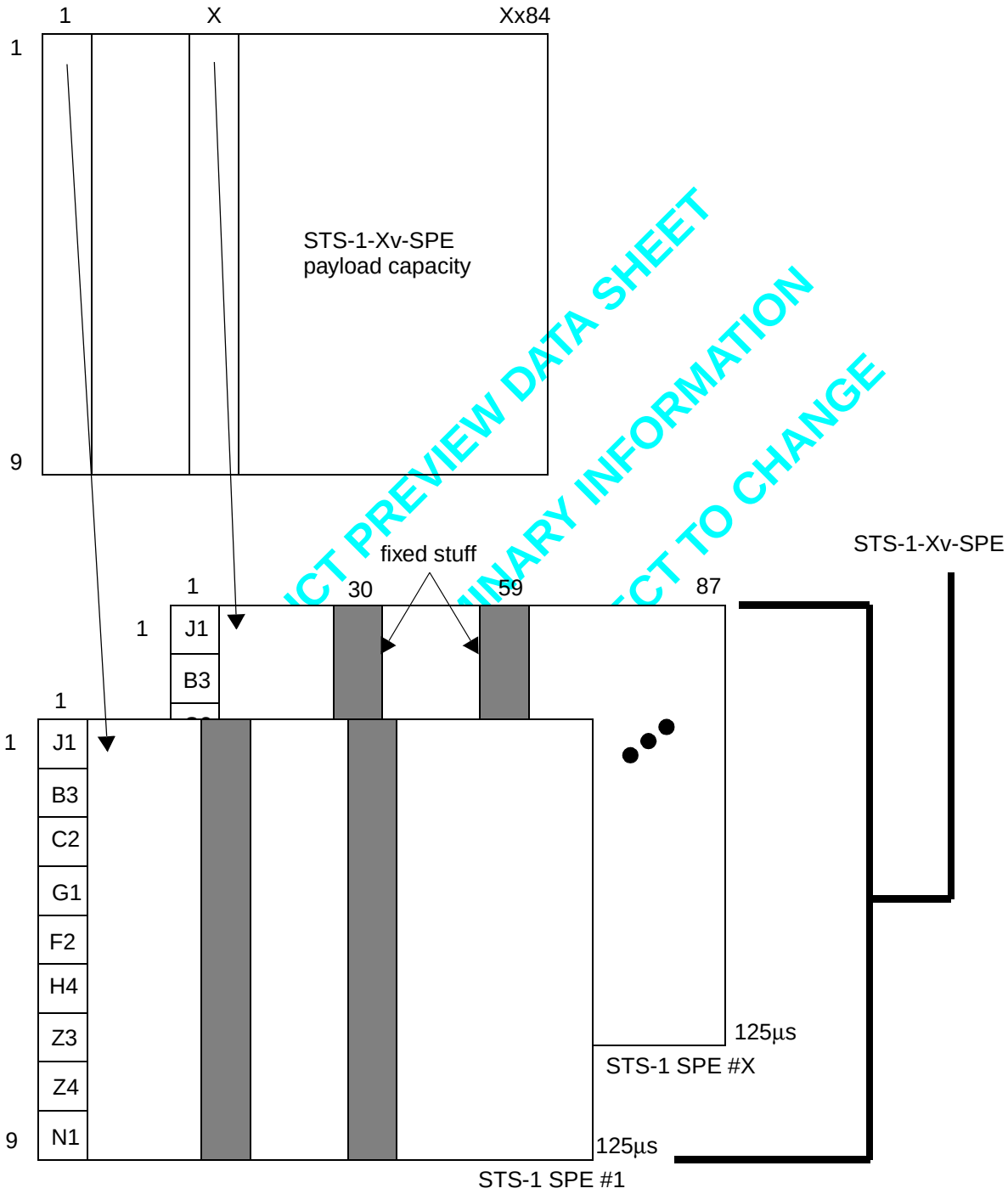


Figure 44. STS-1-Xv-SPE Structure

In SDH mode Ethernet traffic is transported in VC-3-Xv or in VC-4. Just like for the STS-1-Xv-SPE payload capacity the payload capacity for the VC-3-Xv and VC-4 consists of Ethernet traffic which has been encapsulated using GFP, LAPS, LAPF, PPP or transparent HDLC. The VC-3-Xv structure is shown below. Note, a VC-3 is considered high order as long as it is not carried in a TUG-3.

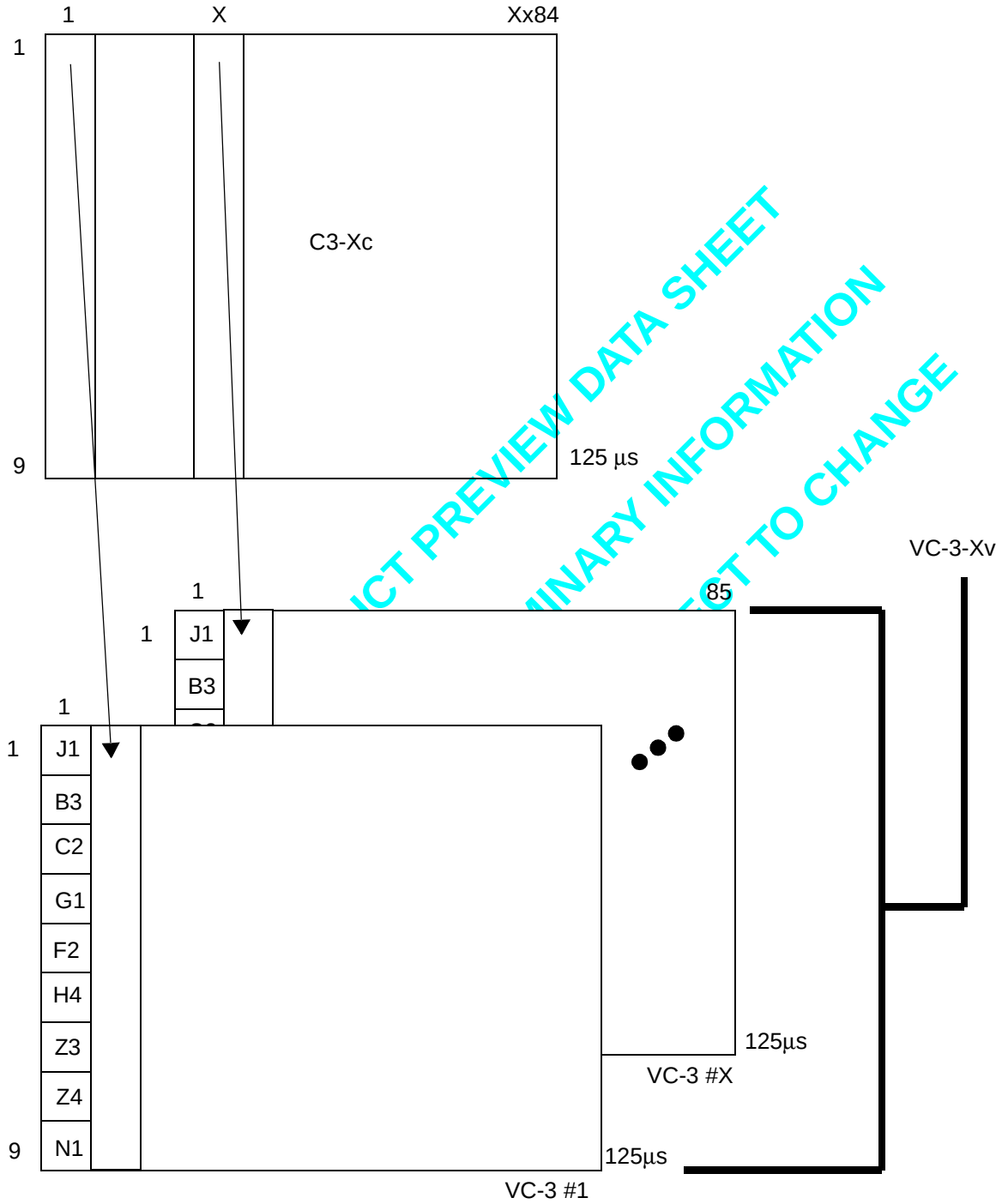


Figure 45. VC-3-Xv Structure

Once the EtherMap-12 has broken up the Ethernet payload into VC-3 or STS-1-SPE they are then multiplexed into their respective SDH or SONET frame structures as shown below. Notice that for the VC-3 structure that no stuff columns exist. However, when inserted into the AU-3, stuff columns are added so that the VC-3 ends up resembling an STS-1-SPE.

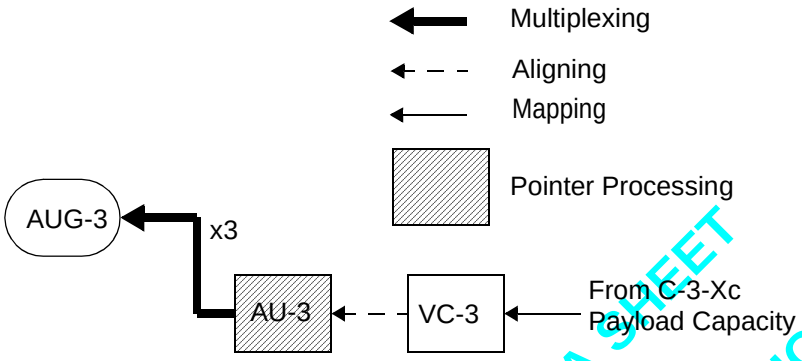


Figure 46. HO SDH Multiplexing Structure Supported by the EtherMap-12

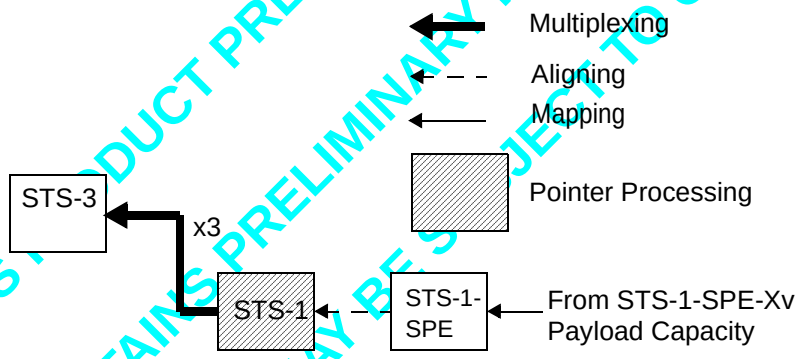


Figure 47. HO SONET Multiplexing Structure Supported by the EtherMap-12

HIGH ORDER VIRTUAL CONCATENATION WITH LCAS

When using high order virtual concatenation in SONET/SDH mode, every high order virtual concatenation group (VCG) can be independently configured to optionally operate in LCAS mode. High order virtual concatenation can be used without LCAS, but LCAS requires low/high order virtual concatenation. The high order virtual concatenation LCAS Control packet definition and format is specified in the ITU-T G.707/Y.1322 standard. The LCAS protocol is specified in the ITU-T G.7042/Y.1305 standard.

For both SONET and SDH modes, the LCAS Control packet is resident in the H4 POH byte.

During initialization/normal operation, the EtherMap-12 device provides support for management and re-allocation of member resources between LCAS and non-LCAS modes for use by multiple high order VCGs. In addition, general add and remove operations are supported using single high level messages.

In the transmit direction, for every member of a high order VCG operating in LCAS mode, the EtherMap-12 device provides for individual source side LCAS hardware-based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- PRBS generation for the Group Identification (GID) bit field.
- CRC-8 generation.
- LCAS Sequence Indicator (SQ) field generation.
- LCAS Control (CTRL) field generation.
- Inter-member messages during add/remove operations.
- For each transmit high order VCG in LCAS mode, selection of a high order member, in the receive direction, that is carrying the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Termination of MST and RS-Ack information from respective sink side LCAS state machine.
- Configurable high order per-member and per-VCG time-out counters for detection of failure during add and remove operations.
- Alarm generation to indicate LCAS source side state machine status.

In the receive direction, for every member of a high order VCG operating in LCAS mode, the EtherMap-12 device provides for individual sink side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- Group Identification (GID) field mismatch detection.
- CRC-8 check.
- LCAS Sequence Indicator (SQ) field processing.
- LCAS Control (CTRL) field processing.
- Generation of MST and RS-Ack status information.
- Detection and processing of Trail Signal Fail (TSF) conditions.
- For each receive high order VCG in LCAS mode, selection of a transmit side high order VCG that is used to transport the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Alarm generation to indicate LCAS sink side state machine status.

CONFIGURATION

General

The virtual concatenation of 8 Ethernet lines within 8 VCGs can be performed with the EtherMap-12. For both Transmit and Receive, it is possible to configure the design in Low order, high order, mixed high order/low order with LCAS or non LCAS on a per VCG basis. The following paragraphs explain how to configure the virtual tributaries and how to extract status information from the device.
Note: A coherency is necessary between the configuration of the Virtual concatenation part of the design and the mapper configuration (for example: High order virtual concatenation with high order mapping). All configuration bits which are defined with «Bklm» indication (**[1..4][1..3][1..7][1..4]**) are dedicated to the low order configuration which is shown in the following table (correspondence between Channel number and Bklm).

Channel	VC-4/STS-3 #(B,0)	Assigned to Low Order #klm
0	0	VT1.5/VC-12 #111
1		VT1.5/VC-12 #112
2		VT1.5/VC-12 #113
3		VT1.5 #114
4		VT/VC-12 #121
...		...
82		VT1.5/VC-12 #373
83		VT1.5 #374
84	1	VT1.5/VC-12 #111
...		
334	3	VT1.5/VC-12 #373
335		VT1.5 #374

Use the following procedure to Add/Remove members to a VCG in Non-LCAS Mode:

Transmit VCG

1) The member to be added must be first assigned to GLOBAL POOL of resources. This is done by setting the control bits cTLOPOOL_x (case of a Tx low order member), cTHOPOOL_x (Tx high order) to 00.

2) Perform a soft reset of the VCG affected (set TX_RESETSx register to 0x91).

3a) Add the member by placing it into the NON-LCAS POOL of resource. This is done by setting the control bits cTLOPOOL_x or cTHOPOOL_x to 01. The sequence indicator and VCG must be assigned to the member.

- OR -

3b) Remove the member by placing it into the GLOBAL POOL state.

4) Clear the soft reset per channel by writing 0x00 in TX_RESETSx.

Receive VCG

1) The member to be added must be first assigned to GLOBAL POOL of resources. This is done by setting the control bits cRLOPOOL_x (Rx low order), cRHOPOOL_x (Rx high order) to 00.

2) Perform a soft reset of the MAC corresponding to the VCG by setting to 1 the Reset Tx Function (bit TBD) (in the address TBD for MAC0).

3) Perform a soft reset of the VCG affected (set RX_RESETSx register to 0x91).

4a) Add the member by placing it into the NON-LCAS POOL of resources. This is done by setting the control bits cRLOPOOL_x or cRHOPOOL_x to 01. The sequence indicator and VCG must be assigned to the member.

- OR -

4b) Remove the member by placing into the GLOBAL POOL state.

5) Clear the soft reset of the MAC by clearing the Reset Tx Function (bit TBD in the address TBD for MAC0).

6) Clear the soft reset per channel by writing 0x00 in RX_RESETSx.

DIFFERENTIAL DELAY COMPENSATION

The EtherMap-12 performs differential delay compensation, for the containers included in a given virtual concatenation group.

This supports the scenario where the virtually concatenated containers travel different paths in the SONET/SDH network, and therefore are received by the EtherMap-12 with a time offset.

The mutliframe indicator field (MFI) is used for differential delay detection. MFI is located in the H4 byte (for high order virtual concatenation) or in the K4/Z7 byte (for low order virtual concatenation).

For each virtual concatenation group (VCG_x, x = 0 - 7), two registers are provided. See below.

Maximum Differential Delay Allowed

Register rMAXDELVCG_x is used to configure the maximum differential delay value allowed amongst the members of a virtual concatenation group (VCG_x). The maximum value that can be configured for both Low Order Virtual Concatenation (LO VCAT) and High Order Virtual Concatenation (HO VCAT) is 64 ms.

Low Order

In LO VCAT, only bits (TBD) of rMAXDELVCG_x are used. The value is configured in steps of 16 ms.

Table 1 shows the five values allowed:

Table 1: Configuration of rMAXDELVCG_x in Low Order VC

Configuration of rMAXDELVCG_x	Multiple of 16 ms	Resulting Maximum Delay Allowed
0x0000	0 x 16 ms	0 ms
0x0080	1 x 16 ms	16 ms
0x0100	2 x 16 ms	32 ms
0x0180	3 x 16 ms	48 ms
0x0200	4 x 16 ms	64 ms

High Order

In HO VCAT, bits (TBD) of rMAXDELVCG_x are used. The value is configured in steps of 125 µs.

Table 2 shows the 512 values allowed:

Table 2: Configuration of rMAXDELVCG_x in High Order VC

Configuration of rMAXDELVCG_x	Multiple of 125 µs	Resulting Maximum Delay Allowed
0x0000	0 x 125 µs	0 ms
0x0001	1 x 125 µs	125 µs
....	...	....
0x0180	384 x 125 µs	48 ms
....	...	....
0x0200	512 x 125 µs	64 ms

Maximum Differential Delay Detected

Register rDIFDELVCG_x reports the maximum differential delay detected among the members of a given virtual concatenation group (VCG_x). The maximum delay that can be detected is 128 ms.

Low Order

In LO VCAT, bits (TBD) of rDIFDELVCG_x represent the maximum differential delay detected among the low order members of a VCG_x.

The register has a granularity of 16 ms: a value of 0001 Hex represents a delay of 16 ms.

The maximum allowed value is 8, corresponding to 128 ms.

If the delay is higher than 128 ms, then bit (TBD) of rDIFDELVCG_x is set, indicating EtherMap-12 is not able to compute such a differential delay, and further, bits (TBD) of rDIFDELVCG_x contain invalid information. Further more in LO VCAT, when the reported differential delay is found to be greater than one configured in the rMAXDELVCG_x register, an alarm, aLOLOA_x, is generated (i.e., at a per VCG_x level).

High Order

In HO VCAT, bits (TBD) of rDIFDELVCG_x represents the maximum differential delay detected among the members of a VCG_x.

The register has a granularity of 125 µs: a value of 0001 Hex represents a delay of 125 µs.

The maximum allowed value is 1024, corresponding to 128 ms.

If the delay is higher than 128 ms, bit (TBD) of rDIFDELVCG_x is set, indicating EtherMap-12 is not able to compute such a differential delay, and further, bits (TBD) of rDIFDELVCG_x contain invalid information. Furthermore in HO VCAT, when the reported differential delay is found to be greater than one configured in the rMAXDELVCG_x register, an alarm, aHOLOA_x, is generated (i.e., at a per VCG_x level). HOL stands for Head Of Line.

Note: In both cases (LO VCAT and HO VCAT), EtherMap-12 can compute a differential delay up to 128 ms, but it can only compensate a maximum differential delay of 64 ms.

ETHERNET LINE INTERFACES

The EtherMap-12 supports two types of Ethernet line interfaces: SMII or GMII. The GMII Ethernet line interface is used only when the EtherMap-12 Ethernet line side is configured for 1000 Mbps operation. The SMII Ethernet line interface is used only when the EtherMap-12 Ethernet line side is configured for 10/100 Mbps operation. An external signal lead, GMII/SMII, provides for selection between either a single GMII Ethernet line interface or up to eight independent SMII Ethernet line interfaces. Note, that the GMII Ethernet line interface uses the same leads as the SMII Ethernet line interface and thus these two Ethernet line interfaces cannot be used simultaneously.

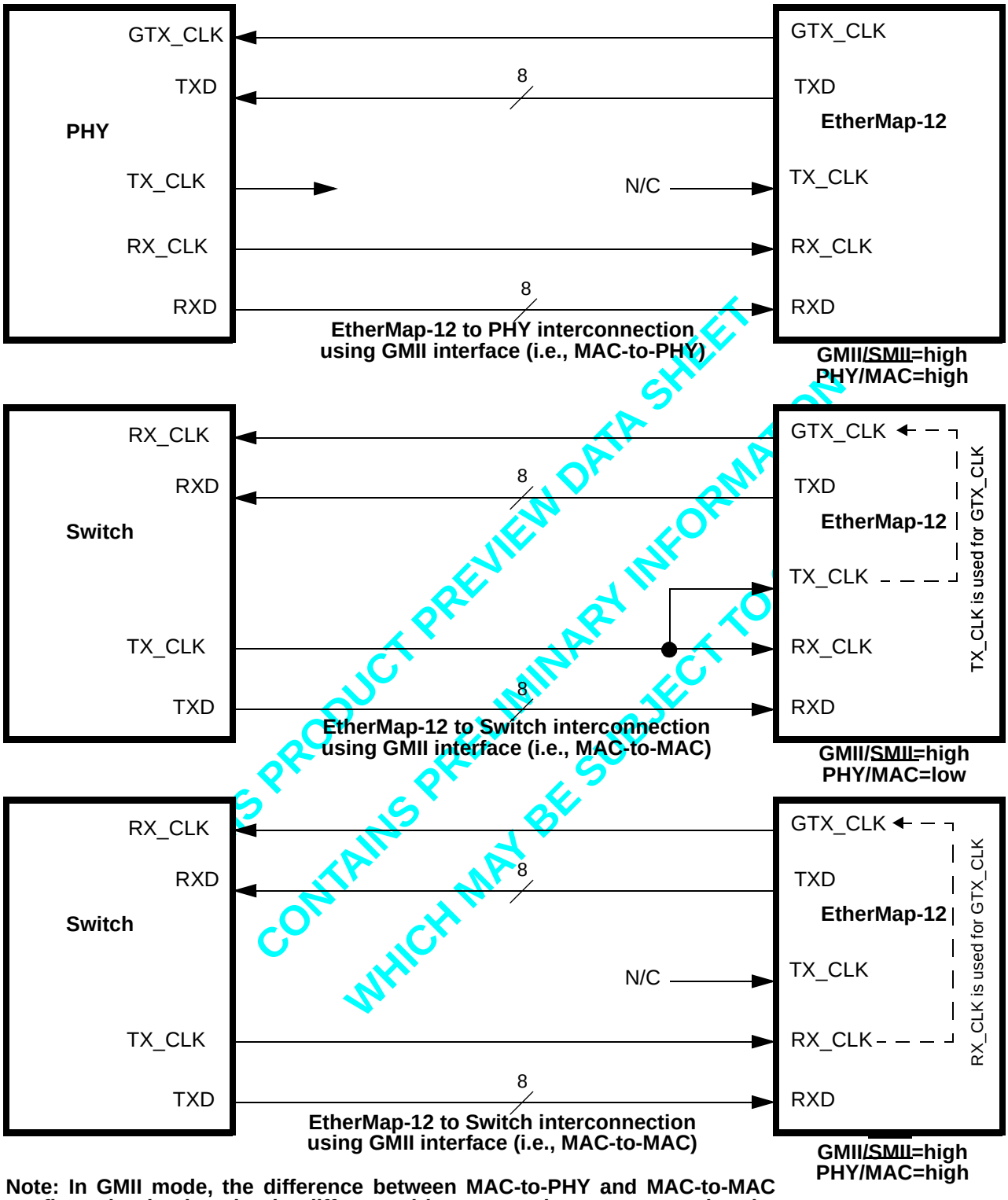
When using the GMII interface, an external signal lead, PHY/MAC, selects the clock source for the output signal, GTX_CLK. This allows for flexible interconnections between EtherMap-12 and other common components such as Ethernet PHY or Switch devices. Figure 48 shows these various interconnection options.

EtherMap-12 supports up to eight independent SMII interfaces. All eight SMII interfaces use a common global clock and common global sync signal (SMII_GCLK). An external signal lead, SYNC_DIR, controls the direction of the sync signal on the SMII_GSYNC signal lead.

The external lead PHY/MAC allows the 8 Ethernet lines of EtherMap-12 to be connected to a PHY or to a MAC. When PHY/MAC is equal to 1, EtherMap-12 is connected to a PHY and then is ready to accept status information from the PHY. When PHY/MAC is equal to 0, EtherMap-12 is considered to be connected to a MAC and then the 8 Ethernet interface need to be configured.

EtherMap-12 supports Half Duplex and Full Duplex for 10/100 Mbps and only Full Duplex for 1000 Mbps.

In addition to the GMII/SMII Ethernet line interfaces, the EtherMap-12 also provides support of control and status to and from external PHYs using a two-wire MII Management Interface (MDC, MDIO) as per IEEE 802.3u. This interface can be used with both GMII/SMII interfaces.



Note: In GMII mode, the difference between MAC-to-PHY and MAC-to-MAC configuration is given by the different wiring, as can be seen comparing the upper and the lower two configurations in this diagram.

Figure 48. EtherMap-12 to PHY or Switch Interconnection Using GMII Interface

ETHERNET MAC BLOCKS

The EtherMap-12 contains eight Ethernet MACs. However, when EtherMap-12 is configured for Gigabit mode, only the first MAC is used for 1000 Mbit/s operation. The remaining MACs are disabled. When EtherMap-12 is configured for 10/100 Mbit/s mode, all eight MACs are enabled and each can be independently configured for 10 or 100 Mbit/s operation. The selection between 10/100 or 1000 Mbit/s mode is done using the external signal lead GMII/SMII and internal registers select between 10 or 100 Mbit/s mode. In addition, if the attached PHY device auto-negotiates between 10 and 100Mbps, this information is passed to the MAC over the SMII interface and overrides any internal register setting.

In the transmit direction (i.e., towards the Ethernet line side), each MAC can be configured to apply or not to apply padding and to append or not to append a valid FCS field to the Ethernet frames. EtherMap-12 supports both Half Duplex mode (CSMA/CD) and Full Duplex mode for 10/100 Mbit/s and Full Duplex mode for 1000 Mbit/s. PAUSE flow control frame generation is fully configurable and supported (as per IEEE 802.3x). Following each Ethernet frame transmission or abortion, EtherMap-12 updates the appropriate transmit side RMON statistic counters.

The general configuration of the MACs is described in Tables TBD (including selection between Full or Half Duplex operation). Furthermore Table TBD specifies Half Duplex configuration such as:

- Configuration of collision window,
- Number of maximum transmission attempts following a collision before abortion,
- Abort or Transmit of an excessively deferred packet,
- Use of alternate binary exponential back-off rule or to immediately re-transmit a packet following a collision during back pressure,
- Use of 802.3 standard tenth collision or programmable alternate binary exponential back-off truncation.

In the receive direction (i.e., from the Ethernet line side), each MAC scans the preamble looking for the Start Frame Delimiter (SFD). The preamble and SFD are stripped and the remaining Ethernet frame is passed on for further processing. In addition, each MAC provides the capability to filter Ethernet frames that have less than a configured Inter-Frame Gap; to detect broadcast or multicast destination addresses; to check length field against the actual length of the data field portion of the Ethernet frame and to check or not the FCS field of the Ethernet frame. EtherMap-12 supports both Half Duplex mode (CSMA/CD) and Full Duplex mode for 10/100 Mbit/s and only Full Duplex mode for 1000 Mbit/s. This means that the PAUSE flow control frame detection is fully configurable and supported (as per IEEE 802.3x). Following each Ethernet frame reception, the appropriate receive side RMON statistic counters are updated.

Tables TBD are used for configuration and control of the MII Management interface. Using the control bits of Table TBD, the MDC (MII Management clock) is derived from the MICCLK clock by applying a divide factor of 4 to 28. It is possible also to suppress or not the preamble information. In order to perform a write access, the following steps need to be followed:

- Configure ‘Register address’ field (with 0x0 for control register) of Table TBD,
- Configure ‘Phy address’ field of Table TBD,
- Write a data value into the ‘MII Mgmt Control’ field of Table TBD,

Similarly, in order to perform a read access, the following steps need to be followed:

- Configure ‘Register address’ field (with 0x1 for control register) of Table TBD,
- Configure ‘Read Cycle’ field of Table TBD,
- Read a data value from the ‘MII Mgmt Status’ field of Table TBD.

ETHERNET HALF DUPLEX

In Half-Duplex mode of operation, two or more Ethernet devices are connected to a common transmission medium and when one Ethernet device transmits, the others listen. In the case where two Ethernet devices transmit at once, a “Collision” is said to have occurred. A “Jam Sequence” is transmitted by the transmitting Ethernet device indicating the occurrence of a collision. The contention is resolved by each of the Ethernet devices responsible for the collision, backing off, and attempting to re-transmit after a time period. This method is called Carrier Sense Multiple Access/Collision Detection (CSMA/CD). The EtherMap-12 Media Access Controller (MAC) implements the 802.3 compliant CSMA/CD algorithm. For a complete definition of this algorithm please refer to the IEEE 802.3 specification. Following is an outline based on the EtherMap-12 MAC.

Note: Carrier Sense and Collision detection status is indicated by the PHY device to the EtherMap-12 via the SMII interface. Please refer to the Serial Media Independent Interface (SMII) specification for further details.

CARRIER SENSE

To begin transmission of an Ethernet frame, the EtherMap-12 Media Access Controller (MAC) uses three different configuration registers. After the transmission of an Ethernet frame, the Back-to-Back Inter Packet Gap (IPG) is enforced. After an Ethernet frame is received, the Non-Back-to-Back IPG (IPG2) is used. Additionally, during the time defined by the IPGR1 configuration register, the MAC monitors the Carrier Sense status. This Carrier Sense window is known as IPG1. If carrier is detected during this window, the MAC does not attempt to transmit. If the carrier becomes active after the IPG1 window, transmission is begun after the proper IPG has elapsed, forcing a collision and subsequent backoff. The Carrier Sense window is typically configured using a two-thirds/one-third ratio, meaning that the carrier is monitored during the first two-thirds of the IPG, and is ignored during the remaining one-third. Since it is not possible for the Ethernet output to backpressure traffic arriving from SONET/SDH, it may be necessary to configure the EtherMap-12 to more aggressively occupy the Ethernet media by reducing the size of the IPG1 window.

COLLISION DETECTION

In the event the EtherMap-12 MAC detects a Collision when the device is transmitting an Ethernet frame, the MAC outputs the 32-bit jam sequence. The jam sequence is made up of several bits of the CRC, inverted to guarantee an invalid CRC upon reception of the frame. The MAC then backs off transmission of the frame (retry) based on the “Truncated Binary Exponential Backoff” (BEB) algorithm. Following this backoff time, the frame is retried. The “No Backoff” configuration bit, when enabled, retransmits the frame without a backoff, following a collision. This option needs to be enabled with caution.

ALTERNATE BEB TRUNCATION

The backoff time following a collision is a controlled randomization process called “truncated binary exponential backoff”. It is defined as an integer multiple of the slot times. The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range: $0 \leq r \leq 2^k$ where k = min(n,10). So, after the first collision, the MAC will backoff either 0 or 1 slot times. After the fifth collision, the MAC will backoff between 0 and 32 slot times. After the tenth collision, the maximum number of slot times to backoff is 1024. By setting the “Alternate BEB Enable” bit, the truncation point can be changed from min(n,10) to min(n,m) where m is set in the “Alternate BEB Truncation” register.

EXCESSIVE COLLISIONS

Upon collision, the MAC attempts re-transmission of the frame. As specified in the IEEE 802.3 specification, a frame has excessive collisions if 15 re-transmission attempts have occurred. The number of retransmission attempts for excessive collisions is configurable. In the event a frame has been excessively deferred, the frame is discarded and will not be transmitted. It is possible to configure the EtherMap-12 not to discard an excessively deferred frame.

HALF-DUPLEX FLOW CONTROL

There is no IEEE 802.3 compliant backpressure mechanism for Half Duplex. The common industry implementation is the “Raise Carrier” method. The EtherMap-12 MAC uses the configurable “Raise Carrier” method for flow control in Half-Duplex mode. In the event the EtherMap-12 MAC needs to backpressure the transmission medium, it raises carrier by transmitting the preamble. Other devices on the transmission Medium defer to the carrier. If a collision occurs due to the raised carrier, the congestion is resolved using the standardized collision-detect, backoff method. The Host can not initiate flow control when raise carrier method is being used.

FLOW CONTROL OPERATION

Because there could be a mismatch of bandwidth rates between an Ethernet port and its corresponding SONET/SDH link (i.e., transporting 100Mbit/s using a single VC-3), EtherMap-12 has the ability to flow control the Ethernet traffic. Depending on the mode of operation of the Ethernet port (i.e., Full Duplex or Half Duplex), the EtherMap-12 provides support for the following types of flow control mechanisms:

- Full Duplex mode (for 10/100/1000 Mbit/s): when configured for Full Duplex mode, the PAUSE frame (as per IEEE 802.3x) is used as a flow control mechanism.
- Half Duplex mode (for 10/100 Mbit/s): when configured for Half Duplex mode, the CSMA/CD algorithm is used as a back-pressure flow control mechanism. The back-pressure scheme uses the 'raise carrier' method. Table TBD provides further details on specific configuration options.

For Full Duplex mode of operation, in the Ethernet-to-SONET direction, the EtherMap-12 provides support for PAUSE frame flow control when 'Transmit Flow Control Enable' and 'Receive Flow Control Enable' control bits are set in Table TBD and the cTFCMODEx register is configured appropriately. In the case of 10/100 Mbit/s, the EtherMap-12 allocates eight separate buffers (i.e., TXFIFOs), on a per Ethernet port basis, within the external SDRAM. In the case of 1000 Mbit/s, the EtherMap-12 allocates a single buffer (i.e., the previous eight separate buffers are concatenated into a single contiguous buffer) for the single Ethernet port within the external SDRAM. The TXFIFOs buffer/rate adapt incoming traffic from the Ethernet ports before they are transmitted onto SONET/SDH. So, when there is a mismatch of bandwidth rates between the Ethernet ports and the SONET/SDH link, a situation can occur where the TXFIFO fill level will begin to increase and eventually lead to an overflow condition. EtherMap-12 employs a mechanism of High (rHWTMK_MSB_x, rHWTMK_LSB_x) and Low (rLWTMK_MSB_x, rLWTMK_LSB_x) watermarks per TXFIFO. Associated with each of these watermarks is a configurable PAUSE frame timer value (i.e., High watermark corresponds to rHWPT_x register and Low watermark corresponds to rLWPT_x register). Lastly, the rHIPSE_x register is used to configure the point in time when the fill level of the TXFIFO is checked in order to determine transmission of further PAUSE frames.

When the fill level of the TXFIFO exceeds the High watermark (i.e., rHWTMK_MSB_x, rHWTMK_LSB_x), the corresponding transmit MAC is requested to generate a PAUSE flow control frame (with a PAUSE timer value as per the rHWPT_x register) towards the Ethernet line side. Once the PAUSE frame is transmitted, the value of the rHWPT_x register is loaded into an internal pause timer (i.e., a separate internal pause timer exists per TXFIFO). This internal pause timer starts to decrement at the rate of the corresponding MAC. As the internal pause timer decrements, when its count value is equal to that of the rHIPSE_x register, at this point the fill level of the TXFIFO is checked and the following possible actions can be taken:

- If the TXFIFO fill level is equal to or above the High watermark, the corresponding transmit MAC will be requested to generate a PAUSE flow control frame using the PAUSE timer value from the rHWPT_x register. At this time, the internal pause timer is re-loaded again with the contents of the rHWPT_x register and begins again to decrement at the rate of the corresponding transmit MAC.
- If the TXFIFO fill level is below the High watermark but above the Low watermark, the corresponding transmit MAC will not request to generate a PAUSE flow control frame and the internal pause timer is reset to zero.
- If the TXFIFO fill level is below the Low watermark, the corresponding transmit MAC will generate a PAUSE flow control frame using the PAUSE timer value from the rLWPT_x register.

Note when a PAUSE frame must be sent to the Ethernet client (SONET to Ethernet direction), if there a frame in the Tx FIFO that has just been started, the transmission of this frame is completed, and the PAUSE frame follows immediately. In other words, the Tx FIFO cannot be preempted.

While the internal pause timer is decrementing and is not equal to zero, if a TXFIFO overflow condition occurs, an alarm aTXFIFOx is asserted, further writes into the TXFIFO are stopped and the last/most recent Ethernet frame found to be incomplete is discarded. Any follow-on Ethernet frames, from the Ethernet line side, are

discarded and counted using the rpcL2TDROPOVFx counter. During this condition, the contents of the TXFIFO continue to be read out and transmitted onto SONET/SDH as the fill level starts to recede. No Idle frames are sent to SONET/SDH side other than those required minimally as per the configured encapsulation protocol. The corresponding transmit MAC makes a request to generate a PAUSE flow control frame (using the contents of the rHWPT_x register) and the internal pause timer begins to decrement (after being loaded with the contents of rHWPT_x register) in order to determine when to check the TXFIFO fill level. When checking the TXFIFO fill level, the following possible actions can be taken:

- If the TXFIFO fill level is still equal to or above the High watermark, then further writes into the TXFIFO remain suspended and the procedure outlined above is followed.
- If the TXFIFO fill level is below the High watermark, then further writes into the TXFIFO are allowed to begin and the procedure outlined above is followed.

For Half Duplex mode of operation, in the Ethernet-to-SONET direction, the EtherMap-12 provides the common back-pressure flow control mechanism in order to manage the TXFIFO fill levels. If the TXFIFO fill level is equal to or above the High watermark, the corresponding transmit MAC will be requested to apply/enable the back-pressure mechanism (by raising carrier). This is also the case when an overflow condition is detected using the alarm, aTXFIFOx. On the other hand, if the TXFIFO fill level is below the Low watermark, the corresponding transmit MAC will not apply/enable the back-pressure mechanism.

In the SONET-to-Ethernet direction, the EtherMap-12 provides the ability to configure handling of PAUSE flow control frames that may be received from the SONET/SDH side. Using the cRFCMODEx register, a selection can be made to pass through or discard the received PAUSE flow control frames, that are to be transmitted to the Ethernet line side. In any event, all received PAUSE flow control frames are counted (per Ethernet port) using the rpcRPAUSEx counter.

When changing flow control parameters from their default values, the following procedure should be followed:

From a Hardware Reset:

1. Configure the flow control parameters (Tables TBD and TBD).
2. De-assert the MAC Soft Reset (see Table TBD - Reset Tx, Reset Rx).
3. Enable the transmit and receive MAC blocks (see Table TBD - Transmit Enable and Receive Enable).

From an already configured device:

1. Disable the transmit and receive MAC blocks.
2. Assert the MAC Soft Reset.
3. Configure the flow control parameters (Tables TBD and TBD).
4. De-assert the MAC Soft Reset.
5. Enable the transmit and receive MAC blocks.

ENCAPSULATION / DECAPSULATION

When the Ethernet line side is configured for SMII interface, the EtherMap-12 device provides support for up to eight independent 10/100 Mbit/s Ethernet MAC blocks. Each 10/100 Mbit/s Ethernet MAC block is further allocated to a dedicated protocol encapsulation/decapsulation block (up to eight independent blocks) for servicing its bi-directional Ethernet frame traffic.

When the Ethernet line side is configured for GMII interface, the EtherMap-12 device provides support for a single 1000 Mbit/s Ethernet MAC block (shared with the first 10/100 Mbit/s Ethernet MAC block). The 1000 Mbit/s Ethernet MAC block is allocated to a dedicated protocol encapsulation/decapsulation block (the first block is shared between 10/100 Mbit/s and 1000 Mbit/s) for servicing its bi-directional Ethernet frame traffic.

Each protocol encapsulation/decapsulation block can be independently configured to use one of the following protocols for transport of Ethernet MAC frames over a SONET/SDH link: Generic Framing Procedure (GFP), Link Access Procedure - SDH (LAPS), Link Access Procedure Frame Mode (LAPF), Point-to-Point Protocol (PPP) with Bridging Control Protocol (BCP) and Transparent HDLC. By default, the protocol encapsulation blocks are configured for LAPS and the protocol decapsulation blocks are configured for Byte-Synchronous HDLC (i.e., LAPS mode).

The procedure for changing the configuration of the encapsulation mode of the MAC is as follows; 1) place all the VT corresponding to the MAC in AIS; 2) perform a soft reset per channel by setting the TX_RESETSx register to 0x91; 3) change the configuration of the corresponding MAC; 4) clear the soft reset per channel by writing 0x00 in TX_RESETSx; 5) remove the AIS indication for all the VT corresponding to the MAC.

In the case of GFP linear frame mode, changing the configuration of the encapsulation mode of the MAC is as follows; 1) place all the VT corresponding to the VCG (assigned to several MAC) in AIS (see Note 1 below); 2) perform a soft reset per channel by setting the TX_RESETSx register to 0x91 to all the MAC involved in the VCG; 3) change the configuration of the corresponding MACs; 4) clear the soft reset per channel by writing 0x00 in TX_RESETSx; 5) remove the AIS indication for all the VT corresponding to the VCG.

The procedure for changing the configuration of the decapsulation mode of one VCG is as follows; 1) Perform a soft reset of the MAC corresponding to the VCG by setting to 1 the Reset Tx Function (bit TBD) (in the address TBD for the corresponding MAC); 2) perform a soft reset per channel by setting the RX_RESETSx register to 0x91; 3) change the configuration of the corresponding VCG; 4) clear the soft reset of the MAC by clearing the Reset Tx Function (bit TBD) (in the address TBD for the corresponding MAC); 5) clear the soft reset per channel by writing 0x00 in RX_RESETSx; 6) enable the MAC corresponding to the VCG.

In the case of GFP linear frame mode, changing the configuration of the decapsulation mode of one VCG is as follows; 1) Perform a soft reset of all the MAC corresponding to the VCG by setting to 1 the Reset Tx Function (bit TBD) (in the address TBD for these MACs); 2) perform a soft reset per channel by setting the RX_RESETSx register to 0x91 for all the corresponding MAC; 3) change the configuration of the corresponding VCG; 4) clear the soft reset of the MAC by clearing the Reset Tx Function (bit TBD) (in the address TBD for the corresponding MACs); 5) clear the soft reset per channel by writing 0x00 in RX_RESETSx for all the corresponding MAC; 6) enable all the MAC corresponding to the VCG.

GFP

Generic Framing Procedure (GFP) is a protocol for mapping packet data into an octet-synchronous transport such as SONET/SDH. Unlike HDLC-based protocols, GFP does not use any special characters for frame delineation. Instead, it uses a cell delineation protocol, such as used by ATM, to encapsulate variable length packets. A fixed amount of overhead is required by the GFP encapsulation that is independent of the contents of the packet size. The GFP protocol is specified in the ITU-T G.7041/Y.1303 standard.

Figure 49 shows the format of a GFP frame with a Ethernet MAC frame payload (denoted by the shaded area) relationship.

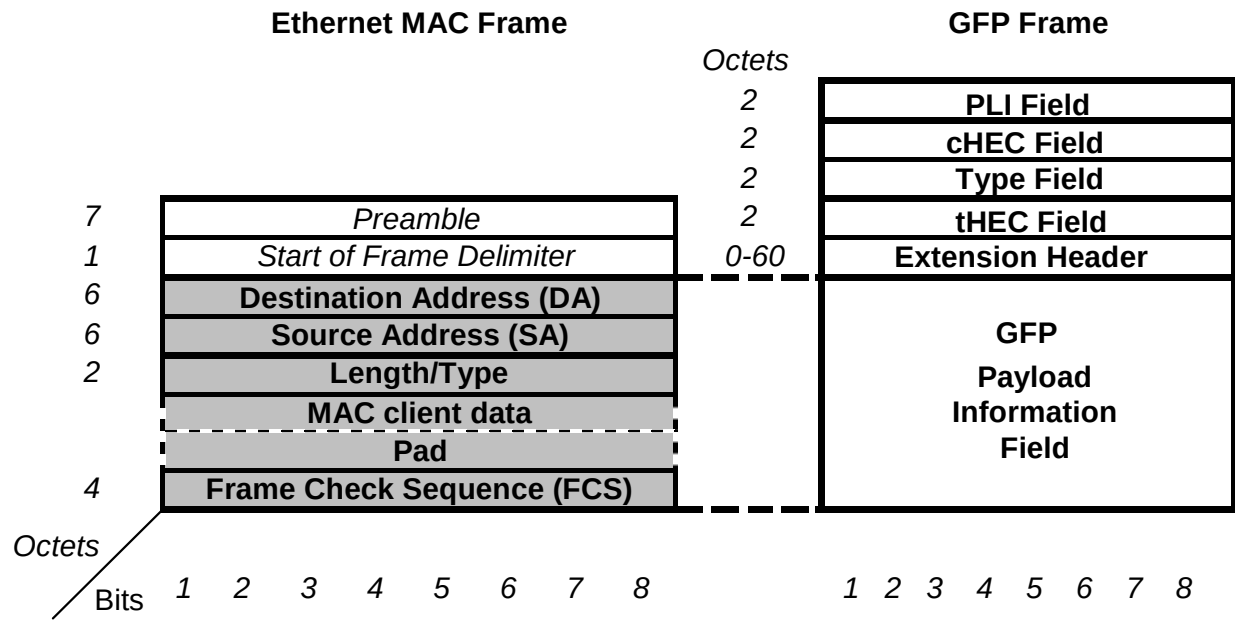


Figure 49. Format of GFP Frame with an Ethernet MAC Frame Payload

As shown in Figure 49, the GFP overhead can consist of two headers:

- A Core header, which consists of a two byte Payload Length Indicator (PLI) field and a two byte Core Header Error Control (cHEC) field. The Core header is used for frame delineation.
- A Payload header, which consists of a Type header and an Extension header (optional).
  - The Type header consists of a two byte Type field and a two byte Type Header Error Control (tHEC) field. The Type header is used to indicate the format and content of the Payload Information field. The EtherMap-12 device supports frame based mapping for Ethernet MAC frames only.
  - The Extension header used for managing logical links, classes of service and source/destination addresses. Two forms of Extension headers are supported: Null Extension Header and Linear Extension Header. For Null Extension header support, no additional Extension header bytes are required (as per ITU-T G.7041/Y.1303). For Linear Extension header support, four bytes are required in addition to the Type header. These consist of a one byte Channel ID (CID) field, a one byte Spare (reserved) field and a two byte Extension Header Error Control (eHEC) field.

As shown in Figure 49, the GFP Payload Information field is used to carry a complete Ethernet MAC frame. Further, an optional Payload FCS field (4 bytes) may be inserted after the GFP Payload Information field. The optional Payload FCS field contains a 32-bit CRC sequence that protects the contents of the GFP Payload Information field only.

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for GFP, the following functions are supported:

- Encapsulate Ethernet MAC frame within a GFP frame. Each Ethernet MAC frame is encapsulated with a Core header, a Payload header and an optional Payload FCS field. For the Core header, the PLI and the cHEC fields are generated. For the Type header within Payload header, the PTI, PFI, EXI, UPI and tHEC fields are generated and configurable.

cPTIx(2-0)	GFP Payload Type Identifier Field Configuration
0x0 - 0x7	Indicates contents of the PTI field for GFP Client Data frames only. (Default = 0x0)

cPFIx bit TBD	GFP Payload FCS Indicator Control
0	The PFI bit within the GFP Payload Header is set to zero (0). GFP Payload FCS field is not inserted. (Default)
1	The PFI bit within the GFP Payload Header is set to one (1). GFP Payload FCS field is inserted.

cEXIx(3-0)	GFP Extension Header Identifier Field Configuration
0x0 - 0xF	Indicates contents of the EXI field with in the GFP Payload header. (Default = 0x0)

cUPIx(7-0)	GFP User Payload Identifier Field Configuration
0x00 - 0xFF	Indicates contents of the UPI field for GFP Client Data frames only. (Default = 0x01)

For the Extension header (when in Linear frame mode) within Payload header, the CID, Spare and eHEC fields are generated and configurable.

cSPAREx (7-0)	GFP SPARE Field Configuration
0x00 - 0xFF	Indicates contents of the SPARE field within the GFP Extension header when using GFP Linear frame structure. (Default = 0x00)

cFECIDx (7-0)	GFP Channel ID (CID) Field Configuration
0x00 - 0xFF	Indicates contents of the CID field within the GFP Extension header when using GFP Linear frame structure. (Default = 0x00)

- GFP Core header scrambling can be enabled/disabled using the cTCSCRx register.

cTCSCRx bit TBD	GFP Core Header Scrambling Control
0	Enable scrambling of GFP Core Header only. (Default)
1	Disable scrambling of GFP Core Header only.

- GFP Client Data and Client Management frame formats are supported.
- GFP Idle frame generation and insertion is supported.
- Self-synchronous scrambler (x^{43} +1 polynomial) for the Payload header, Payload Information field and Payload FCS field (optional) can be enabled/disabled according using the cTPSCRDx register. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

cTPSCRDx bit TBD	GFP Payload Area Scrambling Control
0	Enable scrambling of GFP Payload area only. (Default)
1	Disable scrambling of GFP Payload area only.

cTSCRINITx bit TBD	GFP Payload Scrambler Initialization Control
0	Scrambler is initialized with an all zeros state. (Default)
1	Scrambler is initialized with an all ones state.

- 32-bit CRC sequence generation for the Payload FCS field (optional), over all octets of the GFP Payload Information field only, is supported.
- GFP frame multiplexing (when in Linear frame mode, cEXIx=1) from multiple Ethernet ports using a configurable scheduling algorithm is supported. For further details, please see the following section "GFP Linear Frame Mode Operation" on page 134.
- Detection and handling of errored Ethernet MAC frames on GFP ingress is supported. An alarm, aTETHERRx, is generated when an errored Ethernet MAC frame is detected and discarded for the transmit direction.
- Generation of GFP Client Signal Fail (CSF) indication is supported using the cTGFPTXCSFx register. The cTGFPTXCSFx allows to enter into the CSF mode (when set to 1). In that mode, every 100 ms, a CSF indication is transmitted to the line. The aTGFPCSFx alarm indicates the activation of this mode. To exit from this mode, the cTGFPTXCSFx must be cleared.

cTGFPTXCSFx bit TBD	GFP CSF Frame Transmit Control
0	Disable GFP CSF frame transmit mode. (Default)
1	Enable GFP CSF frame transmit mode. Beginning at the next GFP frame, a CSF indication is transmit every 100 ms period (i.e., no GFP Client Data frames can be transmitted). GFP Idle frames are transmitted in the interim.

- Ability to insert errors in cHEC, tHEC and eHEC fields for testing is configurable respectively using the cTCHECERRx, cTTHECERRx and cTEHECERRx registers (self-clearing type, i.e., error is inserted only in a single frame). Furthermore, the cHEC generator can be initialized to a default state using the cTHECINITIALx register.

cTCHECERRx bit TBD	GFP cHEC Error Insertion
0	Disable cHEC error insertion. (Default)
1	Enable cHEC error insertion. Error is inserted by inverting the calculated cHEC field before transmission.

cTTHECERRx bit TBD	GFP tHEC Error Insertion
0	Disable tHEC error insertion. (Default)
1	Enable tHEC error insertion. Error is inserted by inverting the calculated tHEC field before transmission.

cTEHECERRx bit TBD	GFP eHEC Error Insertion
0	Disable eHEC error insertion. (Default)
1	Enable eHEC error insertion. Error is inserted by inverting the calculated eHEC field before transmission.

cTHECINITIALx bit TBD	GFP cHEC Generator Initialization Control
0	cHEC generator is initialized with an all zeros state. (Default)
1	cHEC generator is initialized with an all ones state.

For each GFP frame byte that is input to the cHEC/tHEC/eHEC generator, the bit-order within the byte can be swapped/reversed using the cTHECSWAPINx register.

cTHECSWAPINx bit TBD	GFP cHEC/tHEC/eHEC Input Swap Control
0	For each GFP frame byte at the input of the cHEC/tHEC/eHEC generator, the bit-order is preserved (i.e., not swapped/reversed). (Default).
1	For each GFP frame byte at the input of the cHEC/tHEC/eHEC generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa).

For each GFP cHEC/tHEC/eHEC byte from the cHEC/tHEC/eHEC generator, the bit-order within the cHEC/tHEC/eHEC byte can be swapped/reversed using the cTHECSWAPOUTx register before transmission to SONET/SDH. This does not affect the cHEC/tHEC/eHEC calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

- Ability to force abort generation is configurable using the cTABTGx register.

cTHECSWAPOUTx bit TBD	GFP cHEC/tHEC/eHEC Output Swap Control
0	For each GFP cHEC/tHEC/eHEC byte that are output from the cHEC/tHEC/eHEC generator, the bit-order is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default).
1	For each GFP cHEC/tHEC/eHEC byte that are output from the cHEC/tHEC/eHEC generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH.

- Detection of FIFO overflow/underflow conditions and size (maximum) of GFP Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTGFPFMERRx alarm. The limit of the GFP Payload Information size is programmable using the register rTMAXFLx. The default value is 0x600. An alarm, aTGFPMAXERx, is generated when the size of the GFP Payload Information exceeds the value configured in rTMAXFLx register.

cTMAXFLx (15-0)	GFP Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in the GFP Payload Information field that is transmitted. (Default = 0x2800). When cPFIx=1, for a GFP payload length that exceeds the configured value in the cTMAXFLx register, the payload FCS is inverted before transmission to SONET/SDH. This will ensure that the terminating end discards the GFP frame. When cPFIx=0, for a GFP payload length that exceeds the configured value in the cTMAXFLx register, the current GFP payload is padded with 0xFF octets up to the configured length.

- Ability to insert GFP Client Management/Control frames by the Host is supported. A 128-byte buffer (using 128 rTCTL_x(8-0) registers) per MAC is provided to store a single GFP Client Management/Control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits TBD) is part of the GFP Client Management/Control frame. The Host must write a valid formatted (including overhead bytes) GFP Client Management/Control frame into the buffer such that only additional processing steps performed are: Core header scrambling and Payload area scrambling (note: if payload FCS is required then this is provided by the Host). The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a GFP Client Management/Control frame.
  - Step 2: Once the GFP Client Management/Control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the GFP Client Management/Control frame is ready for transmission.
  - Step 3: During the next GFP inter-frame window (i.e., after completion of the GFP frame currently being transmitted), the stored GFP Client Management/Control frame is inserted into the datapath for transmission to SONET/SDH.
  - Step 4: Once the GFP Client Management/Control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-12 and an alarm, aTCTLx, is generated. The alarm

can be used to provide an indication of the next available GFP Client Management/Control frame transmission.

sTCTLBx bit TBD	GFP Client Management/Control Frame Buffer Status Indication
0	Buffer is empty and is able to receive a new GFP Client Management/Control frame. (Default)
1	Buffer is full and is not able to receive a new GFP Client Management/Control frame.

cTCTLBRSTx bit TBD	GFP Client Management/Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

- Ability to filter mapping of select GFP frames for transmission to SONET/SDH is provided using cTGFPPDUx register. Transmission of all GFP Client Management/Control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of GFP frames (i.e., including GFP Client Management/Control frames) for transmission to SONET/SDH.

cTGFPPDUx bit TBD	Selective GFP Frame Mapping Filter Control
0	GFP frames are allowed to pass for mapping into SONET/SDH. (Default)
1	GFP frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH.

cTOFFx bit TBD	Generic GFP Frame Mapping Filter Control
0	All types of GFP frames (i.e., including GFP Client Management/Control frames) are allowed to pass for mapping into SONET/SDH. (Default))
1	All types of GFP frames (i.e., including GFP Client Management/Control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only GFP IDLE frames are mapped into SONET/SDH.

- Maintains transmit statistics counters. Two types of counters are provided: the total number of GFP frame payloads transmitted (rpcTGFPFRAMEx register) and the total number of GFP frame payload octets transmitted (rpcTGFPBYTEx register). These are also described in Table TBD.

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for GFP, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a GFP frame after frame delineation and sync is achieved. Robustness of GFP frame delineation acquisition using four virtual framers is configurable using the cRDELTAx register.

cRDELTAx (2-0)	GFP Re-synchronization Control
0x0 - 0x7	Indicates values of DELTA to be used in the GFP delineation process. (Default = 0x1)

- Processing of Null or Linear header types is configurable using the cRGFPHDRx register.

cRGFPHDRx bit TBD	GFP Header Type Processing Control
0	Only GFP NULL header type is processed. GFP frames received with other types of headers are discarded. (Default)
1	Only GFP LINEAR header type is processed. GFP frames received with other types of headers are discarded.

- Core header descrambling can be enabled/disabled using the cRCDSCRx register.

cRCDSCRx bit TBD	GFP Core Header De-scrambling Control
0	Enable de-scrambling of GFP Core Header only. (Default)
1	Disable de-scrambling of GFP Core Header only.

- Single-bit error detection and correction in the Core header, Type header and Extension header is configurable. Multiple-bit error detection in the Core header, Type header and Extension header is supported and these frames are discarded.

cRCORDISx bit TBD	GFP Core Header Single-bit Error Correction Control
0	For GFP Core header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default)
1	For GFP Core header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded.

cRTHECSx bit TBD	GFP Type Header Single-bit Error Correction Control
0	For GFP Type header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default)
1	For GFP Type header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded.

cREHECSx bit TBD	GFP Extension Header Single-bit Error Correction Control
0	For GFP Extension header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default)
1	For GFP Extension header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded.

- GFP Client Data and Client Management frame formats are supported.
- GFP Idle frame detection and discard is supported.
- Self-synchronous descrambler (x^{43} +1 polynomial) for the Payload header, Payload Information field and Payload FCS field (optional) can be enabled/disabled using the cRPSCRDx register.

cRPSCRDx bit TBD	GFP Payload Area De-scrambling Control
0	Enable de-scrambling of GFP Payload area only. (Default)
1	Disable de-scrambling of GFP Payload area only.

- 32-bit CRC sequence generation and checking for the Payload FCS field (optional), over all octets of the GFP Payload Information field only, is supported. An option is provided to pass or discard GFP frames with a FCS error using the cRGFPFCSERx register.

cRGFPFCSERx bit TBD	GFP FCS Check Handling
0	Received GFP frames detected with a Payload FCS error (when FCS is present) are discarded. (Default)
1	Received GFP frames detected with a Payload FCS error (when FCS is present) are not discarded.

- GFP frame demultiplexing (when in Linear frame mode) to multiple Ethernet ports based on configurable CID fields is supported. For further details, please see the following section "GFP Linear Frame Mode Operation" on page 134.
- Detection of GFP Client Signal Fail (CSF) indication is supported.
- Detection of size (maximum) of GFP Payload Information field via alarm and interrupt generation. The maximum size of the received GFP frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRGFPMAXERx, is generated when the size of the received GFP frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

GFP: Host Insertion/Extraction of Management/Control Frames

cRMAXFLx (15-0)	GFP Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in a received GFP frame Payload Information field not including the payload header and FCS bytes. (Default = 0x2800)

GFP HOST EXTRACTION OF MANAGEMENT/CONTROL FRAMES

- Ability to filter and extract GFP Client Management/Control frames by the Host is supported. A 520-byte buffer (using 520 rRLMIx_ (8-0) registers) per MAC is provided to store multiple GFP Client Management/Control frame for the Host extraction. LMI is an acronym for Local Management Interface. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the GFP Client Management/Control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a GFP Client Management/Control frame such that only the following processing have been performed: GFP frame delineation, Core header descrambling and Payload area descrambling. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLAVx status register and causes the 520 byte buffer to clear its present contents. The rRGFPCPx register is used to configure the Payload Header Type field value to be checked in order to extract the GFP Client Management/Control frame and the rRCTLMASKA1x register is used as a bit level mask that is applied to the cRGFPCPx register. Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sRCTLAVx=0 and the Host is not allowed to read for a new GFP Client Management/Control frame.
  - Step 2: Once the GFP Client Management/Control frame has been received, the sRCTLAVx status register is set (sRCTLAVx=1) by the EtherMap-12 to indicate that at least one GFP Client Management/Control frame is ready for extraction by the Host. Further Management/Control frames may be written into the buffer if received. If so, the sRCTLAVx bit will become set again. An alarm is provided (aRCTLOVF) to indicate the overflow of the 520-byte buffer.

sRCTLAVx bit TBD	GFP Client Management/Control Frame Buffer Status Indication
0	Buffer is empty and no complete GFP Client Management/Control frame has been received/stored. (Default)
1	Buffer is full with at least one complete GFP Client Management/Control frame received.

cRCTLBRSTx bit TBD	GFP Client Management/Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

rRGFPCPx(15-0)	GFP Client Management/Control frame Payload Header Type field Contents
0x0000 - 0xFFFF	Indicates contents of the GFP Client Management/Control frame Payload Header Type field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKA1 mask register. (Default = 0x8000) The structure of this register is as follows: PTI field value = Bits (15-13), PFI field value = Bit 12, EXI field value = Bits (11-8) and UPI field value = Bits (7-0).

rRCTLMASKA1x(15-0)	GFP Client Management/Control Frame Payload Header Type Field Contents Mask
0x0000 - 0xFFFF	Mask value that is applied to the rRGFPCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRGFPCPx register is used for filtering. (Default = 0xFFFF)

- Ability to filter decapsulation of select GFP frames that are received from SONET/SDH is provided using cRGFPPDUx register. Reception of all GFP Client Management/Control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

cRGFPPDUx bit TBD	Selective GFP Frame Decapsulation Filter Control
0	All GFP frame types received frames from SONET/SDH are allowed to be decapsulated.
1	Only GFP CSF and GFP Client Management/Control frames matching the rRGFPCPx register are allowed to be decapsulated. (Default)

- Maintains receive statistics counters. All GFP receive side statistic counters are described in Table TBD.

GFP LINEAR FRAME MODE OPERATION

This mode allows support for scenarios where traffic from multiple independent MAC ports can be transported within a single VCG on SONET/SDH. The use of this mode requires configuration for Linear Frame Extension Header (which is added to the transported GFP frame) and of the CID tables (which configure the EtherMap-12 for this operation).

Note that, for each VCG operating in GFP linear frame mode, the Extension Header field (EXI) within the GFP Payload header must be configured using the cEXI register for the transmit side. On the receive side, the cRGFPHDRx register must be configured to allow for correct processing of GFP Linear frames.

Transmit Side Linear Extension Header

The following registers are used for configuration inputs for the Transmit side Linear Extension Header bytes. These bytes are written in during system configuration, and are updated only in a static manner by Host processor.

SPARE field: for each MAC port, the cSPAREx register is used to configure the insertion value of the SPARE field within the Linear frame extension header.

Channel ID field (CID): For each MAC port, the cFECIDx register is used to configure the value of the CID field. This field will be common to all the frames transmitted from that MAC port; thus the contents of the cFECIDx register will represent the originating MAC port ID, when the frame is received by the far-end MAC port.

Transmit Side CID Configuration Tables

When a VCG operates in GFP linear mode, several MAC ports may be configured to be multiplexed into it.

For any VCG, the CIDTablex_0, CIDTablex_1, CIDTablex_2, CIDTablex_3, CIDTablex_4, CIDTablex_5, CIDTablex_6, CIDTablex_7 registers will allow configuration of specific MAC ports that will be multiplexed in that VCG.

These registers are only modified in a static manner by the Host upon initialization of the GFP link.

Note that the 8 MAC ports need not be all involved in the frame multiplexing process: for example, only a

subset of the 'n' Ethernet ports may be multiplexed in a given VCG.

The operation of the CIDTablex registers can be represented with a example scheduling matrix, shown in Table 3. This matrix is used to configure/control the multiplexing process for all the participating MAC ports configured for GFP Linear frame mode.

Table 3 shows an example configuration of the scheduling matrix.

The VCG are represented along the vertical axis; on horizontal axis, the matrix represents the MAC ports that a VCG will service.

Table 3: Scheduling Matrix

VCG0	1	3	1	2	2	3	1	1
VCG1	7	4	7	7	4	7	N	N
VCG2	N	N	N	N	N	N	N	N
VCG3	N	N	N	N	N	N	N	N
VCG4	N	N	N	N	N	N	N	N
VCG5	N	N	N	N	N	N	N	N
VCG6	N	N	N	N	N	N	N	N
VCG7	5	5	5	0	0	5	0	5

Scheduling Matrix Explanation:

1) The above matrix can be interpreted as follows:

- Transport path VCG0 (represented on the top row), will first transmit one frame from MAC1, then one frame from MAC3, then one frame from MAC1, then one frame from MAC2, then one frame from MAC2, then one frame from MAC3, then one frame from MAC1, then one frame from MAC1 etc. This cycle is continuously repeated.
- For transport path VCG 1, the MAC ports are serviced in this order: 7, 4, 7, 7, 4, 7, 4, 7, 7, 4, etc.
- For transport path VCG 2, there are no participating MAC ports.
- For transport path VCG 3, there are no participating MAC ports.
- For transport path VCG 4, there are no participating MAC ports.
- For transport path VCG 5, there are no participating MAC ports.
- For transport path VCG 6, there are no participating MAC ports.
- For transport path VCG 7, the MAC ports are serviced in this order: 5, 5, 5, 0, 0, 5, 0, 5, etc.

2) For each VCG row, each entry identifies the MAC port (configured for GFP Linear frame) to be serviced. Also, each entry represents only one complete Ethernet frame to be accepted each time into the multiplexing process.

3) 'N' represents a null value. The entries are read/serviced from left to right and wrap around to beginning of the cycle after servicing the last entry (i.e., entry number 7). A null value is used to terminate the servicing sequence order back to the first entry in the row (i.e., entry number 1). On initialization/power-up, all entries in the matrix are configured to a null value.

4) A null value cannot exist in the middle of the servicing sequence order (i.e., for example to be used to skip a service cycle). It is only allowed at the end of the servicing sequence order (see 2 above).

5) A MAC port is not used across/in multiple VCGs. However, within a single VCG, an Ethernet port is allowed multiple entries.

6) Only MAC ports configured for GFP Linear frame mode are allowed to participate in the scheduling matrix multiplexing process.

7) Ethernet port 3 is participating in the VCG 0 multiplexing process, this means that VCG 3 is only allowed to use other Ethernet ports if they are configured for GFP Linear Frame mode. No LAPS, LAPF or GFP NULL encapsulated Ethernet frames are allowed in VCG 3.

8) When operating in GFP Linear frame mode, the core header scrambling is performed by each of the separate MAC blocks before the GFP Linear frame is sent to the scheduling matrix for multiplexing.

9) When operating in GFP Linear frame mode, the payload scrambling is only performed after the GFP Linear frames have been multiplexed (as per the scheduling matrix) for each VCG separately.

10) Table 4 shows how the matrix is mapped in the EtherMap-12 register memory map.

Table 4: Scheduling Matrix Mapped in the EtherMap-12 Register Map

x = 0	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 1	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 2	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 3	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 4	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 5	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 6	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7
x = 7	CIDTablex_0	CIDTablex_1	CIDTablex_2	CIDTablex_3	CIDTablex_4	CIDTablex_5	CIDTablex_6	CIDTablex_7

Each register CIDTablex_n comprises of four bits:

The most significant bit, CIDTablex_n [3], indicates "entry active" (when set to '1') or "entry not active" (when set to '0').

The remaining least significant bits, CIDTablex_n [2-0], indicate the select MAC port.

Receive Side Linear Extension Header

The cRGFPHDRx register is used to configure the type of GFP Payload header (i.e., NULL or LINEAR) processing for the GFP receive side.

For the receive direction, the cLECIDx register is used to assign/configure a unique local-end CID number to each receive side MAC port. This is used for processing a match condition between the local-end CID number and the CID field of the received GFP linear frame.

cLECIDx (7-0)	GFP Local-end CID Value Configuration
0x00 - 0xFF	Indicates a unique local-end CID number assigned to a local receive Ethernet port. (Default = 0x00)

Receive Side CID Configuration Tables

For every VCG, operating in GFP Linear frame mode, being received from SONET/SDH side, there is a receive CID table using cRGFPCIDxi (where x = 0 - 7 GFP decapsulation blocks and i = 0 - 7 entries of the

receive CID table) registers. Each table can be configured with up to eight CID values, corresponding to a maximum of eight Ethernet ports. This enables a filtering function to be made on the received GFP frames by comparing their CID field values with the table of expected CID values.

Example:

If VCG0 receives a frame, the CID field is compared against all the CID values listed in cRGFPCID01, cRGFPCID02, cRGFPCID03, cRGFPCID04, cRGFPCID05, cRGFPCID06 and cRGFPCID07 registers.

After this check, one of the following will happen:

i) If CID value of the received frame matches any of CID values in the list, the frame is passed through, the Ethernet frame is decapsulated and forwarded to the local receive Ethernet port with the matching local-end CID number.

ii) For all received GFP linear frames with matching CID values, when a far end receive CSF indication is detected for a select CID value, an alarm, aRGFPFECSFCIDxi (where x = 0 - 7 VCG decapsulation blocks; i = 0 - 7 entries of the receive CID table), is generated for that CID value.

iii) When a match is not detected with the received GFP linear frame, the GFP frame is discarded and an alarm is generated. An alarm, aRGFPCIDERRx (where x = 0 - 7), is generated when the received GFP linear frame contains an unsupported CID value (i.e., a mismatch condition against the local end CID numbers).

Note that the order of the CID in the receive CID table is not important and that a CID number entry can only exist in once in the receive CID table for one given VCG (i.e., cannot have the same CID number entry exist in multiple tables). This check is performed by the software driver.

LAPS

LAPS is a HDLC-like framing structure to encapsulate IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The LAPS protocol is specified in the following standards: ITU-T X.85/Y.1321 and ITU-T X.86.

Figure 50 shows the format of a LAPS frame with a Ethernet MAC frame payload (denoted by the shaded area).

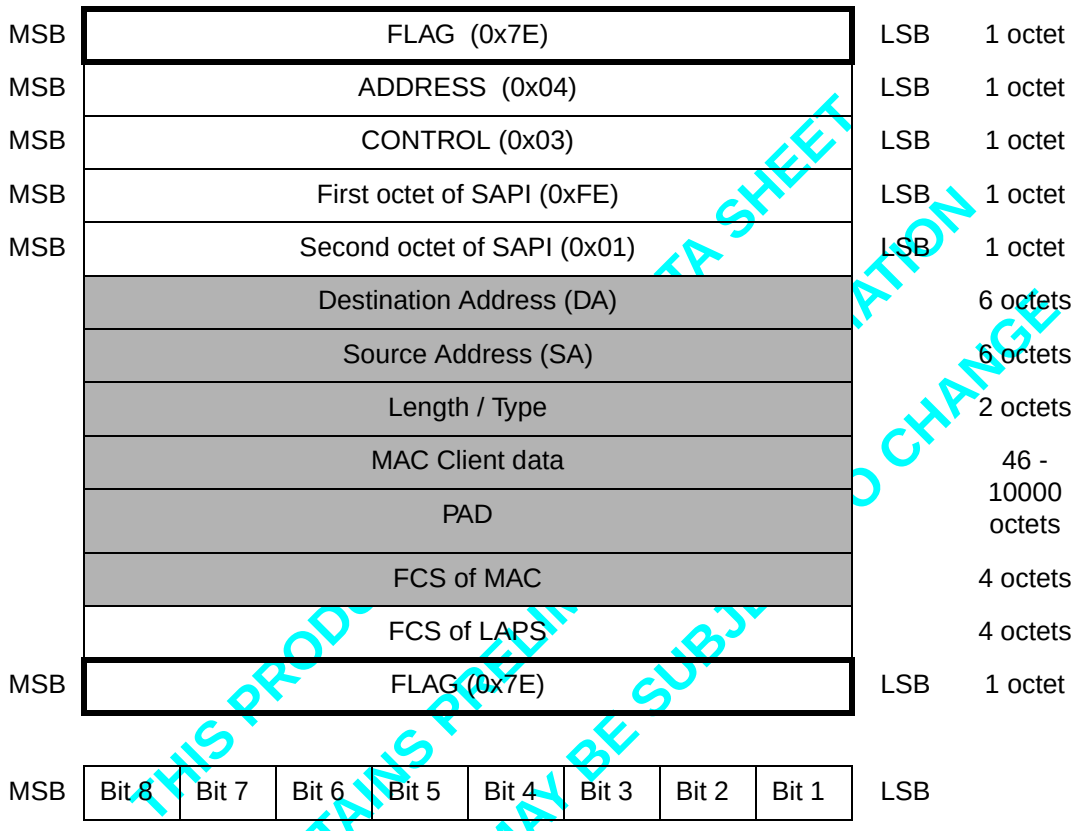


Figure 50. Format of LAPS Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for LAPS, the following functions are supported:

- Encapsulate Ethernet MAC frame within a LAPS frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), ADDRESS, CONTROL and SAPI fields, a 32-bit FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled through configuration. When field insertion is enabled, the contents of the ADDRESS, CONTROL and SAPI fields are configurable.

The management of the ADDRESS and CONTROL field is performed according to the cTACSELx register.

cTACSELx bit TBD	cTACSELx bit TBD	LAPS ADDRESS and CONTROL Field Insertion Management
0	0	ADDRESS and CONTROL field contents set to all zeros.
0	1	ADDRESS and CONTROL field contents contain fixed default values (i.e., ADDRESS=0x04, CONTROL=0x03). (Default).
1	0	Reserved.
1	1	ADDRESS and CONTROL field contents are taken from the rTACFDx register.

The management of the SAPI field is controlled by the cTSAPIx register.

cTSAPIx bit TBD	LAPS SAPI Field Insertion Management
0	SAPI field contents are taken from the rTSAPFDx register.
1	SAPI field contents set to all zeros.

- Shared flag (START and CLOSING) generation is configurable. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive LAPS frames.

cTFLAGx bit TBD	LAPS FLAG Insertion
0	A single flag are inserted between sequential LAPS frames (i.e., a shared flag).
1	Minimum of two flags are inserted between two consecutive LAPS frames. (Default).

- Self-synchronous scrambler (x^{43} +1 polynomial) can be enabled or disabled. The cTSCRDx register allows to enable/disable scrambling of LAPS frame. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

cTSCRDx bit TBD	LAPS Scrambling Control
0	Enable scrambling of LAPS frame. (Default)
1	Disable scrambling of LAPS frame.

cTSCRINITx bit TBD	LAPS Scrambler Initialization Control
0	Scrambler is initialized with an all zeros state. (Default)
1	Scrambler is initialized with an all ones state.

- 32-bit FCS generation over all bits of the ADDRESS, CONTROL, SAPI, Payload Information field (shaded area as shown in Figure 50) not including any Flags and Abort sequences, is configurable using the cTFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALLx register.

cTFCSx bit TBD	LAPS FCS Generation/Calculation Mode
0	32-bit FCS calculation is disabled and all four FCS field octets are not inserted.
1	32-bit FCS calculation is enabled and all four FCS field octets are inserted. (Default)

cTFCSINITIALLx bit TBD	LAPS FCS Generator Initialization Control
0	FCS generator is initialized with an all zeros state.
1	FCS generator is initialized with an all ones state. (Default)

For each LAPS FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

cTFCSSWAPINx bit TBD	LAPS FCS Input Swap Control
0	For each LAPS frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default).
1	For each LAPS frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator.

For each LAPS frame byte that is output from the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPOUTx register before it is transmitted to SONET/SDH.

cTFCSSWAPOUTx bit TBD	LAPS FCS Output Swap Control
0	For each LAPS FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default).
1	For each LAPS FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH.

- Transparency processing (octet stuffing for Flags and Control Escape) is supported. Byte stuffing occurs between START and CLOSING Flags. Stuffing replaces each byte within a LAPS frame that matches the Flag or Control Escape code bytes with a two-byte sequence.

- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

cTFCSEx bit TBD	LAPS FCS Error Insertion
0	The 32-bit FCS is transmitted without any error insertion. (Default)
1	The 32-bit FCS is errored (i.e., inverted) before transmission.

- Ability to force abort generation is configurable. The cTABTGx register allows to force (cTABTGx=1) the abortion of the current encapsulated frame by sending 0x7D and 0x7E bytes.

cTABTGx bit TBD	LAPS Transmit Abort Generation
0	No abort generated. (Default)
1	Current frame under transmission is aborted by 0x7D followed by 0x7E.

- Detection of FIFO overflow/underflow conditions and size (maximum) of LAPS Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTLPFERRx alarm. The limit of the LAPS Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTMAXERx, is generated when the size of the LAPS Payload Information field exceeds the value configured in rTMAXFLx register.

rTMAXFLx (15-0)	LAPS Payload Information Field Size
0x0000 - 0x2800	Indicates maximum number of octets in the LAPS Payload Information field that is transmitted. (Default = 0x2800)

- Ability to insert LAPS control frames by the Host is supported. A 128-byte buffer (using 128 rTCTL_x(8-0) registers) per MAC is provided to store a single LAPS control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPS control frame. The Host must write a valid formatted (including overhead bytes) LAPS control frame into the buffer such that only additional processing steps performed are: FCS calculation, Byte stuffing, addition of flags and scrambling. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a LAPS control frame.
  - Step 2: Once the LAPS control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the LAPS control frame is ready for transmission.
  - Step 3: During the next LAPS inter-frame window (i.e., after the closing flag of the preceding LAPS frame and before the opening flag of the following LAPS frame), the stored LAPS control frame is inserted into the datapath for transmission to SONET/SDH.
  - Step 4: Once the LAPS control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-12 and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available LAPS control frame transmission.

sTCTLBx bit TBD	LAPS Control Frame Buffer Status Indication
0	Buffer is empty and is able to receive a new LAPS control frame. (Default)

sTCTLBx bit TBD	LAPS Control Frame Buffer Status Indication
1	Buffer is full and is not able to receive a new LAPS control frame.

cTCTLBRSTx bit TBD	LAPS Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

- Ability to filter mapping of LAPS frames for transmission to SONET/SDH is provided using cTLPPDUx register. Transmission of all LAPS control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of LAPS frames (i.e., including LAPS control frames) for transmission to SONET/SDH.

cTLPPDUx bit TBD	LAPS Frame Mapping Filter Control
0	LAPS frames are allowed to pass for mapping into SONET/SDH. (Default)
1	LAPS frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH.

cTOFFx bit TBD	Generic LAPS Frame Mapping Filter Control
0	All types of LAPS frames (i.e., including LAPS control frames) are allowed to pass for mapping into SONET/SDH. (Default)
1	All types of LAPS frames (i.e., including LAPS control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH.

- Maintains transmit statistics counters. Two types of counters are provided: the total number of LAPS frame payloads transmitted (rpcTLAPSFRAMEx register) and the total number of LAPS frame payload octets transmitted (rpcTLAPSBYTEx register) to SONET/SDH. These are also described in Table TBD.

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for LAPS, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a LAPS frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of the ADDRESS, CONTROL and SAPI fields of a received LAPS frame are validated against configurable stored values. Further, an option to discard frames with a mismatch of one of the fields, is configurable.
  The cRACSELx(1:0) register allows to configure the type of check to be performed on the ADDRESS and CONTROL field contents.

cRACSELx bit TBD	cRACSELx bit TBD	LAPS ADDRESS and CONTROL Field Contents Check Control
0	0	ADDRESS and CONTROL field contents check is disabled. Assume ADDRESS and CONTROL fields are present.
0	1	ADDRESS and CONTROL field contents checked against fixed values (i.e., ADDRESS=0x04, CONTROL=0x03). (Default).
1	0	Reserved.
1	1	ADDRESS and CONTROL field contents checked against the contents of rRACFDx register.

The cRSAPIx register allows to configure the type of check to be performed on the SAPI field contents.

cRSAPIx bit TBD	LAPS SAPI Field Contents Check Control
0	SAPI field contents check is disabled.
1	SAPI field contents checked against the contents of rRSAPFDx register. (Default)

The cRMMAEx register allows to configure handling of LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents. An alarm, aRLPSFMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL or SAPI field contents of the received LAPS frame.

cRMMAEx bit TBD	LAPS Field Contents Mismatch Management
0	LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is discarded. (Default)
1	LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is not discarded

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRFLAGx register allows to configure the type of flag detection between consecutive LAPS frames.

cRFLAGx bit TBD	LAPS FLAG Detection Control
0	At least two flags to be detected between LAPS frames. (Default).
1	At least a single flag to be detected between LAPS frames (i.e., a shared flag).

- Self-synchronous de-scrambler (x^{43} +1 polynomial) can be enabled or disabled according to the cRSCRDx register.

cRSCRDx bit TBD	LAPS Descrambling Control
0	Enable descrambling of LAPS frame. (Default)
1	Disable descrambling of LAPS frame.

- 32-bit FCS generation and checking over all bits of the ADDRESS, CONTROL, SAPI, Payload Information field (shaded area as shown in Figure 50) not including any Flags and Abort sequences, is configurable. The cRFCS register allows to configure enable/disable LAPS FCS checking. Further, an option is provided to process or discard LAPS frames with a FCS error according to the cRLPFCSERx register. An alarm, aRLPSFCSER, is generated when a LAPS frame is received with FCS error.

cRFCSx bit TBD	LAPS FCS Check
0	32-bit FCS check is disabled and assume all four FCS field octets are not present.
1	32-bit FCS check is enabled. (Default)

cRLPFCSERx bit TBD	LAPS FCS Check Handling (used when FCS Check is Enabled as per cRFCSx Register)
0	Received LAPS frames with FCS error are discarded. (Default)
1	Received LAPS frames with FCS error are not discarded.

For each received LAPS frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

cRFCSSWAPINx bit TBD	LAPS FCS Input Swap Control
0	For each received LAPS frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default).
1	For each received LAPS frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa).

- Transparency processing (octet de-stuffing for Flags and Control Escape) is supported. Byte de-stuffing occurs between START and CLOSING Flags.
- Ability to detect an abort indication via alarm and interrupt generation. To force an abort of the current frame, the cRLPABTGx register needs to set to 1. An alarm, aRLPSABTDx, is generated when an abort indication is detected (i.e., receive 0x7D followed by 0x7E) on the receive side.

cRLPABTGx bit TBD	LAPS Abort Generation
0	No frame aborted. (Default)
1	Current frame under receive is aborted.

- Processing of invalid LAPS frames as per ITU-T X.86.
- Detection of size (minimum and maximum) of LAPS Payload Information field via alarm and interrupt generation. The minimum size of the received LAPS frame (in octets) can be configured using the rRLPMINFLx register (i.e., the number of octets between the opening and closing flags). An alarm, aRLPSSHTERx, is generated when the size of received LAPS frame is less than six octets and this frame is aborted. An alarm, aRLPSMINERx, is generated when the size of the received LAPS frame is greater than six octets but less than the value configured in rRLPMINFLx register. The maximum size of the received LAPS frame Payload

Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRLPSMAXERx, is generated when the size of the received LAPS frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

rRLPMINFLx(7-0)	LAPS Frame Size
0x06 - 0xFF	Indicates minimum number of octets present in a received LAPS frame between opening and closing flags. (Default = 0x06)

rRMAXFLx(15-0)	LAPS Frame Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in a received LAPS frame Payload Information field. (Default = 0x2800)

- Ability to filter and extract LAPS control frames by the Host is supported. A 64-byte buffer (using 64 rRLMIx_(8-0) registers) per MAC is provided to store a single LAPS control frame for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPS control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a LAPS control frame such that only the following processing have been performed: FCS Check, Byte de-stuffing and removal of flags. The sRCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLBx status register (sRCTLBx=0) and enable a new Management/Control frame to be received. The rRLPCPx register is used to configure the SAPI value to be checked in order to extract the LAPS control frame and the rRCTLMASKA1x register is used as a bit level mask that is applied to the cRLPCPx register. Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sRCTLBx=0 and the Host is not allowed to read for a new LAPS control frame.
  - Step 2: Once the LAPS control frame has been received, the sRCTLBx status register is set (sRCTLBx=1) by the EtherMap-12 and an alarm, aRCTLRXx, is generated to indicate that the present LAPS control frame is ready for extraction by the Host. No further LAPS control frames may be written into the buffer (i.e., are discarded silently) until the sRCTLBx status register is cleared. If the received LAPS control frame is bigger than the buffer size, an alarm, aRCTLBERRx, is generated and the buffer must be cleared/reset by the Host.
  - Step 3: Once the LAPS control frame has been extracted, the sRCTLBx status register is cleared (sRCTLBx=0) by the Host. This is to indicate that a follow-on received LAPS control frame may be written into the buffer.

sRCTLBx bit TBD	LAPS Control Frame Buffer Status Indication
0	Buffer is empty and no new LAPS control frame has been received/stored. (Default)
1	Buffer is full with a new LAPS control frame received.

cRCTLBRSTx bit TBD	LAPS Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

rRLPCPx(15-0)	LAPS Control Frame SAPI Field Contents
0x0000 - 0xFFFF	Indicates contents of the LAPS control frame SAPI field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKA1 mask register. (Default = 0x0000)

rRCTLMASKA1x(15-0)	LAPS Control Frame SAPI Field Contents Mask
0x0000 - 0xFFFF	Mask value that is applied to the rRPLCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPLCPx register is used for filtering. (Default = 0xFFFF)

- Ability to filter decapsulation of select LAPS frames (i.e., frames with SAPI field contents equal to rRSAPFDx register) that are received from SONET/SDH is provided using cRLPPDUx register. Reception of all LAPS control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

cRLPPDUx bit TBD	Selective LAPS Frame Decapsulation Filter Control
0	Received frames from SONET/SDH, with SAPI field contents equal to rRSAPFDx register, are allowed to be decapsulated.
1	Received frames from SONET/SDH, with SAPI field contents equal to rRSAPFDx register, are not allowed (i.e., frames are discarded) to be decapsulated. (Default)

- Maintains receive statistics counters. All LAPS receive side statistic counters are described in Table TBD.

LAPF

LAPF is a HDLC-like framing structure to encapsulate an IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The LAPF protocol is specified in the ITU-T Q.922 standard. Use of LAPF for transport of Ethernet MAC frames is specified in RFC2427. The EtherMap-12 device only supports LAPF Bridged frame format.

Figure 51 shows the format of a LAPF Bridged frame with a Ethernet MAC frame payload (denoted by the shaded area).

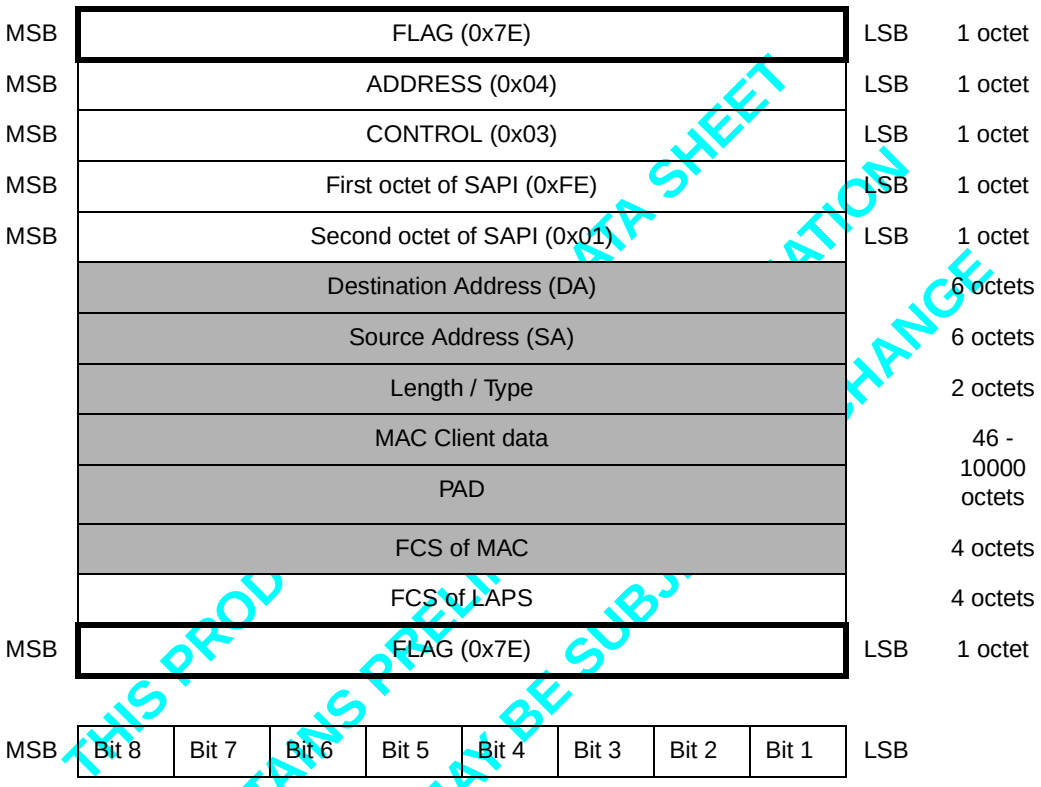


Figure 51. Format of LAPF Bridged Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for LAPF, the following functions are supported:

- Encapsulate Ethernet MAC frame within a LAPF frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields, a 16-bit FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled through configuration according to the cTLFACNOPSELx register. The insertion of the PAD field is also configurable using the cTLFPADx register. When other field insertion is enabled, the contents of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields are configurable according to the registers described into the Table TBD.

cTLFACNOPSELx bit TBD	LAPF ADDRESS, CONTROL, NLPID, OUI and PID Field Insertion Management
0	LAPF overhead field content insertion is enabled. (Default) ADDRESS field contents taken from rTDLCIx, cTCRx, cTFECNx, cTBECNx and cTDEx registers. CONTROL field contents taken from rTLFCNTLx register. NLPID field contents taken from rTNLPIDx register. OUI field contents taken from rTOUIx register. PID field contents taken from rTPIDx register.
1	ADDRESS, CONTROL, NLPID, OUI and PID field contents insertion is disabled. These fields are all set to zero.

cTLFPADx bit TBD	LAPF PAD Field Insertion Management
0	PAD field insertion is enabled and the field contents are taken from the rTPADn register. (Default)
1	PAD field insertion is disabled (i.e., no PAD field is present in the LAPF frame).

- Shared flag (START and CLOSING) generation is configurable according to the cTFLAGx register. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive LAPF frames
- 16-bit FCS generation over all bits of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI, PID and Payload Information fields (shaded area as shown in Figure 51) not including any Flags and Abort sequences, is configurable using the cTFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALLx register.

cTFCSx bit TBD	LAPF FCS Generation/Calculation Mode
0	16-bit FCS calculation is disabled and all FCS field octets are not inserted.
1	16-bit FCS calculation is enabled and all FCS field octets are inserted. (Default)

cTFCSINITIALLx bit TBD	LAPF FCS Generator Initialization Control
0	FCS generator is initialized with an all zeros state.
1	FCS generator is initialized with an all ones state. (Default)

For each LAPF frame byte that is input to the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPINx register.

cTFCSSWAPINx bit TBD	LAPF FCS Input Swap Control
0	For each LAPF frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default).

cTFCSSWAPINx bit TBD	LAPF FCS Input Swap Control
1	For each LAPF frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator.

For each LAPF FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

cTFCSSWAPOUTx bit TBD	LAPF FCS Output Swap Control
0	For each LAPF FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default).
1	For each LAPF FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH.

- Ability to insert LAPF LMI control frames by the Host is supported. A 128-byte buffer (using 128 rTCTL_x(8-0) registers) per MAC is provided to store a single LAPF LMI control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPF LMI control frame. The Host must write a valid formatted (including overhead bytes) LAPF LMI control frame into the buffer such that only additional processing steps performed are: FCS calculation, Bit stuffing and addition of flags. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a LAPF LMI control frame.
  - Step 2: Once the LAPF LMI control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the LAPF LMI control frame is ready for transmission.
  - Step 3: During the next LAPF inter-frame window (i.e., after the closing flag of the preceding LAPF frame and before the opening flag of the following LAPF frame), the stored LAPF LMI control frame is inserted into the datapath for transmission to SONET/SDH.
  - Step 4: Once the LAPF LMI control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-12 and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available LAPF LMI control frame transmission.

sTCTLBx bit TBD	LAPF LMI Control Frame Buffer Status Indication
0	Buffer is empty and is able to receive a new LAPF LMI control frame. (Default)
1	Buffer is full and is not able to receive a new LAPF LMI control frame.

cTCTLBRSTx bit TBD	LAPF LMI Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

- Ability to filter mapping of LAPF frames for transmission to SONET/SDH is provided using cTLFPDUx register. Transmission of all LAPF LMI control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of LAPF frames (i.e., including LAPF LMI control frames) for transmission to SONET/SDH.

cTLFPDUx bit TBD	LAPF Frame Mapping Filter Control
0	LAPF frames are allowed to pass for mapping into SONET/SDH. (Default)
1	LAPF frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH.

cTOFFx bit TBD	Generic LAPF Frame Mapping Filter Control
0	All types of LAPF frames (i.e., including LAPF LMI control frames) are allowed to pass for mapping into SONET/SDH. (Default)
1	All types of LAPF frames (i.e., including LAPF LMI control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH.

- Transparency processing (bit-stuffing for Flags and Control Escape) is supported. Bit stuffing occurs between START and CLOSING Flags.
- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

cTFCSEx bit TBD	LAPF FCS Error Insertion
0	The 16-bit FCS is transmitted without any error insertion. (Default)
1	The 16-bit FCS is errored (i.e., inverted) before transmission.

- Detection of FIFO overflow/underflow conditions and size (maximum) of LAPF Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTLFFERRx alarm. The limit of the LAPF Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTLFMAXERx, is generated when the size of the LAPF Payload Information field exceeds the value configured in rTMAXFLx register.

rTMAXFLx(15-0)	LAPF Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in the LAPF Payload Information field that is transmitted. (Default = 0x2800)

- Maintains transmit statistics counters. Two types of counters are provided: the total number of LAPF frame payloads transmitted (rpcTLAPFFRAMEx register) and the total number of LAPF frame payload octets transmitted (rpcTLAPFBYTEx register) to SONET/SDH. These are also described in Table TBD.

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for LAPF, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a LAPF frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields of a received LAPF frame are validated against configurable stored values. The cRLFACNOPSELx register allows to configure the type of check to performed on the ADDRESS and CONTROL and NLPID and OUI and PID field contents.

cRLFACNOPSELx bit TBD	LAPF ADDRESS, CONTROL, NLPID, OUI and PID Field Insertion Management
0	LAPF overhead field content checking is enabled. (Default) ADDRESS field contents are checked against rRLFADRx register. CONTROL field contents are checked against rRLFCNTLx register. NLPID field contents are checked against rRNLPIDx register. OUI field contents are checked against rROUIx register. PID field contents are checked against rRPIDx register. Register rRPIDx is configured to indicate whether the Ethernet frame FCS is present or not. When rRPIDx=0x0001, the Ethernet frame FCS is present and this Ethernet frame is transmitted onto the Ethernet line. When rRPIDx=0x0007, the Ethernet frame FCS is not present and a new Ethernet FCS (4-bytes) is generated and appended by the MAC before the frame is transmitted onto the Ethernet line.
1	ADDRESS, CONTROL, NLPID, OUI and PID field contents checking is disabled.

The cRLFPADx register allows to configure the type of check to performed on the PAD field contents.

cRLFPADx bit TBD	LAPF PAD Field Insertion Management
0	LAPF PAD field contents checking is enabled for only one PAD field in the received LAPF frame. (Default). The PAD field contents are checked against rRPADx register.
1	LAPF PAD field contents checking is disabled. Assume no PAD field is present in the received LAPF frame.

The cRLFMMAEx register allows to configure handling of LAPF frames with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents. An alarm, aRLFMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents of the received LAPF frame.

cRLFMMAEx bit TBD	LAPF Field Contents Mismatch Management
0	LAPF frame with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents is discarded. (Default)
1	LAPS frame with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents is not discarded

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRLFFLAGx register allows to configure the type of flag detection between consecutive LAPF frames.

cRLFFLAGx bit TBD	LAPF FLAG Detection
0	At least two flags to be detected between LAPF frames. (Default).
1	At least a single flag to be detected between LAPF frames (i.e., a shared flag).

- 16-bit FCS generation and checking over all bits of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI, PID and Payload Information fields (shaded area as shown in Figure 51) not including any Flags and Abort sequences, is configurable using the cRLFFCSx register. Further, an option is provided to process or discard LAPF frames with a FCS error using the cRLFFCSERx register. An alarm, aRLFFCSERx, is generated when a LAPF frame is received with FCS error.

cRLFFCSx bit TBD	LAPF FCS Check
0	16-bit FCS check is disabled and assume all two FCS field octets are not present.
1	16-bit FCS check is enabled. (Default)

cRLFFCSERx bit TBD	LAPF FCS Check Handling (used when FCS Check is Enabled as per cRLFFCSx Register)
0	Received LAPF frames with FCS error are discarded. (Default)
1	Received LAPF frames with FCS error are not discarded.

- For each received LAPF frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

cRFCSSWAPINx bit TBD	LAPF FCS Input Swap Control
0	For each received LAPF frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default).
1	For each received LAPF frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa).

- Transparency processing (bit de-stuffing for Flags and Control Escape) is supported. Bit de-stuffing occurs between START and CLOSING Flags.

- Ability to filter and extract LAPF LMI frames by the Host is supported. A 520-byte buffer (using 520 rRLMIx_(8-0) registers) per MAC is provided to store multiple LAPF LMI buffer for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPF LMI frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a LAPF LMI frame such that only the following processing have been performed: FCS Check, Bit de-stuffing and removal of flags. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLAVx status register and causes the 520-byte buffer to clear its present contents. The cRLMIDLCIx register allows to determine the DLCI field value to be checked in order to extract the LAPF LMI frame. Below is an example of how the Host can use this buffer:
  - Step 1: If the LMI buffer is empty, sRCTLAVx=0 and the Host is not allowed to read for a new LAPF LMI frame.
  - Step 2: Once the LAPF LMI frame has been received, the sRCTLAVx status register is set (sRCTLAVx=1) by the EtherMap-12 to indicate that at least one LAPF LMI frame is ready for extraction by the Host. Further LAPF LMI frames may be written into the buffer if received. If so, the sRCTLAVx bit will become set again. An alarm is provided (aRCTLOVF) to indicate the overflow of the 520-byte buffer.

sRCTLAVx bit TBD	LAPF LMI Frame Buffer Status Indication
0	Buffer is empty and no complete LAPF LMI frame has been received/stored. (Default)
1	Buffer is full with at least one complete LAPF LMI frame received.

cRCTLBRSTx bit TBD	LAPF LMI Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

cRLMIDLCIx bit TBD	LAPF LMI DLCI Field Value Selection
0	LAPF LMI frames with DLCI=0 are filtered for extraction by the Host. (Default)
1	LAPF LMI frames with DLCI=1023 are filtered for extraction by the Host.

- Ability to detect an abort indication via aRLFABTDx alarm and interrupt generation.
- Processing of invalid LAPF frames as per ITU-T Q.922.
- Detection of size (minimum and maximum) of LAPF Payload Information field via alarm and interrupt generation. The minimum size of the received LAPF frame (in octets) can be configured using the rRLFMINFLx register (i.e., the number of octets between the ADDRESS field and closing flag). An alarm, aRLFFSERx, is generated when the size of received LAPF frame is less than three octets (between ADDRESS field and closing flag) and this frame is aborted. An alarm, aRLFMINERx, is generated when the size of the received LAPF frame is greater than three octets but less than the value configured in rRLFMINFLx register. The maximum size of the received LAPF frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRLFMAXERx, is generated when the size of the received LAPF frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

rRLFMINFLx(7-0)	LAPF Frame Size
0x03 - 0xFF	Indicates minimum number of octets present in a received LAPF frame between ADDRESS field and closing flag. (Default = 0x06)

rRMAXFLx(15-0)	LAPF Frame Payload Information Field Size
0x0001 - 0x0640	Indicates maximum number of octets in a received LAPF frame Payload Information field. (Default = 0x0640)

- Provide an indication on the status of the LAPF link for the receive side. The sLNKSTSx status register is used by the Host to determine the state of the LAPF link. After power-up/reset, the LAPF link is set to a 'down' state. While the link is in a 'down' state, only LAPF flags and LMI frames are allowed to be received, Furthermore, while in a 'down' state, when either 64 consecutive LAPF flags or a single valid LAPF frame are received, the link state is set to an 'up' state. An alarm, aLNKSTSUPx, is generated to indicate a change of LAPF link to an 'up' state. While the link is in 'up' state, when 256 consecutive '1's are received, the link state is set to a 'down' state. An alarm, aLNKSTSDWNx, is generated to indicate a change of LAPF link to a 'down' state.
- Ability to filter decapsulation of LAPF frames that are received from SONET/SDH is provided using cRLFPDUx register. Reception of all LAPF LMI frames (i.e., control frames destined for extraction by Host) are not affected by this register.

cRLFPDUx bit TBD	Selective LAPF Frame Decapsulation Filter Control
0	All LAPF frame types received frames from SONET/SDH are allowed to be decapsulated.
1	Only LAPF LMI frames matching the cRLMIDLCIx register are allowed to be decapsulated. (Default)

- Maintains receive statistics counters. All LAPF receive side statistic counters are described in Table TBD.

PPP (WITH BCP AND LCP SUPPORT)

The Point-to-Point Protocol (PPP) is a HDLC-like framing structure and provides a standard method for transporting multi-protocol datagrams over point-to-point links. PPP can be used to encapsulate IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The PPP Bridging Control Protocol (BCP) is specified in the following standards: RFC 1661, RFC 1662, RFC 2878 and RFC 2615.

Figure 52 shows the format of a PPP frame with an Ethernet MAC frame payload (denoted by the shaded area).

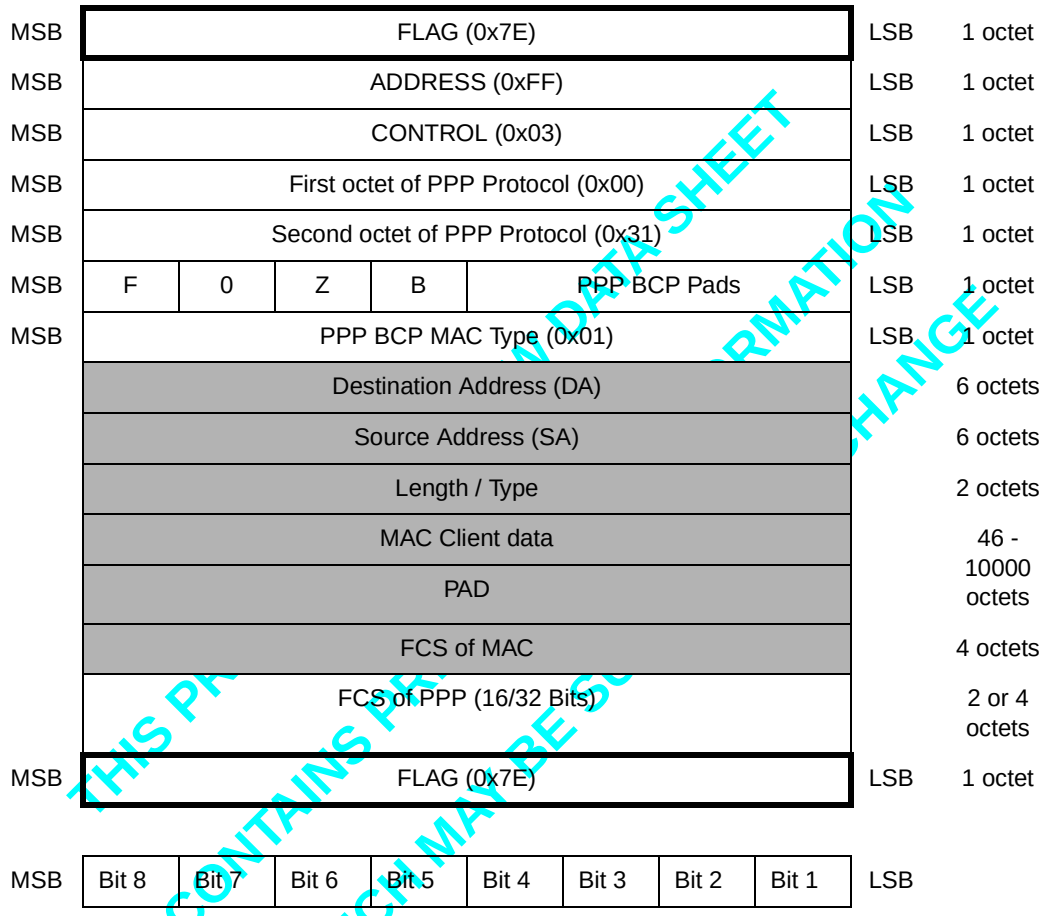


Figure 52. Format of PPP Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for PPP, the following functions are supported:

- Encapsulate Ethernet MAC frame within a PPP frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), ADDRESS, CONTROL, PPP Protocol, PPP BCP Flags, PPP BCP Pad and PPP BCP MAC Type fields, a 16/32-bit PPP FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled via configuration. When field insertion is enabled, the contents of the ADDRESS, CONTROL, PPP Protocol and PPP BCP MAC Type fields are configurable.

  The management of the ADDRESS and CONTROL field is performed according to the cTPPACSELx register.

cTPPACSELx bit TBD	cTPPACSELx bit TBD	PPP ADDRESS and CONTROL Field Insertion Management
0	0	ADDRESS and CONTROL field contents set to all zeros.
0	1	ADDRESS and CONTROL field contents contain fixed default values (i.e., ADDRESS=0xFF, CONTROL=0x03). (Default).
1	0	Reserved.
1	1	ADDRESS and CONTROL field contents are taken from the rTPPACFDx register.

The management of the PPP Protocol field is controlled by the cTPPPIx register.

cTPPPIx bit TBD	PPP Protocol Field Insertion Management
1	PPP Protocol field contents set to all zeros.
0	PPP Protocol field contents are taken from the rTPPFDx register. (Default)

The management of the PPP BCP flag fields (i.e., F, 0, Z, B fields) is performed according to the following registers: cTBCPFLGFx, cTBCPFLG0x, cTBCPFLGZx and cTBCPFLGBx.

cTBCPFLGFx bit TBD	PPP BCP Flag F Field Insertion Management
1	PPP BCP Flag F field contents set to a one (‘1’). (Default)
0	PPP BCP Flag F field contents set to a zero (‘0’).

cTBCPFLG0x bit TBD	PPP BCP Flag 0 Field Insertion Management
1	PPP BCP Flag 0 field contents set to a one (‘1’).
0	PPP BCP Flag 0 field contents set to a zero (‘0’). (Default)

cTBCPFLGZx bit TBD	PPP BCP Flag Z Field Insertion Management
1	PPP BCP Flag Z field contents set to a one (‘1’). (Default)
0	PPP BCP Flag Z field contents set to a zero (‘0’).

cTBCPFLGBx bit TBD	PPP BCP Flag B Field Insertion Management
1	PPP BCP Flag B field contents set to a one (‘1’).
0	PPP BCP Flag B field contents set to a zero (‘0’). (Default)

The contents of the PPP BCP MAC Type field is configurable using the rTBCPMACx register.

rTBCPMACx (15-8)	PPP BCP MAC Type Field Contents Configuration
0x00 - 0xFF	Indicates contents of the PPP BCP MAC Type field. (Default = 0x01)

- PPP padding mode to be applied is configurable. The rTBCPPDMODEx register allows to configure the type of padding mode to be used.

rTBCPPDMODEx bit TBD	rTBCPPDMODEx bit TBD	PPP Padding Mode Control
0	0	No padding is applied. (Default)
0	1	A fixed padding mode is enabled. In this mode, the PPP BCP PADS field is inserted to indicate the number of pad octets that have been inserted within the PPP frame payload.
1	0	Reserved.
1	1	Reserved.

The PPP padding octet alignment mode (i.e., used when fixed padding mode is enabled) is controlled by the rTBCPPDALIGNx register.

rTBCPPDALIGNx bit TBD	rTBCPPDALIGNx bit TBD	PPP Padding Octet Alignment Mode Control
0	0	A 2 octet alignment boundary is used. (Default)
0	1	A 4 octet alignment boundary is used.
1	0	A 8 octet alignment boundary is used.
1	1	A 16 octet alignment boundary is used.

The PPP padding octet alignment calculation mode (i.e., used when fixed padding mode is enabled) is controlled by the cTBCPPDCALCx register.

cTBCPPDCALCx bit TBD	PPP Padding Octet Alignment Calculation Mode Control
0	PPP padding octet alignment calculation is over payload area only. (Default).
1	PPP padding octet alignment calculation is over entire frame area. (i.e., header, payload and FCS bytes)

The contents of the PPP pad octet (i.e., used when fixed padding mode is enabled) is configurable using the rTBCPPADx register.

rTBCPPADx (7-0)	PPP Pad Field Contents Configuration
0x00 - 0xFF	Indicates contents of the PPP pad octet when fixed padding mode is enabled. (Default = 0x00)

- Shared flag (START and CLOSING) generation is configurable. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive PPP frames.

cTFLAGx bit TBD	PPP FLAG Insertion
0	A single flag are inserted between sequential PPP frames (i.e., a shared flag).
1	Minimum of two flags are inserted between two consecutive PPP frames. (Default).

- Self-synchronous scrambler (x^{43} +1 polynomial) can be enabled or disabled. The cTSCRDx register allows to enable/disable scrambling of PPP frame. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

cTSCRDx bit TBD	PPP Scrambling Control
0	Enable scrambling of PPP frame. (Default)
1	Disable scrambling of PPP frame.

cTSCRINITx bit TBD	PPP Scrambler Initialization Control
0	Scrambler is initialized with an all zeros state. (Default)
1	Scrambler is initialized with an all ones state.

- 16 or 32-bit FCS generation over all bits of the ADDRESS, CONTROL, PPP Control, PPP BCP Flags, PPP BCP Pads, PPP BCP MAC Type, Payload Information area (shaded area as shown in Figure 52) and optional pad octet fields not including any Opening/Closing flags and Abort sequences, is configurable using the cTPFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALLx register.

cTPFCSx bit TBD	cTPFCSx bit TBD	PPP FCS Generation/Calculation Mode
0	0	16 and 32-Bit FCS generation/calculation is disabled. FCS octets are not inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH.
0	1	Reserved.

cTPFCSx bit TBD	cTPFCSx bit TBD	PPP FCS Generation/Calculation Mode
1	0	Only 16 FCS generation/calculation is enabled. Two FCS octets are inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH.
1	1	Only 32 FCS generation/calculation is enabled. Four FCS octets are inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH. (Default)

cTFCSINITIALLx bit TBD	PPP FCS Generator Initialization Control
0	FCS generator is initialized with an all zeros state.
1	FCS generator is initialized with an all ones state. (Default)

For each PPP frame byte that is input to the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPINx register.

cTFCSSWAPINx bit TBD	PPP FCS Input Swap Control
0	For each PPP frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default).
1	For each PPP frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator.

For each PPP FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

cTFCSSWAPOUTx bit TBD	PPP FCS Output Swap Control
0	For each PPP FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default).
1	For each PPP FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH.

- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

cTFCSEx bit TBD	PPP FCS Error Insertion
0	The 16 or 32-bit FCS is transmitted without any error insertion. (Default)
1	The 16 or 32-bit FCS is errored (i.e., inverted) before transmission.

- Transparency processing (octet stuffing for Flags and Control Escape) is supported. Byte stuffing occurs between START and CLOSING Flags. Stuffing replaces each byte within a PPP frame that matches the Flag or Control Escape code bytes with a two-byte sequence.
- Ability to force abort generation is configurable. The cTABTGx register allows to force (cTABTGx=1) the abortion of the current encapsulated frame by sending 0x7D and 0x7E bytes.

cTABTGx bit TBD	PPP Transmit Abort Generation
0	No abort generated. (Default)
1	Current frame under transmission is aborted by 0x7D followed by 0x7E. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH.

- Detection of FIFO overflow/underflow conditions and size (maximum) of PPP Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTPPFERRx alarm. The limit of the PPP Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTPPMAXERx, is generated when the size of the PPP Payload Information field exceeds the value configured in rTMAXFLx register.

rTMAXFLx (15-0)	PPP Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in the PPP Payload Information field that is transmitted. (Default = 0x2800)

- Ability to insert PPP Link Control Protocol (LCP)/Network Control Protocol (NCP) control frames by the Host is supported. A 128-byte buffer (using 128 rTCTL_x(8-0) registers) per MAC is provided to store a single PPP LCP/NCP control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the PPP LCP/NCP control frame. The Host must write a valid formatted (including overhead bytes) PPP control frame into the buffer such that only additional processing steps performed are: FCS calculation, Byte stuffing, addition of flags and scrambling. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a PPP LCP/NCP control frame.
  - Step 2: Once the PPP LCP/NCP control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the PPP LCP/NCP control frame is ready for transmission.
  - Step 3: During the next PPP inter-frame window (i.e., after the closing flag of the preceding PPP frame and before the opening flag of the following PPP frame), the stored PPP LCP/NCP control frame is inserted into the datapath for transmission to SONET/SDH.

- Step 4: Once the PPP LCP/NCP control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-12 and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available PPP LCP/NCP control frame transmission.

sTCTLBx bit TBD	PPP LCP/NCP Control Frame Buffer Status Indication
0	Buffer is empty and is able to receive a new PPP LCP/NCP control frame. (Default)
1	Buffer is full and is not able to receive a new PPP LCP/NCP control frame.

cTCTLBRSTx bit TBD	PPP LCP/NCP Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

- Ability to filter mapping of select PPP frames (i.e., frames with PPP Protocol field=0x0031) for transmission to SONET/SDH is provided using cTBPDUx register. Transmission of all PPP LCP/NCP control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of PPP frames (i.e., including PPP LCP/NCP control frames) for transmission to SONET/SDH.

cTBPDUx bit TBD	Selective PPP Frame Mapping Filter Control
0	PPP frames with PPP Protocol field=0x0031 are allowed to pass for mapping into SONET/SDH. (Default)
1	Only LCP/NCP-BCP frames from the host are mapped.

cTOFFx bit TBD	Generic PPP Frame Mapping Filter Control
0	All types of PPP frames (i.e., including PPP LCP/NCP control frames) are allowed to pass for mapping into SONET/SDH. (Default)
1	All types of PPP frames (i.e., including PPP LCP/NCP control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH.

- Maintains transmit statistics counters. Two types of counters are provided: the total number of PPP frame payloads transmitted (rpcTPPFRAMEx register) and the total number of PPP frame payload octets transmitted (rpcTPPBYTEx register) to SONET/SDH. These are also described in Table TBD.

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for PPP, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a PPP frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of the ADDRESS, CONTROL, PPP Protocol, PPP BCP Flags and PPP BCP MAC Type fields of a received PPP frame are validated against configurable stored values. Further, an option to discard frames with a mismatch of one of the fields, is configurable.
  The cRPACSELx register allows to configure the type of check to be performed on the ADDRESS and CONTROL field contents of a received PPP frame.

cRPACSELx bit TBD	cRPACSELx bit TBD	PPP ADDRESS and CONTROL Field Contents Check Control
0	0	ADDRESS and CONTROL field contents check is disabled. Assume ADDRESS and CONTROL fields are present.
0	1	ADDRESS and CONTROL field contents checked against fixed values (i.e., ADDRESS=0xFF, CONTROL=0x03). (Default).
1	0	Reserved.
1	1	ADDRESS and CONTROL field contents checked against the contents of rRPACFDx register.

The cRPPROTx register allows to configure the type of check to be performed on the PPP Protocol fields contents of a received PPP frame.

cRPPROTx bit TBD	PPP Protocol Field Contents Check Control
0	PPP Protocol field contents check is disabled.
1	PPP Protocol field contents checked against the contents of rRPPROTFDx register. (Default)

The cRPFGx register allows to configure the type of check to be performed on the PPP BCP flags field contents of a received PPP frame.

cRPFGx bit TBD	PPP BCP Flags Field Contents Check Control
0	PPP BCP flags field contents check is disabled.
1	PPP BCP flags field contents checked against the contents of rRPFGFDx register. (Default)

The cRPMACx register allows to configure the type of check to be performed on the PPP BCP MAC Type field contents of a received PPP frame.

cRPMACx bit TBD	PPP BCP MAC Type Field Contents Check Control
0	PPP BCP MAC Type field contents check is disabled.
1	PPP BCP MAC Type field contents checked against the contents of rRPMACFDx register. (Default)

The cRPACMMAEx register allows to configure handling of PPP frame with mismatched ADDRESS or CONTROL field contents. An alarm, aRPACMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL field contents of a received PPP frame.

cRPACMMAEx bit TBD	PPP ADDRESS and CONTROL Field Contents Mismatch Management
0	PPP frame with mismatched ADDRESS or CONTROL field contents is discarded. (Default)
1	PPP frame with mismatched ADDRESS or CONTROL field contents is not discarded.

The cRPPROTMMAEx register allows to configure handling of PPP frame with mismatched PPP Protocol field contents. An alarm, aRPPROTMMx, is generated when a mismatch is detected on the PPP Protocol field contents of a received PPP frame.

cRPPROTMMAEx bit TBD	PPP Protocol Field Contents Mismatch Management
0	PPP frame with mismatched PPP Protocol field contents is discarded. (Default)
1	PPP frame with mismatched PPP Protocol field contents is not discarded.

The cRPFGMMAEx register allows to configure handling of PPP frame with mismatched PPP BCP flags field contents. An alarm, aRPFGMMx, is generated when a mismatch is detected on the PPP BCP flags field contents of a received PPP frame.

cRPFGMMAEx bit TBD	PPP PCP Flags Field Contents Mismatch Management
0	PPP frame with mismatched PPP BCP flags field contents is discarded. (Default)
1	PPP frame with mismatched PPP BCP flags field contents is not discarded.

The cRPMACMMAEx register allows to configure handling of PPP frame with mismatched PPP BCP MAC Type field contents. An alarm, aRPMACMMx, is generated when a mismatch is detected on the PPP BCP MAC Type field contents of a received PPP frame.

cRPMACMMAEx bit TBD	PPP BCP MAC Type Field Contents Mismatch Management
0	PPP frame with mismatched PPP BCP MAC Type field contents is discarded. (Default)
1	PPP frame with mismatched PPP BCP MAC Type field contents is not discarded.

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRFLAGx register allows to configure the type of flag detection between consecutive PPP frames.

cRFLAGx bit TBD	PPP Flag Detection Control
0	At least two flags to be detected between PPP frames. (Default).
1	At least a single flag to be detected between PPP frames (i.e., a shared flag).

- Self-synchronous de-scrambler (x^{43} +1 polynomial) can be enabled or disabled according to the cRSCRDx register.

cRSCRDx bit TBD	PPP Descrambling Control
0	Enable descrambling of PPP frame. (Default)
1	Disable descrambling of PPP frame.

- 16 or 32-bit FCS generation and checking over all bits of the ADDRESS, CONTROL, PPP Control, PPP BCP Flags, PPP BCP Pads, PPP BCP MAC Type, Payload Information area (shaded area as shown in Figure 52) not including any Opening/Closing flags and Abort sequences, is configurable. The cRPFCSx register allows to configure enable/disable PPP FCS checking and the cRPCRCSx register allows to configure for use of 16 or 32-bit FCS checking. Further, an option is provided to process or discard PPP frames with a FCS error according to the cRPPPCSERx register. An alarm, aRPPPFCSER, is generated when a PPP frame is received with FCS error.

cRPFCSx bit TBD	PPP FCS Check Control
0	FCS check is disabled and assume all FCS field octets are not present.
1	FCS check is enabled. (Default)

cRPPPCSERx bit TBD	PPP FCS Check Handling (used when FCS Check is Enabled as per cRPFCSx Register)
0	Received PPP frames with FCS error are discarded. (Default)
1	Received PPP frames with FCS error are not discarded.

cRPCRCSx bit TBD	PPP FCS Check Type Select Control
0	32-bit FCS checking used. (Default)
1	16-bit FCS checking used.

For each received PPP frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

cRFCSSWAPINx bit TBD	PPP FCS Input Swap Control
0	For each received PPP frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default).
1	For each received PPP frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa).

- Transparency processing (octet de-stuffing for Flags and Control Escape) is supported. Byte de-stuffing occurs between START and CLOSING Flags.
- Ability to detect an abort indication via alarm and interrupt generation. To force an abort of the current frame, the cRPPPABTGx register needs to be set to 1. An alarm, aRPPPABTDx, is generated when an abort indication is detected (i.e., receive 0x7D followed by 0x7E) on the receive side.

cRPPPABTGx bit TBD	PPP Abort Generation
0	No frame aborted. (Default)
1	Current frame under receive is aborted.

- Ability to select type of padding mode used for decapsulation using cRBCPPDMODEx register.

cRBCPPDMODEx bit TBD	PPP Padding Mode Control
0	A fixed padding mode is used.
1	No padding is used. (Default)

- Processing of invalid PPP frames as per RFC 1662.
- Detection of size (minimum and maximum) of PPP frame via alarm and interrupt generation. The minimum size of the received PPP frame (in octets) can be configured using the rRPPPMINFLx register (i.e., the number of octets between the opening and closing flags). An alarm, aRPPPSHTERx, is generated when the size of received PPP frame is less than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets and this frame is aborted. An alarm, aRPPPMINERx, is generated when the size of the received PPP frame is greater than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets but less than the value configured in rRPPPMINFLx register. The maximum size of the received PPP frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRPPPMAXERx, is generated when the size of the received PPP frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

rRPPPMINFLx(7-0)	PPP Frame Size
0x04 - 0xFF	Indicates minimum number of octets present in a received PPP frame between opening and closing flags. (Default = 0x04 when using 16-bit FCS or 0x06 when using 32-bit FCS)

rRMAXFLx(15-0)	PPP Frame Payload Information Field Size
0x0001 - 0x2800	Indicates maximum number of octets in a received PPP frame Payload Information field. (Default = 0x2800)

- Ability to filter and extract PPP LCP/NCP control frames by the Host is supported. A 520-byte buffer (using 520 rRLMIx_ (8-0) registers) per MAC is provided to store a single PPP LCP/NCP control frame for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the PPP LCP/NCP control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a PPP LCP/NCP control frame such that only the following processing have been performed: FCS Check, Byte de-stuffing and removal of flags. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLAVx status register and causes the 520-byte buffer to clear its present contents. The rRPLCPx register is used to configure the PPP Protocol field value to be checked in order to extract the PPP LCP control frame and the rRCTLMASKA1x register is used as a bit level mask that is applied to the cRPLCPx register. The rRPNCPx register is used to configure the PPP Protocol field value to be checked in order to extract the PPP NCP control frame and the rRCTLMASKB1x register is used as a bit level mask that is applied to the cRPNCPx register. Below is an example of how the Host can use this buffer:
  - Step 1: If the buffer is empty, sRCTLAVx=0 and the Host is not allowed to read for a new PPP LCP/NCP control frame.
  - Step 2: Once the PPP LCP/NCP control frame has been received, the sRCTLAVx status register is set (sRCTLAVx=1) by the EtherMap-12 to indicate at least one PPP LCP/NCP control frame is ready for extraction by the Host. Further PPP LCP/NCP control frames may be written into the buffer if received. If so, the sRCTCLAVx bit will become set again. An alarm is provided (aRCTLOVF) to indicate the overflow of the 520-byte buffer.

sRCTLAVx bit TBD	PPP LCP/NCP Control Frame Buffer Status Indication
0	Buffer is empty and no complete PPP LCP/NCP control frame has been received/stored. (Default)
1	Buffer is full with at least one complete PPP LCP/NCP control frame received.

cRCTLBRSTx bit TBD	PPP LCP/NCP Control Frame Buffer Reset Control
0	Buffer is not in reset state. (Default)
1	Buffer is in reset state.

rRPLCPx(15-0)	PPP LCP Control Frame PPP Protocol Field Contents
0x0000 - 0xFFFF	Indicates contents of the LCP control frame PPP Protocol field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKA1 mask register. (Default = 0xC021)

rRCTLMASKA1x(15-0)	PPP LCP Control Frame PPP Protocol Field Contents Mask
0x0000 - 0xFFFF	Mask value that is applied to the rRPLCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPLCPx register is used for filtering. (Default = 0xFFFF)

rRPNCPx(15-0)	PPP NCP Control Frame PPP Protocol Field Contents
0x0000 - 0xFFFF	Indicates contents of the NCP control frame PPP Protocol field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKB1 mask register. (Default = 0x8031)

rRCTLMASKB1x(15-0)	PPP NCP Control Frame PPP Protocol Field Contents Mask
0x0000 - 0xFFFF	Mask value that is applied to the rRPNCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPNCPx register is used for filtering. (Default = 0xFFFF)

- Ability to filter decapsulation of select PPP frames (i.e., frames with PPP Protocol field=0x0031) that are received from SONET/SDH is provided using cRBPDUx register. Reception of all PPP LCP/NCP control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

cRBPDUx bit TBD	Selective PPP Frame Decapsulation Filter Control
0	Received frames from SONET/SDH, with PPP Protocol field=0x0031, are allowed to be decapsulated.
1	Received frames from SONET/SDH, with PPP Protocol field=0x0031, are not allowed (i.e., frames are discarded) to be decapsulated. (Default)

Maintains receive statistics counters. All PPP receive side statistic counters are described in Table TBD.

TRANSPARENT HDLC

The Transparent HDLC is a generic HDLC-like framing structure and provides a standard method for transporting multi-protocol datagrams over HDLC links.

Figure 53 shows the format of a Transparent HDLC frame with an Ethernet MAC frame payload (denoted by the shaded area).

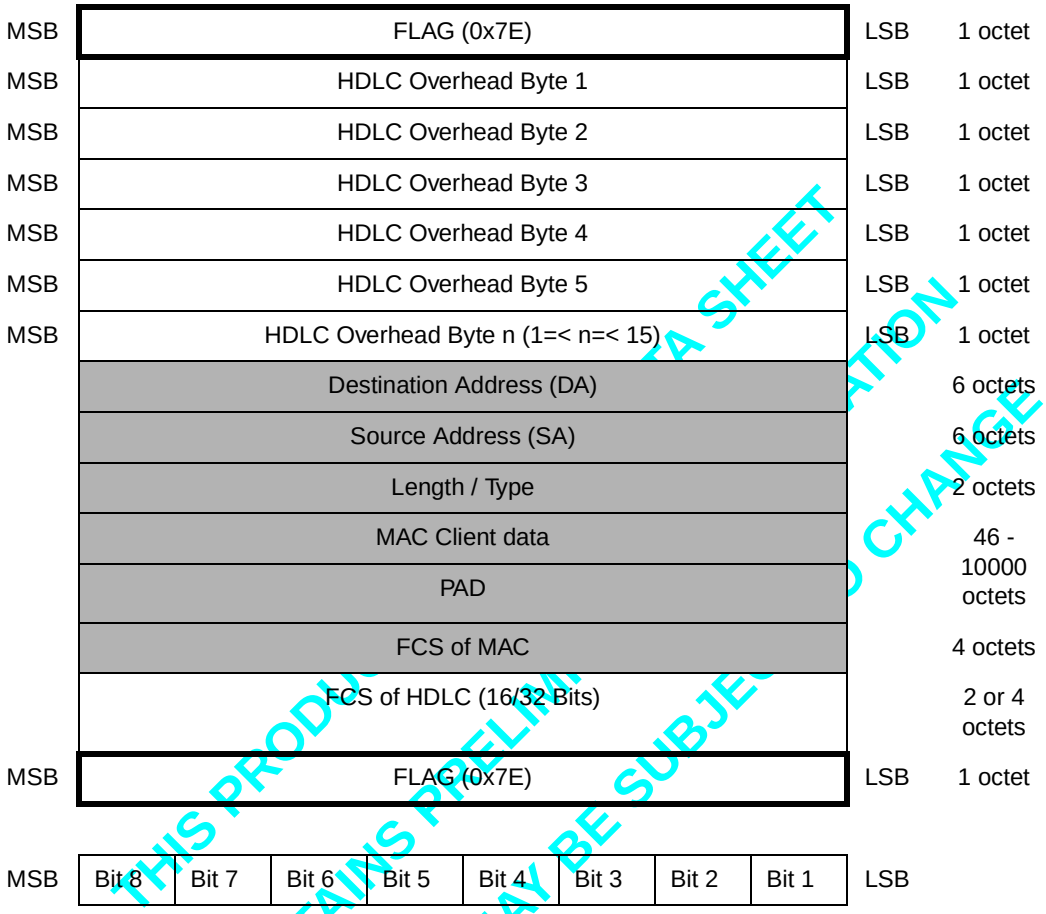


Figure 53. Format of Transparent HDLC Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for Transparent HDLC, the following functions are supported:

- A pre-configured/encapsulated Ethernet MAC frame within a Transparent HDLC frame is provided by the external client (i.e the HDLC Overhead byte(s) have already been configured by the external client). Each Transparent HDLC frame is encapsulated with a START FLAG (0x7E), a 16/32-bit FCS field, and a CLOSING FLAG (0x7E). No other field insertions are allowed except the START Flag.
- Shared flag (START and CLOSING) generation is configurable. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive Transparent HDLC frames.
- Self-synchronous scrambler (x^{43} +1 polynomial) can be enabled or disabled. The cTSCRDx register allows to enable/disable scrambling of Transparent HDLC frame. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

- 16 or 32-bit FCS generation over all bits of the HDLC Overhead bytes, Payload Information area (shaded area as shown in Figure 53) not including any Opening/Closing flags and Abort sequences, is configurable using the cTPFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALLx register.

  For each Transparent HDLC frame byte that is input to the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPINx register.

  For each Transparent HDLC FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.
- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).
- Transparency processing (octet stuffing for Flags and Control Escape) is supported. Byte stuffing occurs between START and CLOSING Flags. Stuffing replaces each byte within a Transparent HDLC frame that matches the Flag or Control Escape code bytes with a two-byte sequence.
- Ability to force abort generation is configurable. The cTABTGx register allows to force (cTABTGx=1) the abortion of the current encapsulated frame by sending 0x7D and 0x7E bytes.
- Detection of FIFO overflow/underflow conditions and size (maximum) of Transparent HDLC Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTPPFERRx alarm. The limit of the Transparent HDLC Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTPPMAXERx, is generated when the size of the Transparent HDLC Payload Information field exceeds the value configured in rTMAXFLx register.
- Maintains transmit statistics counters. Two types of counters are provided: the total number of Transparent HDLC frame payloads transmitted (rpcTPPFRAMEx register) and the total number of Transparent HDLC frame payload octets transmitted (rpcTPPBYTEx register) to SONET/SDH.

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for Transparent HDLC, the following functions are supported:

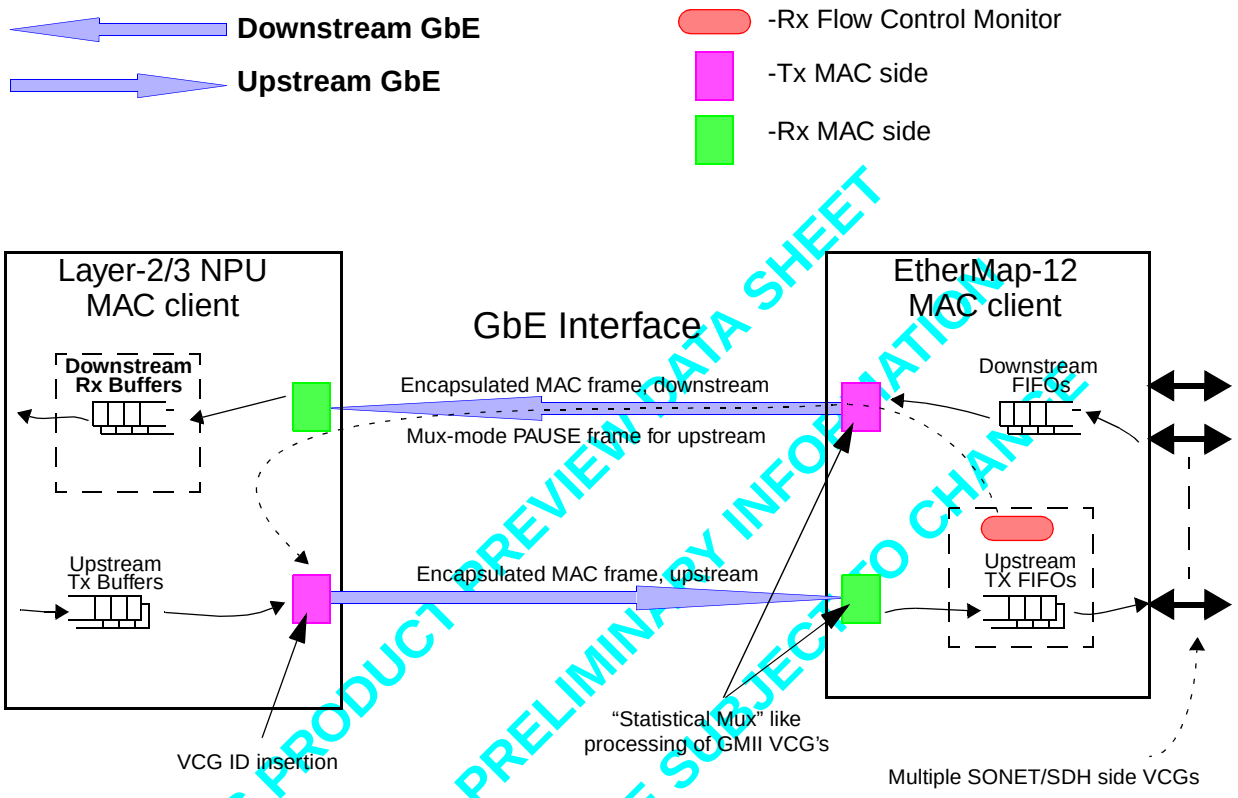
- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRFLAGx register allows to configure the type of flag detection between consecutive Transparent HDLC frames.
- Self-synchronous de-scrambler (x^{43} +1 polynomial) can be enabled or disabled according to the cRSCRDx register.
- 16 or 32-bit FCS generation and checking over all bits of the HDLC Overhead bytes, Payload Information area (shaded area as shown in Figure 53) not including any Opening/Closing flags and Abort sequences, is configurable. The cRPFCSx register allows to configure enable/disable FCS checking and the cRPCRCSx register allows to configure for use of 16 or 32-bit FCS checking. Further, an option is provided to process or discard Transparent HDLC frames with a FCS error according to the cRPPPCSERx register. An alarm, aRPPPFCSER, is generated when a Transparent HDLC frame is received with FCS error.
  For each received Transparent HDLC frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.
- Transparency processing (octet de-stuffing for Flags and Control Escape) is supported. Byte de-stuffing occurs between START and CLOSING Flags.
- Ability to detect an abort indication via alarm and interrupt generation. To force an abort of the current frame, the cRPPPABTGx register needs to be set to 1. An alarm, aRPPPABTDx, is generated when an abort indication is detected (i.e., receive 0x7D followed by 0x7E) on the receive side.
- Processing of invalid Transparent HDLC frames as per RFC 1662.

- Detection of size (minimum and maximum) of Transparent HDLC Payload Information field via alarm and interrupt generation. The minimum size of the received Transparent HDLC frame (in octets) can be configured using the rRPPPMINFLx register (i.e., the number of octets between the opening and closing flags). An alarm, aRPPPSHTERx, is generated when the size of received Transparent HDLC frame is less than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets and this frame is aborted. An alarm, aRPPPMINERx, is generated when the size of the received Transparent HDLC frame is greater than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets but less than the value configured in rRPPPMINFLx register. The maximum size of the received Transparent HDLC frame (in octets) can be configured using the rRMAXFLx register. An alarm, aRPPPMAXERx, is generated when the size of the received Transparent HDLC frame (in octets) exceeds the value configured in rRMAXFLx register.
- Maintains receive statistics counters.

GMII MUX-MODE

This mode is used in applications which require a single external Gigabit Ethernet client to transfer Ethernet frames into multiple VCGs in the SONET/SDH side. Figure 54 below provides an overview of the GMII Mux-mode application.

Figure 54. GMII Mux-Mode Application Overview



Multiplexing packets for independent multiple SONET/SDH side VCGs across a single GMII interface has two major components that are addressed by EtherMap-12:

- An addressing scheme utilizing a destination VCG ID included with the MAC frame assigned by the external source side of the GMII interface identifying the traffic source. The VCG ID is optionally removed by the EtherMap-12, before transmission to SONET/SDH, to recover the original Ethernet MAC frame.
- A modified and flexible 802.3 PAUSE Control frame payload to specify XON/XOFF on a per VCG basis. Each VCG's TX FIFO fill levels are monitored for filling beyond a threshold. Exceeding the threshold results in a PAUSE Frame sent to the opposite MAC client asserting the XOFF state for the TX FIFO that is experiencing congestion. When the TX FIFO returns below a minimum threshold, a second Pause Frame is sent to the opposite MAC client asserting the XON state for the TX FIFO that is relieved of congestion.

Lastly, the GMII Mux-mode is allowed to be independently configured for both Ethernet-to-SONET/SDH and SONET/SDH-to-Ethernet directions.

SDRAM CONTROLLERS

SDRAM MEMORY INTERFACES

These interfaces are used to allow the mapper to connect two external SDRAM Memory Modules. The external SDRAM Memory Modules are used for buffering of Ethernet traffic in both directions. Each of the external SDRAM memory interfaces comprises of a 32-bit data bus, 13-bit address bus, bank address bus, 3-bit command bus, Input/Output Mask bus, system clock (up to 125 MHz) and control enable signals.

The SDRAM control blocks will interface to a dynamic random access memory containing up to 256 Mbits. They will support a quad-bank SDRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

The external SDRAMs will be accessed as 4 banks with a data bus width of 32 bits.

Read and write accesses to the external SDRAMs are burst oriented using alternative bank switching. Access starts at a selected location and continues for a programmed number of locations in a programmed sequence. Access begins with issuing an ACTIVE command, which is then followed by a READ or WRITE command. The address bits issued together with the ACTIVE command are used to select the bank and row to be accessed. The address bits issued together with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM interface blocks will require programmable READ or WRITE burst lengths of 2 locations with or without a burst terminate option. An auto precharge function may be enabled, to initiate a self-timed row precharge, at the end of the burst sequence.

The 256 Mb SDRAM interface blocks may change the row/column address on every clock cycle, in order to achieve a high-speed, fully random access. One bank in precharged while accessing one of the other three banks, thus hiding the precharge cycles and providing high-speed, random-access operation.

The 256 Mb SDRAM control blocks will operate with 3.3V, low-power memory block.

All inputs and outputs are LVTTL-compatible.

CAS Latency

Please refer to timing diagrams SDRAM_read, SDRAM_write. The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The SDRAM interface can be programmed for a latency of three clock cycles. This means that data will be sampled on the third rising edge after the READ command is issued.

BANK/ROW Activation

Please refer to timing diagrams SDRAM_read, SDRAM_write. The ACTIVE command is issued before any READ or WRITE. After issuing the ACTIVE command, the READ or WRITE command may be issued to the selected row, subject to the tRCD specification. The SDRAM block controller is designed for SDRAM having a tRRP (MIN) lower than 16 ns; with a clock rate of 125 MHz. This implies that a READ or WRITE command can be issued on the second rising edge after the ACTIVE command was issued.

Commands

The following commands can be issued by the SDRAM controllers (see the table below):

Command Name	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	MASK	ADDR	BK	NOTES
Command Inhibit Nop	H	X	X	X	X	X	X	
No Operation Nop	L	H	H	H	X	X	X	
Active	L	L	H	H	X	BANK/ROW		
Read	L	H	L	H	L/H	BANK/COL		
Write	L	H	L	L	L/H	BANK/COL	VALID	
Precharge	L	L	H	L	X	CODE	X	
Auto Or Self Refresh	L	L	L	H	X	X	X	
Load Mode Register	L	L	L	L	X	OP-CODE	X	
Write Enable					L		ACTIVE	
Write Inhibit					H		HIGH Z	

RESET CONFIGURATION OF SDRAM CONTROLLER

Upon reset the SDRAM CONTROLLER is configured for a 4 bank 256 Mbit SDRAM. The default configuration parameters are:

- SDRAM size: 256 Mbits.
- AUTO REFRESH period: SDRAM_TRFC = 7.
- SDRAM auto refresh period (expressed in 8 periods of SYSCLK input): SDRARP = 78 (decimal) which creates a 5 µs/row auto refresh period.
- PRECHARGE command period: SDRAM_TRP = 2 (cannot be changed).
- Power-up initialization delay: SDRTINIT = 100. Indicates 100 units of 100 periods of the SYSCLK input, in other words, 10000 times SYSCLK. It is required by the SDRAM prior to issuing any command other than a COMMAND INHIBIT or a NOP.
- Number of AUTO REFRESH performed during initialization (full SDRAM auto-refresh): SDRINIT_AR_MBR = 8. A configured value of 'n' will provide 'n+1' AUTO REFRESH cycles during the initialization period.
- Mode register default value: MBR_VALUE = 0 000 011 0 001.

CONFIGURATION CHANGES/INITIALIZATION

After power-up, or in order to change any of the SDRAM configuration parameter, the following procedure must be used:

- Modify the SDRARP (address TBD), SDRINIT_AR_MBR (address TBD) and/or SDRTINIT (address TBD) registers.
- Write the cSDRAM register (address TBD) with SDRAM_CFG and SDRAM_TRFC new values (if no change, use default values) and with SDRAMINIT field at 1.

All the configuration registers dedicated to the SDRAM controller are described in Table TBD of the Memory Map.

MICROPROCESSOR ACCESS TO SDRAM

Here is the procedure to perform a write access to the SDRAM:

- Write the data to write in the 2 sixteen-bits registers UP_data2WrMSB (address TBD) and UP_data2WrLSB (address TBD).
- Write the address to write in the UP_Addr2WrMSB (bits TBD to TBD of TBD register) and UP_Addr2WrLSB (16 bits of TBD register) registers.
- Set to 1 the UP_WrAddr2Wr register (bit TBD of TBD register). This bit is cleared by the chip at the end of the SDRAM write access.

Here is the procedure to perform a read access to the SDRAM:

- Write the address to read in the UP_Addr2RdMSB (bits TBD to TBD of TBD register) and UP_Addr2RdLSB (16 bits of TBD register) registers.
- Set to 1 the UP_WrAddr2Rd register (bit TBD of TBD register). This bit is cleared at the end of the SDRAM read access.
- When the UP_WrAddr2Rd is cleared, the data is available in the UP_DataRdLSB register (TBD address) for the LSB value and UP_DataRdMSB register (TBD address) for the MSB value.

All the registers for access of the SDRAMs with the microprocessor, are described in the Tables TBD of the Memory Map.

RESET OPERATION

GENERAL

Four types of reset are available in this device, external lead controlled hardware reset, microprocessor controlled hardware reset, microprocessor soft reset and microprocessor controlled global performance counters reset.

EXTERNAL LEAD CONTROLLED HARDWARE RESET

The $\overline{\text{RESET}}$ external lead activates the hardware reset. The actions are as follows:

- The configuration bits are in default state (all Ethernet MAC disabled, SDRAM 256 Mb configuration, encapsulation/de-encapsulation in LAPS mode, all the VT/VC are not allocated to any VCG, the Telecom bus interface is disabled)
- All the interrupt bit mask are in disabling state
- All the performance counters are cleared

MICROPROCESSOR CONTROLLED HARDWARE RESET

When the RESETH byte register (bits TBD of register TBD) is equal to 91 Hex, it activates the hardware reset. The actions are the same as the external lead controlled hardware reset.

To clear the reset action, it is necessary to change the value of the RESETH byte register (bits TBD of register TBD) or to perform an external lead controller hardware reset.

MICROPROCESSOR CONTROLLED SOFT RESET

Sixteen soft reset are available in the device, eight for each direction (Ethernet to SONET/SDH and SONET/SDH to Ethernet). The TX_RESETSx byte registers (bits TBD of registers TBD-TBD) are corresponding to the software reset of the Ethernet line #0 to #7 in the transmit direction. The RX_RESETSx byte registers (bits TBD of registers TBD-TBD) are corresponding to the software reset of the VCG #0 to #7 in the receive direction.

When the value of the byte register of each software RESET is equal to 91 Hex, it activates the corresponding software reset. The actions are as follows:

- All the internal logic is initialized
- No impact on the control/configuration registers or counters

To clear the reset action, it is necessary to change the value of the corresponding software reset byte register or to perform an external lead controller hardware reset or to activate the microprocessor controlled hardware reset (RESETH). Please Note that the soft reset must be kept asserted for 16 µs before releasing it.

The TX_RESETSx needs to be activated and then deactivated whenever the corresponding L1aPTRRAMERRx alarm in register TBD becomes set to avoid a potential lockup condition.

MICROPROCESSOR CONTROLLED GLOBAL PERFORMANCE COUNTER RESET

When the RESETC byte register (bits TBD of register TBD) is equal to 91 Hex, it activates the global performance counter reset. The main actions is to clear all the performance counters.

To clear the reset action, it is necessary to change the value of the global performance counter reset byte register or to perform an external lead controller hardware reset or to activate the microprocessor controlled hardware reset (RESETH). The reset action can also be cleared by the global software rest or any of the 16 per channel software resets.

TELECOM BUS OPERATION

GENERAL

When the EtherMap-12 is configured for Drop timing, the Add bus is byte and multi-frame synchronous with the Drop bus, although delayed by one byte time because of internal processing. For example, if a byte in the STM-4 VC-4 structure using TUG-3, TU-12 mapping is to be added to the Add bus, the time of its placement is derived from the Drop bus timing, and from software instructions specifying which TU-12 number is being added. Note that the TU-12 drop selection can be different than the Add bus selection. An option is provided which enables the Drop bus timing signals to be sent as outputs on the Add bus. When the device is configured for Add bus timing, the add bus data, parity, and add indicator can be either derived from the input Add bus clock, C1J1V1, and SPE signals, or derived from internally generated and outputted clock, C1J1V1, and SPE signals.

DROP BUS INTERFACE

The Drop bus consists of the following leads:

- Input data (TBDD(7-0)),
- Input parity (TBDPAR),
- Input clock (DCLK),
- Input C1, J1, and optional V1 marker pulses (TBDC1J1V1),
- Input payload indication (TBDSPE).

The most significant bit (MSB) of the input data is assigned to TBDD7. The MSB is defined as the first bit received in a SONET/SDH byte (i.e., bit 1 in the SONET/SDH byte). The bus rate is 77.76 MHz. The drop bus is monitored for loss of clock. The Loss of Drop Clock alarm is aLOSSDCLK at bit TBD of register (TBD).

DROP BUS PARITY SELECTION

The parity selection for the Drop bus is according to the following table. A parity error is indicated by the ParityError alarm at bit TBD of register (TBD). Other than an alarm indication, no action is taken by the EtherMap-12.

ParityEven (bit TBD of register TBD)	ParityMode (bit TBD of register TBD)	Drop Bus Parity Selection
0	0	Odd parity is calculated for the data input leads (DD(7-0)).
0	1	Odd parity is calculated for the input leads consisting of data (DD(7-0)), clock (DCLK), C1, J1, and V1 marker pulses (DC1J1V1), and the payload indicator (DSPE).
1	0	Even parity is calculated for the input leads consisting of data (DD(7-0)), clock (DCLK), C1, J1, and V1 marker pulses (DC1J1V1), and the payload indicator (DSPE).
1	1	Even parity is calculated for the data input leads (DD(7-0)).

ADD BUS INTERFACE

The Add bus consists of the following leads:

- Output data (TBAD(7-0)),
- Output parity (TBAPAR),
- Output add-to-bus indicator ($\overline{\text{TBADD}}$)

The timing information can be input or output:

- Input/Output C1, J1, and optional V1 marker pulses (TBAC1J1V1),
- Input/Output payload indication (TBASPE).

The most significant bit (MSB) of the output data is assigned to TBAD7. The MSB is defined as the first bit transmitted in a SONET/SDH byte (i.e., bit 1 in the SONET/SDH byte). The bus rate is 77.76 MHz.

The Add bus is always synchronous to the RTCLK reference clock.

ADD BUS TIMING MODES

The Add bus interface configuration and timing modes are shown in the following table. The TBMODE lead selects the C1J1V1, and SPE signals to be either inputs or outputs. The TBMASTER lead allows the C1J1V1, and SPE signals to be tristated.

The data (TBAD(7-0)), parity (TBADPAR), and add indicator ($\overline{\text{TBADD}}$) leads are always output and their direction is not dependent on the timing mode chosen.

TBMODE	TBMASTER	Add Bus Configuration and Timing Mode
0	X	Add Bus Timing Slave Mode: The C1, J1, V1 marker pulses (TBAC1J1V1), and payload indicator (TBASPE) are inputs.
1	0	Add Bus Timing Master Mode: The C1, J1, V1 marker pulses (TBAC1J1V1), and payload indicator (TBASPE) are outputs.
1	1	Add Bus Timing Master Mode: The C1, J1, V1 marker pulses (TBAC1J1V1), and payload indicator (TBASPE) are tristated.

ADD BUS PARITY SELECTION

The parity selection for the Add bus is according to the following table. Note that the timing mode selected for the Add bus must be consistent with the parity mode selected.

ParityEven (bit TBD, register TBD)	ParityMode (bit TBD, register TBD)	Add Bus Parity Selection
0	0	Odd parity is calculated for the data output leads (AD(7-0)).
0	1	Odd parity is calculated for the output leads consisting of data (AD(7-0)), clock (ACLK), C1, J1, and V1 marker pulses (AC1J1V1), and the payload indicator (ASPE).
1	0	Even parity is calculated for the data output leads (AD(7-0)).
1	1	Even parity is calculated for output leads consisting of data (AD(7-0)), clock (ACLK), C1, J1, and V1 marker pulses (AC1J1V1), and the payload indicator (ASPE).

ADD INDICATOR INVERT

An option is provided for inverting the active level of the Add indicator signal ($\overline{\text{ADD}}$ lead). When a 0 is written to control bit AddInd_ActLow (bit TBD, register TBD), the $\overline{\text{ADD}}$ signal is high when payload is being added to the bus. When a 1 is written to control bit AddInd_ActLow, the $\overline{\text{ADD}}$ signal is low when payload is being added to the bus. This control bit defaults to a 1 upon power-up or via software reset.

ADD BUS DELAY

Options for additional delay of the Add bus data, parity, Add indicator, and optionally the C1J1V1 and SPE signals, relative to either the Add bus or Drop bus timing are shown in the following table. Control field TimingDelay can delay the Add bus outputs by up to fifteen extra clock cycles. All Add bus outputs are delayed one clock from the timing when control field TimingDelay is set to 0, for all timing modes except the Add bus mode in which the timing signals are outputs. For this mode there is always no delay between the output data and timing.

Add bus delay is used to align added data and timing when used in Add bus timing mode with a TranSwitch overhead terminator such as the PHAST®-12N.

TimingDelay (bits TBD, register TBD)	Timing Mode	Add Bus Additional Delay
0-F	Drop bus; Add bus timing outputs Tristated.	Add bus data, parity, and add indicator additional delay is up to 15 clocks from the Drop bus timing.
0-F	Drop bus; Add bus timing outputs active.	Add bus data, parity, add indicator, C1J1V1, and SPE additional delay is up to 15 clocks from the Drop bus timing.
0-F	Add bus; Add bus timing signals are inputs.	Add bus data, parity, and add indicator additional delay is up to 15 clocks from the Add bus timing.

TimingDelay (bits TBD, register TBD)	Timing Mode	Add Bus Additional Delay
0-F	Add bus; Add bus timing signals are outputs.	Add bus additional delay control is disabled.

FORCE VC-3 OR VC-4 TIME SLOTS TO HIGH IMPEDANCE

The data, parity, and Add indicator corresponding to a VC-3 can be forced to a high impedance state by setting control bit HighZ_AU3 at bit TBD of register TBD (VC-3 #1), TBD (VC-3 #2), or TBD (VC-3 #3) to a 1. When operating in the AU-4 mode (control bit AU_Mode, bit TBD in register TBD is a 1), the data, parity, and add indicator for the VC-4 can be forced to a high impedance state by setting all three HighZ_AU3 control bits to a 1.

FORCE TUG-3 TIME SLOTS TO HIGH IMPEDANCE

When operating in the AU-4 mode (control bit AU_Mode, bit TBD in register TBD is a 1), the data, parity, and add indicator corresponding to a TUG-3 can be forced to a high impedance state by setting control bit HighZ_TUG3 at bit TBD of register TBD (TUG-3 #1), TBD (TUG-3 #2), or TBD (TUG-3 #3) to a 1.

FORCE TUG-2 TIME SLOTS TO HIGH IMPEDANCE

The data, parity, and add indicator corresponding to a TUG-2 can be forced to a high impedance state by setting control bit HighZ at bit TBD of register TBD (TUG-2 #1), TBD (TUG-2 #2), TBD (TUG-2 #3),... or TBD (TUG-2 #21) to a 1.

FORCE TU-11/TU-12 TIME SLOTS TO HIGH IMPEDANCE

The data, parity, and add indicator corresponding to a TU-11 can be forced to a high impedance state by setting control bit HighZ at bit TBD of register TBD (TU-11 #1), TBD (TU-11 #2), TBD (TU-11 #3),... or TBD (TU-11 #84) to a 1.

The data, parity, and add indicator corresponding to a TU-12 can be forced to a high impedance state by setting control bit HighZ at bit TBD of register TBD (TU-12 #1), TBD (TU-12 #2), TBD (TU-12 #3),... or TBD (TU-12 #63) to a 1.

BOUNDARY SCAN

Introduction

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides absorbability and controllability for the interface leads of the device. As shown in Figure 55, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRST}}$) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown Figure 35.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 55.

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRST}}$ low. When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals to pass to and from the EtherMap-12 device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation

The maximum frequency the EtherMap-12 device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 35.

The instruction register contains three bits. The EtherMap-12 device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the EtherMap-12 device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the EtherMap-12 boundary scan and instruction registers.

Boundary Scan Reset

Specific control of the $\overline{\text{TRST}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the EtherMap-12. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

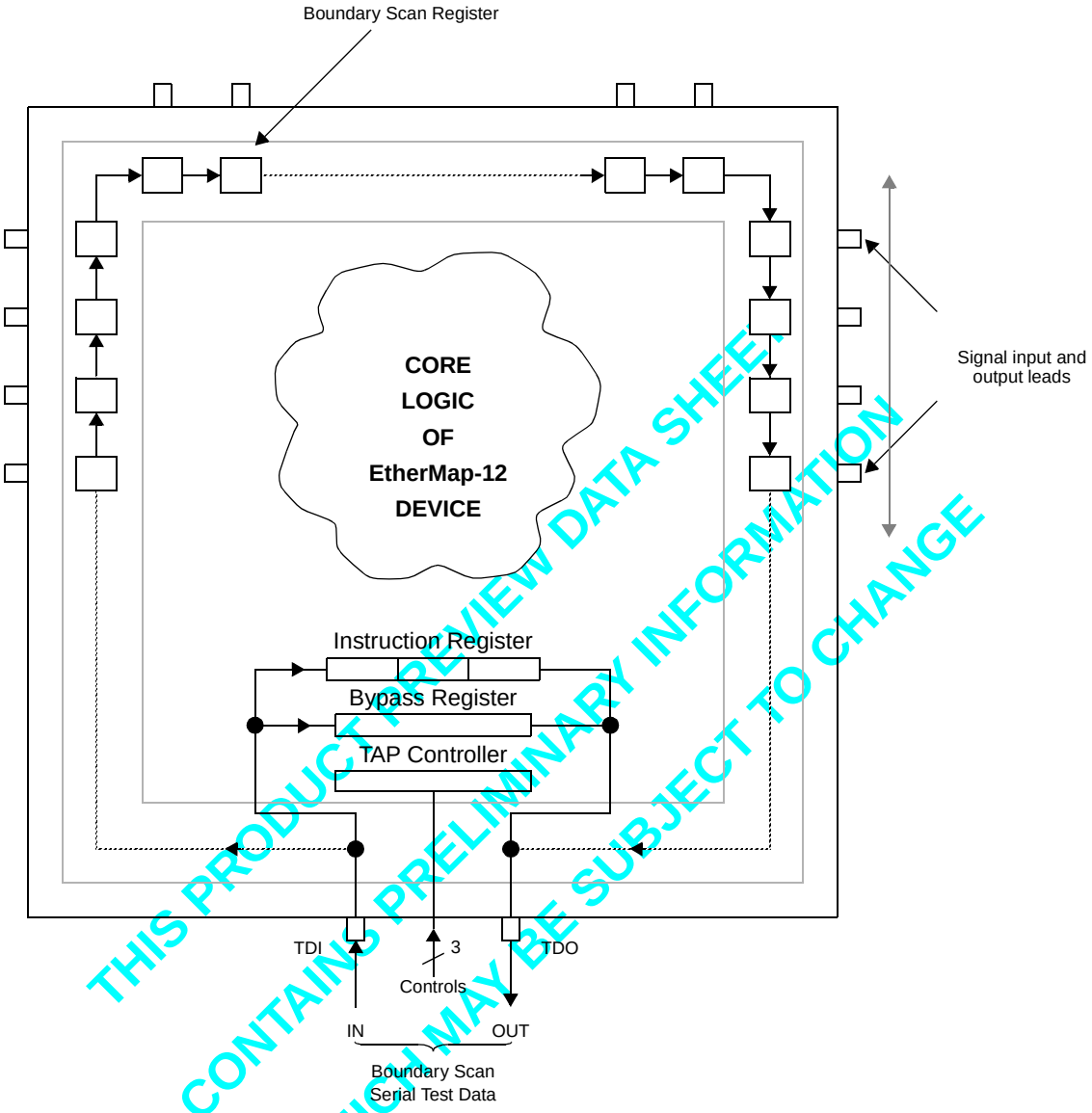


Figure 55. Boundary Scan Schematic

ALARMS, PERFORMANCE AND FAULT MONITORING

This section details out the Alarm/Status and Performance Monitoring features for the EtherMap-12 device. The general features are described herein, with specific listing of all Alarms, Performance Counters appearing in the relevant sections.

TERMINOLOGY

System Alarm (Raw, Unlatched Alarm)

A signal that traces in real time, the evolution of a system property (a system fault, statistic, or any other characteristic that needs monitoring) when appropriately enabled. This signal, then can be monitored for purposes of corrective action or for the purposes of status reporting.

Note that the terms System Alarm, Raw Alarm or Unlatched Alarm may be used interchangeably.

Alarm Event

A transition in the state of a System Alarm.

Note that there can be two types of transitions in a System Alarm - a rising edge, or a falling edge corresponding to ‘Alarm Entry’ or ’Alarm Exit’ respectively.

Latched Alarm

A Latched Alarm for a given Unlatched Alarm, is the associated latched memory for the occurrence of an alarm event (of a single type, or either type) in the unlatched alarm signal. This permits processing of the system alarm without real-time constraints. The active transition or level, which leads to setting of the Latched Alarm, in general may be software configurable.

Secondary Alarm Inhibition

The process of filtering to provide data reduction and unnecessary generation of interrupts, when an alarm event that is at a higher hierarchy leads to the generation of multiple lower order alarms (in other words, lower order alarm events are triggered as a secondary effect). This filtering mechanism (termed herein as ’Secondary Alarm Inhibition) prevents redundant data processing and also the unnecessary interrupt burden that may affect adversely the functioning of the system.

Notes:

- Refer Section 6 of [G806], relating to Defect Correlations.

- The Alarm Inhibition function may be built at the Unlatched Alarm level, or, if GR-253 style reporting requirements need to be supported, then the Alarm Inhibition may be built at the Latched Alarm level.

Trail Signal Failure (TSF)

See [G806]

Server Signal Failure (SSF)

See [G806]

Interrupt Mask

If interrupt generation is a function of a given Latched Alarm, there will be a corresponding dedicated Interrupt Mask bit, that may be set up to disable the particular interrupt. These bits will be software readable and writable.

Performance and Fault Monitoring (PM and FM)

An Unlatched Alarm may have associated with it a corresponding PM/FM feature, that allows a System to monitor the long term evolution of the particular alarm, in a convenient manner.

As an example (refer [GR253] section 6), a System may wish to monitor if a defect occurred over only a single unit time interval, or, if the defect persisted over several unit time intervals with respect to a certain particular alarm, or a group of alarms. The unit time interval may be 1-second, or any other, as laid down by applicable standards (if any), or as required to implement a specified Performance and Fault Monitoring System.

Performance Monitoring (PM)

For TranSwitch devices, the 1-second PM output bit associated with an unlatched alarm indicates the occurrence of an alarm event over the immediately preceding 1-second interval.

Fault Monitoring (FM)

For TranSwitch devices, the 1-second FM output bit associated with an unlatched alarm indicates that the unlatched alarm was continuously asserted, without any alarm events taking place, over the duration of at least the immediately preceding 1-second interval.

1-Second Clock

The 1-second clock defines 1-second time intervals to serve as a time reference for the PM/FM scheme (see ONESEC page TBD-Leads table). This clock typically, may be provided from external sources to TranSwitch devices, and is also used to synchronize the external polling mechanism that would query the PM/FM registers on the TranSwitch device.

Performance Counters

Certain alarm events or parameters are counted for System Performance Monitoring. The counter width (in bits) depends on the event being counted, and time-intervals (that is, estimated maximum counts) between reads. The Performance Counters may adopt one of two schemes:

A. Counters that either roll-over or saturate. Here 'roll-over' means that after the terminal count is reached, the counter wraps around, and continues to count from zero; 'saturate' means that after terminal count is reached, the counter stops incrementing, and freezes at the terminal count.

B. Counters that clear on 1-second boundaries, with existing counts over the 1-second interval transferred to 1-second counter shadow registers (also on the 1-second boundaries). The main event counters are cleared by the microprocessor writing 0's to the counter, or at 1-second boundaries.

Counter scheme (A) is more appropriate if the PM/FM system is not implemented. Scheme (B) is conceptually compatible with the PM/FM system. However, there will be no constraint imposed by this specification in implementing either counter scheme. The implementation of the desired counter scheme is governed by the particular device specification.

UNLATCHED ALARMS

All Unlatched alarms are memory mapped and available to be read out from Read-Only type registers for the actual status.

The Unlatched alarm signal is active high only when asserted.

These signals may be logically grouped together for easy microprocessor readout on a per channel basis, or based on any other appropriate grouping. However, whatever the grouping arrangement is adopted for the Unlatched Alarm signals, the same grouping is applied for the associated Latched Alarms, Mask Bits, and PM/FM bits.

Unlatched Alarms can be both frame based, like SONET/SDH Performance Alarms, or, independent of framing, such as Loss of Signal alarms, or Buffer overflow/underflow alarms etc.

Inhibition of Secondary Unlatched Alarm Generation

The generation of Secondary Unlatched Alarm may be inhibited dynamically, depending on system alarm hierarchy to prevent unnecessary automatic reporting of secondary alarms which arise as a consequence of some primary root cause alarm (the particular inhibiting conditions for a given device). This process is known as 'Defect Correlation' in [G806]. Defect correlation will also inhibit the generation of unnecessary interrupts at a lower layer. Refer figures 6.1 and 6.2 in [G806], that illustrate the process of Alarm Supervision and Defect Correlation at each atomic function. Each atomic function generates AIS as appropriate, based on locally detected defects only. Upstream AIS or upstream TSF/SSF signals are inputs to the atomic function. The defect correlation process in [G806] terminology is described as

c(defect) <--- d(defect) AND (not(inhibition_condition) AND (inhibition_enabled))

There are two components for the inhibition function:

1) Active high Alarm Inhibition condition based on upstream or primary or root cause alarms; (Active_Hi_Alarm_Inhibition_cond). This includes possibly an upstream TSF/SSF.

2) Static, software configurable bit INHIB_alarm_name_EN, that enables such a correlation. Note that provision for the INHIB_alarm_name_EN control bit is optional. On power up, or on a HW reset, this control bit is set up with a zero. The presence of this control gives the system the flexibility to implement defect correlation.

The correlated defect (Unlatched Alarm generated after being operated on by the inhibition function) gives rise to two possible sets of latched alarm event bits, discussed below.

LATCHED ALARMS

Every Unlatched alarm bit (Alarm_name) has a corresponding Latched Alarm bit for interrupt generation (called LAlarm_name, if there is no associated PM/FM).

If there is Performance and Fault Monitoring associated with an unlatched alarm, then there are two separate Latched Alarm bits: (1) One for generating hardware/software interrupts (called L1Alarm_name); and (2) another to be used for PM/FM circuits (called L2Alarm_name) for PM and FM functionality. It should be noted that it is not necessary for PM/FM to be associated with every unlatched alarm, while a latched alarm must exist for every unlatched alarm.

The purpose of the Latched Alarm(s) is two-fold:

1. To generate a Hardware or Software interrupt to flag the occurrence of an alarm event to the external Host Processor or to an on-chip Processor.

2. To derive the Performance and Fault Monitoring (PM/FM) conditions.

The L1Alarm_name bits are latched read-only (R(L)), cleared on a microprocessor read (or on a system reset).

The L2Alarm_name bits, for PM/FM, are Read/Write, cleared either by the microprocessor writing a zero to this bit, or on 1-second clock boundaries (or on system reset).

The general scheme for latched alarm processing is shown below.

LATCHED ALARM BITS FOR INTERRUPT GENERATION (LALARM_NAME/L1ALARM_NAME)

The EtherMap-12 is capable of latching according to the states given in the following table. INRT(1-0) (actual Symbol names are cINRT_GRP125M (Table TBD, on page TBD), cINRT_GRP100M (Table TBD, on page TBD), cINRT_GRPTX20M (Table TBD, on page TBD), cINRT_GRPRX20M (Table TBD, on page TBD) and cINRT_SOTERN_CORE (Table TBD, on page TBD)) are global configuration bits for the group of latched alarm bits for interrupt generation (labelled as LAlarm_name in systems without PM/FM, for example LLOS; and labelled as L1Alarm_name in systems with PM/FM, for example L1LOS). The case for level triggering is included for completeness; most TranSwitch devices are doing away with that option.

At minimum, all TranSwitch devices are configurable for the positive edge only and positive/negative edge events. The negative edge only and the level triggering events are additional optional features of particular devices, to be specified in the device top level FRS. For devices that does not incorporate these options, the INRT(1-0) = (0,0) or (1,0) settings are invalid.

Table 5: Latched Alarm Bit (L1Alarm_name) Transition Selection

INRT1	INRT0	Action
0	0	All Latched Alarm bits (event bits) latch on the positive level (i.e., true state) of the Unlatched Alarm. When a Latched Alarm bit position is cleared, it re-latches if the Unlatched Alarm is still active (true). (This mode is no longer favored in TranSwitch devices; the only purpose of its inclusion is when PM/FM is not provided, this may be one option of monitoring a persistent fault).
0	1	All Latched Alarm bits (event bits) latch on the positive transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm goes inactive and then active again. This is expected to be the most frequently used mode for the Latched Alarm bits.
1	0	All Latched Alarm bits (event bits) latch on the negative transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm goes active and then inactive again. The purpose of these bits is added flexibility, in configuring all events for alarm exit conditions.
1	1	All Latched Alarm bits (event bits) latch on either the positive or negative transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm transitions again.

Software access to this set of latched alarm bits is as follows:

Normal operation: Latched Read Only, and clears on a microprocessor read, or on global resets.

Test mode: Normal Read/Write, and clear on a micro read, or on global resets. It is possible to write a 1 to any latched bit position. There is a global top level device Test Mode control bit, distributed to all constituent IP cores that defaults to 0 on power up or HW Reset.

All L /L1Alarm_name values are readable by Software, before application of masking.

The following diagram of Figure 56 illustrates the above described options.

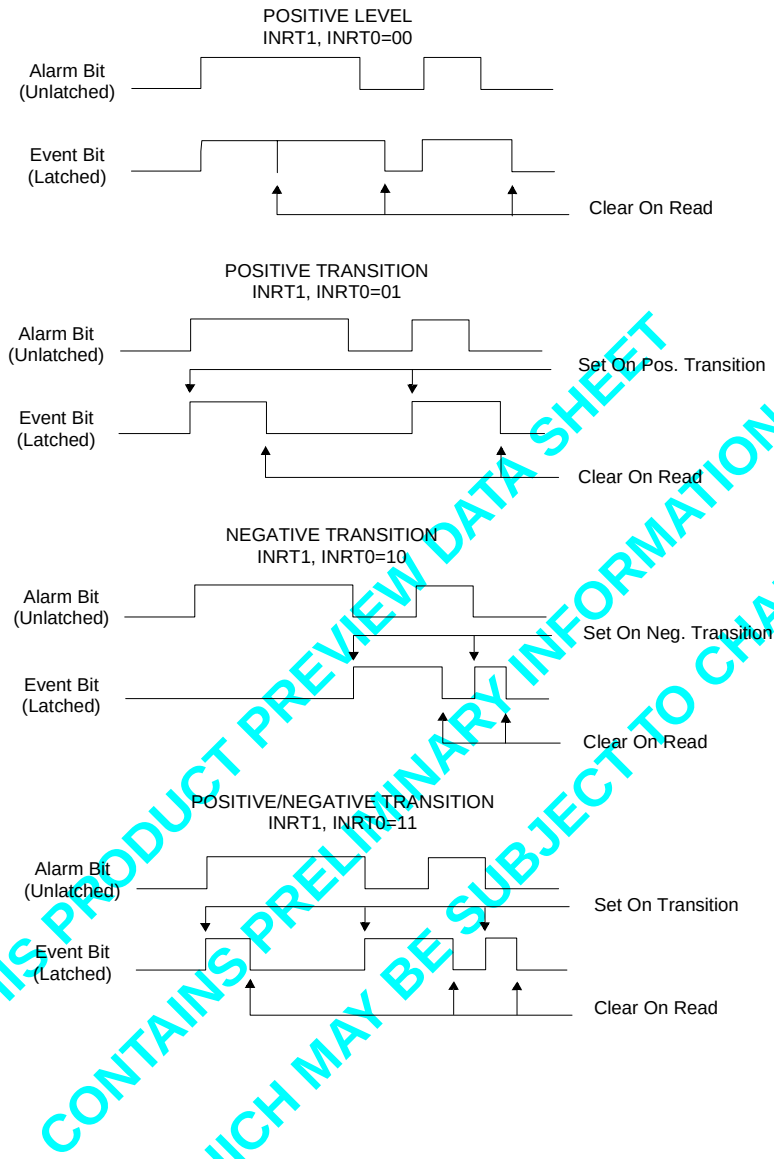


Figure 56. Latched Alarm Bit (L1Alarm_name) Transitions

LATCHED ALARM MASKING BITS (MALARM_NAME)

Each latched alarm L/L1Alarm_name has its own static masking bit that is software configurable, and is named MAlarm_name. The latched alarm combined with the state of the mask bit may generate an interrupt. These individual interrupts are grouped at various levels of hierarchy (with masking provided at each level) and finally be consolidated at a top level software polling register. Depending on individual device requirements, there could also be a single global interrupt mask bit.

The hardware interrupt capability is enabled by writing a 1 into the HINTEN control bit. When disabled, the hardware interrupt indication INT/IRQ lead is tristated (for a device/chip-level output) or, at the IP core level, the o_INT/IRQ signal is in the inactive state, even when a latched indication (event) bit is set. A software polling bit and the hardware interrupt state (when enabled by writing a 1 to HINTEN) indication occurs when one or more

bit locations in the interrupt mask bit locations are written with a '0', and the corresponding latched alarm occurs. Note that the polarity of the INT/IRQ output signal for the Intel/Motorola processor interface is selectable by selecting the appropriate microprocessor interface (not in the scope of the present specification). Please note that setting of a mask bit to 0 enables the actions by an alarm.

The Hardware interrupt state is exited when any one (or more) of the following occurs:

HINTEN control bit is written with a 0

Alarm Mask bit is written with a 1

Latched alarm bit position is cleared

The Software Polling indication is zero when any one (or more) of the following occurs:

Alarm Mask bit is written with a 1

Latched alarm bit position is cleared

Please note that a latched alarm will re-latch if the alarm is active for a positive level transition.

SECONDARY LATCHED ALARM INHIBITION

The process of 'Defect Correlation' in [G806] (refer Section 3.2.1 for references to Defect Correlation), maybe done at the Latched Alarm level. This process is optional to the process described in Section 3.2.1. Note the difference: the process in Section 3.2.1 suppresses generation of the Unlatched alarms, whereas, this process allows the Unlatched alarm to be generated.

The Latched Alarm is inhibited dynamically, depending on system alarm hierarchy to prevent unnecessary automatic latching of secondary alarms which arise as a consequence of some primary root cause alarm.

The above inhibits the generation of unnecessary interrupts, while at the same time, allow the monitoring of the secondary alarms for optional report generation, as certain standards require, since the Unlatched alarms are readable, and their generation is not suppressed (As an example of such a standard, the BellCore/TelCordia GR-253, Sept. 2000: Section 6.2.1.8.4, R6-293 and R6-294, may be cited).

There are three components for the function:

1) Active high Alarm Inhibition condition based on upstream or primary or root cause alarms; (Active_Hi_Alarm_Inhibition_cond).

2) Static, software configurable bit INHIB_alarm_name_EN, that enables such an inhibit (Note that provision for the INHIB_alarm_name_EN control bit is optional). On power up, or on a HW reset, this control bit is set up with a zero.

3) Delayed release of Unlatched alarm signal for interrupt generation when the inhibition condition for the secondary latched alarm is removed ('off-delay' timer). This blocks the generated secondary alarm for sufficiently long duration so that its delayed exit after the exit of the Primary alarm is kept from actuating the secondary latched event. For example, for a VT Demapper, the VT AIS alarm exit could take 3 SONET/SDH multiframes, or 1.5 milliseconds to integrate. If an Upstream AIS alarm is used to inhibit the VT AIS alarm, the inhibit function could stay in effect for 1.5 ms after the Upstream AIS alarm exits.

The Unlatched Alarm when not blocked by the inhibition function, gives rise to two possible sets of latched alarm event bits, discussed above and below.

LATCHED ALARM BITS FOR PM/FM (L2ALARM_NAME), PERFORMANCE MONITORING (PM BITS; PALARM_NAME) AND FAULT MONITORING (FM BITS; FALARM_NAME)

The Latched Alarm bits for PM/FM are capable of latching according to the states given in the following table. LPF(1-0) are global configuration bits for the group of latched event bits for PM/FM. These bits are named L2Alarm_name, corresponding to the Unlatched Alarm, Alarm_name. Also, the corresponding PM and FM bits are named PAlarm_name and FAlarm_name (as an example, the PM/FM bits for the OOF alarm is called POOF and FOOF respectively).

Software access to this set of latched event bits:

Normal mode: Latched Read Only; Writable for 0's only. These latched event bits for PM/FM are cleared by writing them with a zero by the microprocessor, or, on 1-second clock rising edges, or on global resets. Writing 1's have no effect.

Test mode: Normal Read/Write. Are cleared on writing them with a zero by the microprocessor, or, on 1-second clock rising edges, or on global resets.

Masking does not apply to these bits. However, inhibition does apply.

PM/FM registers have a hierarchy that is identical to the basic system alarm hierarchy, that governs the interrupt hierarchy.

Note that 1-second interval boundaries are used to determine the state of a given Alarm or event over the immediately preceding 1-second interval; whether an alarm persisted for multiple seconds; to obtain 1-second performance counts; and to operate the 1-second Performance and Fault Monitoring registers, and Performance Counter shadow registers. The 1-second clock may be an external input, that is distributed globally throughout the device, or, obtained inside the device as a derivative of some other external reference input. The 1-second clock input is synchronized with respect to the time base that the Host microprocessor uses to initiate the 1-second reads. It is extremely important that this be so since otherwise, PM/FM data and performance counts may be lost.

The table below shows the action of these control bits, in selection of the active transition in the main unlatched alarm for setting the latched event bits:

Table 6: Latched Alarm Bit (L2Alarm_name) Transition Selection

LPF1	LPF0	Action
0	0	Latched status bits for PM/FM disabled.
0	1	Latched status indication sets on positive alarm transition.
1	0	Latched status indication sets on negative alarm transition.
1	1	Latched status indication sets on both positive and negative alarm transitions.

The PM/FM latched event bit and the main unlatched alarm together set up the PM/FM indication bits as shown in the following timing diagrams, for all the three active options of the LPF(1-0).

The PM/FM 1-second shadow registers are enabled with the control bit SRGEN set to 1. This control bit also enables the 1-second PM Counter shadow registers if applicable. Note that the PM/FM registers can be cleared either by the microprocessor writing zeros to these locations of the memory map, or on the rising edges of the 1-second clock.

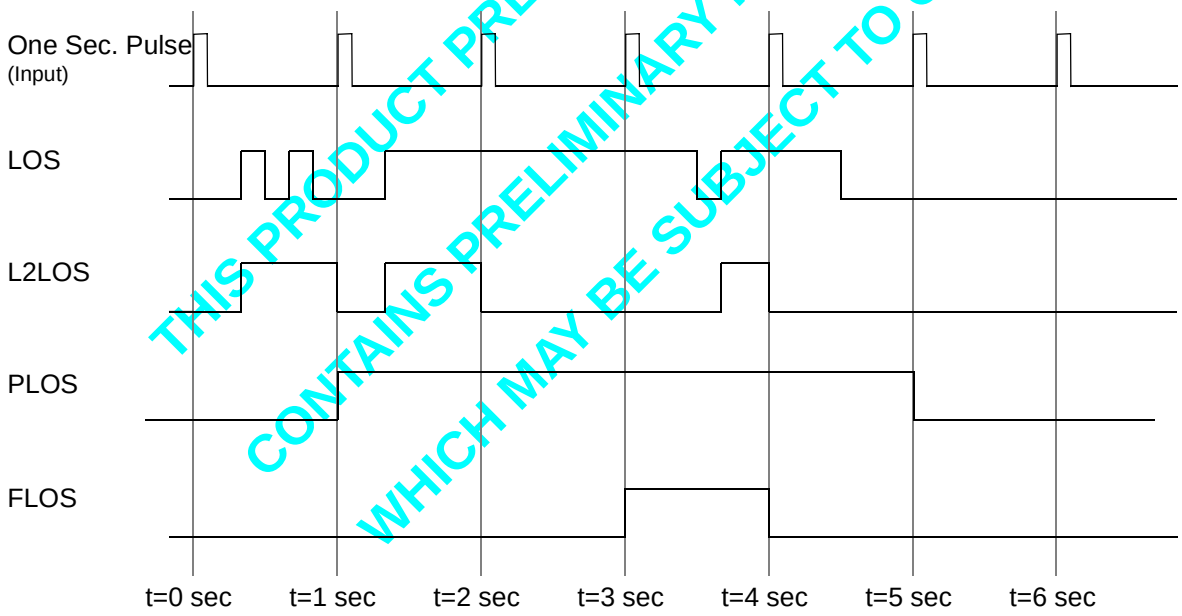
Positive Edge Events

The following diagram shows the case for the rising edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 01, the transition from 0 to 1 of the LOS alarm will cause the L2LOS bit to latch. (The alarm status can be determined by reading periodically the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place).

Assume that the PM/FM shadow registers are enabled. Then on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate (a) the Unlatched Alarm entered in the preceding 1-second interval, OR (b) the current unlatched alarm was active for at least the entire preceding 1-second interval. In addition, the FM indication bit FLOS is set if the alarm is active, but the transition to the active state did not occur in the last 1-second interval (i.e., the alarm has persisted for longer than 1-second). The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, LOS+L2LOS = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, $\overline{LOS}$&L2LOS = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the transition having occurred in the immediately previous interval. Hence, the combination PLOS&$\overline{FLOS}$ = 1 is interpreted as an alarm entry in the immediately previous interval; and FLOS = 1 shows a persistent fault.



Note 1: For this example, latched events are set only on positive event transitions.

Note 2: PLOS = LOS + L2LOS evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: FLOS = LOS & $\overline{L2LOS}$ evaluated at 1-second boundaries (where '&' is a logical and, and $\overline{X}$ is a logical inversion).

Figure 57. Positive Edge Event - PM/FM Signal Generation

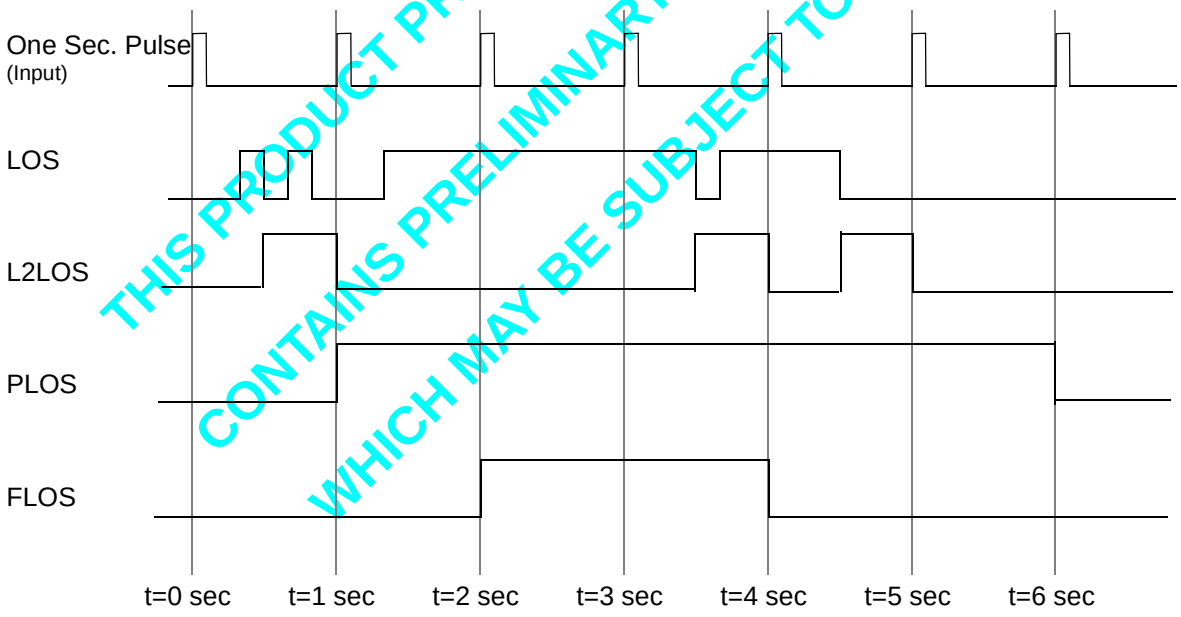
Negative Edge Events

The following diagram shows the case for the falling edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 10, the transition from 1 to 0 of the LOS alarm causes the L2LOS bit to latch. The L2LOS alarm event now signifies an alarm exit. As in the previous case for the rising edge transition, the alarm status can be determined by periodically reading the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place.

Assume that the PM/FM shadow registers are enabled. Then, on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate either: (a) the Unlatched Alarm exited in the preceding 1-second interval, or (b) the current unlatched alarm was active for at least the entire preceding 1-second interval. For the negative transition case, the FM indication bit FLOS is set if the alarm is active, AND the alarm did not clear in the last 1-second interval. The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, LOS+L2LOS = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, LOS&$\overline{\text{L2LOS}}$ = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the negative edge transition having occurred in the immediately previous interval. Hence, for the NEG EDGE event, the combination PLOS&$\overline{\text{FLOS}}$ = 1 is interpreted as the alarm LOS cleared in the immediately previous interval; and FLOS = 1 shows a persistent fault, or the unlatched alarm occurred in the previous interval.



Note 1: For this example, latched events are set only on negative event transitions.

Note 2: PLOS = LOS + L2LOS evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: FLOS = LOS & $\overline{\text{L2LOS}}$ evaluated at 1-second boundaries (where '&' is a logical and, and $\overline{\text{X}}$ is a logical inversion).

Figure 58. Negative Edge Event - PM/FM Signal Generation

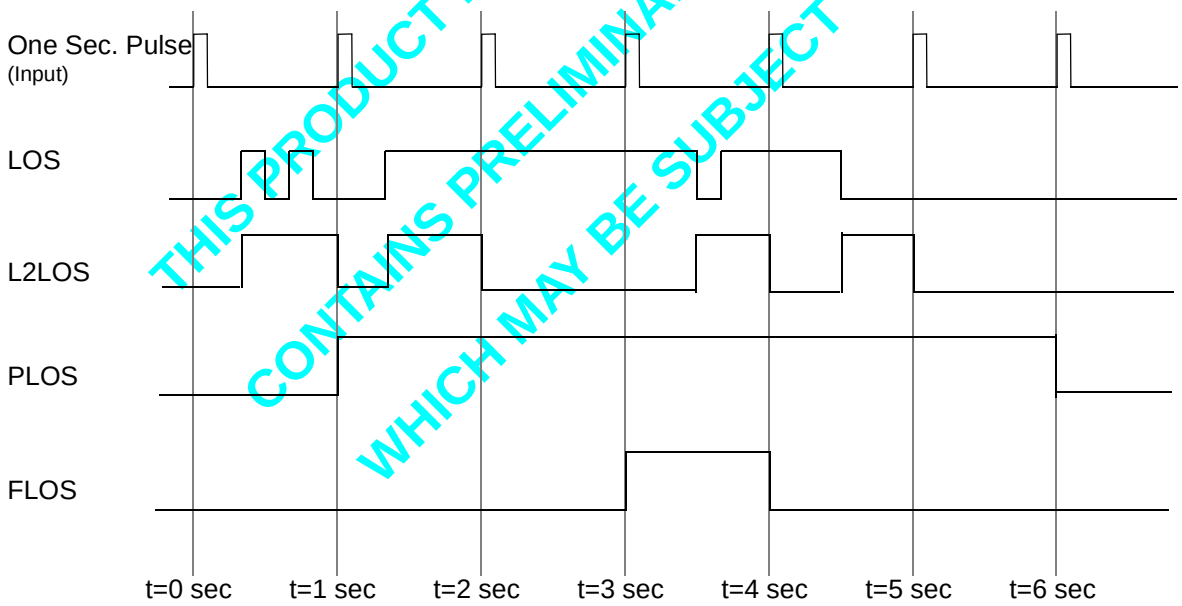
Positive or Negative Edge Events

The following diagram shows the case for the rising or falling edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 11, the transition from 1 to 0, or, from 0 to 1, of the LOS alarm causes the L2LOS bit to latch. The L2LOS event now signifies either an alarm entry or exit. The alarm status can, as in the previous cases, be determined by reading periodically the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place.

Assume that the PM/FM shadow registers are enabled. Then, as before (for the rising edge only or falling edge only cases), on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate either: (a) there was an alarm event, either entry or exit, in the Unlatched Alarm in the previous 1-second interval; OR (b) the Unlatched Alarm has been asserted over the past 1-second interval. For the positive or negative transition case, the FM indication bit FLOS is set if the alarm is active, AND the alarm did not enter or clear in the last 1-second interval (i.e., the alarm has persisted for longer than 1-second). The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, LOS+L2LOS = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, LOS&$\overline{\text{L2LOS}}$ = 1, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the transition having occurred in the immediately previous interval. Hence, for the POS or NEG EDGE event, the combination PLOS&$\overline{\text{FLOS}}$ = 1 is interpreted as the alarm LOS entered or cleared in the immediately previous interval; and FLOS = 1 shows a persistent fault, with the unlatched alarm transition, positive or negative, NOT having occurred in the previous interval.



Note 1: For this example, latched events are set on positive or negative event transitions.

Note 2: PLOS = LOS + L2LOS evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: FLOS = LOS & $\overline{\text{L2LOS}}$ evaluated at 1-second boundaries (where '&' is a logical and, and $\overline{\text{X}}$ is a logical inversion).

Figure 59. Positive/Negative Edge Event - PM/FM Signal Generation

OVERALL ALARM GENERATION AND PM/FM PROCESS DIAGRAM

The following is a signal flow diagram that illustrates the process of generating the L1Alarm_name and L2Alarm_name bits from the common starting input of the Unlatched Alarm (Alarm_name). The diagram is based on the Alarm inhibition process. Included is a basic view of the logic diagram used for setting the software polling bits and the hardware interrupt (where & is an "and" function, and + is an "or" function), using the L1Alarm_name, and the corresponding Mask bit. Note the diagram shows a simplified situation, without any hierarchies. The 'Off Delay' is the time for which the inverter output is held low after the alarm inhibition condition is removed (when INHIB_Alarm_name_EN = 1). A clock together with a counter could be used to realize this delay; the clock is such that counter sizes are minimized, while providing the appropriate level of granularity, so that the smallest required delay can be realized efficiently. The PM/FM Bit generation starting from the L2Alarm_name bit is included. Note that both the L1Alarm_name and the L2Alarm_name bits are subject to the same inhibiting condition.

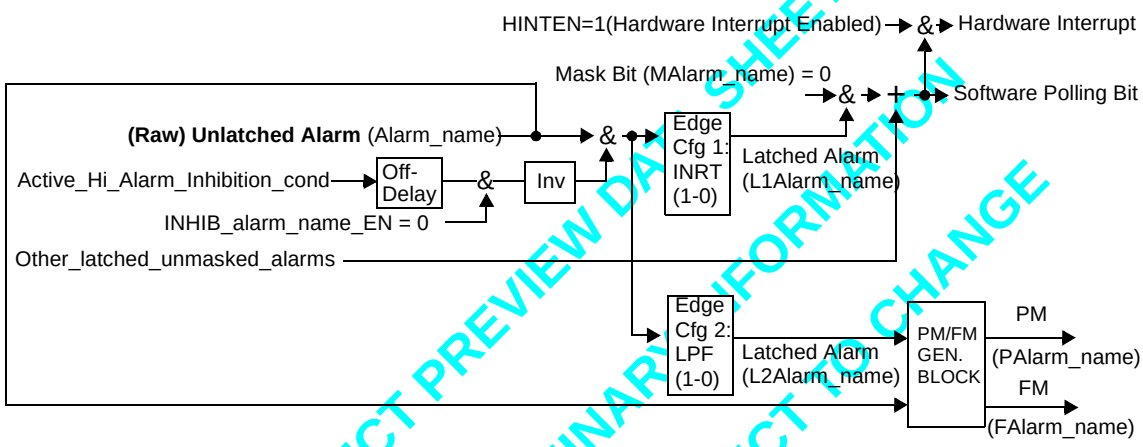


Figure 60. Alarm, Interrupt and PM/FM Generation Process

If the Alarm Inhibition function is adopted, then the signal simplifies as follows:

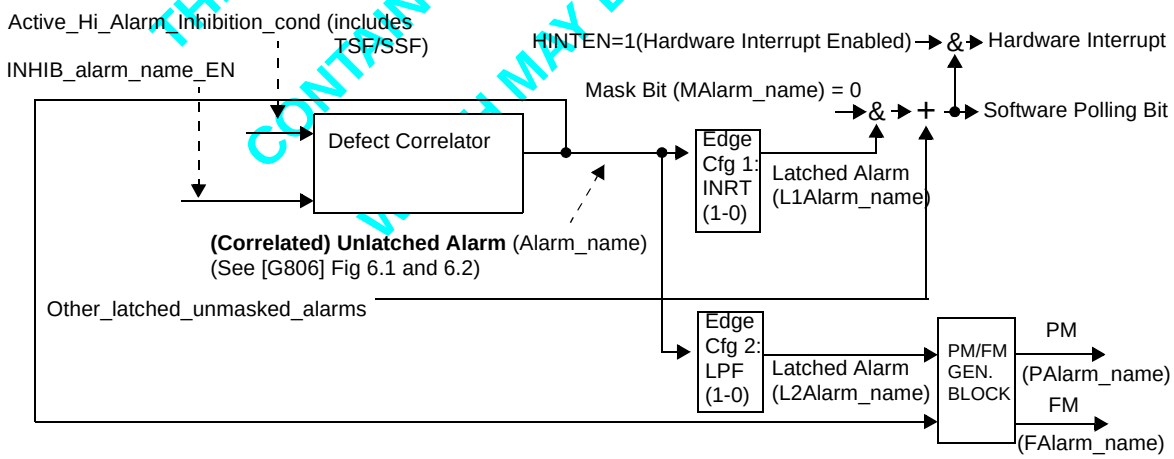


Figure 61. Alarm, Interrupt and PM/FM Generation Process (Inhibition Function)

PERFORMANCE COUNTERS

Performance Counters in the EtherMap-12 device use two different schemes, as dictated by their respective functions:

Scheme A - Counters with Roll-Over/Saturation Option

These performance counters are configurable to be either saturating or non-saturating.

When the performance counters are configured to be saturating, the counters stop at their maximum count. In the saturating mode, counts that occur during a micro read cycle, are held off and the counter updates later. A saturating counter is reset to zero on a microprocessor read cycle.

When the performance counters are configured to be non-saturating they roll over to 0 on the next count after the maximum count is reached (i.e., all ones). In this mode, the counters do not clear on a microprocessor read cycle, but continue to count. When a “reset counters” operation is performed, these performance counters are set to an all-zeros value.

This type of counter is used in the following two areas:

The Encapsulation and Decapsulation blocks, with performance counters described in Tables (TBD). Control bit CROV (address TBD) selects between saturate and roll-over.

The Ethernet MAC blocks, with performance counters described in Tables (TBD). Control bit AUTOZ (address TBD) selects between saturate and roll-over.

All performance counters may be reset simultaneously by writing a 91H to top level register RESETC.

All counters in the device that can be read by the microprocessor, are of the 'Read/Write' type, and for test purposes, the microprocessor is able to write any value to them.

A status alarm bit COUNT with an associated interrupt mask bit MCOUNT is provided. The COUNT status bit is set when any of the performance counters has reached its maximum value in the saturating mode of operation only. When a microprocessor reads the saturated counter, the counter is cleared, but the latched alarm (LCOUNT) is not cleared unless read and cleared separately.

Scheme B - Performance Counters with 1-second Shadow Register Option

The differences from scheme A, are:

1. There are designated bits (1 bit for each counter) available, that take up counter overflow, for each counter.

2. In the event that a terminal count is reached, the overflow bit is used as an indicator. There is no equivalent of the CROV configuration bit as in the case of scheme A.

3. The Counters can only be cleared by the rising edge of a 1-second interval boundary, or, if the microprocessor writes 0’s to the counters. The counters are reset to all 0’s.

4. At the 1-second boundary, the contents of the Performance counter are transferred, along with the overflow indication bit, to a 1-second shadow register for the particular counter, after which the counter is cleared. Thus, the 1-second shadow register for the performance counter updates only on 1-second boundaries.

5. The 1-second shadow registers are enabled with the common shadow register enable control bit, SRGEN.

6. There is no equivalent of the COUNT alarm, for saturated counter operation, as with Scheme A.

Clearing/Resetting of Performance Counters in Scheme B, is accomplished in a manner similar to that of Scheme A.

The shadow register holds its count during a microprocessor read cycle. However, the main Performance Counters may be updated internally on a coincident 1-second boundary, for a count update.

This type of counter is used in the TX Mapper and RX DeMapper block.

ALARM FEATURE COMBINATIONS

Each defined system alarm or event, have associated with it one of the following groups of features:

Group 1:

- A main unlatched alarm signal (Alarm_name).
- A Latched Alarm Indication an Unlatched Alarm, for the purpose of status and interrupt generation (L1Alarm_name).
- Latched Alarm Interrupt Mask bit (MAlarm_name).

Group 2:

- Features Group 1.
- A Latched Alarm Indication for an Unlatched Alarm, for the purpose of 1-second Performance and Fault Monitoring (L2Alarm_name).
- 1-second PM bit (PAlarm_name).
- 1-second FM bit (FAlarm_name).

Group 3:

- Features Group 1.
- Performance Counter.

Group 4:

- Features Group 2.
- Performance Counter.

Group 5:

- Performance Counter Only; Note that there may be Performance Counters that are not associated with any alarm (for example, SONET/SDH Pointer Justification Counters).

Group 6:

- A Latched Alarm Indication for the main unlatched system alarm or event, for the purpose of 1-second Performance and Fault Monitoring (Alarm 2).
- 1-second PM bit.
- 1-second FM bit.
- Performance Counter.

It is the responsibility of the individual device's specification to completely specify for each alarm, the following:

1. Group of features applicable.
2. Main Unlatched Alarm Entry Condition, with standard reference if applicable.
3. Main Unlatched Alarm Exit Condition, with standard reference if applicable.

4. Alarm Action.

5. Hierarchical position of the alarm, that is what secondary alarms and Performance Counter(s) are inhibited on its occurrence.

6. The decision to implement a Scheme A or Scheme B Performance Counters (on a per counter basis, if applicable).

7. Inhibition Definition, Inhibition Extension Times, and Enable control bits as applicable.

SYSTEM ALARM, INTERRUPT, AND PM/FM HIERARCHY

The System Alarm and Interrupt Hierarchy are device specific, and aimed towards providing a convenient software interrupt nesting, so that poll times are considerably reduced. The PM/FM registers follow a similar hierarchy, only difference being that the PM/FM bits are not subject to masking (they are subject to inhibition however).

In general, the Alarm and Interrupt Hierarchy follow one or more of the following grouping schemes:

- Protocol Layers, example for SONET/SDH devices, Section Layer, Line/HO Path Layer, LO Path Layer.
- Channel Numbers (example, alarms/masks grouped based on VT numbers for HDM, or channel numbers for framers etc.).
- Alarm Functionality (e.g., global alarm for a VT LOP condition).
- Receive/Transmit or other special hierarchical groupings).

Each latched alarm bit has a mask bit. In addition, depending on the grouping chosen, each hierarchical level has a consolidated Latched Alarm and associated Mask; may also have PM/FM bits, depending on Alarm Feature Group specified.

The software polling interrupt register provides a way to have the processor poll a register in memory (provided the proper interrupt mask disable bits are set) to indicate the alarms that causes the interrupt or the alarms that are set without having to read all the alarm registers until the active alarm is found.

There is also a hierarchical alarm inhibition scheme that may be implemented, based on needs and standards. The diagram of Figure 62 below illustrates how an alarm and interrupt hierarchy is to be achieved:

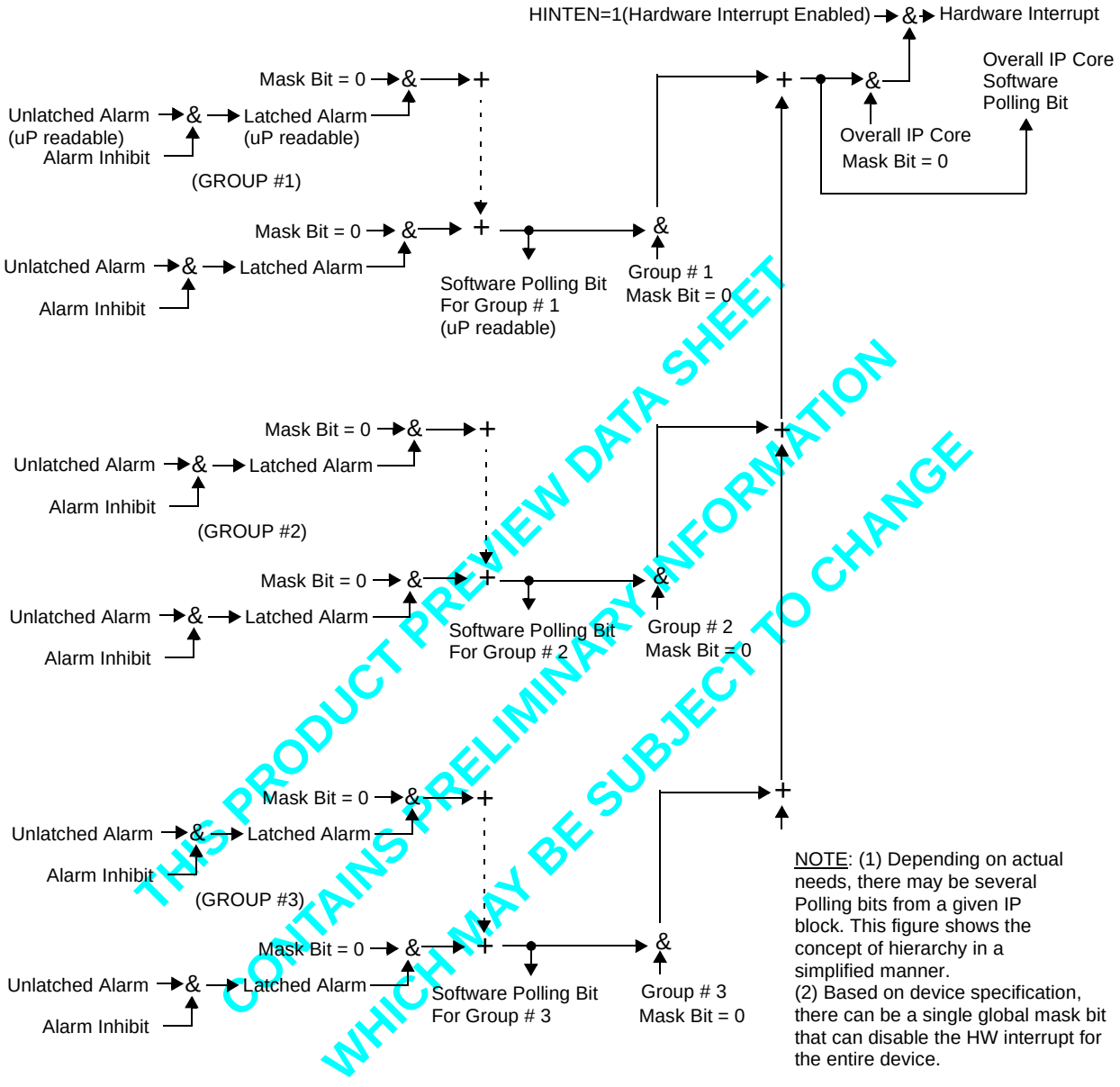


Figure 62. Alarm Interrupt Hierarchy

MAPPER/DEMAPPER PERFORMANCE MONITORING

Pointer Adjustment Counters per Level 3 High Order path:

- Incoming Positive Pointer Adjustment Count,
- Incoming Negative Pointer Adjustment Count.

Pointer Adjustment Counters per Low Order path:

- Incoming Positive Pointer Adjustment Count,
- Incoming Negative Pointer Adjustment Count.

POH counters per High Order Path:

- B3 Near-End Errored BIP Count,
- B3 Near-End Errored Block Count,
- G1 Far-End Error Count, configurable to count either REI errors or errored blocks,
- Near-End Defect Second,
- Far-End Defect Second.

POH counters per Low Order Path:

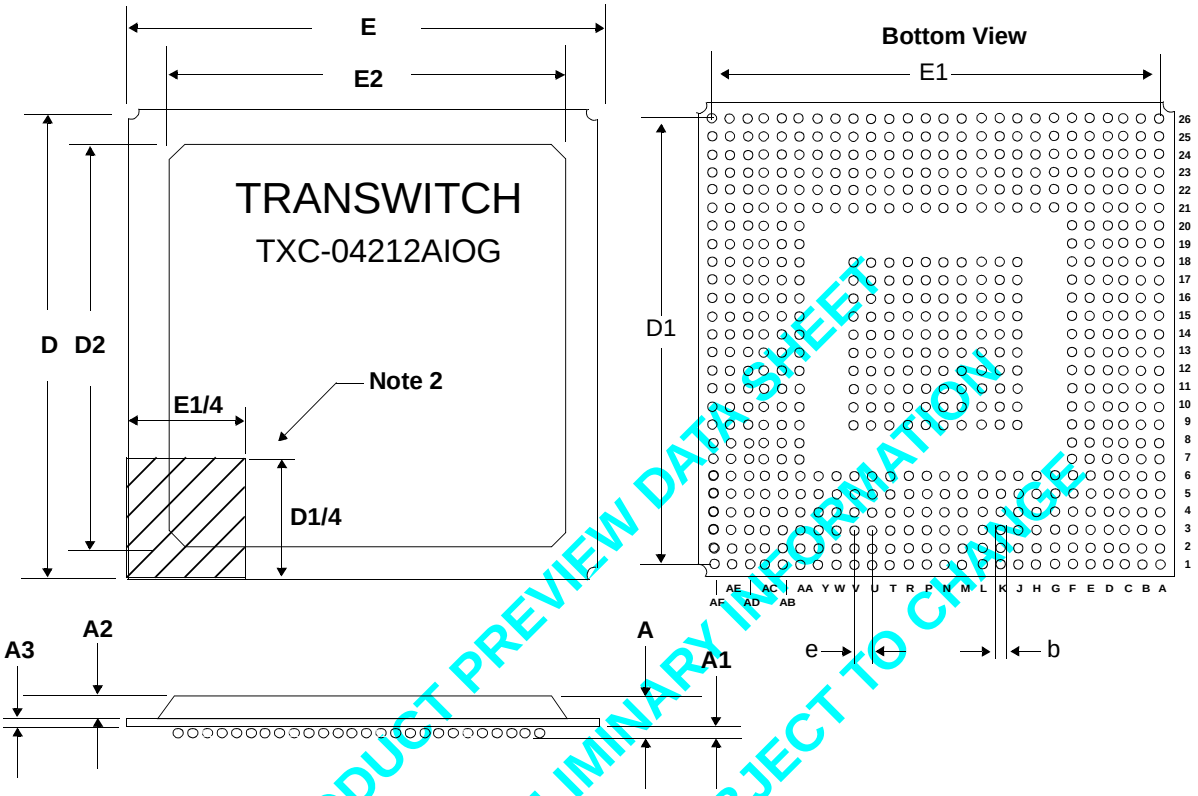
- V5 Near-End Errored BIP Count,
- V5 Near-End Errored Block Count,
- V5 Far-End Errored Block Count,
- Near-End Defect Second,
- Far-End Defect Second.

All performance counters are one second shadow registers and at the one second boundary, the contents of each performance counter is latched into its one second shadow register, after which the performance counter is cleared. These one second shadow registers will hold their value during the entire period between two subsequent one second boundaries.

The one second shadow registers are available for software read-only access. All performance counters are saturating: counting will stop when the maximum count value is reached. All errored BIP and Block counters are dimensioned to cover the maximum count value during a one second interval meaning they can never reach saturation.

PACKAGE INFORMATION

The EtherMap-12 device is packaged in a 27 millimeter (mm) × 27 mm, 580-Lead plastic ball grid array (PBGA) suitable for surface mounting, as shown in Figure 63.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 26 x 26, JEDEC code MO-151.

Dimension (Note 1)	Nominal
A A1 A2	2.23 Nom. 0.5 1.17
A3 (Ref.)	0.56 Nom.
b (Ref.)	0.63 + .07/- 0.13
D	27.0
D1 (BSC)	25.0
D2	25
E	27.0
E1 (BSC)	25.0
E2	25
e (BSC)	1.0

Figure 63. EtherMap-12 TXC-04212 Package Diagram

PRODUCT PREVIEW

ORDERING INFORMATION

Part Number: TXC-04212AIOG 580-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

TXC-03453B, TL3M Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-04222, TEMx28 Device (21/28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04226B, EtherMap-3 Device (Ethernet into STS-3/STM-1 SONET/SDH Mapper). The EtherMap-3 is a highly integrated device that provides for mapping of 10/100/1000 Mbit/s Ethernet into SONET/SDH STS-3/STM-1 Transport payloads. The device supports connection for up to eight 10/100 Mbit/s Ethernet ports, using SMII interfaces, or a single 1000 Mbit/s Ethernet port, using a GMII interface. In the transmit direction, for each port, received Ethernet frames are encapsulated using either GFP, LAPS or LAPF protocol.

TXC-06103, PHAST-3N Device (SDH/SONET STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06212, PHAST-12E Device (Programmable, High-Performance ATM/Packet/Transmission SONET/SDH Terminator for Level 12). A highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher-Order multiplexing, and transmission applications. This PHAST-12 device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06312, PHAST-12N Device (STM-4/OC-12 SDH/SONET Overhead Terminator with Telecom Bus Interface). A highly integrated SDH/SONET overhead terminator device designed for TDM payload mappings. A single PHAST-12N can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each SDH/SONET terminator has a line interface block that performs clock synthesis and clock recovery for four 155 Mbit/s signals or a single 622 Mbit/s serial signal.

TXC-06603, POP-12 Device (OC-12 SONET/SDH Path OVerhead Processor, Retimer, and Cross Connect). The POP-12 integrates VC-3/VC-4 POH processing, AU-3/AU-4 pointer processing retiming, and VC-3/VC-4 cross connect for four Telecom Bus interfaces into one package. It provides an interface to high density mapper applications when used with the TranSwitch PHAST-12E (TXC-06212), and mapper and framer devices. The POP-12 device is designed to provide a seamless interface to the PHAST-12E device.

TXC-06840, Envoy-8FE Device (Octal Fast Ethernet controller). The Envoy-8FE Device is a Serial Media Independent Interface (SMII) to POS-PHY Level 2/3 interface converter transporting Ethernet packets. Envoy-8FE has 8 SMII ports. Packet data from the 8 ports are aggregated onto the POS-PHY interface.

TXC-06842, Envoy-2GE Device (Dual Gigabit Ethernet Controller). The Envoy-2GE Device is a Gigabit Media Independent Interface (GMII) to POS-PHY Level 2/3 interface converter transporting Ethernet packets. Envoy-2GE has 2 GMII ports. Packet data from the 2 ports are aggregated onto the POS-PHY interface.

REFERENCE DOCUMENTS

[1] MPC8260 PowerQUICC User's Manual, MPC8260UM, 4/1999, Rev. D

[2] MPC8260 PowerQUICC User's Manual Errata, MPC8260UMAD/D, 10/2002, Rev 6

[3] MPC8260 GPCM Timing Diagram, App. Note, 8/2000, Rev. 1.0

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007
Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

PRODUCT PREVIEW

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated EtherMap-12 device Data Sheet that have significant differences relative to the previous and now superseded EtherMap-12 Data Sheet:

Updated EtherMap-12 device Data Sheet: *PRODUCT PREVIEW* Edition 2, November 2003

Previous EtherMap-12 device Data Sheet: *PRODUCT PREVIEW* Edition 1A, June 2003

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
Where occurred	Changed 0640 to 2800, 64-byte to 128-byte and 64-byte to 520-byte.
10	Changed last bullet of "Tx and Rx EoS Processors" section.
11	Added last bullet to "10/100/1000 Mbps Ethernet MAC Blocks" section. Changed fourth bullet of "SDRAM Interfaces" section. Changed "Microprocessor Interface" section.
12	Changed the diagram of Figure 1.
13	Changed "Block Diagram Description" section.
14	Changed "SDRAM Memory Interfaces" section.
22 - 44	Added 'Lead No' for its 'Symbol'.
24	Changed Name/Functions for Symbols TBAC1J1V1 and $\overline{\text{TBADD}}$.
25	Changed paragraph above table. Changed Type and Name/Function for Symbol ETNTXGCLK. Changed Name/Function for Symbol ETNTXEN.
26	Changed Name/Functions for Symbols ETNRXDV, ETNRXCLK, ETNMDIO and ETNMDC.
28	Changed Name/Function for Symbol SD1CLKA.
31	Changed Name/Function for Symbol SD2CLKA.
33	Changed Name/Function for Symbol POHTXDLE1.
36	Changed Note below "HOST PROCESSOR INTERFACE SELECTION" table.
43	Changed Symbol for Lead No. AE5. Changed Name/Functions for Symbols TESTIN7-TESTIN0 and TESTOUT7-TESTOUT0.
44	Changed Name/Function for Symbol SCANIN39-SCANIN8.
45	Changed TBD to 16 in the "Thermal Characteristics" table.
46 - 49	Updated "Input, Output and Input/Output Parameters" section.
50	Changed Notes 2 and 3.
51	Added Note 4 and changed Notes 2 and 3.
53	Added Note 4 and changed Notes 2 and 3.
54	Changed Min and Max values, and Unit for Symbol t_{PWH}.
55	Changed title of Figure 12. Changed Unit for Symbol t_{PWH} in the table.
56	Changed title of Figure 13.
58	Changed the diagram of Figure 15 and the table.

Page Number of Updated Data Sheet	Summary of the Change
59	Changed the diagram of Figure 16 and the table.
60	Added new Figure 17 and the table.
61	Added new Figure 18 and the table.
66	Corrected the diagram of Figure 23 and changed Notes 2 and 3.
67	Corrected the diagram of Figure 24.
68	Corrected the diagram of Figure 25 and changed Notes 1 and 2.
69	Corrected the diagram of Figure 26.
71, 73, 75, 77, 79, 81, 83, 85	Reformatted tables.
98	Added "STS-1/AU-3/AU-4 Pointer Generation" section. Changed "TU/VT Pointer Generation" section.
100	Changed "General" section.
105	Changed paragraphs below Figure 38.
108	Changed first four paragraphs of "Low Order Virtual Concatenation with LCAS" section.
109	Changed first four paragraphs of "High Order Virtual Concatenation without LCAS" section.
110	Changed paragraph above Figure 45.
111	Changed paragraph above Figure 46.
112	Changed first four paragraphs of "High Order Virtual Concatenation with LCAS" section.
113	Added "Configuration" section.
115	Added "Differential Delay Compensation" section.
118	Changed the diagram of Figure 48.
119	Changed "Ethernet MAC Blocks" section.
120	Added "Ethernet Half Duplex" section.
122	Changed "Flow Control Operation" section.
124	Changed "Encapsulation / Decapsulation" section.
133	Changed "GFP Host Extraction of Management/Control Frames" title and text above tables.
172	Changed "SDRAM Controllers" section.
175	Added "Reset Operation" section.
194	Added "Performance Counters" section.
199	Updated "Package Information" section.
200	Updated "Ordering Information" section.
202	Updated "Standards Documentation Sources" section.
204	Changed "List of Data Sheet Changes" section.

-NOTES-

PRODUCT PREVIEW

THIS PRODUCT PREVIEW DATA SHEET
CONTAINS PRELIMINARY INFORMATION
WHICH MAY BE SUBJECT TO CHANGE

PRODUCT PREVIEW information documents contain information on products in their formative or design phase of development. Features, characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.

-NOTES-

TranSwitch Corporation • 3 Enterprise Drive • Shelton, CT 06484 USA • Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com