

FEATURES

- Eight 10/100 Mbit/s Ethernet ports, each using a SMII interface
- Single 1000 Mbit/s Ethernet port, using a parallel GMII interface (lead shared with SMII interfaces)
- Ethernet Management interface for control and configuration of externally connected PHYs
- Provides IEEE 802.3 Half Duplex mode on 10/100 Mbit/s and Full Duplex mode on 10/100/1000 Mbit/s Ethernet ports
- Provides IEEE 802.3 Management Statistics (RMON)
- Ethernet frame encapsulation/decapsulation protocols:
 - ITU-T G.7041, Generic Framing Procedure (GFP)
 - ITU-T X.86/X.85, Link Access Procedure SDH (LAPS)
 - ITU-T Q.922, Link Access Procedure Frame Mode (LAPF)
 - RFC1662/3518, PPP Bridging Control Protocol (BCP)
- Performs mapping/demapping of encapsulated Ethernet frames into/from low order (VT1.5 SPE/VT2 SPE/VC-11/VC-12) and high order (STS-1 SPE/VC-3) virtually concatenated payloads
- Performs mapping/demapping of encapsulated Ethernet frames into/from a single contiguous concatenated (STS-3c-SPE/VC-4) payload or a single Low/High order (VT1.5/VT2/VC-11/VC-12/STS-1/VC-3) payload
- Dynamic bandwidth allocation using on-chip LCAS processing (ITU-T G.7042) for low and high order virtual concatenated payloads
- Glueless memory interface to external 64/128/256 Mbit SDRAMs
- Low Order POH and Pointer processing for 84/63 VT1.5/VT2/TU-11/TU-12 and 3 TU-3
- High Order POH processing for STS-1 SPE/VC-3/STS-3c SPE/VC-4
- Byte-wide 19 MHz parallel Add and Drop Telecom Bus interfaces
- Per-port Ethernet side and SONET/SDH system side loopback for system level diagnostics
- 16-bit wide microprocessor interface, selectable between Motorola or Intel
- Boundary scan (IEEE 1149.1 standard)
- + 3.3V and +1.8V power supplies, 5V tolerant I/O leads
- 400-lead plastic ball grid array package (PBGA, 27 mm x 27 mm)
- Device Driver

DESCRIPTION

The EtherMap®-3 Plus is a highly integrated EoS device that provides for mapping of 10/100/1000 Mbit/s Ethernet into SONET/SDH STS-3/STM-1 Transport payloads. The device supports connection for up to eight 10/100 Mbit/s Ethernet ports, using SMII interfaces, or a single 1000 Mbit/s Ethernet port, using a GMII interface. Ethernet frames are encapsulated using either GFP, LAPS, LAPF or PPP/BCP protocol. The encapsulated Ethernet frames are then mapped into either virtually concatenated low or high order payloads, such as VT1.5 SPE/VT2 SPE/VC-11/VC-12/STS-1 SPE/VC-3, or into contiguously concatenated payloads such as STS-3c SPE/VC-4. Low and high order SONET/SDH POH generation and processing/termination is performed. A byte-wide parallel interface Telecom Bus format provides the SONET/SDH interface and may support either Drop bus or Add bus timing modes.

In addition to support for full-rate Ethernet transfer, over-subscribed Ethernet transfers are also supported using back pressure mechanisms (half and full duplex flow control) in order to prevent frame loss. External SDRAM is used for buffering Ethernet frames to support bandwidth oversubscription and flow control operation as well as receive SONET/SDH container alignment and differential delay compensation of low and high order virtually concatenated payloads.

For both low and high order virtually concatenated payloads, optional on-chip standards based LCAS processing is provided to allow hitless dynamic bandwidth adjustments.

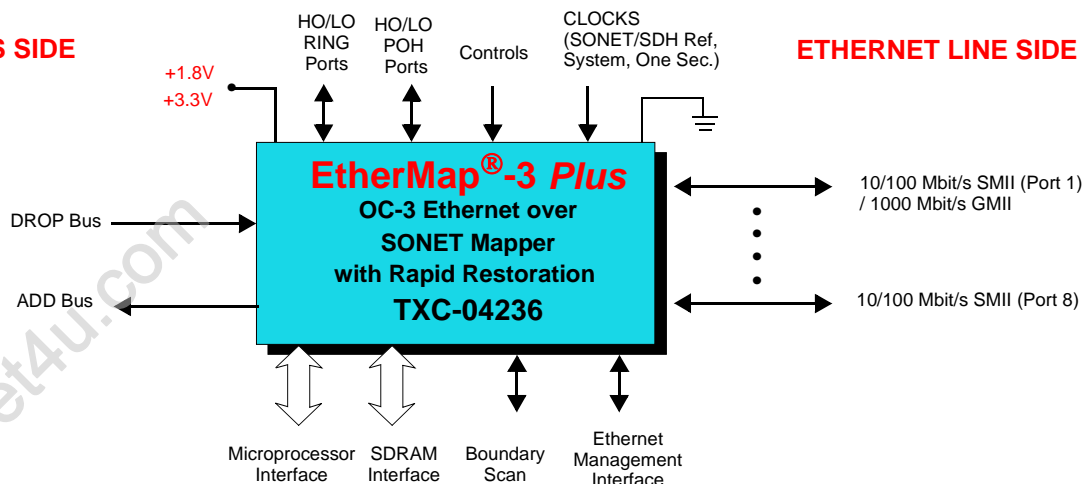
A powerful hardware and RTOS independent EtherMap device driver provides full access to all the features of the device through APIs. It utilizes matched get/set functions and can be easily ported.

APPLICATIONS

- SONET/SDH add/drop and terminal multiplexers
- Multi-service access platforms (MSAP)
- Compact Access or CPE platforms
- IP DSLAMS
- Wireless Backhaul Electronics (RNC/BSC)

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TELECOM BUS SIDE



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TABLE OF CONTENTS

| Section | Page |
|---|------|
| List of Figures | 6 |
| List of Tables | 8 |
| Features | 15 |
| Mappings | 15 |
| Encapsulation Protocols | 15 |
| Ethernet Ports | 16 |
| 10/100/1000 Mbit/s Ethernet Media Access Controller (MAC) Block | 16 |
| SDRAM Interface | 16 |
| Telecom Bus Timing | 16 |
| Alarm Indication Port Interface | 17 |
| POH Port Interface | 17 |
| Microprocessor Interface | 17 |
| JTAG Interface | 17 |
| Block Diagram | 18 |
| Block Diagram Description | 19 |
| Data Processing/Flow | 19 |
| 10/100/1000 Mbit/s Ethernet Media Access Controller (MAC) Block | 22 |
| SONET/SDH Mapping | 23 |
| Mapper Block | 23 |
| Demapper Block | 25 |
| Ethernet Ports | 27 |
| Microprocessor Interface | 27 |
| SDRAM Memory Interface | 27 |
| Parallel Telecom Bus Interface | 27 |
| High and Low Order POH (Path Overhead Byte) Port Interface | 29 |
| High and Low Order Alarm Indication Port Interface | 29 |
| Alarms and Performance Monitoring Blocks | 29 |
| JTAG Interface | 29 |
| Power-Up Sequencing | 29 |
| Application Example | 30 |
| Lead Diagram | 31 |
| Lead Descriptions | 32 |
| Absolute Maximum Ratings and Environmental Limitations (Referenced to VSS) | 47 |
| Thermal Characteristics | 47 |
| Power Requirements | 48 |
| Input, Output and Input/Output Parameters | 49 |
| Timing Characteristics | 54 |
| Operation | 93 |
| SONET/SDH Processing | 93 |
| General | 93 |
| Transmit High Order Path Termination (VC-3/VC-4/STS-1/STS-3C POH Generator) | 97 |
| General | 97 |
| J1 | 97 |
| B3 | 97 |
| C2 | 97 |
| G1 | 97 |
| H4 | 98 |
| F2, F3/Z3, K3/Z4, and N1/Z5 | 98 |
| Receive High Order Path Termination (VC-3/VC-4/STS-1/STS-3C POH Monitor) | 98 |
| General | 98 |
| J1 | 98 |
| B3 | 99 |
| C2 | 100 |
| G1 | 100 |
| H4 | 100 |
| F2, F3/Z3, K3/Z4, and N1/Z5 | 100 |
| High Order POH Port Interface | 100 |
| High Order Alarm Indication Port Interface | 101 |
| AU-4 and AU-3 Pointer Generation | 102 |
| Drop Bus Timing Mode | 102 |
| Add Bus Timing Mode 1 | 102 |
| Add Bus Timing Mode 2 | 103 |
| TU-3 Pointer Generation | 103 |
| TU-3 Pointer Tracking | 103 |
| VC-3/STS-1/TUG-3 Timeslot Interchange | 103 |
| VT/TU Pointer Tracking | 103 |
| VT/TU Pointer Generation | 103 |
| Low Order Timeslot Interchange | 103 |



TABLE OF CONTENTS (cont.)

| Section | Page |
|---|------|
| Transmit Low Order Path Termination (Low Order POH Generator) | 104 |
| General | 104 |
| J2 | 104 |
| BIP-2 | 104 |
| Signal Label | 105 |
| REI/RDI | 105 |
| K4/Z7 Bit 2 | 105 |
| V5 RFI | 105 |
| N2/Z6 | 105 |
| Receive Low Order Path Termination (Low Order POH Monitor) | 106 |
| General | 106 |
| J2 | 106 |
| BIP-2 | 106 |
| Signal Label | 107 |
| REI/RDI/RFI | 107 |
| K4/Z7 Bit 2 | 107 |
| N2/Z6 | 107 |
| Low Order and High Order Path Monitor Alarm Registers | 108 |
| Low Order POH Port Interface | 110 |
| Low Order Alarm Indication Port Interface | 111 |
| SONET/SDH Protection Switching Recovery Time | 112 |
| Virtual Concatenation and LCAS | 113 |
| Low Order Virtual Concatenation without LCAS | 113 |
| Low Order Virtual Concatenation with LCAS | 115 |
| High Order Virtual Concatenation without LCAS | 116 |
| High Order Virtual Concatenation with LCAS | 119 |
| Configuration for Virtual concatenation and LCAS | 120 |
| General | 120 |
| Configuring Transmit VCAT (Ethernet to SONET/SDH) | 121 |
| Configuring Receive VCAT (SONET/SDH to Ethernet) | 122 |
| LCAS-Specific Configuration - Transmit | 123 |
| Assigning Unused VCGs (When at least one VCG is LCAS) | 124 |
| Dynamic Mapping and Virtual Concatenation Changes | 124 |
| VCG Tributary Assignments (Adding and Removing Members) | 124 |
| Changing VCG Encapsulation/Decapsulation Mode | 126 |
| Changing VCG SONET/SDH Structure | 126 |
| Differential Delay Compensation | 129 |
| Maximum Differential Delay Allowed | 129 |
| Maximum Differential Delay Detected | 130 |
| Ethernet Support | 131 |
| SMII and GMII Interfaces | 131 |
| Ethernet MAC Blocks | 133 |
| Ethernet Frame Size | 134 |
| Ethernet Half Duplex | 134 |
| Carrier Sense | 134 |
| Collision Detection | 134 |
| Alternate BEB Truncation | 135 |
| Excessive Collisions | 135 |
| Half-Duplex Flow Control | 135 |
| Flow Control Operation | 136 |
| Overview | 136 |
| Full Duplex flow control | 136 |
| Definitions | 136 |
| Flow Control Algorithm | 136 |
| TxFIFO Overflow | 136 |
| External Pause Frames | 136 |
| Configuring Full Duplex Flow Control | 137 |
| Changing Configurations | 138 |
| Encapsulation/Decapsulation | 139 |
| Setting the Encapsulation Mode | 139 |
| Changing the Encapsulation Mode | 140 |
| GFP | 141 |
| GFP Host Insertion/Extraction of Management/Control Frames | 148 |
| GFP Linear Frame Mode Operation | 150 |
| Transmit Side Linear Extension Header | 150 |
| Transmit Side CID Configuration Tables | 150 |
| Receive Side Linear Extension Header | 152 |
| Receive Side CID Configuration Tables | 152 |
| LAPS | 153 |

TABLE OF CONTENTS (cont.)

| Section | Page |
|--|-------------|
| LAPF | 162 |
| PPP (with BCP and LCP Support) | 170 |
| SDRAM Controller | 183 |
| SDRAM Memory Interface | 183 |
| CAS Latency | 183 |
| BANK/ROW Activation | 183 |
| Commands | 184 |
| Reset Configuration of SDRAM Controller | 184 |
| Configuration Changes/Initialization | 184 |
| Microprocessor Access to SDRAM | 185 |
| Reset Operation | 186 |
| General | 186 |
| External Lead Controlled Hardware Reset | 186 |
| Microprocessor Controlled Hardware Reset | 186 |
| Microprocessor Controlled Soft Reset | 186 |
| Microprocessor Controlled Global Performance Counter Reset | 186 |
| Telecom Bus Operation | 187 |
| General | 187 |
| Drop Bus Interface | 187 |
| Drop Bus Parity Selection | 187 |
| Add Bus Interface | 188 |
| Add Bus Timing Modes | 188 |
| Add Bus Parity Selection | 189 |
| Add Bus Delay | 190 |
| Telecom Bus Tributary Activation/Tri-State Control | 191 |
| VC-3/VC-4 | 191 |
| TUG-3 | 191 |
| TUG-2 | 191 |
| TU-11/TU-12 | 191 |
| Loop Backs | 193 |
| MAC Loopback | 193 |
| Telecom Bus Loopbacks | 194 |
| Boundary Scan | 195 |
| Introduction | 195 |
| Boundary Scan Operation | 195 |
| Boundary Scan Schematic | 196 |
| Boundary Scan Chain | 196 |
| Memory Information | 197 |
| General Device Registers | 200 |
| Table 10 through 12 - General Configuration and Status of the Device | 200 |
| Ethernet MAC Registers | 201 |
| Tables 13 through 17 - Status Information of the MAC | 201 |
| Tables 18 through 23 - Configuration of the MAC | 210 |
| Tables 24 through 29 - MII Management Interface (used for MAC0 only) | 215 |
| Ethernet MAC Registers | 217 |
| Tables 30 through 34 - Configuration, Alarms and Interrupts of the Ethernet MACs | 217 |
| Tx Encapsulation Registers | 219 |
| Tables 35 through 47 - Configuration, Status and Alarms of the Encapsulation Block | 219 |
| Rx Decapsulation Registers | 236 |
| Tables 48 through 61 - Configuration, Status and Alarms of the Decapsulation Block | 236 |
| SDRAM Control Registers | 268 |
| Table 62 - SDRAM Control and SDRAM Interface Configuration | 268 |
| Table 63 and 64 - Microprocessor Access to the SDRAM (Indirect Access) | 269 |
| Tx Virtual Concatenation Registers | 270 |
| Tables 65 through 75 - Configuration, Status and Alarms of the Transmit (Ethernet to SONET) Virtual Concatenation Block | 270 |
| Rx Virtual Concatenation Registers | 283 |
| Tables 76 through 85 - Configuration, Status and Alarm of the Receive (SONET to Ethernet) Virtual Concatenation Block | 283 |
| Ethernet to SONET Handling Registers | 295 |
| Tables 86 through 90 - Configuration and Status of the Ethernet Frame Format Block (Output of the Ethernet MAC) | 295 |
| Table 91 through 103 - Ethernet Buffering and Flow Control in Transmit (Ethernet to SONET) and Receive (SONET to Ethernet) Paths | 296 |
| Tx Mapper Block Registers | 302 |
| Tables 104 through 107 - Configuration, Status and Interrupt handling of the Transmit Mapper Block | 302 |
| Tables 108 through 118 - Configuration of the Transmit Mapper Block | 302 |
| Rx DeMapper Block Registers | 306 |
| Tables 119 through 131 - Configuration, Status and Alarms for the Receive Demapper Block | 306 |



TABLE OF CONTENTS (cont.)

| Section | Page |
|--|------|
| Tables 132 through 154 - Configuration, Status and Alarms of the Low Order POH Monitor | 308 |
| Tables 155 through 162 - Configuration, Status and Alarms of the Low Order | |
| Tx Alarm Indication (RING) Port | 316 |
| Table 163 - Configuration of the Low Order Rx Alarm Indication (RING) Port | 317 |
| Tables 164 through 166 - Configuration and Status of the general Low Order Interrupt Controller | 318 |
| Table 167 - Configuration of the High Order Rx Alarm Indication (RING) Port | 318 |
| Tables 168 through 176 - Configuration, Status and Alarms of the High Order | |
| Tx Alarm Indication (RING) Port | 318 |
| Tables 177 through 209 - Configuration, Status and Alarms of the High Order POH Monitor | 320 |
| Tables 210 through 222 - Configuration, Status and Alarms of the TU-3 PTR Tracker | 332 |
| Tables 223 and 224 - Configuration of TU-3 Cross Connect | 334 |
| Tables 225 through 237 - Configuration, Status and Alarms of the TU-3 PTR Generator | 335 |
| Tables 238 through 242 - Configuration of High Order (VC-3 and VC-4) POH Generator | 337 |
| Tables 243 through 250 - Configuration, Status and Alarms of the TU-3 Retimer | 339 |
| Tables 251 through 258 - Configuration, Status and Alarms of the AU-3/4 Retimer | 341 |
| Tables 259 through 261 - Configuration and Status of the General High Order Interrupt Controller | 342 |
| Tables 262 through 280 - Configuration, Status and Alarms of the Rx Combus Interface | 343 |
| Tables 281 through 302 - Configuration, Status and Alarms of the Tx Combus Interface | 347 |
| Tables 303 through 305 - Configuration and Status of the General Combus Interface Interrupt Controller | 350 |
| Tables 306 through 308 - Configuration and Status of the General VTMAPPER Interrupt Controller | 351 |
| Alarms, Performance and Fault Monitoring | 353 |
| Terminology | 353 |
| System Alarm (Raw, Unlatched Alarm) | 353 |
| Alarm Event | 353 |
| Latched Alarm | 353 |
| Secondary Alarm Inhibition | 353 |
| Interrupt Mask | 354 |
| Performance and Fault Monitoring (PM and FM) | 354 |
| Performance Monitoring (PM) | 354 |
| Fault Monitoring (FM) | 354 |
| 1-Second Clock | 354 |
| Performance Counters | 354 |
| Unlatched Alarms | 355 |
| Inhibition of Secondary Unlatched Alarm Generation | 355 |
| Latched Alarms | 355 |
| Latched Alarm Bits for Interrupt Generation (Lalarm_name/L1alarm_name) | 356 |
| Latched Alarm Masking Bits (Malarm_name) | 357 |
| Secondary Latched Alarm Inhibition | 358 |
| Latched Alarm Bits for PM/FM (L2ALARM_name), Performance Monitoring | |
| (PM Bits; Palarm_name) and Fault Monitoring (FM Bits; Falarm_name) | 359 |
| Positive Edge Events | 360 |
| Negative Edge Events | 361 |
| Positive or Negative Edge Events | 362 |
| Overall Alarm Generation and PM/FM Process Diagram | 363 |
| Performance Counters | 364 |
| Scheme A - Counters with Roll-Over/Saturation Option | 364 |
| Scheme B - Performance Counters with 1-second Shadow Register Option | 364 |
| Alarm Feature Combinations | 365 |
| System Alarm, Interrupt, and PM/FM Hierarchy | 366 |
| Alarm Interrupt Tree | 368 |
| Register Tree | 376 |
| Mapper/Demapper Performance Monitoring | 378 |
| Mapper/Demapper Interrupt Tree | 379 |
| Mapper/Demapper PM/FM Tree per Block | 383 |
| Mapper/Demapper Consequent Actions per Block | 390 |
| Package Information | 394 |
| Ordering Information | 395 |
| Related Products | 395 |
| Standards Documentation Sources | 396 |
| List of Data Sheet Changes | 398 |

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LIST OF FIGURES

| Figure | Page |
|---------------|--|
| 1 | Functional Block Diagram of the EtherMap-3 Plus 18 |
| 2 | Low Order Virtual Concatenation Structure for SONET/SDH 19 |
| 3 | High Order Virtual Concatenation Structure for SONET/SDH 20 |
| 4 | Fixed stuff columns in High Order VC-3-Xv/STS-1-Xv SPE 21 |
| 5 | Mapping of Ethernet Frames Over SONET/SDH 23 |
| 6 | Typical Application using the EtherMap-3 Plus and PHAST-3N Devices 30 |
| 7 | EtherMap-3 Plus TXC-04236 Lead Diagram 31 |
| 8 | Drop Bus Timing (Only AD, APAR, and ADD are Output) 54 |
| 9 | Drop Bus Timing (Only AD, APAR, and ADD are Output) 56 |
| 10 | Drop Bus Timing (all ADD Bus Signals are Outputs) 58 |
| 11 | Drop Bus Timing (all ADD Bus Signals are Outputs) 59 |
| 12 | ADD Bus Timing (Timing Signals are Inputs) 60 |
| 13 | ADD Bus Timing (Timing Signals are Inputs) 61 |
| 14 | ADD Bus Timing (Timing Signals are Outputs) 62 |
| 15 | Tx GMII Ethernet Interface 63 |
| 16 | Rx GMII Ethernet Interface 64 |
| 17 | Tx/Rx SMII Ethernet Interface (SYNC as an Output) 65 |
| 18 | Tx/Rx SMII Ethernet Interface (SYNC as an Input) 66 |
| 19 | Ethernet Management Interface 67 |
| 20 | SDRAM Interface - Single Word Read 68 |
| 21 | SDRAM Interface - Single Word Write 69 |
| 22 | SDRAM Interface - Burst Read 70 |
| 23 | SDRAM Interface - Burst Write 71 |
| 24 | Rx VC-3 POH Byte Interface 72 |
| 25 | Tx VC-3 POH Byte Interface 73 |
| 26 | Rx Low Order POH Byte Interface 74 |
| 27 | Tx Low Order POH Byte Interface 75 |
| 28 | Rx VC-3 Alarm Indication Port Interface 76 |
| 29 | Tx VC-3 Alarm Indication Port Interface 77 |
| 30 | Rx Low Order Alarm Indication Port Interface 78 |
| 31 | Tx Low Order Alarm Indication Port Interface 79 |
| 32 | Asynchronous Microprocessor Interface: Intel-type Write Cycle Timing 80 |
| 33 | Asynchronous Microprocessor Interface: Intel-type Read Cycle Timing 82 |
| 34 | Asynchronous Microprocessor Interface: Motorola 68360-type Write Cycle Timing 84 |
| 35 | Asynchronous Microprocessor Interface: Motorola 68360-type Read Cycle Timing 86 |
| 36 | Synchronous Microprocessor Interface: Motorola MPC860-type Read Cycle Timing 88 |
| 37 | Synchronous Microprocessor Interface: Motorola MPC860-type Write Cycle Timing 90 |
| 38 | Boundary Scan Timing 92 |
| 39 | Functional Block Diagram of the Mapper/Demapper 93 |
| 40 | Functional Model of the Mapper/Demapper 94 |
| 41 | Mapper/Demapper Bypass Modes 95 |
| 42 | VT1.5-Xv-SPE Structure 113 |
| 43 | LO SDH Multiplexing Structure 1 Supported by the EtherMap-3 Plus 114 |
| 44 | LO SDH Multiplexing Structure 3 Supported by the EtherMap-3 Plus 114 |
| 45 | LO SDH Multiplexing Structure 2 Supported by the EtherMap-3 Plus 114 |
| 46 | LO SDH Multiplexing Structure 4 Supported by the EtherMap-3 Plus 115 |
| 47 | LO SONET Multiplexing Structure Supported by the EtherMap-3 Plus 115 |
| 48 | High Order STS-1-Xv-SPE/VC-3-Xv Structure 117 |
| 49 | Low Order VC-3-Xv Structure 118 |
| 50 | HO SONET/SDH Multiplexing Structure Supported by the EtherMap-3 Plus 119 |
| 51 | EtherMap-3 Plus to PHY or Switch Interconnection Using GMII Interface 132 |
| 52 | Format of GFP Frame with an Ethernet MAC Frame Payload 141 |



LIST OF FIGURES (cont.)

| Figure | Page |
|--|------|
| 53 Format of LAPS Frame with an Ethernet MAC Frame Payload | 153 |
| 54 Format of LAPF Bridged Frame with an Ethernet MAC Frame Payload | 162 |
| 55 Format of PPP Frame with an Ethernet MAC Frame Payload | 170 |
| 56 MAC Loopback | 193 |
| 57 Telecom Bus Loopbacks | 194 |
| 58 Boundary Scan Schematic | 196 |
| 59 Latched Alarm Bit (L1Alarm_name) Transitions | 357 |
| 60 Positive Edge Event - PM/FM Signal Generation | 360 |
| 61 Negative Edge Event - PM/FM Signal Generation | 361 |
| 62 Positive/Negative Edge Event - PM/FM Signal Generation | 362 |
| 63 Alarm, Interrupt and PM/FM Generation Process | 363 |
| 64 Alarm, Interrupt and PM/FM Generation Process (Inhibition Function) | 363 |
| 65 Alarm Interrupt Hierarchy | 367 |
| 66 Alarm Interrupt Tree Part A | 368 |
| 67 Alarm Interrupt Tree Part A to Part B | 369 |
| 68 Alarm Interrupt Tree Part B to Part C | 370 |
| 69 Alarm Interrupt Tree Part C to Parts D1, D2 and D3 | 371 |
| 70 Alarm Interrupt Tree Parts D1, D2 and D3 to Parts E1 and E2 | 372 |
| 71 Alarm Interrupt Tree Parts E1 and E2 to Parts F1 and F2 | 373 |
| 72 Alarm Interrupt Tree Parts F1 and F2 to Part G | 374 |
| 73 Alarm Interrupt Tree Part G | 375 |
| 74 Register Tree Parts A1, A2 and A3 | 376 |
| 75 Register Tree Parts A1, A2 and A3 (continued) | 377 |
| 76 Mapper/Demapper Interrupt Tree Part A | 379 |
| 77 Mapper/Demapper Interrupt Tree Part A to Parts B1 and B2 | 380 |
| 78 Mapper/Demapper Interrupt Tree Parts B1 and B2 to Part C | 381 |
| 79 Mapper/Demapper Interrupt Tree Part C | 382 |
| 80 Mapper/Demapper RX_VC3_POH_MONITOR PM/FM Trees | 383 |
| 81 Mapper/Demapper RX_VC-4_POH_MONITOR PM/FM Trees | 384 |
| 82 Mapper/Demapper TX_COMBUS PM/FM Trees | 385 |
| 83 Mapper/Demapper RX_TU3_PTR PM/FM Trees | 386 |
| 84 Mapper/Demapper TX_TU3_PTR PM/FM Trees | 386 |
| 85 Mapper/Demapper RX_COMBUS PM/FM Trees | 387 |
| 86 Mapper/Demapper LODMP_POHMONITOR PM/FM Trees | 388 |
| 87 Mapper/Demapper LODMP_Ptr PM/FM Trees | 389 |
| 88 EtherMap-3 Plus TXC-04236 Package Diagram | 394 |

LIST OF TABLES

| Table | Page |
|--|-------------|
| 1 TU-3 Pointer Tracker/Retimer Modes | 96 |
| 2 TU-3 Pointer Generator Modes | 96 |
| 3 SONET/SDH Protection Switching Recovery Time | 112 |
| 4 Configuration of rMAXDELVCG_x in Low Order VC | 129 |
| 5 Configuration of rMAXDELVCG_x in High Order VC | 129 |
| 6 Allowed Range for High/Low Watermark Registers | 137 |
| 7 Scheduling Matrix | 150 |
| 8 Scheduling Matrix Mapped in the EtherMap-3 Plus Register Map | 151 |
| 9 Memory Map Overview | 197 |
| 10 General Device Configuration (RW) | 200 |
| 11 General Device Status (RO) | 200 |
| 12 ID Registers (RO) | 200 |
| 13 MAC Combined Receive and Transmit Counters | 201 |
| 14 MAC Receive Counters | 202 |
| 15 MAC Transmit Counters | 204 |
| 16 MAC Interface Status Registers | 206 |
| 17 MAC Carry and Carry Mask Registers | 207 |
| 18 MAC Configuration Registers | 210 |
| 19 MAC Station Address Registers | 211 |
| 20 MAC IPG / IFG Registers | 212 |
| 21 MAC Half Duplex Registers | 213 |
| 22 MAC Maximum Frame Registers | 213 |
| 23 MAC Test Registers | 214 |
| 24 MAC MII Mgmt Configuration Registers | 215 |
| 25 MAC MII Mgmt Command Registers | 215 |
| 26 MAC MII Mgmt Address Registers | 216 |
| 27 MAC MII Mgmt Control Registers | 216 |
| 28 MAC MII Mgmt Status Registers | 216 |
| 29 MAC MII Mgmt Indicators Registers | 216 |
| 30 MAC Block - General Configuration (RW) | 217 |
| 31 MAC Block - Alarms (RO) | 217 |
| 32 MAC Block - Alarm and Interrupt Masks (RW) | 218 |
| 33 MAC Block - Latched Alarms (RR) | 218 |
| 34 MAC Block - Interrupts (RO) | 218 |
| 35 Encapsulation Block - General Configuration (RW) | 219 |
| 36 Encapsulation Block - LAPS Configuration (RW) | 221 |
| 37 Encapsulation Block - LAPF Configuration (RW) | 222 |
| 38 Encapsulation Block - GFP Configuration (RW) | 223 |
| 39 Encapsulation Block - PPP Configuration (RW) | 226 |
| 40 Encapsulation Block - Control Frame Buffers (RW) | 227 |
| 41 Encapsulation Block - Status (RW) | 228 |
| 42 Encapsulation Block - Status Registers (RO) | 228 |
| 43 Encapsulation Block - Performance Counters | 228 |
| 44 Encapsulation Block - Alarms (RO) | 231 |
| 45 Encapsulation Block - Alarm and Interrupt Masks (RW) | 232 |
| 46 Encapsulation Block - Interrupts (RO) | 233 |
| 47 Encapsulation Block - Latched Alarms (RR) | 235 |
| 48 Decapsulation Block - General Configuration (RW) | 236 |
| 49 Decapsulation Block - LAPS Configuration (RW) | 238 |
| 50 Decapsulation Block - LAPF Configuration (RW) | 240 |



LIST OF TABLES (cont.)

| Table | Page |
|---|------|
| 51 Decapsulation Block - Control Buffer Status (RW) | 242 |
| 52 Decapsulation Block - Link Status (RO) | 242 |
| 53 Decapsulation Block - GFP Configuration (RW) | 243 |
| 54 Decapsulation Block - PPP Configuration (RW) | 245 |
| 55 Decapsulation Block - LMI Buffers (RO) | 247 |
| 56 Decapsulation Block - Alarms (RO) | 247 |
| 57 Decapsulation Block - Alarm and Interrupt Masks (RW) | 251 |
| 58 Decapsulation Block - Latched Alarms (RR) | 255 |
| 59 Decapsulation Block - Interrupts (RO) | 258 |
| 60 Decapsulation Block - Performance Counters | 259 |
| 61 Decapsulation Block - Status (RR) | 266 |
| 62 SDRAM Control - General Configuration (RW) | 268 |
| 63 SDRAM - Access Control Registers (RW) | 269 |
| 64 SDRAM - Access Results Registers (RO) | 269 |
| 65 Tx Virtual Concatenation Block - General Configuration (RW) | 270 |
| 66 Tx Virtual Concatenation Block - LCAS Alarms (RO) | 272 |
| 67 VT/VC Address Offsets | 273 |
| 68 Tx Virtual Concatenation Block - LCAS Alarm and Interrupt Masks (RW) | 275 |
| 69 Tx Virtual Concatenation Block - LCAS Latched Alarms (RR) | 277 |
| 70 Tx Virtual Concatenation Block - LCAS Interrupts (RO) | 278 |
| 71 Tx Virtual Concatenation Block - Low Order Tributary Configuration (RW) | 279 |
| 72 Tx Virtual Concatenation Block - High Order Tributary Configuration (RW) | 279 |
| 73 Tx Virtual Concatenation Block - LCAS Configuration (RW) | 279 |
| 74 VT/VC Address Offsets (cTLOK4VCEN_x and cTLOCRCERR_x Only) | 280 |
| 75 Tx Virtual Concatenation Block - Status (RO) | 282 |
| 76 Rx Virtual Concatenation Block - General Configuration Registers (RW) | 283 |
| 77 Rx Virtual Concatenation Block - Alarms (RO) | 285 |
| 78 Rx Virtual Concatenation Block - Alarm and Interrupt Masks (RW) | 286 |
| 79 Rx Virtual Concatenation Block - Latched Alarms (RR) | 290 |
| 80 Rx Virtual Concatenation Block - Interrupts (RO) | 291 |
| 81 Rx Virtual Concatenation Block - Low Order Tributary Configuration (RW) | 292 |
| 82 Rx Virtual Concatenation Block - High Order Tributary Configuration (RW) | 293 |
| 83 Rx Virtual Concatenation Block - Status (RO) | 293 |
| 84 Rx Virtual Concatenation Block - Frame Counter Status (RO) | 294 |
| 85 Rx Virtual Concatenation Block - Differential Delay Status (RO) | 294 |
| 86 Ethernet Frame Format Block - General Configuration (RW) | 295 |
| 87 Ethernet Frame Format Block - Alarms (RO) | 295 |
| 88 Ethernet Frame Format Block - Alarm and Interrupt Masks (RW) | 295 |
| 89 Ethernet Frame Format Block - Latched Alarms (RR) | 295 |
| 90 Ethernet Frame Format Block - Interrupts (RO) | 295 |
| 91 SONET to Ethernet - General Configuration and Watermarks (RW) | 296 |
| 92 SONET to Ethernet - SDRAM Alarms (RO) | 297 |
| 93 SONET to Ethernet - SDRAM Alarm and Interrupt Masks (RW) | 297 |
| 94 SONET to Ethernet - SDRAM Latched Alarms RR) | 297 |
| 95 SONET to Ethernet - SDRAM Interrupts (RO) | 298 |
| 96 SONET to Ethernet - SDRAM Performance Counters (RR) | 298 |
| 97 SONET to Ethernet - SDRAM FIFO Status (RO) | 298 |
| 98 Ethernet to SONET - Flow Control Configuration (RW) | 298 |
| 99 SDRAM Controller Alarm (Tx and Rx) (RO) | 299 |
| 100 SDRAM Controller (Tx and Rx Direction) (RW) | 300 |
| 101 SDRAM Controller (Tx and Rx Directions) (RR) | 300 |

LIST OF TABLES (cont.)

| Table | Page |
|---|-------------|
| 102 Ethernet to SONET, SDRAM Output - Interrupts (RO) | 301 |
| 103 Ethernet to SONET, SDRAM Output - Performance Counters | 301 |
| 104 Mapper Block - Reset (RW) | 302 |
| 105 Mapper Block - Interrupt Configuration (RO) | 302 |
| 106 Mapper Block - Interrupt Mask (RW) | 302 |
| 107 Mapper and Demapper Block - Status (RO) | 302 |
| 108 Mapper Block - Timing Configuration (RW) | 302 |
| 109 Mapper Block - TUG-3/VC-3 Configuration (RW) | 303 |
| 110 Mapper Block - TUG-2 Configuration (RW) | 303 |
| 111 Mapper Block - Pointer Configuration (RW) | 303 |
| 112 Mapper Block - General Configuration, Low Order (RW) | 303 |
| 113 Mapper Block - TUG-2 Configuration (RW) | 303 |
| 114 Mapper Block - POH Configuration (RW) | 303 |
| 115 Mapper Block - Cross Connect Configuration (RW) | 304 |
| 116 Mapper Block - V4 Configuration (RW) | 304 |
| 117 Mapper Block - POH Byte Values (RW) | 304 |
| 118 Mapper Block - Bypass Control (RW) | 305 |
| 119 Demapper Block - General Configuration (RW) | 306 |
| 120 Demapper Block - Bypass Control (RW) | 306 |
| 121 Demapper Block - TUG-2 Configuration (RW) | 306 |
| 122 Demapper Block - Performance Counters Shadow Registers (RO) | 306 |
| 123 Demapper Block - Alarm Control (RW) | 307 |
| 124 Demapper Block - Interrupts (RO) | 307 |
| 125 Demapper Block - Alarms (RO) | 307 |
| 126 Demapper Block - Latched Alarms (R/COW-1) | 307 |
| 127 Demapper Block - Alarm Masks (RW) | 307 |
| 128 LODMP_Ptr_DefectCorrelations_LP (R/COW-0) | 308 |
| 129 LODMP_Ptr_DefectCorrelations_PM (RO) | 308 |
| 130 LODMP_Ptr_DefectCorrelations_FM (RO) | 308 |
| 131 Demapper Block - POH Byte Monitors (RO) | 308 |
| 132 LO POH Monitor - Bypass Control (RW) | 308 |
| 133 LO POH Monitor - J2 Trace Message Handling | 309 |
| 134 LO POH Monitor - POH Byte Monitors (RO) | 309 |
| 135 LO POH Monitor - Accepted Values (RO) | 309 |
| 136 LO POH Monitor - Expected Values (RW) | 309 |
| 137 LO POH Monitor - General Configuration (RW) | 310 |
| 138 LO POH Monitor - Channel Configuration (RW) | 311 |
| 139 LO POH Monitor - Channel Status (RO) | 311 |
| 140 LO POH Monitor - Channel Report (RO) | 311 |
| 141 LO POH Monitor - Channel Defects (RO) | 311 |
| 142 LO POH Monitor - Defect Correlations (RO) | 312 |
| 143 LO POH Monitor - Latched Defects (R/COW-1) | 312 |
| 144 LO POH Monitor - Defect Correlations Latched For PMFM (R/COW-0) | 313 |
| 145 LO POH Monitor - PM Defect Correlations Monitor (RO) | 313 |
| 146 LO POH Monitor - FM Defect Correlations Monitor (RO) | 313 |
| 147 LO POH Monitor - Defect Correlations Mask (R/W) | 314 |
| 148 LO POH Monitor - Defect Correlations Configuration (RW) | 314 |
| 149 LO POH Monitor - Defect Correlations Summary (RO) | 315 |
| 150 LO POH Monitor - Defect Correlations Summary Mask (RW) | 315 |
| 151 LO POH Monitor - Defect Correlations Group Summary (RO) | 315 |
| 152 LO POH Monitor - Performance Monitor One Second Latch (RO) | 315 |



LIST OF TABLES (cont.)

| Table | Page |
|---|------|
| 153 LO POH Monitor - Performance Counters (RW) | 315 |
| 154 LO POH Monitor - Performance Counter Shadow Registers (RO) | 315 |
| 155 Tx LO Ring Port - General Configuration (RW) | 316 |
| 156 Tx LO Ring Port - Event Latch (COW-1) | 316 |
| 157 Tx LO Ring Port - Performance Counters (RW) | 316 |
| 158 Tx LO Ring Port - Performance Counter Shadow Registers (RO) | 316 |
| 159 Tx LO Ring Port - Defects | 317 |
| 160 Tx LO Ring Port - Interrupt Mask (RW) | 317 |
| 161 Tx LO Ring Port - Event Interrupt (RO) | 317 |
| 162 Tx LO Ring Port - Defect Interrupt (RO) | 317 |
| 163 Rx LO Ring Port - Configuration (RW) | 317 |
| 164 LO Interrupt Controller - Interrupts (RO) | 318 |
| 165 LO Interrupt Controller - Interrupt Masks (RW) | 318 |
| 166 LO Interrupt Controller - Summary (RO) | 318 |
| 167 Rx HO Ring Port - Configuration (RW) | 318 |
| 168 Tx HO Ring Port - Configuration (RW) | 318 |
| 169 Tx HO Ring Port - Counter Configuration (RW) | 319 |
| 170 Tx HO Ring Port - Event Latch (COW-1) | 319 |
| 171 Tx HO Ring Port - Performance Counters (RW) | 319 |
| 172 Tx HO Ring Port - Performance Counter Shadow Registers (RO) | 319 |
| 173 Tx HO Ring Port - Defects | 319 |
| 174 Tx HO Ring Port - Interrupt Mask (RW) | 320 |
| 175 Tx HO Ring Port - General Interrupt (RO) | 320 |
| 176 Tx HO Ring Port - Defect Interrupt (RO) | 320 |
| 177 HO POH Monitor - Received-64 Byte Trace Message (RO) | 320 |
| 178 HO POH Monitor - Received 16-Byte Trace Message (RO) | 321 |
| 179 HO POH Monitor - Accepted Bytes (RO) | 321 |
| 180 HO POH Monitor - Expected J1 Bytes (RW) | 321 |
| 181 HO POH Monitor - Expected C2 Bytes (RW) | 321 |
| 182 HO POH Monitor - Received POH Bytes (RO) | 321 |
| 183 HO POH Monitor - Accepted POH Bytes (RO) | 322 |
| 184 HO POH Monitor - Configuration (RW) | 322 |
| 185 HO POH Monitor - Loopback Control (RW) | 322 |
| 186 HO POH Monitor - Channel Configuration (RW) | 322 |
| 187 HO POH Monitor - Channel Status (RO) | 324 |
| 188 HO POH Monitor - Channel Defects (RO) | 324 |
| 189 HO POH Monitor - J1 Message Status (RO) | 324 |
| 190 HO POH Monitor - Defects (RO) | 325 |
| 191 HO POH Monitor - Latched Defects (R/COW-1) | 325 |
| 192 HO POH Monitor - Defect Masks (RW) | 326 |
| 193 HO POH Monitor - Defects Latched For PMFM (R/COW-0) | 326 |
| 194 HO POH Monitor - Defects PM (RO) | 327 |
| 195 HO POH Monitor - Defects FM (RO) | 327 |
| 196 HO POH Monitor - Defect Configuration (RW) | 328 |
| 197 HO POH Monitor - Defect Summary (RO) | 328 |
| 198 HO POH Monitor - Defect Summary Mask (RW) | 329 |
| 199 HO POH Monitor - Defect Group Summary (RO) | 329 |
| 200 HO POH Monitor - APS Event (RO) | 329 |
| 201 HO POH Monitor - Latched APS Event (R/COW-1) | 329 |
| 202 HO POH Monitor - APS Event Mask (RW) | 329 |
| 203 HO POH Monitor - APS Interrupt (RO) | 330 |

LIST OF TABLES (cont.)

| Table | Page |
|--|-------------|
| 204 HO POH Monitor - Performance Counters (RW) | 330 |
| 205 HO POH Monitor - Performance Counters One Second Latch (RO) | 330 |
| 206 HO POH Monitor - Performance Counter Shadow Registers (RO) | 330 |
| 207 HO POH Monitor - Performance Counter Configuration (RW) | 331 |
| 208 HO POH Monitor - Counter Reset (WO) | 331 |
| 209 HO POH Monitor - PMFM Configuration (RW) | 331 |
| 210 TU-3 PTR Tracker - General Configuration (RW) | 332 |
| 211 TU-3 PTR Tracker - Per Channel Configuration (RW) | 332 |
| 212 TU-3 PTR Tracker - Defects (RO) | 332 |
| 213 TU-3 PTR Tracker - Defects Latched For Interrupt (R/COW-1) | 333 |
| 214 TU-3 PTR Tracker - Defects Latched For PMFM (R/COW-0) | 333 |
| 215 TU-3 PTR Tracker - Defects PM (RO) | 333 |
| 216 TU-3 PTR Tracker - Defects FM (RO) | 333 |
| 217 TU-3 PTR Tracker - Defect Masks (RW) | 333 |
| 218 TU-3 PTR Tracker - Defect Summary (RO) | 333 |
| 219 TU-3 PTR Tracker - Defect Summary Mask (RW) | 333 |
| 220 TU-3 PTR Tracker - Defect Group Summary (RO) | 333 |
| 221 TU-3 PTR Tracker - Performance Counters (RW) | 334 |
| 222 TU-3 PTR Tracker - Performance Counter Shadow Registers (RO) | 334 |
| 223 Transmit VC-3/STS-1/TUG-3 Time Slot Interchange (RW) | 334 |
| 224 Receive VC-3/STS-1/TUG-3 Time Slot Interchange (RW) | 334 |
| 225 TU-3 PTR Generator - General Configuration (RW) | 335 |
| 226 TU-3 PTR Generator - Per Channel Configuration (RW) | 335 |
| 227 TU-3 PTR Generator - Defects (RO) | 335 |
| 228 TU-3 PTR Generator - Defects Latched For Interrupt (R/COW-1) | 336 |
| 229 TU-3 PTR Generator - Defects Latched For PMFM (R/COW-0) | 336 |
| 230 TU-3 PTR Generator - Defects PM (RO) | 336 |
| 231 TU-3 PTR Generator - Defects FM (RO) | 336 |
| 232 TU-3 PTR Generator - Defect Mask (RW) | 336 |
| 233 TU-3 PTR Generator - Defect Summary (RO) | 336 |
| 234 TU-3 PTR Generator - Defect Summary Mask (RW) | 336 |
| 235 TU-3 PTR Generator - Defect Group Summary (RO) | 336 |
| 236 TU-3 PTR Generator - Performance Counters (RW) | 337 |
| 237 TU-3 PTR Generator - Performance Counter Shadow Registers (RO) | 337 |
| 238 HO POH Generator - Channel Control (RW) | 337 |
| 239 HO POH Generator - Configuration (RW) | 338 |
| 240 HO POH Generator - J1 Message Bytes (RW) | 338 |
| 241 HO POH Generator - POH Insertion Values (RW) | 338 |
| 242 HO POH Generator - POH Port Monitors (RO) | 339 |
| 243 TU-3 Retimer - General Configuration (RW) | 339 |
| 244 TU-3 Retimer - Per Channel Configuration (RW) | 339 |
| 245 TU-3 Retimer - Defects (RO) | 339 |
| 246 TU-3 Retimer - Defects Latched For Interrupt (R/COW-1) | 339 |
| 247 TU-3 Retimer - Defect Masks (RW) | 340 |
| 248 TU-3 Retimer - Defect Group Summary (RO) | 340 |
| 249 TU-3 Retimer - Sequencer Configuration (RW) | 340 |
| 250 TU-3 Retimer - Sequencer Data (RW) | 340 |
| 251 AU-3/4 Retimer - General Configuration (RW) | 341 |
| 252 AU-3/4 Retimer - Per Channel Configuration (RW) | 341 |
| 253 AU-3/4 Retimer - Defects (RO) | 341 |
| 254 AU-3/4 Retimer - Defects Latched For Interrupt (R/COW-1) | 341 |



LIST OF TABLES (cont.)

| Table | Page |
|--|------|
| 255 AU-3/4 Retimer - Defect Masks (RW) | 341 |
| 256 AU-3/4 Retimer - Defect Group Summary (RO) | 341 |
| 257 AU-3/4 Retimer - Ptr Leak Reset Value (RW) | 342 |
| 258 AU-3/4 Retimer - Performance Counters (RO) | 342 |
| 259 HO Interrupt Controller - Interrupts (RO) | 342 |
| 260 HO Interrupt Controller - Interrupt Masks (RW) | 343 |
| 261 HO Interrupt Controller - Interrupt Group Summary (RO) | 343 |
| 262 Rx Combust Interface - General Configuration (RW) | 343 |
| 263 Rx Combust Interface - Per Channel Configuration (RW) | 344 |
| 264 Rx Combust Interface - Per Channel Status (RO) | 344 |
| 265 Rx Combust Interface - Defects (RO) | 344 |
| 266 Rx Combust Interface - Defects Latched For Interrupt (R/COW-1) | 344 |
| 267 Rx Combust Interface - Defects Latched For PMFM (R/COW-0) | 344 |
| 268 Rx Combust Interface - Defects PM (RO) | 344 |
| 269 Rx Combust Interface - Defects FM (RO) | 344 |
| 270 Rx Combust Interface - Defect Masks (RW) | 345 |
| 271 Rx Combust Interface - Defect Group Summary (RO) | 345 |
| 272 Rx Combust Interface - Per Channel Defects (RO) | 345 |
| 273 Rx Combust Interface - Per Channel Defects Latched For Interrupt (R/COW-1) | 345 |
| 274 Rx Combust Interface - Per Channel Defects Latched For PMFM (R/COW-0) | 345 |
| 275 Rx Combust Interface - Per Channel Defects PM (RO) | 345 |
| 276 Rx Combust Interface - Per Channel Defects FM (RO) | 345 |
| 277 Rx Combust Interface - Per Channel Defect Masks (RW) | 346 |
| 278 Rx Combust Interface - Per Channel Defect Summary (RO) | 346 |
| 279 Rx Combust Interface - Per Channel Defect Summary Masks (RW) | 346 |
| 280 Rx Combust Interface - Per Channel Defect Group Summary (RO) | 346 |
| 281 Tx Combust Interface - General Configuration (RW) | 347 |
| 282 Tx Combust Interface - AUG1 Configuration (RW) | 347 |
| 283 Tx Combust Interface - AU-3 Configuration (RW) | 347 |
| 284 Tx Combust Interface - TUG-2 Configuration (RW) | 348 |
| 285 Tx Combust Interface - TU-11/TU-12 Configuration (RW) | 348 |
| 286 Tx Combust Interface - Defects (RO) | 348 |
| 287 Tx Combust Interface - Defects Latched For Interrupt (R/COW-1) | 348 |
| 288 Tx Combust Interface - Defect Masks (RW) | 348 |
| 289 Tx Combust Interface - Defects Latched For PMFM (R/COW-0) | 348 |
| 290 Tx Combust Interface - Defects PM (RO) | 348 |
| 291 Tx Combust Interface - Defects FM (RO) | 348 |
| 292 Tx Combust Interface - Defect Group Summary (RO) | 349 |
| 293 Tx Combust Interface - Per Channel Defects (RO) | 349 |
| 294 Tx Combust Interface - Per Channel Defects Latched For Interrupt (R/COW-1) | 349 |
| 295 Tx Combust Interface - Per Channel Defect Masks (RW) | 349 |
| 296 Tx Combust Interface - Per Channel Defects Latched For PMFM (R/COW-0) | 349 |
| 297 Tx Combust Interface - Per Channel Defects PM (RO) | 349 |
| 298 Tx Combust Interface - Per Channel Defects FM (RO) | 349 |
| 299 Tx Combust Interface - Per Channel Defect Summary (RO) | 350 |
| 300 Tx Combust Interface - Per Channel Defect Summary Masks (RW) | 350 |
| 301 Tx Combust Interface - Per Channel Defect Group Summary (RO) | 350 |
| 302 Tx Combust Interface - Defect Configuration (RW) | 350 |
| 303 Combust Interrupt Controller - Interrupts (RO) | 350 |
| 304 Combust Interrupt Controller - Interrupt Masks (RW) | 351 |
| 305 Combust Interrupt Controller - Interrupt Group Summary (RO) | 351 |

LIST OF TABLES (cont.)

| Table | | Page |
|--------------|--|-------------|
| 306 | Mapper Interrupt Controller - Interrupts (RO) | 351 |
| 307 | Mapper Interrupt Controller - Interrupt Masks (RW) | 351 |
| 308 | Mapper Interrupt Controller - Interrupt Group Summary (RO) | 351 |
| 309 | Reserved Registers | 351 |
| 310 | Latched Alarm Bit (L1Alarm_name) Transition Selection | 356 |
| 311 | Latched Alarm Bit (L2Alarm_name) Transition Selection | 359 |

FEATURES

The EtherMap-3 Plus supports the following features:

MAPPINGS

- EtherMap-3 Plus maps Ethernet traffic of up to (8) 10/100 Mb/s SMII ports or (1)1000 Mb/s GMII port onto SONET/SDH
- Performs Virtual Concatenation for SONET/SDH, compensating for up to 48 ms of differential delay
- Implements Link Capacity Adjustment Scheme (LCAS) to allow the size of the virtual concatenation groups to be changed dynamically with hitless switching.
- Supports both High Order and Low Order Virtual Concatenation
 - STS-3c SPE
 - STS-3 / STS-1 SPE, STS-1-Xv
 - STS-3 / STS-1 / VT1.5 SPE, VT1.5-Xv
 - STS-3 / STS-1 / VT2 SPE, VT2-Xv
 - STM-1 / AUG-1 / AU-4 / VC-4
 - STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3, VC-3-Xv¹
 - STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12 / VC-12, VC-12-Xv
 - STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv
 - STM-1 / AUG-1 / AU-3 / VC-3, VC-3-Xv
 - STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12, VC-12-Xv
 - STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv
- All supported virtual concatenation mappings can be mixed according to the [G.707] multiplexing structure up to a total payload rate equivalent to one STS-3/STM-1 signal.
- Supports a mix of 100 Mbit/s and 10 Mbit/s traffic (up to 8 ports).
- For 10/100 Mb/s operation (up to 8 ports), can virtually concatenate up to 63 VC-12/VT2 SPEs or 64 VC-11/VT1.5-SPEs.
- For 100 Mb/s operation, a single VC-4 or a single STS-3c SPE can be used, or
 - Can virtually concatenate up to 64 VC-11s or up to 63 VC-12s or up to 3 VC-3s
 - Can virtually concatenate up to 64 VT1.5-SPEs or up to 63 VT2-SPEs or up to 3 STS-1-SPEs
- For 1000 Mb/s
 - Supports either a single VC-4, or can virtually concatenate up to 3 VC-3s
 - Supports either a single STS-3c-SPE, or can virtually concatenate up to 3 STS-1-SPEs

ENCAPSULATION PROTOCOLS

- EtherMap-3 Plus supports one of four encapsulation protocols per Ethernet MAC:
 - LAPS (Link Access Procedure SDH)
 - LAPF (Link Access Procedure for Framed Mode service)
 - GFP (Generic Framing Procedure)
 - PPP (with BCP support)

1. Note: in ITU-T SDH a VC-3 can either be high order (AU-3/STS-1) or low order (TU-3). In the remainder of the EtherMap-3 Plus data sheet high order and low order refers to the type of path overhead bytes rather than the order of the path in the multiplexing hierarchy. Though both low and high order VC-3 mapping is supported, VC-3 operation will be covered in the high order path sections.

ETHERNET PORTS

The EtherMap-3 Plus provides the following Ethernet Port features:

- Eight independent SMII (Serial Media Independent Interfaces) for 10/100 Mbit/s Ethernet
 - Global 125 MHz reference clock
 - Global Synchronization signal
 - Lead selects PHY or Switch connection to external client
- Single GMII (Gigabit MII) for 1000 Mbit/s Ethernet
 - Lead shared with the SMII ports
- Selection of GMII or SMII is selected through a lead
- Ethernet Management Interface
- PHY or Switch Selection

10/100/1000 MBIT/S ETHERNET MEDIA ACCESS CONTROLLER (MAC) BLOCK

- Compliant to IEEE 802.3, 802.3u, 802.3x, 802.3z, and 802.3ac
- Full Duplex Operation in 10/100/1000 Mbit/s
- Half Duplex Operation in 10/100 Mbit/s
- MAC control sub layer provides support for control frames including PAUSE frames
- Provides support for statistics gathering based on RMON MIB Group 1, RMON MIB Group 2, RMON MIB Group 3, RMON MIB Group 9, RMON MIB 2, and the dot 3 Ethernet MIB

SDRAM INTERFACE

- Glueless interface to external 64 Mbits, 128 Mbits, or 256 Mbits SDRAM devices
- 32 Data, 13 Address, 1 Chip Select, 1 Clock, 1 Clock Enable, 1 Row Address Strobe, 1 Column Address Strobe, 1 Write Enable Strobe, 1 Data Bus Mask, and 2 Bank Address leads
- Buffers TX/RX data transfers
- Clock frequency of 100 MHz
- Programmable Refresh Period
- CAS latency of 3 supported
- Refresh operation is transparent to the user
- Trp timing of the selected SDRAM must be below 30 ns.

TELECOM BUS TIMING

A single Telecom Bus interface is provided for interfacing to the SONET/SDH line through one of TranSwitch's TOH/POH Terminator devices such as the PHAST[®]-3N or the PHAST-12E/POP-12 chip set. Timing for adding tributaries to the Add bus is derived from either the Drop bus or the Add bus. The EtherMap-3 Plus provides the following timing modes for the Add bus:

- Drop bus timing
 - Add bus timing is derived from the Drop bus timing input signals
 - Drop bus: C1J1, SPE, Optional V1, Data, Clock and Parity signal leads are inputs
 - Add bus: C1J1, SPE, Optional V1, Data, Clock, Parity and Add Indication signal leads are outputs. The C1J1, SPE, Optional V1, and clock can be optionally disabled.
- Add bus timing (two modes)
 - Add bus timing is derived from the Add bus timing input signals



- Drop bus: C1J1, SPE, Optional V1, Data, Clock, and Parity signal leads are inputs
- Add bus: C1J1, Clock, Optional V1 and SPE signal leads are inputs; Data, Parity and Add Indication signal leads are outputs
- Add bus timing is derived from an external reference clock
 - Drop bus: C1J1, SPE, Optional V1, Data, Clock and Parity signal leads are inputs
 - Add bus: C1J1, SPE, Optional V1, Data, Clock, Parity and Add Indication signal leads are outputs

ALARM INDICATION PORT INTERFACE

- High Order Alarm Indication Port to support ring applications
- Low Order Alarm Indication Port to support ring applications

POH PORT INTERFACE

- High Order POH Port for access to POH bytes
- Low Order POH Port for access to POH bytes

MICROPROCESSOR INTERFACE

- 16-bit Address and Data bus
- Motorola or Intel style split bus supported
- Interrupt request lead
- Interrupt mask bits for controlling generation of hardware interrupt requests

JTAG INTERFACE

- IEEE 1149.1 compliant TAP is provided for board level testing.

BLOCK DIAGRAM

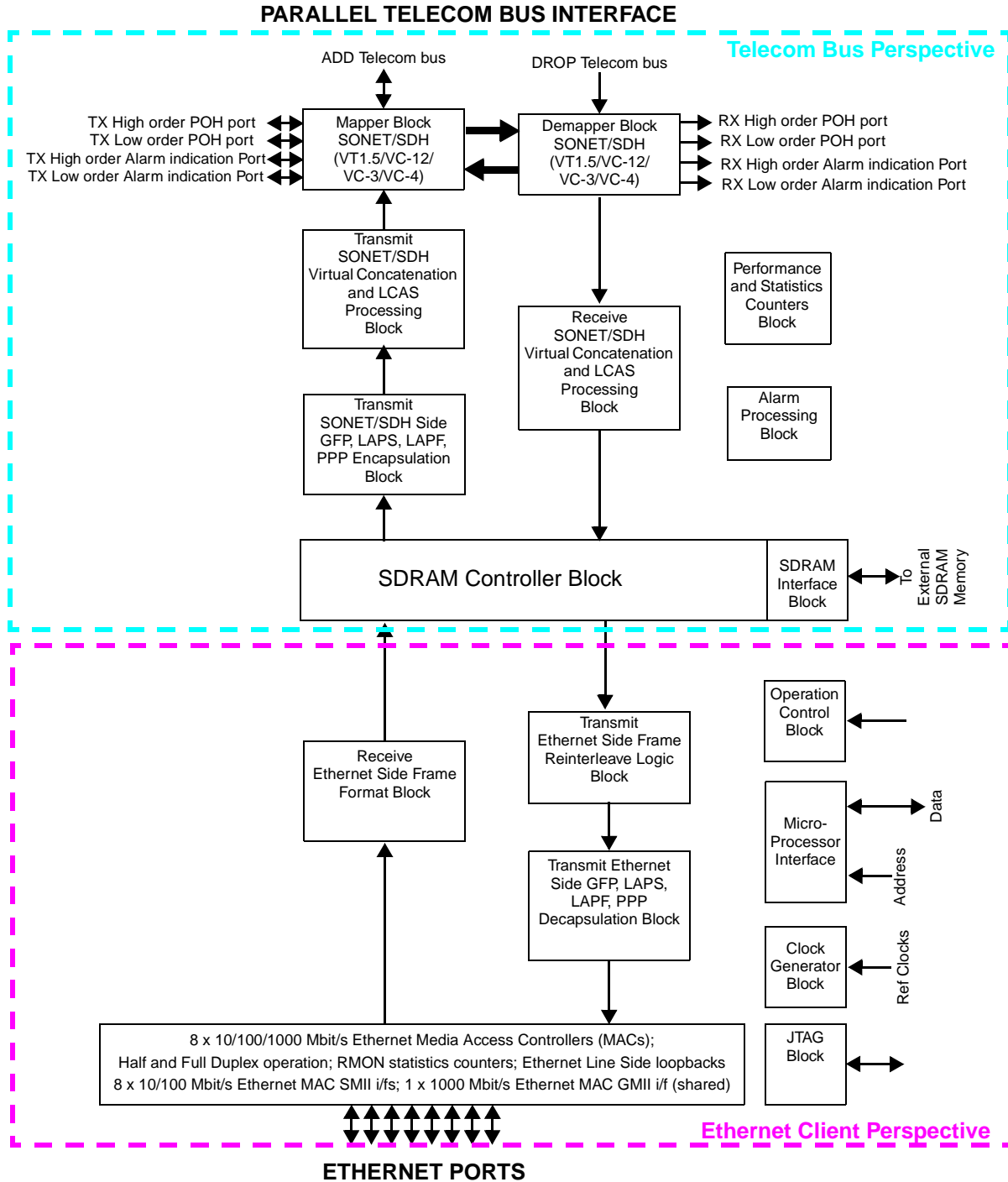


Figure 1. Functional Block Diagram of the EtherMap-3 Plus

BLOCK DIAGRAM DESCRIPTION

The following sections describe the functional block diagram of the EtherMap-3 Plus shown in Figure 1 above:

DATA PROCESSING/FLOW

In general, the EtherMap-3 Plus provides functionality for mapping and demapping of Ethernet frames to and from SONET/SDH virtual concatenated tributary structures in both LCAS/non-LCAS mode. The figures below represent the virtual tributary structures that are supported by the EtherMap-3 Plus device.

Figure 2 shows the low order virtual concatenation structure for VT1.5-Xv SPE, VT2-Xv SPE, VC-11-Xv and VC-12-Xv. A VC-11-Xv/VT1.5-Xv SPE provides a payload area of X VC-11/VT1.5 SPE payload capacity as shown. The Ethernet payload is mapped into X individual VC-11s/VT1.5 SPEs which form the VC-11-Xv/VT1.5-Xv SPE. Each VC-11/VT1.5 SPE has its own POH and can be sent throughout the SONET/SDH network individually and then reassembled at the destination. The same principle applies for a VC-12-Xv/VT2-Xv SPE.

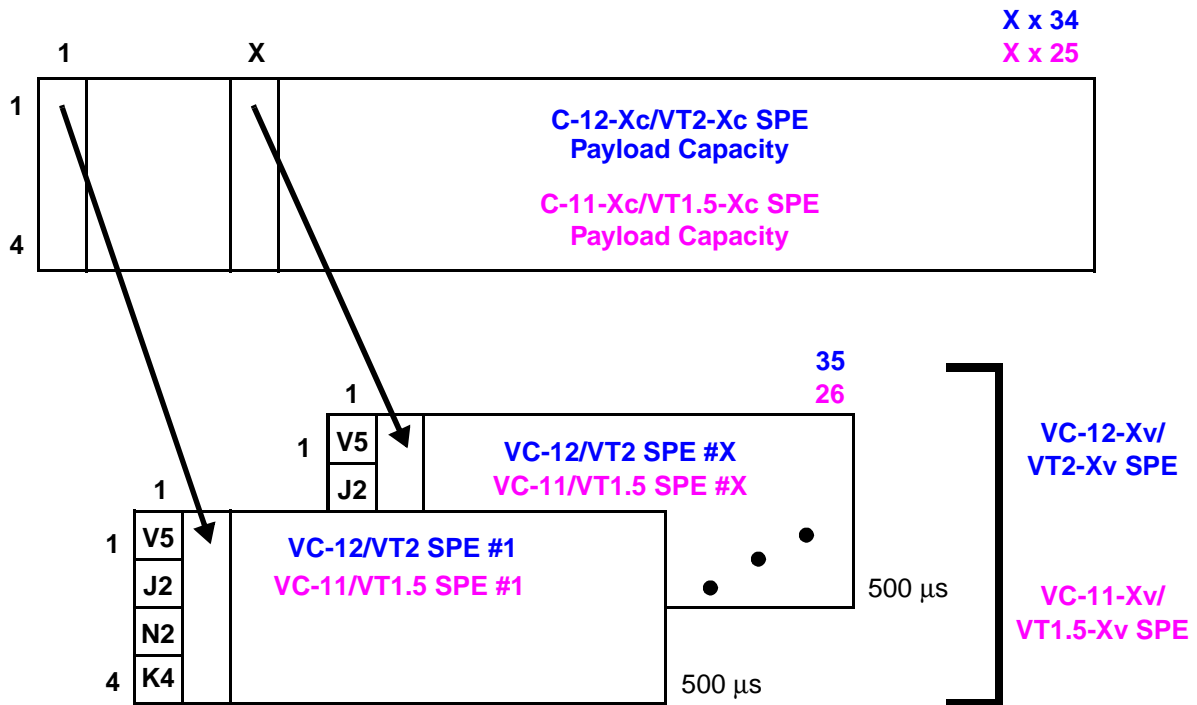


Figure 2. Low Order Virtual Concatenation Structure for SONET/SDH

Figure 3 shows the high order virtual concatenation structure for STS-1-Xv and VC-3-Xv. This structure provides a contiguous payload area of X VC-3/STS-1 SPE with a payload capacity of X*48384 kbit/s as shown. The payload capacity (i.e., the encapsulated Ethernet frames) is mapped into X individual VC-3s/STS-1 SPEs which form the VC-3-Xv/STS-1-Xv SPE. For high order VC-3s and STS-1 SPEs fixed stuff column are added (Figure 4). Each VC-3/STS-1 SPE has its own POH. Just like for the low order case above, the VC-3s/STS-1-SPEs can travel through the SONET/SDH network independently and are reassembled at their destination to recover the Ethernet data.

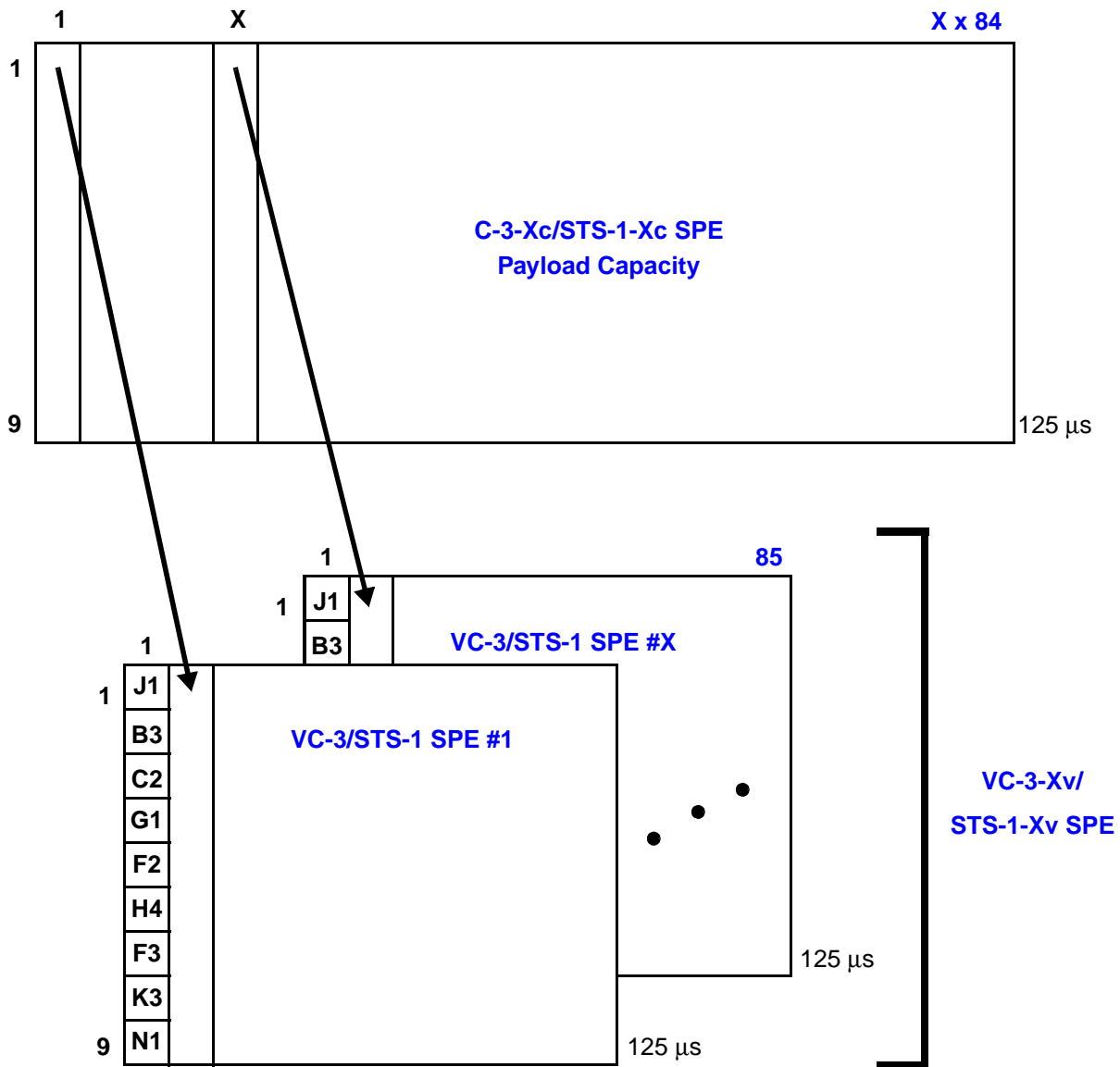


Figure 3. High Order Virtual Concatenation Structure for SONET/SDH

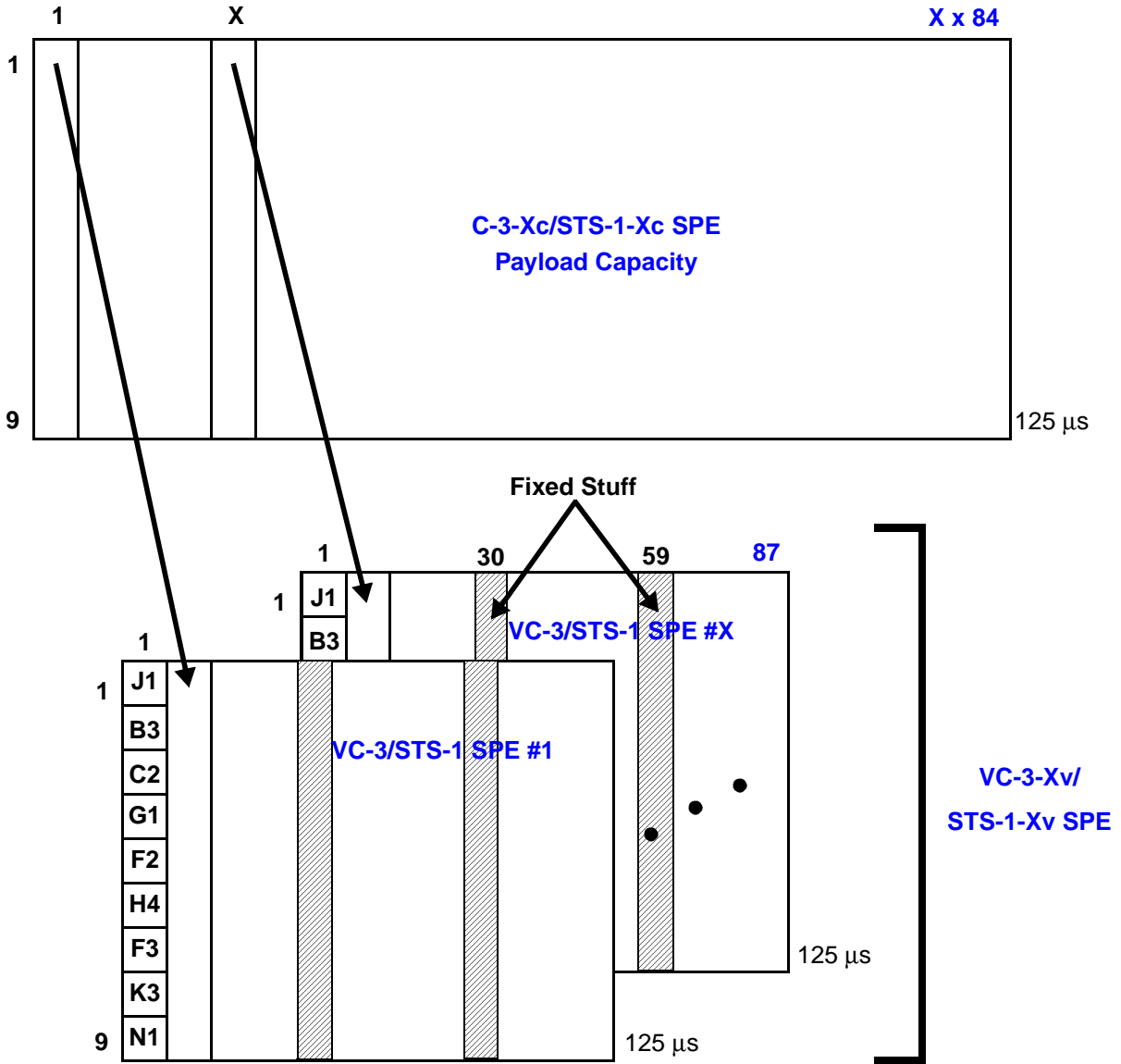


Figure 4. Fixed stuff columns in High Order VC-3-Xv/STS-1-Xv SPE

On the SONET/SDH side, the EtherMap-3 Plus supports an STM-1/STS-3/STS-3c like structure using a single TranSwitch defined Telecom bus operating at 19.44 MHz. On the Ethernet Line side, the EtherMap-3 Plus supports up to EIGHT 10/100 Mbit/s Ethernet ports or ONE 1000 Mbit/s (Gigabit) Ethernet port. The eight 10/100 Mbit/s Ethernet ports each support the industry standard SMII interface. The single Gigabit Ethernet port supports the industry standard GMII interface and is lead shared with the SMII interfaces.

In the transmit direction (Ethernet-to-SONET/SDH), the EtherMap-3 Plus terminates the 10/100/1000 Mbit/s Ethernet traffic. The Ethernet frames from configured port(s) are extracted and buffered in an external SDRAM memory. The external SDRAM is primarily used for implementing flow control when the Ethernet line side bandwidth is greater than the allocated bandwidth on the SONET/SDH side (i.e., an over-subscription situation). Based on system configuration, Ethernet frames from each of the Ethernet ports are encapsulated using one of the supported link layer protocols: GFP, LAPS, LAPF or PPP independently. The encapsulated

Ethernet frames are then byte interleaved over preselected SONET/SDH containers and transported using virtual concatenation. The EtherMap-3 Plus provides complete High and Low order path overhead generation for the SONET/SDH containers. The bandwidth of SONET/SDH containers using virtual concatenation, are allowed to increase or decrease in a hitless fashion through the use of an integrated link capacity adjustment scheme (LCAS). The SONET/SDH containers carrying Ethernet frames are then transmitted to an upstream SONET/SDH Overhead Terminator device such as TranSwitch's PHAST-3N, using a parallel telecom bus.

In the receive direction (SONET/SDH-to-Ethernet), the EtherMap-3 Plus terminates a parallel telecom bus with SONET/SDH containers carrying encapsulated (GFP, LAPS, LAPF, PPP) Ethernet frames. The EtherMap-3 Plus provides complete High and Low order path overhead processing for the SONET/SDH tributaries. The SONET/SDH containers are then extracted and buffered using the external SDRAM memory. This memory is primarily used for providing alignment and differential delay compensation for the select SONET/SDH containers which form part of the virtual concatenation group. Once alignment and delay compensation has been achieved, the Ethernet frames are byte reinterleaved from the SONET/SDH containers to form their original frame structure on a per port basis. The Ethernet frames are then extracted from one of the encapsulations (GFP, LAPS, LAPF or PPP) used at the transmit side and passed onto the Ethernet port for transmission to the external client(s).

10/100/1000 MBIT/S ETHERNET MEDIA ACCESS CONTROLLER (MAC) BLOCK

The interface for the 10/100 Mbit/s Ethernet ports and a 1000 Mbit/s Ethernet port are supported by an integrated Ethernet MAC block. This block supports the eight 10/100 Mbit/s ports and the single 1000 Mbit/s port. The 10/100/1000 Mbit/s Ethernet MAC block is IEEE 802.3, 802.3x, 802.3z and 802.3ac compliant and supports Full Duplex/Half Duplex for 10/100 Mbit/s Ethernet MAC and only Full Duplex for 1000 Mbit/s Ethernet MAC (MAC implements the IEEE 802.3 MAC Control layer and PAUSE operation for flow control) mode of operation.

The main features which are supported by this block are as follows:

- Connection to external 10/100/1000 Mbit/s Ethernet PHYs or 10/100/1000 Mbit/s Ethernet Switch devices via either 8 SMII interfaces OR a single GMII interface
- Line side loopbacks for diagnostic capability
- Verify frame integrity (FCS and Length checks)
- Egress Ethernet frame encapsulation, such as, padding to achieve minimum length and FCS generation
- Programmable IPG/IFG
- Maximum frame size - 9600 bytes in SMII mode, 1650 bytes in GMII mode
- Transparent to IEEE 802.3-1998 VLAN (Virtual LAN) byte
- Supports IEEE 802.3 mandatory Control and Management Registers
- Over Subscription support by Device Configuration and Flow Control
- Option to support IEEE 802.3-1998 Flow Control at each Ethernet port
- Programmable watermarks for FIFO full conditions
- In Full Duplex mode, automatic generation of Pause frames based on FIFO fill levels. In Half Duplex mode, automatic back pressure flow control based on FIFO fill levels.
- Control to disable acting on received PAUSE frames, that enables transparent transmission of the Ethernet PAUSE frame and Reconciliation of Frames.
- Control and Statistics (to IEEE 802.3z-1998) that includes among others:
 - Detection of device, initialization, Device ID
 - Standard Control and Status Registers grouped by function: MAC Receive and Transmit Control Registers, MAC Receive and Transmit Status Registers, RMON registers (for Network Management), Flow Control Registers, MII Management Registers, Ethernet Interface Control and Status Registers
 - Performance counters to ensure roll-over compliance with standards

- Provides statistic counters to support RMON implementations (minimum support for Ethernet Statistics Group, Ethernet History Group, Alarm Group, Event Group).

SONET/SDH MAPPING

The EtherMap-3 Plus device supports mapping of Ethernet frames over SONET/SDH containers using the mappings shown in Figure 5.

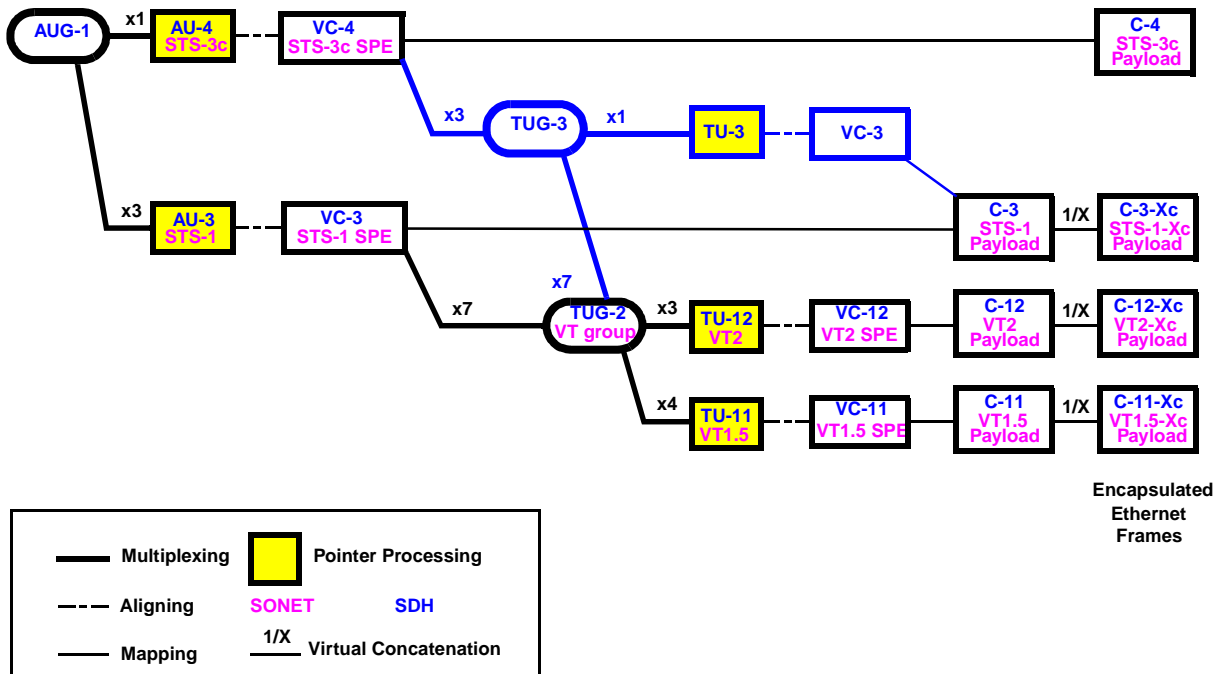


Figure 5. Mapping of Ethernet Frames Over SONET/SDH

MAPPER BLOCK

This block provides mapping and multiplexing for Low order and High order tributaries (carrying Ethernet framed data) into STS-3/STS-3c/STM-1 structures transmitted on the Add side telecom bus. A range of SONET/SDH rates and format mappings are supported as indicated below:

- STS-3c SPE
- STS-3 / STS-1 SPE
- STS-3 / STS-1 / VT1.5 SPE
- STS-3 / STS-1 / VT2 SPE
- STM-1 / AUG-1 / AU-4 / VC-4
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12 / VC-12
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11 / VC-11
- STM-1 / AUG-1 / AU-3 / VC-3
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11

- SONET Low Order: supports up to 84 x VT1.5s or up to 63 VT2s
- SONET High Order: supports up to 3 x STS-1 SPEs
- SDH Low Order: up to 84 x VC-11s or supports up to 63 x VC-12s or up to VC-3s
- SDH High Order: supports up to 3 x VC-3s

Low order VT/VC tributaries are formatted into an STS-3 or STM-1 structure. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 78 for TU-11/VT1.5 and 105 for TU-12/VT2. The microprocessor writes the signal label, and the value of the J2 message as a 16-byte message. The device provides either single-bit or extended RDI using the V5 and K4/Z7 bytes. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Remote Error Indication (REI) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated for the V5 byte. Control bits are provided for generating unequipped status, generating VT/TU AIS, and inserting REI and BIP-2 errors in the V5 byte. Control bits are also provided that enable the microprocessor to insert overhead byte test values, including the V4 byte. A list of the VT/TU Overhead byte generation functions is listed below:

- J2 Byte
 - 16 Byte Microprocessor written message
 - J2 Forced to ZERO option
- V5 and K4/Z7 byte
 - Signal label insertion
 - REI Insertion (from receive side)
 - RFI Insertion
 - Host Processor control
 - BIP-2 calculation and Insertion
 - RDI Insertion (from receive side)
 - Enable bits for alarms and Host Processor control
 - Single or extended RDI (bit 8 in V5 byte and bits 5, 6, 7 in K4/Z7 byte)
 - Generate RDI for at least 20 superframes
 - Mask Alarm Bits from sending RDI
 - Microprocessor control
 - Control spare bits in K4/Z7 byte
 - All bits in single bit RDI
 - Bits 1 through 4, and bit 8 in K4/Z7 byte
- N2/Z6 byte: No Tandem connection support
- Unequipped Channel Generation
- Supervisory Unequipped Generation
- VT/TU AIS Generation
- Low order VT/TU Pointer generation
 - Fixed to 105 for TU-12/VT2 Asynchronous Format
 - Fixed to 78 for TU-11/VT1.5 Asynchronous Format
- High order VC-3/STS-1 SPE Overhead byte generation
 - Insertion of the POH bytes into the STS-1s and VC-3s that are being mapped with the asynchronous line signals
 - J1 byte
 - 16-byte message insertion - ETSI Applications
 - 64-byte message insertion - ANSI Applications
 - H4 byte
 - The ability to generate the V1 sequence for lower order tributaries should be provided when not in the higher order virtual concatenation mode

- C2 byte
 - Signal Label Insertion
- B3 byte
 - BIP-8 Calculation and Insertion
 - Mask bit
- G1 byte
 - Single-bit (ETSI) or extended RDI generation (ANSI)
 - REI (path FEBE) insertion
 - Bit 8 insertion
- N1/Z5 byte: No tandem connection support
- Transmit Path AIS Generation for the STS-1/AU-3/TUG-3
 - Overrides Unequipped generation
- Transmit Unequipped Generation for the STS-1/AU-3/TUG-3
 - Supervisory Unequipped generation option
- High order TU-3 (VC-3)/STS-1 Pointer generation:
 - In Drop Bus timing mode the pointer bytes follow the drop C1J1 pulses
 - In Add Bus Timing Mode 1 the pointer bytes follow the add C1J1 pulses
 - In Add Bus Timing Mode 2 the pointer bytes are fixed at 0
- High order VC-4/STS-3c SPE Overhead byte generation
 - Can be generated by PHAST-3N or EtherMap-3 Plus
- High order VC-4/STS-3 SPE Pointer generation
 - All pointer generation is handled by an external Overhead Terminator device such as PHAST-3N or POP-12

DEMAPPER BLOCK

The Demapper Block provides the demapping and demultiplexing of the Low order and High order tributaries from STS-3/STS-3c/STM-1 structures received on the Drop side telecom bus. The range of formats that are supported by the Mapper Block are also supported by the Demapper Block as shown below:

- STS-3c SPE
- STS-3 / STS-1 SPE
- STS-3 / STS-1 / VT1.5 SPE
- STS-3 / STS-1 / VT2 SPE
- STM-1 / AUG-1 / AU-4 / VC-4
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12 / VC-12
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11 / VC-11
- STM-1 / AUG-1 / AU-3 / VC-3
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11
- SONET Low Order: supports up to 84 x VT1.5s or up to 63 VT2s
- SONET High Order: supports up to 3 x STS-1 SPEs
- SDH Low Order: up to 84 x VC-11s or supports up to 63 x VC-12s or up to 3 x VC-3s
- SDH High Order: supports up to 3 x VC-3s

The EtherMap-3 Plus device provides processing of the SONET/SDH overhead bytes as follows:

- Microprocessor Access to
 - All VT/TU overhead bytes, the V1/V2 pointer bytes, and the V4 byte for each channel are available for a microprocessor read cycle, as well as the H4 and V5/K4 Bytes.
- H4 Byte Multiframe Detectors or V1 pulse (C1J1V1) reference input
 - Determines Location of V1/V2 Pointer Bytes
- Pointer Tracking for V1/V2 Pointer Bytes
 - ETSI/ITU/ANSI State Machine
 - Incorrect Size Bits Detection
 - Positive/Negative Justification 8-bit Counters

For low order tributaries, this Demapper block performs pointer processing based on the location of the V1 and V2 bytes. The pointer bytes are monitored for loss of pointer and Alarm Indication Signal (AIS). The pointer tracking process is based on ETSI/ITU-T standards, which also meets ANSI requirements. Pointer increments and decrements are also counted, and the size bits are monitored for the correct value. This block also processes and monitors the various alarms found in the four overhead bytes. These operations including signal label mismatch detection, unequipped status detection, BIP-2 parity error detection and bit/block error counter, REI error counting, RFI detector, and single-bit or extended Remote Defect Indications (RDI). The RX Demapper performs a 16-byte J2 trail trace comparison on the channels selected. N2/Z6 byte processing is not supported.

Below is a bullet list of the High order VC-3/STS-1 SPE Overhead byte processing that is performed by the Demapper block:

- All received POH bytes and applicable alarm indications are made accessible for the micro-processor.
 - J1 byte trace mismatch detection
 - 16-byte trail trace alignment (MFAS pattern) and comparison - ETSI Applications
 - 64-byte message alignment (Multiframe Alignment on MFAS pattern or CR/LF alignment)
- H4 byte
 - The ability to detect and generate a V1 pulse from the H4 byte sequence for lower order tributaries is supported.
- C2 byte
 - Signal label mismatch
 - Unequipped detection and generation
 - VC AIS detection
- G1 byte
 - Single-bit (ETSI) or extended RDI detection (ANSI)
 - REI (path FEBE) calculation with 16-bit Bit or Block error count
 - Bit 8 access for host processor access
- N1/Z5 byte: Not supported

The Demapper provides complete TU-3 pointer tracking state machines including applicable alarm indications. Other higher order POH processing can be done by an external device such as the PHAST-3N or POP-12 device; high order pointer processing must be done by an external device such as the PHAST-3N or POP-12.

ETHERNET PORTS

The EtherMap-3 *Plus* provides eight independent Full Duplex/Half Duplex Serial Media Independent Interfaces (SMII) to support 10/100 Mbit/s Ethernet traffic and a single Full Duplex GMII port to support 1000 Mbit/s Ethernet traffic. Please note, the SMII interfaces are signal-shared with the GMII interface and they cannot be used together. On power-up, the GMII/SMII lead (see [“Lead Descriptions” on page 32](#)) selects between SMII and GMII interfaces.

The SMII ports allow the EtherMap-3 *Plus* to be connected to an external 10/100 Mbit/s Ethernet client (PHY/Switch). The configuration choice (PHY/Switch) is made on power-up/initialization through the PHY/MAC signal lead (see [“Lead Descriptions” on page 32](#)). The SMII interface is comprised of two signals per port (TX Data and RX Data), a global synchronization signal and a global 125 MHz reference clock. Up to eight 10/100 Mbit/s Ethernet signals (or any combination).

The Gigabit Media Independent Interface (GMII) is used to allow the mapper to connect to an external 1000 Mbit/s Ethernet client (PHY/Switch). The EtherMap-3 *Plus* device supports a SINGLE GMII interface. Please note, the GMII interface is signal-shared with the SMII interfaces and the configuration choice is made on power-up/initialization. The GMII interface is comprised of two independent RX and TX 8-bit data paths, a transmit enable signal, and a receive data valid signal. Status outputs report when coding violations are detected. Network status inputs are provided for reporting errored frames and frame received in error. All signals are synchronous to the clock.

A single Ethernet Management interface is provided on the EtherMap-3 *Plus* to connect to an external Ethernet PHY in order to configure and control its operation. This interface is used by both of the eight 10/100 Mbit/s ports or a single 1000 Mbit/s port. It is comprised of an output Management Data clock signal and a bidirectional Management Data signal that allows serial data to be clocked in and out of the external PHY device. All data transfers are synchronous to the clock signal and provides support for up to 32 PHYs.

MICROPROCESSOR INTERFACE

The EtherMap-3 *Plus*'s microprocessor interface provides support for either a standard Motorola, or a Intel split address/data bus interface which allows access to the EtherMap-3 *Plus*'s memory map register locations through a 16-bit data bus. There is a 16-bit address bus. A15 is the most significant bit in the location's address. A0 of the device will correspond to A1 of the microprocessor address bus. The mode of operation is configurable via two external package signal leads. An interrupt request lead is provided to allow the maskable interrupt bits to generate interrupts to the external microprocessor, thus reducing required Host CPU bandwidth.

SDRAM MEMORY INTERFACE

This interface is used to allow the mapper to connect an external SDRAM memory device. The external SDRAM memory device is used for buffering of Ethernet traffic in both directions and provides a “glueless” interface to 64 Mbits, 128 Mbits and 256 Mbits external SDRAM memory devices.

Virtually concatenated VCs are realigned and differential delay is accommodated by the SDRAM during the reconstruction process of the received frame.

PARALLEL TELECOM BUS INTERFACE

The Telecom Bus interface enables the EtherMap-3 *Plus* to connect to an upstream SONET/SDH Line Overhead Terminator such as TranSwitch's PHAST-3N for OC-3/STM-1 applications. For OC-12/STM-4 applications, the EtherMap-3 *Plus* would connect to TranSwitch's POP-12/PHAST-12E chip set. The Telecom Bus interface is collectively comprised of a single Drop (RX) and a single Add (TX) bus.

The EtherMap-3 *Plus* supports a single telecom bus architecture which consists of a single Drop and a single Add bus. This is the same bus architecture supported by other TranSwitch Mappers (e.g., TL3M) and

SONET/SDH Overhead Terminators (e.g., PHAST-3N, PHAST-12E, POP-12) products. The Telecom Bus operates at 19.44 MHz rate.

The telecom bus interface consists of byte wide data, 19.44 MHz (STM-1/STS-3) clock, SPE indication, C1J1(V1) pulses, even or odd parity indication, and an Add bus active indicator.

The EtherMap-3 *Plus* supports either Drop bus or Add bus timing modes. The $\overline{\text{ABUST}}$ (see "[Lead Descriptions](#)" on page 32) lead is used to provide this selection. This approach prevents bus contention upon power up or device reset.

Drop bus timing mode: In this mode, the Add bus timing is derived from the Drop bus timing input signals. When Drop bus timing mode is selected, the Add bus interface output leads are byte-wide data, a parity indicator, and an add-to-bus indicator. The Add bus clock, SPE and C1J1V1 signals, which are derived from the Drop bus, can be output or disabled. The selection is performed by a package lead.

Note the following restrictions apply when using Drop bus timing mode:

- 1) In SONET (STS-3 / STS-1-SPEs) mode, high order virtual concatenation is not supported.
- 2) In SONET (STS-3 / STS-1 SPEs / VT1.5s) mode, selection of low order tributaries (VT1.5s) for a virtual concatenation group is restricted to the same STS-1 SPE. Note that this means that any virtual concatenation group in this mode is limited to a maximum of 28 VT1.5s.
- 3) In SDH (STM-1 / AU-3 / VC-3 / TUG-2s / TU-12s / VC-12s) mode, selection of low order tributaries (VC-12s) for a virtual concatenation group is restricted to the same VC-3. Note that this means that any virtual concatenation group in this mode is limited to a maximum 21 VC-12s.

Add bus timing mode(s): In these modes, the Add bus interface timing is independent of the Drop bus interface timing and the above restrictions do not apply. Using a control bit, the Add bus interface timing signals can be configured as follows:

Add bus timing mode 1:

- Byte Clock, 19.44 MHz (input);
- SPE indicator (input);
- C1J1V1 indicator (input);
- Byte-wide Data (output);
- Parity indicator (output);
- Add-to-bus indicator (output);

Note: In this timing mode, the external timing source must ensure the three pointers (J1 pulses) when operating in STS-3/AU-3 mode, are synchronized and fixed relative to each other (i.e., there must not be any pointer movements relative to each other). The same principle applies when operating in STM-1 or STS-3c mode; no pointer adjustments are allowed on the ADD Bus. The TranSwitch PHAST-3N overhead terminator device can provide the external timing required for this mode.

Add bus timing mode 2: The Add bus interface signals are as follows:

- Byte Clock, 19.44 MHz (output), derived from input clock lead;
- SPE indicator (output);
- C1J1V1 indicator (output);
- Byte-wide Data (output);
- Parity indicator (output);
- Add-to-bus indicator (output);

Note: In this timing mode, the EtherMap-3 *Plus* sources the timing signals.

Drop bus parity can be configured to be checked over data only or over all bus signals, and to check for even or odd parity. The Drop Bus clock is monitored for stuck high and stuck low conditions. Add Bus parity can be generated as odd or even and can be generated over data only or over all signals. The Add to bus indicator

goes active to indicate when VT/TU/VC/SPE data is being added to the Add Telecom Bus. When data is not being added to the Add telecom bus, the Add data and parity are Tristated.

HIGH AND LOW ORDER POH (PATH OVERHEAD BYTE) PORT INTERFACE

The POH byte interface provides an alternative access to all of the SONET/SDH Low Order and High Order tributary POH bytes for external processing. There are two interfaces. One interface is for VT1.5/VT2/VC-11/VC-12 POH and the second interface is for STS-1/VC-3 POH or STS-3c/VC-4 POH.

Individual POH fields except TTI, Signal label and BIP-2/BIP-8 fields can be inserted into the POH from the transmit POH byte interface.

All POH bytes are provided at their respective receive POH byte interface for external processing.

HIGH AND LOW ORDER ALARM INDICATION PORT INTERFACE

The Alarm Indication Port is provided to transport the remote information (RI) signal from a mate POH monitor to the POH generator. The remote information includes REI, RDI and various extended RDI indications. There are two separate Alarm Indication Ports; one for VT1.5/VT2/VC-11/VC-12 RI, and one for STS-1/VC-3 RI or STS-3c/VC-4 RI.

ALARMS AND PERFORMANCE MONITORING BLOCKS

This block maintains and updates the statistics/performance counters for GFP, LAPS, LAPF, PPP (for all Ethernet ports) and is accessible by the host. The following types of statistics/performance counters are provided by this block:

- Flag error counters
- Payload size violation counters
- FCS error counters
- Control Field mismatch counters
- Total number of payload frames/octets transmitted counters
- Total number of payload frames/octets received counters

Mapper/Demapper statistics/performance counters (for all tributaries) are grouped within and are a part of the Mapper/Demapper block.

JTAG INTERFACE

This interface provides a five signal Boundary Scan capability that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test. In addition to the TAP, a lead is provided to place the output buffers in a high impedance state for systems that do not support the IEEE 1149.1 standard.

POWER-UP SEQUENCING

During power-up, I/O Supply Voltage VDD33 (3.3V) must lead the VDD18 (1.8V), VDDP18 (1.8V) and VDDPA18 (1.8V) supplies. In addition, the Core Supply Voltage (VDD18) needs to be brought up after I/O Supply Voltage, and can be brought up together with VDDP18 and VDDPA18 supplies. After power up, the I/O Supply Voltage must not go below the Core Supply Voltage by more than 0.5V at any time, including power down. The maximum interval that VDD18, VDDP18 and VDDPA18, must be powered up after VDD33 depends on the slew rate of power ramp-up in customer's application.

APPLICATION EXAMPLE

The EtherMap-3 Plus can be used in a broad array of telecommunications applications, such as:

- SONET/SDH add/drop and terminal multiplexers
- Multi-service access platforms (MSAP)
- Compact Access or CPE platforms
- IP DSLAMS
- Wireless Backhaul Electronics (RNC/BSC)

Multi-service Ethernet Aggregation with OC-3/STM-1 Uplink

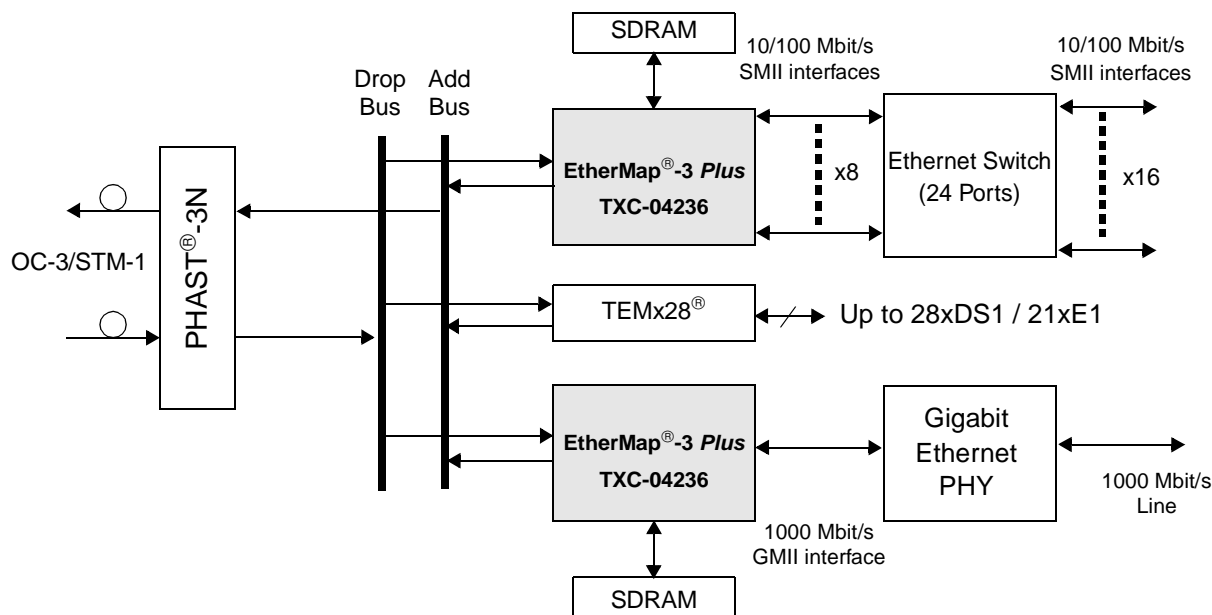
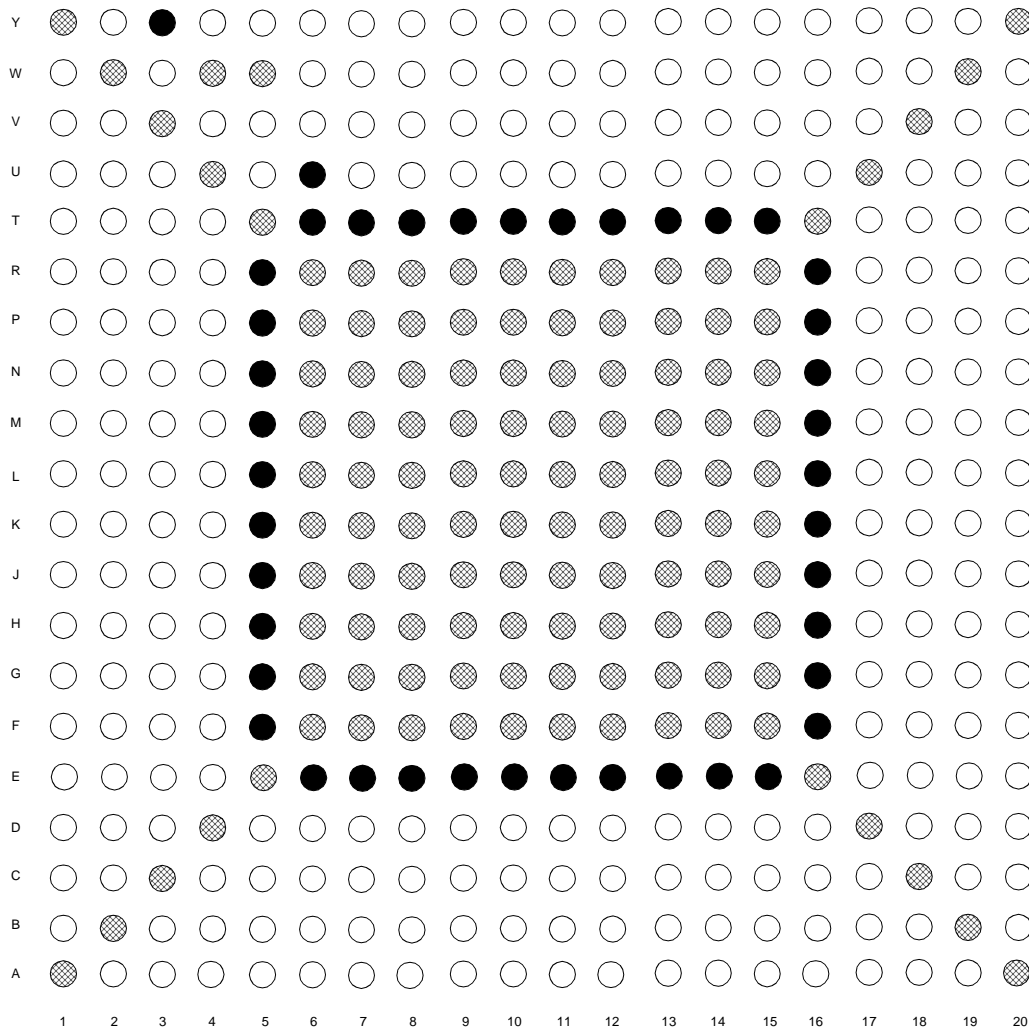


Figure 6. Typical Application using the EtherMap-3 Plus and PHAST-3N Devices

Figure 6 shows a Multiservice STM-1/STS-3 application using the EtherMap-3 Plus. The TEMx28[®] device provides access to 28xDS1 or 21 E1 channels of the STS-3/STM-1 signal. The two EtherMap-3 Plus devices are used to map Gigabit Ethernet into an STS-1-SPE/VC-3 container and a mix of 10/100 Mbit/s Ethernet Traffic into VT1.5-SPE/VT-2-SPE/VC-11/VC-12. As is demonstrated by this application, a very small number of TranSwitch components enables a board to be developed which can be used to simultaneously support a mixture of 10/100/1000 Mbit/s Ethernet Traffic and T1/E1 Traffic. By adding TranSwitch's TL3M device to the Telecom Bus, DS3 and E3 can also be supported.

LEAD DIAGRAM

BOTTOM VIEW



Notes:

1. This is the bottom view. The leads are solder balls. See [Figure 88](#) for package information. This view is rotated relative to the bottom view in [Figure 88](#).
2. Power supply leads are shown as solid black circles, ground leads as cross-hatched circles.

Figure 7. EtherMap-3 Plus TXC-04236 Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND, AND NO CONNECT LEADS

| Symbol | Lead No. | I/O/P* | Name/Function |
|---------|--|--------|---|
| VDD33 | E7, E9, E12, E14, G5, G16, J5, J16, M5, M16, P5, P16, T7, T9, T12, T14 | P | VDD33: +3.3 volt power supply, ±5% (See “Power-Up Sequencing” on page 29). |
| VDD18 | E6, E8, E10, E11, E13, E15, F5, F16, H5, H16, K5, K16, L5, L16, N5, N16, R5, R16, T6, T8, T10, T11, T13, T15 | P | VDD18: +1.8 volt power supply, ±5% (See “Power-Up Sequencing” on page 29). |
| VSS | A1, A20, B2, B19, C3, C18, D4, D17, E5, E16, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T5, T16, U4, U17, V3, V18, W2, W19, Y1, Y20 | P | Ground: 0 (zero) Volts reference. |
| VDDP18 | Y3 | P | VDDP18: +1.8 volt digital power supply for the PLL, ±5% (See “Power-Up Sequencing” on page 29). |
| VDDPA18 | U6 | P | VDDPA18: +1.8 volt analog power supply for the PLL, ±5% (See “Power-Up Sequencing” on page 29). |
| VSSP18 | W4 | P | VSSP18: digital ground for the PLL. |
| VSSPA18 | W5 | P | VSSPA18: analog ground for the PLL. |
| NC | A2, A6, A10, A11, A19, B1, B3, B7, B11, B15, B18, B20, C2, C4, C8, C14, C17, C19, D5, D13, D16, D18, U8, U18, V2, V4, V7, V17, V19, W1, W3, W10, W14, W18, W20, Y2, Y9, Y10, Y15, Y19 | - | No Connect: These leads are not to be connected, not even to another no connect lead, and must be left floating. Connection of an NC lead may impair performance or cause damage to the device. NC leads that are currently unused may be assigned functions in a future version of the device, affecting its usability in applications which have not left them floating. |

* Note: I = Input; O = Output; OD=Open Drain Output; P = Power; T = Tristate:



DATA SHEET

EtherMap-3 Plus
TXC-04236

DROP SIDE LOW ORDER TRIBUTARY TELECOM BUS INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---------|------------------------------------|-------|---------|--|
| DD(7-0) | D10, A9, B9, C10, A12, C9, A8, B10 | I | LVTTL-5 | Drop Bus Data In: Byte wide data corresponding to the STM-1/STS-3c/STS-3 signal from the Drop bus. The first bit received (dropped) corresponds to bit 7. |
| DCLK | B12 | I | LVTTL-5 | Drop Bus Clock: This clock operates at 19.44 MHz for STM-1/STS-3c/STS-3 operation and is used to clock data and other signals into the EtherMap-3 Plus. Drop bus byte wide data, the parity bit, SPE indication, and the C1J1(V1) signals are clocked into the EtherMap-3 Plus core on negative transitions of this clock. This clock is also used for timing and may be used to derive the like named Add bus byte wide data, add, VT/TU indications, and parity bits. In Drop timing mode, this clock is used to source the Add traffic and should therefore be +/- 20 ppm maximum. If Drop timing mode is selected, this clock must be present before the initial configuration of the device. |
| DC1J1V1 | A13 | I | LVTTL-5 | Drop Bus SPE Indicator/Multiframe Pulse: An active high timing signal that carries frame and SPE information. Is high during the J0 and J1 bytes in the STM-1/STS-3c/STS-3 payload. Three J1 pulses are present for STS-3 operation and one J1 pulse is present for STM-1/STS-3c operation. The V1 pulse is optional in the C1J1 signal. When the V1 pulse is not provided, the EtherMap-3 Plus core provides H4 detectors to determine the location of the V1/V2 bytes in place of using the V1 pulse. When the V1 pulses are provided, there will be up to three V1 pulses for STS-3 operation and one V1 pulse for STM-1/STS-3c operation. The DC1J1V1 signal works in conjunction with the DSPE signal. The C1 pulse identifies the location of the J0 byte in the STM-1/STS-c/STS-3 signals, when DSPE signal is low. The J1 pulses identify the starting location of the J1 bytes in the STM-1/STS-3c/STS-3 signal when DSPE is high. The V1 pulses occur every four frames (after the frame where the H4 byte is set to 00H) following the J1 pulse(s). |
| DSPE | D11 | I | LVTTL-5 | Drop Bus SPE Indicator: A signal that is active high during each byte of the STM-1/STS-3c/STS-3 POH and payload bytes, and low during Transport Overhead byte times. |
| DPAR | C11 | I | LVTTL-5 | Drop Bus Parity Bit: Parity bit input signal that represents the parity calculation for each data byte, SPE, and C1J1V1 signal from the bus. Even or odd parity may be detected, and an option for checking the parity over DD(7-0) only or over all of the drop bus signals is provided. A parity error is reported but otherwise has no effect on the operation of the EtherMap-3 Plus core. |

ADD SIDE LOW ORDER TRIBUTARY TELECOM BUS INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---------|---|-------|------------------------------|--|
| AD(7-0) | D6, D7, C6, B5, A4, B6, C7, A5 | O(T) | LVC MOS 8 mA | Add Bus Data Byte In: Byte wide data that corresponds to the selected VT/TU//VC. |
| ACLK | B8 | I/O | LVTTL-5/ LVC MOS 12 mA | <p>Add Bus Clock: This clock operates at 19.44 MHz. When add bus timing is selected and ctBADD=0, a clock on this input must be provided for add bus timing. In this case AC1J1V1 and ASPE are clocked in on negative transitions of this clock while AD(7-0), APAR, and ADD are clocked out on positive transitions of this clock.</p> <p>This above case is the default value for ctBADD. When add bus timing is selected and ctBADD=1, a clock is output on this lead. AC1J1V1, ASPE, AD(7-0), APAR, and ADD are clocked out on positive transitions of this clock. In that case, RTCLK and DCLK clock inputs must be active.</p> <p>When drop bus timing is selected, an option (\overline{ABTE} is low) is provided for outputting this clock along with the other Add Bus signals, which are derived from DCLK, otherwise this lead is disabled.</p> <p>If Add slave timing mode is selected, this input clock must be already present during the initial configuration of the device.</p> <p>If Add master timing mode is selected, this output clock must be pulled high with a weak pull-up (like 10k ohm). After a hard reset, the first microprocessor access must be to set the ctBADD register to 1. At this moment, the EtherMap-3 Plus will be able to drive the clock.</p> |
| AC1J1V1 | A7 | I/O | LVTTL-5/ LVC MOS 8 mA | <p>Add Bus SPE Indicator/Multiframe Pulse: When add bus timing is selected and ctBADD=0, this signal is an input and must be provided for add bus timing. When add bus timing is selected and ctBADD=1, this signal is output by the device for add bus timing.</p> <p>Composite active high input timing signal that carries STM-1, STS-3c, or STS-3 starting frame and J1 byte location information. This timing signal functions in conjunction with the ASPE signal. The C1 (J0) pulse identifies the location of the first C1 (J0) byte in the SONET/SDH frame when ASPE is low. A J1 pulse identifies the starting location of the J1 byte for the VC-4 signal or STS-3c-SPE or three J1 pulses identify the starting location of the three J1 bytes for the STS-1-SPE signals when ASPE is high. One or more V1 pulses may be present for asynchronous VT/TU mappings to determine the starting location of the V1 byte.</p> <p>When drop bus timing is selected, an option (\overline{ABTE} is low) is provided for outputting this signal, otherwise this lead is disabled.</p> |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|-------------------------|----------|-------|----------------------------|--|
| ASPE | D9 | I/O | LVTTL-5/ LVCMOS 8 mA | Add Bus SPE Indicator: When add bus timing is selected and cTBADD=0 , this signal is an input and must be provided for add bus timing. When add bus timing is selected and cTBADD=1 , this signal is output by the device for add bus timing. This signal is active high during each byte of the STS-3/STM-1/STS-1 payload, and low during Transport Overhead times. When drop bus timing is selected, an option ($\overline{\text{ABTE}}$ is low) is provided for outputting this signal, otherwise this lead is disabled. |
| APAR | D8 | O(T) | LVCMOS 8mA | Add Bus Parity Bit: An odd or even parity output signal which is calculated over the byte wide add data. This 3-state lead is only active when there is data being added to the Add bus. A control bit is provided that allows even parity to be calculated. |
| $\overline{\text{ADD}}$ | C5 | O | LVCMOS 8 mA | Add Bus Add Data Present Indicator: This active low signal is present when output data to the Add bus is valid. It identifies the location of all of the VT/TU/VC time slots being added to the Add bus. When in VC-4/STS-3c mode, when the HighZ_AU3 bits are set to '0' for all 3 timeslots, the entire VC-4/STS-3c SPE will be indicated as active. Additionally in the Add bus master mode, the H1, H2, H3 pointer bytes that are output will be indicated as active. |

ETHERNET GMII/ 8xSMII INTERFACES

The control lead $\overline{\text{GMII/SMII}}$ selects when low, the group of eight SMII Ethernet interfaces, and when high, selects the single GMII interface. The GMII interface is described in the section below, and also how the leads are shared with the SMII interface leads. Each SMII interface is comprised of a 125 MHz Serial Data Transmit Output (SMII_DOn) and Serial Data Receive Input (SMII_DIn); where n = 1-8. The SMII data interface is a serial streaming of the standard 100 Mbit/s (Fast Ethernet) MII interface (Media Independent Interface).

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---------|----------|-------|-----------------|---|
| GTX_CLK | Y13 | O | LVCMOS 12 mA | Gigabit Ethernet Transmit Clock Output: The GTX_CLK is used to drive the TXD(7-0), TX_EN, and TX_ER signals; runs at 125 MHz. |
| TX_CLK | U11 | I | LVTTL-5 | Transmit Clock: This is a 125 MHz input clock, required only in GMII mode, and only in these two cases: 1) When control lead $\overline{\text{PHY/MAC}}$ is low. 2) When the MAC Loopback (see page 193) is selected. To comply with 802.3ab, the frequency tolerance must be +/- 0.01%. |

EtherMap-3 Plus
TXC-04236

DATA SHEET



| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---------------------------------|---|-------|-----------------------------|---|
| TX_EN /(SMII_ GSYNC) | W13 | I/O | LVTTL-5/ LVCMOS 12 mA | GMII Transmit Enable/Global SMII SYNC: When GMII/SMII control lead is high, this lead is used to output a control signal to indicate valid data is being presented on the GMII TXD(7-0) leads. When GMII/SMII control lead is low and SYNC_DIR control lead is high, this lead is used to output a global SYNC signal (i.e., common for all eight SMII interfaces). When GMII/SMII control lead is low and SYNC_DIR control lead is low, this lead is used to input a global SYNC signal (i.e., common for all eight SMII interfaces). |
| TX_ER | V12 | O | LVCMOS 8 mA | Transmit Error: This output signal is asserted to indicate to the PHY that a coding violation was received in the input data stream. |
| TXD(7-0) /(SMII_ DO(8-1)) | U12, Y14, V13, U13, W15, Y16, V14, U14 | O | LVCMOS 12 mA | Transmit Data Out: Data output is transmitted as a group of eight data signals, by the RS to the PHY. When GMII/SMII control lead is low, these leads operate as the eight SMII interface Data Out signals - SMII_DOn (n = 1 - 8) and correspond to the MAC # (i.e., TXD7 corresponds to SMIIIDO8). |
| RXD(7-0) /(SMII_ DI(8-1)) | Y11, Y8, U10, V10, V9, W9, W8, U9 | I | LVTTL-5 | Receive Data In: Data received by the PHY is passed as a group of eight data signals to the DTE. When GMII/SMII control lead is low, these leads operate as the eight SMII interface Data In signals - SMII_DIn (n = 1 - 8) and correspond to the MAC # (i.e., RXD7 corresponds to SMIIIDI8). |
| RX_DV | W11 | I | LVTTL-5 | Receive Data Valid: This signal is asserted by the PHY to indicate to the DTE that valid data (octets) are being presented on the RXD(7-0) inputs. |
| RX_ER | Y12 | I | LVTTL-5 | Receive Data Error: This signal is asserted to indicate to the DTE a frame received in error. |
| RX_CLK /(SMII_ GCLK) | V11 | I | LVTTL | Receive Clock: The clock is recovered by the PHY from the incoming data stream, and passed onto the DTE. RX_CLK runs at either 2.5 MHz for 10 Mbit/s Ethernet or 25 MHz for 100 Mbit/s operation. When GMII/SMII control lead is low, operates as the 125 MHz SMII_GCLK. Note: The duty cycle should be 40% to 60%. To comply with 802.3ab, the frequency tolerance must be +/- 0.01%. |
| MDIO | Y7 | I/O | LVTTL-5/ LVCMOS 8 mA | Management Data I/O: Data input/output for the IEEE 802.3u compliant Management and Status interface. |
| MDC | V8 | O | LVCMOS 8 mA | Management Data Interface Clock: The management data I/O (MDIO) is clocked into and out of the EtherMap-3 on the rising edge of this clock. The frequency for this clock is derived from the microprocessor clock input (MICCLK) divided by a factor of 4 to 28 (Max = 12.5 MHz, see Mgmt Clock Select Table 24, on page 215). |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

SDRAM INTERFACE

The following table shows a standard 32 bit wide Data, SDRAM interface. There are thirteen address bits, that include bank Selection as needed; input mask bits (byte-wise); write enable, RAS/CAS, clock and clock enable.

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|------------|--|--------|----------------------------|---|
| DATA(31-0) | N18, R20, P18, T20, R18, U20, T18, V20, T17, U19, R17, T19, P17, R19, N17, P19, E17, D19, F17, E19, G17, F19, H17, G19, H18, F20, G18, E20, F18, D20, E18, C20 | I/O(T) | LVTTL/ LV3CMOS 16 mA | SDRAM Controller External Data I/O: 32 bits wide data bus; byte wise tristateable. Bit 0 is the least significant bit. |
| ADDR(12-0) | K18, K19, N20, J20, K20, L19, L18, L17, M18, M17, P20, N19, M19 | O | LV3CMOS 16 mA | Address Bus: 13 bits wide. Bit 0 is the least significant bit. |
| BA(1-0) | M20, L20 | O | LV3CMOS 16 mA | Bank Select: These signals are used to select the Banks in a standard SDRAM. |

| Symbol | Lead No. | I/O/P | Type | Name/Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|-------------------------|------------------------|--|---|-------------------------|-------------------------|------------------------|----------|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| $\overline{\text{RAS}}$ | J19 | O | LV3CMOS 16 mA | <p>Row Address Strobe: For control of external SDRAM. This signal along with $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the command being given to the external SDRAM.</p> <table border="1"> <thead> <tr> <th>$\overline{\text{RAS}}$</th> <th>$\overline{\text{CAS}}$</th> <th>$\overline{\text{WE}}$</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>NOP: No operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ACTIVE: Used to activate a row in a particular bank. The BA(1-0) selects the bank, and ADDR(12-0) selects the row.</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>READ: Used to initialize the SDRAM for a burst read.</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>WRITE: Used to initialize the SDRAM for a burst write.</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>PRECHARGE: Deactivate open row in a bank or banks.</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>AUTO REFRESH: This command is performed every 2480 SYSCLK period, to ensure that all of the SDRAM rows are refreshed. This default setting can be changed by SDRARP at register address 0x1d604.</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>LOAD MODE REGISTER: This command is issued at the end of the configuration step, to configure the internal mode register of the SDRAM. It is the last command before the SDRAM to be ready for read/write accesses.</td> </tr> </tbody> </table> | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Function | 1 | 1 | 1 | NOP: No operation | 0 | 1 | 1 | ACTIVE: Used to activate a row in a particular bank. The BA(1-0) selects the bank, and ADDR(12-0) selects the row. | 1 | 0 | 1 | READ: Used to initialize the SDRAM for a burst read. | 1 | 0 | 0 | WRITE: Used to initialize the SDRAM for a burst write. | 0 | 1 | 0 | PRECHARGE: Deactivate open row in a bank or banks. | 0 | 0 | 1 | AUTO REFRESH: This command is performed every 2480 SYSCLK period, to ensure that all of the SDRAM rows are refreshed. This default setting can be changed by SDRARP at register address 0x1d604. | 0 | 0 | 0 | LOAD MODE REGISTER: This command is issued at the end of the configuration step, to configure the internal mode register of the SDRAM. It is the last command before the SDRAM to be ready for read/write accesses. |
| $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | NOP: No operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | ACTIVE: Used to activate a row in a particular bank. The BA(1-0) selects the bank, and ADDR(12-0) selects the row. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | READ: Used to initialize the SDRAM for a burst read. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | WRITE: Used to initialize the SDRAM for a burst write. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | PRECHARGE: Deactivate open row in a bank or banks. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | AUTO REFRESH: This command is performed every 2480 SYSCLK period, to ensure that all of the SDRAM rows are refreshed. This default setting can be changed by SDRARP at register address 0x1d604. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | LOAD MODE REGISTER: This command is issued at the end of the configuration step, to configure the internal mode register of the SDRAM. It is the last command before the SDRAM to be ready for read/write accesses. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{CAS}}$ | H19 | O | LV3CMOS 16 mA | <p>Column Address Strobe: For control of external SDRAM. This signal along with $\overline{\text{WE}}$ and $\overline{\text{RAS}}$ define the command being given to the external SDRAM. Refer to the table in the $\overline{\text{RAS}}$ lead description.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{WE}}$ | J17 | O | LV3CMOS 8 mA | <p>Write Enable: For control of external SDRAM. This signal along with $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ define the command being given to the external SDRAM. Refer to the table in the $\overline{\text{RAS}}$ lead description.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{CS}}$ | H20 | O | LV3CMOS 16 mA | <p>Chip Select: For control of external SDRAM. Used to select and deselect external SDRAM.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MASK | G20 | O | LV3CMOS 8 mA | <p>Mask Bits: This control output is used to mask out the standard 32 bit wide SDRAM memory interface. It is used to tristate the SDRAM data bus during a READ cycle and to mask the SDRAM data bus during a WRITE cycle.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



DATA SHEET

EtherMap-3 Plus
TXC-04236

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|--|
| CLK | J18 | O | LV3CMOS 16 mA | Interface Clock: For control of external SDRAM. All SDRAM interface signals are sampled/output on the rising edge of this clock, which runs at 100 MHz. |
| CLKE | K17 | O | LV3CMOS 16 mA | Interface Clock Enable: Tied high internally. Can be used to drive the clock enable pin of an external SDRAM. |

RECEIVE VC-3 PATH OVERHEAD (VC-3POH) BYTE INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|---|
| RPCLK | C13 | O | LVC MOS 12 mA | Receive VC-3POH Interface Clock: The receive VC-3POH address (RPADD), address latch enable (RPALE), data (RPDAT), and data latch enable (RPDLE) signals are clocked out on falling edges of this clock (2.43 MHz). |
| RPALE | A14 | O | LVC MOS 4 mA | Receive VC-3POH Interface Address Latch Enable: A positive 8 (RPCLK) clock cycle-wide pulse that indicates a valid address (eight consecutive bits) present on RPADD. |
| RPADD | D12 | O | LVC MOS 4 mA | Receive VC-3POH Interface Address: The states present on this lead during address latch enable time indicate the output VC-3POH byte and the SDH/SONET format. Eight consecutive bits make up a valid address. |
| RPDLE | B13 | O | LVC MOS 4 mA | Receive VC-3POH Interface Data Latch Enable: A positive 8 (RPCLK) clock cycle-wide pulse that indicates valid data present on RPDAT. |
| RPDAT | C12 | O | LVC MOS 4 mA | Receive VC-3POH Interface Data: The states present on this lead over eight consecutive bits, during data latch enable time constitute the output byte data selected by the address. |

TRANSMIT VC-3 PATH OVERHEAD (VC-3POH) BYTE INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|---|
| TPCLK | D3 | O | LVC MOS 12 mA | Transmit VC-3POH Interface Clock: The transmit POH address (TPADD), address latch enable (TPALE), and data latch enable (RPDLE) signals are clocked out on falling edge of TPCLK (2.43 MHz). Data (TPDAT), is clocked in on the rising edge of this clock. |
| TPALE | E4 | O | LVC MOS 4 mA | Transmit VC-3POH Interface Address Latch Enable: A positive 8 (TPCLK) clock cycle-wide pulse that indicates a valid address (eight consecutive bits) present on TPADD. |
| TPADD | C1 | O | LVC MOS 4 mA | Transmit VC-3POH Interface Address: The states present on this lead during address latch enable time indicate the output POH byte and the SDH/SONET format. Eight consecutive bits make up a valid address. |
| TPDLE | D2 | O | LVC MOS 4 mA | Transmit VC-3POH Interface Data Latch Enable: A positive 8 (TPCLK) clock cycle-wide pulse that indicates valid data present on TPDAT. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|---------|---|
| TPDAT | E3 | I | LVTTL-5 | Transmit VC-3POH Interface Data: The states present on this lead over eight consecutive bits, during data latch enable time, constitute the input byte data selected by the address. |

RECEIVE LOWER ORDER PATH OVERHEAD (LOPOH) BYTE INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|--|
| RPCLK1 | D15 | O | LVC MOS 12 mA | Receive LOPOH Interface Clock: The receive LOPOH address (RPADD1), address latch enable (RPALE1), data (RPDAT1), and data latch enable (RPDLE1) signals are clocked out on falling edges of this clock (19.44 MHz). |
| RPALE1 | A17 | O | LVC MOS 4 mA | Receive LOPOH Interface Address Latch Enable: A positive 12 (RPCLK1) clock cycle-wide pulse that indicates a valid address (twelve consecutive bits) present on RPADD1. |
| RPADD1 | B16 | O | LVC MOS 4 mA | Receive LOPOH Interface Address: The states present on this lead during address latch enable time indicate the output LOPOH byte and the SDH/SONET format. Twelve consecutive bits make up a valid address. |
| RPDLE1 | C15 | O | LVC MOS 4 mA | Receive LOPOH Interface Data Latch Enable: A positive 8 (RPCLK1) clock cycle-wide pulse that indicates valid data present on RPDAT1. |
| RPDAT1 | D14 | O | LVC MOS 4 mA | Receive LOPOH Interface Data: The states present on this lead over eight consecutive bits, during data latch enable time constitute the output byte data selected by the address. |

TRANSMIT LOWER ORDER PATH OVERHEAD (LOPOH) BYTE INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|---|
| TPCLK1 | F3 | O | LVC MOS 12 mA | Transmit LOPOH Interface Clock: The transmit LOPOH address (TPADD1), address latch enable (TPALE1), and data latch enable (RPDLE1) signals are clocked out on falling edge of TPCLK1 (19.44 MHz). Data (TPDAT1), is clocked in on the rising edge of this clock. |
| TPALE1 | G4 | O | LVC MOS 4 mA | Transmit LOPOH Interface Address Latch Enable: A positive 12 (TPCLK1) clock cycle-wide pulse that indicates a valid address (twelve consecutive bits) present on TPADD1. |
| TPADD1 | E1 | O | LVC MOS 4 mA | Transmit LOPOH Interface Address: The states present on this lead during address latch enable time indicate the output LOPOH byte and the SDH/SONET format. Twelve consecutive bits make up a valid address. |
| TPDLE1 | F2 | O | LVC MOS 4 mA | Transmit LOPOH Interface Data Latch Enable: A positive 8 (TPCLK1) clock cycle-wide pulse that indicates valid data present on TPDAT1. |
| TPDAT1 | G3 | I | LVTTL-5 | Transmit LOPOH Interface Data: The states present on this lead over eight consecutive bits, during data latch enable time, constitute the input byte data selected by the address. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

RECEIVE (VC-3) HIGH ORDER ALARM INDICATION PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|---|
| RAIPF | A16 | O | LVC MOS 4 mA | Receive HO Alarm Indication Port Frame Pulse: A active high one (RAIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream. |
| RAIPC | A15 | O | LVC MOS 12 mA | Receive HO Alarm Indication Port Clock: A 19.44 MHz output clock used for clocking the frame pulse (RAIPF) and the serial data (RAIPD) into the mate device. |
| RAIPD | B14 | O | LVC MOS 4 mA | Receive HO Alarm Indication Port Data: A serial frame that contains the REI count and RDI alarm states for the high order SPE/VCs. |

TRANSMIT (VC-3) High Order ALARM INDICATION PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|---------|---|
| TAIPF | F4 | I | LVTTL-5 | Transmit HO Alarm Indication Port Frame Pulse: A active high one (TAIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream. Connected to RAIPF on mate device. |
| TAIPC | D1 | I | LVTTL-5 | Transmit HO Alarm Indication Port Clock: A 19.44 MHz output clock used for clocking in the frame pulse (TAIPF1) and the serial data (TAIPD1). Connected to RAIPC on mate device. |
| TAIPD | E2 | I | LVTTL-5 | Transmit HO Alarm Indication Port Data: A serial frame that contains the REI count, RDI alarm states, and the Tandem Connection monitoring and alarm states for the individual TU-3 VC-3 Paths. Connected to RAIPD on mate device. |

RECEIVE LOW ORDER ALARM INDICATION PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|------------------|---|
| RAIPF1 | A18 | O | LVC MOS 4 mA | Receive LO Alarm Indication Port Frame Pulse: A active high one (RAIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream. |
| RAIPC1 | B17 | O | LVC MOS 12 mA | Receive LO Alarm Indication Port Clock: A 19.44 MHz output clock used for clocking the frame pulse (RAIPF1) and the serial data (RAIPD1) into the mate device. |
| RAIPD1 | C16 | O | LVC MOS 4 mA | Receive LO Alarm Indication Port Data: A serial frame that contains the REI count and RDI alarm states for the VT/TUs. |

TRANSMIT LOW ORDER ALARM INDICATION PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|---------|--|
| TAIPF1 | H4 | I | LVTTL-5 | Transmit LO Alarm Indication Port Frame Pulse: A active high one (TAIPC) clock cycle-wide frame pulse that identifies bit 1 in the data stream. Connected to RAIPF1 on mate device. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|---------|---|
| TAIPC1 | F1 | I | LVTTL-5 | Transmit LO Alarm Indication Port Clock: A 19.44 MHz output clock used for clocking in the frame pulse (TAIPF1) and the serial data (TAIPD1). Connected to RAIPC1 on mate device. |
| TAIPD1 | G2 | I | LVTTL-5 | Transmit LO Alarm Indication Port Data: A serial frame that contains the REI count, RDI alarm states, and the Tandem Connection monitoring and alarm states for the individual LO VT/TU Paths. Connected to RAIPD1 on mate device. |

CONTROLS

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|-------------------------------|----------|-------|----------|--|
| $\overline{\text{GMII/SMII}}$ | W16 | I | LVTTL-5p | GMII/SMII Interface Select: A low selects 8x SMII Ethernet interfaces in place of a single GMII. This lead has an internal pull-up resistor. |
| $\overline{\text{HIGHZ}}$ | Y17 | I | LVTTL-5p | High Impedance Select: A low forces all output leads, except for the boundary scan data output TDO, to the high impedance state for testing purposes. This lead has an internal pull-up resistor. |
| $\overline{\text{RESET}}$ | V16 | I | LVTTL-5p | Reset: An active low signal used for resetting the internal cores and performance counters within the EtherMap-3 Plus to preset values. The reset must be applied only after power is applied and stable, and the clocks are also stable. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor. After de-assertion of this lead, a 2 microsecond wait period must be observed, where no microprocessor access can be made. |
| $\overline{\text{ABTE}}$ | W17 | I | LVTTL-5p | Add Bus Timing Signals Enabled: An active low signal enables the ACLK, ASPE, AC1J1V1 to be outputs when drop bus timing is selected. This lead has an internal pull up resistor. A high on this lead causes those signals to be tristated. |
| $\overline{\text{ABUST}}$ | Y18 | I | LVTTL-5p | Add Bus Timing Selection: A low selects the add bus timing mode. When add bus timing is selected, ACLK, ASPE, and AC1J1V1, can be programmed to be inputs and used to source the AD(7-0), APAR, and ADD signal, or they can be generated internally and be provided as output signals. A high selects drop bus timing. The signals for the add direction are derived from the drop bus. This lead has an internal pull up resistor. |
| $\overline{\text{PHY/MAC}}$ | U16 | I | LVTTL-5p | PHY/MAC Interface Select: In SMII mode, a low selects the MAC-to-MAC interconnection type for the Ethernet side, while a high selects the MAC-to-PHY interconnection. In GMII mode, a high, selects RX_CLK as the source for GTX_CLK and a low, selects TX_CLK as the source for GTX_CLK. Note: In GMII mode, if the MAC loopback is enabled, TX_CLK is always required as the source of GTX_CLK, independent of PHY/MAC state. This lead has an internal pull-up resistor. In SMII mode, whatever the value of this input, RX_CLK is used as reference clock. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|----------|----------|-------|----------|---|
| SYNC_DIR | W12 | I | LVTTL-5p | Global SYNC Direction Select: In SMII mode and when low, the SMII_GSYNC signal is an input. In SMII mode and when high, the SMII_GSYNC signal is an output. In GMII mode, this lead must be kept high. This lead has an internal pull-up resistor. |

CLOCK INTERFACES

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--------|----------|-------|----------|---|
| RTCLK | A3 | I | LVTTL-5d | Reference Mapper/Demapper clock: This clock is a 19.44 MHz clock, (40% - 60% max. duty cycle) used by the Mapper/Demapper blocks. The RTCLK signal is required for all operating modes, but in Add Bus Master Mode (cTBADD = 1, lead ABUST = low) this input should be +/- 20 ppm maximum, since in that mode it is the source of ACLK. This clock does not have to have any relationship to ACLK. |
| SYSCLK | W7 | I | LVTTL-5 | System Reference Clock: A 50 MHz input clock, with max. 40% - 60% duty cycle and minimum accuracy of +/- 100 ppm. This clock is internally doubled via a PLL to 100 MHz and is used as the system clock for all other functions except the Mapper/Demapper block. |
| ONESEC | B4 | I | LVTTL-5d | One Second Performance Measurement Clock: This clock input is used for the one second shadow counters, and PM/FM alarm registers. This input can be either below: a) 1.0 Hz (+/- 32 ppm) clock, b) 1.0 Hz pulse, with a minimum 51.44 ns high time. |

HOST PROCESSOR INTERFACE

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---------|--|-------|---------|--|
| MICCLK | H3 | I | LVTTL-5 | Microprocessor Clock: This clock should come from the microprocessor being interfaced to this device. For Intel and Motorola 68360 modes, it is recommended that this lead be connected to the microprocessor bus clock. In Motorola MPC860 mode, this clock must be synchronous to the microprocessor bus clock. |
| A(15-0) | V1, U1, R4, U2, T3, P2, N2, R1, R3, T2, P4, N4, M4, M3, T1, P3 | I | LVTTL-5 | Address Bus: These leads are active high address line inputs that are used by the host processor for accessing the EtherMap-3 Plus for a read/write cycle. A15 is the most significant bit in the location's address. A0 of the device will correspond to A1 of the microprocessor address bus. |

EtherMap-3 Plus
TXC-04236
DATA SHEET


| Symbol | Lead No. | I/O/P | Type | Name/Function |
|--|--|--------|----------------------------|--|
| D(15-0) | L2, H1, G1, J4, K4, K3, M1, H2, L1, L3, J1, J3, K2, J2, N1, K1 | I/O(T) | LVTTL-5/ LVCMOS 8 mA | Data Bus: Bidirectional data lines used for transferring data between the EtherMap-3 Plus and the host processor. D15 is the most significant bit. |
| $\overline{\text{SEL}}$ | N3 | I | LVTTL-5p | Select: A low enables data transfers between the host processor and the EtherMap-3 Plus a read/write cycle. This lead has an internal pull-up resistor. |
| $\overline{\text{WR}}/$ $\overline{\text{DS}}/\overline{\text{TS}}$ | M2 | I | LVTTL-5 | Write Enable (Intel Mode)/Data Strobe (Motorola Mode)/Transfer Start (Motorola Mode): An active low signal. Intel Mode: Asserted low to initiate a write cycle. Motorola 68360 Mode: This is the data strobe signal which indicates that the host processor is ready to accept data during a read cycle or has put valid data on the bus during a write cycle. Motorola MPC860 Mode: Indicates the start of a new bus cycle when it becomes asserted. |
| $\overline{\text{RD}}/$ $(\text{RD}/\overline{\text{WR}})$ | R2 | I | LVTTL-5 | Read (Intel Mode) or Read/Write (Both Motorola Modes): An active low signal that is asserted low to initiate a Read cycle in the Intel Mode. In either of the Motorola Modes, high on this lead initiates a Read, and low initiates a Write. |
| $\overline{\text{READY}}/$ $\overline{\text{DTACK}}/\overline{\text{TA}}$ | P1 | OD | LVCMOS 24 mA | Ready (Intel Mode)/Data Transfer Acknowledge (Motorola Mode)/Transfer Acknowledge (Motorola Mode): Intel Mode: A high indicates that a transfer to/from the memory can be accomplished. The high (active) state is kept for two MICCLK cycles. Motorola 68360 Mode: This lead is an active low, and indicates either that the data on the bus is valid during a Read operation, or, indicates data acceptance during a Write operation. The low (active) state is kept for two MICCLK cycles. Motorola MPC860 Mode: This lead is an active low, and indicates either that the data on the bus is valid during a Read operation, or, indicates data acceptance during a Write operation. The low (active) state is synchronous to MICCLK and is one MICCLK cycle wide. Note: This output is an open-drain buffer which requires an external pull-up resistor. |
| $\text{INT}/\overline{\text{IRQ}}$ | L4 | O | LVCMOS 8 mA | Interrupt: Intel Mode: A high on this output lead signals an interrupt request to the host processor. Both Motorola Modes: A low on this output lead signals an interrupt request to the host processor. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| Symbol | Lead No. | I/O/P | Type | Name/Function | | | | | | | | | | | | | | | |
|-----------|----------|--------------------------------------|---------|--|-------|-------|-----------|---|---|----------------------------|---|---|-------------------------------------|---|---|--------------------------------------|---|---|-------------|
| MOTO(1-0) | U3, T4 | I | LVTTL-5 | <p>Intel/Motorola: Selector lead for selecting the Intel/Motorola interface:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>MOTO1</th> <th>MOTO0</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Intel Processor Interface.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Motorola 68360 Processor Interface.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Motorola MPC860 Processor Interface.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Do not use.</td> </tr> </tbody> </table> | MOTO1 | MOTO0 | Interface | 0 | 0 | Intel Processor Interface. | 0 | 1 | Motorola 68360 Processor Interface. | 1 | 0 | Motorola MPC860 Processor Interface. | 1 | 1 | Do not use. |
| MOTO1 | MOTO0 | Interface | | | | | | | | | | | | | | | | | |
| 0 | 0 | Intel Processor Interface. | | | | | | | | | | | | | | | | | |
| 0 | 1 | Motorola 68360 Processor Interface. | | | | | | | | | | | | | | | | | |
| 1 | 0 | Motorola MPC860 Processor Interface. | | | | | | | | | | | | | | | | | |
| 1 | 1 | Do not use. | | | | | | | | | | | | | | | | | |

BOUNDARY SCAN (IEEE STANDARD 1149.1)

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|-------------------------|----------|-------|-----------------|--|
| TCK | V6 | I | LVTTL-5 | Test Boundary Scan Clock: This signal is used to shift data into TDI on its rising edge and out of TDO on its falling edge. The maximum clock frequency is 10 MHz. |
| TDI | U7 | I | LVTTL-5p | Test Boundary Scan Data Input: Serial test instructions and data are clocked into this lead on the rising edge of TCK. This lead has an internal pull-up resistor. |
| TDO | Y5 | O | LVC MOS 8 mA | Test Boundary Scan Data Output: Serial data test instructions and data are clocked out of this lead on the falling edge of TCK. When inactive, this lead goes to a high impedance state. |
| TMS | W6 | I | LVTTL-5p | Test Boundary Scan Mode Select: This input lead is sampled on the rising edge of TCK. It is used to place the Test Access Port controller into various states, as defined in IEEE 1149.1. An internal pull-up holds this lead high during normal operation. This lead has an internal pull-up resistor. |
| $\overline{\text{TRS}}$ | Y6 | I | LVTTL-5p | Test Boundary Scan Reset: An active low signal that asynchronously resets the Test Access Port controller. The reset must be present for a minimum of 50 ns. Specific control of this lead is required in order to ensure normal operation of the device. This lead should be held low whenever boundary scan operations are not being performed. This lead has an internal pull-up resistor. |

TEST

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|------------|----------|-------|-----------------|--|
| SCAN_EN | V15 | I | LVTTTL-5d | Scan Enable: This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low. |
| MBIST_MODE | U5 | I | LVTTTL-5d | Memory Bist: This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low. |
| PLL_BYPASS | V5 | I | LVTTTL-5d | PLL Bypass: This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low. |
| PLLOUT | Y4 | O | LVC MOS 4 mA | PLL Output: This lead is used for TranSwitch Testing purposes only. This lead should be left open (floating). |
| SCAN_MODE | U15 | I | LVTTTL-5d | Scan Mode: This lead is used for TranSwitch Testing purposes only. This lead has an internal pull-down to VSS and should be held low. |

**ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS** (REFERENCED TO VSS)

| Parameter | Symbol | Min | Max | Unit | Conditions |
|--|-------------------|-----------|------------|-------|--------------------------|
| I/O Supply voltage (3.3V) | V _{DD33} | -0.3 | 3.9 | V | Note 1, 4 |
| Core Supply voltage (1.8V) | V _{DD18} | -0.3 | 2.1 | V | Note 1, 4 |
| DC input voltage LVTTTL input voltage LVTTTL-5 input voltage | V _{IN} | 0 -0.5 | 3.3 5.5 | V | Note 1, 4 |
| Storage temperature range | T _S | -55 | +150 | °C | Note 1 |
| Ambient Operating Temperature | T _A | -40 | +85 | °C | 0 ft/min linear airflow |
| Moisture Exposure Level | ME | 5 | | Level | per IPC/JEDEC J-STD-020B |
| Relative Humidity, during assembly | RH | 30 | 60 | % | Note 2 |
| Relative Humidity, in-circuit | RH | 0 | 100 | % | non-condensing |
| ESD Classification | ESD | 2 | | kV | Note 3 |

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114-B.
4. Device core is 1.8 V only. All input signals leads accept 5V signals except for SMII/GMII and SDRAM memory interface signals which accept only 3.3V signals.

THERMAL CHARACTERISTICS

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--|-----|------|-----|------|---|
| Thermal resistance: junction to ambient | | 14.7 | | °C/W | Test performed with package assembled on JEDEC standard Multilayer test board with 0 ft/min linear airflow. |

POWER REQUIREMENTS

GMII MODE (traffic running on one single port)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------------------|------|------|------|------|-----------------|
| V_{DD33} | 3.15 | 3.30 | 3.45 | V | |
| I_{DD33} | 84.8 | 90.9 | 98.7 | mA | Note 1 |
| V_{DD18} | 1.71 | 1.80 | 1.89 | V | |
| I_{DD18} | 840 | 900 | 980 | mA | Note 1 |
| Power Dissipation, $P_{DDTOTAL}$ | 1700 | 1920 | 2203 | mW | Note 2, 3, 4, 6 |
| Power Dissipation, $P_{DDTOTAL5}$ | 1785 | 2016 | 2313 | mW | Note 4, 5 |

SMII MODE (traffic running on one single port)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------------------|------|------|------|------|-----------------|
| V_{DD33} | 3.15 | 3.30 | 3.45 | V | |
| I_{DD33} | 60.0 | 63.5 | 90 | mA | Note 1 |
| V_{DD18} | 1.71 | 1.80 | 1.89 | V | |
| I_{DD18} | 700 | 740 | 860 | mA | Note 1 |
| Power Dissipation, $P_{DDTOTAL}$ | 1379 | 1547 | 1945 | mW | Note 2, 3, 4, 7 |
| Power Dissipation, $P_{DDTOTAL5}$ | 1448 | 1619 | 2043 | mW | Note 4, 5 |

SMII MODE (traffic running on all eight ports)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------------------|------|------|------|------|-----------------|
| V_{DD33} | 3.15 | 3.30 | 3.45 | V | |
| I_{DD33} | 84.6 | 90.7 | 112 | mA | Note 1 |
| V_{DD18} | 1.71 | 1.80 | 1.89 | V | |
| I_{DD18} | 760 | 810 | 870 | mA | Note 1 |
| Power Dissipation, $P_{DDTOTAL}$ | 1559 | 1758 | 2020 | mW | Note 2, 3, 4, 7 |
| Power Dissipation, $P_{DDTOTAL5}$ | 1637 | 1846 | 2122 | mW | Note 4, 5 |

Notes:

1. For I_{DD33} and I_{DD18} , the figure reported represents the absolute minimum and maximum across all the following variations: $1.7 < V_{DD18} < 1.9$ and $3.15 < V_{DD33} < 3.45$ and $-40\text{ }^{\circ}\text{C} < T \text{ (temperature)} < 85\text{ }^{\circ}\text{C}$.
2. For the total power, the maximum consumption occurs when both V_{DD33} and V_{DD18} are at their maximum test value. The minimum consumption occurs when both V_{DD33} and V_{DD18} are at their minimum test value. Very small effect of temperature on the power consumption has been observed.
3. The figure for Typical power was measured at $V_{DD33} = 3.3\text{ V}$ and $V_{DD18} = 1.8\text{ V}$.
4. The Max and Min values of power have been rounded to the nearest higher 0.01 W.
5. $P_{DDTOTAL5}$ represent the $P_{DDTOTAL}$ value reported on the above, line plus 5% to cover the process and temperature variations that may exist.
6. Measurement taken with traffic injected at 1 Gbps, with flow control enabled. Packet size was 64 bytes.
7. Measurement taken with traffic injected at 100 Mbps, with flow control enabled. Packet size was 1514 bytes.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR LVTTTL-5 (5 VOLT TOLERANT)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|-----|-----|----------------|---------|--|
| V_{IH} | 2.0 | | 5.0 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| V_{IL} | | | 0.8 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| Input leakage current | | | $\pm 15 \mu A$ | μA | $V_{DD33} = 3.45$, $V_{in} = V_{DD}$ or GND |
| Input capacitance | | 5 | | pF | |

INPUT PARAMETERS FOR LVTTTL-5p (5 VOLT TOLERANT, with PULL-UP RESISTOR)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|-----|-----|-----|---------|-------------------------------------|
| V_{IH} | 2.0 | | 5.0 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| V_{IL} | | | 0.8 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| Input leakage current | 28 | | 105 | μA | $V_{DD33} = 3.45$; Input = 0 volts |
| Input capacitance | | 5 | | pF | |

INPUT PARAMETERS FOR LVTTTL-5d (5 VOLT TOLERANT, with PULL-DOWN RESISTOR)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|-----|-----|-----|---------|--|
| V_{IH} | 2.0 | | 5.0 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| V_{IL} | | | 0.8 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| Input leakage current | 28 | | 105 | μA | $V_{DD33} = 3.45$; Input = 3.45 volts |
| Input capacitance | | 5 | | pF | |

INPUT PARAMETERS FOR LVTTTL (3.3 VOLT TOLERANT)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|-----|-----|----------|---------|--|
| V_{IH} | 2.0 | | | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| V_{IL} | | | 0.8 | V | $3.15 \leq V_{DD33} \leq 3.45$ |
| Input leakage current | | | ± 15 | μA | $V_{DD33} = 3.45$, $V_{in} = V_{DD}$ or GND |
| Input capacitance | | 5 | | pF | |

OUTPUT PARAMETERS FOR LVCMOS 24mA (Open Drain)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|---|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -24 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 24 |
| I _{OL} | | 24 | | mA | |
| I _{OH} | | -24 | | mA | |
| t _{RISE} | 1.17 | | 2.25 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 0.87 | | 1.77 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD33}.

OUTPUT PARAMETERS FOR LVCMOS 12mA

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|---|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -12 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 12 |
| I _{OL} | | 12 | | mA | |
| I _{OH} | | -12 | | mA | |
| t _{RISE} | 1.43 | | 2.71 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.22 | | 2.45 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

OUTPUT PARAMETERS FOR LVCMOS 8mA

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|--|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -8 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 8 |
| I _{OL} | | 8 | | mA | |
| I _{OH} | | -8 | | mA | |
| t _{RISE} | 1.78 | | 3.38 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.65 | | 3.22 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

OUTPUT PARAMETERS FOR LVCMOS 4mA

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|--|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -4 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 4 |
| I _{OL} | | 4 | | mA | |
| I _{OH} | | -4 | | mA | |
| t _{RISE} | 2.97 | | 5.54 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 2.95 | | 5.66 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

OUTPUT PARAMETERS FOR LV3CMOS 16mA (do not use pull-ups to more than 3.3V with these outputs)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|---|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -16 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 16 |
| I _{OL} | | 16 | | mA | |
| I _{OH} | | -16 | | mA | |
| t _{RISE} | 1.28 | | 2.87 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.04 | | 2.65 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

OUTPUT PARAMETERS FOR LV3CMOS 8mA (do not use pull-ups to more than 3.3V with these outputs)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--------------------|------|-----|------|------|--|
| Output capacitance | | 30 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -8 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 8 |
| I _{OL} | | 8 | | mA | |
| I _{OH} | | -8 | | mA | |
| t _{RISE} | 1.78 | | 3.41 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.65 | | 3.38 | ns | C _{LOAD} = 30 pF |
| Leakage tristate | | | ±15 | µA | 0 to 3 V input |

INPUT/OUTPUT PARAMETERS FOR LVTTTL-5 INPUT AND LVCMOS OUTPUT 12mA
(5 VOLT TOLERANT Input)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|------|-----|------|------|---|
| V _{IH} | 2.0 | | | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| V _{IL} | | | 0.8 | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| Input leakage current | | | ±15 | μA | 0 to 3.3 V input |
| Input capacitance | | 5 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -12 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 12 |
| I _{OL} | | 12 | | mA | |
| I _{OH} | | -12 | | mA | |
| t _{RISE} | 1.44 | | 2.72 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.23 | | 2.45 | ns | C _{LOAD} = 30 pF |

INPUT/OUTPUT PARAMETERS FOR LVTTTL-5 INPUT AND LVCMOS OUTPUT 8mA
(5 VOLT TOLERANT Input)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|------|-----|------|------|--|
| V _{IH} | 2.0 | | | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| V _{IL} | | | 0.8 | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| Input leakage current | | | ±15 | μA | 0 to 3.3 V input |
| Input capacitance | | 5 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -8 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 8 |
| I _{OL} | | 8 | | mA | |
| I _{OH} | | -8 | | mA | |
| t _{RISE} | 1.79 | | 3.40 | ns | C _{LOAD} = 30 pF |
| t _{FALL} | 1.67 | | 3.24 | ns | C _{LOAD} = 30 pF |



**INPUT/OUTPUT PARAMETERS FOR LVTTTL INPUT AND LV3CMOS OUTPUT 16mA
(3.3V VOLT TOLERANT Input)**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|------|-----|------|------|---|
| V _{IH} | 2.0 | | | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| V _{IL} | | | 0.8 | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| Input leakage current | | | ±15 | µA | 0 to 3.3 V input |
| Input capacitance | | 5 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -16 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 16 |
| I _{OL} | | 16 | | mA | |
| I _{OH} | | -16 | | mA | |
| t _{RISE} | 1.76 | | 2.85 | ns | C _{LOAD} = 25 pF |
| t _{FALL} | 1.60 | | 2.64 | ns | C _{LOAD} = 25 pF |

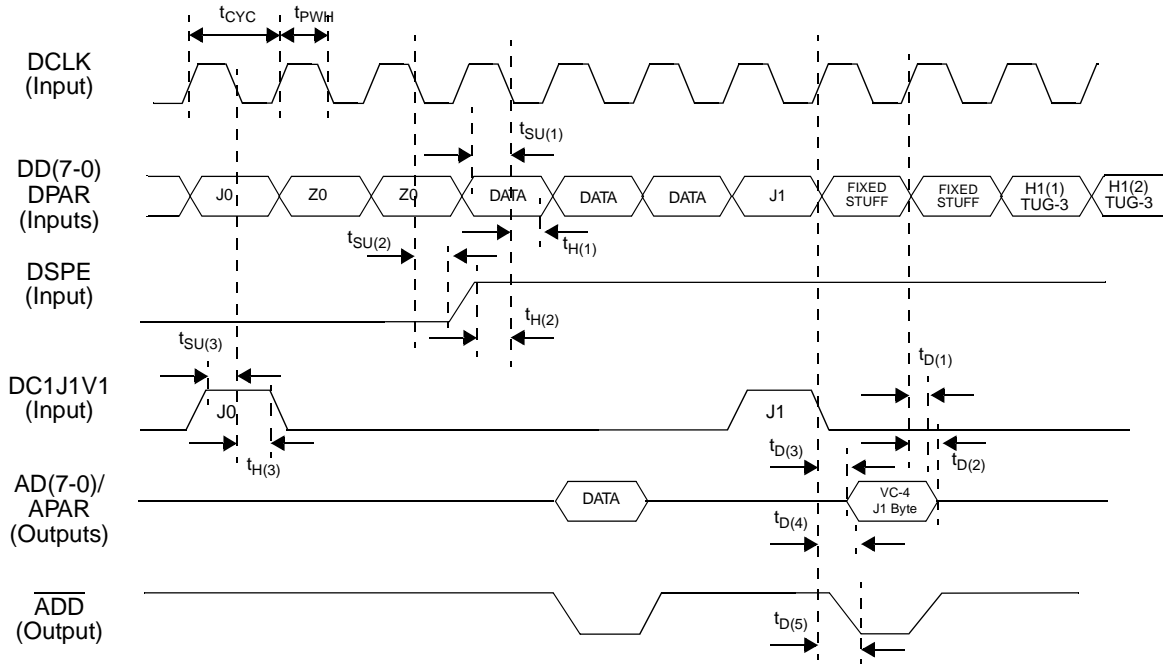
**INPUT/OUTPUT PARAMETERS FOR LVTTTL INPUT AND LV3CMOS OUTPUT 8mA
(3.3V VOLT TOLERANT Input)**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------------------|------|-----|------|------|--|
| V _{IH} | 2.0 | | | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| V _{IL} | | | 0.8 | V | 3.15 ≤ V _{DD33} ≤ 3.45 |
| Input leakage current | | | ±15 | µA | 0 to 3.3 V input |
| Input capacitance | | 5 | | pF | |
| V _{OH} | 2.4 | | | V | V _{DD33} = 3.15; I _{OH} = -8 |
| V _{OL} | | | 0.4 | V | V _{DD33} = 3.15; I _{OL} = 8 |
| I _{OL} | | 8 | | mA | |
| I _{OH} | | -8 | | mA | |
| t _{RISE} | 1.80 | | 3.39 | ns | C _{LOAD} = 25 pF |
| t _{FALL} | 1.78 | | 3.36 | ns | C _{LOAD} = 25 pF |

TIMING CHARACTERISTICS

This section presents the detailed timing characteristics for the EtherMap-3 Plus in Figures 8 through 38 with values of the timing parameters tabulated below each waveform diagram. All outputs are measured with a maximum load capacitance of 50 pF unless otherwise stated. Timing parameters are measured at the voltage levels of $(V_{OH} + V_{OL})/2$ for output signals and $(V_{IH} + V_{IL})/2$ for input signals.

Figure 8. Drop Bus Timing (Only AD, APAR, and ADD are Output)



50 pF Load

Notes:

1. STM-1 mode with TUG-3 mapping is shown (TUG-3 #A selected).
2. If STS-3 mode was used there would be three J1 pulses that would be asynchronous with respect to each other. However the timing (i.e., setup and hold, and propagation delays) would not change.
3. Transmit TimingDelay = 1 (see register 0x184c8).

See parameter table on next page.



DATA SHEET

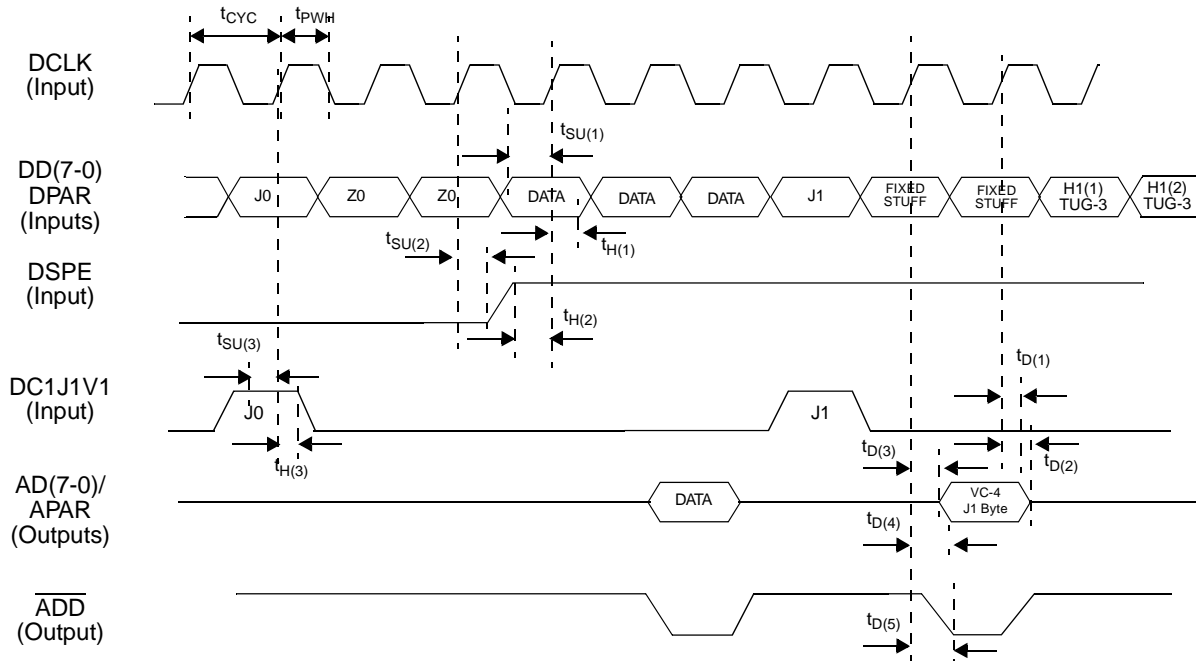
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------------|-------------|-----|-------|-----|------|
| DCLK clock period | t_{CYC} | | 51.44 | | ns |
| DCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| DD(7-0)/DPAR setup time to DCLK↓ | $t_{SU(1)}$ | 5 | | | ns |
| DD(7-0)/DPAR hold time after DCLK↓ | $t_{H(1)}$ | 0 | | | ns |
| DSPE setup time to DCLK↓ | $t_{SU(2)}$ | 6 | | | ns |
| DSPE hold time after DCLK↓ | $t_{H(2)}$ | 0 | | | ns |
| DC1J1V1 setup time to DCLK↓ | $t_{SU(3)}$ | 6 | | | ns |
| DC1J1V1 hold time after DCLK↓ | $t_{H(3)}$ | 0 | | | ns |
| AD(7-0)/APAR stable from DCLK↑ | $t_{D(1)}$ | 7 | | 30 | ns |
| AD(7-0)/APAR tristated from DCLK↑ | $t_{D(2)}$ | 8 | | 20 | ns |
| AD(7-0)/APAR turn on from DCLK↑ | $t_{D(3)}$ | 2.5 | | 20 | ns |
| AD(7-0)/APAR valid from DCLK↑ | $t_{D(4)}$ | 5 | | 30 | ns |
| ADD delay after DCLK↑ | $t_{D(5)}$ | 5 | | 30 | ns |

Note:

- The inputs DD(7-0)/DPAR, DC1J1V1 and DSPE are sampled on the falling edge of DCLK according to the setting of configuration bit Active Edge (see [Table 281](#), on [page 347](#)).

Figure 9. Drop Bus Timing (Only AD, APAR, and ADD are Output)



50 pF Load

Notes:

1. STM-1 mode with TUG-3 mapping is shown (TUG-3 #A selected).
2. If STS-3 mode was used there would be three J1 pulses that would be asynchronous with respect to each other. However the timing (i.e., setup and hold, and propagation delays) would not change.
3. Transmit TimingDelay = 1 (see register [0x184c8](#)).

See parameter table on next page.



DATA SHEET

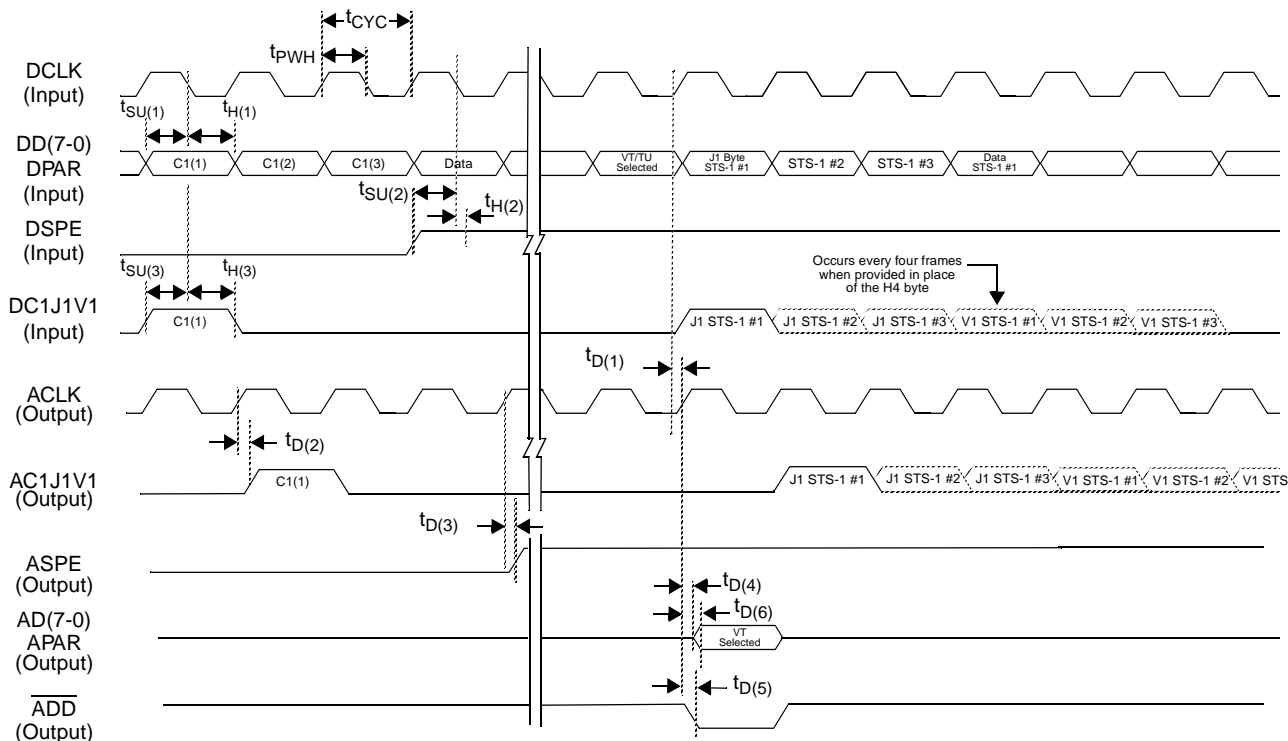
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|-------|-----|------|
| DCLK clock period | t_{CYC} | | 51.44 | | ns |
| DCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| DD(7-0)/DPAR setup time to DCLK \uparrow | $t_{SU(1)}$ | 5 | | | ns |
| DD(7-0)/DPAR hold time after DCLK \uparrow | $t_{H(1)}$ | 2 | | | ns |
| DSPE setup time to DCLK \uparrow | $t_{SU(2)}$ | 10 | | | ns |
| DSPE hold time after DCLK \uparrow | $t_{H(2)}$ | 5 | | | ns |
| DC1J1V1 setup time to DCLK \uparrow | $t_{SU(3)}$ | 10 | | | ns |
| DC1J1V1 hold time after DCLK \uparrow | $t_{H(3)}$ | 5 | | | ns |
| AD(7-0)/APAR stable from DCLK \uparrow | $t_{D(1)}$ | 7 | | 30 | ns |
| AD(7-0)/APAR tristated from DCLK \uparrow | $t_{D(2)}$ | 8 | | 20 | ns |
| AD(7-0)/APAR turn on from DCLK \uparrow | $t_{D(3)}$ | 2.5 | | 20 | ns |
| AD(7-0)/APAR valid from DCLK \uparrow | $t_{D(4)}$ | 5 | | 30 | ns |
| \overline{ADD} delay after DCLK \uparrow | $t_{D(5)}$ | 5 | | 30 | ns |

Note:

- The inputs DD(7-0)/DPAR, DC1J1V1 and DSPE are sampled on the rising edge of DCLK according to the setting of configuration bit Active Edge (see [Table 281](#), on [page 347](#)).

Figure 10. Drop Bus Timing (all ADD Bus Signals are Outputs)



50 pF Load

Notes:

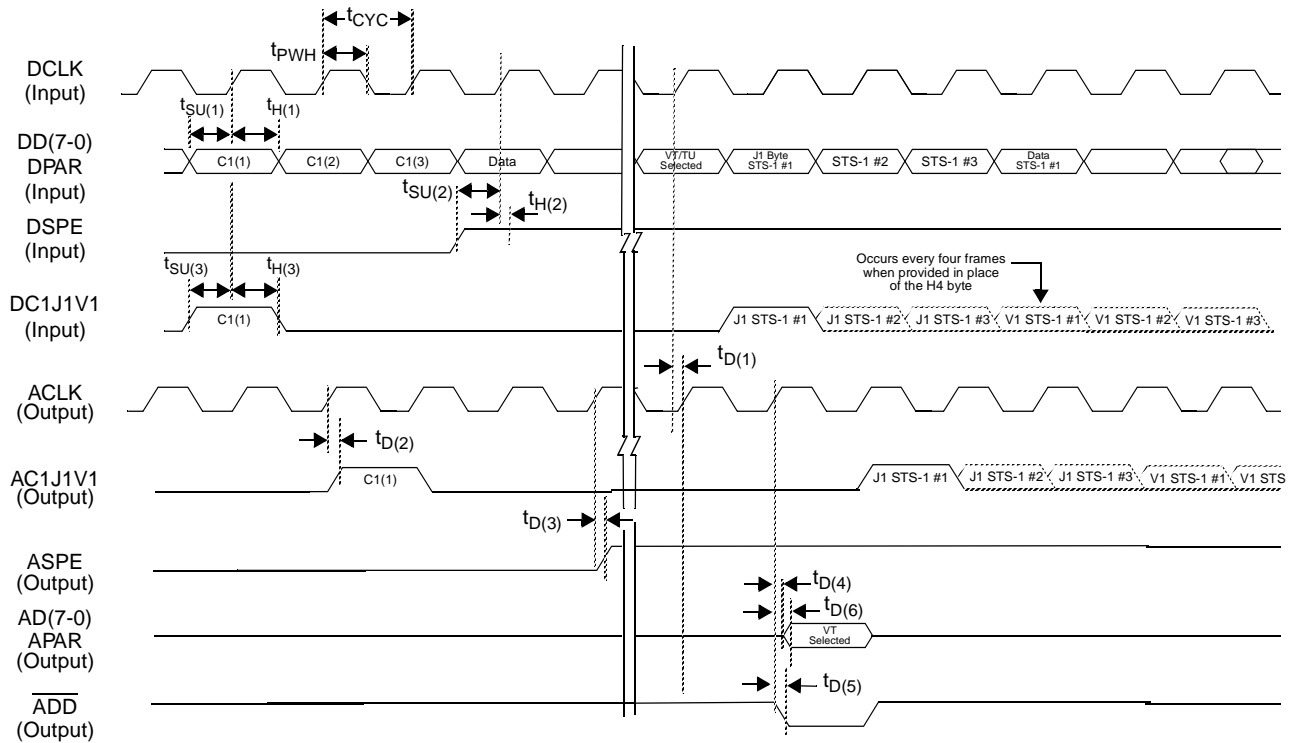
1. A single VT/TU is shown for illustration purposes (last VT of STS-1 #3 selected).
2. STS-3 mode is shown. If STM-1 mode was used there would be one J1 pulse and three TUG-3s, or three J1 pulses and three AU-3s. However the timing (i.e., setup and hold, and propagation delays) would not change.
3. Transmit TimingDelay = 1 (see register 0x184c8).

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------|-----|-------|-----|------|
| DCLK clock period | t_{CYC} | | 51.44 | | ns |
| DCLK duty cycle t_{PWH}/t_{CYC} | | 40 | 50 | 60 | % |
| DD(7-0)/DPAR setup time before DCLK↓ | $t_{SU(1)}$ | 5 | | | ns |
| DD(7-0)/DPAR hold time after DCLK↓ | $t_{H(1)}$ | 0 | | | ns |
| DSPE setup time before DCLK↓ | $t_{SU(2)}$ | 6 | | | ns |
| DSPE hold time after DCLK↓ | $t_{H(2)}$ | 0 | | | ns |
| DC1J1V1 setup time before DCLK↓ | $t_{SU(3)}$ | 6 | | | ns |
| DC1J1V1 hold time after DCLK↓ | $t_{H(3)}$ | 0 | | | ns |
| ACLK ↑ delay from DCLK↑ | $t_{D(1)}$ | 2 | | 10 | ns |
| AC1J1V1 delay from ACLK↑ | $t_{D(2)}$ | 3 | | 30 | ns |
| ASPE delay from ACLK↑ | $t_{D(3)}$ | 3 | | 30 | ns |
| AD(7-0)/APAR turn on from ACLK↑ | $t_{D(4)}$ | 3 | | 30 | ns |
| ADD delay from ACLK↑ | $t_{D(5)}$ | 3 | | 30 | ns |
| AD(7-0)/APAR out valid delay from ACLK↑ | $t_{D(6)}$ | 3 | | 30 | ns |

Note:

1. The inputs DD(7-0)/DPAR, DC1J1V1 and DSPE are sampled on the falling edge of DCLK according to the setting of configuration bit Active Edge (see Table 281, on page 347).

Figure 11. Drop Bus Timing (all ADD Bus Signals are Outputs)



50 pF Load

Notes:

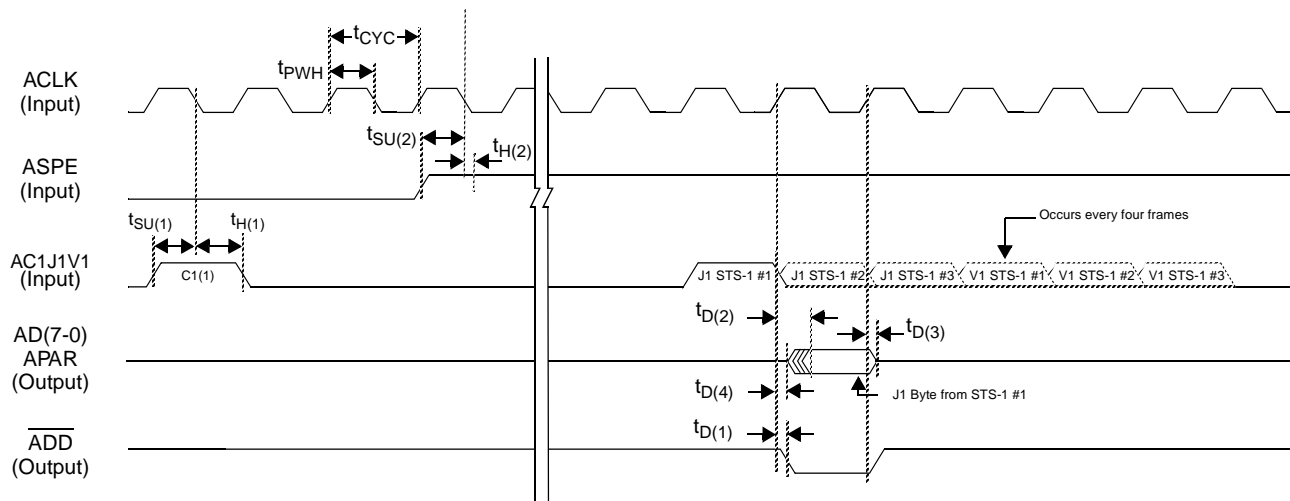
1. A single VT/TU is shown for illustration purposes (last VT/TU of STS-1/VC-3 #3 selected).
2. STS-3 mode is shown. If STM-1 mode was used there would be one J1 pulse and three TUG-3s, or three J1 pulses and three AU-3s. However the timing (i.e., setup and hold, and propagation delays) would not change.
3. Transmit TimingDelay = 1 (see register 0x184c8).

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------|-----|-------|-----|------|
| DCLK clock period | t_{CYC} | | 51.44 | | ns |
| DCLK duty cycle t_{PWH}/t_{CYC} | | 40 | 50 | 60 | % |
| DD(7-0)/DPAR setup time before DCLK \uparrow | $t_{SU(1)}$ | 5 | | | ns |
| DD(7-0)/DPAR hold time after DCLK \uparrow | $t_{H(1)}$ | 2 | | | ns |
| DSPE setup time before DCLK \uparrow | $t_{SU(2)}$ | 10 | | | ns |
| DSPE hold time after DCLK \uparrow | $t_{H(2)}$ | 5 | | | ns |
| DC1J1V1 setup time before DCLK \uparrow | $t_{SU(3)}$ | 10 | | | ns |
| DC1J1V1 hold time after DCLK \uparrow | $t_{H(3)}$ | 5 | | | ns |
| ACLK \uparrow delay from DCLK \uparrow | $t_{D(1)}$ | 2 | | 10 | ns |
| AC1J1V1 delay from ACLK \uparrow | $t_{D(2)}$ | 3 | | 30 | ns |
| ASPE delay from ACLK \uparrow | $t_{D(3)}$ | 3 | | 30 | ns |
| AD(7-0)/APAR turn on from ACLK \uparrow | $t_{D(4)}$ | 3 | | 30 | ns |
| ADD delay from ACLK \uparrow | $t_{D(5)}$ | 3 | | 30 | ns |
| AD(7-0)/APAR out valid delay from ACLK \uparrow | $t_{D(6)}$ | 3 | | 30 | ns |

Note:

1. The inputs DD(7-0)/DPAR, DC1J1V1 and DSPE are sampled on the rising edge of DCLK according to the setting of configuration bit Active Edge (see Table 281, on page 347).

Figure 12. ADD Bus Timing (Timing Signals are Inputs)



50 pF Load

Notes:

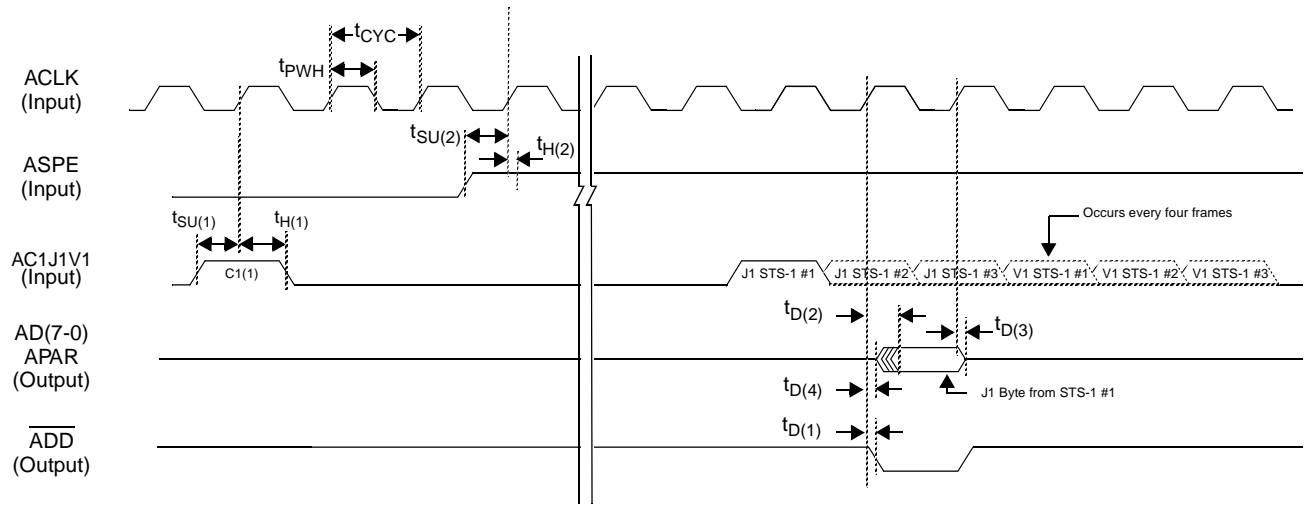
1. A single tributary is shown for illustration purposes (STS-1 #1).
2. A delay of '1' clock cycle is shown (selected in register 0x184c8).
3. STS-3 mode is shown. If STM-1 mode was used there would be one J1 pulse and three TUG-3s, or three J1 pulses and three AU-3s. However the timing (i.e., setup and hold, and propagation delays) would not change.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|-------|-----|------|
| ACLK clock period | t_{CYC} | | 51.44 | | ns |
| ACLK duty cycle, t_{PWH}/t_{CYC} | | 40 | 50 | 60 | % |
| AC1J1V1 setup time before ACLK↓ | $t_{SU(1)}$ | 5 | | | ns |
| AC1J1V1 hold time after ACLK↓ | $t_{H(1)}$ | 0 | | | ns |
| ASPE setup time before ACLK↓ | $t_{SU(2)}$ | 5 | | | ns |
| ASPE hold time after ACLK↓ | $t_{H(2)}$ | 0 | | | ns |
| AD(7-0)/APAR out valid delay from ACLK↑ | $t_{D(2)}$ | 5 | | 30 | ns |
| AD(7-0)/APAR to tristate delay from ACLK↑ | $t_{D(3)}$ | 5 | | 30 | ns |
| \overline{ADD} add indicator delayed from ACLK↑ | $t_{D(1)}$ | 5 | | 30 | ns |
| AD(7-0)/APAR out tristate to driven delay from ACLK↑ | $t_{D(4)}$ | 2.5 | | 30 | ns |

Note:

1. The inputs AC1J1V1 and ASPE are sampled on the falling edge of ACLK according to the setting of configuration bit Active Edge (see Table 281, on page 347).

Figure 13. ADD Bus Timing (Timing Signals are Inputs)



50 pF Load

Notes:

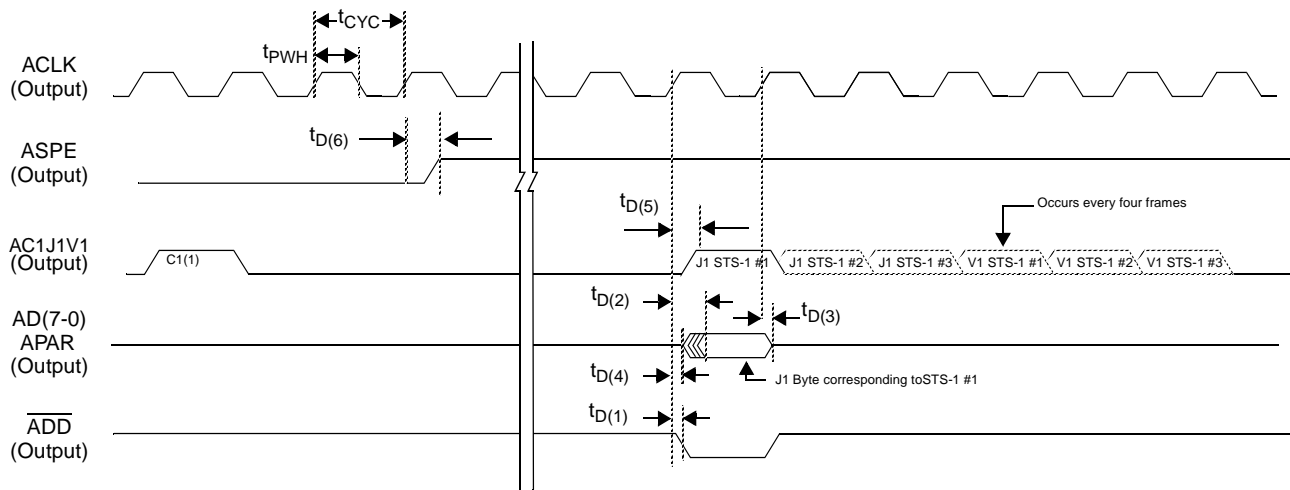
1. A single tributary is shown for illustration purposes (STS-1 #1).
2. A delay of '1' clock cycle is shown (selected in register 0x184c8).
3. STS-3 mode is shown. If STM-1 mode was used there would be one J1 pulse and three TUG-3s, or three J1 pulses and three AU-3s. However the timing (i.e., setup and hold, and propagation delays) would not change.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|-------|-----|------|
| ACLK clock period | t_{CYC} | | 51.44 | | ns |
| ACLK duty cycle, t_{PWH}/t_{CYC} | | 40 | 50 | 60 | % |
| AC1J1V1 setup time before ACLK \uparrow | $t_{SU(1)}$ | 15 | | | ns |
| AC1J1V1 hold time after ACLK \uparrow | $t_{H(1)}$ | 1 | | | ns |
| ASPE setup time before ACLK \uparrow | $t_{SU(2)}$ | 15 | | | ns |
| ASPE hold time after ACLK \uparrow | $t_{H(2)}$ | 1 | | | ns |
| AD(7-0)/APAR out valid delay from ACLK \uparrow | $t_{D(2)}$ | 5 | | 30 | ns |
| AD(7-0)/APAR to tristate delay from ACLK \uparrow | $t_{D(3)}$ | 5 | | 30 | ns |
| \overline{ADD} add indicator delayed from ACLK \uparrow | $t_{D(1)}$ | 5 | | 30 | ns |
| AD(7-0)/APAR out tristate to driven delay from ACLK \uparrow | $t_{D(4)}$ | 2.5 | | 30 | ns |

Note:

1. The inputs AC1J1V1 and ASPE are sampled on the rising edge of ACLK according to the setting of configuration bit Active Edge (see Table 281, on page 347).

Figure 14. ADD Bus Timing (Timing Signals are Outputs)



50 pF Load

Notes:

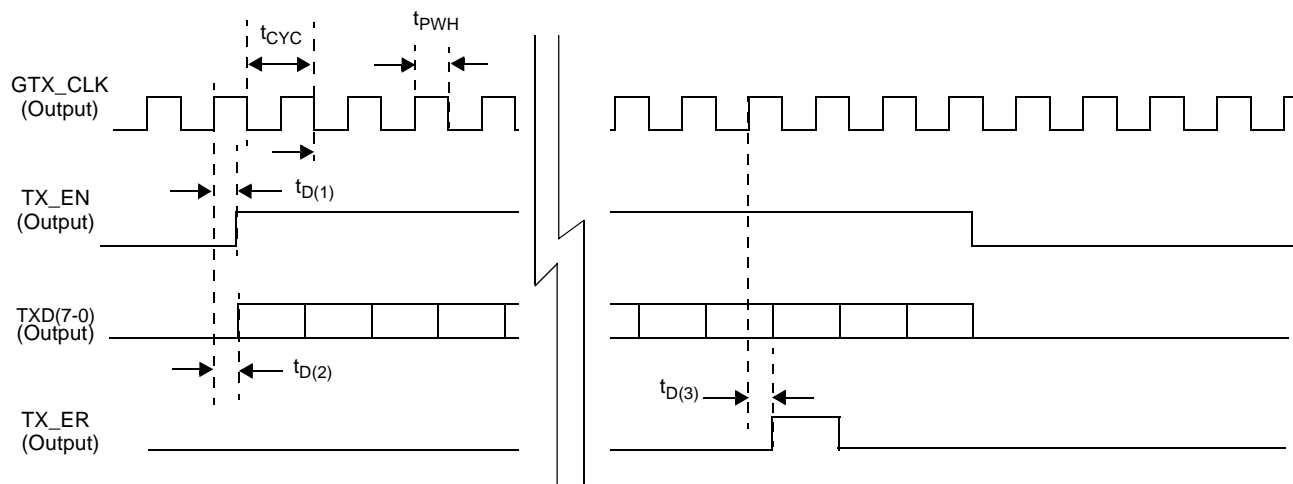
1. A single tributary is shown for illustration purposes (STS-1 #1).
2. A delay of '0' clock cycle is shown (selected in register [0x184c8](#)).
3. STS-3 mode is shown. If STM-1 mode was used there would be one J1 pulse and three TUG-3s, or three J1 pulses and three AU-3s. However the timing (i.e., setup and hold, and propagation delays) would not change.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-------|-----|------|
| ACLK clock period | t_{CYC} | | 51.44 | | ns |
| ACLK duty cycle, t_{PWH}/t_{CYC} | | 40 | 50 | 60 | % |
| AC1J1V1 out valid delay from ACLK \uparrow | $t_{D(5)}$ | 4 | | 30 | ns |
| ASPE out valid delay from ACLK \uparrow | $t_{D(6)}$ | 4 | | 30 | ns |
| AD(7-0)/APAR out valid delay from ACLK \uparrow | $t_{D(2)}$ | 4 | | 30 | ns |
| AD(7-0)/APAR to tristate delay from ACLK \uparrow | $t_{D(3)}$ | 3.5 | | 30 | ns |
| ADD add indicator delayed from ACLK \uparrow | $t_{D(1)}$ | 5 | | 30 | ns |
| AD(7-0)/APAR out tristate to driven delay from ACLK \uparrow | $t_{D(4)}$ | 3 | | 20 | ns |

Note:

1. ACLK is derived from RTCLK input (lead A3) and should be a SONET/SDH clock of +/- 20 ppm or better.

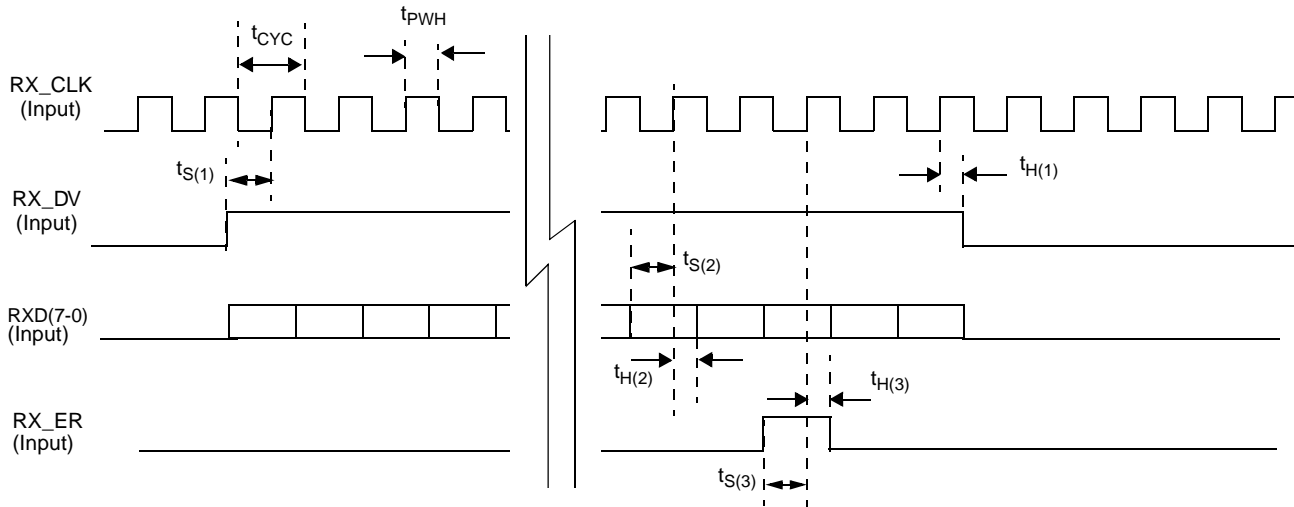
Figure 15. Tx GMII Ethernet Interface



5 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| GTX_CLK clock period | t_{CYC} | | 8 | | ns |
| GTX_CLK duty cycle, t_{PWH}/t_{CYC} | | 40 | | 60 | % |
| TX_EN out valid delay from GTX_CLK \uparrow | $t_{D(1)}$ | 1.4 | | 4.5 | ns |
| TXD(7-0) out valid delay from GTX_CLK \uparrow | $t_{D(2)}$ | 1.4 | | 4.5 | ns |
| TX_ER out valid delay from GTX_CLK \uparrow | $t_{D(3)}$ | 1.4 | | 4.5 | ns |

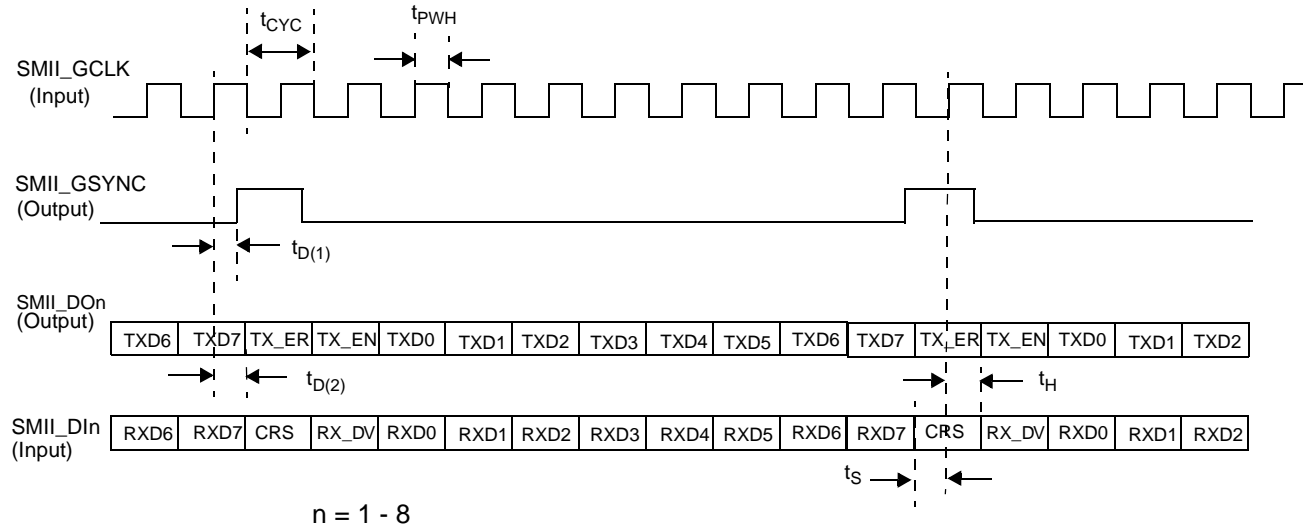
Figure 16. Rx GMII Ethernet Interface



10 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| RX_CLK clock period | t_{CYC} | | 8 | | ns |
| RX_CLK duty cycle, t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| RX_DV setup time before RX_CLK \uparrow | $t_{S(1)}$ | 2 | | | ns |
| RX_DV hold time after RX_CLK \uparrow | $t_{H(1)}$ | 0 | | | ns |
| RXD(7-0) setup time before RX_CLK \uparrow | $t_{S(2)}$ | 2 | | | ns |
| RXD(7-0) hold time after RX_CLK \uparrow | $t_{H(2)}$ | 0 | | | ns |
| RX_ER setup time before RX_CLK \uparrow | $t_{S(3)}$ | 2 | | | ns |
| RX_ER hold time after RX_CLK \uparrow | $t_{H(3)}$ | 0 | | | ns |

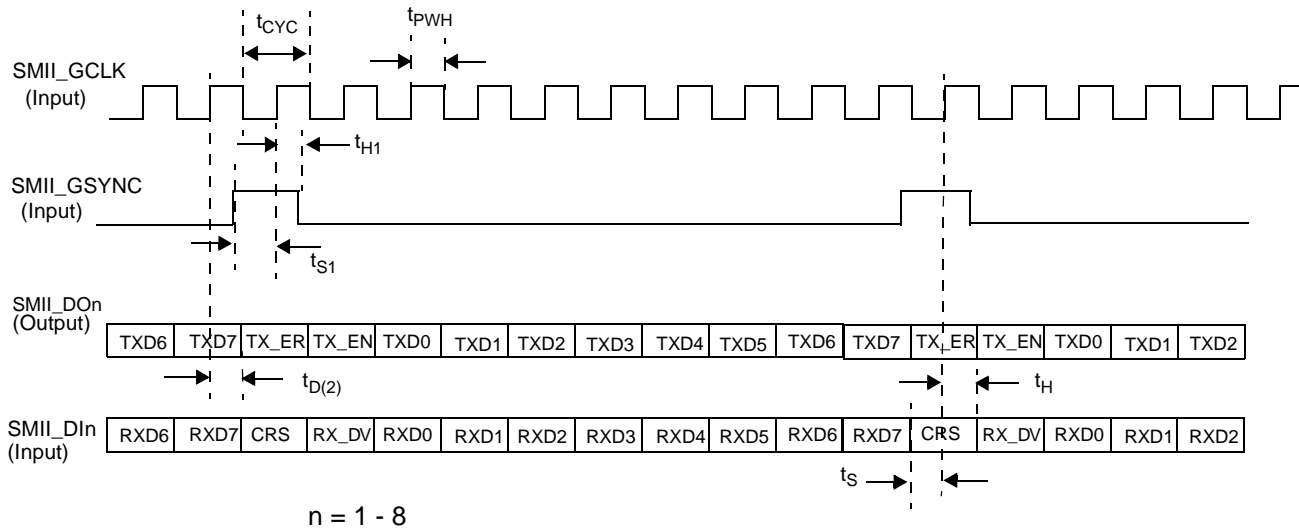
Figure 17. Tx/Rx SMII Ethernet Interface (SYNC as an Output)



10 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| SMII_GCLK clock period | t_{CYC} | | 8 | | ns |
| SMII_GCLK duty cycle, t_{PWH}/t_{CYC} | | 40 | | 60 | % |
| SMII_GSYNC out valid delay from SMII_GCLK \uparrow | $t_{D(1)}$ | 1.5 | | 4.5 | ns |
| SMII_DOn out valid delay from SMII_GCLK \uparrow | $t_{D(2)}$ | 1.5 | | 4.5 | ns |
| SMII_DIn setup time before SMII_GCLK \uparrow | t_S | 2.0 | | | ns |
| SMII_DIn hold time after SMII_GCLK \uparrow | t_H | 1 | | | ns |

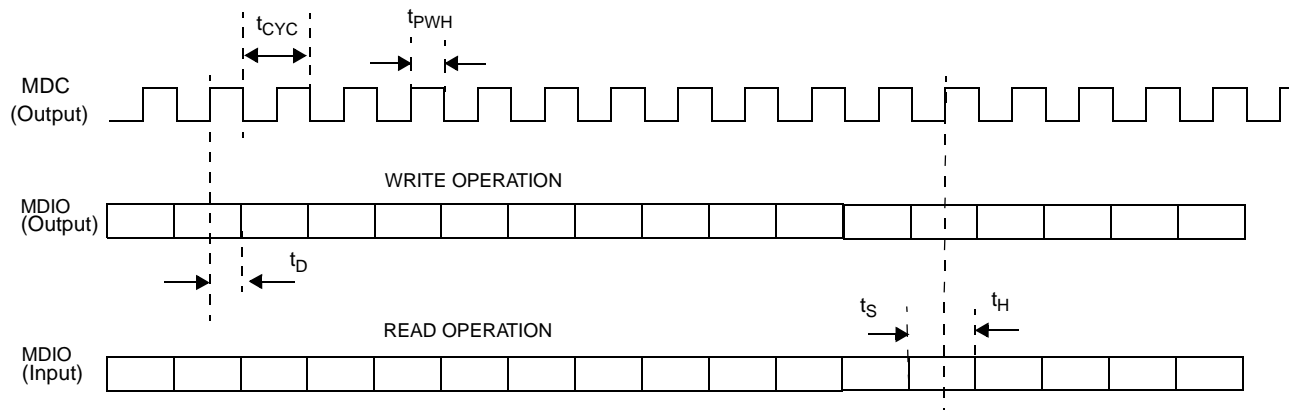
Figure 18. Tx/Rx SMII Ethernet Interface (SYNC as an Input)



10 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| SMII_GCLK clock period | t_{CYC} | | 8 | | ns |
| SMII_GCLK duty cycle, t_{PWH}/t_{CYC} | | 40 | | 60 | % |
| SMII_GSYNC setup time before SMII_GCLK \uparrow | t_{S1} | 2.0 | | | ns |
| SMII_GSYNC hold time after SMII_GCLK \uparrow | t_{H1} | 1 | | | |
| SMII_DOn out valid delay from SMII_GCLK \uparrow | $t_{D(2)}$ | 1.5 | | 4.5 | ns |
| SMII_DIn setup time before SMII_GCLK \uparrow | t_S | 2.0 | | | ns |
| SMII_DIn hold time after SMII_GCLK \uparrow | t_H | 1 | | | ns |

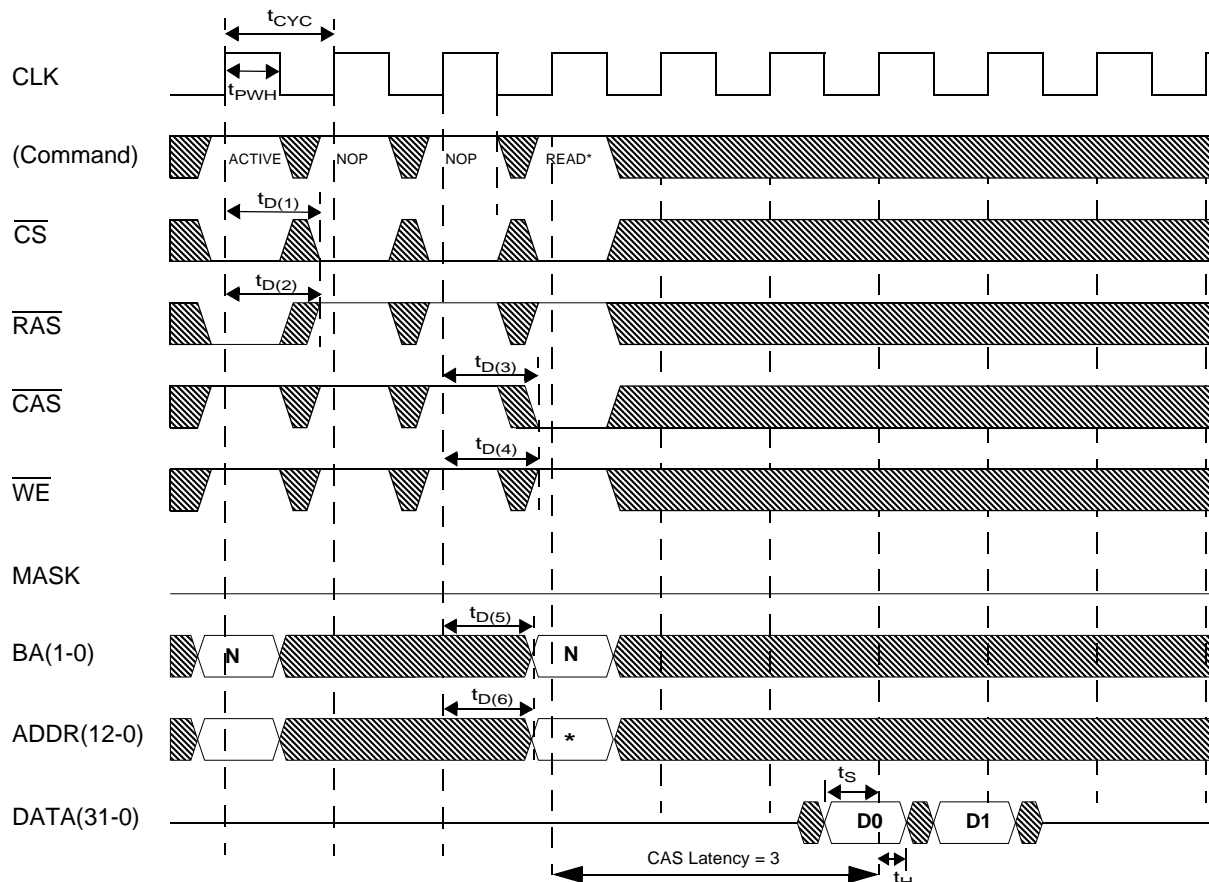
Figure 19. Ethernet Management Interface



10 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|-----|-----|------|
| MDC clock period | t_{CYC} | | 160 | | ns |
| MDC pulse width | t_{PWH} | | 80 | | ns |
| MDIO out valid delay from MDC \uparrow | t_D | 10 | | 50 | ns |
| MDIO setup time before MDC \uparrow | t_S | 10 | | | ns |
| MDIO hold time after MDC \uparrow | t_H | 5 | | | ns |

Figure 20. SDRAM Interface - Single Word Read

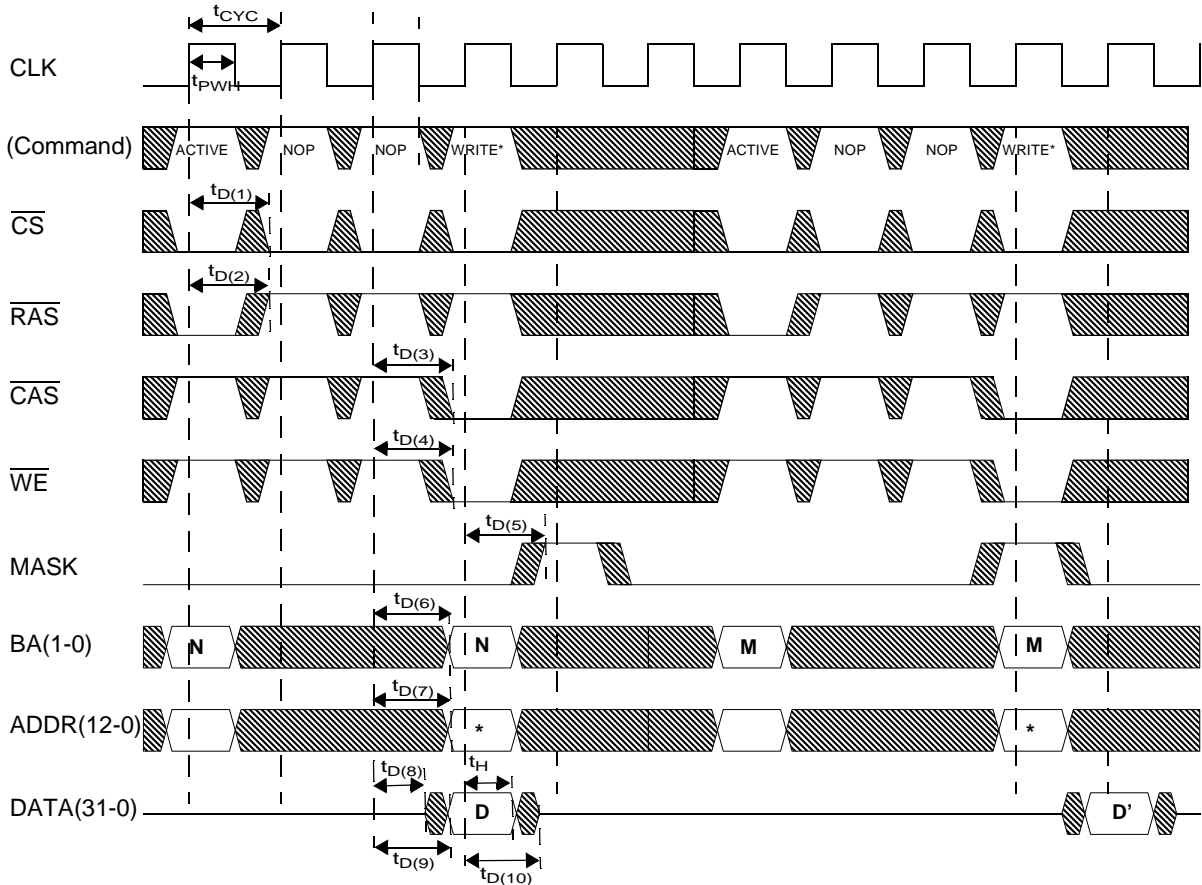


Note*: All read commands enable the auto precharge feature with ADDR(10)=1

30 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|-----|-----|------|
| CLK clock period | t_{CYC} | | 10 | | ns |
| CLK duty cycle, t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| \overline{CS} valid delay from $CLK\uparrow$ | $t_{D(1)}$ | 2.9 | | 7 | ns |
| \overline{RAS} valid delay from $CLK\uparrow$ | $t_{D(2)}$ | 2.9 | | 7 | ns |
| \overline{CAS} valid delay from $CLK\uparrow$ | $t_{D(3)}$ | 2.9 | | 7 | ns |
| \overline{WE} valid delay from $CLK\uparrow$ | $t_{D(4)}$ | 2.9 | | 7 | ns |
| BA(1-0) valid delay from $CLK\uparrow$ | $t_{D(5)}$ | 2.9 | | 7 | ns |
| ADDR(12-0) valid delay from $CLK\uparrow$ | $t_{D(6)}$ | 2.9 | | 7 | ns |
| DATA(31-0) setup time to $CLK\uparrow$ | t_S | 2.5 | | | ns |
| DATA(31-0) hold time from $CLK\uparrow$ | t_H | 1 | | | ns |

Figure 21. SDRAM Interface - Single Word Write

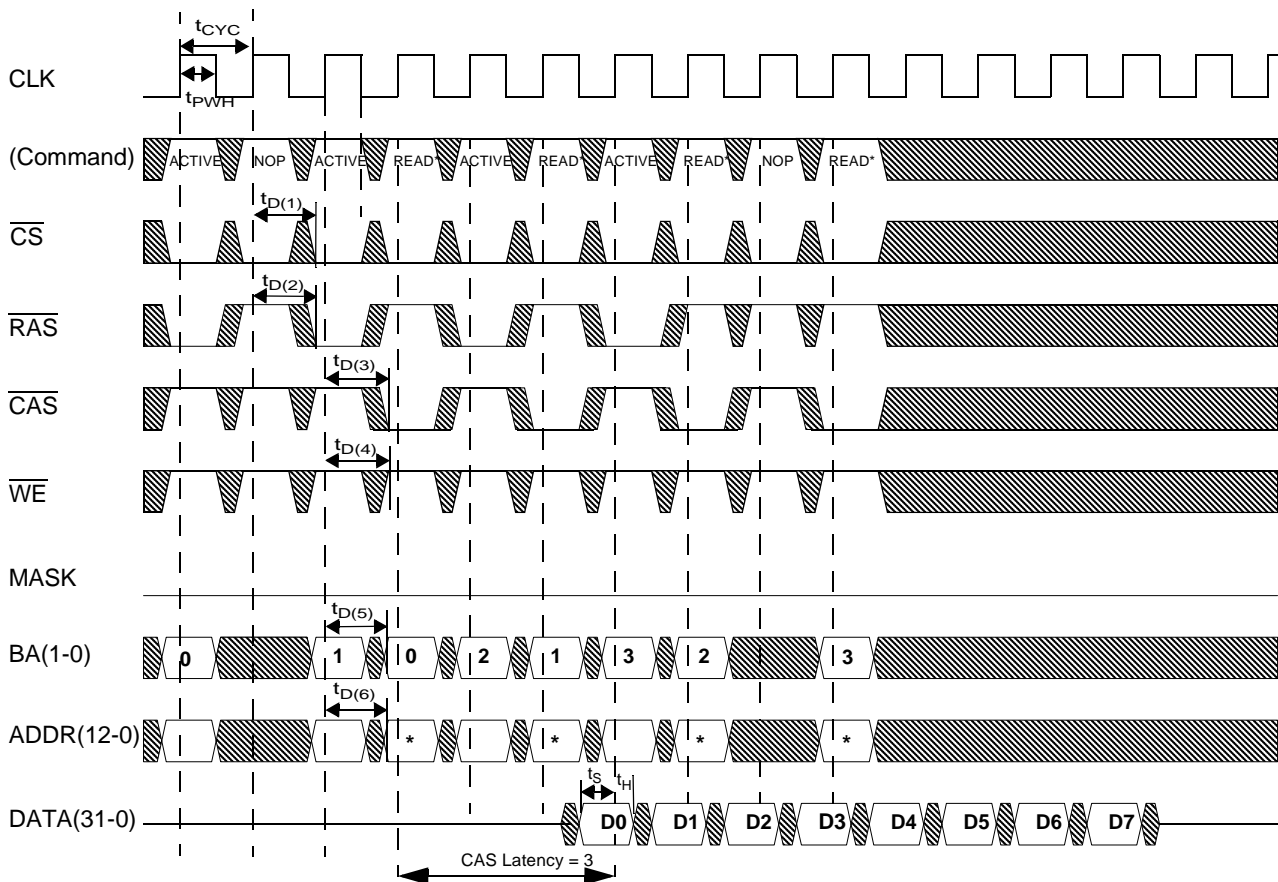


Note*: All write commands enable the auto precharge feature with ADDR(10)=1

30 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|-----|-----|------|
| CLK clock period | t_{CYC} | | 10 | | ns |
| CLK duty cycle, t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| \overline{CS} valid delay from $CLK\uparrow$ | $t_{D(1)}$ | 2.9 | | 7 | ns |
| \overline{RAS} valid delay from $CLK\uparrow$ | $t_{D(2)}$ | 2.9 | | 7 | ns |
| \overline{CAS} valid delay from $CLK\uparrow$ | $t_{D(3)}$ | 2.9 | | 7 | ns |
| \overline{WE} valid delay from $CLK\uparrow$ | $t_{D(4)}$ | 2.9 | | 7 | ns |
| MASK valid delay from $CLK\uparrow$ | $t_{D(5)}$ | 2.9 | | 7 | ns |
| BA(1-0) valid delay from $CLK\uparrow$ | $t_{D(6)}$ | 2.9 | | 7 | ns |
| ADDR(12-0) valid delay from $CLK\uparrow$ | $t_{D(7)}$ | 2.9 | | 7 | ns |
| DATA(31-0) tristate to driven from $CLK\uparrow$ | $t_{D(8)}$ | 2.8 | | 7 | ns |
| DATA(31-0) valid delay from $CLK\uparrow$ | $t_{D(9)}$ | 2.8 | | 7 | ns |
| DATA(31-0) valid hold from $CLK\uparrow$ | t_H | 2.9 | | 7 | ns |
| DATA(31-0) driven to tristate from $CLK\uparrow$ | $t_{D(10)}$ | 2.9 | | 7 | ns |

Figure 22. SDRAM Interface - Burst Read

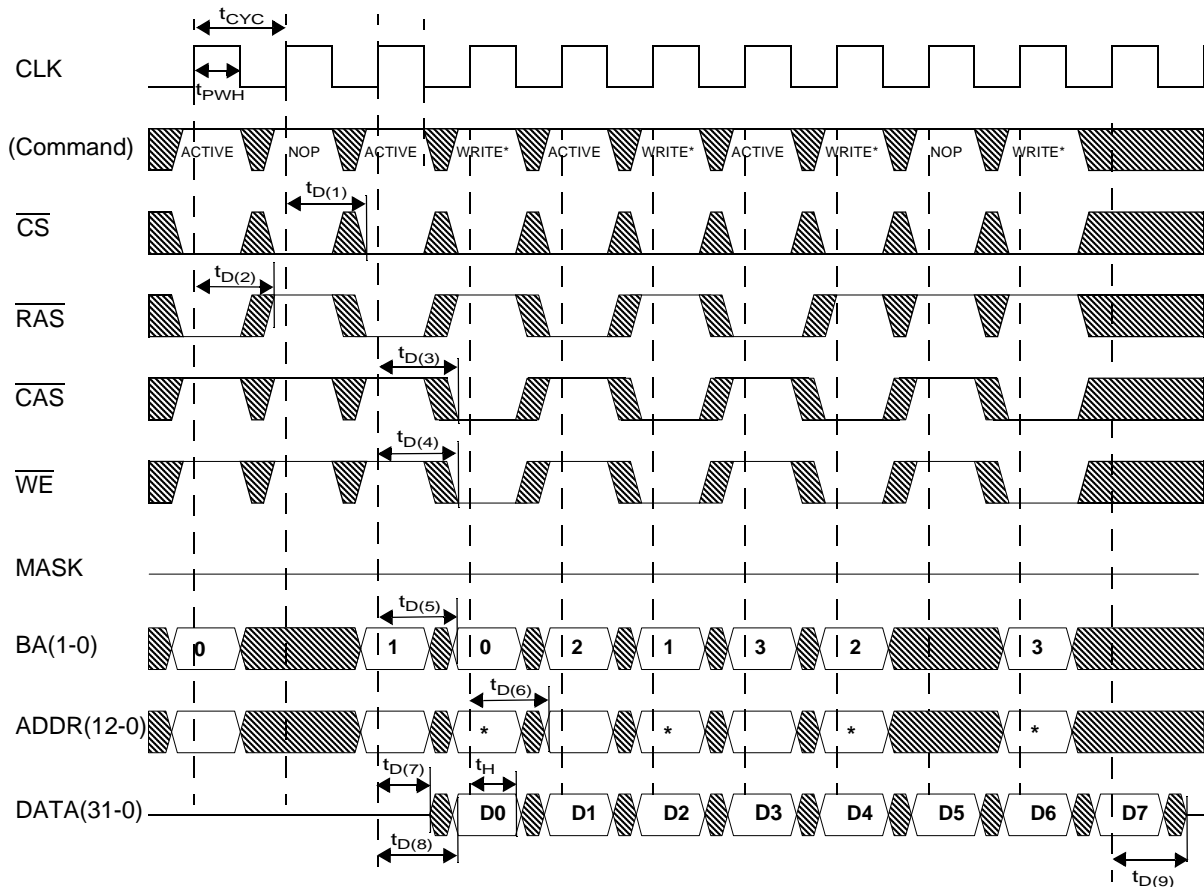


Note*: All read commands enable the auto precharge feature with ADDR(10)=1

30 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| CLK clock period | t_{CYC} | | 10 | | ns |
| CLK duty cycle, t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| \overline{CS} valid delay from CLK \uparrow | $t_{D(1)}$ | 2.9 | | 7 | ns |
| \overline{RAS} valid delay from CLK \uparrow | $t_{D(2)}$ | 2.9 | | 7 | ns |
| \overline{CAS} valid delay from CLK \uparrow | $t_{D(3)}$ | 2.9 | | 7 | ns |
| \overline{WE} valid delay from CLK \uparrow | $t_{D(4)}$ | 2.9 | | 7 | ns |
| BA(1-0) valid delay from CLK \uparrow | $t_{D(5)}$ | 2.9 | | 7 | ns |
| ADDR(12-0) valid delay from CLK \uparrow | $t_{D(6)}$ | 2.9 | | 7 | ns |
| DATA(31-0) setup time to CLK \uparrow | t_S | 2.5 | | | ns |
| DATA(31-0) hold time from CLK \uparrow | t_H | 1 | | | ns |

Figure 23. SDRAM Interface - Burst Write



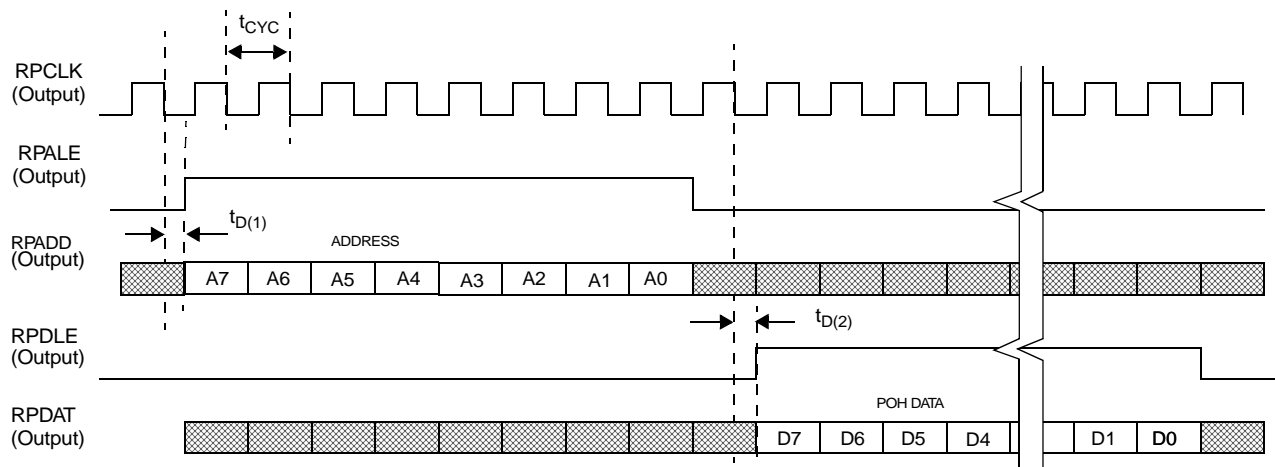
Note*: All write commands enable the auto precharge feature with ADDR(10)=1

30 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|-----|-----|------|
| CLK clock period | t_{CYC} | | 10 | | ns |
| CLK duty cycle, t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| \overline{CS} valid delay from CLK \uparrow | $t_{D(1)}$ | 2.9 | | 7 | ns |
| \overline{RAS} valid delay from CLK \uparrow | $t_{D(2)}$ | 2.9 | | 7 | ns |
| \overline{CAS} valid delay from CLK \uparrow | $t_{D(3)}$ | 2.9 | | 7 | ns |
| \overline{WE} valid delay from CLK \uparrow | $t_{D(4)}$ | 2.9 | | 7 | ns |
| BA(1-0) valid delay from CLK \uparrow | $t_{D(5)}$ | 2.9 | | 7 | ns |
| ADDR(12-0) valid delay from CLK \uparrow | $t_{D(6)}$ | 2.9 | | 7 | ns |
| DATA(31-0) tristate to driven from CLK \uparrow | $t_{D(7)}$ | 2.8 | | 7 | ns |
| DATA(31-0) valid delay from CLK \uparrow | $t_{D(8)}$ | 2.8 | | 7 | ns |
| DATA(31-0) valid hold from CLK \uparrow | t_H | 2.9 | | 7 | ns |
| DATA(31-0) driven to tristate from CLK \uparrow | $t_{D(9)}$ | 2.9 | | 7 | ns |

Note: For burst accesses $t_{D(8)}$ and t_H apply as the delay and hold parameters between successive data bytes.

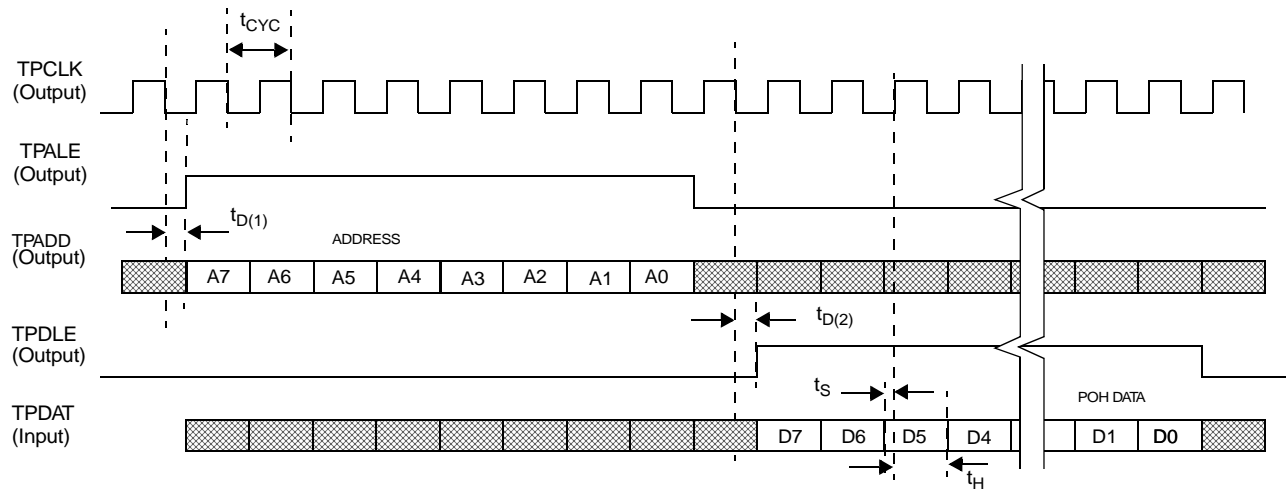
Figure 24. Rx VC-3 POH Byte Interface



50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|-------|-----|------|
| RPCLK clock period | t_{CYC} | | 51.44 | | ns |
| RPCLK clock duty cycle | | 40 | | 60 | % |
| RPALE/RPADD out valid delay from RPCLK↓ | $t_{D(1)}$ | 4 | | 16 | ns |
| RPDLE/RPDAT out valid delay from RPCLK↓ | $t_{D(2)}$ | 4 | | 16 | ns |

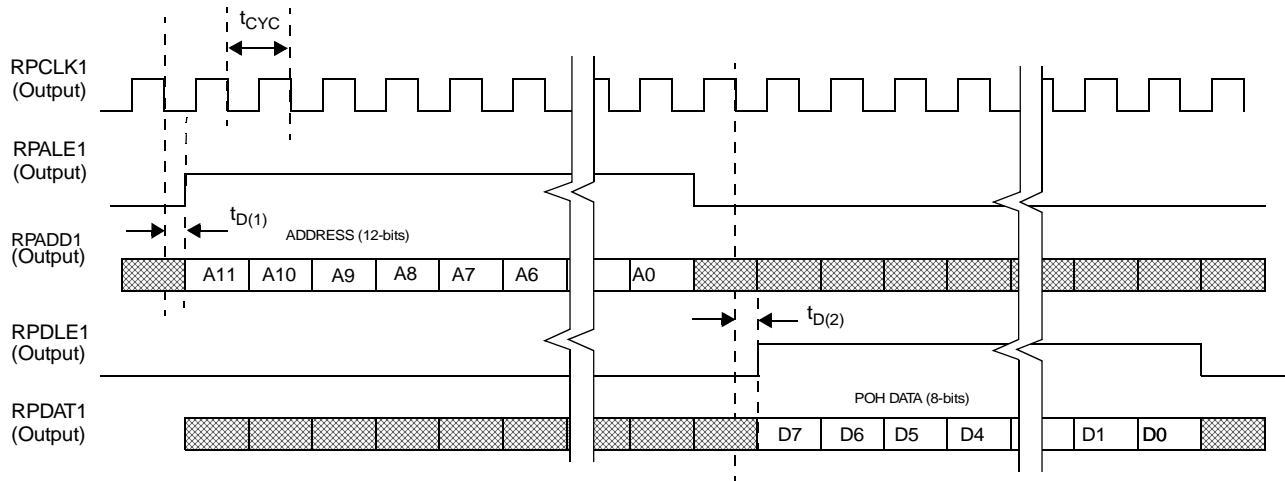
Figure 25. Tx VC-3 POH Byte Interface



50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------|-----|-------|-----|------|
| TPCLK clock period | t_{CYC} | | 51.44 | | ns |
| TPCLK clock duty cycle | | 40 | | 60 | % |
| TPALE/TPADD out valid delay from TPCLK↓ | $t_{D(1)}$ | 4 | | 16 | ns |
| TPDLE out valid delay from TPCLK↓ | $t_{D(2)}$ | 4 | | 16 | ns |
| TPDAT setup time before TPCLK↑ | t_s | 13 | | | ns |
| TPDAT hold time after TPCLK↑ | t_H | 0 | | | ns |

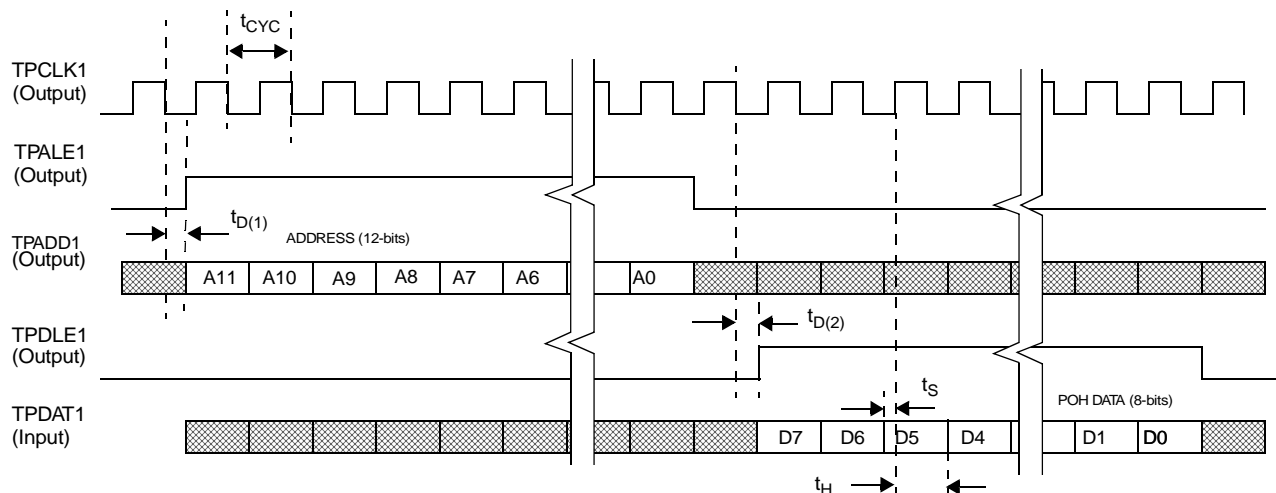
Figure 26. Rx Low Order POH Byte Interface



50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-------|-----|------|
| RPCLK1 clock period | t_{cyc} | | 51.44 | | ns |
| RPCLK1 clock duty cycle | | 40 | | 60 | % |
| RPALE1/RPADD1 out valid delay from RPCLK1↓ | $t_{D(1)}$ | 4 | | 16 | ns |
| RPDLE1/RPDAT1 out valid delay from RPCLK1↓ | $t_{D(2)}$ | 4 | | 16 | ns |

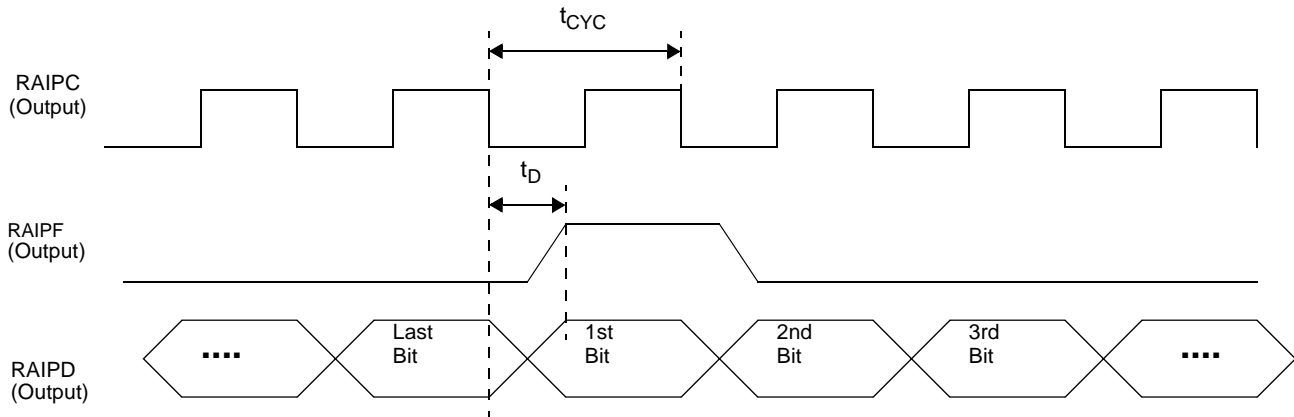
Figure 27. Tx Low Order POH Byte Interface



50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-------|-----|------|
| TPCLK1 clock period | t_{CYC} | | 51.44 | | ns |
| TPCLK1 clock duty cycle | | 40 | | 60 | % |
| TPALE1/TPADD1 out valid delay from TPCLK1↓ | $t_{D(1)}$ | 4 | | 16 | ns |
| TPDLE1 out valid delay from TPCLK1↓ | $t_{D(2)}$ | 4 | | 16 | ns |
| TPDAT1 setup time before TPCLK1↑ | t_s | 13 | | | ns |
| TPDAT1 hold time after TPCLK1↑ | t_h | 0.1 | | | ns |

Figure 28. Rx VC-3 Alarm Indication Port Interface



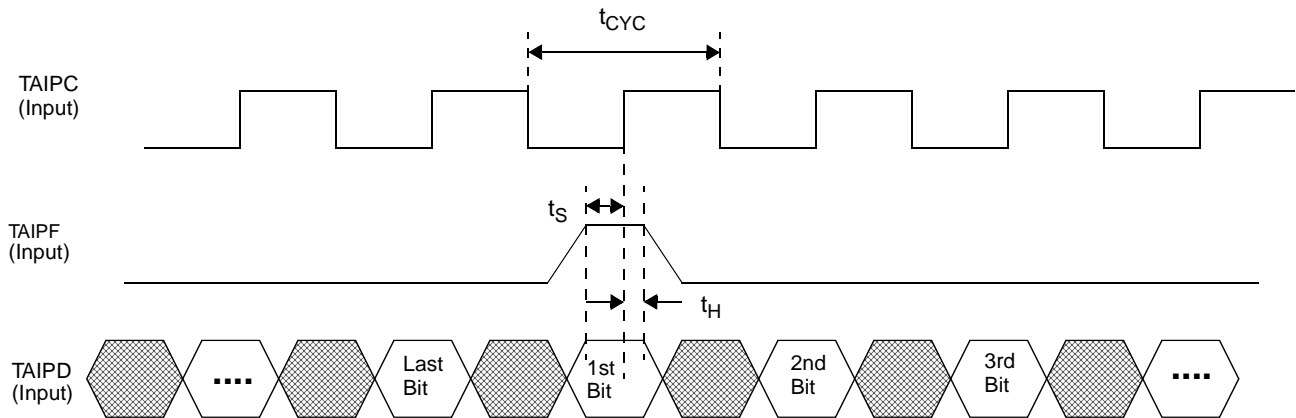
50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|-----|-----|------|
| RAIPC clock period | t_{cyc} | | 206 | | ns |
| RAIPC clock duty cycle | | 40 | | 60 | % |
| RAIPF/RAIPD output valid delay from RAIPC↓ | t_D | 4 | | 15 | ns |

Notes:

1. All the output signals are synchronous with the rising edge of internal clock SYSCLK (RTCLK=19.44MHz). According to a configuration bit, the framing pulse and the data can be "generated" on the falling edge or rising edge of RAIPC or RAIPC1.
2. The minimum value of t_D (4 ns) is maintained because the data and framing pulse are placed on the output when the falling/rising edge of the RAIPC/RAIPC1 is placed on the output. The maximum value of t_D is also maintained.

Figure 29. Tx VC-3 Alarm Indication Port Interface



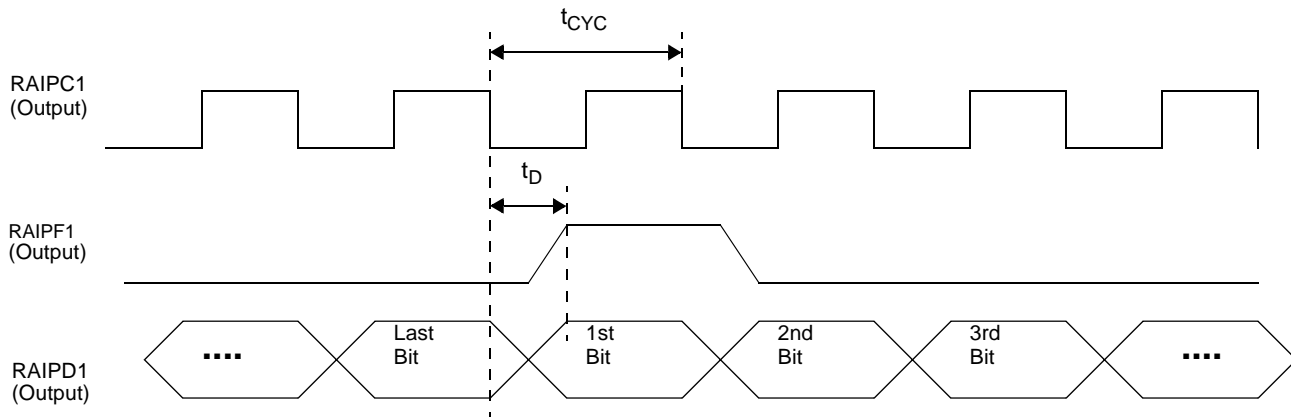
50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|-----|-----|------|
| TAIPC clock period | t_{cyc} | | 206 | | ns |
| TAIPC clock duty cycle | | 40 | | 60 | % |
| TAIPF/TAIPD setup time before TAIPC \uparrow | t_s | 60 | | | ns |
| TAIPF/TAIPD hold time after TAIPC \uparrow | t_H | 60 | | | ns |

Notes:

1. All 3 inputs are double synchronized with the rising edge of SYSCLK (RTCLK=19.44MHz). The TAIPC/TAIPC1 input clocks are working at SYSCLK divided by 4.
2. If 2 EtherMap-3 Plus devices are linked with the alarm indication ports, since the RAIPF is set to 1 during one RAIPC period (200 ns), the duration of the framing pulse is close to 200 ns at the input of TAIPF.

Figure 30. Rx Low Order Alarm Indication Port Interface



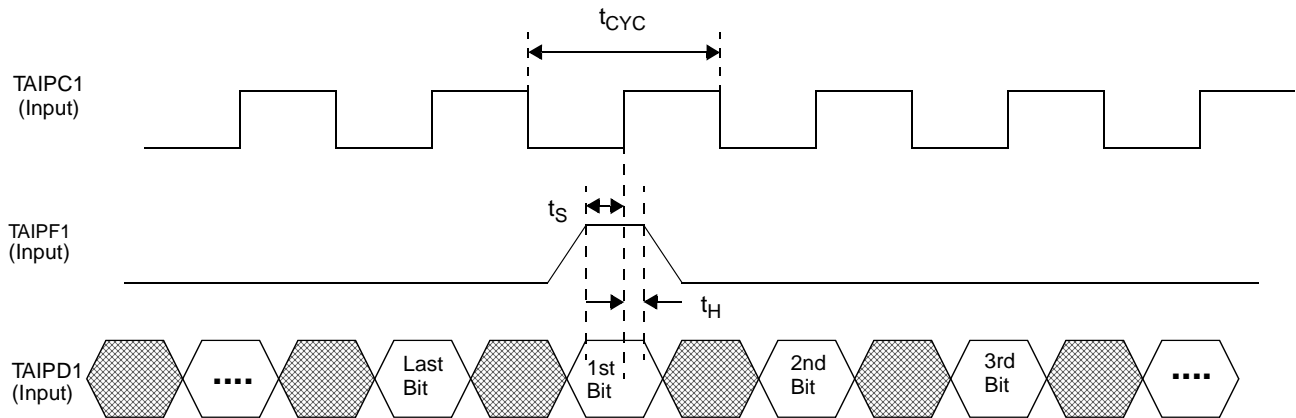
50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------|-----|-----|-----|------|
| RAIPC1 clock period | t_{cyc} | | 206 | | ns |
| RAIPC1 clock duty cycle | | 40 | | 60 | % |
| RAIPF1/RAIPD1 output valid delay from RAIPC1↓ | t_D | 4 | | 15 | ns |

Notes:

1. All the output signals are synchronous with the rising edge of internal clock SYSCLK (RTCLK=19.44MHz). According to a configuration bit, the framing pulse and the data can be "generated" on the falling edge or rising edge of RAIPC or RAIPC1.
2. The minimum value of t_D (4 ns) is maintained because the data and framing pulse are placed on the output when the falling/rising edge of the RAIPC/RAIPC1 is placed on the output. The maximum value of t_D is also maintained.

Figure 31. Tx Low Order Alarm Indication Port Interface



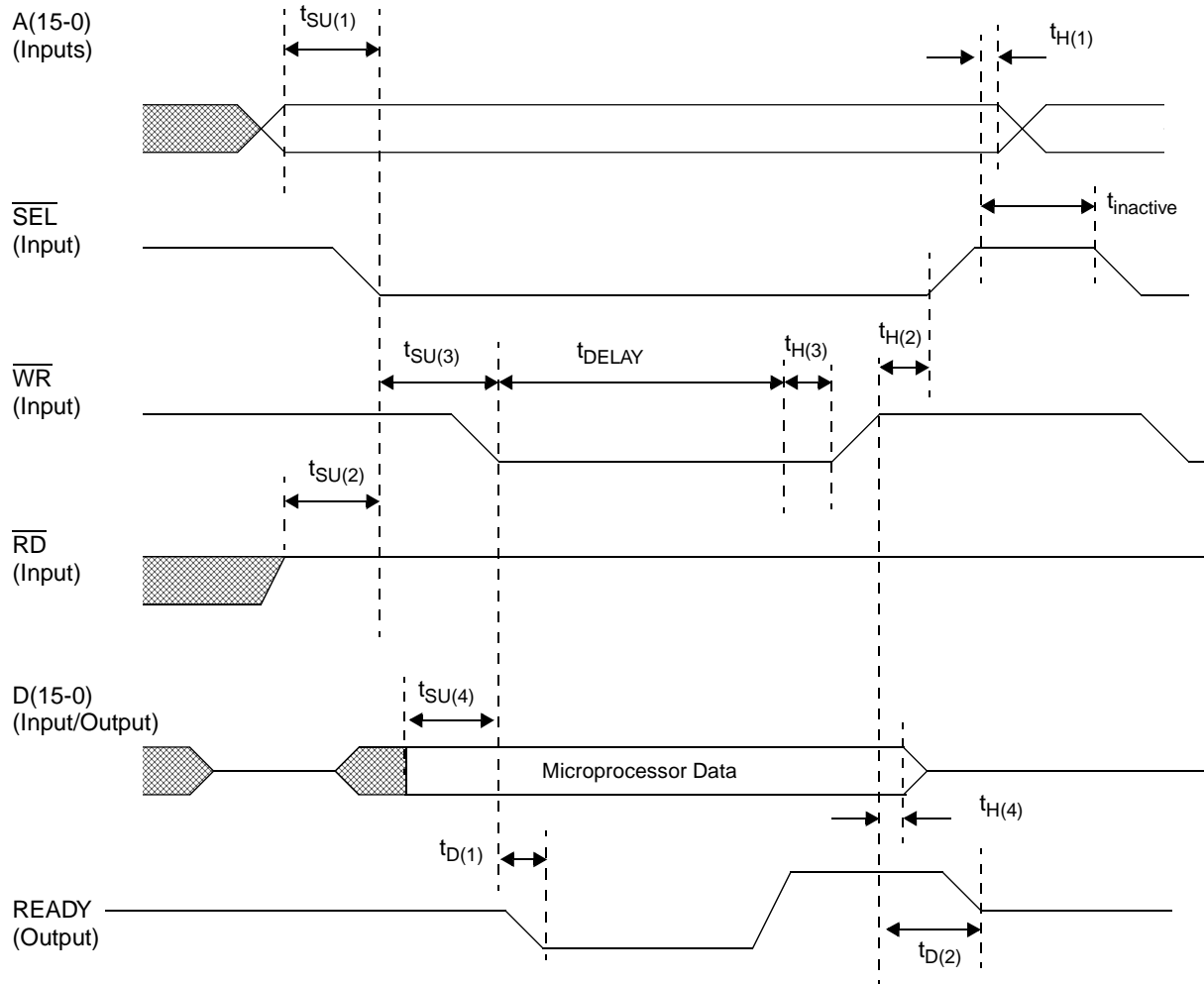
50 pF Load

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------|-----|-----|-----|------|
| TAIPC1 clock period | t_{CYC} | | 206 | | ns |
| TAIPC1 clock duty cycle | | 40 | | 60 | % |
| TAIPF1/TAIPD1 setup time before TAIPC1 \uparrow | t_S | 60 | | | ns |
| TAIPF1/TAIPD1 hold time after TAIPC1 \uparrow | t_H | 60 | | | ns |

Notes:

1. All the 3 inputs are double synchronized on the rising edge of SYSCLK (RTCLK=19.44MHz). The TAIPC/TAIPC1 input clocks are working at SYSCLK divided by 4.
2. If 2 EtherMap-3 Plus devices are linked with the alarm indication ports, since the RAIPF is set to 1 during one RAIPC period (200 ns), the duration of the framing pulse is close to 200 ns at the input of TAIPF.

Figure 32. Asynchronous Microprocessor Interface: Intel-type Write Cycle Timing



50 pF Load

See parameter table on next page.



DATA SHEET

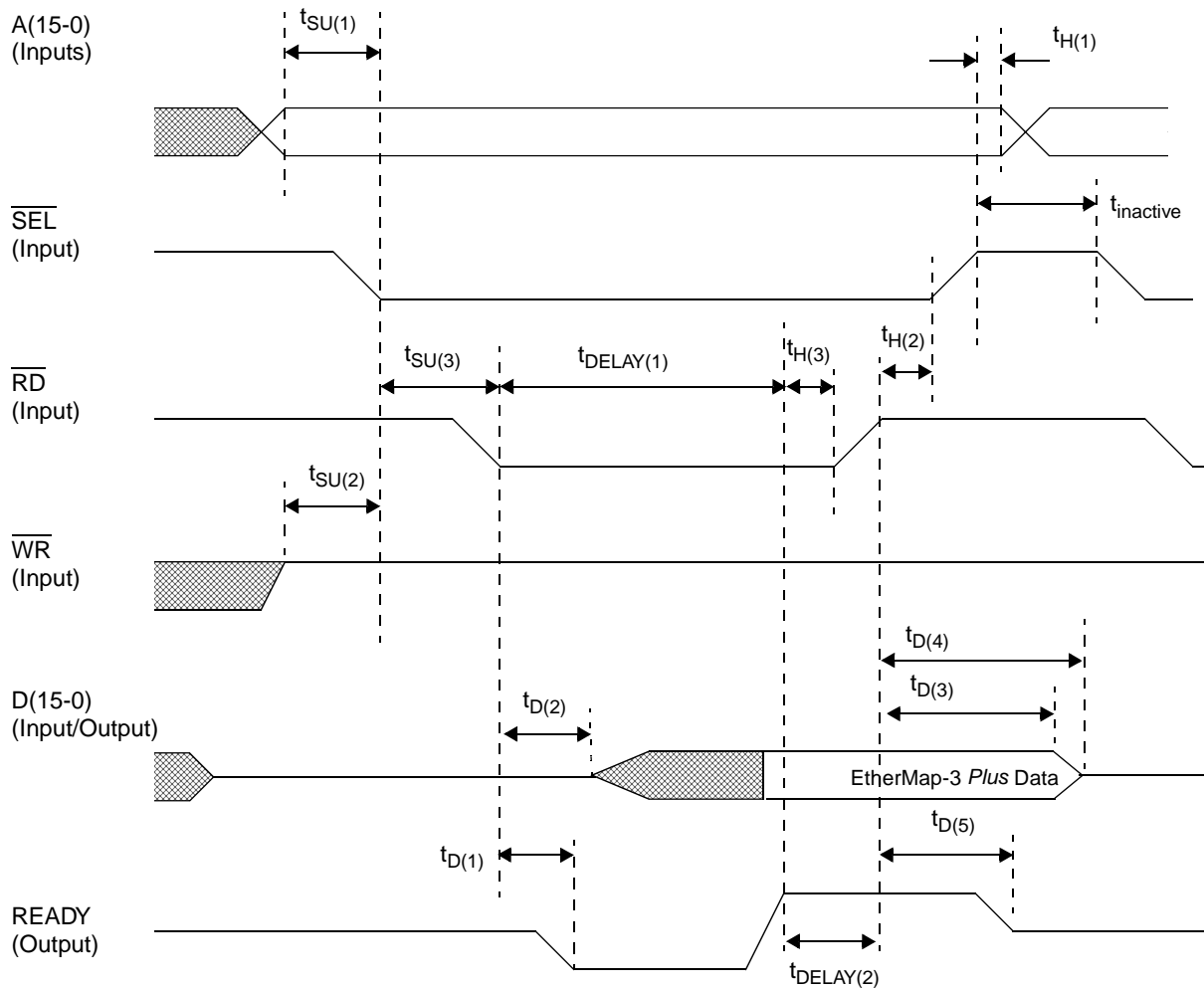
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------------|---------------|-----|---------------------------|------|
| MICCLK clock period (not shown in diagram) (see Note 1) | t_{CYC} | 20 | | Note 2 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| A(15-0) setup time to \overline{SEL} assertion | $t_{SU(1)}$ | 0 | | | ns |
| A(15-0) hold time from \overline{SEL} deassertion | $t_{H(1)}$ | 0 | | | ns |
| \overline{RD} deassertion setup time to \overline{SEL} assertion | $t_{SU(2)}$ | 0 | | | ns |
| \overline{SEL} assertion setup time to \overline{WR} assertion | $t_{SU(3)}$ | 5 | | | ns |
| \overline{WR} and \overline{SEL} assertion to READY valid delay | $t_{D(1)}$ | 2 | | 13 | ns |
| \overline{WR} or \overline{SEL} deassertion to READY Tristate delay | $t_{D(2)}$ | 2 | | 17 | ns |
| \overline{SEL} deassertion (high) time between accesses | $t_{INACTIVE}$ | 10 | | | ns |
| \overline{SEL} hold time from \overline{WR} deassertion | $t_{H(2)}$ | 5 | | | ns |
| \overline{WR} hold time from READY assertion | $t_{H(3)}$ | 0 | | | ns |
| D(15-0) input setup time to \overline{WR} assertion | $t_{SU(4)}$ | 5 | | | ns |
| D(15-0) input hold from \overline{WR} deassertion | $t_{H(4)}$ | $t_{CYC} + 5$ | | | ns |
| READY assertion from \overline{WR} assertion | t_{DELAY} | t_{CYC} | | $6 * t_{CYC} + 1.3 \mu s$ | - |

Notes:

1. MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 33. Asynchronous Microprocessor Interface: Intel-type Read Cycle Timing



50 pF Load

See parameter table on next page.



DATA SHEET

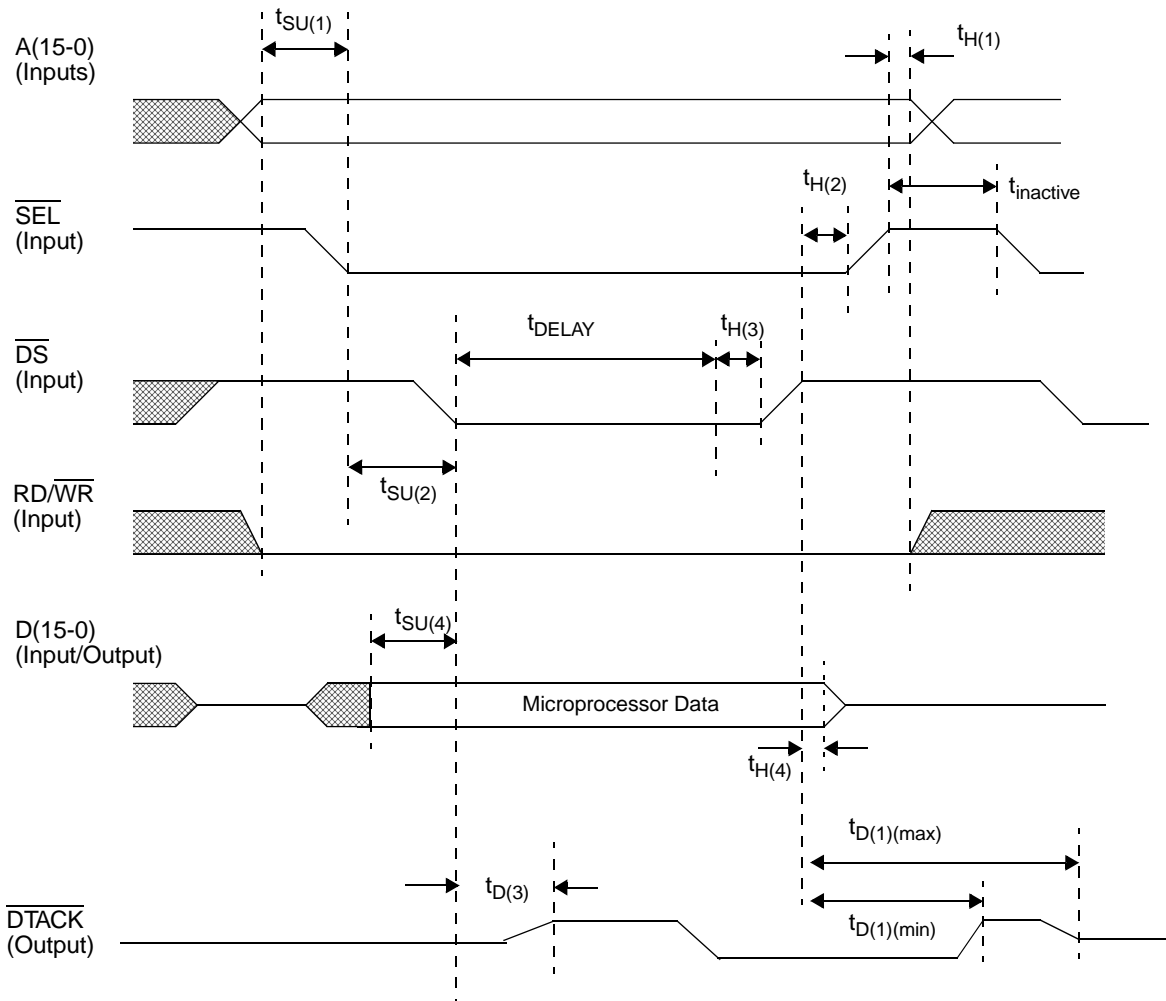
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|----------------|-----------|-----|-------------------------|------|
| MICCLK clock period (not shown in diagram) (see Note 1) | t_{CYC} | 20 | | Note 3 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| A(15-0) setup time to \overline{SEL} assertion | $t_{SU(1)}$ | 0 | | | ns |
| A(15-0) hold time from \overline{SEL} deassertion | $t_{H(1)}$ | 0 | | | ns |
| \overline{WR} deassertion setup time to \overline{SEL} assertion | $t_{SU(2)}$ | 0 | | | ns |
| \overline{SEL} assertion setup time to \overline{RD} assertion | $t_{SU(3)}$ | 5 | | | ns |
| \overline{RD} and \overline{SEL} assertion to READY valid delay | $t_{D(1)}$ | 2 | | 13 | ns |
| \overline{SEL} deassertion (high) time between accesses | $t_{INACTIVE}$ | t_{CYC} | | | ns |
| \overline{SEL} hold time from \overline{RD} deassertion | $t_{H(2)}$ | 5 | | | ns |
| \overline{RD} hold time from READY assertion | $t_{H(3)}$ | 0 | | | ns |
| READY assertion from \overline{RD} and \overline{SEL} assertion | t_{DELAY} | t_{CYC} | | $6*t_{CYC} + 1.3 \mu s$ | - |
| D(15-0) output tristate turned off from \overline{RD} and \overline{SEL} assertion | $t_{D(2)}$ | 2 | | 11 | ns |
| D(15-0) output valid delay from \overline{RD} or \overline{SEL} deassertion | $t_{D(3)}$ | 1 | | | ns |
| D(15-0) output tristate delay from \overline{RD} or \overline{SEL} deassertion | $t_{D(4)}$ | 3 | | 14 | ns |
| \overline{RD} or \overline{SEL} deassertion to READY Tristate delay | $t_{D(5)}$ | 2 | | 17 | ns |
| D(15-0) output rise and fall times | t_r, t_f | 2.49 | | Note 2 | ns |
| READY assertion to \overline{RD} deassertion | $t_{DELAY(2)}$ | | | $2*t_{CYC}$ | ns |

Notes:

1. The MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. t_r Max = 4.70 ns and t_f Max = 4.76 ns.
3. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 34. Asynchronous Microprocessor Interface: Motorola 68360-type Write Cycle Timing



50 pF Load

See parameter table on next page.



DATA SHEET

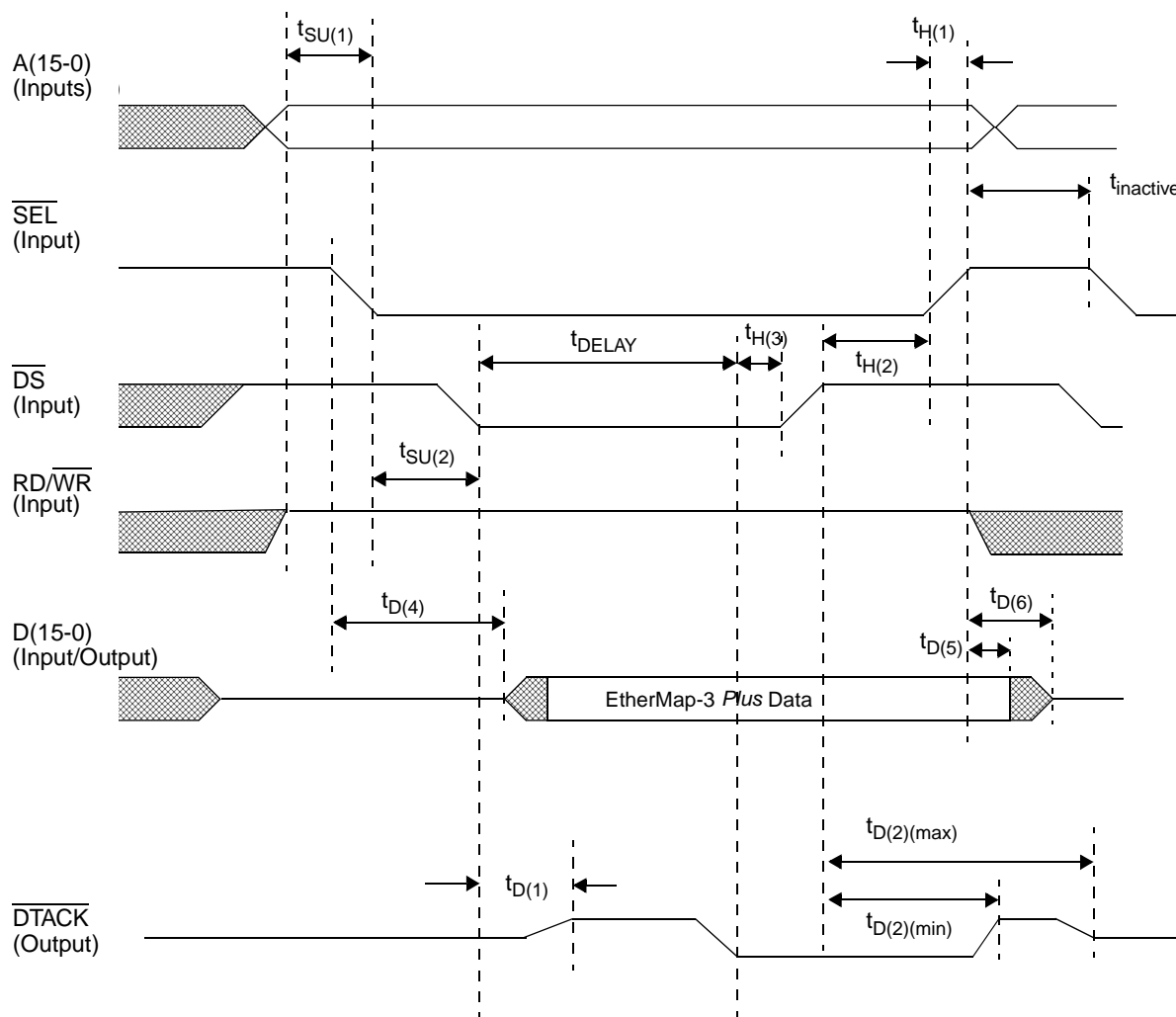
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------------|-----------|-----|-------------------------|------|
| MICCLK clock period (not shown in diagram) (see Note 1) | t_{CYC} | 20 | | Note 2 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| A(15-0)/RD \overline{WR} setup time to \overline{SEL} assertion | $t_{SU(1)}$ | 0.0 | | | ns |
| A(15-0)/RD \overline{WR} hold time from \overline{SEL} deassertion | $t_{H(1)}$ | 6.0 | | | ns |
| \overline{SEL} assertion setup time to \overline{DS} assertion | $t_{SU(2)}$ | 5.0 | | | ns |
| \overline{SEL} and \overline{DS} assertion to \overline{DTACK} valid delay | $t_{D(3)}$ | 0.0 | | 15 | ns |
| \overline{SEL} or \overline{DS} deassertion to \overline{DTACK} deassertion delay | $t_{D(1)}$ | 1.0 | | 15 | ns |
| \overline{SEL} deassertion (high) time between accesses | $t_{INACTIVE}$ | t_{CYC} | | | ns |
| \overline{SEL} hold time from \overline{DS} deassertion | $t_{H(2)}$ | 3.0 | | | ns |
| \overline{DS} hold time from \overline{DTACK} assertion | $t_{H(3)}$ | 0.0 | | | ns |
| D(15-0) input setup time to \overline{DS} assertion | $t_{SU(4)}$ | 5.0 | | | ns |
| D(15-0) input valid hold from \overline{DS} deassertion | $t_{H(4)}$ | t_{CYC} | | | ns |
| \overline{DTACK} assertion from \overline{DS} assertion | t_{DELAY} | t_{CYC} | | $6*t_{CYC} + 1.3 \mu s$ | - |

Notes:

1. The MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 35. Asynchronous Microprocessor Interface: Motorola 68360-type Read Cycle Timing



50 pF Load

See parameter table on next page.



DATA SHEET

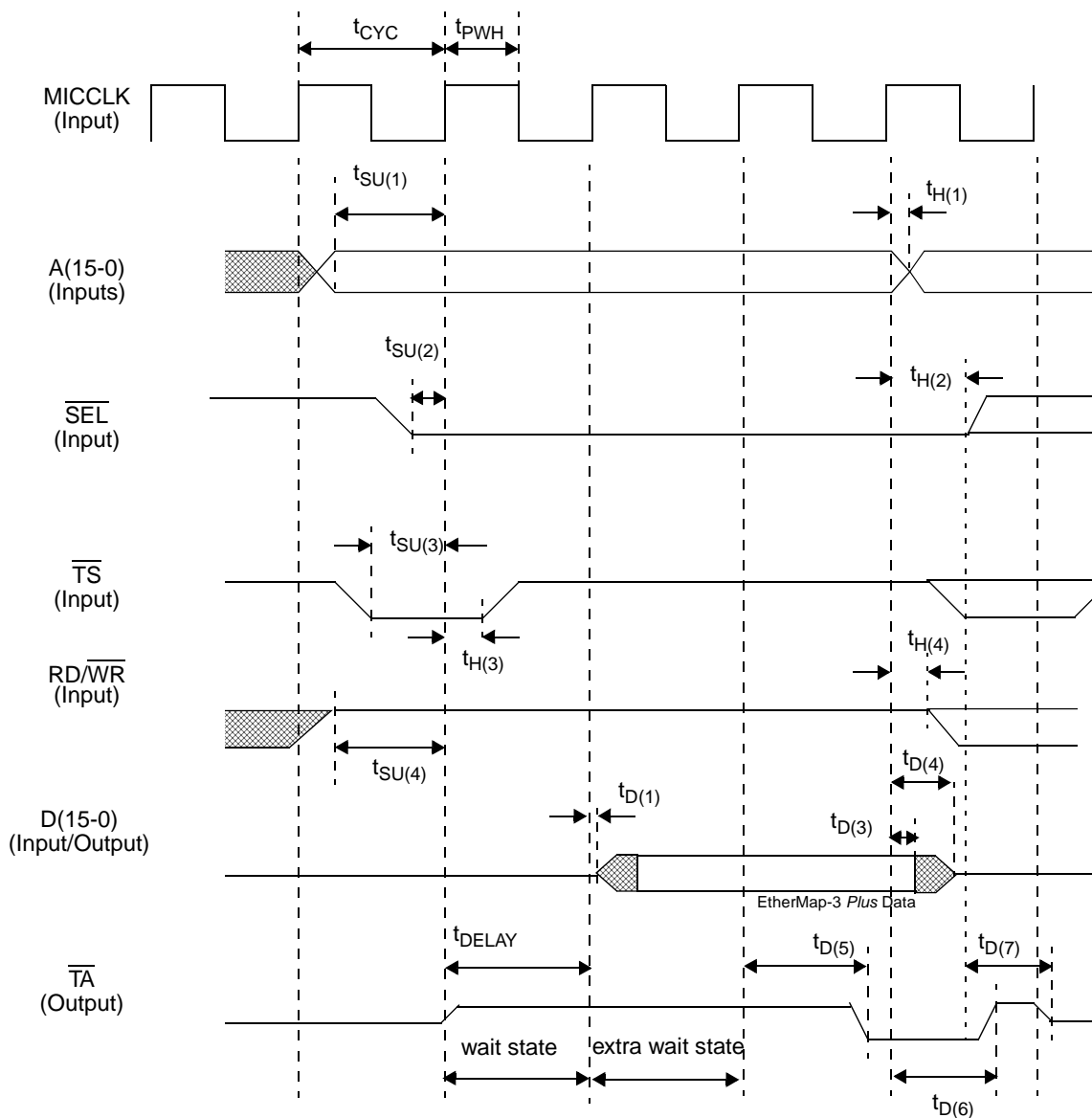
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------------|-----------|-----|-------------------------|------|
| MICCLK clock period (not shown in diagram) (see Note 1) | t_{CYC} | 20 | | Note 3 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 45 | | 55 | % |
| $A/RD/\overline{WR}$ setup time to \overline{SEL} assertion | $t_{SU(1)}$ | 0.0 | | | ns |
| $A/RD/\overline{WR}$ hold time from \overline{SEL} deassertion | $t_{H(1)}$ | 6.0 | | | ns |
| \overline{SEL} assertion setup time to \overline{DS} assertion | $t_{SU(2)}$ | 5.0 | | | ns |
| \overline{SEL} and \overline{DS} assertion to \overline{DTACK} valid delay | $t_{D(1)}$ | 0.0 | | 23 | ns |
| \overline{SEL} or \overline{DS} deassertion to \overline{DTACK} deassertion delay | $t_{D(2)}$ | 1.0 | | 23 | ns |
| \overline{SEL} deassertion (high) time between accesses | $t_{INACTIVE}$ | t_{CYC} | | | ns |
| \overline{SEL} hold time from \overline{DS} deassertion | $t_{H(2)}$ | 3.0 | | | ns |
| \overline{DS} hold time from \overline{DTACK} assertion | $t_{H(3)}$ | 0.0 | | | ns |
| \overline{DTACK} assertion from \overline{DS} assertion | t_{DELAY} | t_{CYC} | | $6*t_{CYC} + 1.3 \mu s$ | - |
| D(15-0) output tristate turned off from \overline{SEL} assertion | $t_{D(4)}$ | 3.0 | | 17 | ns |
| D(15-0) output valid hold from \overline{SEL} deassertion | $t_{D(5)}$ | 1.0 | | | ns |
| D(15-0) output tristated from \overline{SEL} deassertion | $t_{D(6)}$ | 3.0 | | 14 | ns |
| D(15-0) output rise and fall times | t_r, t_f | 2.49 | | Note 2 | ns |

Notes:

1. The MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. t_r Max = 4.70 ns and t_f Max = 4.76 ns.
3. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 36. Synchronous Microprocessor Interface: Motorola MPC860-type Read Cycle Timing



50 pF Load

Notes:

1. Only one wait state is shown (i.e., $t_{DELAY} = 1$ MICCLK cycle), but the EtherMap-3 Plus can insert more wait states by keeping \overline{TA} deasserted for additional clock cycles. Thus t_{DELAY} can be extended for a maximum of 30 MICCLK cycles. The extension of t_{DELAY} is caused by states of the internal logic and is not programmable by the user.
2. \overline{SEL} can be held low for multiple accesses without being brought high.
3. An extra wait state is inserted to meet setup/hold time of data / \overline{TA} .

See parameter table on next page.



DATA SHEET

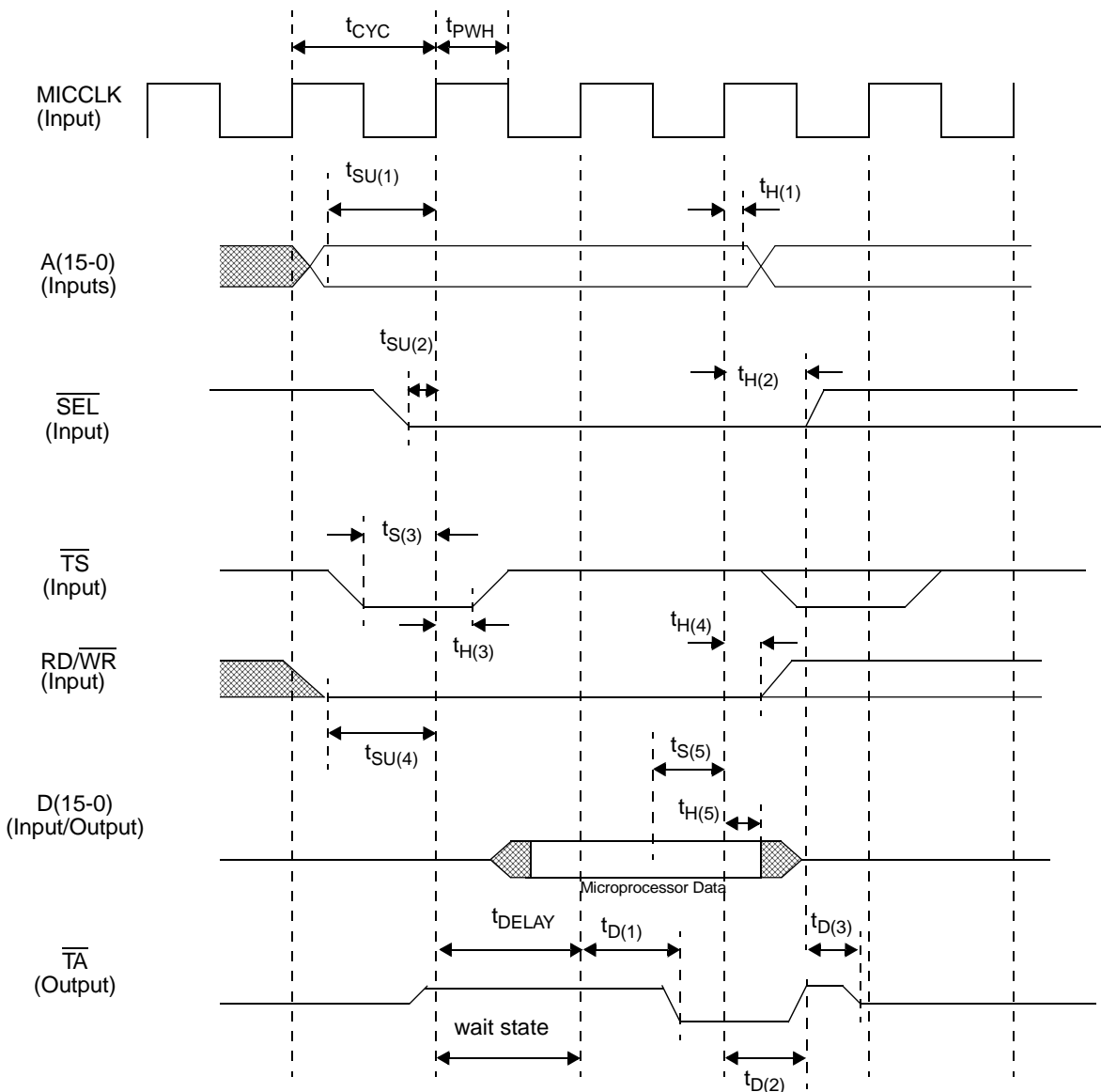
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------|-----------|-----|-------------------------------|------|
| MICCLK clock period (see Note 1) | t_{CYC} | 20 | | Note 3 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 40 | | 60 | % |
| A(15-0) setup time to MICCLK \uparrow | $t_{SU(1)}$ | 4 | | | ns |
| A(15-0) hold time from MICCLK \uparrow | $t_{H(1)}$ | 1 | | | ns |
| \overline{SEL} setup time to MICCLK \uparrow | $t_{SU(2)}$ | 4 | | | ns |
| \overline{SEL} hold time from MICCLK \uparrow | $t_{H(2)}$ | 1 | | | ns |
| \overline{TS} setup time to MICCLK \uparrow | $t_{SU(3)}$ | 4 | | | ns |
| \overline{TS} hold time from MICCLK \uparrow | $t_{H(3)}$ | 1 | | | ns |
| $\overline{RD}/\overline{WR}$ setup time to MICCLK \uparrow | $t_{SU(4)}$ | 4 | | | ns |
| $\overline{RD}/\overline{WR}$ hold time from MICCLK \uparrow | $t_{H(4)}$ | 3 | | | ns |
| D(15-0) output driven from MICCLK \uparrow | $t_{D(1)}$ | 0 | | 15 | ns |
| D(15-0) output stable from MICCLK \uparrow | $t_{D(3)}$ | 3 | | 15 | ns |
| D(15-0) output tristate from MICCLK \uparrow | $t_{D(4)}$ | 4 | | 17 | ns |
| \overline{TA} output driven low and stable from MICCLK \uparrow | $t_{D(5)}$ | 0 | | 10 | ns |
| \overline{TA} output driven high from MICCLK \uparrow | $t_{D(6)}$ | 3 | | 10 | ns |
| \overline{TA} output tristate from \overline{SEL} \uparrow | $t_{D(7)}$ | 4 | | 17 | ns |
| \overline{TA} assertion from \overline{TS} assertion | t_{DELAY} | t_{CYC} | | $6 \cdot t_{CYC} + 1.3 \mu s$ | - |
| D(15-0) output rise and fall times | t_r, t_f | 2.49 | | Note 2 | ns |

Notes:

1. The MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. t_r Max = 4.70 ns and t_f Max = 4.76 ns.
3. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 37. Synchronous Microprocessor Interface: Motorola MPC860-type Write Cycle Timing



50 pF Load

Notes:

1. Only one wait state is shown (i.e., $t_{DELAY} = 1$ MICCLK cycle), but the EtherMap-3 Plus can insert more wait states by keeping \overline{TA} deasserted for additional clock cycles. Thus t_{DELAY} can be extended for a maximum of 30 MICCLK cycles. The extension of t_{DELAY} is caused by states of the internal logic and is not programmable by the user.
2. \overline{SEL} can be held low for multiple accesses without being brought high.

See parameter table on next page.



DATA SHEET

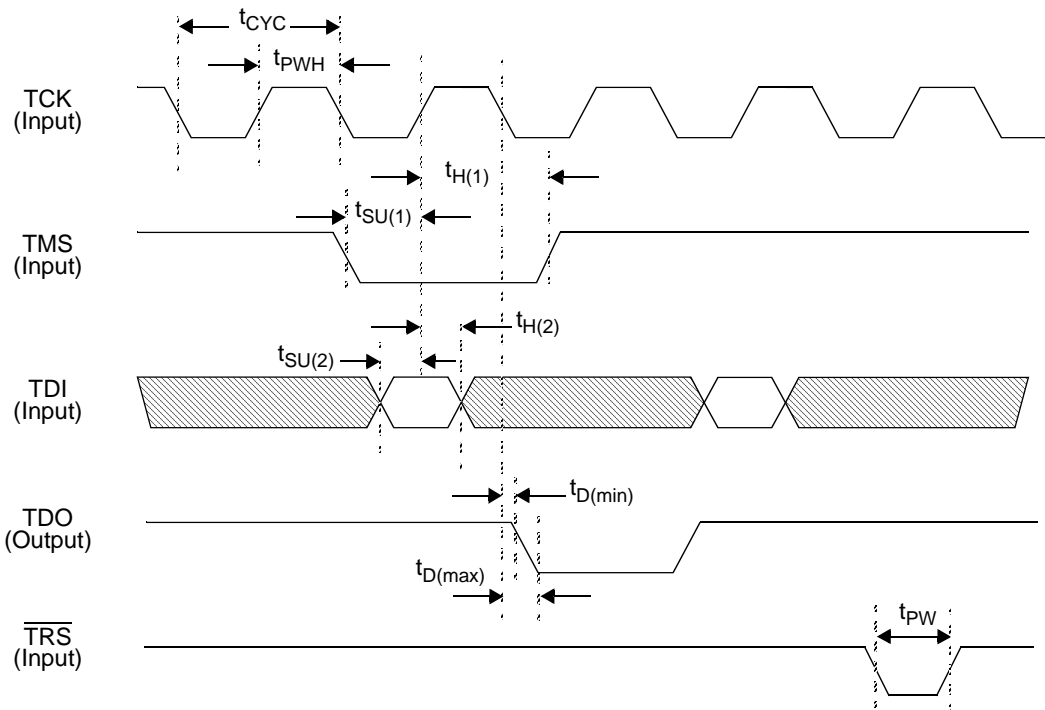
EtherMap-3 Plus
TXC-04236

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------|-----------|-----|-------------------------|------|
| MICCLK clock period (see Note 1) | t_{CYC} | 20 | | Note 2 | ns |
| MICCLK duty cycle t_{PWH}/t_{CYC} | | 40 | | 60 | % |
| A(15-0) setup time to MICCLK \uparrow | $t_{SU(1)}$ | 4 | | | ns |
| A(15-0) hold time from MICCLK \uparrow | $t_{H(1)}$ | 1 | | | ns |
| \overline{SEL} setup time to MICCLK \uparrow | $t_{SU(2)}$ | 4 | | | ns |
| \overline{SEL} hold time from MICCLK \uparrow | $t_{H(2)}$ | 1 | | | ns |
| \overline{TS} setup time to MICCLK \uparrow | $t_{SU(3)}$ | 4 | | | ns |
| \overline{TS} hold time from MICCLK \uparrow | $t_{H(3)}$ | 1 | | | ns |
| RD/\overline{WR} setup time to MICCLK \uparrow | $t_{SU(4)}$ | 4 | | | ns |
| RD/\overline{WR} hold time from MICCLK \uparrow | $t_{H(4)}$ | 3 | | | ns |
| D(15-0) setup time to MICCLK \uparrow | $t_{SU(5)}$ | 4 | | | ns |
| D(15-0) hold time from MICCLK \uparrow | $t_{H(5)}$ | 1.5 | | | ns |
| \overline{TA} output driven low and stable from MICCLK \uparrow | $t_{D(1)}$ | 0 | | 10 | ns |
| \overline{TA} output driven high from MICCLK \uparrow | $t_{D(2)}$ | 3 | | 10 | ns |
| \overline{TA} output tristate from $\overline{SEL}\uparrow$ | $t_{D(3)}$ | 4 | | 17 | ns |
| \overline{TA} assertion from \overline{TS} assertion | t_{DELAY} | t_{CYC} | | $6*t_{CYC} + 1.3 \mu s$ | - |
| D(15-0) output rise and fall times | t_r, t_f | 4.8 | | 5.3 | ns |

Notes:

1. The MICCLK must always be applied to the EtherMap-3 Plus to run the microprocessor interface.
2. For GMII mode, the minimum MICCLK clock frequency is 25 MHz. For SMII mode, the minimum MICCLK clock frequency is 6.5 MHz.

Figure 38. Boundary Scan Timing



| Parameter | Symbol | Min | Max | Unit |
|--|-------------|-----|-----|------|
| TCK clock period | t_{CYC} | 50 | | ns |
| TCK clock duty cycle t_{PWH}/t_{CYC} | | 40 | 60 | % |
| TMS setup time to TCK \uparrow | $t_{SU(1)}$ | 3.0 | | ns |
| TMS hold time after TCK \uparrow | $t_{H(1)}$ | 15 | | ns |
| TDI setup time to TCK \uparrow | $t_{SU(2)}$ | 3.0 | | ns |
| TDI hold time after TCK \uparrow | $t_{H(2)}$ | 15 | | ns |
| TDO delay from TCK \downarrow | t_D | 4.0 | 20 | ns |
| \overline{TRS} pulse width | t_{PW} | 50 | | ns |

OPERATION

SONET/SDH PROCESSING

General

The Mapper and Demapper blocks provide the SONET/SDH processing of the EtherMap-3 Plus. The Mapper maps and multiplexes (virtual concatenated) payload into a VC-4/STS-3c/VC-3/STS-1 structure on the ADD Telecom bus. Conversely the Demapper demaps and demultiplexes a VC-4/STS-3c/VC-3/STS-1 structure from the DROP Telecom bus into (virtual concatenated) payload. Figure 39 shows a functional block diagram of the Mapper and Demapper blocks.

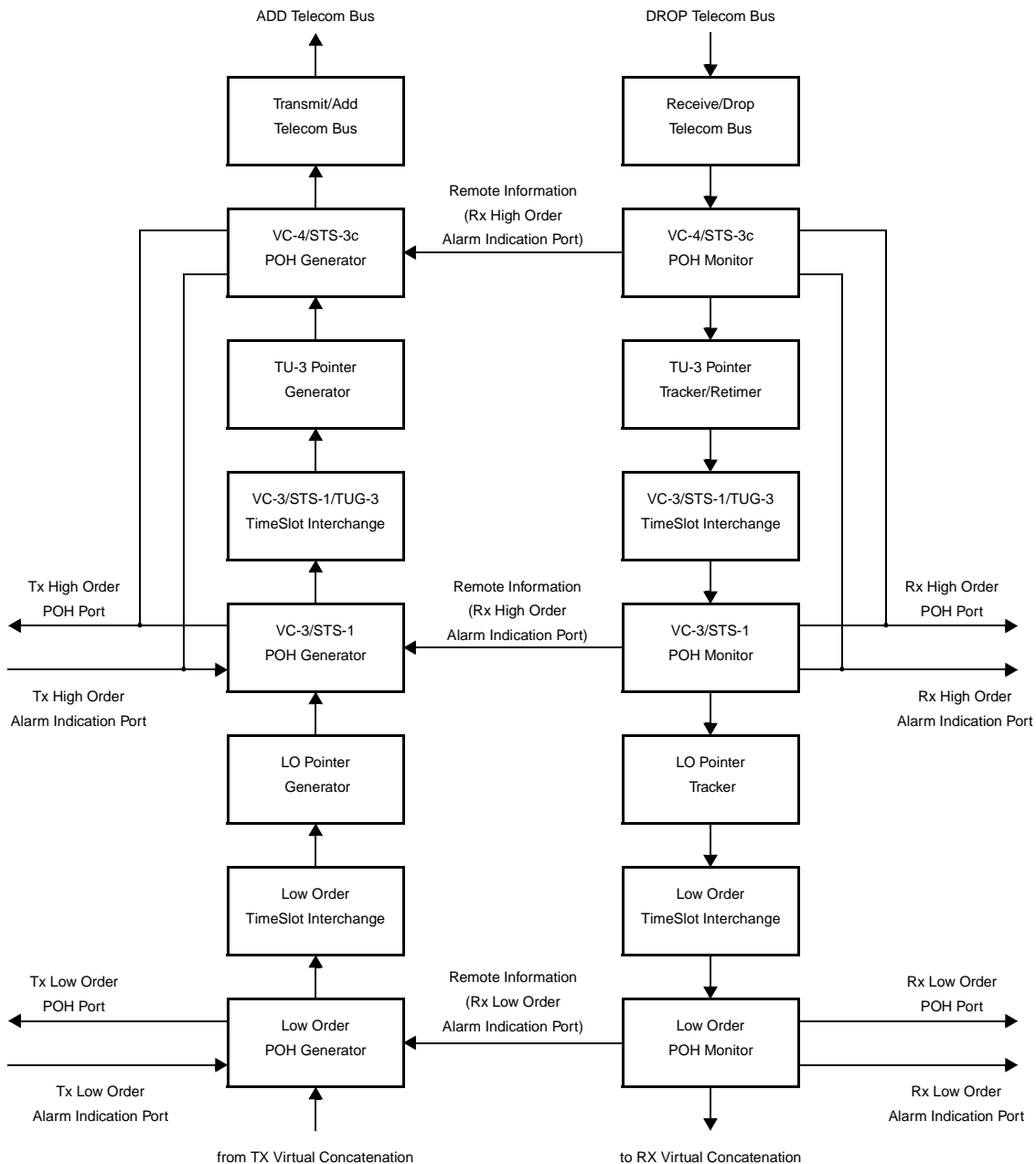


Figure 39. Functional Block Diagram of the Mapper/Demapper

Figure 40 presents a bi-directional functional model according to ITU-T G.783 of the functionality made available through the Mapper and Demapper blocks (also see ITU-T G.806 for the terminology used). The Telecom bus is represented as server layer to the S3 or S4 high order path layer.

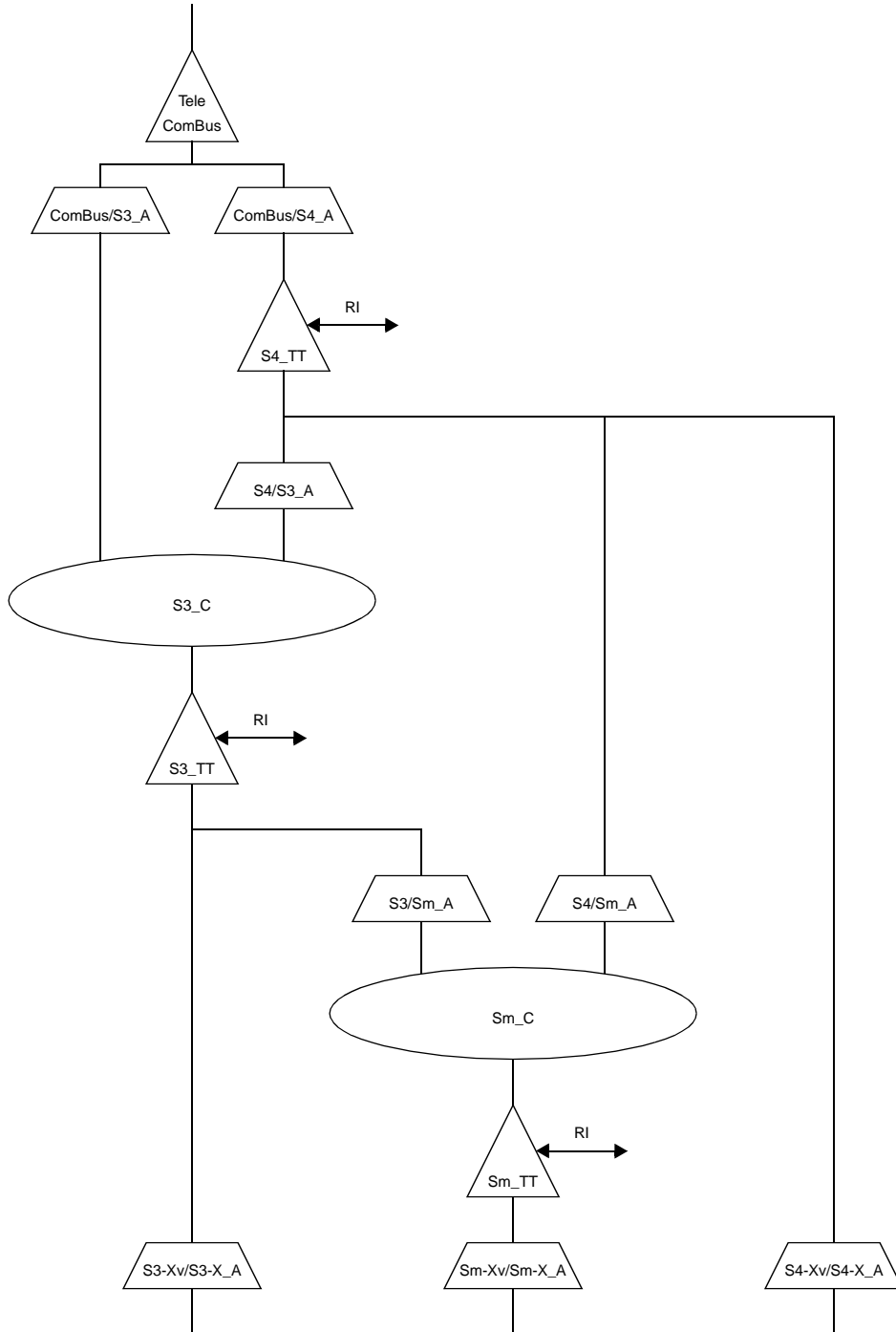


Figure 40. Functional Model of the Mapper/Demapper

Bypass Modes

Each of the Mapper and Demapper blocks has a bypass mode which can be configured per STS-1/VC-3/TUG-3 timeslot to obtain the desired SONET/SDH mapping structure.

Superimposing functional model and block diagram in [Figure 41](#) reveals which blocks require bypassing.

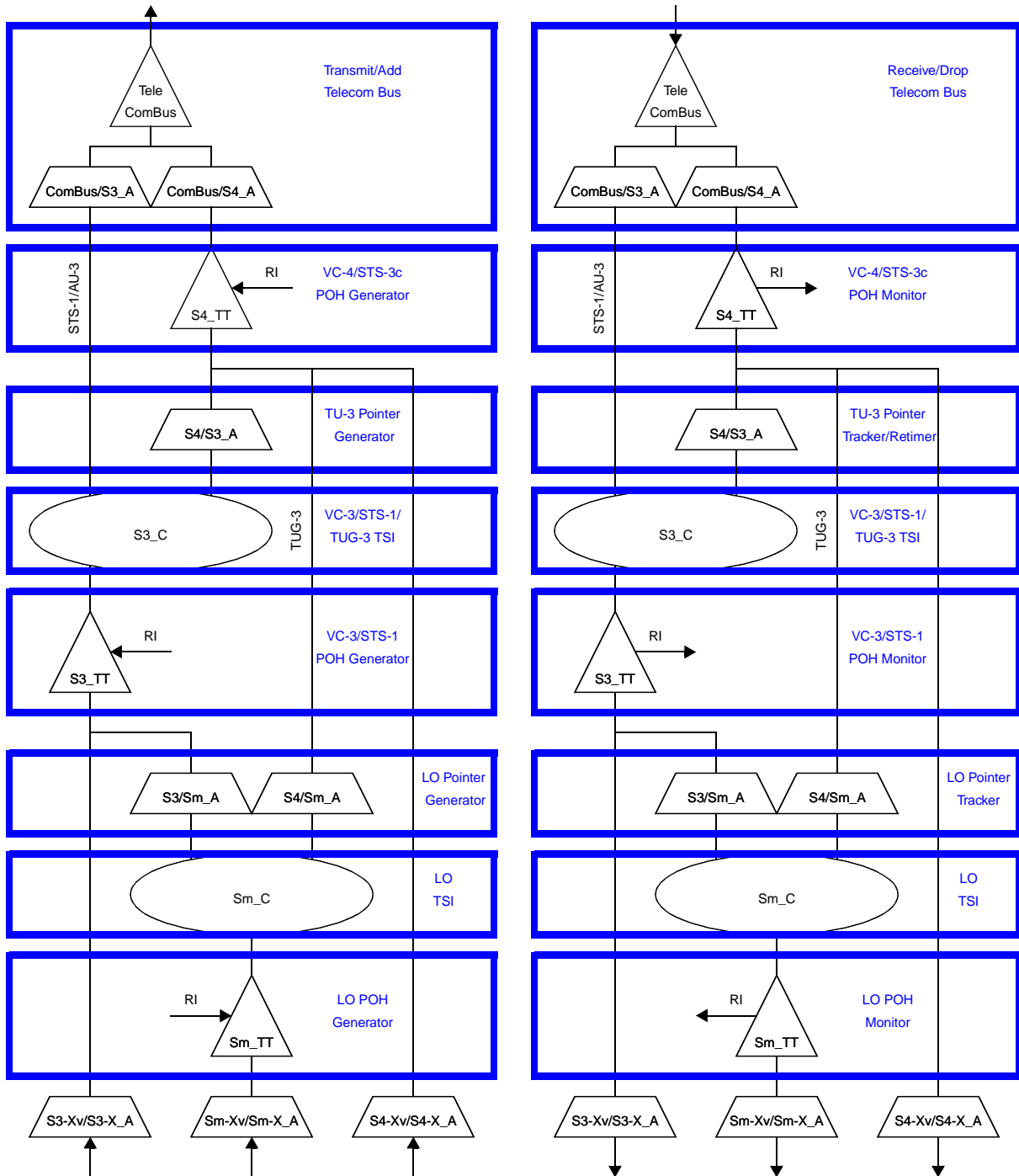


Figure 41. Mapper/Demapper Bypass Modes

Receive Direction:

- The VC-4/STS-3c POH Monitor is bypassed by setting bit 1 (Bypass) of address 0x1f680,
- The TU-3 Pointer Tracker/Retimer can be physically bypassed (the output of the VC-4/STS-3c POH Monitor is also distributed as additional port to the Receive VC-3/STS-1/TUG-3 TSI, i.e., the path from S4_TT to S4-Xv/S4-X_A) for an unstructured VC-4/STS-3c signal. For substructured VC-4 or AU-3/STS-1 based signals the TU-3 Pointer Tracker/Retimer supports the following modes per high order time slot by writing the AUG1_Format and TUG3_Format bits at address 0x19c80 (0x19c90, 0x19ca0):

Table 1: TU-3 Pointer Tracker/Retimer Modes

| 0x19c80/90/a0 | Mode | |
|---------------|-------------------------------|---------------------|
| 0x0000 | AU-3/STS-1 mapping | Combus/S3_A to S3_C |
| 0x0001 | AU-4/VC-4/TUG-3/TU-3 mapping | S4_TT to S4/S3_A |
| 0x0003 | AU-4/VC-4/TUG-3/TUG-2 mapping | S4_TT to S4/Sm_A |

- The Receive VC-3/STS-1/TUG-3 TSI is bypassed by connecting straight through,
- The VC-3/STS-1 POH Monitor can be bypassed per high order time slot by setting bit 1 (Bypass) of address 0x1d900 (0x1d920, 0x1d940),
- The Low Order Pointer Tracker can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x1c620 (0x1c622, 0x1c624),
- The Receive Low Order TSI can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x1c600 (0x1c602, 0x1c604),
- The Low Order POH Monitor can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x148e0 (0x148e2, 0x148e4), additionally for a VC-4/STS-3c non-substructured bypass (S4_TT to S4-Xv/S4-X_A) the VC-4 has C4 register at address 0x14800 has to be set.

Transmit Direction:

- The VC-4/STS-3c POH Generator is bypassed by setting bit 3 (PassPOH) of address 0x1d058,
- The TU-3 Pointer Generator supports the following modes per high order time slot by writing the Conversion Type register at address 0x19ee0 (0x19ee8, 0x19ef0):

Table 2: TU-3 Pointer Generator Modes

| 0x19ee0/e8/f0 | Mode | |
|---------------|--------------------------------|--|
| 0x0000 | AU-3/STS-1 mapping | S3_C to Combus/S3_A |
| 0x0001 | AU-4/VC-4/TUG-3/TU-3 mapping | Special case where internally AU-3 is generated and converted to TUG-3. The AU-4 has a fixed pointer, but the TU-3 pointers may adjust to cope with phase differences between the TU-3 and AU-3. |
| 0x0002 | AU-4/VC-4/TUG-3/TU-3 mapping | S3_C to S4/S3_A |
| 0x0004 | AU-4/VC-4/TUG-3/TUG-2 mapping | S4/Sm_A to S4_TT |
| 0x0005 | AU-4/VC-4 unstructured mapping | S4-Xv/S4-X_A to S4_TT |

- The Transmit VC-3/STS-1/TUG-3 TSI is bypassed by connecting straight through,
- The VC-3/STS-1 POH Generator can be bypassed per high order time slot by setting bit 3 (PassPOH) of address 0x1f960 (0x1f962, 0x1f964),
- The Low Order Pointer Generator can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x1a480 (0x1a482, 0x1a484),
- The Transmit Low Order TSI can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x1a4c0 (0x1a4c2, 0x1a4c4),
- The Low Order POH Generator can be bypassed per high order time slot by writing 0x0001 to the ByPass register at address 0x1a440 (0x1a442, 0x1a444),



TRANSMIT HIGH ORDER PATH TERMINATION (VC-3/VC-4/STS-1/STS-3C POH Generator)

General

The EtherMap-3 Plus optionally provides transmit high order path termination functions for one STS-3c-SPE/VC-4s and three STS-1-SPE/VC-3s.

J1

The transmitted J1 path trace message can be written by the microprocessor for transmission into the uP_J1MessageBytes RAM at address 0x1d080 (0x1fa00, 0x1fa80, 0x1fb00). The EtherMap-3 Plus device supports 16 or 64 byte long repeating messages, the length can be selected via the J1_Length64 register, i.e., bit 0 at address 0x1d040 (0x1f900, 0x1f902, 0x1f904).

B3

The B3 is calculated and transmitted for each SPE/VC.

For test purposes the EtherMap-3 Plus supports a B3 error mask in the POH RAM, at address 0x1d000 (0x1f800, 0x1f810, 0x1f820). When the B3_Masking register, bit 1 at address 0x1d040 (0x1f900, 0x1f902, 0x1f904), is set, the calculated B3 is xor'ed with the B3 error mask before being inserted into the signal.

C2

The C2 signal label can be written by the microprocessor for transmission into the C2 position of the POH RAM at address 0x1d002 (0x1f802, 0x1f812, 0x1f822).

The EtherMap-3 Plus also has the option to source an unequipped signal by setting the ForceUneq register (bit 1 at address 0x1d058 (0x1f960, 0x1f962, 0x1f964)) or a supervisory unequipped SPE/VC by setting the ForceSupUneq register (bit 2 at address 0x1d058 (0x1f960, 0x1f962, 0x1f964)).

G1

The received B3 errors are automatically inserted into the G1 byte as path REI.

The EtherMap-3 Plus has on option to transmit either a single bit path RDI or an enhanced 3-bit path RDI. Selection is made via the OneBitRDI register (bit 3 at address 0x1d058 (0x1f960, 0x1f962, 0x1f964)).

The transmitted G1 bytes can be generated from local alarm conditions or derived from the Alarm Indication Port Interface. The selection is made per high order path timeslot on the high order Alarm Indication Port interface via the SelectInterface register at address (0x19a80+4(decimal)*timeslot). See the High Order Alarm Indication Port Interface section for the time slot assignment.

| 0x19a80+4(decimal)*timeslot | SelectInterface |
|-----------------------------|--|
| 0 | RDI and REI generated from local alarm conditions. |
| 1 | RDI and REI derived from high order alarm indication port interface. |

When the uni-directional option is active by setting the G1_UniDirectional register (bit 2 at address 0x1d058 (0x1f960, 0x1f962, 0x1f964)), all transmitted remote information is set to zero.

H4

The H4 byte can be written by the microprocessor into the POH RAM, at address 0x1d008 (0x1f808, 0x1f818, 0x1f828), or by the High Order POH port interface for transmission, or it can be selected to carry the V1/V2 multiframe in case the SPE/VC is substructured into low order VT/TUs, or it can be selected to carry the virtual concatenation multiframe and control packets in case high order virtual concatenation is active for this SPE/VC. This selection is made via the H4_Control register, bits 11-10 at address 0x1d040 (0x1f900, 0x1f902, 0x1f904):

| bit 11 | bit 10 | H4_Control |
|--------|--------|---|
| 0 | 0 | Insert H4 from the POH RAM, e.g. for an unstructured, non-virtual concatenated VC-4/STS-3c. |
| 0 | 1 | Insert H4 from the High Order POH port. |
| 1 | 0 | Pass the multiframe and control word for a virtual concatenated VC-3/STS-1. |
| 1 | 1 | Generate the V1/V2 multiframe for VC-3/VC-4/STS-1 SPE substructured into LO VT/TU's. |

F2, F3/Z3, K3/Z4, and N1/Z5

The F2, F3/Z3, K3/Z4, and N1/Z5 bytes can be written by the microprocessor into the POH RAM, see [Table 241, on page 338](#), or by the High Order POH port interface for transmission. These values are static and are not acted upon by the EtherMap-3 Plus transmit logic.

The source can be selected via the F2_Control, F3_Control, K3_Control and N1_Control registers (bits 9, 12, 13 and 14 at address 0x1d040 (0x1f900, 0x1f902, 0x1f904)): a value of 0 selects the POH RAM, a value of 1 selects the POH port.

RECEIVE HIGH ORDER PATH TERMINATION (VC-3/VC-4/STS-1/STS-3C POH Monitor)**General**

The EtherMap-3 Plus optionally provides receive high order path termination functions for one STS-3c-SPE/VC-4s and three VC-3/STS-1-SPE/VC-3s.

The received POH bytes are always forwarded to the receive high order POH Port interface and written to the receive high order POH RAM at address 0x1f640 (0x1d800, 0x1d820, 0x1d840).

J1

Both 16 and 64 byte messages can be received. The expected J1 path trace message can be configured at address 0x1f500 (0x1de00, 0x1de80, 0x1df00). The received J1 path trace is compared with the microprocessor written expected J1 path trace. If a mismatch occurs between received and expected J1 path trace, a trace identifier mismatch defect (dTIM) is declared. An all-zero path trace is also reported to allow detection of an unequipped signal versus a supervisory unequipped signal.

The microprocessor can retrieve the value of the received J1 path trace of one VC-4/STS-3c and of one VC-3/STS-1 path termination at a time.

| Address | Register | Description |
|-------------------------------|-------------------|---|
| 0x1f400 (0x1db00) | | Accepted 64 byte Trace Message |
| 0x1f742 (0x1dc42), bit 0 | J1_Report_Enable | Enable reporting of the accepted J1 trace message for the J1_Report_Channel. |
| 0x1f742 (0x1dc42), bit 2-1 | J1_Report_Channel | Select the VC-4/STS-3c SPE (VC-3/STS-1 SPE) channel for which the J1 accepted trace message is retrieved. |
| 0x1f760 (0x1dc50), bit 0 | J1_Stable_1 | A constantly repeating single J1 byte has been detected. |
| 0x1f760 (0x1dc50), bit 1 | J1_Stable_16 | A 16-byte J1 trace message has been detected. |
| 0x1f760 (0x1dc50), bit 2 | J1_Stable_64 | A 64-byte J1 trace message has been detected. |

The number of trace message multiframes to set or reset the TIM Defect is configurable via registers J1_NrOfFramesToSetTim (bits 6-3 at address 0x1f682 (0x1d902, 0x1d922, 0x1d942)) and J1_NrOfFramesToResetTim (bits 10-7 at address 0x1f682 (0x1d902, 0x1d922 and 0x1d942)).

B3

Performance monitor counters are provided for the B3 errors and B3 block errors.

Optionally the burst error degraded signal defect can be detected. The threshold values and interval times are configurable per high order path via registers B3_SetThresHold, B3_ClearThreshold, B3_SetNrOfIntervals and B3_ClearNrOfIntervals at address 0x1f688-0x1f68c (0x1d908-0x1d90c, 0x1d928-0x1d92c, 0x1d948-0x1d94c).

The Signal Degrade registers pertain to the detection of the degraded signal defect, assuming a bursty distribution of errors, as in 6.2.3.1.2/G.806. Above registers correspond to the DEGTHR and DEGM settings referred to by 6.2.3.1.2/G.806. The EtherMap-3 Plus does not detect "Excessive error" (Excessive error assumes a Poisson distribution of errors, as in 6.2.3.1.1/G.806).

The detection algorithms assuming bursty distribution uses the one second block error counts for performance monitoring. The one second clock ONESEC (see [page 43](#)), is required.

The degraded signal defect (dDEG) is declared if B3_SetNrOfIntervals consecutive bad intervals (interval is the one second period used for performance monitoring) are detected. An interval is declared bad if the number of errored blocks in that interval \geq Degraded Threshold (B3_SetThresHold).

The degraded signal defect is cleared if B3_ClearNrOfIntervals consecutive good intervals are detected. An interval is declared good if the number of errored blocks in that interval $<$ B3_ClearThreshold.

The parameters B3_SetNrOfIntervals and B3_ClearNrOfIntervals are provisionable in the range 2 to 10.

The DEGTHR parameters B3_SetThresHold and B3_ClearThreshold are to be provisioned as a number of errored blocks in the range of $0 < \text{DEGTHR} \leq \text{Number of blocks in the interval}$, i.e., 8000.

C2

Unequipped detection (dUNEQ) and VC AIS detection (dAIS) is performed on the incoming C2 byte. The expected C2 signal label can be written by the microprocessor at address 0x1f750 (0x1dcb0, 0x1dcb2, 0x1dcb4). If a mismatch occurs between the received C2 and the expected C2, a payload mismatch defect (dPLM) is declared.

The accepted C2 value is written to the on-chip RAM for retrieval by the microprocessor at address 0x1f738, (0x1dc60, 0x1dc64, 0x1dc68).

G1

A performance monitoring counter is provided for the path REI.

The G1 byte is monitored for the presence of single bit or enhanced path RDI.

H4

The H4 byte is written to the on-chip RAM for retrieval by the microprocessor. It can be optionally monitored for the V1/V2 multiframe in case the SPE/VC is substructured into low order VT/TUs, or the virtual concatenation multiframe in case high order virtual concatenation is active for this SPE/VC. The selection is made per high order path via the H4_MultiFrameType register (bits 1-0 at address 0x1f690 (0x1d910, 0x1d930, 0x1d950)).

| H4_MultiFrameType | |
|-------------------|---|
| 00 | Disable monitoring of H4 for VC-4/STS-3c SPE. |
| 01 | Monitor the V1/V2 multiframe for a VC-3/VC-4/STS-1 SPE substructured into low order VT/TUs. |
| 10 | Monitor the virtual concatenation multiframe. |
| 11 | Disable monitoring of H4 for VC-3/STS-1 SPE. |

F2, F3/Z3, K3/Z4, and N1/Z5

The F2, F3/Z3, K3/Z4, and N1/Z5 are written to the on-chip high order POH RAM for retrieval by the microprocessor.

HIGH ORDER POH PORT INTERFACE

All received high order POH bytes of all VC-3/STS-1 and VC-4/STS-3c are output on the receive High Order POH port interface.

The transmit High Order POH port interface allows inserting most high order POH byte into the VC-3/STS-1 and VC-4/STS-3c POH. J1 and C2 cannot be selected from the transmit HO POH port interface, while the B3 BIP-8 is used as error mask on the calculated BIP-8 for test purposes.

Each interface consists of clock, data, data enable, address and address enable lines.



The address is a 8-bit word with following format:

| A7-A6 | A5-A4 | A3 | A2 | A1 | A0 | |
|------------------|--------------------|----|----|----|----|-------|
| 00 (Reserved) | Channel Number | 0 | 0 | 0 | 0 | J1 |
| | 00 = VC-3/STS-1 #1 | 0 | 0 | 0 | 1 | B3 |
| | 01 = VC-3/STS-1 #2 | 0 | 0 | 1 | 0 | C2 |
| | 10 = VC-3/STS-1 #3 | 0 | 0 | 1 | 1 | G1 |
| | 11 = VC-4/STS-3c | 0 | 1 | 0 | 0 | F2 |
| | | 0 | 1 | 0 | 1 | H4 |
| | | 0 | 1 | 1 | 0 | F3/Z3 |
| | | 0 | 1 | 1 | 1 | K3/Z4 |
| | | 1 | 0 | 0 | 0 | N1/Z5 |

HIGH ORDER ALARM INDICATION PORT INTERFACE

The High Order Alarm Indication Port Interface transports the Remote Information (RI) from the VC-3/STS-1 and VC-4/STS-3c POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to insert by the POH generator.

The High Order POH monitor blocks multicast the Remote Information of all VC-3/STS-1 and VC-4/STS-3c channels to the High Order POH generator blocks and the Receive High Order Alarm Indication Port Interface.

The High Order POH generator blocks can select per VC-3/STS-1 and VC-4/STS-3c channel if the Remote Information is taken from the Transmit High Order Alarm Indication Port Interface or the internal Remote Information provided by the High Order POH monitor blocks.

Each interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the high order alarm indication port data frame.

Each high order alarm indication port data frame consists of 16 timeslots of 32 bits per timeslot:

| | | | | | | | | | | | | | | | | | |
|------------|----|----|-----|---|---|----|----|-----|---|---|-----|----|----|-----|---|-----|-----|
| Frame | X | | | | | | | | | | | | | | | X+1 | |
| TimeSlot | 0 | | | | | 1 | | | | | ... | 15 | | | | | ... |
| Bit Number | 31 | 30 | ... | 1 | 0 | 31 | 30 | ... | 1 | 0 | ... | 31 | 30 | ... | 1 | 0 | ... |

The first 12 time slots are assigned to VC-3/STS-1 Remote Information, the last 4 time slots to VC-4/STS-3c Remote Information:

| TimeSlot | Assigned to |
|----------|--------------------------|
| 0 | VC-3/STS-1 #1 |
| 1 | VC-3/STS-1 #2 |
| 2 | VC-3/STS-1 #3 |
| 3..11 | Reserved for VC-3/STS-1 |
| 12 | VC-4/STS-3c #1 |
| 13..15 | Reserved for VC-4/STS-3c |

Each 32-bit timeslot has a field for the REI and RDI. A valid flag indicates if the value in a field is valid and needs to be processed. Invalid values are ignored.

| Bit Number | Name | Description |
|------------|-----------|--|
| 31 | REI-valid | REI value in bits 30..27 is valid. |
| 30..27 | REI | REI value |
| 26 | Reserved | |
| 25 | RDI-valid | RDI values in bits 24..22 are valid |
| 24 | RDI-S | Enhanced RDI Server failure, contributes to single bit RDI |
| 23 | RDI-C | Enhanced RDI Connectivity failure, contributes to single bit RDI |
| 22 | RDI-P | Enhanced RDI Path failure |
| 21..4 | Reserved | |
| 3..0 | CRC-4 | CRC-4 over bits 31..4 |

AU-4 AND AU-3 POINTER GENERATION

The generation of the AU-4 and AU-3 pointer depends upon the timing mode selected for the Telecom bus interface (this mode is controlled by lead ABUST and register cTBADD).

Drop Bus Timing Mode

In Drop Bus timing mode the AU-4 (or AU-3) pointer bytes follow the drop DC1J1V1 pulses.

Add Bus Timing Mode 1

In Add Bus Timing Mode 1 (alias "add slave mode") the AU-4 (or AU-3) pointer bytes follow the pulses on input signal AC1J1V1.

The AC1J1V1 pulses (generated by external circuitry like the TranSwitch PHAST-3N) must correspond to a fixed pointer value (in other words, the distance between C1 pulse and J1 pulse must be fixed). Any fixed value is acceptable.

Note that the EtherMap-3 Plus does NOT insert the H1 H2 byte value on the AD leads. It must be inserted by the external circuitry (like the PHAST-3N).

Add Bus Timing Mode 2

In Add Bus Timing Mode 2 (alias "add master mode") the AU-4 (or AU-3) pointer bytes are fixed at 0.

Note that the EtherMap-3 *Plus* does NOT insert the H1 H2 byte value on the AD leads. It must be inserted by external circuitry (like the PHAST-3N).

TU-3 POINTER GENERATION

In all the timing modes, the TU-3 pointer has a fixed value of 595. Also, the EtherMap-3 *Plus* inserts the TU-3 byte value on the AD leads.

TU-3 POINTER TRACKING

The incoming negative and positive TU-3 pointer adjustments are counted for performance monitoring.

The LOP and Pointer AIS defects are detected.

VC-3/STS-1/TUG-3 TIMESLOT INTERCHANGE

In each direction the VC-3/STS-1/TUG-3 timeslots can be interchanged. Each TSI output VC-3/STS-1/TUG-3 timeslot can be configured to connect to any TSI input timeslot (SourceSlot) or to send an unequipped (ForceUneq) or AIS (ForceAIS) signal.

VT/TU POINTER TRACKING

The incoming negative and positive pointer adjustments are counted for performance monitoring.

The LOP and Pointer AIS defects are detected.

The V1, V2, and V4 bytes are written to the on-chip RAM for retrieval by the microprocessor (V1 RAM at 0x1cf00, V2 RAM at 0x1c000, V4 RAM at 0x1c200).

VT/TU POINTER GENERATION

The VT1.5/TU-11 pointer has a fixed value selectable between 0 and 78. The VC-12/TU-12 pointer has a fixed value selectable between 0 and 105. The pointer value of 0 is selected via registers PointerValueZero, bit 0 at address 0x13d00+channel, and PointerZeroValue, bit 1 at address 0x1a800+4(decimal)*channel. For each channel both registers need to correspond.

The V4 byte for each low order timeslot can be written by the microprocessor at address 0x1a000+channel.

LOW ORDER TIMESLOT INTERCHANGE

In each direction the low order timeslots can be interchanged. Each low order TSI output timeslot can be configured to connect to any TSI input timeslot within the same high order container. This means it is not possible to connect timeslots between AU-3/STS-1's. Unequipped or AIS signals need to be generated via the low order POH generator.

Cross connects are made by writing the appropriate value into the MAPRAM_data cross connect map. This array of 84 elements is indexed by the output channel number, its value represents the input channel number to be connected to this output channel.

The cross connect map consists of two banks of 84 elements. The cross connect hardware reads the information from the active bank, while the software can only write to the inactive bank. When a new configuration is written to the inactive bank, both banks can be swapped.

Software can select which of the banks is visible for reading.

| Rx TSI | Tx TSI | Description |
|---|---------------------------------------|---|
| UseDefaultMapping | | When set, the cross connect map is disabled: each klm output timeslot is connected to the corresponding klm input timeslot. |
| 0x1c672, bit 1 | 0x1a400, bit 1 | |
| MAPRAM_data | | Cross connect map. Disabled if UseDefault-Mapping is set. |
| 0x1c400 | 0x1a600 | |
| Active_MAPRAM_Bank_ID 0x1c672, bit 2 | UpperMAPRAMValid 0x1a400, bit 2 | Selects the active MAPRAM bank: hardware reads from the active bank, software writes to the inactive bank. |
| Bank_ID_MAPRAM 0x1c674, bit 0 | ReadUpperMAPRAMBank 0x1a400, bit 3 | Selects the MAPRAM bank visible for reading by software. |

TRANSMIT LOW ORDER PATH TERMINATION (Low Order POH Generator)

General

The EtherMap-3 Plus provides transmit low order path termination functions for up to 84 VT1.5-SPE/VC-11s or 63 VT2-SPE/VC-12s. The Low Order POH generators are numbered according to the klm numbering:

$$\text{Channel} = (k-1)*28+(l-1)*4+(m-1)$$

| Channel | Assigned to low order #klm |
|---------|----------------------------|
| 0 | VT1.5/VT2/VC-11/VC-12 #111 |
| 1 | VT1.5/VT2/VC-11/VC-12 #112 |
| 2 | VT1.5/VT2/VC-11/VC-12 #113 |
| 3 | VT1.5/VC-11 #114 |
| 4 | VT1.5/VT2/VC-11/VC-12 #121 |
| ... | ... |
| 82 | VT1.5/VT2/VC-11/VC-12 #373 |
| 83 | VT1.5/VC-11 #374 |

J2

The J2 path trace can be written by the microprocessor for transmission as a 16 byte long repeating message in the Transmit Low Order POH Ram at address 0x1b000+16(decimal)*channel. This 16 byte frame is identical to the 16 byte frame of the J0. The MSB of byte 1 should be set to 1 and is the trace identifier frame alignment signal.

BIP-2

The V5 BIP-2 is calculated and transmitted for each VT/VC.

For test purposes the EtherMap-3 Plus supports a BIP-2 error mask in the Transmit Low Order POH RAM, at address 0x1b000. When the BIP2_Error register, bit 0 at address 0x1a800+4(decimal)*channel, is set, the calculated BIP-2 is exor'ed with the BIP-2 error mask before being inserted into the V5 byte.



Signal Label

Both the V5 signal label (in the transmit Low Order POH RAM at address 0x1b000) and the K4/Z7 extended signal label (Ext_SignalLabel register at address 0x1a802+4(decimal)*channel) can be written by the microprocessor for transmission.

The V5 signal label must be set to '101' to activate the generation of the K4/Z7 bit 1 MFAS and Extended Signal Label.

The EtherMap-3 Plus also has the option to source an unequipped signal or a supervisory unequipped VT/VC through the SendUneq and UneqSelect registers at address 0x1a800+4(decimal)*channel.

| SendUneq bit 3 | UneqSelect bit 4 | Description |
|----------------|------------------|---------------------------------------|
| 0 | X | Source an equipped VT/VC. |
| 1 | 0 | Source an unequipped VT/VC. |
| 1 | 1 | Source a supervisory unequipped VT/VC |

REI/RDI

The received V5 BIP-2 errors are automatically inserted into the V5 path REI. The EtherMap-3 Plus has an option to transmit either a single bit V5 path RDI or an enhanced 4-bit V5/K4/Z7 path RDI. To enable the 4-bit enhanced path RDI, the Low Order POH generation, per VT/VC needs to be configured to 3-bit RDI mode. The transmitted REI/RDI can be generated from local alarm conditions or derived from the Alarm Indication Port Interface. When the uni-directional option is active, all transmitted remote information is set to zero.

K4/Z7 Bit 2

The K4/Z7 bit 2 can be written by the microprocessor or by the High Order POH port interface for transmission, or it can be selected to carry the virtual concatenation multiframe and control packets in case low order virtual concatenation is active for this VT/VC. In the latter case, the extended signal label in K4/Z7 bit 1 has to be activated to generate the MFAS word (see Signal Label above).

The source for the K4/Z7 bit 2 can be selected per low order channel through register LO_VC_Source, bits 7-6 at address 0x1a804+4(decimal)*channel.

| bit 7 | bit 6 | LO_VC_Source |
|-------|-------|---|
| 0 | 0 | Insert K4/Z7 bit 2 from the POH RAM. |
| 0 | 1 | Insert K4/Z7 bit 2 from the High Order POH port. |
| 1 | 0 | Reserved |
| 1 | 1 | Pass the multiframe and control word for a virtual concatenated VT1.5-SPE/VT2-SPE/VC-11/VC-12 |

V5 RFI

The V5 RFI bit can be written by the microprocessor for transmission. This value is static and is not acted upon by the EtherMap-3 Plus transmit logic.

N2/Z6

The N2/Z6 byte can be written by the microprocessor or by the Low Order POH port interface for transmission. This value is static and is not acted upon by the EtherMap-3 Plus transmit logic.

RECEIVE LOW ORDER PATH TERMINATION (Low Order POH Monitor)**General**

The EtherMap-3 *Plus* provides receive low order path termination functions for up to 84 VT1.5-SPEs/VC-11s or 63 VT2-SPEs/VC-12s. Like the low order POH generators, the low order POH monitors are numbered according to the klm numbering:

$$\text{Channel} = (k-1)*28+(l-1)*4+(m-1)$$

The received POH bytes are always forwarded to the receive Low Order POH Port interface and written to the receive low order POH RAM at address $0x17800+4(\text{decimal})*\text{channel}$.

J2

The EtherMap-3 *Plus* supports 16 byte J2 trace messages. The received J2 path trace message can be compared with a microprocessor written expected J2 path trace at address $0x16000+16(\text{decimal})*\text{channel}$. If a mismatch occurs between received and expected J2 path trace, a trace identifier mismatch defect (dTIM) is declared. An all-zero path trace is also reported to allow detection of an unequipped signal versus a supervisory unequipped signal.

The microprocessor can retrieve the value of the received J2 path trace of one low order path termination at a time.

| Address | Register | Description |
|-------------------|-------------------|--|
| 0x14980 | | Accepted 16 byte Trace Message |
| 0x14800, bit 8 | J2_Report_Enable | Enable reporting of the accepted J2 trace message for the J2_Report_Channel. |
| 0x14802, bit 15-9 | J2_Report_Channel | Select the VT/VC channel for which the J2 accepted trace message is retrieved. |
| 0x148c0, bit 0 | J2_Stable_1 | A constantly repeating single J2 byte has been detected. |
| 0x148c0, bit 1 | J2_Stable_16 | A 16-byte J2 trace message has been detected. |

The number of trace message multiframes to set or reset the TIM Defect is configurable via registers J2_NrOfFramesToSetTim (bits 3-0 at address 0x14802) and J2_NrOfFramesToResetTim (bits 7-4 at address 0x14802).

BIP-2

Performance monitor counters are provided for the V5 BIP-2 errors and V5 BIP-2 block errors.

Optionally the burst error degraded signal defect can be detected. The threshold values and interval times are configurable per low order path via registers BIP2_DEG_SetThresHold, BIP2_DEG_ClearThreshold, BIP2_DEG_SetNrOfIntervals and BIP2_DEG_ClearNrOfIntervals at address $0x17c04-0x17c06 (+ 4*\text{channel})$.

The Signal Degrad registers pertain to the detection of the degraded signal defect, assuming a bursty distribution of errors, as in 6.2.3.1.2/G.806. Above registers correspond to the DEGTHR and DEGM settings referred to by 6.2.3.1.2/G.806. The EtherMap-3 *Plus* does not detect "Excessive error" (Excessive error assumes a Poisson distribution of errors, as in 6.2.3.1.1/G.806).

The detection algorithms assuming bursty distribution uses the one second block error counts for performance monitoring. The one second clock ONESEC (see [page 43](#)), is required.



The degraded signal defect (dDEG) is declared if BIP2_DEG_SetNrOfIntervals consecutive bad intervals (interval is the one second period used for performance monitoring) are detected. An interval is declared bad if the number of errored blocks in that interval \geq Degraded Threshold (BIP2_DEG_SetThresHold).

The degraded signal defect is cleared if BIP2_DEG_ClearNrOfIntervals consecutive good intervals are detected. An interval is declared good if the number of errored blocks in that interval $<$ BIP2_DEG_ClearThreshold.

The parameters BIP2_DEG_SetNrOfIntervals and BIP2_DEG_ClearNrOfIntervals are provisionable in the range 2 to 10.

The DEGTHR parameters BIP2_DEG_SetThresHold and BIP2_DEG_ClearThreshold are to be provisioned as a number of errored blocks in the range of $0 < \text{DEGTHR} \leq$ Number of blocks in the interval, i.e., 2000.

Signal Label

Unequipped detection (dUNEQ) and VC AIS detection (dAIS) is performed on the incoming V5 signal label. The expected V5 signal label and the expected K4/Z7 extended signal label can be written by the microprocessor. If a mismatch occurs between the received and the expected (extended) signal label, a payload mismatch defect (dPLM) is declared.

The accepted V5 signal label and K4/Z7 extended signal label values are written to the on-chip RAM for retrieval by the microprocessor.

| Address | Register | Description |
|----------------------------|---------------|---|
| 0x14000+4(decimal)*channel | TSL_Accepted | Accepted V5 trail signal label. |
| 0x14002+4(decimal)*channel | ETSL_Accepted | Accepted K4/Z7 extended trail signal label. |
| 0x14400+4(decimal)*channel | TSL_Expected | Expected V5 trail signal label. |
| 0x14402+4(decimal)*channel | ETSL_Expected | Expected K4/Z7 extended trail signal label. |

The number of (multi-)frames to accept a TSL or Extended TSL value is configurable via registers TSL_NrOfIntervals (bits 10-7 at address 0x14800) and ETSL_NrOfIntervals (bits 14-11 at address 0x14800).

REI/RDI/RFI

A performance monitoring counter is provided for the path REI.

The V5/K4/Z7 bytes are monitored for the presence of single bit or enhanced path RDI.

The V5 byte is monitored for the presence of RFI

K4/Z7 Bit 2

The K4/Z7 bit 2 can be optionally monitored for the virtual concatenation multiframe in case lower order virtual concatenation is active for this SPE/VC.

N2/Z6

The N2/Z6 byte is written to the on-chip RAM for retrieval by the microprocessor.

LOW ORDER AND HIGH ORDER PATH MONITOR ALARM REGISTERS

This paragraph gives explanation of the different alarm registers available for the low order and high order POH monitors. (LODMP_POHMONITOR, T_VCI_RX_VCX_POH), as well as the performance/fault monitoring feature of EtherMap-3 Plus.

Also, this explanation completes Tables 137 to 151 and Tables 188 to 199.

1. CHANNEL DEFECTS (Channel_Defects_record):

Each bit in this array indicates in real time an alarm detected in the received POH Referring to ITU G.783, G.806, these alarms are the detected defects: dUNEQ, dTIM, dTTIZERO. None of these defects are inhibited by another one. This type of record allows the user to monitor the real time alarms, disregarding the alarm inhibitions.

2. DEFECT CORRELATIONS UNLATCHED (Channel_Defect_Correlations_Unlatched):

For these alarms, defect inhibitions are taken into account. A specific alarm is asserted only if higher order alarm are not present, this is expressed in ITU G.783 and G.806, in equations like this one:

$$cUNEQ = dUNEQ \text{ and (not } CI_SSF) \text{ and dTTIZERO and dTIM}$$

$$cTIM = dTIM \text{ and (not } CI_SSF) \text{ and (not (dUNEQ and dTTIZERO))}$$

The inhibitions of one alarm by another can also be configured. The configuration record to do this for the LODMP_POHMONITOR is LODMP_POHMONITOR_Defect_Correlations_Config. The configuration is common for all the LO channels.

Example. when UNEQ_SSF_Inhibit_Disable = TRUE then the expression for cUNEQ becomes:

$$cUNEQ = dUNEQ \text{ and dTtiZero and dTIM}$$

3. DEFECT CORRELATIONS LATCHED (Channel_Defect_Correlations_LatchForInt):

These are the same as 2. above, but latched. These registers are read only and clear when read. A latched bit can be cleared by writing a one (1) to that bit; writing a zero (0) has no effect.

4. MASK (Channel_Defect_Correlations_Mask):

Each bit in this array is associated with a latched alarm; each bit will prevent its corresponding alarm from generating an interrupt.

5. DEFECT CORRELATIONS LATCHED for PM, FM (Channel_Defect_Correlations_LatchForPMFM)

These are the same as 3. above, but latched for PM and FM. These registers are read only and are cleared on each one second boundary (not cleared on read). They can also be cleared by writing a zero (0) to each bit; writing a one (1) has no effect.

6. PERFORMANCE MONITORING (PM) (Channel_Defect_Correlations_PM):

This is a latched alarm indicating that an alarm has occurred over the immediately preceding 1 second interval. Only cleared on each one second boundary.

7. FAULT MONITORING (FM) (Channel_Defect_Correlations_FM):

This is a latched alarm indicating that the unlatched alarm was continuously asserted, without any alarm events taking place, over the full duration of the immediately preceding 1 second interval. Only cleared on each one second boundary.

Additional explanation about 6 and 7 (USE OF THE ONESEC CLOCK):

The one second clock defines one second time intervals to serve as a time reference for the PM/FM scheme. Purpose of Performance and Fault Monitoring (PM and FM): an Unlatched Alarm may have associated with it a corresponding PM/FM feature, that allows a System to monitor the long term evolution of the particular alarm, in a convenient manner. As an example, a System may wish to monitor if a defect occurred over only a single unit time interval, or, if the defect persisted over several unit time intervals with respect to a certain particular alarm, or a group of alarms. The unit time interval may be 1 second, or any other, as laid down by applicable standards (if any), or as required to implement a specified Performance and Fault Monitoring System.

8. DEFECT CORRELATIONS CONFIGURATION (Channel_Defect_Correlations_Config of type):

This configures the way the defects are inhibited in point 2:

E.g., the inhibition expression `cDEG <- dDEG and (not dTIM) and (not CI_SSF)` can have each contribution disabled separately.

The Channel_Defect_Correlations_Config registers are called `<defect>_<inhibitor>_Inhibit_Disable`. This means there is a term `'and (not <inhibitor>')` in the correlation for `<defect>`.

- When cleared the inhibition of `<defect>` by the term with `<inhibitor>` is enabled (=default).
- When set the inhibition of `<defect>` by the term with `<inhibitor>` is disabled.

Example: `cDEG` has the `DEG_SSF_Inhibit_Disable` and the `DEG_TIM_Inhibit_Disable` associated:

```
cDEG <- dDEG
and ((not dTIM) or DEG_TIM_Inhibit_Disable)
and ((not CI_SSF) or DEG_SSF_Inhibit_Disable)
```

9. DEFECT CORRELATIONS SUMMARY (Defect_Correlations_Summary):

- LatchForInt: for every channel, this bit is the or-reduce of the DEFECT_CORRELATIONS_LATCHED bits combined with the MASK bits for that channel. (Bit-wise masking happens before or-reducing).
- PM: for every channel, this bit is the or-reduce of the PM bits for that channel.
- FM: for every channel, this bit is the or-reduce of the FM bits for that channel.

10. Array `LODMP_POHMONITOR_Defect_Correlations_Summary_Mask` has the same function as MASK, and is associated with the LatchForInt bit in the `LODMP_POHMONITOR_Defect_Correlations_Summary` array. Note that every channel has 1 Summary_Mask bit.

11. LODMP_POHMONITOR_Defect_Correlations_GroupSummary

- Interrupt: this bit is the or-reduce of the LatchForInt bits of `LODMP_POHMONITOR_Defect_Correlations_Summary` combined with the Masks from `LODMP_POHMONITOR_Defect_Correlations_Summary_Mask`. (Masking happens before or-reducing) This bit is equal to the interrupt generated by the block.
- PM: the or-reduce of the PM bits for all channels in the `LODMP_POHMONITOR_Defect_Correlations_Summary`
- FM: the or-reduce of the FM bits for all channels in the `LODMP_POHMONITOR_Defect_Correlations_Summary`

LOW ORDER POH PORT INTERFACE

All received low order POH bytes of all 63/84 timeslots are output on the receive Low Order POH port interface.

The transmit Low Order POH port interface allows inserting most low order POH fields into the low order POH. The V5 BIP-2 field is used as error mask on the calculated BIP-2 for test purposes.

Per low order channel and per POH field the low order POH Port Interface can be selected as the source of that field. If a POH byte transports multiple fields, each field can be selected independently.

| Address | Bits | Register | Description |
|----------------------------|-------|----------------|--|
| 0x1a804+4(decimal)*channel | 1-0 | REI_Source | Set to '01' to insert the REI (V5 bit 3) field from the POH port |
| | 3-2 | RDI_Source | Set to '01' to insert the RDI (V5 bit 8 and K4/Z7 bits 5-7) field from the POH port |
| | 5-4 | Ext_TSL_Source | Set to '01' to insert the Extended TSL field (K4/Z7 bit 1) from the POH port |
| | 7-6 | LO_VC_Source | Set to '01' to insert the Low Order Virtual Concatenation control word field (K4/Z7 bit 2) from the POH port |
| | 9-8 | APS_Source | Set to '01' to insert the APS field (K4/Z7 bits 3-4) from the POH port |
| | 11-10 | DL_Source | Set to '01' to insert the Data Link field (K4/Z7 bit 8) from the POH port |
| 0x1a806+4(decimal)*channel | 1-0 | J2_Source | Set to '01' to insert the J2 byte from the POH port |
| | 3-2 | N2_Source | Set to '01' to insert the N2/Z6 byte from the POH port |

Each interface consists of clock, data, data enable, address and address enable lines.

The address is a 12-bit word with following format:

| A11-A9 | A8-A2 | A1 | A0 | |
|-------------------|----------------------------------|----|----|-------|
| 000 (Reserved) | TimeSlot Number (range 0..83) | 0 | 0 | V5 |
| | | 0 | 1 | J2 |
| | | 1 | 0 | N2/Z6 |
| | | 1 | 1 | K4/Z7 |

The low order time slots are numbered according to the klm numbering: $TimeSlot = (k-1)*28+(l-1)*4+(m-1)$

| TimeSlot | Assigned to low order #klm |
|----------|----------------------------|
| 0 | VT1.5/VT2/VC-11/VC-12 #111 |
| 1 | VT1.5/VT2/VC-11/VC-12 #112 |
| 2 | VT1.5/VT2/VC-11/VC-12 #113 |
| 3 | VT1.5/VC-11 #114 |
| 4 | VT1.5/VT2/VC-11/VC-12 #121 |
| ... | ... |
| 82 | VT1.5/VT2/VC-11/VC-12 #373 |
| 83 | VT1.5/VC-11 #374 |



LOW ORDER ALARM INDICATION PORT INTERFACE

The Low Order Alarm Indication Port Interface transports the Remote Information (RI) from the Low Order POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to insert by the POH generator.

The Low Order POH monitor blocks multicast the Remote Information of all Low Order channels to the Low Order POH generator blocks and the Receive Low Order Alarm Indication Port Interface.

The Low Order POH generator blocks can select per Low Order channel if the Remote Information is taken from the Transmit Low Order Alarm Indication Port Interface or the internal Remote Information provided by the Low Order POH monitor blocks.

Each interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the low order alarm indication port data frame.

Each low order alarm indication port data frame consists of 84 timeslots of 16 bits per timeslot:

| | | | | | | | | | | | | | | | | | |
|------------|----|----|-----|---|---|----|----|-----|-----|----|-----|----|----|-----|---|-----|-----|
| Frame | X | | | | | | | | | | | | | | | X+1 | |
| TimeSlot | 0 | | | | 1 | | | | ... | 83 | | | | ... | | | |
| Bit Number | 15 | 14 | ... | 1 | 0 | 15 | 14 | ... | 1 | 0 | ... | 15 | 14 | ... | 1 | 0 | ... |

The low order time slots are numbered according to the klm numbering: $TimeSlot = (k-1)*28+(l-1)*4+(m-1)$

| TimeSlot | Assigned to low order #klm |
|----------|----------------------------|
| 0 | VT1.5/VT2/VC-11/VC-12 #111 |
| 1 | VT1.5/VT2/VC-11/VC-12 #112 |
| 2 | VT1.5/VT2/VC-11/VC-12 #113 |
| 3 | VT1.5/VC-11 #114 |
| 4 | VT1.5/VT2/VC-11/VC-12 #121 |
| ... | ... |
| 82 | VT1.5/VT2/VC-11/VC-12 #373 |
| 83 | VT1.5/VC-11 #374 |

Each 16-bit timeslot has a field for the REI and RDI. A valid flag indicates if the value in a field is valid and needs to be processed. Invalid values are ignored.

| Bit Number | Name | Description |
|------------|-----------|--|
| 15 | REI-valid | REI value in bit 14 is valid. |
| 14 | REI | REI value |
| 13 | RDI-valid | RDI values in bits 12..10 are valid |
| 12 | RDI-S | Enhanced RDI Server failure, contributes to single bit RDI |
| 11 | RDI-C | Enhanced RDI Connectivity failure, contributes to single bit RDI |
| 10 | RDI-P | Enhanced RDI Path failure |
| 9..4 | Reserved | |
| 3..0 | CRC-4 | CRC-4 over bits 15..4 |

SONET/SDH PROTECTION SWITCHING RECOVERY TIME

A typical, EtherMap-3 Plus standards-compliant ADM in Unidirectional Path Switched Ring (UPSR) mode sends a tributary payload in both directions around the ring and receives from one of the two paths. If errors or a failure occur on the chosen receive path, the ADM switches over to the other path to resume communication. The SONET/SDH required restoration time of each HO or LO path from the detection of a failure is 50 milliseconds or less. The detection time requirement varies depending on the line rate and the bit error rate. SONET/SDH paths are assumed to be restored when the POH bytes and pointers have no detected errors (e.g., LOP or AIS). H4 and K4 multiframe alignment and sequence numbers are not included. UPSR switching times are typically shorter due to the fact that the switch decisions are made only at the receiving ADM(s). For BLSR, ADM to ADM communication via the K1/K2 bytes is required to perform the switch.

Table 3 below lists the functions and the times required in presenting a new signal to one or more paths used to carry an Ethernet payload in the EtherMap-3 Plus.

Table 3: SONET/SDH Protection Switching Recovery Time

| Mode | Total Delay | See Note: |
|------------|----------------------------|-----------|
| HO wo/VCAT | SONET/SDH + 0.5 msec. | 1 |
| LO wo/VCAT | SONET/SDH + 2.0 msec. | 1 |
| HO w/VCAT | SONET/SDH + Pda + 12 msec. | 1,2 |
| LO w/VCAT | SONET/SDH + Pda + 72 msec. | 1,2,3 |

Notes:

1. SONET/SDH = Basic SONET/SDH Line and individual Paths restoration time after a protection switch (i.e., which does not include the individual Paths differential delay compensation time within a virtual concatenation group).
2. Pda = Maximum Path Difference.
3. The time listed assumes that the new path is initiated as the result of a selection made on-chip (e.g., changing to an idle LO path or a microprocessor triggered reset of a path). If the path is switched external to the device and the new path only exhibits possibly an NDF and new K4 (e.g., due to a Signal Degrade condition), the standards require a K4 detection of the failure which can add up to 70 msec or more to the listed value.

The EtherMap-3 Plus adds very little delay to HO paths in VCAT mode and will achieve the desired 50 millisecond switchover times in UPSR applications where differential path delays are small. LO VCAT applications will experience more unavailability time during a switchover, but no more than the standards dictate. The main reason for additional delays is that both detection and restoration may only be observable via the K4 bytes in each LO path, for example, a single LO path with a VCAT group carried by a high order path experiencing a Signal Degrade. Only a new K4 multiframe sequence would be presented to the EtherMap-3 Plus. Shorter unavailability times are possible with VCAT and LCAS, but the target ADMs must support unprotected or Non-preemptable Unprotected Traffic (NUT) and the end customers must accept reduced bandwidth during failures.

VIRTUAL CONCATENATION AND LCAS

The EtherMap-3 Plus device takes a contiguous piece of Ethernet bandwidth and breaks it up into a number of individual SPE/VC which travel independently through the SONET/SDH network and are reassembled at their destination back into the contiguous piece of Ethernet bandwidth. The EtherMap-3 Plus also performs the converse, by taking the SPE/VC that it has received from a sending device and reassembling it back into a contiguous piece of Ethernet bandwidth.

Two tremendous advantages are immediately obvious:

- 1) Since the Ethernet traffic is traveling through the network in a standard size SPE/VC only the equipment at the end points needs to be changed.
- 2) Granularity of bandwidth used can be variable and in increments of the SPE/VC that is used. This is useful for the transport of payloads, such as Ethernet, which do not efficiently fit into one of the standard SPE/VC.

The EtherMap-3 Plus device also supports LCAS (Link Capacity Adjustment Scheme). This is a mechanism where the allocated bandwidth for an Ethernet link can be dynamically reconfigured without causing any hits on to the existing traffic flow.

The sections below describe in greater detail how the EtherMap-3 Plus performs virtual concatenation.

LOW ORDER VIRTUAL CONCATENATION WITHOUT LCAS

Ethernet traffic is transported in low order VT1.5-Xv-SPE/VC-11-Xv or VT2-Xv-SPE/VC-12-Xv virtual concatenation groups as follows:

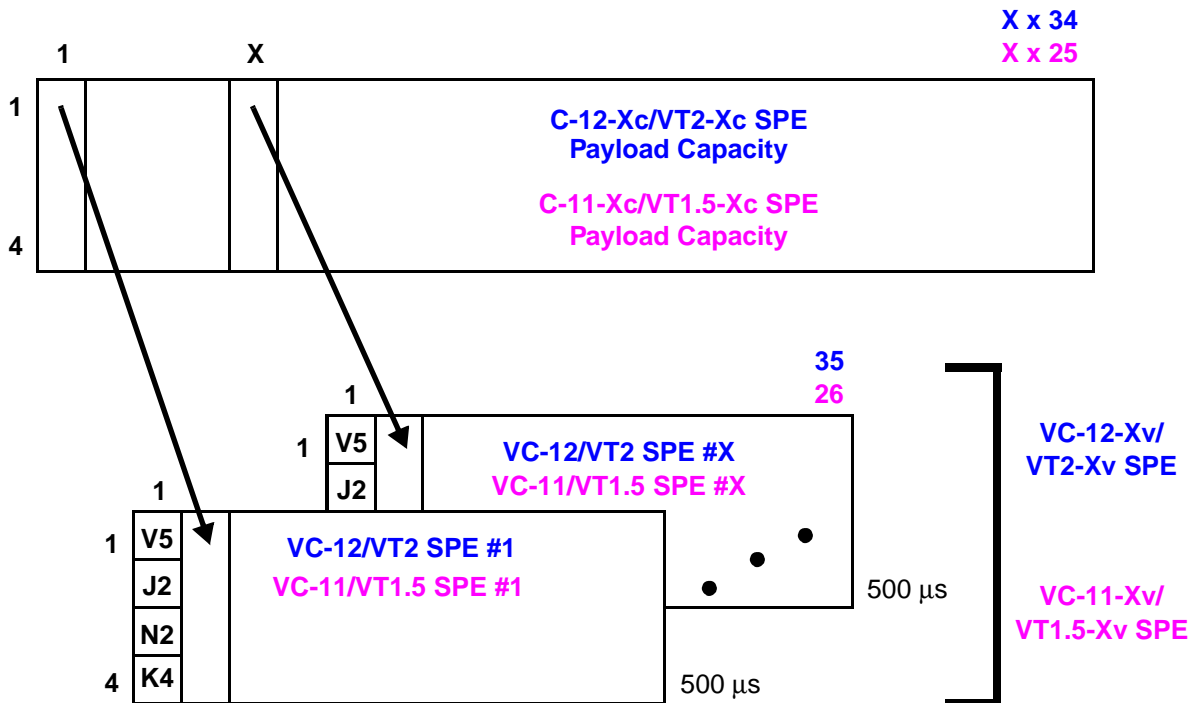


Figure 42. VT1.5-Xv-SPE Structure

The payload capacity consists of Ethernet traffic which has been encapsulated in one of four ways: GFP, LAPS, LAPF or PPP. More will be said about these encapsulation methods in following sections.

In SDH mode Ethernet traffic can also be transported in VC-3-Xv as shown in Figure 49. Note, a VC-3 is considered high order if carried in an AU-3, and low order if carried in a TUG-3; in this case the VC-3s are mapped to a TUG-3 as shown in Figure 44. Also note that the EtherMap-3 Plus has the capability to map the VC-3s to either a TUG-3 or AU-3.

Once the EtherMap-3 Plus has broken up the Ethernet payload into VT2-SPE/VC-12 or VT1.5-SPE/VC-11 they are then multiplexed into their respective SDH or SONET frame structures as shown below.

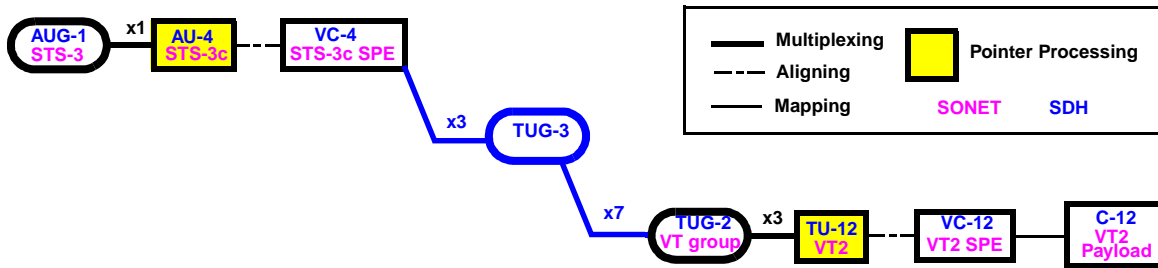


Figure 43. LO SDH Multiplexing Structure 1 Supported by the EtherMap-3 Plus

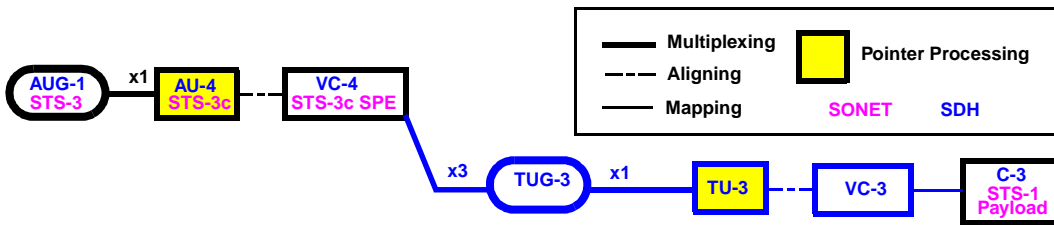


Figure 44. LO SDH Multiplexing Structure 3 Supported by the EtherMap-3 Plus

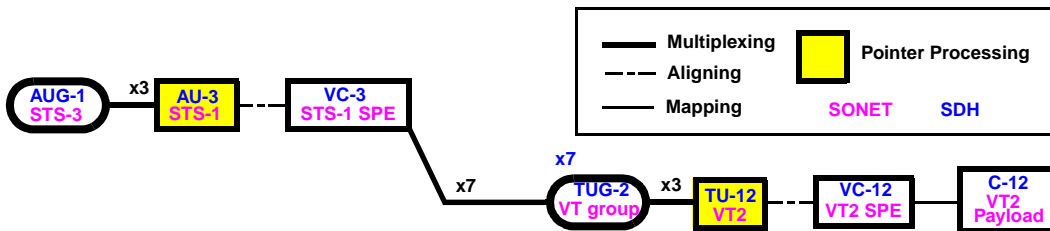


Figure 45. LO SDH Multiplexing Structure 2 Supported by the EtherMap-3 Plus

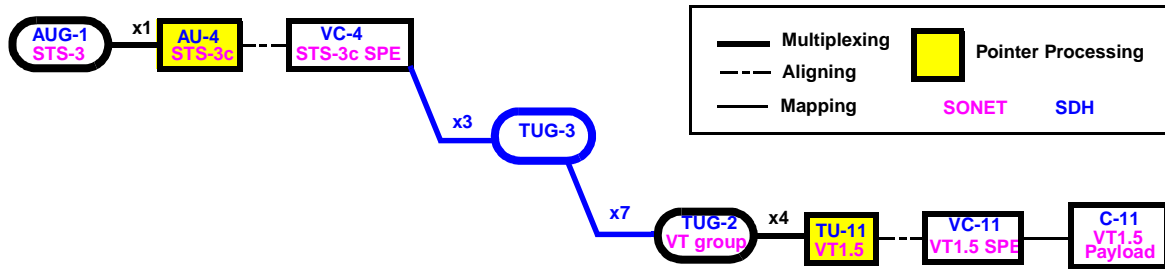


Figure 46. LO SDH Multiplexing Structure 4 Supported by the EtherMap-3 Plus

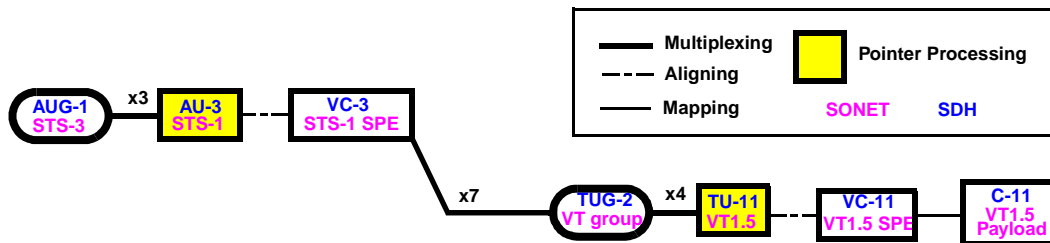


Figure 47. LO SONET Multiplexing Structure Supported by the EtherMap-3 Plus

LOW ORDER VIRTUAL CONCATENATION WITH LCAS

When using low order virtual concatenation in SONET/SDH mode, every low order virtual concatenation group (VCG) can be independently optionally configured to operate in LCAS mode. Note, low order virtual concatenation can be used without LCAS, but LCAS requires virtual concatenation. The low order virtual concatenation LCAS Control packet definition and format is specified in the ITU-T G.707/Y.1322 standard. The LCAS protocol is specified in the ITU-T G.7042/Y.1305 standard.

The LCAS Control packet is resident in the K4/Z7 [Bit 2] POH byte.

During initialization/normal operation, the EtherMap-3 Plus device provides support for management and re-allocation of member resources between LCAS and non-LCAS modes for use by multiple low order VCGs. In addition, general add and remove operations are supported using single high level messages.

In the transmit direction, for every member of a low order VCG operating in LCAS mode, the EtherMap-3 Plus device provides for individual source side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- PRBS generation for the Group Identification (GID) bit field.
- CRC-3 generation.
- LCAS Sequence Indicator (SQ) field generation.
- LCAS Control (CTRL) field generation.
- Inter-member messages during add/remove operations.
- For each transmit low order VCG in LCAS mode, selection of a high/low order member, in the receive direction, that is carrying the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Termination of MST and RS-Ack information from respective sink side LCAS state machine.
- Configurable low order per-member and per-VCG time-out counters for detection of failure during add and remove operations.
- Alarm generation to indicate LCAS source side state machine status.

In the receive direction, for every member of a low order VCG operating in LCAS mode, the EtherMap-3 Plus device provides for individual sink side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- Group Identification (GID) field mismatch detection.
- CRC-3 check.
- LCAS Sequence Indicator (SQ) field processing.
- LCAS Control (CTRL) field processing.
- Generation of MST and RS-Ack status information.
- Detection and processing of Trail Signal Fail (TSF) conditions.
- For each receive low order VCG in LCAS mode, selection of a transmit side high/low order VCG that is used to transport the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Alarm generation to indicate LCAS sink side state machine status.

HIGH ORDER VIRTUAL CONCATENATION WITHOUT LCAS

In SONET mode Ethernet traffic is transported in STS-1-Xv-SPE or in a STS-3c-SPE. The STS-1-Xv-SPE structure is shown in the figure below. The STS-1-Xv-SPE payload capacity or the STS-3c-SPE data consists of Ethernet traffic which has been encapsulated in one of four ways: GFP, LAPS, LAPF or PPP.

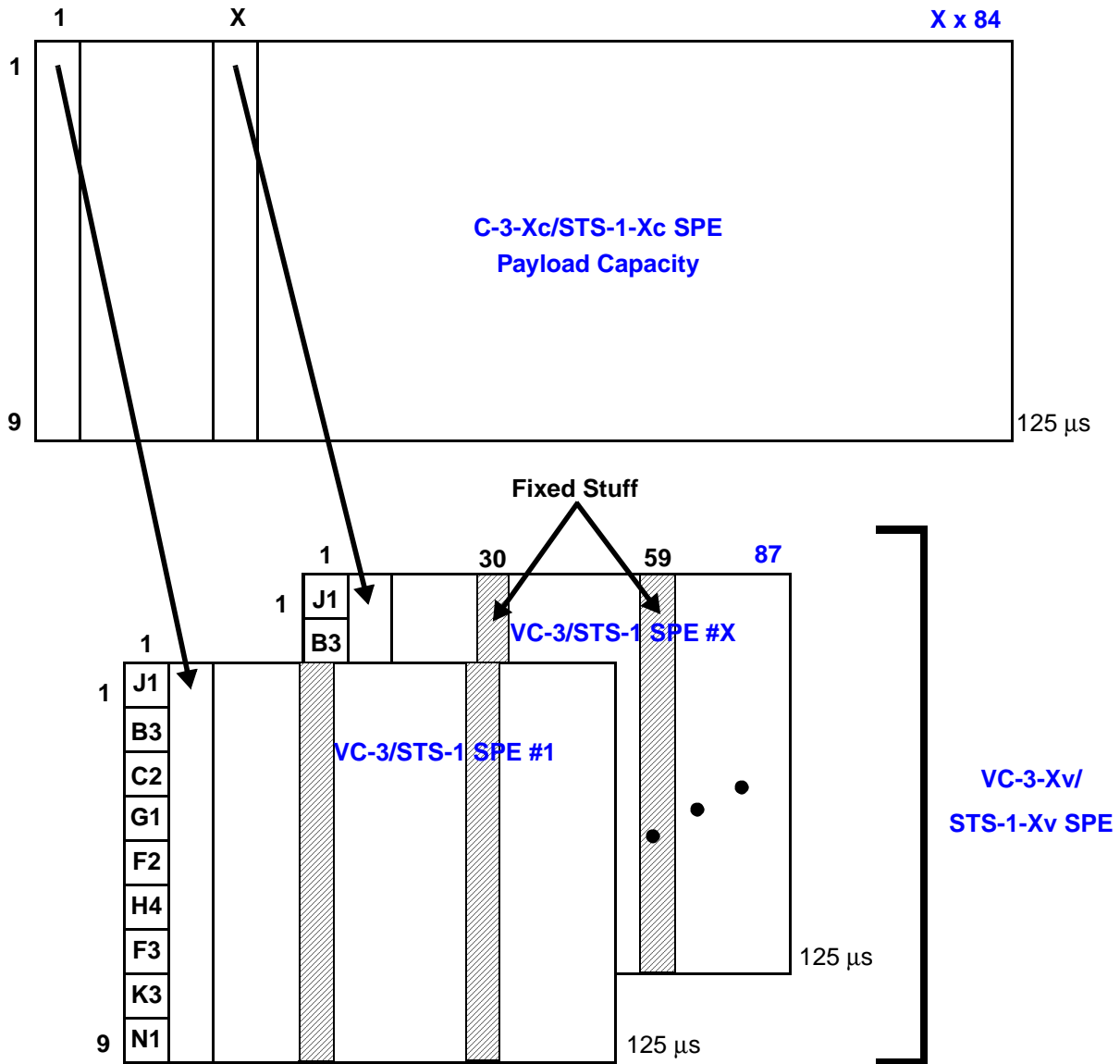


Figure 48. High Order STS-1-Xv-SPE/VC-3-Xv Structure

In SDH mode Ethernet traffic is transported in VC-3-Xv or in VC-4. Just like for the STS-1-Xv-SPE payload capacity the payload capacity for the VC-3-Xv and VC-4 consists of Ethernet traffic which has been encapsulated in one of four ways: GFP, LAPS, LAPF or PPP. The VC-3-Xv structure is shown below. Note, a VC-3 is considered high order as long as it is not carried in a TUG-3.

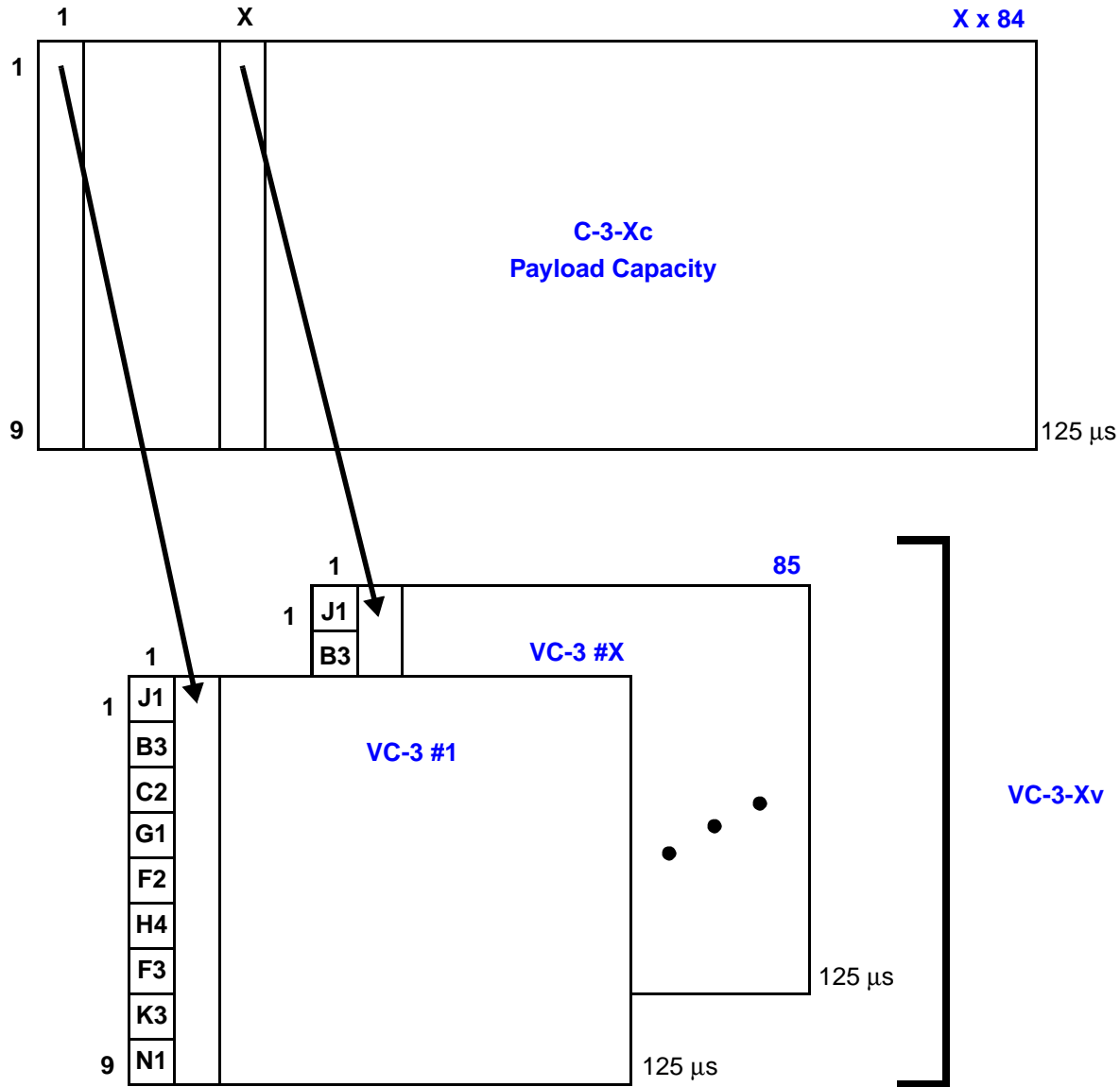


Figure 49. Low Order VC-3-Xv Structure

Once the EtherMap-3 Plus has broken up the Ethernet payload into VC-3 or STS-1-SPE they are then multiplexed into their respective SDH or SONET frame structures as shown below. Notice that for the VC-3 structure that no stuff columns exist. However, when inserted into the AU-3, stuff columns are added so that the VC-3 ends up resembling an STS-1-SPE.

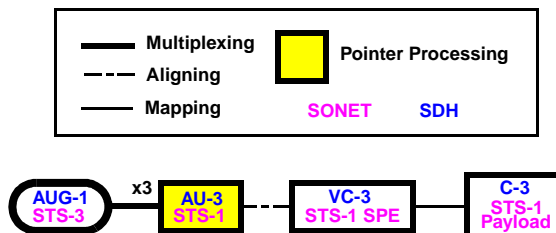


Figure 50. HO SONET/SDH Multiplexing Structure Supported by the EtherMap-3 Plus

HIGH ORDER VIRTUAL CONCATENATION WITH LCAS

When using high order virtual concatenation in SONET/SDH mode, every high order virtual concatenation group (VCG) can be independently optionally configured to operate in LCAS mode. Note, high order virtual concatenation can be used without LCAS, but LCAS requires virtual concatenation. The high order virtual concatenation LCAS Control packet definition and format is specified in the ITU-T G.707/Y.1322 standard. The LCAS protocol is specified in the ITU-T G.7042/Y.1305 standard.

The LCAS Control packet is resident in the H4 POH byte.

During initialization/normal operation, the EtherMap-3 Plus device provides support for management and re-allocation of member resources between LCAS and non-LCAS modes for use by multiple high order VCGs. In addition, general add and remove operations are supported using single high level messages.

In the transmit direction, for every member of a high order VCG operating in LCAS mode, the EtherMap-3 Plus device provides for individual source side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- PRBS generation for the Group Identification (GID) bit field.
- CRC-8 generation.
- LCAS Sequence Indicator (SQ) field generation.
- LCAS Control (CTRL) field generation.
- Inter-member messages during add/remove operations.
- For each transmit high order VCG in LCAS mode, selection of a high/low order member, in the receive direction, that is carrying the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Termination of MST and RS-Ack information from respective sink side LCAS state machine.
- Configurable high order per-member and per-VCG time-out counters for detection of failure during add and remove operations.
- Alarm generation to indicate LCAS source side state machine status.

In the receive direction, for every member of a high order VCG operating in LCAS mode, the EtherMap-3 Plus device provides for individual sink side LCAS hardware based state machines as per the ITU-T G.7042/Y.1305. The following additional functions are also supported:

- Group Identification (GID) field mismatch detection.
- CRC-8 check.

- LCAS Sequence Indicator (SQ) field processing.
- LCAS Control (CTRL) field processing.
- Generation of MST and RS-Ack status information.
- Detection and processing of Trail Signal Fail (TSF) conditions.
- For each receive high order VCG in LCAS mode, selection of a transmit side high/low order VCG that is used to transport the Member Status (MST) and Re-Sequence Acknowledge (RS-Ack) information.
- Alarm generation to indicate LCAS sink side state machine status.

CONFIGURATION FOR VIRTUAL CONCATENATION AND LCAS

General

The virtual concatenation of the 8 Ethernet lines within 8 VCGs can be performed with the EtherMap-3 Plus. For both Transmit and Receive, it is possible to configure the design in Low order, high order, mixed high order/low order, with LCAS or without LCAS, on a per VCG basis. The following paragraphs explain how to configure the virtual tributaries and how to extract status information from the device.

Note: A coherency is necessary between the configuration of the Virtual concatenation part of the design and the mapper configuration (for example: High order virtual concatenation with high order mapping). This applies also to any unused SONET/SDH container.

Low order configurations use the <klm> indication as described in the [“Transmit Low Order Path Termination \(Low Order POH Generator\)” on page 104](#). The standards allow only 64 VT/VC members per VCG.

Both VCAT Tx & RX (VCT/VCR) blocks can be configured to support the different mappings with a combination of registers defined below.

Selection of Mappings for VCAT blocks

| cTHOVC4 cRHOVC4 | cTHOVC3_[1..3] cRHOVC3_[1..3] | cSNTSDH ^a | Mappings possible for VCAT blocks |
|--------------------|----------------------------------|----------------------|---|
| 1 | NA | NA | STS-3c SPE STM-1 / AUG-1 / AU-4 / VC-4 |
| 0 | 11 | 0 | STS-3 / STS-1 SPE, STS-1-Xv STM-1 / AUG-1 / AU-3 / VC-3, VC-3-Xv |
| 0 | 11 | 1 | STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TU-3 / VC-3, VC-3-Xv |
| 0 | 00 | 0 | STS-3 / STS-1 / VT1.5 SPE, VT1.5-Xv STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv |
| 0 | 00 | 1 | STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-12 / VC-12, VC-12-Xv |
| 0 | 01 | 0 | NA |
| 0 | 01 ^b | 1 | STS-3 / STS-1 / VT2 SPE, VT2-Xv STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12, VC-12-Xv |

a. cSNTSDH bit is common to Rx & Tx VCAT blocks.

b. LO_SDH_AU3 mapping implies that all three VC-3 are configured in the same way (cTHOVC3/cRHOVC3 = 01).

It is important to note that depending on ADD/DROP timing mode, some mappings restrictions will apply. In DROP Timing Mode, because of unalignment of STS-1/TUG-3, following mappings become impossible:

- STS-3 / STS-1 SPE, STS-1-Xv where X > 1
- STS-3 / STS-1 / VT1.5 SPE, VT1.5-Xv where VT1.5s are spread over several STS-1s
- STS-3 / STS-1 / VT2 SPE, VT2-Xv where VT-2s are spread over several STS-1s
- STM-1 / AUG-1 / AU-4 / VC-4 / TUG-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv where VC-11s are spread over several TUG-3s
- STM-1 / AUG-1 / AU-3 / VC-3, VC-3-Xv where X > 1
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-11 / VC-11, VC-11-Xv where VC-11s are spread over several AU-3s
- STM-1 / AUG-1 / AU-3 / VC-3 / TUG-2 / TU-12 / VC-12, VC-12-Xv where VC-12s are spread over several AU-3s

Configuring Transmit VCAT (Ethernet to SONET/SDH)

The transmit side configuration/status is controlled by the following registers:

- **cSNTSDH** which indicates the SONET or SDH configuration. A single register is used for all the VCGs in transmit and receive direction. Default value is 0 (=SONET).
- **Configuration of the 3 High order virtual tributaries:**
 - cTHOVC4(6) indicates if there is no virtual concatenation with mapping on VC-4/STS-3c (when this bit is set to 1) or if the virtual concatenation exists (default value = 0)
 - cTHOVC3_1(5:4) indicates if the STS-1#1 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
 - cTHOVC3_2(3:2) indicates if the STS-1#2 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
 - cTHOVC3_3(1:0) indicates if the STS-1#3 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
- **Configuration of each VCG (LCAS/non-LCAS, ITU/ANSI, non standard ITU/ANSI):**
 - cTMST_VT(9:3) is used only in LCAS mode to select the tributary which carries MST and RS_ACK. Made by concatenation of AU3 # (bits 9-8), TUG2 # (bits 7-5) and TU1 # (bits 4-3). Default value is 0.
 - cTLCAS(2) is used to indicate the configuration of the VCG (LCAS or non LCAS). Default value is 0 means non LCAS.
 - cTHOVCG(1:0) indicate if the VCG is used in Low order ITU/ANSI (00, default value), in Low order non standard ITU/ANSI (01 value) or in high order ITU/ANSI (11 value).
- **cTVC4MAC(7:0):** choice of the MAC which will be mapped into VC-4/STS-3c. Ex: 00000100 means that the MAC #2 is mapped into VC-4/STS-3c. 00000001 means that the MAC#0 is mapped into VC-4/STS-3c.
- **Configuration of each low order virtual tributary:**
 - cTLOSQ (10:5)_klm: Sequence indicator of the virtual tributary. Default is 0x3F.
 - cTLOVCG (4:2)_klm: number of assigned VCG. Default is 0.
 - cTLOPOOL (1:0)_klm: assignation to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
- **Status of each low order virtual tributary:**
 - sTLOSQ (14:9)_klm: current sequence indicator of the virtual tributary. Default is 0x3F.
 - sTLOCTRL (8:5)_klm: Command/state field in LCAS/non LCAS. Default value is 0 (non LCAS). 0001 means ADD, 0010 means NORM, 0011 means EOS, 0101 means IDLE and 1111 means DNU in LCAS mode.

- sTLOVCG (4:2)_klm: number of assigned VCG. Default is 0.
- sTLOPOOL (1:0)_klm: assignment to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
- **Configuration of each STS-1/VC-3 used in high order virtual concatenation:**
 - cTHOPOOL_[1..3] (1:0): assignment to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
 - cTHOVCG_[1..3] (4:2): number of assigned VCG. Default is 0.
 - cTHOSQ[1..3] (12:5): sequence indicator value of each STS-1/VC-3 in case of high order virtual concatenation.
- **Status of each STS-1/VC-3 used in high order virtual concatenation:**
 - sTHOPOOL_[1..3] (1:0): assignment to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
 - sTHOVCG_[1..3] (4:2): number of assigned VCG. Default is 0.
 - sTHOCTRL_[1..3] (8:5): Command/state field in LCAS/non LCAS. Default value is 0 (non LCAS). 0001 means ADD, 0010 means NORM, 0011 means EOS, 0101 means IDLE and 1111 means DNU in LCAS mode.
- **sTHOSQ_[1..3](7:0):** configuration status of sequence indicator value of each STS-1/VC-3 in case of high order virtual concatenation.

Configuring Receive VCAT (SONET/SDH to Ethernet)

The receive side configuration/status is controlled by the following registers:

- **cSNTSDH** which indicates the SONET or SDH configuration. common with transmit virtual concatenation.
- **Configuration of the 3 High order virtual tributaries:**
 - cRHOVC4(6) indicates if there is no virtual concatenation i.e., with mapping on VC-4/STS-3c (when this bit is set to 1) or if the virtual concatenation exists (default value = 0)
 - cRHOVC3_1(5:4) indicates if the STS-1#1 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
 - cRHOVC3_2(3:2) indicates if the STS-1#2 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
 - cRHOVC3_3(1:0) indicates if the STS-1#3 is configured in low order (VT1.5/VT2 or VC-11/VC-12 (TUG-3)) with the value 00 (default), configured in low order in VC-12 (AU-3) in SDH only with the value 01 and in high order with the value 11.
- **Configuration of each VCG (LCAS/non-LCAS, ITU/ANSI, non standard ITU/ANSI):**
 - TX_VCG_x(5:3) is used only in LCAS mode to select the transmit VCG which carries MST and RS_ACK generated by LCAS Sink process. Default value is 0
 - cRLCAS_x(2) is used to indicate the configuration of the VCG (LCAS or non LCAS). Default value is 0 means non LCAS.
 - cRVCG_x(1:0) indicate if the VCG is used in Low order ITU/ANSI (00, default value), in Low order non standard ITU/ANSI (01 value) or in high order ITU/ANSI (11 value).
- **cRVC4MAC(7:0):** choice of the MAC which is mapped into VC-4/STS-3c. Ex: 00000100 means that the MAC #2 is mapped into VC-4/STS-3c. 00000001 means that the MAC#0 is mapped into VC-4/STS-3c.
- **Configuration of each low order virtual tributary:**
 - cRLOFMSTFAIL(11)_klm: Forces MST to Fail condition when set to 1 otherwise normal generation of MST.
 - cRLOSQ (10:5)_klm: Expected sequence indicator of the virtual tributary. Default is 0x3F.
 - cRLOVCG (4:2)_klm: number of assigned VCG. Default is 0.
 - cRLOPOOL (1:0)_klm: assignment Global/non-LCAS/LCAS_Idle/LCAS_Active pool.

- **Status of each low order virtual tributary:**
 - sRLOSQ(14:9)_klm: Extracted sequence indicator of the virtual tributary. Default is 0x3F.
 - sRLOCTRL (8:5)_klm]: Extracted Command/state field in LCAS/non LCAS. Default value is 0 (non LCAS). 0001 means ADD, 0010 means NORM, 0011 means EOS, 0101 means IDLE and 1111 means DNU in LCAS mode.
 - sRLOVCG (4:2)_klm: number of assigned VCG. Default is 0.
 - sRLOPOOL (1:0)_klm: assignation to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
- **Frame Count of each low order virtual tributary:**
 - sRLOMFI_x(4:0)_klm: extracted MFI value.
 - sRLOFC_x (9:5)_klm: extracted Frame count value.
- **Configuration of each STS-1/VC-3 used in high order virtual concatenation:**
 - cRHOPOOL_[1..3] (1:0): assignation to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
 - cRHOVCG_[1..3] (4:2): number of assigned VCG. Default is 0.
 - cRHOSQ_[1..3] (10:5): Expected sequence indicator of the virtual tributary. Default is 0xFF.
 - cRHOFMSTFAIL(11)_[1..3][1..7][1..4]: Forcing MST to Fail condition when set to 1 otherwise normal generation of MST.
- **Status of each STS-1/VC-3 used in high order virtual concatenation:**
 - sRHOPOOL_[1..3] (1:0): assignation to Global/non-LCAS/LCAS_Idle/LCAS_Active pool.
 - sRHOVCG_[1..3] (4:2): number of assigned VCG. Default is 0.
 - sRHOCTRL_[1..3] (8:5): Extracted Command/state field in LCAS/non LCAS. Default value is 0 (non LCAS). 0001 means ADD, 0010 means NORM, 0011 means EOS, 0101 means IDLE and 1111 means DNU in LCAS mode.
- **Frame count status of each STS-1/VC-3 used in high order virtual concatenation:**
 - sRHOMFI1_x(3:0)_[1..3]: Extracted MFI1 value.
 - sRHOMFI2_x (11:4)_[1..3]: Extracted MFI2 value.
- **sRHOSQ_[1..3](7:0):** status of the extracted sequence indicator value of each STS-1/VC-3 in case of high order virtual concatenation.

LCAS-Specific Configuration - Transmit

- cTLOK4VCEN_klm: Enables the transmission of the K4 bit 2 when set to 1 for each low order virtual tributary (default = 0).
- cTLOCRCERR_klm: initialization of the shift register for the CRC calculation for each low order virtual tributary. A zero initializes the register to 0 for normal operation. A one initializes the register to 1 and causes CRC errors to be generated.
- cTHOH4VCEN_[1..3]: Enables the transmission of the H4 byte when set to 1 for each high order virtual tributary (default = 0).
- cTHOHCRCERR_[1..3]: initialization of the shift register for the CRC calculation in high order only for the STS-1/VC-3. A zero initializes the register to 0 for normal operation. A one initializes the register to 1 and causes CRC errors to be generated.
- cTLOLCPRD1_klm(9:0): Terminal count of timeout counter (unit = ms) when adding the member on low order. Use for detection of MST_OK after an add command.
- cTHOLCPRD1_[1..3](9:0): Terminal count of timeout counter (unit = ms) when adding the member in High order. Use for detection of MST_OK after an add command.
- cTLCPRD2_[1..8](9:0): Terminal count of timeout counter (unit = ms) when adding the member in the VCG. Use for detection of RS_ACK after an add command.
- cTLCPRD3_[1..8](9:0): Terminal count of timeout counter (unit = ms) when removing the member in the VCG. Use for detection of RS_ACK after a remove command.

Assigning Unused VCGs (When at least one VCG is LCAS)

For MST extraction by the source:

Unused VCGs cannot point to the same member used for extraction by the used VCG(s). For example in a low order case, if VT/VC #111 is used for extraction, then the extraction controls for the remaining 7 VCGs must be changed, since they default to pointing to VT/VC #111. The following is an example of how to configure the other VCG's if only VCG0 is used for extraction.

0x1EC88 0300 - VCG1 (MAC 1) -> Unused, no MST/RS_ACK extraction
 0x1EC8a 0300 - VCG2 (MAC 2) -> Unused, no MST/RS_ACK extraction
 0x1EC8c 0300 - VCG3 (MAC 3) -> Unused, no MST/RS_ACK extraction
 0x1EC8e 0300 - VCG4 (MAC 4) -> Unused, no MST/RS_ACK extraction
 0x1EC90 0300 - VCG5 (MAC 5) -> Unused, no MST/RS_ACK extraction
 0x1EC92 0300 - VCG6 (MAC 6) -> Unused, no MST/RS_ACK extraction
 0x1EC94 0300 - VCG7 (MAC 7) -> Unused, no MST/RS_ACK extraction

The value 0x0300 represents an invalid member number since it points to AU3/STS1 #4, that is not a valid tributary index.

For MST generation by the sink:

Unused VCGs cannot point to the same VCG used for MST generation by the used VCG(s). For example, if VCG0 is used for generation, then the generation controls for the remaining 7 VCGs must be changed, since they default to pointing to VCG0. The following is an example of how to configure the other VCG's if only VCG0 is used for generation.

0x1f00a 0008 - MST and RS_ACK inserted into Tx VCG1 for receive VCG1
 0x1f00c 0010 - MST and RS_ACK inserted into Tx VCG2 for receive VCG2
 0x1f00e 0018 - MST and RS_ACK inserted into Tx VCG3 for receive VCG3
 0x1f010 0020 - MST and RS_ACK inserted into Tx VCG4 for receive VCG4
 0x1f012 0028 - MST and RS_ACK inserted into Tx VCG5 for receive VCG5
 0x1f014 0030 - MST and RS_ACK inserted into Tx VCG6 for receive VCG6
 0x1f016 0038 - MST and RS_ACK inserted into Tx VCG7 for receive VCG7

The values shown point to the same VCG number as the received VCG number.

DYNAMIC MAPPING AND VIRTUAL CONCATENATION CHANGES**VCG Tributary Assignments (Adding and Removing Members)**

The following procedures must be followed when adding or removing containers to/from an active VCG. For non-LCAS re-assignment, the source/sink, add/remove procedures can be followed in any order. For reassignment involving LCAS VCGs, the LCAS protocol must be respected and will limit the order in which events occur. Multiple tributary reassignment is described in each procedure. Single tributary reassignment is performed using the same steps. For initial configuration, the add procedures can be followed.

The procedures below refer to TX and RX MAC Reset. These functions are accomplished by setting both the Reset Tx/Rx Function bit (bit 0/1) and the Reset Tx/Rx MAC Control bit (bit 2/3) in configuration register 0x00002. Please note that all MAC registers must be accessed as 16-bit register pairs, even when only a 16-bit register access is needed. Registers 0x00000 and 0x00002 are a pair. For writes, the 16 MSBs (address bit 0 is high) must be written first. For reads, the 16 LSBs (address bit 0 is low) must be read first.

Note: z = H (high order) or L (low order)

Case 1: Re-assign multiple VC-11/VC-12 or VC-3/TUG-3 from VCGx to VCGy, Non-LCAS mode:

Below are listed four stand-alone procedures that can be executed in any order. When moving a tributary between VCGs, the order below will minimize resynchronization time.

Remove Procedure - Transmit

TX Channel X Reset ON (Rx MACx Reset first, then VCGx Reset)
 Change cTzOPOOL to Global for all containers to be removed from VCGx
 Change cTzOSQ to resequence the *remaining* members of VCGx
 Delay if needed (members must remain in GLOBAL pool for a minimum of 16 ms LO (2 ms HO) before moving to non-LCAS pool)
 TX Channel X Reset OFF (VCGx Reset first, then Rx MACx Reset)

Remove Procedure - Receive

RX Channel X Reset ON (VCGx Reset first, then Tx MACx Reset)
 Change cRzOPOOL to global for all containers to be removed from VCGx
 Change cRzOSQ to resequence the *remaining* members of VCGx
 RX Channel X Reset OFF (Tx MACx Reset first, then VCGx Reset)

Add Procedure - Receive

RX Channel Y Reset ON (VCGy Reset first, then Tx MACy Reset)
 Change cRzOVCG to VCGy for all containers to be added into VCGy
 Change cRzOPOOL to non-LCAS for all containers to be added into VCGy
 RX Channel Y Reset OFF (Tx MACy Reset first, then VCGy Reset)

Add Procedure - Transmit

TX Channel Y Reset ON (Rx MACy Reset first, then VCGy Reset)
 Change cTzOVCG to VCGy for all containers to be added into VCGy
 Change cTzOPOOL to non-LCAS for all containers to be added into VCGy
 TX Channel Y Reset OFF (VCGy Reset first, then Rx MACy Reset)

Case 2: Re-assign multiple VC-11/VC-12 or VC-3/TUG-3 from VCGx to VCGy, LCAS mode:

In LCAS mode, a Remove or Add procedure involves steps at both the sink and the source. When moving a tributary between VCGs, the tributary must be removed first and then added.

Remove Procedure

Step 1 - Remove at the Source

for first tributary:

Change cTzOPOOL to LCAS IDLE (wait for alarm REM or PRD3)

Change cTzOPOOL to GLOBAL

Change cTHOH4VCEN_[1..3] or cTLOK4VCEN_klm to disable

then move on to the next tributary

Delay if needed (members must remain in GLOBAL pool for a minimum of 16 ms LO (2 ms HO) before moving to LCAS IDLE pool)

Step 2 - Remove at the Sink

for first tributary:

Change cRzOPOOL to LCAS IDLE (wait for aRLCASREM)

Change cRzOPOOL to GLOBAL

then move on to the next tributary

Add Procedure

Step 1 - Add at the Sink

for first tributary:

Change cRzOVCG to VCGy

Change cRzOPOOL to LCAS IDLE

Change cRzOPOOL to LCAS ACTIVE

Read aRLCASADDED

then move on to the next tributary

Step 2 - Add at the Source

for first tributary:

Change cTzOVCG to VCGy

Change cTHOH4VCEN_[1..3] or cTLOK4VCEN_klm to enable

Change cTzOPOOL to LCAS IDLE

Delay if needed (members must remain in IDLE pool for a minimum of 16 ms LO (2 ms HO) before moving to LCAS ACTIVE pool)

Change cTzOPOOL to LCAS ACTIVE (check PRD1, PRD2, aTLCASADDED)

then move on to the next tributary

Step 3 - (Optional) Verify at the Sink

Read aRLCASADDED alarm

(Allows the Add Procedure to be verified at the sink end, and also clears the alarm for its next use.)

Case 3: Re-assign multiple VC-11/VC-12 or VC-3/TUG-3 from VCGx (LCAS) to VCGy (non-LCAS):

Use the Case 2 Remove Procedure and the Case 1 Add Procedure, completing the Removes before performing any Adds. Alternatively, the LCAS remove and non-LCAS Add can be completed at the source before any operations are done at the sink.

Case 4: Re-assign multiple VC-11/VC-12 or VC-3/TUG-3 from VCGx (non-LCAS) to VCGy (LCAS):

Use the Case 1 Remove Procedure (Rx and Tx in any order), then follow the Case 2 Add Procedure.

Changing VCG Encapsulation/Decapsulation Mode

The procedures for changing encapsulation mode are covered in the Encapsulation/Decapsulation section beginning on [page 139](#).

Changing VCG SONET/SDH Structure

This section deals with changing the fundamental SONET/SDH structure of a VCG. When changing a VCG from high-order mode to low-order mode (or vice-versa), or when changing to/from STS-3c/VC-4 mode, the following procedures must be followed.

The VCG Tributary Reassignment procedure defined above is referenced by this procedure and should be maintained except where noted below.

For non-LCAS reconfiguration, the transmitter and receiver reconfiguration procedures below can be followed in either order. For reconfiguration involving LCAS VCGs, the LCAS protocol must be respected and will limit the order in which events occur. As such, for any reconfiguration involving addition of LCAS VCGs in which only non-LCAS VCGs are removed, the Receiver Reconfiguration procedure below is performed first. For any reconfiguration in which LCAS VCGs are removed and are either added or not added, the Transmitter Reconfiguration below is performed first. However, when LCAS VCGs are added, no member can be added to the LCAS ACTIVE pool at the transmitter until after the Receiver Reconfiguration procedure is completed.

Transmitter Reconfiguration

Changing High-Order/Low-Order Assignment (HO->LO or LO->HO)

- 1) Empty the changing VCGs by moving their containers to the GLOBAL pool. This is done by following the applicable tributary assignment procedure (non-LCAS or LCAS) starting on page [page 124](#). For non-LCAS, the soft resets of the Tx VCGs and Rx MACs being added are not released.
- 2) If not done in step 1, apply soft reset to any Tx VCG and Rx MAC to be used in the new configuration
- 3) Freeze all VCGs that are to be used (cTFCRSTx in [Table 65](#) on [page 271](#))
- 4) Reconfigure the Mapper for the new SONET/SDH structure
- 5) Reconfigure the VCGs (cTVCG_x, cTLCAS_x, cTMST_VT_x in [Table 65](#) on [page 271](#))
- 6) Reconfigure the STS-1/VC-3s (cTHOVC3_n in [Table 65](#) on [page 270](#))
- 7) Allocate containers to the VCGs using the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For LCAS VCGs, first release the Tx VCG and Rx MAC resets.
- 8) Release the cTFCRST bits for the changed VCGs

Note: For the following configurations, step 4 above is performed after step 6:

LLL => LLH; LHL => LHH; LLH => LHH; LLL => HLH; HLL => HLH; LLL => LLH; HLL => LLH;
 LHL => LLH, where L = low order and H = high order and, for example, HLL => LLH indicates that STS1#1/VC3#1 is changing from high order to low order and STS1#3/VC3#3 is changing from low order to high order.

Changing FROM STS-3c/VC-4

- 1) Apply soft reset to the Tx VCG and Rx MAC that is assigned to the STS-3c/VC-4
- 2) Freeze all VCGs to be configured (cTFCRSTx in [Table 65](#) on [page 271](#))
- 3) Reconfigure the Mapper Block for the new SONET/SDH structure
- 4) Reconfigure the VCGs (cTVCG_x, cTLCAS_x, cTMST_VT_x in [Table 65](#) on [page 271](#))
- 5) Reconfigure the STS-1/VC-3s (cTHOVC3_n in [Table 65](#) on [page 270](#))
- 6) Configure for non STS-3c/VC-4 mode (cTHOVC4 in [Table 65](#) on [page 270](#))
- 7) Remove STS-3c/VC-4 Ethernet port mapping (cTVC4MAC in [Table 65](#) on [page 270](#))
- 8) Allocate containers to the VCGs using the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For LCAS VCGs, first release the Tx VCG and Rx MAC resets.
- 9) Release the cTFCRST bits for the newly configured VCGs
- 10) If not released during step 8, release the soft reset of the Tx VCG and Rx MAC that was formerly assigned to the STS-3c/VC-4

Changing TO STS-3c/VC-4

- 1) Empty all VCGs by moving their containers to the GLOBAL pool. This is done by following the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For non-LCAS, the Rx MAC soft reset is not released for the Ethernet port that will be mapped to the STS-3c/VC-4.
- 2) If not done in step 1, apply Rx MAC soft reset to the Ethernet port that will be mapped to the STS-3c/VC-4
- 3) Apply Tx Soft Reset to all of the emptied VCGs and the VCG that will be mapped to the STS-3c/VC-4.
- 4) Freeze all emptied VCGs (cTFCRST in [Table 65](#) on [page 271](#))
- 5) Reconfigure the Mapper Block for the new SONET/SDH structure
- 6) Add the STS-3c/VC-4 Ethernet port mapping (cTVC4MAC in [Table 65](#) on [page 270](#))
- 7) Configure for STS-3c/VC-4 mode (cTHOVC4 in [Table 65](#) on [page 270](#))
- 8) Release the cTFCRST bits of the emptied VCGs and the new STS-3c/VC-4 VCG
- 9) Release the Rx MAC soft reset of the Ethernet port that is now mapped to the STS-3c/VC-4
- 10) Release Tx Soft Reset of all emptied VCGs and the new STS-3c/VC-4 VCG

Receiver Reconfiguration

Changing High-Order/Low-Order Assignment (HO->LO or LO->HO)

- 1) Empty the changing VCGs by moving their containers to the GLOBAL pool. This is done by following the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For non-LCAS, the soft reset of the Rx VCG and Tx MAC being added are not released.
- 2) If not done in step 1, apply soft reset to any Rx VCG and Tx MAC to be used in the new configuration
- 2) Reconfigure the VCGs (cRVCG_x, cRLCAS_x, TX_VCG_x in [Table 76](#) on [page 284](#))
- 3) Reconfigure the STS-1/VC-3s (cRHOVC3_n in [Table 76](#) on [page 283](#))
- 4) Reconfigure the Demapper Block - When reconfiguring from high to low order, there must be at least 1 ms of delay between enable of the LO pointer processor (0x1C620/2/4->0x0000) and enable of the LO POH monitor (0x148E0/2/4->0x0000)
- 5) Allocate containers to the VCGs using the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For LCAS VCGs, first release the Rx VCG and Tx MAC resets.

Changing FROM STS-3c/VC-4

- 1) Stop data flow from the Demapper (set addresses 0x148e0, 0x148e2 and 0x148e4 to 0x0)
- 2) Apply soft reset to all Rx VCGs
- 3) Apply Tx MAC soft reset to all eight MACs
- 4) Configure the 3 STS-1/VC-3s (cRHOVC3_n in [Table 76](#) on [page 283](#)). Do not exit STS-3c/VC-4 mode.
- 5) Release Rx soft reset of all eight VCGs
- 6) Configure for non STS-3c/VC-4 mode (cRHOVC4 in [Table 76](#) on [page 283](#))
- 7) Remove the STS-3c/VC-4 Ethernet port mapping (cRVC4MAC in [Table 76](#) on [page 284](#))
- 8) Apply Rx soft reset to all eight VCGs
- 9) Reconfigure the VCGs (cRVCG_x, cRLCAS_x, TX_VCG_x in [Table 76](#) on [page 284](#))
- 10) Reconfigure the Demapper Block for the new SONET/SDH structure
- 11) For HO STS-1/VC-3s only: allow data flow from the Demapper (set addresses 0x148e0, 0x148e2 and 0x148e4 to 0x1)
- 12) Allocate containers to the VCGs using the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For LCAS VCGs, first release the Rx VCG and Tx MAC soft resets.
- 13) Release Tx MAC soft reset of all MACs not released in step 12
- 14) Release Rx soft reset of all VCGs not released in step 12

Changing TO STS-3c/VC4

- 1) Empty all VCGs by moving their containers to the GLOBAL pool. This is done by following the applicable tributary assignment procedure (non-LCAS or LCAS) starting on [page 124](#). For non-LCAS only, the Tx MAC soft reset is not released for the Ethernet port that will be mapped to the STS-3c/VC-4.
- 2) If not done in step 1, apply Tx MAC soft reset to the Ethernet port that will be mapped to the STS-3c/VC-4
- 3) Apply Rx soft reset to all eight VCGs
- 4) Release Rx soft reset of all eight VCGs
- 5) Add the STS-3c/VC-4 Ethernet port mapping (cRVC4MAC in [Table 76](#) on [page 284](#))
- 6) Configure for STS-3c/VC-4 mode (cRHOVC4 in [Table 76](#) on [page 283](#))
- 7) Reconfigure the Demapper Block for the new SONET/SDH structure
- 8) Apply Rx soft reset to all eight VCGs
- 9) Release the Tx MAC soft reset of the Ethernet port now mapped to the STS-3c/VC-4
- 10) Release the Rx soft reset of all eight VCGs

DIFFERENTIAL DELAY COMPENSATION

The EtherMap-3 *Plus* performs differential delay compensation for the containers included in a given virtual concatenation group.

This supports the scenario where the virtually concatenated containers travel different paths in the SONET/SDH network and therefore are received by the EtherMap-3 *Plus* with a time offset.

The mutliframe indicator field (MFI) is used for differential delay compensation. MFI is located in the H4 byte (for high order virtual concatenation) or in the K4/Z7 byte (for low order virtual concatenation).

For each virtual concatenation group (VCG_x, x = 0 - 7), two registers are provided. See below.

Maximum Differential Delay Allowed

Register rMAXDELVCG_x is used to configure the maximum differential delay value allowed amongst the members of a virtual concatenation group (VCG_x). The maximum value that can be configured for both Low Order Virtual Concatenation (LO VCAT) and High Order Virtual Concatenation (HO VCAT) is 48 ms.

Low Order

In LO VCAT, only bits (9-7) of rMAXDELVCG_x are used. The value is configured in steps of 16 ms.

Table 4 shows the values allowed:

Table 4: Configuration of rMAXDELVCG_x in Low Order VC

| Configuration of rMAXDELVCG_x | Multiple of 16 ms | Resulting Maximum Delay Allowed |
|-------------------------------|-------------------|---------------------------------|
| 0x0000 | 0 x 16 ms | 0 ms |
| 0x0080 | 1 x 16 ms | 16 ms |
| 0x0100 | 2 x 16 ms | 32 ms |
| 0x0180 | 3 x 16 ms | 48 ms |

High Order

In HO VCAT, bits (9-0) of rMAXDELVCG_x are used. The value is configured in steps of 125 μ s.

Table 5 shows the values allowed:

Table 5: Configuration of rMAXDELVCG_x in High Order VC

| Configuration of rMAXDELVCG_x | Multiple of 125 μ s | Resulting Maximum Delay Allowed |
|-------------------------------|-------------------------|---------------------------------|
| 0x0000 | 0 x 125 μ s | 0 ms |
| 0x0001 | 1 x 125 μ s | 125 μ s |
| | ... | |
| 0x0180 | 384 x 125 μ s | 48 ms |

Maximum Differential Delay Detected

Register rDIFDELVCG_x reports the maximum differential delay detected among the members of a given virtual concatenation group (VCG_x). The maximum delay that can be detected is 128 ms.

Low Order

In LO VCAT, bits (3-0) of rDIFDELVCG_x represent the maximum differential delay detected among the low order members of a VCG_x.

The register has a granularity of 16 ms: a value of 0001 Hex represents a delay of 16 ms.

The maximum allowed value is 8, corresponding to 128 ms.

If the delay is higher than 128 ms, then bit (11) of rDIFDELVCG_x is set, indicating EtherMap-3 Plus is not able to compute such a differential delay, and further, bits (3-0) of rDIFDELVCG_x contain invalid information. Furthermore, in LO VCAT, when the reported differential delay is found to be greater than that configured in the rMAXDELVCG_x register, an alarm, aLOLOA_x, is generated per VCG_x.

High Order

In HO VCAT, bits (10-0) of rDIFDELVCG_x represents the maximum differential delay detected among the members of a VCG_x.

The register has a granularity of 125 μ s: a value of 0001 Hex represents a delay of 125 μ s.

The maximum allowed value is 1024, corresponding to 128 ms.

If the delay is higher than 128 ms, bit (11) of rDIFDELVCG_x is set, indicating EtherMap-3 Plus is not able to compute such a differential delay, and further, bits (10-0) of rDIFDELVCG_x contain invalid information. Furthermore, in HO VCAT, when the reported differential delay is found to be greater than that configured in the rMAXDELVCG_x register, an alarm, aHOLOA_x, is generated per VCG_x.

In both cases (LO VCAT and HO VCAT), EtherMap-3 Plus can compute a differential delay up to 128 ms, but it can only compensate a maximum differential delay of 48 ms.

ETHERNET SUPPORT

SMII AND GMII INTERFACES

The EtherMap-3 *Plus* supports two types of Ethernet line interfaces: SMII or GMII. The GMII Ethernet line interface is used only when the EtherMap-3 *Plus* Ethernet line side is configured for 1000 Mbps operation. The SMII Ethernet line interface is used only when the EtherMap-3 *Plus* Ethernet line side is configured for 10/100 Mbps operation. An external signal lead, GMII/SMII, provides for selection between either a single GMII Ethernet line interface or up to eight independent SMII Ethernet line interfaces. Note, that the GMII Ethernet line interface uses the same leads as the SMII Ethernet line interface and thus these two Ethernet line interfaces cannot be used simultaneously.

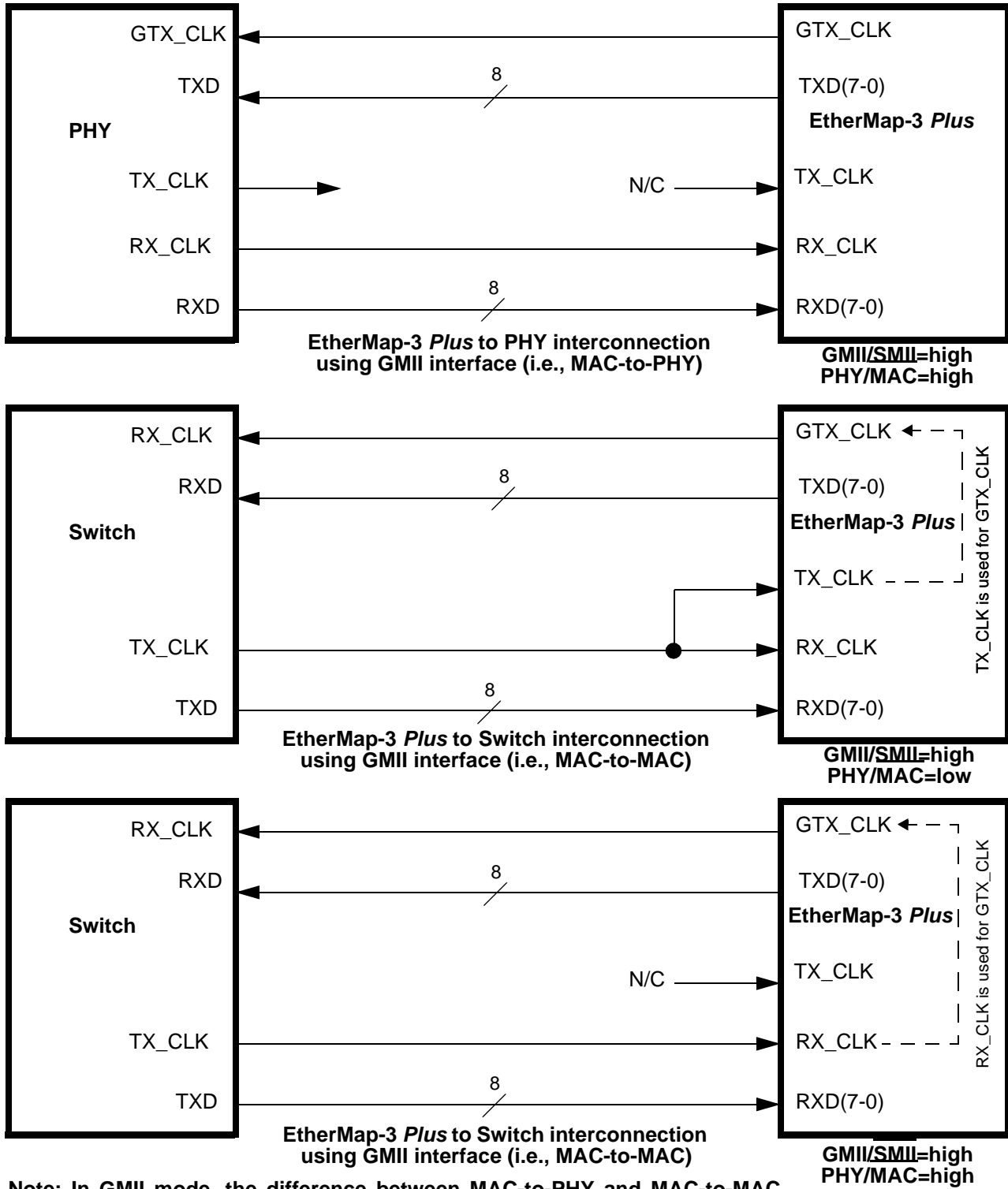
When using the GMII interface, an external signal lead, PHY/ $\overline{\text{MAC}}$, selects the clock source for the output signal, GTX_CLK. This allows for flexible interconnections between EtherMap-3 *Plus* and other common components such as Ethernet PHY or Switch devices. [Figure 51](#) shows these various interconnection options.

EtherMap-3 *Plus* supports up to eight independent SMII interfaces. All eight SMII interfaces use a common global clock and common global sync signal (SMII_GCLK). An external signal lead, SYNC_DIR, controls the direction of the sync signal on the SMII_GSYNC signal lead.

The external lead PHY/ $\overline{\text{MAC}}$ allows the 8 Ethernet lines of EtherMap-3 *Plus* to be connected to a PHY or to a MAC. When PHY/ $\overline{\text{MAC}}$ is equal to 1, EtherMap-3 *Plus* is connected to a PHY and then is ready to accept status information from the PHY. When PHY/ $\overline{\text{MAC}}$ is equal to 0, EtherMap-3 *Plus* is considered to be connected to a MAC and then the 8 Ethernet interface need to be configured.

EtherMap-3 *Plus* supports Half Duplex and Full Duplex for 10/100 Mbps and only Full Duplex for 1000 Mbps.

In addition to the GMII/SMII Ethernet line interfaces, the EtherMap-3 *Plus* also provides support of control and status to and from external PHYs using a two-wire MII Management Interface (MDC, MDIO) as per IEEE 802.3u. This interface can be used with both GMII/SMII interfaces.



Note: In GMIi mode, the difference between MAC-to-PHY and MAC-to-MAC configuration is given by the different wiring, as can be seen comparing the upper and the lower two configurations in this diagram.

Figure 51. EtherMap-3 Plus to PHY or Switch Interconnection Using GMIi Interface

ETHERNET MAC BLOCKS

The EtherMap-3 *Plus* contains eight Ethernet MACs. Each of these MACs can support a 10/100/1000 Mbit/s operation. However, when EtherMap-3 *Plus* is configured for Gigabit mode, only the first MAC is used for 1000 Mbit/s operation. The remaining MACs are disabled. When EtherMap-3 *Plus* is configured for 10/100 Mbit/s mode, all eight MACs are enabled and each can be independently configured for 10 or 100 Mbit/s operation. The selection between 10/100 or 1000 Mbit/s mode is done using the external signal lead GMII/SMII and further internal registers to select between 10 or 100 Mbit/s mode only. In addition, if the attached PHY device auto-negotiates between 10 and 100 Mbps, this information is passed to the MAC over the SMII interface and overrides any internal register setting. Link status is available in registers shown in [Table 16](#).

In the transmit direction (i.e., towards the Ethernet line side), each MAC can be configured to apply or not to apply padding and to append or not to append a valid FCS field to the Ethernet frames. EtherMap-3 *Plus* supports both Half Duplex mode (CSMA/CD) and Full Duplex mode for 10/100 Mbit/s and Full Duplex mode for 1000 Mbit/s. PAUSE flow control frame generation is fully configurable and supported (as per IEEE 802.3x). Following each Ethernet frame transmission or abortion, EtherMap-3 *Plus* updates the appropriate transmit side RMON statistic counters.

The general configuration of the MACs is described in Tables [18-22](#) (including selection between Full or Half Duplex operation). Furthermore [Table 21](#) specifies Half Duplex configuration such as:

- Configuration of collision window,
- Number of maximum transmission attempts following a collision before abortion,
- Abort or Transmit of an excessively deferred packet,
- Use of alternate binary exponential back-off rule or to immediately re-transmit a packet following a collision during back pressure,
- Use of 802.3 standard tenth collision or programmable alternate binary exponential back-off truncation.

In the receive direction (i.e., from the Ethernet line side), each MAC scans the preamble looking for the Start Frame Delimiter (SFD). The preamble and SFD are stripped and the remaining Ethernet frame is passed on for further processing. In addition, each MAC provides the capability to filter Ethernet frames that have less than a configured Inter-Frame Gap; to detect broadcast or multicast destination addresses; to check length field against the actual length of the data field portion of the Ethernet frame and to check or not the FCS field of the Ethernet frame. EtherMap-3 *Plus* supports both Half Duplex mode (CSMA/CD) and Full Duplex mode for 10/100 Mbit/s and only Full Duplex mode for 1000 Mbit/s. This means that the PAUSE flow control frame detection is fully configurable and supported (as per IEEE 802.3x). Following each Ethernet frame reception, the appropriate receive side RMON statistic counters are updated.

Tables [24-29](#) are used for configuration and control of the MII Management interface. Using the control bits of [Table 24](#), the MDC (MII Management clock) is derived from the MICCLK clock by applying a divide factor between 4 and 28. It is also possible to suppress or not the preamble information. To perform a write access, the following steps are followed:

- Configure 'Register Address' field (with 0x0 for control register of the PHY) of [Table 26](#),
- Configure 'Phy Address' field of [Table 26](#),
- Write a data value into the 'MII Mgmt Control' field of [Table 27](#),

Similarly, to perform a read access, the following steps are followed:

- Configure 'Register Address' field (with 0x1 for control register of the PHY) of [Table 26](#),
- Configure 'Read Cycle' field of [Table 25](#),
- Read a data value from the 'MII Mgmt Status' field of [Table 28](#).

Ethernet Frame Size

Ethernet frames received which are shorter than the Ethernet standard of 64 bytes are counted as undersize or fragments (see [Table 14, on page 202](#)) but are still passed through the MAC block if the FCS is correct.

The maximum Ethernet frame size that is passed through the MAC is configurable using the Maximum Frame Length register (0x00010, [Table 22 on page 213](#)). This 16-bit register can be configured for up to 64K frame lengths, but extremely large frames are not guaranteed to pass through the device. The actual maximum frame size supported depends on traffic conditions, but the following statements hold true:

- When using any number of SMII interfaces, the device can support the full SONET line rate with frames sizes up to 9600 bytes.
- When using the GMII interface, the device can transmit frames up to 1650 bytes in length at the full SONET line rate while receiving a continuous stream of 64 byte frames. Larger frames on the receive path will allow larger Ethernet frames to be transmitted. If the same frame size is used in both directions, the device can support the full SONET line rate with frames up to 3000 bytes.
- For both the SMII and GMII interfaces, slower SONET line rates can support larger Ethernet frame sizes.

ETHERNET HALF DUPLEX

In Half-Duplex mode of operation, two or more Ethernet devices are connected to a common transmission medium and when one Ethernet device transmits, the others listen. In the case where two Ethernet devices transmit at once, a "Collision" is said to have occurred. A "Jam Sequence" is transmitted by the transmitting Ethernet device indicating the occurrence of a collision. The contention is resolved by each of the Ethernet devices responsible for the collision, backing off, and attempting to re-transmit after a time period. This method is called Carrier Sense Multiple Access/Collision Detection (CSMA/CD). The EtherMap-3 Plus Media Access Controller (MAC) implements the 802.3 compliant CSMA/CD algorithm. For a complete definition of this algorithm please refer to the IEEE 802.3 specification. Following is an outline based on the EtherMap-3 Plus MAC.

Note: Carrier Sense and Collision detection status is indicated by the PHY device to the EtherMap-3 Plus via the SMII interface. Please refer to the Serial Media Independent Interface (SMII) specification for further details.

Carrier Sense

To begin transmission of an Ethernet frame, the EtherMap-3 Plus Media Access Controller (MAC) uses three different configuration registers. After the transmission of an Ethernet frame, the Back-to-Back Inter Packet Gap (IPG) is enforced. After an Ethernet frame is received, the Non-Back-to-Back IPG (IPG2) is used. Additionally, during the time defined by the IPGR1 configuration register, the MAC monitors the Carrier Sense status. This Carrier Sense window is known as IPG1. If carrier is detected during this window, the MAC does not attempt to transmit. If the carrier becomes active after the IPG1 window, transmission is begun after the proper IPG has elapsed, forcing a collision and subsequent backoff. The Carrier Sense window is typically configured using a two-thirds/one-third ratio, meaning that the carrier is monitored during the first two-thirds of the IPG, and is ignored during the remaining one-third. Since it is not possible for the Ethernet output to backpressure traffic arriving from SONET/SDH, it may be necessary to configure the EtherMap-3 Plus to more aggressively occupy the Ethernet media by reducing the size of the IPG1 window.

Collision Detection

In the event the EtherMap-3 Plus MAC detects a Collision when the device is transmitting an Ethernet frame, the MAC outputs the 32-bit jam sequence. The jam sequence is made up of several bits of the CRC, inverted to guarantee an invalid CRC upon reception of the frame. The MAC then backs off transmission of the frame (retry) based on the "Truncated Binary Exponential Backoff" (BEB) algorithm. Following this backoff time, the frame is retried. The "No Backoff" configuration bit, when enabled, retransmits the frame without a backoff, following a collision. This option needs to be enabled with caution.

Alternate BEB Truncation

The backoff time following a collision is a controlled randomization process called “truncated binary exponential backoff”. It is defined as an integer multiple of the slot times. The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer r in the range: $0 \leq r \leq 2^k$ where $k = \min(n,10)$. So, after the first collision, the MAC will backoff either 0 or 1 slot times. After the fifth collision, the MAC will backoff between 0 and 32 slot times. After the tenth collision, the maximum number of slot times to backoff is 1024. By setting the “Alternate BEB Enable” bit, the truncation point can be changed from $\min(n,10)$ to $\min(n,m)$ where m is set in the “Alternate BEB Truncation” register.

Excessive Collisions

Upon collision, the MAC attempts re-transmission of the frame. As specified in the IEEE 802.3 specification, a frame has excessive collisions if 15 re-transmission attempts have occurred. The number of retransmission attempts for excessive collisions is configurable. In the event a frame has been excessively deferred, the frame is discarded and will not be transmitted. It is possible to configure the EtherMap-3 *Plus* not to discard an excessively deferred frame.

Half-Duplex Flow Control

There is no IEEE 802.3 compliant backpressure mechanism for Half Duplex. The common industry implementation is the “Raise Carrier” method. The EtherMap-3 *Plus* MAC uses the configurable “Raise Carrier” method for flow control in Half-Duplex mode. In the event the EtherMap-3 *Plus* MAC needs to backpressure the transmission medium, it raises carrier by transmitting the preamble. Other devices on the transmission Medium defer to the carrier. If a collision occurs due to the raised carrier, the congestion is resolved using the standardized collision-detect, backoff method. The duration of a raised carrier is kept below 3.3 ms in 10 Mbps mode and 33 ms in 100 Mbps mode so that the anti-jabber limitation in the PHY device is not exceeded. To avoid an excessive deferral condition at the sender, a maximum of 16 of these raised carriers bursts will be sent, after which a transmit packet must go out before the carrier can be raised again. The Host can not initiate flow control when the raise carrier method is being used.

FLOW CONTROL OPERATION

OVERVIEW

Because there could be a mismatch of data rates between an Ethernet port and its corresponding SONET/SDH link (i.e., transporting 100 Mbit/s using a single VC-3), EtherMap-3 *Plus* has the ability to backpressure the Ethernet traffic. Depending on the mode of operation of the Ethernet port (i.e., Full Duplex or Half Duplex), the EtherMap-3 *Plus* provides support for the following types of flow control mechanisms:

- Full Duplex mode (for 10/100/1000 Mbit/s): when configured for Full Duplex mode, the PAUSE frame (as per IEEE 802.3) is used as a flow control mechanism.
- Half Duplex mode (for 10/100 Mbit/s): when configured for Half Duplex mode, the CSMA/CD algorithm is used as a backpressure flow control mechanism. The backpressure scheme uses the 'raise carrier' method. [Table 21](#) provides further details on specific configuration options.

FULL DUPLEX FLOW CONTROL

Definitions

The EtherMap-3 *Plus* uses several structures to implement full duplex flow control. First, each MAC channel has a separate "TxFIFO" that is used to buffer Ethernet frames and perform rate adaptation between the Ethernet and SONET/SDH data rates. Each TxFIFO has a configurable High Watermark and a configurable Low Watermark. Associated with the watermarks are the High Pause Time Value and Low Pause Time Value. These values get inserted into outgoing PAUSE frames in the pause_time field and create the concept of a High Pause Frame and Low Pause Frame which carry the High Pause Time Value and Low Pause Time Value, respectively. In typical XON/XOFF implementations the High Pause Frame carries a fairly large or maximum time value and the Low Pause frame simply carries a time value of zero. Finally, there is an internal Sample Timer that determines when the TxFIFO depth is sampled. When a High Pause Frame is queued for transmission, the Sample Timer is loaded with the High Pause Time Value and is decremented until it reaches a configurable Terminal Value, at which point it has expired.

Flow Control Algorithm

A High Pause Frame is sent when any of the following are true:

- The TxFIFO depth is rising and the High Watermark is crossed and the Sample Timer is not decrementing
- The Sample Timer expires and the TxFIFO depth is above the High Watermark

A Low Pause Frame is sent when any of the following are true:

- The TxFIFO depth is falling and the Low Watermark is crossed and the Sample Timer is not decrementing
- The Sample Timer expires and the TxFIFO depth is below the Low Watermark

TxFIFO Overflow

If the attached Ethernet client does not properly respond to Pause Frames, then an overflow of the TxFIFO is the likely result (indicated by the aTXFIFO alarm, [Table 99](#) on [page 299](#)). If the FIFO does overflow, further writes to the fifo are prevented and incoming Ethernet traffic is discarded while observing frame boundaries (no partial frames are written into the FIFO). FIFO reads continue to take place allowing the fifo level to recede. Once the fifo depth falls to the High Watermark, writes are again allowed. During all of this, the flow control algorithm remains in effect, so if the Sample Timer expires while the FIFO depth is above the High Watermark, or if the fifo depth rises and crosses the High Watermark, additional outgoing Pause Frames will be sent.

External Pause Frames

In addition to generating Pause Frames for flow control purposes, it is also possible for the EtherMap-3 *Plus* to receive Pause frames from either the Ethernet input interface, or from the SONET/SDH line interface.



In the Ethernet-to-SONET direction, several options exist for managing Pause Frames. If the arriving Pause Frame is detected and acted upon, then the corresponding Tx MAC stops transmission for the amount of time indicated in the pause_time field. This behavior is configured by setting the Receive Flow Control Enable bit described in [Table 18](#) on [page 210](#).

Whether or not the received Pause Frame is used to stop outgoing Ethernet traffic, the Pause Frame can be optionally encapsulated into the SONET/SDH stream. This is controlled using the cTFCMODE bits described in [Table 86](#) on [page 295](#).

In the SONET-to-Ethernet direction, Pause Frames are never used to stop traffic. They can either be passed through to the Ethernet output or discarded, depending on the setting of the cRFCMODE bit described in [Table 48](#) on [page 236](#). In any event, all Pause Frames received from SONET/SDH are counted (per Ethernet port) using the rpcRPAUSEx counter.

Configuring Full Duplex Flow Control

The following registers are used to configure full duplex flow control:

| Concept | Register | Location |
|------------------------------|------------------------------|--------------------------|
| Enable | Transmit Flow Control Enable | Table 18 |
| | Receive Flow Control Enable | |
| TxFIFO High Watermark | rHWTMK_MSB_x | Table 98 |
| | rHWTMK_LSB_x | |
| TxFIFO Low Watermark | rLWTMK_MSB_x | |
| | rLWTMK_LSB_x | |
| High Pause Time Value | rHWPT_x | Table 30 |
| Low Pause Time Value | rLWPT_x | |
| Sample Timer Terminal Value | rHIPSE_x | |
| E-to-S Pause Frame Filtering | cTFCMODE | Table 86 |
| S-to-E Pause Frame Filtering | cRFCMODE | Table 48 |

The allowed ranges for the High/Low Watermarks depend on the SDRAM configuration (SDRAM_CFG bit) and the selection of GMII/SMII mode, as shown in the table below.

Table 6: Allowed Range for High/Low Watermark Registers

| Mode | SDRAM Size | Memory Allocated to Each FIFO | Minimum Value for rLWTMK_MSB_x, rLWTMK_LSB_x | Maximum Value for rHWTMK_MSB_x, rHWTMK_LSB_x |
|------|------------|-------------------------------|--|--|
| SMII | 8MB | 32 kB | 0000 0020 | 0000 1FFF |
| | 16MB | 64 kB | 0000 0020 | 0000 3FFF |
| | 32MB | 128 kB | 0000 0020 | 0000 7FFF |
| GMII | 8MB | 256 kB | 0000 0020 | 0000 FFFF |
| | 16MB | 512 kB | 0000 0020 | 0001 FFFF |
| | 32MB | 1 MB | 0000 0020 | 0003 FFFF |

Notes:

1. In the watermark registers, one step of 1 HEX corresponds to four bytes in the FIFO. For example, if you lower the watermark by a hex value of "1", the FIFO threshold will be lowered by four bytes.
2. For the High watermark, the maximum allowed value corresponds to the whole allocated FIFO space minus one 32 bit word (4 bytes). For example, in the last line of table above, 3 FFFF corresponds to 1,048,572 bytes, which is the whole allocated TXFIFO space (1* 1024*1024 bytes) minus one 32 bit word (4 bytes).

Changing Configurations

When changing flow control parameters from their default values, the following procedures should be followed:

From a Hardware Reset:

1. Configure the flow control parameters ([Table 30](#) and [Table 98](#)).
2. De-assert the MAC Soft Reset (see [Table 18](#) - Reset Tx, Reset Rx).
3. Enable the transmit and receive MAC blocks (see [Table 18](#) - Transmit Enable and Receive Enable).

From an already configured device:

1. Disable the transmit and receive MAC blocks.
2. Assert the MAC Soft Reset.
3. Configure the flow control parameters ([Table 30](#) and [Table 98](#)).
4. De-assert the MAC Soft Reset.
5. Enable the transmit and receive MAC blocks.

ENCAPSULATION/DECAPSULATION

When the Ethernet line side is configured for SMII interface, the EtherMap-3 *Plus* device provides support for up to eight independent 10/100 Mbit/s Ethernet MAC blocks. Each 10/100 Mbit/s Ethernet MAC block is further allocated to a dedicated protocol encapsulation/decapsulation block (up to eight independent blocks) for servicing its bi-directional Ethernet frame traffic.

When the Ethernet line side is configured for GMII interface, the EtherMap-3 *Plus* device provides support for a single 1000 Mbit/s Ethernet MAC block (shared with the first 10/100 Mbit/s Ethernet MAC block). The 1000 Mbit/s Ethernet MAC block is allocated to a dedicated protocol encapsulation/decapsulation block (the first block is shared between 10/100 Mbit/s and 1000 Mbit/s) for servicing its bi-directional Ethernet frame traffic.

Each protocol encapsulation/decapsulation block can be independently configured to use one of the following protocols for transport of Ethernet MAC frames over a SONET/SDH link: Generic Framing Procedure (GFP), Link Access Procedure - SDH (LAPS), Link Access Procedure Frame Mode (LAPF) and Point-to-Point Protocol (PPP) with Bridging Control Protocol (BCP). By default, the protocol encapsulation blocks are configured for LAPS and the protocol decapsulation blocks are configured for Byte-Synchronous HDLC (i.e., LAPS mode).

Encapsulation configuration and status registers are described in Tables 35-47. Decapsulation registers are described in Tables 48-61.

SETTING THE ENCAPSULATION MODE

The mode of encapsulation is configurable according to the cTENCAPx register.

| cTENCAPx, bit 1 | cTENCAPx, bit 0 | Encapsulation Modes |
|-----------------|-----------------|---------------------|
| 0 | 0 | LAPS (Default). |
| 0 | 1 | LAPF. |
| 1 | 0 | GFP. |
| 1 | 1 | PPP (with BCP). |

The mode of decapsulation is configurable according to the cRDECAPx register. When the mode of decapsulation is configured to Byte-Synchronous HDLC, the cRHDLcx register must be used to select between LAPS or PPP (with BCP) type.

| cRDECAPx, bit 1 | cRECAPx, bit 0 | Decapsulation Modes |
|-----------------|----------------|--|
| 0 | 0 | Byte-Synchronous HDLC (Default). |
| 0 | 1 | LAPF. |
| 1 | 0 | GFP. |
| 1 | 1 | Disabled (i.e., no decapsulation is used and block is not used). |

| cRHDLcx, bit 3 | Byte-Synchronous HDLC Decapsulation Mode |
|----------------|--|
| 0 | LAPS (Default). |
| 1 | PPP (with BCP). |

CHANGING THE ENCAPSULATION MODE

Since encapsulation mode is chosen separately for each VCG, it is possible to change the encapsulation for a particular VCG without affecting traffic on VCGs that are not changing, provided the procedure described below is followed. During the time the encapsulation is changing, payload traffic for that VCG will be interrupted, so it is appropriate to send AIS on all tributaries associated with the changing VCG. High Order AIS can be forced by setting bit 0 of Address 0x1f960, 0x1f962, or 0x1f964 according to the High Order tributary desired. This will insert VC AIS. Set the pointer bytes to all 1s. Set bit 0 of Address 0x19ee6, 0x19eee, or 0x19ef6 depending upon which High Order tributary that is to have AIS inserted into it. To insert AIS into a Low Order tributary, bit 2 of Address 0x1a800+channel#x8 can be set.

As with the VCG reconfiguration procedures, the procedures below refer to TX and RX MAC Reset. See the reassignment procedures beginning on [page 124](#) for the details of TX and RX MAC Reset.

All modes except GFP Linear Mode:**Changing Encapsulation (Transmit path)**

Send AIS on all Tribs in the VCG
TX Channel X Reset ON
(Rx MACx Reset first, then VCGx Reset)
Change encapsulation mode of the VCG
TX Channel X Reset OFF
(VCGx Reset first, then Rx MACx Reset)
Remove AIS condition across the entire VCG

Changing Decapsulation (Receive path)

RX Channel X Reset ON
(VCGx Reset first, then TX MACx Reset)
Change decapsulation mode of the VCG
RX Channel X Reset OFF
(TX MACx Reset first, then VCGx Reset)

GFP Linear Mode:

In Linear Mode, multiple MAC channels are assigned to a single VCG, so all MACs that make up a VCG will need to be held in reset during the change.

Changing Encapsulation (Transmit path)

Send AIS on all Tribs in the VCG
TX Channel X Reset ON
(Rx MACx Reset for all MACs involved in the VCG, then VCGx Reset)
Change encapsulation mode of the VCG
TX Channel X Reset OFF
(VCGx Reset first, then Rx MACx Reset for all MACs involved)
Remove AIS condition across the entire VCG

Changing Decapsulation (Receive path)

RX Channel X Reset ON
(VCGx Reset first, then TX MACx Reset for all MACs involved in the VCG)
Change decapsulation mode of the VCG
RX Channel X Reset OFF
(TX MACx Reset for all MACs involved, then VCGx Reset)

GFP

Generic Framing Procedure (GFP) is protocol for mapping packet data into an octet-synchronous transport such as SONET/SDH. Unlike HDLC-based protocols, GFP does not use any special characters for frame delineation. Instead, it uses a cell delineation protocol, such as used by ATM, to encapsulate variable length packets. A fixed amount of overhead is required by the GFP encapsulation that is independent of the contents of the packet. The GFP protocol is specified in the ITU-T G.7041/Y.1303 standard.

Figure 52 shows the format of a GFP frame with a Ethernet MAC frame payload (denoted by the shaded area) relationship.

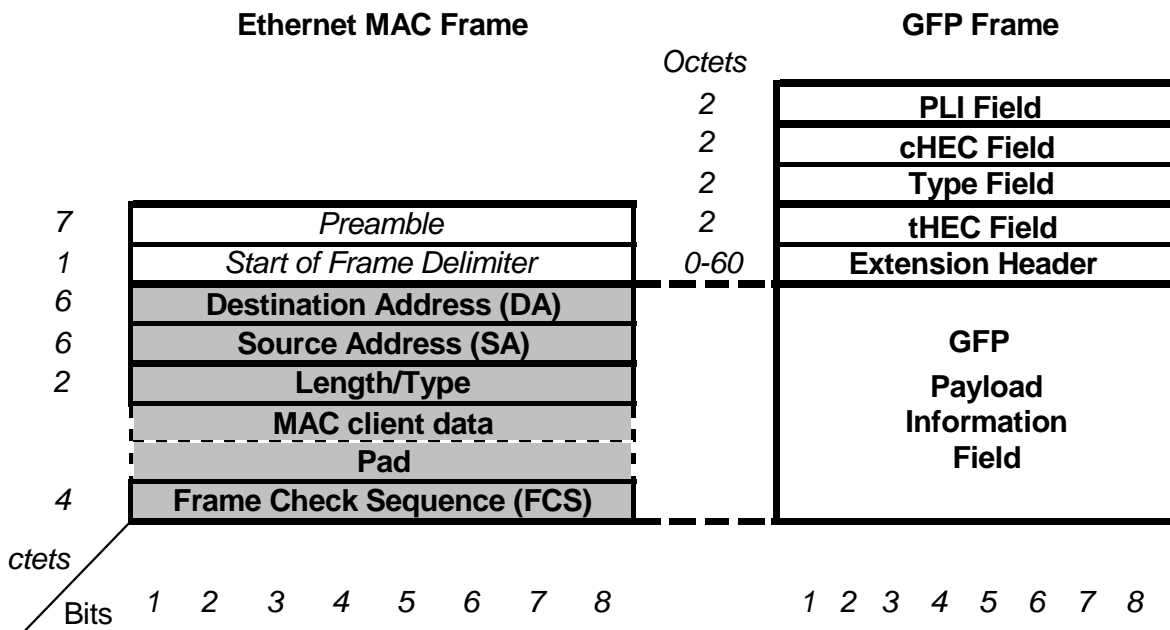


Figure 52. Format of GFP Frame with an Ethernet MAC Frame Payload

As shown in Figure 52, the GFP overhead can consist of two headers:

- A Core header, which consists of a two byte Payload Length Indicator (PLI) field and a two byte Core Header Error Control (cHEC) field. The Core header is used for frame delineation.
- A Payload header, which consists of a Type header and an Extension header (optional).
 - The Type header consists of a two byte Type field and a two byte Type Header Error Control (tHEC) field. The Type header is used to indicate the format and content of the Payload Information field. The EtherMap-3 Plus device supports frame based mapping for Ethernet MAC frames only.
 - The Extension header used for managing logical links, classes of service and source/destination addresses. Two forms of Extension headers are supported: Null Extension Header and Linear Extension Header. For Null Extension header support, no additional Extension header bytes are required (as per ITU-T G.7041/Y.1303). For Linear Extension header support, four bytes are required in addition to the Type header. These consist of a one byte Channel ID (CID) field, a one byte Spare (Reserved) field and a two byte Extension Header Error Control (eHEC) field.

As shown in Figure 52, the GFP Payload Information field is used to carry a complete Ethernet MAC frame. Further, an optional a Payload FCS field (4 bytes) may be inserted after the GFP Payload Information field. The optional Payload FCS field contains a 32-bit CRC sequence that protects the contents of the GFP Payload Information field only.

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for GFP, the following functions are supported:

- Encapsulate Ethernet MAC frame within a GFP frame. Each Ethernet MAC frame is encapsulated with a Core header, a Payload header and an optional Payload FCS field. For the Core header, the PLI and the cHEC fields are generated. For the Type header within Payload header, the PTI, PFI, EXI, UPI and tHEC fields are generated and configurable.

| | |
|-------------------|--|
| cPTIx(2-0) | GFP Payload Type Identifier Field Configuration |
| 0x0 - 0x7 | Contents of the PTI field for GFP Client Data frames only. (Default = 0x0) |

| | |
|--------------------|--|
| cPFIx bit 3 | GFP Payload FCS Indicator Control |
| 0 | The PFI bit within the GFP Payload Header is set to zero (0). GFP Payload FCS field is not inserted. (Default) |
| 1 | The PFI bit within the GFP Payload Header is set to one (1). GFP Payload FCS field is inserted. |

| | |
|-------------------|---|
| cEXIx(3-0) | GFP Extension Header Identifier Field Configuration |
| 0x0 - 0xF | Contents of the EXI field with in the GFP Payload header. (Default = 0x0) |

| | |
|-------------------|---|
| cUPIx(7-0) | GFP User Payload Identifier Field Configuration |
| 0x00 - 0xFF | Contents of the UPI field for GFP Client Data frames only. (Default = 0x01) |

For the Extension header (when in Linear frame mode) within Payload header, the CID, Spare and eHEC fields are generated and configurable.

| | |
|----------------------|---|
| cSPAREx (7-0) | GFP SPARE Field Configuration |
| 0x00 - 0xFF | Contents of the SPARE field within the GFP Extension header when using GFP Linear frame structure. (Default = 0x00) |

| | |
|----------------------|---|
| cFECIDx (7-0) | GFP Channel ID (CID) Field Configuration |
| 0x00 - 0xFF | Contents of the CID field within the GFP Extension header when using GFP Linear frame structure. (Default = 0x00) |

- GFP Core header scrambling can be enabled/disabled using the cTCSCRx register.

| | |
|----------------------|--|
| cTCSCRx bit 3 | GFP Core Header Scrambling Control |
| 0 | Enable scrambling of GFP Core Header only. (Default) |
| 1 | Disable scrambling of GFP Core Header only. |

- GFP Client Data and Client Management frame formats are supported.
- GFP Idle frame generation and insertion is supported.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

- Self-synchronous scrambler ($x^{43} + 1$ polynomial) for the Payload header, Payload Information field and Payload FCS field (optional) can be enabled/disabled according using the cTPSCRDx register. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

| cTPSCRDx bit 7 | GFP Payload Area Scrambling Control |
|---------------------------|---|
| 0 | Enable scrambling of GFP Payload area only. (Default) |
| 1 | Disable scrambling of GFP Payload area only. |

| cTSCRINITx bit 0 | GFP Payload Scrambler Initialization Control |
|-----------------------------|---|
| 0 | Scrambler is initialized with an all zeros state. (Default) |
| 1 | Scrambler is initialized with an all ones state. |

- 32-bit CRC sequence generation for the Payload FCS field (optional), over all octets of the GFP Payload Information field only, is supported.
- GFP frame multiplexing (when in Linear frame mode, cEXIx=1) from multiple Ethernet ports using a configurable scheduling algorithm is supported. For further details, please see the following section [“GFP Linear Frame Mode Operation” on page 150.](#)
- Detection and handling of errored Ethernet MAC frames on GFP ingress is supported. An alarm, aTETHERRx, is generated when an errored Ethernet MAC frame is detected and discarded for the transmit direction.
- Generation of GFP Client Signal Fail (CSF) indication is supported using the cTGFPTXCSFx register. The cTGFPTXCSFx allows to enter into the CSF mode (when set to 1). In that mode, every 100 ms, a CSF indication is transmitted to the line. The aTGFPXCSFx alarm indicates the activation of this mode. To exit from this mode, the cTGFPTXCSFx must be cleared.

| cTGFPTXCSFx bit 4 | GFP CSF Frame Transmit Control |
|------------------------------|---|
| 0 | Disable GFP CSF frame transmit mode. (Default) |
| 1 | Enable GFP CSF frame transmit mode. Beginning at the next GFP frame, a CSF indication is transmit every 100 ms period (i.e., no GFP Client Data frames can be transmitted). GFP Idle frames are transmitted in the interim. |

- Ability to insert errors in cHEC, tHEC and eHEC fields for testing is configurable respectively using the cTCHECERRx, cTTHECERRx and cTEHECERRx registers (self-clearing type, i.e., error is inserted only in a single frame). Furthermore, the cHEC generator can be initialized to a default state using the cTHECINITIALx register.

| cTCHECERRx bit 0 | GFP cHEC Error Insertion |
|-----------------------------|--|
| 0 | Disable cHEC error insertion. (Default) |
| 1 | Enable cHEC error insertion. Error is inserted by inverting the calculated cHEC field before transmission. |

| cTTHECERRx bit 1 | GFP tHEC Error Insertion |
|-----------------------------|--|
| 0 | Disable tHEC error insertion. (Default) |
| 1 | Enable tHEC error insertion. Error is inserted by inverting the calculated tHEC field before transmission. |

| cTEHECERRx bit 2 | GFP eHEC Error Insertion |
|-----------------------------|--|
| 0 | Disable eHEC error insertion. (Default) |
| 1 | Enable eHEC error insertion. Error is inserted by inverting the calculated eHEC field before transmission. |

| cTHECINITIALx bit 0 | GFP cHEC Generator Initialization Control |
|--------------------------------|--|
| 0 | cHEC generator is initialized with an all zeros state. (Default) |
| 1 | cHEC generator is initialized with an all ones state. |

For each GFP frame byte that is input to the cHEC/tHEC/eHEC generator, the bit-order within the byte can be swapped/reversed using the cTHECSWAPINx register.

| cTHECSWAPINx bit 0 | GFP cHEC/tHEC/eHEC Input Swap Control |
|-------------------------------|---|
| 0 | For each GFP frame byte at the input of the cHEC/tHEC/eHEC generator, the bit-order is preserved (i.e., not swapped/reversed). (Default). |
| 1 | For each GFP frame byte at the input of the cHEC/tHEC/eHEC generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). |

For each GFP cHEC/tHEC/eHEC byte from the cHEC/tHEC/eHEC generator, the bit-order within the cHEC/tHEC/eHEC byte can be swapped/reversed using the cTHECSWAPOUTx register before transmission to SONET/SDH. This does not affect the cHEC/tHEC/eHEC calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

| cTHECSWAPOUTx bit 0 | GFP cHEC/tHEC/eHEC Output Swap Control |
|--------------------------------|--|
| 0 | For each GFP cHEC/tHEC/eHEC byte that are output from the cHEC/tHEC/eHEC generator, the bit-order is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default). |
| 1 | For each GFP cHEC/tHEC/eHEC byte that are output from the cHEC/tHEC/eHEC generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH. |

- Ability to force abort generation is configurable using the cTABTGx register.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

- Detection of FIFO overflow/underflow conditions and size (maximum) of GFP Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTGPFMERRx alarm. The limit of the GFP Payload Information size is programmable using the register rTMAXFLx. The default value is 0x600. An alarm, aTGFPMAXERx, is generated when the size of the GFP Payload Information exceeds the value configured in rTMAXFLx register.

| cTMAXFLx (15-0) | GFP Payload Information Field Size |
|----------------------------|--|
| 0x0001 - 0x0640 | Indicates maximum number of octets in the GFP Payload Information field that is transmitted. (Default = 0x0640). When cPFIx=1, for a GFP payload length that exceeds the configured value in the cTMAXFLx register, the payload FCS is inverted before transmission to SONET/SDH. This will ensure that the terminating end discards the GFP frame. When cPFIx=0, for a GFP payload length that exceeds the configured value in the cTMAXFLx register, the current GFP payload is padded with 0xFF octets up to the configured length. |

- Ability to insert GFP Client Management/Control frames by the Host is supported. A 64-byte buffer (using 64 rTCTL_x(8-0) registers) per MAC is provided to store a single GFP Client Management/Control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the GFP Client Management/Control frame. The Host must write a valid formatted (including overhead bytes) GFP Client Management/Control frame into the buffer such that only additional processing steps performed are: Core header scrambling and Payload area scrambling (note: if payload FCS is required then this is provided by the Host). The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a GFP Client Management/Control frame.
 - Step 2: Once the GFP Client Management/Control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the GFP Client Management/Control frame is ready for transmission.
 - Step 3: During the next GFP inter-frame window (i.e., after completion of the GFP frame currently being transmitted), the stored GFP Client Management/Control frame is inserted into the datapath for transmission to SONET/SDH.
 - Step 4: Once the GFP Client Management/Control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-3 Plus and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available GFP Client Management/Control frame transmission.

| sTCTLBx bit 0 | GFP Client Management/Control Frame Buffer Status Indication |
|--------------------------|---|
| 0 | Buffer is empty and is able to receive a new GFP Client Management/Control frame. (Default) |
| 1 | Buffer is full and is not able to receive a new GFP Client Management/Control frame. |

| cCTLBRSTx bit 0 | GFP Client Management/Control Frame Buffer Reset Control |
|----------------------------|---|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

- Ability to filter mapping of select GFP frames for transmission to SONET/SDH is provided using cTGFPDUX register. Transmission of all GFP Client Management/Control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of GFP frames (i.e., including GFP Client Management/Control frames) for transmission to SONET/SDH.

| cTGFPDUX bit 9 | Selective GFP Frame Mapping Filter Control |
|---------------------------|---|
| 0 | GFP frames are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | GFP frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. |

| cTOFFx bit 6 | Generic GFP Frame Mapping Filter Control |
|-------------------------|---|
| 0 | All types of GFP frames (i.e., including GFP Client Management/Control frames) are allowed to pass for mapping into SONET/SDH. (Default)) |
| 1 | All types of GFP frames (i.e., including GFP Client Management/Control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only GFP IDLE frames are mapped into SONET/SDH. |

- Maintains transmit statistics counters. Two types of counters are provided: the total number of GFP frame payloads transmitted (rpcTGFPFRAMEx register) and the total number of GFP frame payload octets transmitted (rpcTGFPBYTEx register). These are also described in [Table 43](#).

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for GFP, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a GFP frame after frame delineation and sync is achieved. Robustness of GFP frame delineation acquisition using four virtual framers is configurable using the cRDELTAx register.

| cRDELTAx (2-0) | GFP Re-synchronization Control |
|---------------------------|--|
| 0x0 - 0x7 | Indicates values of DELTA to be used in the GFP delineation process. (Default = 0x1) |

- Processing of Null or Linear header types is configurable using the cRGFPHDRx register.

| cRGFPHDRx bit 10 | GFP Header Type Processing Control |
|-----------------------------|--|
| 0 | Only GFP NULL header type is processed. GFP frames received with other types of headers are discarded. (Default) |
| 1 | Only GFP LINEAR header type is processed. GFP frames received with other types of headers are discarded. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

- Core header descrambling can be enabled/disabled using the cRCDSCRx register.

| cRCDSCRx bit 0 | GFP Core Header De-scrambling Control |
|---------------------------|---|
| 0 | Enable de-scrambling of GFP Core Header only. (Default) |
| 1 | Disable de-scrambling of GFP Core Header only. |

- Single-bit error detection and correction in the Core header, Type header and Extension header is configurable. Multiple-bit error detection in the Core header, Type header and Extension header is supported and these frames are discarded.

| cRCORDISx bit 1 | GFP Core Header Single-bit Error Correction Control |
|----------------------------|---|
| 0 | For GFP Core header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default) |
| 1 | For GFP Core header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded. |

| cRTHECSx bit 2 | GFP Type Header Single-bit Error Correction Control |
|---------------------------|---|
| 0 | For GFP Type header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default) |
| 1 | For GFP Type header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded. |

| creHECSx bit 3 | GFP Extension Header Single-bit Error Correction Control |
|---------------------------|--|
| 0 | For GFP Extension header, enable Single-bit error correction and all received GFP frames detected with single-bit errors are corrected and passed. (Default) |
| 1 | For GFP Extension header, disable Single-bit error correction and all received GFP frames detected with single-bit errors are discarded. |

- GFP Client Data and Client Management frame formats are supported.
- GFP Idle frame detection and discard is supported.
- Self-synchronous descrambler ($x^{43} + 1$ polynomial) for the Payload header, Payload Information field and Payload FCS field (optional) can be enabled/disabled using the cRPSCRdx register.

| cRPSCRdx bit 4 | GFP Payload Area De-scrambling Control |
|---------------------------|--|
| 0 | Enable de-scrambling of GFP Payload area only. (Default) |
| 1 | Disable de-scrambling of GFP Payload area only. |

- 32-bit CRC sequence generation and checking for the Payload FCS field (optional), over all octets of the GFP Payload Information field only, is supported. An option is provided to pass or discard GFP frames with a FCS error using the cRGFPFCSErX register.

| cRGFPFCSErX bit 9 | GFP FCS Check Handling |
|------------------------------|--|
| 0 | Received GFP frames detected with a Payload FCS error (when FCS is present) are discarded. (Default) |
| 1 | Received GFP frames detected with a Payload FCS error (when FCS is present) are not discarded. |

- GFP frame demultiplexing (when in Linear frame mode) to multiple Ethernet ports based on configurable CID fields is supported. For further details, please see the following section [“GFP Linear Frame Mode Operation” on page 150.](#)
- Detection of GFP Client Signal Fail (CSF) indication is supported.
- Detection of size (maximum) of GFP Payload Information field via alarm and interrupt generation. The maximum size of the received GFP frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRGFPMAXERx, is generated when the size of the received GFP frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

| cRMAXFLx (15-0) | GFP Payload Information Field Size |
|----------------------------|---|
| 0x0001 - 0x0640 | Indicates maximum number of octets in a received GFP frame Payload Information field not including the payload header and FCS bytes. (Default = 0x0640) |

GFP HOST INSERTION/EXTRACTION OF MANAGEMENT/CONTROL FRAMES

- Ability to filter and extract GFP Client Management/Control frames by the Host is supported. A 64-byte buffer (using 64 rRLMlx_ (8-0) registers) per MAC is provided to store a single GFP Client Management/Control frame for the Host extraction. LMI is an acronym for Local Management Interface. The MSB bit (bit 8), when set to ‘1’, of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the GFP Client Management/Control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a GFP Client Management/Control frame such that only the following processing have been performed: GFP frame delineation, Core header descrambling and Payload area descrambling. The sRCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLBx status register (sRCTLBx=0) and enable a new Management/Control frame to be received. The rRGFPx register is used to configure the Payload Header Type field value to be checked in order to extract the GFP Client Management/Control frame and the rRCTLMASKA1x register is used as a bit level mask that is applied to the cRGFPx register. Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sRCTLBx=0 and the Host is not allowed to read for a new GFP Client Management/Control frame.
 - Step 2: Once the GFP Client Management/Control frame has been received, the sRCTLBx status register is set (sRCTLBx=1) by the EtherMap-3 Plus and an alarm, aRCTLRXx, is generated to indicate that the present GFP Client Management/Control frame is ready for extraction by the Host. No further GFP Client Management/Control frames may be written into the buffer (i.e., are discarded silently) until the sRCTLBx status register is cleared. If the received GFP Client Management/Control frame is bigger than the buffer size, an alarm, aRCTLBERRx, is generated and the buffer must be cleared/reset by the Host.



- Step 3: Once the GFP Client Management/Control frame has been extracted, the sRCTLBx status register is cleared (sRCTLBx=0) by the Host. This is to indicate that a follow-on received GFP Client Management/Control frame may be written into the buffer.

| sRCTLBx bit 0 | GFP Client Management/Control Frame Buffer Status Indication |
|---------------|--|
| 0 | Buffer is empty and no new GFP Client Management/Control frame has been received/stored. (Default) |
| 1 | Buffer is full with a new GFP Client Management/Control frame received. |

| cRCTLBRSTx bit 0 | GFP Client Management/Control Frame Buffer Reset Control |
|------------------|--|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

| rRGFPCPx(15-0) | GFP Client Management/Control frame Payload Header Type field Contents |
|-----------------|--|
| 0x0000 - 0xFFFF | Indicates contents of the GFP Client Management/Control frame Payload Header Type field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKA1 mask register. (Default = 0x8000) The structure of this register is as follows: PTI field value = Bits (15-13), PFI field value = Bit 12, EXI field value = Bits (11-8) and UPI field value = Bits (7-0). |

| rRCTLMASKA1x(15-0) | GFP Client Management/Control Frame Payload Header Type Field Contents Mask |
|--------------------|---|
| 0x0000 - 0xFFFF | Mask value that is applied to the rRGFPCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRGFPCPx register is used for filtering. (Default = 0xFFFF) |

- Ability to filter decapsulation of select GFP frames that are received from SONET/SDH is provided using cRGFPPDUx register. Reception of all GFP Client Management/Control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

| cRGFPPDUx bit 11 | Selective GFP Frame Decapsulation Filter Control |
|------------------|--|
| 0 | All GFP frame types received frames from SONET/SDH are allowed to be decapsulated. |
| 1 | Only GFP CSF and GFP Client Management/Control frames matching the rRGFPCPx register are allowed to be decapsulated. (Default) |

- Maintains receive statistics counters. All GFP receive side statistic counters are described in [Table 60](#).

GFP LINEAR FRAME MODE OPERATION

This mode allows support for scenarios where traffic from multiple independent MAC ports can be transported within a single VCG on SONET/SDH. The use of this mode requires configuration for Linear Frame Extension Header (which is added to the transported GFP frame) and of the CID tables (which configure the EtherMap-3 Plus for this operation).

Note that, for each VCG operating in GFP linear frame mode, the Extension Header field (EXI) within the GFP Payload header must be configured using the cEXI register for the transmit side. On the receive side, the cRGFPHDRx register must be configured to allow for correct processing of GFP Linear frames.

Transmit Side Linear Extension Header

The following registers are used for configuration inputs for the Transmit side Linear Extension Header bytes. These bytes are written in during system configuration, and are updated only in a static manner by Host processor.

SPARE field: for each MAC port, the cSPAREx register is used to configure the insertion value of the SPARE field within the Linear frame extension header.

Channel ID field (CID): For each MAC port, the cFECIDx register is used to configure the value of the CID field. This field will be common to all the frames transmitted from that MAC port; thus the contents of the cFECIDx register will represent the originating MAC port ID, when the frame is received by the far-end MAC port.

Transmit Side CID Configuration Tables

When a VCG operates in GFP linear mode, several MAC ports may be configured to multiplexed in it.

For any VCG, the CIDTablex_0, CIDTablex_1, CIDTablex_2, CIDTablex_3, CIDTablex_4, CIDTablex_5, CIDTablex_6, CIDTablex_7 registers will allow configuration of specific MAC ports that will multiplexed in that VCG.

These registers are only modified in a static manner by the Host upon initialization of the GFP link.

Note that the 8 MAC ports need not be all involved in the frame multiplexing process: for example, only a subset of the 'n' Ethernet ports may be multiplexed in a given VCG.

The operation of the CIDTablex registers can be represented with a example scheduling matrix, shown in [Table 7](#). This matrix is used to configure/control the multiplexing process for all the participating MAC ports configured for GFP Linear frame mode.

[Table 7](#) shows an example configuration of the scheduling matrix.

The VCG are represented along the vertical axis; on horizontal axis, the matrix represents the MAC ports that a VCG will service.

Table 7: Scheduling Matrix

| | | | | | | | | |
|------|---|---|---|---|---|---|---|---|
| VCG0 | 1 | 3 | 1 | 2 | 2 | 3 | 1 | 1 |
| VCG1 | 7 | 4 | 7 | 7 | 4 | 7 | N | N |
| VCG2 | N | N | N | N | N | N | N | N |
| VCG3 | N | N | N | N | N | N | N | N |
| VCG4 | N | N | N | N | N | N | N | N |
| VCG5 | N | N | N | N | N | N | N | N |
| VCG6 | N | N | N | N | N | N | N | N |
| VCG7 | 5 | 5 | 5 | 0 | 0 | 5 | 0 | 5 |



Scheduling Matrix Explanation:

1) The above matrix can be interpreted as follows:

- Transport path VCG0 (represented on the top row), will first transmit one frame from MAC1, then one frame from MAC3, then one frame from MAC1, then one frame from MAC2, then one frame from MAC2, then one frame from MAC3, then one frame from MAC1, then one frame from MAC1 etc. This cycle is continuously repeated.
- For transport path VCG 1, the MAC ports are serviced in this order: 7, 4, 7, 7, 4, 7, 4, 7, 7, 4, etc.
- For transport path VCG 2, there are no participating MAC ports.
- For transport path VCG 3, there are no participating MAC ports.
- For transport path VCG 4, there are no participating MAC ports.
- For transport path VCG 5, there are no participating MAC ports.
- For transport path VCG 6, there are no participating MAC ports.
- For transport path VCG 7, the MAC ports are serviced in this order: 5, 5, 5, 0, 0, 5, 0, 5, etc.

2) For each VCG row, each entry identifies the MAC port (configured for GFP Linear frame) to be serviced. Also, each entry represents only one complete Ethernet frame to be accepted each time into the multiplexing process.

3) 'N' represents a null value. The entries are read/serviced from left to right and wrap around to beginning of the cycle after servicing the last entry (i.e., entry number 7). A null value is used to terminate the servicing sequence order back to the first entry in the row (i.e., entry number 1). On initialization/power-up, all entries in the matrix are configured to a null value.

4) A null value cannot exist in the middle of the servicing sequence order (i.e., for example to be used to skip a service cycle). It is only allowed at the end of the servicing sequence order (see 2 above).

5) A MAC port is not used across/in multiple VCGs. However, within a single VCG, an Ethernet port is allowed multiple entries.

6) Only MAC ports configured for GFP Linear frame mode are allowed to participate in the scheduling matrix multiplexing process.

7) Ethernet port 3 is participating in the VCG 0 multiplexing process, this means that VCG 3 is only allowed to use other Ethernet ports if they are configured for GFP Linear Frame mode. No LAPS, LAPF or GFP NULL encapsulated Ethernet frames are allowed in VCG 3.

8) When operating in GFP Linear frame mode, the core header scrambling is performed by each of the separate MAC blocks before the GFP Linear frame is sent to the scheduling matrix for multiplexing.

9) When operating in GFP Linear frame mode, the payload scrambling is only performed after the GFP Linear frames have been multiplexed (as per the scheduling matrix) for each VCG separately.

10) Table 8 shows how the matrix is mapped in the EtherMap-3 Plus register memory map.

Table 8: Scheduling Matrix Mapped in the EtherMap-3 Plus Register Map

| | | | | | | | | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| x = 0 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 1 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 2 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 3 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |

| | | | | | | | | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| x = 4 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 5 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 6 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |
| x = 7 | CIDTablex_0 | CIDTablex_1 | CIDTablex_2 | CIDTablex_3 | CIDTablex_4 | CIDTablex_5 | CIDTablex_6 | CIDTablex_7 |

Each register CIDTablex_n comprises of four bits:

The most significant bit, CIDTablex_n [3], indicates "entry active" (when set to '1') or "entry not active" (when set to '0').

The remaining least significant bits, CIDTablex_n [2-0], indicate the select MAC port.

Receive Side Linear Extension Header

The cRGFPHDRx register is used to configure the type of GFP Payload header (i.e., NULL or LINEAR) processing for the GFP receive side.

For the receive direction, the cLECIDx register is used to assign/configure a unique local-end CID number to each receive side MAC port. This is used for processing a match condition between the local-end CID number and the CID field of the received GFP linear frame.

| cLECIDx (7-0) | GFP Local-end CID Value Configuration |
|--------------------------|---|
| 0x00-0xFF | Indicates a unique local-end CID number assigned to a local receive Ethernet port. (Default = 0x00) |

Receive Side CID Configuration Tables

For every VCG, operating in GFP Linear frame mode, being received from SONET/SDH side, there is a receive CID table using cRGFPCIDxi (where x = 0 - 7 GFP decapsulation blocks and i = 0 - 7 entries of the receive CID table) registers. Each table can be configured with up to eight CID values, corresponding to a maximum of eight Ethernet ports. This enables a filtering function to be made on the received GFP frames by comparing their CID field values with the table of expected CID values.

Example:

If VCG0 receives a frame, the CID field is compared against all the CID values listed in cRGFPCID01, cRGFPCID02, cRGFPCID03, cRGFPCID04, cRGFPCID05, cRGFPCID06 and cRGFPCID07 registers.

After this check, one of the following will happen:

- i) If CID value of the received frame matches any of CID values in the list, the frame is passed through, the Ethernet frame is decapsulated and forwarded to the local receive Ethernet port with the matching local-end CID number.
- ii) For all received GFP linear frames with matching CID values, when a far end receive CSF indication is detected for a select CID value, an alarm, aRGFPFECSFCIDxi (where x = 0 - 7 VCG decapsulation blocks; i = 0 - 7 entries of the receive CID table), is generated for that CID value.
- iii) When a match is not detected with the received GFP linear frame, the GFP frame is discarded and an alarm is generated. An alarm, aRGFPCIDERRx (where x = 0 - 7), is generated when the received GFP linear frame contains an unsupported CID value (i.e., a mismatch condition against the local end CID numbers).

Note that the order of the CID in the receive CID table is not important and that a CID number entry can only exist in once in the receive CID table for one given VCG (i.e., cannot have the same CID number entry exist in multiple tables). This check is performed by the software driver.

LAPS

LAPS is a HDLC-like framing structure to encapsulate IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The LAPS protocol is specified in the following standards: ITU-T X.85/Y.1321 and ITU-T X.86.

Figure 53 shows the format of a LAPS frame with a Ethernet MAC frame payload (denoted by the shaded area).

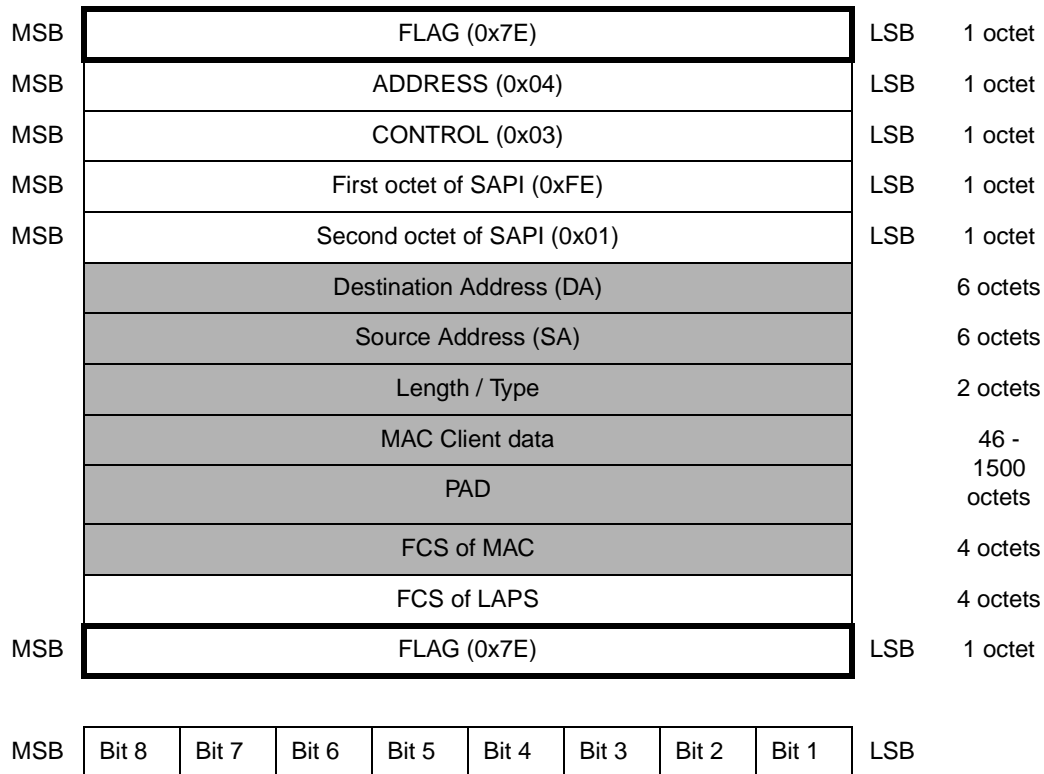


Figure 53. Format of LAPS Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for LAPS, the following functions are supported:

- Encapsulate Ethernet MAC frame within a LAPS frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), ADDRESS, CONTROL and SAPI fields, a 32-bit FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled through configuration. When field insertion is enabled, the contents of the ADDRESS, CONTROL and SAPI fields are configurable.

The management of the ADDRESS and CONTROL field is performed according to the cTACSELx register.

| cTACSELx bit 2 | cTACSELx bit 1 | LAPS ADDRESS and CONTROL Field Insertion Management |
|----------------|----------------|--|
| 0 | 0 | ADDRESS and CONTROL field contents set to all zeros. |

| cTACSELx bit 2 | cTACSELx bit 1 | LAPS ADDRESS and CONTROL Field Insertion Management |
|---------------------------|---------------------------|--|
| 0 | 1 | ADDRESS and CONTROL field contents contain fixed default values (i.e., ADDRESS=0x04, CONTROL=0x03). (Default). |
| 1 | 0 | Reserved. |
| 1 | 1 | ADDRESS and CONTROL field contents are taken from the rTACFDx register. |

The management of the SAPI field is controlled by the cTSAPIx register.

| cTSAPIx bit 3 | LAPS SAPI Field Insertion Management |
|--------------------------|---|
| 0 | SAPI field contents are taken from the rTSAPFDx register. |
| 1 | SAPI field contents set to all zeros. |

- Shared flag (START and CLOSING) generation is configurable. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive LAPS frames.

| cTFLAGx bit 0 | LAPS FLAG Insertion |
|--------------------------|---|
| 0 | A single flag are inserted between sequential LAPS frames (i.e., a shared flag). |
| 1 | Minimum of two flags are inserted between two consecutive LAPS frames. (Default). |

- Self-synchronous scrambler ($x^{43} + 1$ polynomial) can be enabled or disabled. The cTSCRDX register allows to enable/disable scrambling of LAPS frame. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

| cTSCRDX bit 2 | LAPS Scrambling Control |
|--------------------------|--|
| 0 | Enable scrambling of LAPS frame. (Default) |
| 1 | Disable scrambling of LAPS frame. |

| cTSCRINITx bit 0 | LAPS Scrambler Initialization Control |
|-----------------------------|---|
| 0 | Scrambler is initialized with an all zeros state. (Default) |
| 1 | Scrambler is initialized with an all ones state. |

- 32-bit FCS generation over all bits of the ADDRESS, CONTROL, SAPI, Payload Information field (shaded area as shown in [Figure 53](#)) not including any Flags and Abort sequences, is configurable using the cTFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALx register.

| cTFCSx bit 3 | LAPS FCS Generation/Calculation Mode |
|-------------------------|---|
| 0 | 32-bit FCS calculation is disabled and all four FCS field octets are not inserted. |
| 1 | 32-bit FCS calculation is enabled and all four FCS field octets are inserted. (Default) |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| cTFCSSINITIALx bit 0 | LAPS FCS Generator Initialization Control |
|---------------------------------|--|
| 0 | FCS generator is initialized with an all zeros state. |
| 1 | FCS generator is initialized with an all ones state. (Default) |

For each LAPS FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

| cTFCSSWAPINx bit 0 | LAPS FCS Input Swap Control |
|-------------------------------|--|
| 0 | For each LAPS frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default). |
| 1 | For each LAPS frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator. |

For each LAPS frame byte that is output from the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPOUTx register before it is transmitted to SONET/SDH.

| cTFCSSWAPOUTx bit 0 | LAPS FCS Output Swap Control |
|--------------------------------|--|
| 0 | For each LAPS FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default). |
| 1 | For each LAPS FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH. |

- Transparency processing (octet stuffing for Flags and Control Escape) is supported. Byte stuffing occurs between START and CLOSING Flags. Stuffing replaces each byte within a LAPS frame that matches the Flag or Control Escape code bytes with a two-byte sequence.
- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

| cTFCSEx bit 4 | LAPS FCS Error Insertion |
|--------------------------|--|
| 0 | The 32-bit FCS is transmitted without any error insertion. (Default) |
| 1 | The 32-bit FCS is errored (i.e., inverted) before transmission. |

- Ability to force abort generation is configurable. The cTABTGx register allows to force (cTABTGx=1) the abortion of the current encapsulated frame by sending 0x7D and 0x7E bytes.

| cTABTGx bit 5 | LAPS Transmit Abort Generation |
|--------------------------|---|
| 0 | No abort generated. (Default) |
| 1 | Current frame under transmission is aborted by 0x7D followed by 0x7E. |

- Detection of FIFO overflow/underflow conditions and size (maximum) of LAPS Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTLPFERRx alarm. The limit of the LAPS Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTMAXERx, is generated when the size of the LAPS Payload Information field exceeds the value configured in rTMAXFLx register.

| rTMAXFLx (15-0) | LAPS Payload Information Field Size |
|----------------------------|--|
| 0x0000 - 0x0640 | Indicates maximum number of octets in the LAPS Payload Information field that is transmitted. (Default = 0x0640) |

- Ability to insert LAPS control frames by the Host is supported. A 64-byte buffer (using 64 rTCTL_x(8-0) registers) per MAC is provided to store a single LAPS control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPS control frame. The Host must write a valid formatted (including overhead bytes) LAPS control frame into the buffer such that only additional processing steps performed are: FCS calculation, Byte stuffing, addition of flags and scrambling. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a LAPS control frame.
 - Step 2: Once the LAPS control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the LAPS control frame is ready for transmission.
 - Step 3: During the next LAPS inter-frame window (i.e., after the closing flag of the preceding LAPS frame and before the opening flag of the following LAPS frame), the stored LAPS control frame is inserted into the datapath for transmission to SONET/SDH.
 - Step 4: Once the LAPS control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-3 Plus and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available LAPS control frame transmission.

| sTCTLBx bit 0 | LAPS Control Frame Buffer Status Indication |
|--------------------------|--|
| 0 | Buffer is empty and is able to receive a new LAPS control frame. (Default) |
| 1 | Buffer is full and is not able to receive a new LAPS control frame. |

| cTCTLBRSTx bit 0 | LAPS Control Frame Buffer Reset Control |
|-----------------------------|--|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

- Ability to filter mapping of LAPS frames for transmission to SONET/SDH is provided using cTLPPDUx register. Transmission of all LAPS control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of LAPS frames (i.e., including LAPS control frames) for transmission to SONET/SDH.



| cTLPPDUx bit 4 | LAPS Frame Mapping Filter Control |
|---------------------------|--|
| 0 | LAPS frames are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | LAPS frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. |

| cTOFFx bit 6 | Generic LAPS Frame Mapping Filter Control |
|-------------------------|---|
| 0 | All types of LAPS frames (i.e., including LAPS control frames) are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | All types of LAPS frames (i.e., including LAPS control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH. |

- Maintains transmit statistics counters. Two types of counters are provided: the total number of LAPS frame payloads transmitted (rpcTLAPSFRAmEx register) and the total number of LAPS frame payload octets transmitted (rpcTLAPSBYTEx register) to SONET/SDH. These are also described in [Table 43](#).

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for LAPS, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a LAPS frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of the ADDRESS, CONTROL and SAPI fields of a received LAPS frame are validated against configurable stored values. Further, an option to discard frames with a mismatch of one of the fields, is configurable.
The cRACSELx(1:0) register allows to configure the type of check to be performed on the ADDRESS and CONTROL field contents.

| cRACSELx bit 4 | cRACSELx bit 3 | LAPS ADDRESS and CONTROL Field Contents Check Control |
|---------------------------|---------------------------|--|
| 0 | 0 | ADDRESS and CONTROL field contents check is disabled. Assume ADDRESS and CONTROL fields are present. |
| 0 | 1 | ADDRESS and CONTROL field contents checked against fixed values (i.e., ADDRESS=0x04, CONTROL=0x03). (Default). |
| 1 | 0 | Reserved. |
| 1 | 1 | ADDRESS and CONTROL field contents checked against the contents of rRACFDx register. |

The cRSAPIx register allows to configure the type of check to be performed on the SAPI field contents.

| cRSAPIx bit 5 | LAPS SAPI Field Contents Check Control |
|--------------------------|--|
| 0 | SAPI field contents check is disabled. |
| 1 | SAPI field contents checked against the contents of rRSAPFDx register. (Default) |

The cRMMAEx register allows to configure handling of LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents. An alarm, aRLPSFMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL or SAPI field contents of the received LAPS frame.

| cRMMAEx bit 6 | LAPS Field Contents Mismatch Management |
|--------------------------|--|
| 0 | LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is discarded. (Default) |
| 1 | LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is not discarded |

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRFLAGx register allows to configure the type of flag detection between consecutive LAPS frames.

| cRFLAGx bit 1 | LAPS FLAG Detection Control |
|--------------------------|--|
| 0 | At least two flags to be detected between LAPS frames. (Default). |
| 1 | At least a single flag to be detected between LAPS frames (i.e., a shared flag). |

- Self-synchronous de-scrambler ($x^{43} + 1$ polynomial) can be enabled or disabled according to the cRSCRDx register.

| cRSCRDx bit 0 | LAPS Descrambling Control |
|--------------------------|--|
| 0 | Enable descrambling of LAPS frame. (Default) |
| 1 | Disable descrambling of LAPS frame. |

- 32-bit FCS generation and checking over all bits of the ADDRESS, CONTROL, SAPI, Payload Information field (shaded area as shown in [Figure 53](#)) not including any Flags and Abort sequences, is configurable. The cRFCSx register allows to configure enable/disable LAPS FCS checking. Further, an option is provided to process or discard LAPS frames with a FCS error according to the cRLPFCSERx register. An alarm, aRLPSFCSER, is generated when a LAPS frame is received with FCS error.

| cRFCSx bit 2 | LAPS FCS Check |
|-------------------------|--|
| 0 | 32-bit FCS check is disabled and assume all four FCS field octets are not present. |
| 1 | 32-bit FCS check is enabled. (Default) |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| cRLPFCSERx bit 8 | LAPS FCS Check Handling (used when FCS Check is Enabled as per cRFCSSx Register) |
|-----------------------------|---|
| 0 | Received LAPS frames with FCS error are discarded. (Default) |
| 1 | Received LAPS frames with FCS error are not discarded. |

For each received LAPS frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

| cRFCSSWAPINx bit 0 | LAPS FCS Input Swap Control |
|-------------------------------|--|
| 0 | For each received LAPS frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default). |
| 1 | For each received LAPS frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). |

- Transparency processing (octet de-stuffing for Flags and Control Escape) is supported. Byte de-stuffing occurs between START and CLOSING Flags.
- Ability to detect an abort indication via alarm and interrupt generation. To force an abort of the current frame, the cRLPABTGx register needs to set to 1. An alarm, aRLPSABTDx, is generated when an abort indication is detected (i.e., receive 0x7D followed by 0x7E) on the receive side.

| cRLPABTGx bit 7 | LAPS Abort Generation |
|----------------------------|---|
| 0 | No frame aborted. (Default) |
| 1 | Current frame under receive is aborted. |

- Processing of invalid LAPS frames as per ITU-T X.86.
- Detection of size (minimum and maximum) of LAPS Payload Information field via alarm and interrupt generation. The minimum size of the received LAPS frame (in octets) can be configured using the rRLPMINFLx register (i.e., the number of octets between the opening and closing flags). An alarm, aRLPSSHTRx, is generated when the size of received LAPS frame is less than six octets and this frame is aborted. An alarm, aRLPSMINERx, is generated when the size of the received LAPS frame is greater than six octets but less than the value configured in rRLPMINFLx register. The maximum size of the received LAPS frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRLPSMAXERx, is generated when the size of the received LAPS frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

| rRLPMINFLx(7-0) | LAPS Frame Size |
|------------------------|---|
| 0x06 - 0xFF | Indicates minimum number of octets present in a received LAPS frame between opening and closing flags. (Default = 0x06) |

| rRMAXFLx(15-0) | LAPS Frame Payload Information Field Size |
|-----------------------|---|
| 0x0001 - 0x0640 | Indicates maximum number of octets in a received LAPS frame Payload Information field. (Default = 0x0640) |

- Ability to filter and extract LAPS control frames by the Host is supported. A 64-byte buffer (using 64 rRLMlx_ (8-0) registers) per MAC is provided to store a single LAPS control frame for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPS control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a LAPS control frame such that only the following processing have been performed: FCS Check, Byte de-stuffing and removal of flags. The sRCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLBx status register (sRCTLBx=0) and enable a new Management/Control frame to be received. The rRLPCPx register is used to configure the SAPI value to be checked in order to extract the LAPS control frame and the rRCLMASKA1x register is used as a bit level mask that is applied to the cRLPCPx register. Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sRCTLBx=0 and the Host is not allowed to read for a new LAPS control frame.
 - Step 2: Once the LAPS control frame has been received, the sRCTLBx status register is set (sRCTLBx=1) by the EtherMap-3 Plus and an alarm, aRCLTRXx, is generated to indicate that the present LAPS control frame is ready for extraction by the Host. No further LAPS control frames may be written into the buffer (i.e., are discarded silently) until the sRCTLBx status register is cleared. If the received LAPS control frame is bigger than the buffer size, an alarm, aRCLTBERRx, is generated and the buffer must be cleared/reset by the Host.
 - Step 3: Once the LAPS control frame has been extracted, the sRCTLBx status register is cleared (sRCTLBx=0) by the Host. This is to indicate that a follow-on received LAPS control frame may be written into the buffer.

| sRCTLBx bit 0 | LAPS Control Frame Buffer Status Indication |
|----------------------|---|
| 0 | Buffer is empty and no new LAPS control frame has been received/stored. (Default) |
| 1 | Buffer is full with a new LAPS control frame received. |

| cRCTLBRSTx bit 0 | LAPS Control Frame Buffer Reset Control |
|-------------------------|--|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

| rRLPCPx(15-0) | LAPS Control Frame SAPI Field Contents |
|----------------------|--|
| 0x0000 - 0xFFFF | Indicates contents of the LAPS control frame SAPI field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCLMASKA1 mask register. (Default = 0x0000) |

| rRCLMASKA1x(15-0) | LAPS Control Frame SAPI Field Contents Mask |
|--------------------------|---|
| 0x0000 - 0xFFFF | Mask value that is applied to the rRPLCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPLCPx register is used for filtering. (Default = 0xFFFF) |



- Ability to filter decapsulation of select LAPS frames (i.e., frames with SAPI field contents equal to rRSAPFDx register) that are received from SONET/SDH is provided using cRLPPDUx register. Reception of all LAPS control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

| cRLPPDUx bit 9 | Selective LAPS Frame Decapsulation Filter Control |
|---------------------------|---|
| 0 | Received frames from SONET/SDH, with SAPI field contents equal to rRSAPFDx register, are allowed to be decapsulated. |
| 1 | Received frames from SONET/SDH, with SAPI field contents equal to rRSAPFDx register, are not allowed (i.e., frames are discarded) to be decapsulated. (Default) |

- Maintains receive statistics counters. All LAPS receive side statistic counters are described in [Table 60](#).

LAPF

LAPF is a HDLC-like framing structure to encapsulate IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The LAPF protocol is specified in the ITU-T Q.922 standard. Use of LAPF for transport of Ethernet MAC frames is specified in RFC2427. The EtherMap-3 Plus device only supports LAPF Bridged frame format.

Figure 54 shows the format of a LAPF Bridged frame with a Ethernet MAC frame payload (denoted by the shaded area).

| Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Octet |
|--|-------|-------|-------|-------|-------|-------|-----------|-------|
| FLAG (0x7E) | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Upper DLCI | | | | | | C/R | EA (0x00) | 2 |
| Lower DLCI | | | | FECN | BECN | DE | EA (0x01) | 3 |
| CONTROL (0x03) | | | | | | | | 4 |
| PAD (0x00) | | | | | | | | 5 |
| NLPID (0x80) | | | | | | | | 6 |
| OUI (0x00) | | | | | | | | 7 |
| OUI (0x80) | | | | | | | | 8 |
| OUI (0xC2) | | | | | | | | 9 |
| PID (0x00) | | | | | | | | 10 |
| PID (0x07) | | | | | | | | 11 |
| First octet of MAC Destination Address | | | | | | | | 12 |
| MAC Frame | | | | | | | | |
| Last octet of MAC Frame before LAN FCS | | | | | | | | N-3 |
| LAPF Frame Check Sequence (FCS) - First Octet | | | | | | | | N-2 |
| LAPF Frame Check Sequence (FCS) - Second Octet | | | | | | | | N-1 |
| FLAG (0x7E) | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | N |

Figure 54. Format of LAPF Bridged Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for LAPF, the following functions are supported:

- Encapsulate Ethernet MAC frame within a LAPF frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields, a 16-bit FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled through configuration according to the cTLFACNOPSELx register. The insertion of the PAD field is also configurable using the cTLFPADx register. When other field insertion is enabled, the contents of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields are configurable according to the registers described into the [Table 37](#).



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| cTLFACNOPSELx bit 3 | LAPF ADDRESS, CONTROL, NLPID, OUI and PID Field Insertion Management |
|--------------------------------|---|
| 0 | LAPF overhead field content insertion is enabled. (Default) ADDRESS field contents taken from rTDLCLx, cTCRx, cTFECNx, cTBECLx and cTDEx registers. CONTROL field contents taken from rTLFCNTLx register. NLPID field contents taken from rTNLPIDx register. OUI field contents taken from rTOUIx register. PID field contents taken from rTPIDx register. |
| 1 | ADDRESS, CONTROL, NLPID, OUI and PID field contents insertion is disabled. These fields are all set to zero. |

| cTLFPADx bit 4 | LAPF PAD Field Insertion Management |
|---------------------------|---|
| 0 | PAD field insertion is enabled and the field contents are taken from the rTPADn register. (Default) |
| 1 | PAD field insertion is disabled (i.e., no PAD field is present in the LAPF frame). |

- Shared flag (START and CLOSING) generation is configurable according to the cTFLAGx register. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive LAPF frames
- 16-bit FCS generation over all bits of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI, PID and Payload Information fields (shaded area as shown in [Figure 54](#)) not including any Flags and Abort sequences, is configurable using the cTFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALx register.

| cTFCSx bit 3 | LAPF FCS Generation/Calculation Mode |
|-------------------------|--|
| 0 | 16-bit FCS calculation is disabled and all FCS field octets are not inserted. |
| 1 | 16-bit FCS calculation is enabled and all FCS field octets are inserted. (Default) |

| cTFCSINITIALx bit 0 | LAPF FCS Generator Initialization Control |
|--------------------------------|--|
| 0 | FCS generator is initialized with an all zeros state. |
| 1 | FCS generator is initialized with an all ones state. (Default) |

For each LAPF frame byte that is input to the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSSWAPINx register.

| cTFCSSWAPINx bit 0 | LAPF FCS Input Swap Control |
|-------------------------------|--|
| 0 | For each LAPF frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default). |
| 1 | For each LAPF frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator. |

For each LAPF FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

| cTFCSSWAPOUTx bit 0 | LAPF FCS Output Swap Control |
|--------------------------------|--|
| 0 | For each LAPF FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default). |
| 1 | For each LAPF FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH. |

- Ability to insert LAPF LMI control frames by the Host is supported. A 64-byte buffer (using 64 rTCTL_x(8-0) registers) per MAC is provided to store a single LAPF LMI control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPF LMI control frame. The Host must write a valid formatted (including overhead bytes) LAPF LMI control frame into the buffer such that only additional processing steps performed are: FCS calculation, Bit stuffing and addition of flags. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBxRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a LAPF LMI control frame.
 - Step 2: Once the LAPF LMI control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the LAPF LMI control frame is ready for transmission.
 - Step 3: During the next LAPF inter-frame window (i.e., after the closing flag of the preceding LAPF frame and before the opening flag of the following LAPF frame), the stored LAPF LMI control frame is inserted into the datapath for transmission to SONET/SDH.
 - Step 4: Once the LAPF LMI control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-3 Plus and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available LAPF LMI control frame transmission.



| sTCTLBx bit 0 | LAPF LMI Control Frame Buffer Status Indication |
|--------------------------|--|
| 0 | Buffer is empty and is able to receive a new LAPF LMI control frame. (Default) |
| 1 | Buffer is full and is not able to receive a new LAPF LMI control frame. |

| cTCTLBRSTx bit 0 | LAPF LMI Control Frame Buffer Reset Control |
|-----------------------------|--|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

- Ability to filter mapping of LAPF frames for transmission to SONET/SDH is provided using cTLFPDUx register. Transmission of all LAPF LMI control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of LAPF frames (i.e., including LAPF LMI control frames) for transmission to SONET/SDH.

| cTLFPDUx bit 6 | LAPF Frame Mapping Filter Control |
|---------------------------|--|
| 0 | LAPF frames are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | LAPF frames are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. |

| cTOFFx bit 6 | Generic LAPF Frame Mapping Filter Control |
|-------------------------|---|
| 0 | All types of LAPF frames (i.e., including LAPF LMI control frames) are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | All types of LAPF frames (i.e., including LAPF LMI control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH. |

- Transparency processing (bit-stuffing for Flags and Control Escape) is supported. Bit stuffing occurs between START and CLOSING Flags.
- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

| cTFCSEx bit 4 | LAPF FCS Error Insertion |
|--------------------------|--|
| 0 | The 16-bit FCS is transmitted without any error insertion. (Default) |
| 1 | The 16-bit FCS is errored (i.e., inverted) before transmission. |

- Detection of FIFO overflow/underflow conditions and size (maximum) of LAPF Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTLFFERRx alarm. The limit of the LAPF Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTLFMAXERx, is generated when the size of the LAPF Payload Information field exceeds the value configured in rTMAXFLx register.

| rTMAXFLx(15-0) | LAPF Payload Information Field Size |
|-----------------|--|
| 0x0001 - 0x0640 | Indicates maximum number of octets in the LAPF Payload Information field that is transmitted. (Default = 0x0640) |

- Maintains transmit statistics counters. Two types of counters are provided: the total number of LAPF frame payloads transmitted (rpcTLAPFFRAMEx register) and the total number of LAPF frame payload octets transmitted (rpcTLAPFBYTEx register) to SONET/SDH. These are also described in [Table 43](#).

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for LAPF, the following functions are supported:

- Decapsulate to extract the Ethernet MAC frame from within a LAPF frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI and PID fields of a received LAPF frame are validated against configurable stored values. The cRLFACNOPSELx register allows to configure the type of check to performed on the ADDRESS and CONTROL and NLPID and OUI and PID field contents.

| cRLFACNOPSELx bit 1 | LAPF ADDRESS, CONTROL, NLPID, OUI and PID Field Insertion Management |
|---------------------|--|
| 0 | LAPF overhead field content checking is enabled. (Default) ADDRESS field contents are checked against rRLFADRx register. CONTROL field contents are checked against rRLFCNTLx register. NLPID field contents are checked against rRNLPIDx register. OUI field contents are checked against rROUIx register. PID field contents are checked against rRPIDx register. Register rRPIDx is configured to indicate whether the Ethernet frame FCS is present or not. When rRPIDx=0x0001, the Ethernet frame FCS is present and this Ethernet frame is transmitted onto the Ethernet line. When rRPIDx=0x0007, the Ethernet frame FCS is not present and a new Ethernet FCS (4-bytes) is generated and appended by the MAC before the frame is transmitted onto the Ethernet line. |
| 1 | ADDRESS, CONTROL, NLPID, OUI and PID field contents checking is disabled. |

The cRLFPADx register allows to configure the type of check to performed on the PAD field contents.

| cRLFPADx bit 3 | LAPF PAD Field Insertion Management |
|----------------|--|
| 0 | LAPF PAD field contents checking is enabled for only one PAD field in the received LAPF frame. (Default). The PAD field contents are checked against rRPADx register. |
| 1 | LAPF PAD field contents checking is disabled. Assume no PAD field is present in the received LAPF frame. |



The cRLFMMAEx register allows to configure handling of LAPF frames with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents. An alarm, aRLFMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents of the received LAPF frame.

| cRLFMMAEx bit 5 | LAPF Field Contents Mismatch Management |
|-----------------|---|
| 0 | LAPF frame with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents are discarded. (Default) |
| 1 | LAPS frame with mismatched ADDRESS or CONTROL or PAD or NLPID or OUI or PID field contents are not discarded |

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRLFFLAGx register allows to configure the type of flag detection between consecutive LAPF frames.

| cRLFFLAGx bit 0 | LAPF FLAG Detection |
|-----------------|--|
| 0 | At least two flags to be detected between LAPF frames. (Default). |
| 1 | At least a single flag to be detected between LAPF frames (i.e., a shared flag). |

- 16-bit FCS generation and checking over all bits of DLCI, C/R, EA, FECN, BECN, DE, CONTROL, PAD, NLPID, OUI, PID and Payload Information fields (shaded area as shown in Figure 54) not including any Flags and Abort sequences, is configurable using the cRLFFCSx register. Further, an option is provided to process or discard LAPF frames with a FCS error using the cRLFFCSERx register. An alarm, aRLFFCSERx, is generated when a LAPF frame is received with FCS error.

| cRLFFCSx bit 6 | LAPF FCS Check |
|----------------|---|
| 0 | 16-bit FCS check is disabled and assume all two FCS field octets are not present. |
| 1 | 16-bit FCS check is enabled. (Default) |

| cRLFFCSERx bit 7 | LAPF FCS Check Handling (used when FCS Check is Enabled as per cRLFFCSx Register) |
|------------------|---|
| 0 | Received LAPF frames with FCS error are discarded. (Default) |
| 1 | Received LAPF frames with FCS error are not discarded. |

- For each received LAPF frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

| cRFCSSWAPINx bit 0 | LAPF FCS Input Swap Control |
|--------------------|--|
| 0 | For each received LAPF frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default). |
| 1 | For each received LAPF frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). |

- Transparency processing (bit de-stuffing for Flags and Control Escape) is supported. Bit de-stuffing occurs between START and CLOSING Flags.
- Ability to filter and extract LAPF LMI frames by the Host is supported. A 64-byte buffer (using 64 rRLMlx_(8-0) registers) per MAC is provided to store a single LAPF LMI buffer for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the LAPF LMI frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a LAPF LMI frame such that only the following processing have been performed: FCS Check, Bit de-stuffing and removal of flags. The sRCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLBx status register (sRCTLBx=0) and enable a new Management/Control frame to be received. The cRLMIDLCLx register allows to determine the DLCI field value to be checked in order to extract the LAPF LMI frame. Below is an example of how the Host can use this buffer:
 - Step 1: If the LMI buffer is empty, sRCTLBx=0 and the Host is not allowed to read for a new LAPF LMI frame.
 - Step 2: Once the LAPF LMI frame has been received, the sRCTLBx status register is set (sRCTLBx=1) by the EtherMap-3 Plus and an alarm, aRCTLRXx, is generated to indicate that the present LAPF LMI frame is ready for extraction by the Host. No further LAPF LMI frames may be written into the buffer (i.e., are discarded silently) until the sRCTLBx status register is cleared. If the received LAPF LMI frame is bigger than the buffer size, an alarm, aRCTLBERRx, is generated and the buffer must be cleared/reset by the Host.
 - Step 3: Once the LAPF LMI frame has been extracted, the sRCTLBx status register is cleared (sRCTLBx=0) by the Host. This is to indicate that a follow-on received LAPF LMI frame may be written into the buffer.

| sRCTLBx bit 0 | LAPF LMI Frame Buffer Status Indication |
|--------------------------|---|
| 0 | Buffer is empty and no new LAPF LMI frame has been received/stored. (Default) |
| 1 | Buffer is full with a new LAPF LMI frame received. |

| cRCTLBRSTx bit 0 | LAPF LMI Frame Buffer Reset Control |
|-----------------------------|--|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

| cRLMIDLCLx bit 2 | LAPF LMI DLCI Field Value Selection |
|-----------------------------|--|
| 0 | LAPF LMI frames with DLCI=0 are filtered for extraction by the Host. (Default) |
| 1 | LAPF LMI frames with DLCI=1023 are filtered for extraction by the Host. |

- Ability to detect an abort indication via aRLFABTDx alarm and interrupt generation.
- Processing of invalid LAPF frames as per ITU-T Q.922.
- Detection of size (minimum and maximum) of LAPF Payload Information field via alarm and interrupt generation. The minimum size of the received LAPF frame (in octets) can be configured using the rRLFMINFLx register (i.e., the number of octets between the ADDRESS field and closing flag). An alarm, aRLFFSERx, is generated when the size of received LAPF frame is less than three octets (between ADDRESS field and closing flag) and this frame is aborted. An alarm, aRLFMINERx, is generated when the size of the received LAPF frame is greater than three octets but less than the value configured in



rRLFMINFLx register. The maximum size of the received LAPF frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRLFMAXERx, is generated when the size of the received LAPF frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

| rRLFMINFLx(7-0) | LAPF Frame Size |
|-----------------|--|
| 0x03 - 0xFF | Indicates minimum number of octets present in a received LAPF frame between ADDRESS field and closing flag. (Default = 0x06) |

| rRMAXFLx(15-0) | LAPF Frame Payload Information Field Size |
|-----------------|---|
| 0x0001 - 0x0640 | Indicates maximum number of octets in a received LAPF frame Payload Information field. (Default = 0x0640) |

- Provide an indication on the status of the LAPF link for the receive side. The sLNKSTSx status register is used by the Host to determine the state of the LAPF link. After power-up/reset, the LAPF link is set to a 'down' state. While the link is in a 'down' state, only LAPF flags and LMI frames are allowed to be received, Furthermore, while in a 'down' state, when either 64 consecutive LAPF flags or a single valid LAPF frame are received, the link state is set to an 'up' state. An alarm, aLNKSTSUPx, is generated to indicate a change of LAPF link to an 'up' state. While the link is in 'up' state, when 256 consecutive '1's are received, the link state is set to a 'down' state. An alarm, aLNKSTSDWNx, is generated to indicate a change of LAPF link to a 'down' state. Note in case of AIS on the telecom bus side, the sLNKSTSx status information is only updated in VC-4 mode. In all other virtual concatenation modes, AIS is filtered earlier in the SONET to Ethernet direction.
- Ability to filter decapsulation of LAPF frames that are received from SONET/SDH is provided using cRLFPDUx register. Reception of all LAPF LMI frames (i.e., control frames destined for extraction by Host) are not affected by this register.

| cRLFPDUx bit 7 | Selective LAPF Frame Decapsulation Filter Control |
|----------------|---|
| 0 | All LAPF frame types received frames from SONET/SDH are allowed to be decapsulated. |
| 1 | Only LAPF LMI frames matching the cRLMIDLCIx register are allowed to be decapsulated. (Default) |

- Maintains receive statistics counters. All LAPF receive side statistic counters are described in [Table 60](#).

PPP (WITH BCP AND LCP SUPPORT)

The Point-to-Point Protocol (PPP) is a HDLC-like framing structure and provides a standard method for transporting multi-protocol datagrams over point-to-point links. PPP can be used to encapsulate IEEE 802.3 Ethernet MAC frame to provide a point-to-point Full Duplex simultaneous bidirectional operation. The PPP Bridging Control Protocol (BCP) is specified in the following standards: RFC 1661, RFC 1662, RFC 2878, RFC 2615 and RFC 3518.

Figure 55 shows the format of a PPP frame with an Ethernet MAC frame payload (denoted by the shaded area).

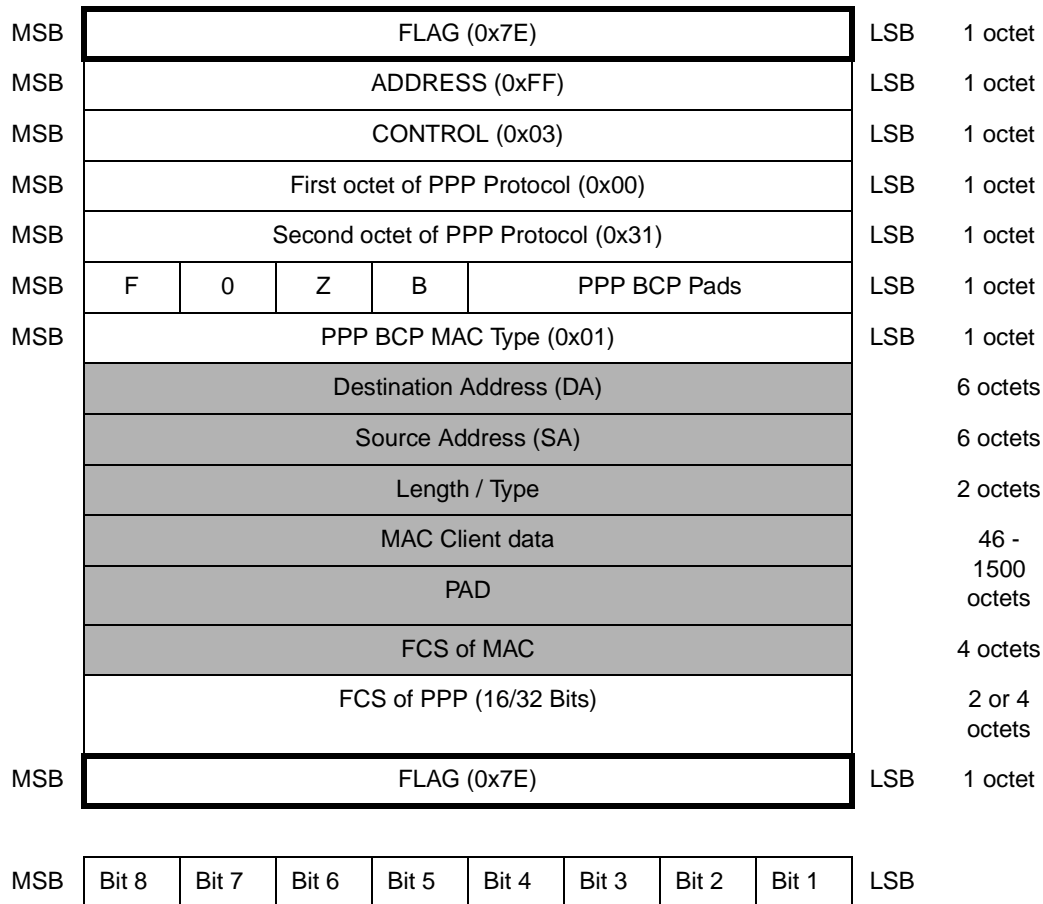


Figure 55. Format of PPP Frame with an Ethernet MAC Frame Payload

In the transmit direction (Ethernet-to-SONET/SDH), for each encapsulation block configured for PPP, the following functions are supported:

- Encapsulate Ethernet MAC frame within a PPP frame. Each Ethernet MAC frame is encapsulated with a START FLAG (0x7E), ADDRESS, CONTROL, PPP Protocol, PPP BCP Flags, PPP BCP Pad and PPP BCP MAC Type fields, a 16/32-bit PPP FCS field, and a CLOSING FLAG (0x7E). Field insertions except the START Flag can be disabled via configuration. When field insertion is enabled, the contents of the ADDRESS, CONTROL, PPP Protocol and PPP BCP MAC Type fields are configurable.

The management of the ADDRESS and CONTROL field is performed according to the cTPPACSELx register.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| cTPPACSELx bit 3 | cTPPACSELx bit 2 | PPP ADDRESS and CONTROL Field Insertion Management |
|-----------------------------|-----------------------------|--|
| 0 | 0 | ADDRESS and CONTROL field contents set to all zeros. |
| 0 | 1 | ADDRESS and CONTROL field contents contain fixed default values (i.e., ADDRESS=0xFF, CONTROL=0x03). (Default). |
| 1 | 0 | Reserved. |
| 1 | 1 | ADDRESS and CONTROL field contents are taken from the rTPPACFDx register. |

The management of the PPP Protocol field is controlled by the cTPPPIx register.

| cTPPPIx bit 4 | PPP Protocol Field Insertion Management |
|--------------------------|--|
| 1 | PPP Protocol field contents set to all zeros. |
| 0 | PPP Protocol field contents are taken from the rTPPFDx register. (Default) |

The management of the PPP BCP flag fields (i.e., F, 0, Z, B fields) is performed according to the following registers: cTBCPFLGFx, cTBCPFLG0x, cTBCPFLGZx and cTBCPFLGBx.

| cTBCPFLGFx bit 5 | PPP BCP Flag F Field Insertion Management |
|-----------------------------|---|
| 1 | PPP BCP Flag F field contents set to a one ('1'). (Default) |
| 0 | PPP BCP Flag F field contents set to a zero ('0'). |

| cTBCPFLG0x bit 6 | PPP BCP Flag 0 Field Insertion Management |
|-----------------------------|--|
| 1 | PPP BCP Flag 0 field contents set to a one ('1'). |
| 0 | PPP BCP Flag 0 field contents set to a zero ('0'). (Default) |

| cTBCPFLGZx bit 7 | PPP BCP Flag Z Field Insertion Management |
|-----------------------------|---|
| 1 | PPP BCP Flag Z field contents set to a one ('1'). (Default) |
| 0 | PPP BCP Flag Z field contents set to a zero ('0'). |

| cTBCPFLGBx bit 8 | PPP BCP Flag B Field Insertion Management |
|-----------------------------|--|
| 1 | PPP BCP Flag B field contents set to a one ('1'). |
| 0 | PPP BCP Flag B field contents set to a zero ('0'). (Default) |

The contents of the PPP BCP MAC Type field is configurable using the rTBCPMACx register.

| rTBCPMACx (15-8) | PPP BCP MAC Type Field Contents Configuration |
|-----------------------------|---|
| 0x00 - 0xFF | Indicates contents of the PPP BCP MAC Type field. (Default = 0x01) |

- PPP padding mode to be applied is configurable. The rTBCPPDMODEx register allows to configure the type of padding mode to be used.

| rTBCPPDMODEx bit 1 | rTBCPPDMODEx bit 0 | PPP Padding Mode Control |
|-------------------------------|-------------------------------|--|
| 0 | 0 | No padding is applied. (Default) |
| 0 | 1 | A fixed padding mode is enabled. In this mode, the PPP BCP PADS field is inserted to indicate the number of pad octets that have been inserted within the PPP frame payload. |
| 1 | 0 | Reserved. |
| 1 | 1 | Reserved. |

The PPP padding octet alignment mode (i.e., used when fixed padding mode is enabled) is controlled by the rTBCPPDALIGNx register.

| rTBCPPDALIGNx bit 3 | rTBCPPDALIGNx bit 2 | PPP Padding Octet Alignment Mode Control |
|--------------------------------|--------------------------------|--|
| 0 | 0 | A 2 octet alignment boundary is used. (Default) |
| 0 | 1 | A 4 octet alignment boundary is used. |
| 1 | 0 | A 8 octet alignment boundary is used. |
| 1 | 1 | A 16 octet alignment boundary is used. |

The PPP padding octet alignment calculation mode (i.e., used when fixed padding mode is enabled) is controlled by the cTBCPPDCALCx register.

| cTBCPPDCALCx bit 10 | PPP Padding Octet Alignment Calculation Mode Control |
|--------------------------------|--|
| 0 | PPP padding octet alignment calculation is over payload area only. (Default). |
| 1 | PPP padding octet alignment calculation is over entire frame area. (i.e., header, payload and FCS bytes) |

The contents of the PPP pad octet (i.e., used when fixed padding mode is enabled) is configurable using the rTBCPPADx register.



| rTBCPPADx (7-0) | PPP Pad Field Contents Configuration |
|--------------------|---|
| 0x00 - 0xFF | Indicates contents of the PPP pad octet when fixed padding mode is enabled. (Default = 0x00) |

- Shared flag (START and CLOSING) generation is configurable. Idle flag generation and insertion is supported. The cTFLAGx register allows to configure the minimum number of flags to be inserted between two consecutive PPP frames.

| cTFLAGx bit 0 | PPP FLAG Insertion |
|------------------|--|
| 0 | A single flag are inserted between sequential PPP frames (i.e., a shared flag). |
| 1 | Minimum of two flags are inserted between two consecutive PPP frames. (Default). |

- Self-synchronous scrambler ($x^{43} + 1$ polynomial) can be enabled or disabled. The cTSCRDX register allows to enable/disable scrambling of PPP frame. Furthermore, the scrambler can be initialized to a default state using the cTSCRINITx register.

| cTSCRDX bit 2 | PPP Scrambling Control |
|------------------|---|
| 0 | Enable scrambling of PPP frame. (Default) |
| 1 | Disable scrambling of PPP frame. |

| cTSCRINITx bit 0 | PPP Scrambler Initialization Control |
|---------------------|---|
| 0 | Scrambler is initialized with an all zeros state. (Default) |
| 1 | Scrambler is initialized with an all ones state. |

- 16 or 32-bit FCS generation over all bits of the ADDRESS, CONTROL, PPP Control, PPP BCP Flags, PPP BCP Pads, PPP BCP MAC Type, Payload Information area (shaded area as shown in [Figure 55](#)) and optional pad octet fields not including any Opening/Closing flags and Abort sequences, is configurable using the cTPFCSx register. Furthermore, the FCS generator can be initialized to a default state using the cTFCSINITIALx register.

| cTPFCSx bit 1 | cTPFCSx bit 0 | PPP FCS Generation/Calculation Mode |
|------------------|------------------|---|
| 0 | 0 | 16 and 32-Bit FCS generation/calculation is disabled. FCS octets are not inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH. |
| 0 | 1 | Reserved. |

| cTPFCSx bit 1 | cTPFCSx bit 0 | PPP FCS Generation/Calculation Mode |
|--------------------------|--------------------------|---|
| 1 | 0 | Only 16 FCS generation/calculation is enabled. Two FCS octets are inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH. |
| 1 | 1 | Only 32 FCS generation/calculation is enabled. Four FCS octets are inserted in the PPP frame. This also applies to any PPP BCP Control frames received from the host and for transmission to SONET/SDH. (Default) |

| cTFCSINITIALx bit 0 | PPP FCS Generator Initialization Control |
|--------------------------------|--|
| 0 | FCS generator is initialized with an all zeros state. |
| 1 | FCS generator is initialized with an all ones state. (Default) |

For each PPP frame byte that is input to the FCS generator, the bit-order within the byte can be swapped/reversed using the cTFCSWAPINx register.

| cTFCSWAPINx bit 0 | PPP FCS Input Swap Control |
|------------------------------|---|
| 0 | For each PPP frame byte at the input of the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed). In this case, the least significant bit of each byte is input first into the FCS generator. (Default). |
| 1 | For each PPP frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). In this case, the most significant bit of each byte is input first into the FCS generator. |

For each PPP FCS byte from the FCS generator, the bit-order within the FCS byte can be swapped/reversed using the cTFCSWAPOUTx register before transmission to SONET/SDH. This does not affect the FCS calculation result but rather the transmission bit-order of each FCS byte into SONET/SDH.

| cTFCSWAPOUTx bit 0 | PPP FCS Output Swap Control |
|-------------------------------|---|
| 0 | For each PPP FCS byte output from the FCS generator, the bit-order within is preserved (i.e., not swapped/reversed) before being transmit to SONET/SDH. (Default). |
| 1 | For each PPP FCS byte output from the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa) before being transmit to SONET/SDH. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

- Ability to insert FCS errors for testing is configurable using a self-clearing cTFCSEx register (i.e., error is inserted only in a single frame).

| cTFCSEx bit 4 | PPP FCS Error Insertion |
|--------------------------|--|
| 0 | The 16 or 32-bit FCS is transmitted without any error insertion. (Default) |
| 1 | The 16 or 32-bit FCS is errored (i.e., inverted) before transmission. |

- Transparency processing (octet stuffing for Flags and Control Escape) is supported. Byte stuffing occurs between START and CLOSING Flags. Stuffing replaces each byte within a PPP frame that matches the Flag or Control Escape code bytes with a two-byte sequence.
- Ability to force abort generation is configurable. The cTABTGx register allows to force (cTABTGx=1) the abortion of the current encapsulated frame by sending 0x7D and 0x7E bytes.

| cTABTGx bit 5 | PPP Transmit Abort Generation |
|--------------------------|--|
| 0 | No abort generated. (Default) |
| 1 | Current frame under transmission (including BCP control frame from the host) is aborted by 0x7D followed by 0x7E. The first aborted packet will contain two abort indications. |

- Detection of FIFO overflow/underflow conditions and size (maximum) of PPP Payload Information field via alarm and interrupt generation. The detection of FIFO overflow/underflow is observable according to the aTPPFERRx alarm. The limit of the PPP Payload Information size (in octets) is programmable using the rTMAXFLx(15-0) register. An alarm, aTPPMAXERx, is generated when the size of the PPP Payload Information field exceeds the value configured in rTMAXFLx register.

| rTMAXFLx (15-0) | PPP Payload Information Field Size |
|----------------------------|---|
| 0x0001 - 0x0640 | Indicates maximum number of octets in the PPP Payload Information field that is transmitted. (Default = 0x0640) |

- Ability to insert PPP Link Control Protocol (LCP)/Network Control Protocol (NCP) control frames by the Host is supported. A 64-byte buffer (using 64 rTCTL_x(8-0) registers) per MAC is provided to store a single PPP LCP/NCP control frame from the Host. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the PPP LCP/NCP control frame. The Host must write a valid formatted (including overhead bytes) PPP control frame into the buffer such that only additional processing steps performed are: FCS calculation, Byte stuffing, addition of flags and scrambling. The sTCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cTCTLBRSTx register. This reset will cause the buffer to discard its contents and clear the sTCTLBx status register (sTCTLBx=0). Below is an example of how the Host can use this buffer:
 - Step 1: If the buffer is empty, sTCTLBx=0 and the Host is allowed to write a PPP LCP/NCP control frame.
 - Step 2: Once the PPP LCP/NCP control frame has been written. the Host must set the sTCTLBx status register (sTCTLBx=1) to indicate that the PPP LCP/NCP control frame is ready for transmission.
 - Step 3: During the next PPP inter-frame window (i.e., after the closing flag of the preceding PPP frame and before the opening flag of the following PPP frame), the stored PPP LCP/NCP control frame is inserted into the datapath for transmission to SONET/SDH.

- Step 4: Once the PPP LCP/NCP control frame has been transmitted, the sTCTLBx status register is cleared (sTCTLBx=0) by the EtherMap-3 Plus and an alarm, aTCTLx, is generated. The alarm can be used to provide an indication of the next available PPP LCP/NCP control frame transmission.

| sTCTLBx bit 0 | PPP LCP/NCP Control Frame Buffer Status Indication |
|--------------------------|---|
| 0 | Buffer is empty and is able to receive a new PPP LCP/NCP control frame. (Default) |
| 1 | Buffer is full and is not able to receive a new PPP LCP/NCP control frame. |

| cTCTLBRSTx bit 0 | PPP LCP/NCP Control Frame Buffer Reset Control |
|-----------------------------|---|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

- Ability to filter mapping of select PPP frames (i.e., frames with PPP Protocol field=0x0031) for transmission to SONET/SDH is provided using cTBPDUX register. Transmission of all PPP LCP/NCP control frames (i.e., control frames received from the Host) are not affected by this register. The cTOFFx register can be used to filter mapping of all types of PPP frames (i.e., including PPP LCP/NCP control frames) for transmission to SONET/SDH.

| cTBPDUX bit 9 | Selective PPP Frame Mapping Filter Control |
|--------------------------|---|
| 0 | PPP frames with PPP Protocol field=0x0031 are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | Only LCP/NCP-BCP frames from the host are mapped. |

| cTOFFx bit 6 | Generic PPP Frame Mapping Filter Control |
|-------------------------|---|
| 0 | All types of PPP frames (i.e., including PPP LCP/NCP control frames) are allowed to pass for mapping into SONET/SDH. (Default) |
| 1 | All types of PPP frames (i.e., including PPP LCP/NCP control frames) are not allowed (i.e., frames are discarded) to pass for mapping into SONET/SDH. Only flags (i.e., 0x7E octets) are mapped into SONET/SDH. |

- Maintains transmit statistics counters. Two types of counters are provided: the total number of PPP frame payloads transmitted (rpcTPPFRAMEx register) and the total number of PPP frame payload octets transmitted (rpcTPPBYTEx register) to SONET/SDH. These are also described in [Table 43](#).

In the receive direction (SONET/SDH-to-Ethernet), for each decapsulation block configured for PPP, the following functions are supported:



- Decapsulate to extract the Ethernet MAC frame from within a PPP frame. Field extraction and checking, except the START and CLOSING Flags, can be disabled through configuration. When field extraction and checking is enabled, the contents of the ADDRESS, CONTROL, PPP Protocol, PPP BCP Flags and PPP BCP MAC Type fields of a received PPP frame are validated against configurable stored values. Further, an option to discard frames with a mismatch of one of the fields, is configurable. The cRPACSELx register allows to configure the type of check to be performed on the ADDRESS and CONTROL field contents of a received PPP frame.

| cRPACSELx bit 2 | cRPACSELx bit 1 | PPP ADDRESS and CONTROL Field Contents Check Control |
|--------------------|--------------------|--|
| 0 | 0 | ADDRESS and CONTROL field contents check is disabled. Assume ADDRESS and CONTROL fields are present. |
| 0 | 1 | ADDRESS and CONTROL field contents checked against fixed values (i.e., ADDRESS=0xFF, CONTROL=0x03). (Default). |
| 1 | 0 | Reserved. |
| 1 | 1 | ADDRESS and CONTROL field contents checked against the contents of rRPACFDx register. |

The cRPPROTx register allows to configure the type of check to be performed on the PPP Protocol fields contents of a received PPP frame.

| cRPPROTx bit 11 | PPP Protocol Field Contents Check Control |
|--------------------|--|
| 0 | PPP Protocol field contents check is disabled. |
| 1 | PPP Protocol field contents checked against the contents of rRPPROTFDx register. (Default) |

The cRPFGx register allows to configure the type of check to be performed on the PPP BCP flags field contents of a received PPP frame.

| cRPFGx bit 5 | PPP BCP Flags Field Contents Check Control |
|-----------------|---|
| 0 | PPP BCP flags field contents check is disabled. |
| 1 | PPP BCP flags field contents checked against the contents of rRPFGFDx register. (Default) |

The cRPMACx register allows to configure the type of check to be performed on the PPP BCP MAC Type field contents of a received PPP frame.

| cRPMACx bit 7 | PPP BCP MAC Type Field Contents Check Control |
|------------------|---|
| 0 | PPP BCP MAC Type field contents check is disabled. |
| 1 | PPP BCP MAC Type field contents checked against the contents of rRPMACFDx register. (Default) |

The cRPACMMEx register allows to configure handling of PPP frame with mismatched ADDRESS or CONTROL field contents. An alarm, aRPACMMx, is generated when a mismatch is detected on the ADDRESS or CONTROL field contents of a received PPP frame.

| cRPACMMEx bit 0 | PPP ADDRESS and CONTROL Field Contents Mismatch Management |
|----------------------------|---|
| 0 | PPP frame with mismatched ADDRESS or CONTROL field contents is discarded. (Default) |
| 1 | PPP frame with mismatched ADDRESS or CONTROL field contents is not discarded. |

The cRPPROTMMEx register allows to configure handling of PPP frame with mismatched PPP Protocol field contents. An alarm, aRPPROTMMx, is generated when a mismatch is detected on the PPP Protocol field contents of a received PPP frame.

| cRPPROTMMEx bit 12 | PPP Protocol Field Contents Mismatch Management |
|-------------------------------|---|
| 0 | PPP frame with mismatched PPP Protocol field contents is discarded. (Default) |
| 1 | PPP frame with mismatched PPP Protocol field contents is not discarded. |

The cRPFGMMAEx register allows to configure handling of PPP frame with mismatched PPP BCP flags field contents. An alarm, aRPFGMMAx, is generated when a mismatch is detected on the PPP BCP flags field contents of a received PPP frame.

| cRPFGMMAEx bit 6 | PPP PCP Flags Field Contents Mismatch Management |
|-----------------------------|--|
| 0 | PPP frame with mismatched PPP BCP flags field contents is discarded. (Default) |
| 1 | PPP frame with mismatched PPP BCP flags field contents is not discarded. |

The cRPMACMMEx register allows to configure handling of PPP frame with mismatched PPP BCP MAC Type field contents. An alarm, aRPMACMMx, is generated when a mismatch is detected on the PPP BCP MAC Type field contents of a received PPP frame.

| cRPMACMMEx bit 8 | PPP BCP MAC Type Field Contents Mismatch Management |
|-----------------------------|---|
| 0 | PPP frame with mismatched PPP BCP MAC Type field contents is discarded. (Default) |
| 1 | PPP frame with mismatched PPP BCP MAC Type field contents is not discarded. |

- Shared flag (START and CLOSING) detection is configurable. Idle flag detection and discard is supported. The cRFLAGx register allows to configure the type of flag detection between consecutive PPP frames.

| cRFLAGx bit 1 | PPP Flag Detection Control |
|--------------------------|---|
| 0 | At least two flags to be detected between PPP frames. (Default). |
| 1 | At least a single flag to be detected between PPP frames (i.e., a shared flag). |



- Self-synchronous de-scrambler ($x^{43} + 1$ polynomial) can be enabled or disabled according to the cRSCRDx register.

| cRSCRDx bit 0 | PPP Descrambling Control |
|------------------|---|
| 0 | Enable descrambling of PPP frame. (Default) |
| 1 | Disable descrambling of PPP frame. |

- 16 or 32-bit FCS generation and checking over all bits of the ADDRESS, CONTROL, PPP Control, PPP BCP Flags, PPP BCP Pads, PPP BCP MAC Type, Payload Information area (shaded area as shown in Figure 55) not including any Opening/Closing flags and Abort sequences, is configurable. The cRPFCSx register allows to configure enable/disable PPP FCS checking and the cRPCRCSx register allows to configure for use of 16 or 32-bit FCS checking. Further, an option is provided to process or discard PPP frames with a FCS error according to the cRPPPCSERx register. An alarm, aRPPPFCSER, is generated when a PPP frame is received with FCS error.

| cRPFCSx bit 4 | PPP FCS Check Control |
|------------------|--|
| 0 | FCS check is disabled and assume all FCS field octets are not present. |
| 1 | FCS check is enabled. (Default) |

| cRPPPCSERx bit 10 | PPP FCS Check Handling (used when FCS Check is Enabled as per cRPFCSx Register) |
|----------------------|---|
| 0 | Received PPP frames with FCS error are discarded. (Default) |
| 1 | Received PPP frames with FCS error are not discarded. |

| cRPCRCSx bit 3 | PPP FCS Check Type Select Control |
|-------------------|-------------------------------------|
| 0 | 32-bit FCS checking used. (Default) |
| 1 | 16-bit FCS checking used. |

For each received PPP frame byte that is input to the FCS generator for checking, the bit-order within the byte can be swapped/reversed using the cRFCSSWAPINx register.

| cRFCSSWAPINx bit 0 | PPP FCS Input Swap Control |
|-----------------------|---|
| 0 | For each received PPP frame byte at the input of the FCS generator, the bit-order is preserved (i.e., not swapped/reversed). (Default). |
| 1 | For each received PPP frame byte at the input of the FCS generator, the bit-order is not preserved (i.e., is swapped/reversed, MSB becomes LSB and vice-versa). |

- Transparency processing (octet de-stuffing for Flags and Control Escape) is supported. Byte de-stuffing occurs between START and CLOSING Flags.

- Ability to detect an abort indication via alarm and interrupt generation. To force an abort of the current frame, the cRPPPABTGx register needs to be set to 1. An alarm, aRPPPABTDx, is generated when an abort indication is detected (i.e., receive 0x7D followed by 0x7E) on the receive side.

| cRPPPABTGx bit 9 | PPP Abort Generation |
|-----------------------------|---|
| 0 | No frame aborted. (Default) |
| 1 | Current frame under receive is aborted. |

- Ability to select type of padding mode used for decapsulation using cRBCPPDMODEx register.

| cRBCPPDMODEx bit 13 | PPP Padding Mode Control |
|--------------------------------|---------------------------------|
| 0 | A fixed padding mode is used. |
| 1 | No padding is used. (Default) |

- Processing of invalid PPP frames as per RFC 1662.
- Detection of size (minimum and maximum) of PPP frame via alarm and interrupt generation. The minimum size of the received PPP frame (in octets) can be configured using the rRPPPMINFLx register (i.e., the number of octets between the opening and closing flags). An alarm, aRPPPSHTERx, is generated when the size of received PPP frame is less than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets and this frame is aborted. An alarm, aRPPPMINERx, is generated when the size of the received PPP frame is greater than four (when using 16-bit FCS) or six (when using 32-bit FCS) octets but less than the value configured in rRPPPMINFLx register. The maximum size of the received PPP frame Payload Information field (in octets) can be configured using the rRMAXFLx register. An alarm, aRPPPMAXERx, is generated when the size of the received PPP frame Payload Information field (in octets) exceeds the value configured in rRMAXFLx register.

| rRPPPMINFLx(7-0) | PPP Frame Size |
|-------------------------|--|
| 0x04 - 0xFF | Indicates minimum number of octets present in a received PPP frame between opening and closing flags. (Default = 0x04 when using 16-bit FCS or 0x06 when using 32-bit FCS) |

| rRMAXFLx(15-0) | PPP Frame Payload Information Field Size |
|-----------------------|--|
| 0x0001 - 0x0640 | Indicates maximum number of octets in a received PPP frame Payload Information field. (Default = 0x0640) |

- Ability to filter and extract PPP LCP/NCP control frames by the Host is supported. A 64-byte buffer (using 64 rRLMlx_ (8-0) registers) per MAC is provided to store a single PPP LCP/NCP control frame for the Host extraction. The MSB bit (bit 8), when set to '1', of each byte is a valid bit to indicate that the current byte (bits 7-0) is part of the PPP LCP/NCP control frame. This applies up to the first byte where MSB = 0 (bit 8); all other bytes after and including the byte with MSB = 0 are not a part of the received frame. The Host is provided with a PPP LCP/NCP control frame such that only the following processing have been performed: FCS Check, Byte de-stuffing and removal of flags. The sRCTLBx status register (which can be accessed by the Host) is provided to indicate the empty/full state of the buffer. A reset of the buffer can be generated using the cRCTLBRSTx register. This reset will clear the sRCTLBx status register (sRCTLBx=0) and enable a new Management/Control frame to be received. The rRPLCPx register is used to configure the PPP Protocol field value to be checked in order to extract the PPP LCP control frame and the rRCLMASKA1x register is used as a bit level mask that is applied to the cRPLCPx register. The rRPNCPx register is used to



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

configure the PPP Protocol field value to be checked in order to extract the PPP NCP control frame and the rRCTLMASKB1x register is used as a bit level mask that is applied to the cRPNCPx register. Below is an example of how the Host can use this buffer:

- Step 1: If the buffer is empty, sRCTLBx=0 and the Host is not allowed to read for a new PPP LCP/NCP control frame.
- Step 2: Once the PPP LCP/NCP control frame has been received, the sRCTLBx status register is set (sRCTLBx=1) by the EtherMap-3 Plus and an alarm, aRCTLRXx, is generated to indicate that the present PPP LCP/NCP control frame is ready for extraction by the Host. No further PPP LCP/NCP control frames may be written into the buffer (i.e., are discarded silently) until the sRCTLBx status register is cleared. If the received PPP LCP/NCP control frame is bigger than the buffer size, an alarm, aRCTLBERRx, is generated and the buffer must be cleared/reset by the Host.
- Step 3: Once the PPP LCP/NCP control frame has been extracted, the sRCTLBx status register is cleared (sRCTLBx=0) by the Host. This is to indicate that a follow-on received PPP LCP/NCP control frame may be written into the buffer.

| sRCTLBx bit 0 | PPP LCP/NCP Control Frame Buffer Status Indication |
|--------------------------|--|
| 0 | Buffer is empty and no new PPP LCP/NCP control frame has been received/stored. (Default) |
| 1 | Buffer is full with a new PPP LCP/NCP control frame received. |

| cRCTLBRSTx bit 0 | PPP LCP/NCP Control Frame Buffer Reset Control |
|-----------------------------|---|
| 0 | Buffer is not in reset state. (Default) |
| 1 | Buffer is in reset state. |

| rRPLCPx(15-0) | PPP LCP Control Frame PPP Protocol Field Contents |
|----------------------|--|
| 0x0000 - 0xFFFF | Indicates contents of the LCP control frame PPP Protocol field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKA1 mask register. (Default = 0xC021) |

| rRCTLMASKA1x(15-0) | PPP LCP Control Frame PPP Protocol Field Contents Mask |
|---------------------------|---|
| 0x0000 - 0xFFFF | Mask value that is applied to the rRPLCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPLCPx register is used for filtering. (Default = 0xFFFF) |

| rRPNCPx(15-0) | PPP NCP Control Frame PPP Protocol Field Contents |
|----------------------|--|
| 0x0000 - 0xFFFF | Indicates contents of the NCP control frame PPP Protocol field that is checked against a received control frame for extraction to the Host. This is used in conjunction with the rRCTLMASKB1 mask register. (Default = 0x8031) |

| rRCTLMASKB1x(15-0) | PPP NCP Control Frame PPP Protocol Field Contents Mask |
|---------------------------|---|
| 0x0000 - 0xFFFF | Mask value that is applied to the rRPNCPx register contents to aid in the filtering process. When the mask bit is set (i.e., to a 1), the corresponding bit of the rRPNCPx register is used for filtering. (Default = 0xFFFF) |

- Ability to filter decapsulation of select PPP frames (i.e., frames with PPP Protocol field=0x0031) that are received from SONET/SDH is provided using cRBPDUx register. Reception of all PPP LCP/NCP control frames (i.e., control frames destined for extraction by Host) are not affected by this register.

| cRBPDUx bit 14 | Selective PPP Frame Decapsulation Filter Control |
|---------------------------|--|
| 0 | Received frames from SONET/SDH, with PPP Protocol field=0x0031, are allowed to be decapsulated. |
| 1 | Received frames from SONET/SDH, with PPP Protocol field=0x0031, are not allowed (i.e., frames are discarded) to be decapsulated. (Default) |

Maintains receive statistics counters. All PPP receive side statistic counters are described in [Table 60](#).

SDRAM CONTROLLER

SDRAM MEMORY INTERFACE

This interface is used to allow the mapper to connect an external SDRAM memory module. The external SDRAM memory module is used for buffering of Ethernet traffic in both directions. The SDRAM memory interface comprises of a 32-bit data bus, 13-bit address bus, 2-bit bank address bus, 3-bit command bus, Input/Output Mask bus, SDRAM clock (100 MHz) and control enable signals.

The SDRAM control block will interface to a dynamic random access memory containing up to 256 Mbits. It will support a quad-bank SDRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

The external SDRAM will be accessed as 4 banks of 2k/4k/8k rows by 256 columns by 32 bits. In the memory module selected, the Precharge command period (Trp) minimum value must be lower than 30 ns.

Read and write accesses to the external SDRAM are burst oriented using alternative bank switching; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with issuing an ACTIVE command, which is then followed by a READ or WRITE command. The address bits issued together with the ACTIVE command are used to select the bank and row to be accessed (BA(1-0) select the bank, ADDR(12-0) select the row). The address bits issued together with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM interface block will require programmable READ or WRITE burst lengths of 2 locations. An auto precharge function may be enabled, to initiate a self-timed row precharge, at the end of the burst sequence.

The 128 Mb SDRAM interface block may change the row/column address on every clock cycle, in order to achieve a high-speed, fully random access. One bank is precharged while accessing one of the other three banks, thus hiding the precharge cycles and providing high-speed, random-access operation.

The 128 Mb SDRAM control block will operate with 3.3V, low-power memory block.

All inputs and outputs are LVTTTL-compatible.

CAS Latency

Please refer to timing diagrams SDRAM_read, SDRAM_write. The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The SDRAM interface can be programmed for a latency of three clock cycles: this means that data will be sampled on the third rising edge after the READ command is issued.

BANK/ROW Activation

Please refer to timing diagrams SDRAM_read, SDRAM_write. The ACTIVE command will be issued before any READ or WRITE. After issuing the ACTIVE, the READ or WRITE command may be issued to the selected row, subject to the t RCD specification. The SDRAM block controller is designed for SDRAM having a t RCD (MIN) lower than 20 ns; with a clock rate of 100 MHz, this implies that a READ or WRITE command can be issued on the second rising edge after the ACTIVE command was issued.

Commands

The following commands can be issued by the SDRAM controller (see the table below):

| Command Name | CS | RAS | CAS | WE | MASK | ADDR | BA | NOTES |
|----------------------|----|-----|-----|----|------|----------|--------|-------|
| Command Inhibit Nop | H | X | X | X | X | X | X | |
| No Operation Nop | L | H | H | H | X | X | X | |
| Active | L | L | H | H | X | BANK/ROW | | |
| Read | L | H | L | H | L/H | BANK/COL | | |
| Write | L | H | L | L | L/H | BANK/COL | VALID | |
| Precharge | L | L | H | L | X | CODE | X | |
| Auto Or Self Refresh | L | L | L | H | X | X | X | |
| Load Mode Register | L | L | L | L | X | OP-CODE | X | |
| Write Enable | | | | | L | | ACTIVE | |
| Write Inhibit | | | | | H | | HIGH Z | |

RESET CONFIGURATION OF SDRAM CONTROLLER

Upon reset the SDRAM CONTROLLER is configured for a 4 bank 64 Mbit SDRAM. The default configuration parameters are:

- SDRAM size: SDRAM_CFG = 0 for a 64 Mbit SDRAM.
- AUTO REFRESH period: SDRAM_TRFC = 7.
- SDRAM auto refresh period expressed in 8 periods of SYSCLK input: SDRARP = 155 (decimal) which creates a 24 μ s/row auto refresh period. This register must be changed to 78 (decimal) for a 12 μ s/row auto refresh period.
- PRECHARGE command period: SDRAM_TRP = 2 (cannot be changed).
- Power-up initialization delay: SDRTINIT = 100. Indicates 100 units of 100 periods of the SYSCLK input, in other words, 10000 times SYSCLK. It is required by the SDRAM prior to issuing any command other than a COMMAND INHIBIT or a NOP.
- Number of AUTO REFRESH performed during initialization (full SDRAM auto-refresh): SDRINIT_AR_MBR = 8. Note: A configured value of 'n' will provide 'n+1' AUTO REFRESH cycles during the initialization period.
- Mode register default value: MBR_VALUE = 0 000 011 0 001.

CONFIGURATION CHANGES/INITIALIZATION

After power-up, or in order to change any of the SDRAM configuration parameter, the following procedure must be used:

1. Set the RESETS register at address 19482H to 0091H.
2. Configure the SDRAM control and interface registers in data sheet [Table 62](#).
3. Set and clear the SDRAM_INIT bit, bit 0 at address 1D600H.
4. Set the RESETS register at address 19482H to 0000H.

Note: There is no time constraint between step 3 and step 4.

All the configuration registers dedicated to the SDRAM controller are described in [Table 62](#) of the Memory Map.

MICROPROCESSOR ACCESS TO SDRAM

Here is the procedure to perform a write access to the SDRAM:

- Write the data to write in the 2 sixteen-bits registers UP_data2WrMSB (address 0x1d63a) and UP_data2WrLSB (address 0x1d638).
- Write the address to write in the UP_Addr2WrMSB (bits 6 to 0 of 0x1d636 register) and UP_Addr2WrLSB (16 bits of 0x1d634 register) registers.
- Set to 1 the UP_WrAddr2Wr register (bit 0 of 0x1d63e register). This bit is cleared by the chip at the end of the SDRAM write access.

Here is the procedure to perform a read access to the SDRAM:

- Write the address to read in the UP_Addr2RdMSB (bits 6 to 0 of 0x1d632 register) and UP_Addr2RdLSB (16 bits of 0x1d630 register) registers.
- Set to 1 the UP_WrAddr2Rd register (bit 0 of 0x1d63c register). This bit is cleared at the end of the SDRAM read access.
- When the UP_WrAddr2Rd is cleared, the data is available in the UP_DataRdLSB register (0x1d620 address) for the LSB value and UP_DataRdMSB register (0x1d622 address) for the MSB value.

All the registers to access to the SDRAM with the microprocessor are described into the Tables [63](#) and [64](#) of the Memory Map.

RESET OPERATION

GENERAL

Four types of reset are available in this device, external lead controlled hardware reset, microprocessor controlled hardware reset, microprocessor soft reset and microprocessor controlled global performance counters reset.

EXTERNAL LEAD CONTROLLED HARDWARE RESET

The $\overline{\text{RESET}}$ external lead activates the hardware reset. The actions are as follows:

- The configuration bits are in default state (all Ethernet MAC disabled, SDRAM 64 Mb configuration, encapsulation/de-encapsulation in LAPS mode, all the VT/VC are not allocated to any VCG, the Telecom bus interface is disabled).
- All the interrupt bit mask are in disabling state.
- All the performance counters are cleared.
- A 2 microsecond wait time must be observed after the external lead controlled hardware reset is asserted before which any microprocessor accesses can be made.

MICROPROCESSOR CONTROLLED HARDWARE RESET

The RESETH register provides the same reset action as the $\overline{\text{RESET}}$ external lead, but is directly addressable through the microprocessor interface. This reset is activated by writing a 0x91 to bits 7-0 of the RESETH register. The register is self-clearing.

A 2 microsecond wait time must be observed after the microprocessor controlled hardware reset is asserted before which any microprocessor accesses can be made.

The RESETH function is not available in Motorola 860 mode.

MICROPROCESSOR CONTROLLED SOFT RESET

Sixteen soft reset are available in the device, eight for each direction (Ethernet to SONET/SDH and SONET/SDH to Ethernet). The TX_RESETSx byte registers (bits 7-0 of registers 0x19486-0x19494) are corresponding to the software reset of the Ethernet line #0 to #7 in the transmit direction. The RX_RESETSx byte registers (bits 7-0 of registers 0x19496-0x194a4) are corresponding to the software reset of the VCG #0 to #7 in the receive direction.

When the value of the byte register of each software RESET is equal to 91 Hex, it activates the corresponding software reset. The actions are as follows:

- All the internal logic is initialized
- No impact on the control/configuration registers or counters

To clear the reset action, it is necessary to change the value of the corresponding software reset byte register or to perform an external lead controller hardware reset or to activate the microprocessor controlled hardware reset (RESETH).

MICROPROCESSOR CONTROLLED GLOBAL PERFORMANCE COUNTER RESET

When the RESETC byte register (bits 7-0 of register 0x19484) is equal to 91 Hex, it activates the global performance counter reset. The main actions is to clear all the performance counters.

To clear the reset action, it is necessary to change the value of the global performance counter reset byte register or to perform an external lead controlled hardware reset or to activate the microprocessor controlled hardware reset (RESETH). The reset action can also be cleared by the global software reset or any of the 16 per channel software resets.

TELECOM BUS OPERATION

GENERAL

When the EtherMap-3 *Plus* is configured for Drop timing, the Add bus is byte and multi-frame synchronous with the Drop bus, although delayed by one byte time because of internal processing. For example, if a byte in the STM-1 VC-4 structure using TUG-3, TU-12 mapping is to be added to the Add bus, the time of its placement is derived from the Drop bus timing, and from software instructions specifying which TU-12 number is being added. Note that the TU-12 drop selection can be different than the Add bus selection. An option is provided which enables the Drop bus timing signals to be sent as outputs on the Add bus. When the device is configured for Add bus timing, the add bus data, parity, and add indicator can be either derived from the input Add bus clock, C1J1V1, and SPE signals, or derived from internally generated clock, C1J1V1, and SPE signals, which are also provided as outputs. When the internal timing generator is used, all timing outputs are derived from RTCLK.

DROP BUS INTERFACE

The Drop bus consists of the following leads:

- Input data (DD(7-0)),
- Input clock (DCLK),
- Input parity (DPAR),
- Input C1, J1, and optional V1 marker pulses (DC1J1V1),
- Input payload indication (DSPE).

The most significant bit (MSB) of the input data is assigned to DD7. The MSB is defined as the first bit received in a SONET/SDH byte (i.e., bit 1 in the SONET/SDH byte). The bus rate is 19.44 MHz for STS-3 and STM-1 operation. The STS-1 rate is not supported. The drop bus is monitored for loss of clock. The Loss of Drop Clock alarm is aLOSSDCLK at bit 0 of register 0x198c6.

DROP BUS PARITY SELECTION

The parity selection for the Drop bus is according to the following table. A parity error is indicated by the ParityError alarm at bit 1 of register Defects. Other than an alarm indication, no action is taken by the EtherMap-3 *Plus*.

| ParityEven (bit 0 of register 0x1d57a) | ParityMode (bit 1 of register 0x1d57a) | Drop Bus Parity Selection |
|--|--|--|
| 0 | 0 | Odd parity is calculated for the data input leads (DD(7-0)). |
| 0 | 1 | Odd parity is calculated for the input leads consisting of data (DD(7-0)), C1, J1, and V1 marker pulses (DC1J1V1), and the payload indicator (DSPE). |

| ParityEven (bit 0 of register 0x1d57a) | ParityMode (bit 1 of register 0x1d57a) | Drop Bus Parity Selection |
|--|--|---|
| 1 | 0 | Even parity is calculated for the input leads consisting of data (DD(7-0)), C1, J1, and V1 marker pulses (DC1J1V1), and the payload indicator (DSPE). |
| 1 | 1 | Even parity is calculated for the data input leads (DD(7-0)). |

ADD BUS INTERFACE

The Add bus consists of the following leads:

- Output data (AD(7-0)),
- Output parity (APAR),
- Output add-to-bus indicator (\overline{ADD})

The timing information can be input or output:

- Input/Output clock (ACLK),
- Input/Output C1, J1, and optional V1 marker pulses (AC1J1V1),
- Input/Output payload indication (ASPE),

The most significant bit (MSB) of the output data is assigned to AD7. The MSB is defined as the first bit transmitted in a SONET/SDH byte (i.e., bit 1 in the SONET/SDH byte). The bus rate is 19.44 MHz for STS-3 and STM-1 operation. The STS-1 rate is not supported.

ADD BUS TIMING MODES

The Add bus interface configuration and timing modes are shown in the following table. The \overline{ABUST} lead selects either the Drop bus or the Add bus as the timing source for the Add bus, i.e., Drop bus or Add bus timing mode. The \overline{ABTE} lead is enabled in Drop bus timing mode and either enables or Tristates the Add bus clock, C1J1V1, and SPE outputs. The cTBADD control bit is enabled in Add bus timing mode and selects the Add bus clock, C1J1V1, and SPE signals to be either inputs or outputs.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| cTBADD (bit 0, register 0x194a8) | Lead ABUST | Lead ABTE | Add Bus Configuration and Timing Mode |
|---|-------------------|------------------|---|
| 0 | Low | X | Add Bus Timing Mode: The output leads consist of data (AD(7-0)), parity (ADPAR), and add indicator (ADD). The input leads consist of clock (ACLK), C1, J1, V1 marker pulses (AC1J1V1), and payload indicator (ASPE). Refer to Figure 12 . |
| 1 | Low | X | Add Bus Timing Mode: All leads are output leads consisting of data (AD(7-0)), parity (ADPAR), add indicator (ADD), clock (ACLK), C1, J1, V1 marker pulses (AC1J1V1), and payload indicator (ASPE). Refer to Figure 14 . |
| 0 | High | Low | Drop Bus Timing Mode: The output leads consist of data (AD(7-0)), parity (ADPAR), add indicator (ADD), clock (ACLK), C1, J1, V1 marker pulses (AC1J1V1), and payload indicator (ASPE). The clock, C1J1V1 and SPE signals are derived from the Drop bus. The V1 pulse is derived from either the V1 pulse present in the Drop bus C1J1V1 signal, or from the Drop side H4 byte detectors. Refer to Figure 10 . |
| 0 | High | High | Drop Bus Timing Mode: The output leads consist of data (AD(7-0)), parity (ADPAR), and add indicator (ADD). The clock (ACLK), C1, J1, and V1 marker pulses (AC1J1V1), and the payload indicator (ASPE) leads are Tristated. The data, parity, and add indicator signals are derived from the Drop bus clock, C1J1V1, and SPE signals. Refer to Figure 8 . |

ADD BUS PARITY SELECTION

The parity selection for the Add bus is according to the following table. Note that the timing mode selected for the Add bus must be consistent with the parity mode selected.

| ParityEven (bit 13, register 0x184c8) | ParityMode (bit 12, register 0x184c8) | Add Bus Parity Selection |
|--|--|---|
| 0 | 0 | Odd parity is calculated for the data output leads (AD(7-0)). |
| 0 | 1 | Odd parity is calculated for the output leads consisting of data (AD(7-0)), C1, J1, and V1 marker pulses (AC1J1V1), and the payload indicator (ASPE). |

| ParityEven (bit 13, register 0x184c8) | ParityMode (bit 12, register 0x184c8) | Add Bus Parity Selection |
|---|---|--|
| 1 | 0 | Even parity is calculated for the data output leads (AD(7-0)). |
| 1 | 1 | Even parity is calculated for output leads consisting of data (AD(7-0)), C1, J1, and V1 marker pulses (AC1J1V1), and the payload indicator (ASPE). |

ADD BUS DELAY

Options for controlling the delay of the add-bus Data, Parity and Add indicator, relative to either the Add bus or Drop bus timing signals (Clock, C1J1V1 and SPE) are shown in the following table. The control field 'TimingDelay' is used to set the phase relationship between the timing reference signals and the Add bus Data, Parity and Add indicator outputs by up to fifteen extra clock cycles.

In the drop bus timing mode where the add bus timing signals are output, there is a fixed relationship between the input and output timing determined by selecting the ActiveEdge (rising or falling) per [Figure 10](#) and [Figure 11](#). The TimingDelay parameter is used to select the phase relationship of the output Data, Parity and Add Indicator with respect to the input timing; therefore TimingDelay affects only the delay of add bus data with respect to drop bus timing signals in this mode.

The delay of the Add bus data can be adjusted to match a wide variety of conditions, making it easy to use the EtherMap-3 Plus device in applications involving other TranSwitch as well as non-TranSwitch products.

| TimingDelay (bits 10-7, register 0x184c8) | Timing Mode | Add Bus Delay |
|--|---|--|
| 1-F | Drop bus; Add bus timing outputs Tristated. | The delay of Add bus data, parity, and add indicator from the <u>Drop bus timing</u> can be programmed (from 1 to 15 clock cycles). |
| 1-F | Drop bus; Add bus timing outputs active. | The delay of Add bus data, parity, add indicator, C1J1V1, and SPE from the <u>Drop bus timing</u> can be programmed (from 1 to 15 clock cycles). |
| 1-F | Add bus (Slave); Add bus timing signals are inputs. | The delay of Add bus data, parity, and add indicator from the <u>Add bus timing</u> can be programmed (from 1 to 15 clock cycles). |
| 0-F | Add bus (Master); Add bus timing signals are outputs. | The delay of Add bus data, parity, and add indicator from the <u>Add bus timing</u> can be programmed (from 0 to 15 clock cycles). |

Note: When using multiple EtherMap-3 Plus devices on the same Telecom Bus, the user has several options for system configuration. For example, EtherMap-3 Plus #1 may operate in add bus master mode, and the remaining EtherMap-3 Plus devices will operate in add slave mode; the timing delay should be configured to 1 on all devices.

Additionally, since EtherMap-3 Plus #1 will output its timing and data on the rising edge of the clock, it is advisable to configure the sampling edge of the add bus of the other EtherMap-3 Plus devices to the falling edge.

TELECOM BUS TRIBUTARY ACTIVATION/TRI-STATE CONTROL

A priority scheme has been implemented to control the tri-state and activation of tributaries on the Telecom Add Bus. When a tributary is made active, it is no longer possible to tri-state associated lower order tributaries. To tri-state a tributary, it is necessary to tri-state all associated higher order tributaries. In this way, individual tributaries within a tributary group can be selectively tri-stated.

VC-3/VC-4

The data, parity, and add indicator corresponding to a VC-3 can be forced to a high impedance state by setting control bit HighZ_AU3 at bit 3 of register 0x184e8 (VC-3 #1), 0x184ea (VC-3 #2), or 0x184ec (VC-3 #3) to a 1. When operating in the AU-4 mode (control bit AU_Mode, bit 0 in register 0x184cc is a 1), the data, parity, and add indicator for the VC-4 can be forced to a high impedance state by setting all three HighZ_AU3 control bits to a 1. Correspondingly, when the HighZ_AU3 control bit(s) are set to 0, the VC-3 or VC-4 data, parity and add indicator are activated.

TUG-3

When operating in the AU-4 mode (control bit AU_Mode, bit 0 in register 0x184cc is a 1), the data, parity, and add indicator corresponding to a TUG-3 can be controlled as follows (note that all three HighZ_AU3 control bits are set to the same value for AU-4 mode, and corresponding to the values shown in the following table):

| Address | Bit 4 (HighZ_TUG3) | Bit 3 (HighZ_AU3) | Operation |
|--|--------------------|-------------------|--|
| 0x184e8 (TUG-3 #1), 0x184ea (TUG-3 #2), 0x184ec (TUG-3 #3) | x | 0 | The data, parity, and add indicator are active for all VC-4 POH, stuff, and TUG-3 byte times. |
| | 0 | 1 | The data, parity, and add indicator are active for each TUG-3 in which the HighZ_TUG3 control bit is set to 0 (inactive for VC-4 POH and stuff byte times) |
| | 1 | 1 | The data, parity, and add indicator are inactive for each TUG-3 in which the HighZ_TUG3 control bit is set to 1 (unless TUG-2 or TU-12 tributaries within the TUG-3 are activated, causing activation of the data, parity, and add indicator for those tributaries). |

TUG-2

The data, parity, and add indicator corresponding to a TUG-2 can be forced to a high impedance state by setting control bit HighZ at bit 1 of register 0x18480 (TUG-2 #1), 0x18482 (TUG-2 #2), 0x18484 (TUG-2 #3), ... or 0x184a8 (TUG-2 #21) to a 1, provided the corresponding HighZ_AU3 control bit is set to a 1 (AU-3 mode), or the corresponding HighZ_TUG3 and all three HighZ_AU3 control bits are set to a 1 (AU-4 mode). Setting a corresponding higher order tributary to the active state also activates the TUG-2 independent of the TUG-2 HighZ control bit setting. A TUG-2 can be selectively activated by setting all corresponding higher order HighZ control bits to a 1, and setting the selected TUG-2 HighZ control bit to a 0.

TU-11/TU-12

The data, parity, and add indicator corresponding to a TU-11 can be forced to a high impedance state by setting control bit HighZ at bit 0 of register 0x18500 (TU-11 #1), 0x18502 (TU-11 #2), 0x18504 (TU-11 #3), ... or 0x185a6 (TU-11 #84) to a 1. All corresponding higher order tributaries must be set to the high impedance state. Setting a corresponding higher order tributary to the active state also activates the TU-11 independent of the TU-11 HighZ control bit setting. A TU-11 can be selectively activated by setting all corresponding higher order HighZ control bits to a 1, and setting the selected TU-11 HighZ control bit to a 0.

The data, parity, and add indicator corresponding to a TU-12 can be forced to a high impedance state by setting control bit HighZ at bit 0 of register 0x18500 (TU-12 #1), 0x18502 (TU-12 #2), 0x18504 (TU-12 #3), ... or 0x185a6 (TU-12 #63) to a 1. All corresponding higher order tributaries must be set to the high impedance state. Setting a corresponding higher order tributary to the active state also activates the TU-12 independent of the TU-12 HighZ control bit setting. A TU-12 can be selectively activated by setting all corresponding higher order HighZ control bits to a 1, and setting the selected TU-12 HighZ control bit to a 0.

LOOP BACKS

MAC LOOPBACK

The MAC loopback is enabled by setting bit 8 at address 0x00000 to '1'. When this bit is set, the Transmit outputs of one given MAC are looped back to the Receive inputs of the same MAC. The MAC will operate at the same speed as its attached PHY device. If the PHY is not connected, the MAC will run at 10 Mbps.

When this loopback is selected, frames are transmitted to the client. In GMII mode only, if this loopback is selected, a 125 MHz clock must be provided to the TX_CLK input lead.

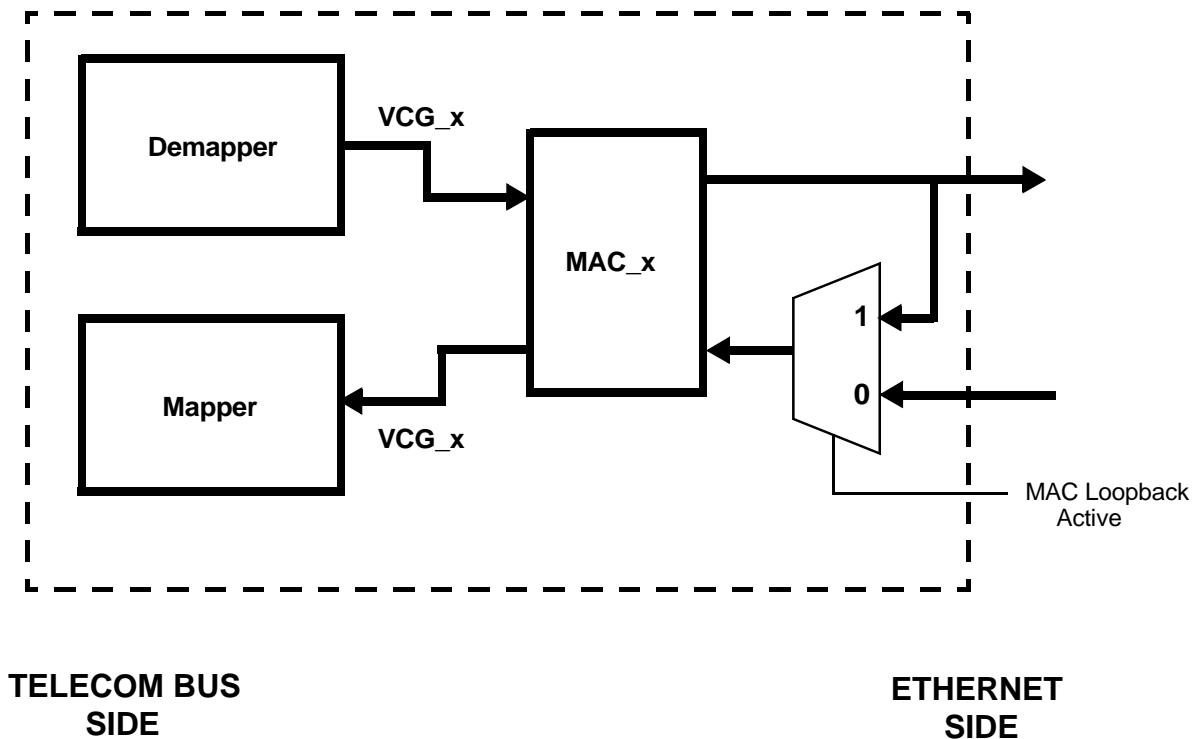


Figure 56. MAC Loopback

TELECOM BUS LOOPBACKS

The EtherMap-3 Plus supports two types of telecom bus loopbacks:

SONET/SDH Line Side loopback from receive to transmit telecom bus: The DROP bus signals are looped into the ADD bus leads. All programmed delays between data and timing in the add telecom bus block are disregarded and all ADD bus signals become outputs regardless of the timing mode selected.

Also, when this loopback is selected:

- a. In ADD bus timing slave mode, the drop data will not be passed through to the decapsulation block to the TX MAC.
- b. In ADD bus timing master mode and Drop bus timing modes, data will be passed through to the downstream blocks.

| LoopBackActive (bit 6 of register 0x184c8) | SONET/SDH Line Side loopback |
|---|------------------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

Ethernet or Local Side loopback from transmit to receive telecom bus: The ADD bus signals are looped into the demapper block and signals on the DROP bus are ignored. The ADD bus data is also passed on to the external signal leads. When this loopback is selected, the C2 overhead byte expected on the drop side must match the C2 transmitted on the add side.

| LoopBackActive (bit 0 of register 0x1f754) | Ethernet/Local Side loopback |
|---|------------------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

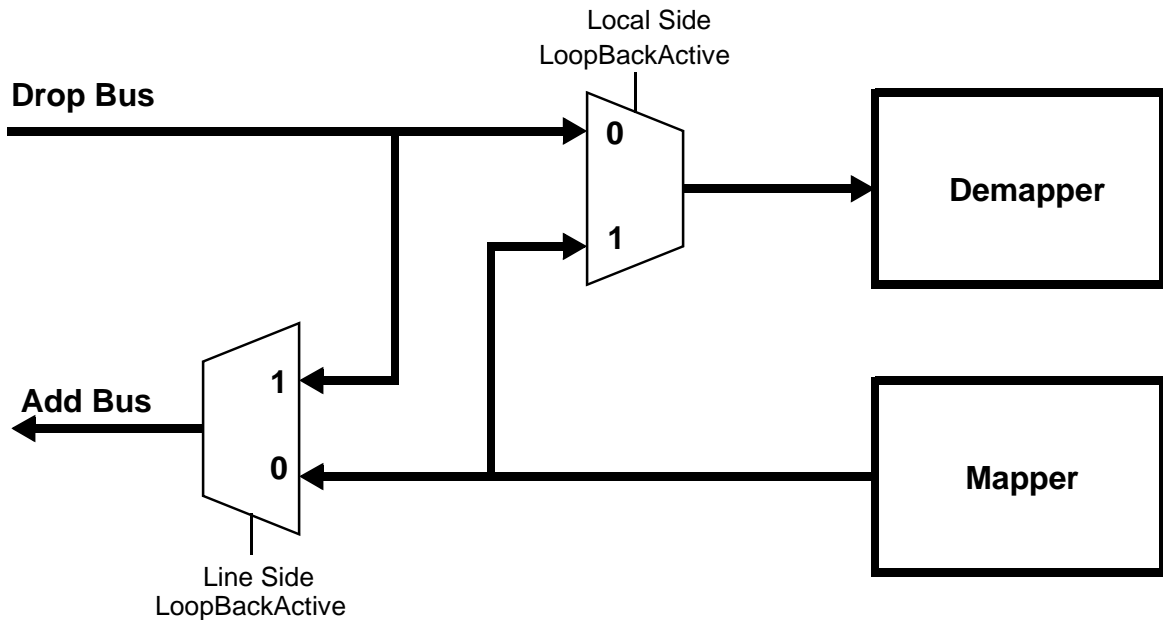


Figure 57. Telecom Bus Loopbacks

BOUNDARY SCAN

INTRODUCTION

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in [Figure 58](#), one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in [Figure 38](#).

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in [Figure 58](#).

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the EtherMap-3 Plus devices internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

BOUNDARY SCAN OPERATION

The maximum frequency the EtherMap-3 Plus device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in [Figure 58](#). The EtherMap-3 Plus device performs the following boundary scan test instructions:

The EXTEST test instruction provides the ability to test the connectivity of the EtherMap-3 Plus device to external circuitry.

The SAMPLE/PRELOAD test instruction provides the ability to examine the values of the Input and Output pins without interfering with device operation, and to initialize the Boundary Scan Register with new values for the next operation.

The BYPASS test instruction provides the ability to bypass the EtherMap-3 Plus boundary scan and instruction registers.

The IDCODE test instruction provides a unique device identification for the EtherMap-3 Plus device.

The HIGHZ test instruction provides the ability to drive all 3-state outputs and bidirectional pins to their high impedance state.

The CLAMP test instruction provides the ability to drive the component pins of the chip from the boundary scan register, while the bypass register is selected as the serial path between TDI and TDO. The component pins will not switch while the CLAMP instruction is selected.

BOUNDARY SCAN RESET

Specific control of the $\overline{\text{TRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the EtherMap-3 Plus. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the Input, Output and Input/Output Parameters section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

BOUNDARY SCAN SCHEMATIC

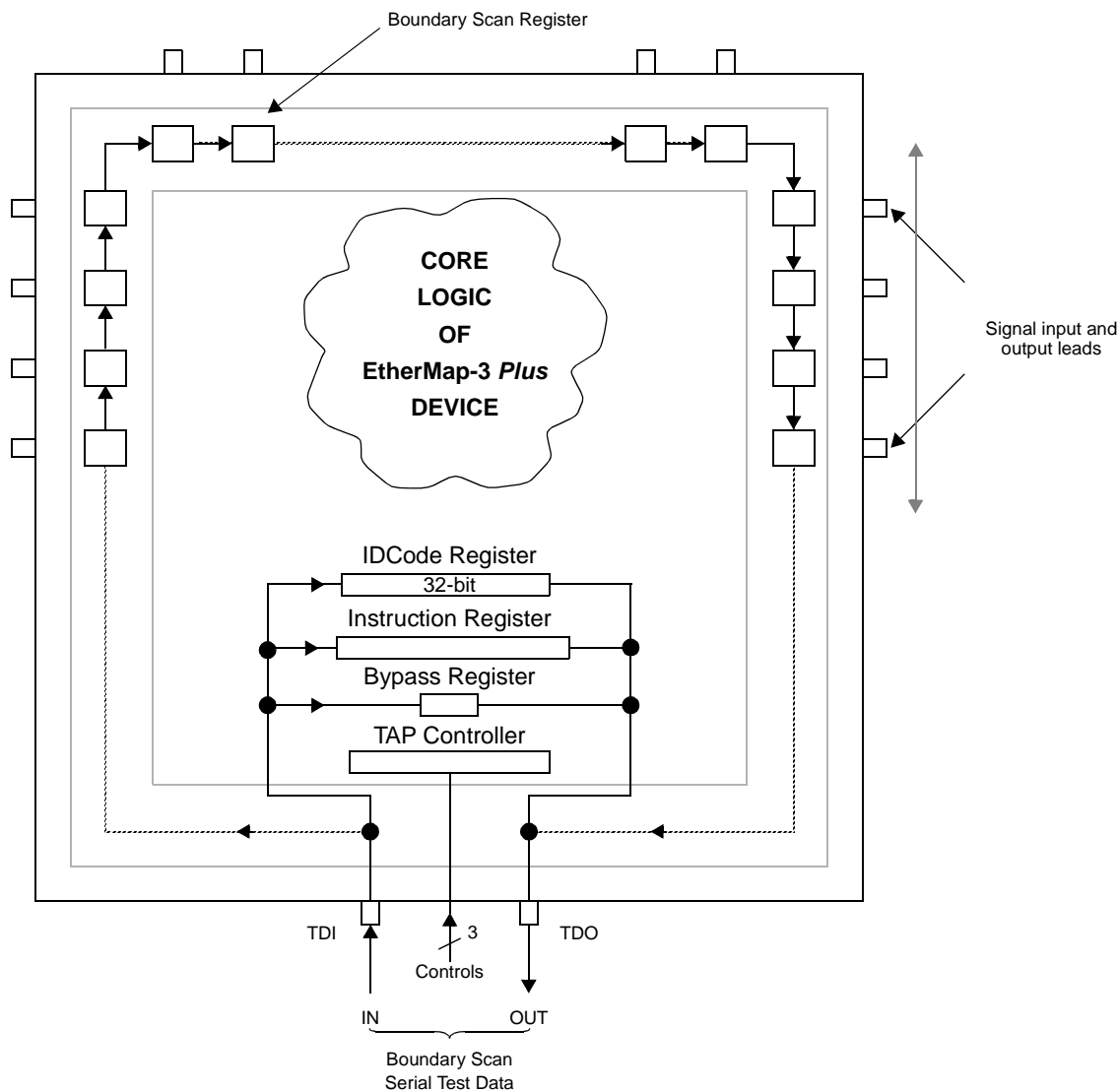


Figure 58. Boundary Scan Schematic

BOUNDARY SCAN CHAIN

A boundary scan description language (BSDL) source file is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com.



MEMORY INFORMATION

For Tables 10 through 12 and 35 through 308 access is as follows:

RW=Read/Write, R/COW=Read/Clear On Write, RO=Read Only, RR=Read-Reset WO=Write Only and COW=Clear On Write. Please note that initial values for status registers can change immediately after reset.

Table 9: Memory Map Overview

| Table / Offset | Functional block | Description |
|---------------------------------------|--------------------------------|--|
| Table 18-Table 23 Offset = 0x00000 | Ethernet interface port #1 | MAC for SMII port #1 and GMII interface Configuration registers |
| Table 13-Table 17 Offset = 0x00000 | Ethernet interface port #1 | MAC for SMII port #1 and GMII interface Status registers |
| Table 18-Table 23 Offset = 0x02000 | Ethernet interface port #2 | MAC for SMII port #2 Configuration registers |
| Table 13-Table 17 Offset = 0x02000 | Ethernet interface port #2 | MAC for SMII port #2 Status registers |
| Table 18-Table 23 Offset = 0x04000 | Ethernet interface port #3 | MAC for SMII port #3 Configuration registers |
| Table 13-Table 17 Offset = 0x04000 | Ethernet interface port #3 | MAC for SMII port #3 Status registers |
| Table 18-Table 23 Offset = 0x06000 | Ethernet interface port #4 | MAC for SMII port #4 Configuration registers |
| Table 13-Table 17 Offset = 0x06000 | Ethernet interface port #4 | MAC for SMII port #4 Status registers |
| Table 18-Table 23 Offset = 0x08000 | Ethernet interface port #5 | MAC for SMII port #5 Configuration registers |
| Table 13-Table 17 Offset = 0x08000 | Ethernet interface port #5 | MAC for SMII port #5 Status registers |
| Table 18-Table 23 Offset = 0x0a000 | Ethernet interface port #6 | MAC for SMII port #6 Configuration registers |
| Table 13-Table 17 Offset = 0x0a000 | Ethernet interface port #6 | MAC for SMII port #6 Status registers |
| Table 18-Table 23 Offset = 0x0c000 | Ethernet interface port #7 | MAC for SMII port #7 Configuration registers |
| Table 13-Table 17 Offset = 0x0c000 | Ethernet interface port #7 | MAC for SMII port #7 Status registers |
| Table 18-Table 23 Offset = 0x0e000 | Ethernet interface port #8 | MAC for SMII port #8 Configuration registers |
| Table 13-Table 17 Offset = 0x0e000 | Ethernet interface port #8 | MAC for SMII port #8 Status registers |
| Table 24-Table 29 | Ethernet MII management | |
| Table 30 | Ethernet interface ports 1-8 | General configuration |
| Table 31-Table 34 | Ethernet interface ports 1-8 | Alarms of the 8 Ethernet interfaces |
| Table 65 Table 71 Table 72 | Transmit Virtual concatenation | Virtual concatenation configuration per VCG and per member in Low/High order |
| Table 73 | Transmit LCAS | LCAS configuration per VCG and per member in Low/High order |

Table 9: Memory Map Overview

| Table / Offset | Functional block | Description |
|--|---|---|
| Table 75 | Transmit Virtual concatenation | Status information per VCG and per member in Low/high order |
| Table 66-Table 70 | Transmit LCAS | LCAS alarm/mask/interruption per VCG and per member in Low/High order |
| Table 179 | VCI_RX_VC4_POH | VC-4 POH Monitor |
| Table 238-Table 242 | VCI_TX_VC3_POH | VC-3 POH Generator |
| Table 48 Table 49 Table 50 Table 53 Table 54 | Receive Decapsulation Block MAC#1-8 | Configuration of the decapsulation blocks |
| Table 55 | Receive Decapsulation Block MAC#1-8 | Control frame buffer for decapsulation blocks |
| Table 56-Table 60 | Receive Decapsulation Block MAC#1-8 | Alarms, Masks, Interrupts and performance counters for all decapsulation blocks |
| Table 51 Table 52 Table 61 | Receive Decapsulation Block MAC#1-8 | Status of the decapsulation blocks |
| Table 109 | VCI_TX_TIMING_GENERATOR | |
| Table 162 | VCI_TX_LO_ALARM_PORT | Transmit Low Order Ring/Alarm Interface port |
| Table 294 | VCI_TX_COMBUS | Transmit (Add) Telecom Bus interface |
| Table 35-Table 39 | Transmit Encapsulation Block MAC#1-8 | Configuration of the encapsulation blocks |
| Table 40 | Transmit Encapsulation Block MAC#1-8 | Control frame buffer for encapsulation blocks |
| Table 41-Table 47 | Transmit Encapsulation Block MAC#1-8 | Status, Alarms, performance counters, interrupts of encapsulation blocks |
| Table 76 Table 81 Table 82 | Receive Virtual concatenation and LCAS processing block | Virtual concatenation configuration per VCG and per member in Low/High order & LCAS configuration |
| Table 77-Table 80 | Receive Virtual concatenation and LCAS processing block | Alarm, Mask, interrupts |
| Table 83-Table 85 | Receive Virtual concatenation and LCAS processing block | Status information per VCG and per member in Low/high order |
| Table 91 Table 98 | Ethernet Buffering and flow control in Tx Ethernet to SONET/SDH direction | Configuration registers |
| Table 92-Table 97 Table 99-Table 103 | Ethernet Buffering and flow control in Tx Ethernet to SONET/SDH direction | Status, alarm, interrupt, performance counters |
| Table 168 | VCI_TX_ALARM_PORT | Transmit High Order Ring/Alarm Interface port |
| Table 210 | VCI_RX_TU3_PTR | TU-3 Pointer Tracker |
| Table 236 | VCI_TX_TU3_PTR | TU-3 Pointer Generator |
| Table 238-Table 242 | VCI_TX_VC4_POH | VC-4 POH Generator |
| Table 163 | VCI_RX_LO_ALARM_PORT | Receive Low Order Ring/Alarm Interface port |

Table 9: Memory Map Overview

| Table / Offset | Functional block | Description |
|-------------------|--|--|
| Table 167 | VCI_RX_ALARM_PORT | Receive High Order Ring/Alarm Interface port |
| Table 86 | Ethernet Frame Format block Ethernet to SONET/SDH direction | Configuration registers |
| Table 87-Table 90 | Ethernet Frame Format block Ethernet to SONET/SDH direction | Alarms, status, interrupt, performance counters |
| Table 10-Table 12 | General configuration of EtherMap-3 Plus | Device ID, general status, hardware/software reset |
| Table 212 | VCI_AU_RETIMER | High Order Retimer |
| Table 267 | VCI_RX_COMBUS | Receive (Drop) Telecom Bus interface |
| 0x1d240 | VCI_ETTC | Transmit Ethernet FIFO Controller |
| Table 104 | VCI_MAPDEMAP | |
| Table 166 | VCI_VTMPR_IC | |
| Table 261 | VCI_C3_TO_AUG1_IC | |
| Table 62 | VCI_RAMC | SDRAM Controller |
| Table 223 | VCI_L3XCON | STS-1/VC-3/TUG-3 Time Slot Interchange blocks |
| Table 305 | VCI_COMBUS_IC | |
| Table 308 | VCI_VTMP_TOP_IC | |
| Table 135 | VCI_LO_DEMAPPER_POH | Low Order POH Monitor |
| Table 116 | VCI_LO_MAPPER | |
| Table 131 | VCI_LO_DEMAPPER | |
| Table 182 | VCI_RX_VC3_POH | VC-3 POH Monitor |
| Table 250 | VCI_L3_RETIMER | TU-3 Retimer |

Notes:

1. DCLK clock is always needed for accessing the registers of the VCI_RX_COMBUS virtual component (or "block"). DCLK clock is needed for accessing all the blocks in the Mapper/Demapper part when in drop bus timing mode. In these two cases, when the DCLK clock is missing, an acknowledge is generated after 256 RTCLK clock cycles.
2. In all timing modes, when a wrong (not existent) address is accessed, an acknowledge is generated after or 256 RTCLK clock cycles. This is not true for the MAC block: if wrong (not existent) address within the MAC block is accessed, NO acknowledge is generated.
3. During the initial configuration of the device, a) Drop timing mode: the input DCLK will be required; b) Add slave timing mode: the input ACLK will be required; c) Add master timing mode: the output ACLK must be pulled high with a weak pull-up (~10k ohm). After a hard reset, the first microprocessor access must be to set the cTBADD register to 1. At this moment, the EtherMap-3 Plus will be able to drive the clock.

GENERAL DEVICE REGISTERS

Table 10 through 12 - General Configuration and Status of the Device

Table 10: General Device Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|----------------------|------|------------------|--------|--|
| 0x19480 | 7-0 | RESETH | 0x0000 | Global Hard Reset 0x91: reset state, self-clearing others: non reset state A 2 microsecond wait time must be observed after 0x91 is written, before which any other microprocessor accesses can be made. This function is not available in Motorola 860 mode. |
| 0x19482 | 7-0 | RESETS | 0x0000 | Global Soft Reset |
| 0x19484 | 7-0 | RESETC | 0x0000 | Performance Counter reset 0x91: reset state others: non reset state |
| 0x19486 – 0x19494 | 7-0 | TX_RESETSx | 0x0000 | TX soft reset for VCG Channels 0-7 (Ethernet to SONET direction) 0x91: reset state others: non reset state This reset must be activated for a minimum of 16 μs. |
| 0x19496 – 0x194a4 | 7-0 | RX_RESETSx | 0x0000 | RX soft reset for VCG Channels 0-7 (SONET to Ethernet direction) 0x91: reset state others: non reset state This reset must be activated for a minimum of 16 μs. |
| 0x194a6 | 0 | cCROV | 0x0000 | Non-Saturating mode for the performance counters 1: non saturating mode ==> roll over to 0 0: saturating mode. Performance counters are cleared on read. |
| 0x194a8 | 0 | ctBADD | 0x0000 | ADD bus timing configuration mode (linked with \overline{ABUST} and \overline{ABTE} inputs) 0: Add telecom bus in slave mode 1: Add telecom bus in master mode |
| 0x194aa – 0x194c8 | 15-0 | Internalx (0-15) | 0x0000 | Reserved |

Table 11: General Device Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x19440 | 0 | GMII/SMII | 0x0000 | Status of the GMII/SMII input pin |
| 0x19442 | 0 | HIGHZ | 0x0000 | Status of the HIGHZ input pin |
| 0x19444 | 0 | ABTE | 0x0000 | Status of the \overline{ABTE} input pin |
| 0x19446 | 0 | ABUST | 0x0000 | Status of the \overline{ABUST} input pin |
| 0x19448 | 0 | PHY/MAC | 0x0000 | Status of the PHY/MAC input pin |
| 0x1944a | 0 | SYNC_DIR | 0x0000 | Status of the SYNC_DIR input pin |

Table 12: ID Registers (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------|-----------------|---|
| 0x19400 | 15-0 | ManufactureId | 0x00D7 | Manufacture Id |
| 0x19402 | 15-0 | PartNumber | 0x4236 | Part Number |
| 0x19404 | 15-0 | VersionMask | see Description | Device Version Level - Device Mask Level 0x0001 = TXC-04236-AIBG, Revision B |

ETHERNET MAC REGISTERS

The MAC tables shown below are for SMII port one, and the GMII interface. The starting Address for SMII port two is offset by 0x02000, the starting Address for SMII port three is offset by 0x04000, the starting Address for SMII port four is offset by 0x06000, the starting Address for SMII port five is offset by 0x08000, the starting Address for SMII port six is offset by 0x0a000, the starting Address for SMII port seven is offset by 0x0c000, and the starting Address for SMII port eight is offset by 0x0e000.

All MAC registers must be accessed as 16-bit register pairs, even when only a 16-bit register access is needed. Registers 0x00000 and 0x00002 are a pair, registers 0x00004 and 0x00006 are a pair,etc. For writes, the 16 MSBs (Address bit 0 is high) must be written first. For reads, the 16 LSBs (Address bit 0 is low) must be read first.

Tables 13 through 17 - Status Information of the MAC**Table 13: MAC Combined Receive and Transmit Counters**

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-------------|--------|---|
| 0x01080 | 15-0 | TR64_LOWER | 0x0000 | Transmit and Receive 64 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01082 | 8-0 | TR64_UPPER | 0x0000 | Transmit and Receive 64 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01084 | 15-0 | TR127_LOWER | 0x0000 | Transmit and Receive 65 to 127 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01086 | 8-0 | TR127_UPPER | 0x0000 | Transmit and Receive 65 to 127 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01088 | 15-0 | TR255_LOWER | 0x0000 | Transmit and Receive 128 to 255 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x0108a | 8-0 | TR255_UPPER | 0x0000 | Transmit and Receive 128 to 255 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x0108c | 15-0 | TR511_LOWER | 0x0000 | Transmit and Receive 256 to 511 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x0108e | 8-0 | TR511_UPPER | 0x0000 | Transmit and Receive 256 to 511 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01090 | 15-0 | TR1K_LOWER | 0x0000 | Transmit and Receive 512 to 1023 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01092 | 8-0 | TR1K_UPPER | 0x0000 | Transmit and Receive 512 to 1023 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01094 | 15-0 | TRMAX_LOWER | 0x0000 | Transmit and Receive 1024 to 1518 Byte Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x01096 | 8-0 | TRMAX_UPPER | 0x0000 | Transmit and Receive 1024 to 1518 Byte Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing Bits but including FCS bytes). |

Table 13: MAC Combined Receive and Transmit Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-------------|--------|--|
| 0x01098 | 15-0 | TRMGV_LOWER | 0x0000 | Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter (lower 16 Bits): Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing Bits but including FCS bytes). |
| 0x0109a | 8-0 | TRMGV_UPPER | 0x0000 | Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter (upper 9 Bits): Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing Bits but including FCS bytes). |

Table 14: MAC Receive Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-------------|--------|---|
| 0x0109c | 15-0 | RBYT_LOWER | 0x0000 | Receive Byte Counter (lower 16 Bits): The Statistic Counter register is incremented by the byte count of frames received with 0 to 1518 bytes (i.e., includes all overhead bytes such as DA/SA/TL), including those in bad packets, excluding framing Bits (i.e., Preamble, SFD) but including FCS bytes. |
| 0x0109e | 11-0 | RBYT_UPPER | 0x0000 | Receive Byte Counter (upper 12 Bits): The Statistic Counter register is incremented by the byte count of frames received with 0 to 1518 bytes (i.e., includes all overhead bytes such as DA/SA/TL), including those in bad packets, excluding framing Bits (i.e., Preamble, SFD) but including FCS bytes. |
| 0x010a0 | 15-0 | RPKT_LOWER | 0x0000 | Receive Packet Counter (lower 16 Bits): Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets). |
| 0x010a2 | 8-0 | RPKT_UPPER | 0x0000 | Receive Packet Counter (upper 9 Bits): Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets). |
| 0x010a4 | 15-0 | RFCS_LOWER | 0x0000 | Receive FCS Error Counter (lower 16 bits): Incremented for each frame received that has a integral 64 to 1518 length and contains a Frame Check Sequence error. |
| 0x010a6 | 1-0 | RFCS_UPPER | 0x0000 | Receive FCS Error Counter (upper 2 bits): Incremented for each frame received that has a integral 64 to 1518 length and contains a Frame Check Sequence error. |
| 0x010a8 | 15-0 | RMCA_LOWER | 0x0000 | Receive Multicast Packet Counter (lower 16 Bits): Incremented for each Multicast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors. |
| 0x010aa | 8-0 | RMCA_UPPER | 0x0000 | Receive Multicast Packet Counter (upper 9 Bits): Incremented for each Multicast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors. |
| 0x010ac | 15-0 | RBCA_LOWER | 0x0000 | Receive Broadcast Packet Counter (lower 16 Bits): Incremented for each Broadcast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors. |
| 0x010ae | 8-0 | RBCA_UPPER | 0x0000 | Receive Broadcast Packet Counter (upper 9 Bits): Incremented for each Broadcast good frame of lengths 64 to 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors. |
| 0x010b0 | 15-0 | RXCF_LOWER | 0x0000 | Receive Control Frame Packet Counter (lower 16 Bits): Incremented for each MAC Control frame received (PAUSE and Unsupported). |
| 0x010b2 | 1-0 | RXCF_UPPER | 0x0000 | Receive Control Frame Packet Counter (upper 2 Bits): Incremented for each MAC Control frame received (PAUSE and Unsupported). |
| 0x010b4 | 15-0 | RXPFL_LOWER | 0x0000 | Receive PAUSE Frame Packet Counter (lower 16 bits): Incremented each time a valid PAUSE MAC Control frame is received. |
| 0x010b6 | 1-0 | RXPFL_UPPER | 0x0000 | Receive PAUSE Frame Packet Counter (upper 2 bits): Incremented each time a valid PAUSE MAC Control frame is received. |
| 0x010b8 | 15-0 | RXUO_LOWER | 0x0000 | Receive Unknown Opcode Counter (lower 16 bits): Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE. |
| 0x010ba | 1-0 | RXUO_UPPER | 0x0000 | Receive Unknown Opcode Counter (upper 2 bits): Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 14: MAC Receive Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------|--------|---|
| 0x010bc | 15-0 | RALN_LOWER | 0x0000 | Receive Alignment Error Counter (lower 16 bits): Incremented for each received frame from 64 to 1518 (non VLAN) or 1522 (VLAN) which contains an invalid FCS and is not an integral number of bytes. |
| 0x010be | 1-0 | RALN_UPPER | 0x0000 | Receive Alignment Error Counter (upper 2 bits): Incremented for each received frame from 64 to 1518 (non VLAN) or 1522 (VLAN) which contains an invalid FCS and is not an integral number of bytes. |
| 0x010c0 | 15-0 | RFLR_LOWER | 0x0000 | Receive Frame Length Error Counter (lower 16 bits): Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46 - 1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value. |
| 0x010c2 | 1-0 | RFLR_UPPER | 0x0000 | Receive Frame Length Error Counter (upper 2 bits): Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46 - 1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value. |
| 0x010c4 | 15-0 | RCDE_LOWER | 0x0000 | Receive Code Error Counter (lower 16 bits): Incremented each time a valid carrier was present and at least one invalid data symbol was detected. |
| 0x010c6 | 1-0 | RCDE_UPPER | 0x0000 | Receive Code Error Counter (upper 2 bits): Incremented each time a valid carrier was present and at least one invalid data symbol was detected. |
| 0x010c8 | 15-0 | RCSE_LOWER | 0x0000 | Receive False Carrier Counter (lower 16 bits): Incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an '0xE' on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames. |
| 0x010ca | 1-0 | RCSE_UPPER | 0x0000 | Receive False Carrier Counter (upper 2 bits): Incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an '0xE' on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames. |
| 0x010cc | 15-0 | RUND_LOWER | 0x0000 | Receive Undersize Packet Counter (lower 16 bits): Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors. |
| 0x010ce | 1-0 | RUND_UPPER | 0x0000 | Receive Undersize Packet Counter (upper 2 bits): Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors. |
| 0x010d0 | 15-0 | ROVR_LOWER | 0x0000 | Receive Oversize Packet Counter (lower 16 bits): Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors. |
| 0x010d2 | 1-0 | ROVR_UPPER | 0x0000 | Receive Oversize Packet Counter (upper 2 bits): Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors. |
| 0x010d4 | 15-0 | RFRG_LOWER | 0x0000 | Receive Fragments Counter (lower 16 bits): Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS, includes integral and non-integral lengths. |
| 0x010d6 | 1-0 | RFRG_UPPER | 0x0000 | Receive Fragments Counter (upper 2 bits): Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS, includes integral and non-integral lengths. |
| 0x010d8 | 15-0 | RJBR_LOWER | 0x0000 | Receive Jabber Counter (lower 16 bits): Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors. |
| 0x010da | 1-0 | RJBR_UPPER | 0x0000 | Receive Jabber Counter (upper 2 bits): Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors. |
| 0x010dc | 15-0 | Reserved | 0x0000 | Reserved |

Table 14: MAC Receive Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|-------------|
| 0x010de | 1-0 | Reserved | 0x0000 | Reserved |

Table 15: MAC Transmit Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------|--------|---|
| 0x010e0 | 15-0 | TBYT_LOWER | 0x0000 | Transmit Byte Counter (lower 16 Bits): Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes. |
| 0x010e2 | 11-0 | TBYT_UPPER | 0x0000 | Transmit Byte Counter (upper 12 Bits): Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes. |
| 0x010e4 | 15-0 | TPKT_LOWER | 0x0000 | Transmit Packet Counter (lower 16 Bits): Incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast, and Multicast packets). |
| 0x010e6 | 8-0 | TPKT_UPPER | 0x0000 | Transmit Packet Counter (upper 9 Bits): Incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast, and Multicast packets). |
| 0x010e8 | 15-0 | TCMA_LOWER | 0x0000 | Transmit Multicast Packet Counter (lower 16 Bits): Incremented for each Multicast valid frame transmitted (excluding Broadcast frames). |
| 0x010ea | 8-0 | TCMA_UPPER | 0x0000 | Transmit Multicast Packet Counter (upper 9 Bits): Incremented for each Multicast valid frame transmitted (excluding Broadcast frames). |
| 0x010ec | 15-0 | TCBA_LOWER | 0x0000 | Transmit Broadcast Packet Counter (lower 16 Bits): Incremented for each Broadcast frame transmitted (excluding Multicast frames). |
| 0x010ee | 8-0 | TCBA_UPPER | 0x0000 | Transmit Broadcast Packet Counter (upper 9 Bits): Incremented for each Broadcast frame transmitted (excluding Multicast frames). |
| 0x010f0 | 15-0 | TXPF_LOWER | 0x0000 | Transmit PAUSE Frame Packet Counter (lower 16 Bits): Incremented each time a valid PAUSE MAC Control frame is transmitted. |
| 0x010f2 | 1-0 | TXPF_UPPER | 0x0000 | Transmit PAUSE Frame Packet Counter (upper 2 Bits): Incremented each time a valid PAUSE MAC Control frame is transmitted. |
| 0x010f4 | 15-0 | TDFR_LOWER | 0x0000 | Transmit Deferral Packet Counter (lower 16 Bits): Incremented each time a packet is deferred on its first transmission attempt. Does not include frames involved in collisions. |
| 0x010f6 | 1-0 | TDFR_UPPER | 0x0000 | Transmit Deferral Packet Counter (upper 2 Bits): Incremented each time a packet is deferred on its first transmission attempt. Does not include frames involved in collisions. |
| 0x010f8 | 15-0 | TEDF_LOWER | 0x0000 | Transmit excessive Deferral Packet Counter (lower 16 Bits): Incremented each time a frame is aborted for an excessive period of time |
| 0x010fa | 1-0 | TEDF_UPPER | 0x0000 | Transmit excessive Deferral Packet Counter (upper 2 Bits): Incremented each time a frame is aborted for an excessive period of time |
| 0x010fc | 15-0 | TSCL_LOWER | 0x0000 | Transmit Single collision packet Counter (lower 16 Bits): Incremented each time a packet is transmitted which experienced exactly one collision during transmission |
| 0x010fe | 1-0 | TSCL_UPPER | 0x0000 | Transmit Single collision packet Counter (upper 2 Bits): Incremented each time a packet is transmitted which experienced exactly one collision during transmission |
| 0x01100 | 15-0 | TMCL_LOWER | 0x0000 | Transmit multiple collision Packet Counter (lower 16 Bits): Incremented each time a frame which experienced 2-15 collisions (including any late collisions) during transmission as defined in the Retransmission maximum value. |
| 0x01102 | 1-0 | TMCL_UPPER | 0x0000 | Transmit multiple collision Packet Counter (upper 2 Bits): Incremented each time a frame which experienced 2-15 collisions (including any late collisions) during transmission as defined in the Retransmission maximum value. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 15: MAC Transmit Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------|--------|---|
| 0x01104 | 15-0 | TLCL_LOWER | 0x0000 | Transmit Late collision Packet Counter (lower 16 Bits): Incremented each time a packet which experienced a late collision during a transmission attempt. |
| 0x01106 | 1-0 | TLCL_UPPER | 0x0000 | Transmit Late collision Packet Counter (upper 2 Bits): Incremented each time a packet which experienced a late collision during a transmission attempt. |
| 0x01108 | 15-0 | TXCL_LOWER | 0x0000 | Transmit Excessive collision Packet Counter (lower 16 Bits): Incremented each time a packet experienced 16 collisions during transmission and was aborted. |
| 0x0110a | 1-0 | TXCL_UPPER | 0x0000 | Transmit Excessive collision Packet Counter (upper 2 Bits): Incremented each time a packet experienced 16 collisions during transmission and was aborted. |
| 0x0110c | 15-0 | TNCL_LOWER | 0x0000 | Transmit total collision Packet Counter (lower 16 Bits): Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals in the Transmit and Receive. This register does not include collisions that occur in an excessive collision condition. |
| 0x0110e | 1-0 | TNCL_UPPER | 0x0000 | Transmit total collision Packet Counter (upper 2 Bits): Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals in the Transmit and Receive. This register does not include collisions that occur in an excessive collision condition. |
| 0x01110 | 15-0 | Reserved | 0x0000 | Reserved |
| 0x01112 | 1-0 | Reserved | 0x0000 | Reserved |
| 0x01114 | 15-0 | Reserved | 0x0000 | Reserved |
| 0x01116 | 1-0 | Reserved | 0x0000 | Reserved |
| 0x01118 | 15-0 | TJBR_LOWER | 0x0000 | Transmit Jabber Frame Counter (lower 16 bits): Incremented for each oversized transmitted frame with an incorrect FCS value. |
| 0x0111a | 1-0 | TJBR_UPPER | 0x0000 | Transmit Jabber Frame Counter (upper 2 bits): Incremented for each oversized transmitted frame with an incorrect FCS value. |
| 0x0111c | 15-0 | TFCS_LOWER | 0x0000 | Transmit FCS Error Counter (lower 16 bits): Incremented for every valid sized packet with an incorrect FCS value. |
| 0x0111e | 1-0 | TFCS_UPPER | 0x0000 | Transmit FCS Error Counter (upper 2 bits): Incremented for every valid sized packet with an incorrect FCS value. |
| 0x01120 | 15-0 | TXCF_LOWER | 0x0000 | Transmit Control Frame Counter (lower 16 bits): Incremented for every valid size frame with a Type Field signifying a Control frame. |
| 0x01122 | 1-0 | TXCF_UPPER | 0x0000 | Transmit Control Frame Counter (upper 2 bits): Incremented for every valid size frame with a Type Field signifying a Control frame. |
| 0x01124 | 15-0 | TOVR_LOWER | 0x0000 | Transmit Oversize Frame Counter (lower 16 bits): Incremented for each oversized transmitted frame with a correct FCS value. |
| 0x01126 | 1-0 | TOVR_UPPER | 0x0000 | Transmit Oversize Frame Counter (upper 2 bits): Incremented for each oversized transmitted frame with a correct FCS value. |
| 0x01128 | 15-0 | TUND_LOWER | 0x0000 | Transmit Undersize Frame Counter (lower 16 bits): Incremented for every frame less than 64 bytes, with a correct FCS value. When in half-duplex mode, the actual transmit undersize frame count is determined by TUND_LOWER (register 0x01128), TUND_UPPER (register 0x0112a), TXCL_LOWER (register 0x01108), TXCL_UPPER (register 0x0110a), TLCL_LOWER (register 0x01104) and TLCL_UPPER (register 0x01106). |
| 0x0112a | 1-0 | TUND_UPPER | 0x0000 | Transmit Undersize Frame Counter (upper 2 bits): Incremented for every frame less than 64 bytes, with a correct FCS value. When in half-duplex mode, the actual transmit undersize frame count is determined by TUND_LOWER (register 0x01128), TUND_UPPER (register 0x0112a), TXCL_LOWER (register 0x01108), TXCL_UPPER (register 0x0110a), TLCL_LOWER (register 0x01104) and TLCL_UPPER (register 0x01106). |

Table 15: MAC Transmit Counters

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------|--------|---|
| 0x0112c | 15-0 | TFRG_LOWER | 0x0000 | Transmit Fragment Counter (lower 16 bits): Incremented for every frame less than 64 bytes, with an incorrect FCS value. |
| 0x0112e | 1-0 | TFRG_UPPER | 0x0000 | Transmit Fragment Counter (upper 2 bits): Incremented for every frame less than 64 bytes, with an incorrect FCS value. |

Table 16: MAC Interface Status Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|----------|-----------------|--------|--|
| 0x0003c | 0 | Jabber | 0x0000 | JABBER: When read as a '1', the MAC has detected a Jabber condition. When read as a '0', the MAC has not detected a Jabber condition. This bit latches high. |
| | 1 | Sqe Error | | SQE ERROR: When read as a '1', the MAC has detected an SQE Error. When read as a '0', the MAC has not detected an SQE Error. This bit latches high. |
| | 2 | Loss of Carrier | | LOSS OF CARRIER: When read as a '1', the MAC has detected a Loss of Carrier. When read as a '0', the MAC has not detected a Loss of Carrier. This bit latches high. |
| | 3 | Reserved | | |
| | 4 | Speed | | SPEED: When read as a '1', the Serial MII PHY is operating at 100 Mbit/s mode. When read as a '0', the Serial MII PHY is operating at 10 Mbit/s. |
| | 5 | Full Duplex | | FULL DUPLEX: When read as a '1', the Serial MII PHY is operating in Full Duplex mode. When read as a '0', the Serial MII PHY is operating in Half Duplex mode. |
| | 6 | Link OK | | LINK OK: When read as a '1', the Serial MII PHY has detected a valid link. When read as a '0', the Serial MII PHY has not detected a valid link. |
| | 7 | Jabber | | JABBER: When read as a '1', the Serial MII PHY has detected a jabber condition on the link. When read as a '0', the Serial MII PHY has not detected a jabber condition. |
| | 8 | Clash | | CLASH: When read as a '1', the Serial MII module is in MAC to MAC mode with the partner in 10 Mbit/s and/or Half Duplex mode indicative of a configuration error. When read as a '0', the Serial MII module is either in PHY mode or in a properly configured MAC to MAC mode. |
| | 9 | Excess Defer | | EXCESS DEFER: This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high. Its default is '0'. |
| 15-10 | Reserved | | | |

Note: Carry register Bits are cleared on carry register write while respective Bit is asserted. When one of the below Carry mask Bits are set to zero, the corresponding interrupt Bit is allowed to cause interrupt indications on output CARRY.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 17: MAC Carry and Carry Mask Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|-------|-----------|---|--|
| 0x01130 | 0 | Reserved | 0 | Reserved |
| | 1 | C1RJB | 0 | Carry register 1 RJBR Counter Carry Bit |
| | 2 | C1RFR | 0 | Carry register 1 RFRG Counter Carry Bit |
| | 3 | C1ROV | 0 | Carry register 1 ROVR Counter Carry Bit |
| | 4 | C1RUN | 0 | Carry register 1 RUND Counter Carry Bit |
| | 5 | C1RCS | 0 | Carry register 1 RCSE Counter Carry Bit |
| | 6 | C1RCD | 0 | Carry register 1 RCDE Counter Carry Bit |
| | 7 | C1RFL | 0 | Carry register 1 RFLR Counter Carry Bit |
| | 8 | C1RAL | 0 | Carry register 1 RALN Counter Carry Bit |
| | 9 | C1RXU | 0 | Carry register 1 RXUO Counter Carry Bit |
| | 10 | C1RXP | 0 | Carry register 1 RXPF Counter Carry Bit |
| | 11 | C1RXC | 0 | Carry register 1 RXCF Counter Carry Bit |
| | 12 | C1RBC | 0 | Carry register 1 RBCA Counter Carry Bit |
| | 13 | C1RMC | 0 | Carry register 1 RMCA Counter Carry Bit |
| | 14 | C1RFC | 0 | Carry register 1 RFCS Counter Carry Bit |
| 15 | C1RPK | 0 | Carry register 1 RPKT Counter Carry Bit | |
| 0x01132 | 0 | C1RBY | 0 | Carry register 1 RBYT Counter Carry Bit |
| | 9 | C1MGV | 0 | Carry register 1 TRMGV Counter Carry Bit |
| | 10 | C1MAX | 0 | Carry register 1 TRMAX Counter Carry Bit |
| | 11 | C11K | 0 | Carry register 1 TR1K Counter Carry Bit |
| | 12 | C1511 | 0 | Carry register 1 TR511 Counter Carry Bit |
| | 13 | C1255 | 0 | Carry register 1 TR255 Counter Carry Bit |
| | 14 | C1127 | 0 | Carry register 1 TR127 Counter Carry Bit |
| | 15 | C164 | 0 | Carry register 1 TR64 Counter Carry Bit |

Table 17: MAC Carry and Carry Mask Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|-------|-----------|---|---|
| 0x01134 | 0 | Reserved | 0 | Reserved |
| | 1 | Reserved | 0 | Reserved |
| | 2 | C2TNC | 0 | Carry register 2 TNCL Counter Carry Bit |
| | 3 | C2TXC | 0 | Carry register 2 TXCL Counter Carry Bit |
| | 4 | C2TLC | 0 | Carry register 2 TLCL Counter Carry Bit |
| | 5 | C2TMA | 0 | Carry register 2 TMAL Counter Carry Bit |
| | 6 | C2TSC | 0 | Carry register 2 TSCL Counter Carry Bit |
| | 7 | C2TED | 0 | Carry register 2 TEDF Counter Carry Bit |
| | 8 | C2TDF | 0 | Carry register 2 TDFR Counter Carry Bit |
| | 9 | C2TPF | 0 | Carry register 2 TXPF Counter Carry Bit |
| | 10 | C2TBC | 0 | Carry register 2 TBCA Counter Carry Bit |
| | 11 | C2TMC | 0 | Carry register 2 TMCA Counter Carry Bit |
| | 12 | C2TPK | 0 | Carry register 2 TPKT Counter Carry Bit |
| | 13 | C2TBY | 0 | Carry register 2 TBYT Counter Carry Bit |
| | 14 | C2TFG | 0 | Carry register 2 TFRG Counter Carry Bit |
| 15 | C2TUN | 0 | Carry register 2 TUND Counter Carry Bit | |
| 0x01136 | 0 | C2TOV | 0 | Carry register 2 TOVR Counter Carry Bit |
| | 1 | C2TCF | 0 | Carry register 2 TXCF Counter Carry Bit |
| | 2 | C2TFC | 0 | Carry register 2 TFCS Counter Carry Bit |
| | 3 | C2TJB | 0 | Carry register 2 TJBR Counter Carry Bit |
| 0x01138 | 0 | Reserved | 1 | Reserved |
| | 1 | M1RJB | 1 | Mask register 1 RJBR Counter Carry Bit |
| | 2 | M1RFR | 1 | Mask register 1 RFRG Counter Carry Bit |
| | 3 | M1ROV | 1 | Mask register 1 ROVR Counter Carry Bit |
| | 4 | M1RUN | 1 | Mask register 1 RUND Counter Carry Bit |
| | 5 | M1RCS | 1 | Mask register 1 RCSE Counter Carry Bit |
| | 6 | M1RCD | 1 | Mask register 1 RCK0 Counter Carry Bit |
| | 7 | M1RFL | 1 | Mask register 1 RFLR Counter Carry Bit |
| | 8 | M1RAL | 1 | Mask register 1 RALN Counter Carry Bit |
| | 9 | M1RXU | 1 | Mask register 1 RXUO Counter Carry Bit |
| | 10 | M1RXP | 1 | Mask register 1 RXPF Counter Carry Bit |
| | 11 | M1RXC | 1 | Mask register 1 RXCF Counter Carry Bit |
| | 12 | M1RBC | 1 | Mask register 1 RBCA Counter Carry Bit |
| | 13 | M1RMC | 1 | Mask register 1 RMCA Counter Carry Bit |
| | 14 | M1RFC | 1 | Mask register 1 RFCS Counter Carry Bit |
| 15 | M1RPK | 1 | Mask register 1 RPKT Counter Carry Bit | |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 17: MAC Carry and Carry Mask Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|------|---|
| 0x0113a | 0 | M1RBY | 1 | Mask register 1 RBYT Counter Carry Bit |
| | 9 | M1MGV | 1 | Mask register 1 TRMGV Counter Carry Bit |
| | 10 | M1MAX | 1 | Mask register 1 TRMAX Counter Carry Bit |
| | 11 | M11K | 1 | Mask register 1 TR1K Counter Carry Bit |
| | 12 | M1511 | 1 | Mask register 1 TR511 Counter Carry Bit |
| | 13 | M1255 | 1 | Mask register 1 TR255 Counter Carry Bit |
| | 14 | M1127 | 1 | Mask register 1 TR127 Counter Carry Bit |
| | 15 | M164 | 1 | Mask register 1 TR64 Counter Carry Bit |
| 0x0113c | 0 | Reserved | 1 | Reserved |
| | 1 | Reserved | 1 | Reserved |
| | 2 | M2TNC | 1 | Mask register 2 TNCL Counter Carry Bit |
| | 3 | M2TXC | 1 | Mask register 2 TXCL Counter Carry Bit |
| | 4 | M2TLC | 1 | Mask register 2 TLCL Counter Carry Bit |
| | 5 | M2TMA | 1 | Mask register 2 TMAL Counter Carry Bit |
| | 6 | M2TSC | 1 | Mask register 2 TSCL Counter Carry Bit |
| | 7 | M2TED | 1 | Mask register 2 TEDF Counter Carry Bit |
| | 8 | M2TDF | 1 | Mask register 2 TDFR Counter Carry Bit |
| | 9 | M2TPF | 1 | Mask register 2 TXPF Counter Carry Bit |
| | 10 | M2TBC | 1 | Mask register 2 TBCA Counter Carry Bit |
| | 11 | M2TMC | 1 | Mask register 2 TMCA Counter Carry Bit |
| | 12 | M2TPK | 1 | Mask register 2 TPD0 Counter Carry Bit |
| | 13 | M2TBY | 1 | Mask register 2 TBYT Counter Carry Bit |
| | 15 | M2TUN | 1 | Mask register 2 TUND Counter Carry Bit |
| 0x0113e | 0 | M2TOV | 1 | Mask register 2 TOVR Counter Carry Bit |
| | 1 | M2TCF | 1 | Mask register 2 TXCF Counter Carry Bit |
| | 2 | M2TFC | 1 | Mask register 2 TFCS Counter Carry Bit |
| | 3 | M2TJB | 1 | Mask register 2 TJBR Counter Carry Bit |

Tables 18 through 23 - Configuration of the MAC

Table 18: MAC Configuration Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------------------------|--------|---|
| 0x00000 | 0 | Transmit Enable | 0x0000 | TRANSMIT ENABLE: Setting this bit will allow the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames. Its default is '0'. It is possible for one frame to be transmitted after the Transmit Enable bit is set to zero. To avoid this the transmit MAC can be disabled by using the Reset Tx MAC control bit. |
| | 1 | Synchronized Enable | | SYNCHRONIZED TRANSMIT: Read only status bit - a one indicates that the Transmit Enable is synchronized to the transmit stream. |
| | 2 | Receive Enable | | RECEIVE ENABLE: Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames. Its default is '0'. |
| | 3 | Synchronized Received Enable | | SYNCHRONIZED RECEIVE ENABLE: Read only status bit - a one indicates that the Receive Enable is synchronized to the receive data stream. |
| | 4 | Transmit Flow Control Enable | | TRANSMIT FLOW CONTROL ENABLE: Setting this bit will allow the Transmit MAC Control to send PAUSE Flow Control frames when requested by the system. Clearing this bit prevents the Transmit MAC Control from sending Flow Control frames. Default is '0'. |
| | 5 | Receive Flow Control Enable | | RECEIVE FLOW CONTROL ENABLE: Setting this bit will cause the Receive MAC Control to detect and act on PAUSE Flow Control frames. Clearing this bit causes the Receive MAC Control to ignore PAUSE Flow Control frames. Its default is '0'. |
| | 7-6 | Reserved | | |
| | 8 | Loop Back | | LOOP BACK: Setting this bit will cause the MAC Transmit outputs to be looped back to the MAC Receive inputs. Clearing this bit results in normal operation. Default is '0'. When this loopback is selected, frames are transmitted to the client. |
| | 15-9 | Reserved | | |
| 0x00002 | 0 | Reset Tx Function | 0x8000 | RESET TX FUNCTION: Setting this bit will put the Transmit Function block in reset. This block performs the frame transmission protocol. Its default is '0'. |
| | 1 | Reset Rx Function | | RESET RX FUNCTION: Setting this bit will put the Receive Function block in reset. This block performs the receive frame protocol. Its default is '0'. |
| | 2 | Reset Tx MAC Control | | RESET TX MAC CONTROL: Setting this bit will put the Transmit MAC Control block in reset. This block multiplexes data and Control frame transfers. It also responds to XOFF PAUSE Control frames. Its default is '0'. |
| | 3 | Reset Rx MAC Control | | RESET RX MAC CONTROL: Setting this bit will put the Receive MAC Control block in reset. This block detects Control frames and contains the pause timers. Its default is '0'. |
| | 13-4 | Reserved | | |
| | 14 | Reserved | | |
| | 15 | Soft Reset | | SOFT RESET: Setting this bit will put all modules within the MAC in reset except the Host Interface. The Host Interface is reset via HRST. Its default is '1'. This bit must remain set to 1 during configuration of the port, associated encapsulation/decapsulation blocks and mapper/demapper blocks. (i.e., This should be cleared only after the reset of the desired blocks, including MACs, are configured.) |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 18: MAC Configuration Registers

| Address | Bit | HW Symbol | Init | Description | | | | | | | | | | | | | | | |
|----------------------------------|-----------------|--|--------|---|----------------|-------|-------|----------|---|---|----------------------------------|---|---|------------------------------|---|---|----------|---|---|
| 0x00004 | 0 | Full Duplex | 0x7000 | FULL DUPLEX: Setting this bit will configure the MAC to operate in Full Duplex mode. Clearing this bit will configure the MAC to operate in Half Duplex mode only. Its default is '1'. | | | | | | | | | | | | | | | |
| | 1 | CRC Enable | | CRC ENABLE: Set this bit to have the MAC append a CRC on all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC. If the configuration bit PAD/CRC ENABLE or the per-packet PAD/CRC ENABLE is set, CRC ENABLE is ignored. Its defaults is '0' | | | | | | | | | | | | | | | |
| | 2 | Pad / CRC Enable | | PAD / CRC ENABLE: Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC. Its defaults is '0'. | | | | | | | | | | | | | | | |
| | 3 | Reserved | | | | | | | | | | | | | | | | | |
| | 4 | Length Field Checking | | LENGTH FIELD CHECKING: Set this bit to cause the MAC to check the frame's length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired. Its default is '0'. | | | | | | | | | | | | | | | |
| | 5 | Huge Frame Enable | | HUGE FRAME ENABLE: Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value. Its default is '0'. | | | | | | | | | | | | | | | |
| | 7-6 | Reserved | | | | | | | | | | | | | | | | | |
| | 9-8 | Interface Mode | | INTERFACE MODE: This field determines the type of interface the MAC is connected to: <table border="0" style="margin-left: 20px;"> <tr> <td>Interface Mode</td> <td style="text-align: center;">Bit 9</td> <td style="text-align: center;">Bit 8</td> </tr> <tr> <td>Reserved</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> </tr> <tr> <td>Nibble Mode (10/100 Mbit/s SMII)</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Byte Mode (1000 Mbit/s GMII)</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> <tr> <td>Reserved</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> </tr> </table> Its default is '0x0'. | Interface Mode | Bit 9 | Bit 8 | Reserved | 0 | 0 | Nibble Mode (10/100 Mbit/s SMII) | 0 | 1 | Byte Mode (1000 Mbit/s GMII) | 1 | 0 | Reserved | 1 | 1 |
| | Interface Mode | Bit 9 | | Bit 8 | | | | | | | | | | | | | | | |
| Reserved | 0 | 0 | | | | | | | | | | | | | | | | | |
| Nibble Mode (10/100 Mbit/s SMII) | 0 | 1 | | | | | | | | | | | | | | | | | |
| Byte Mode (1000 Mbit/s GMII) | 1 | 0 | | | | | | | | | | | | | | | | | |
| Reserved | 1 | 1 | | | | | | | | | | | | | | | | | |
| 11-10 | Reserved | | | | | | | | | | | | | | | | | | |
| 15-12 | Preamble Length | PREAMBLE LENGTH: This field determines the length of the preamble field of the packet, in bytes. Valid range for this field is 0x2 through 0x7 and the default is 0x7. | | | | | | | | | | | | | | | | | |

Table 19: MAC Station Address Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------------|--------|---|
| 0x00040 | 7-0 | Station Address | 0x0000 | STATION ADDRESS, 4 th octet: This field holds the fourth octet of the station Address. The fourth octet is stored in 7:0 and defaults to '0x00'. |
| | 15-8 | Station Address | | STATION ADDRESS, 3 rd octet: This field holds the third octet of the station Address. The third octet is stored in 15:8 and defaults to '0x00'. |
| 0x00042 | 7-0 | Station Address | 0x0000 | STATION ADDRESS, 2 nd octet: This field holds the second octet of the station Address. The second octet is stored in 23:16 and defaults to '0x00'. |
| | 15-8 | Station Address | | STATION ADDRESS, 1 st octet: This field holds the first octet of the station Address. The first octet is stored in 31:24 and defaults to '0x00'. |

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------------|--------|---|
| 0x00046 | 7-0 | Station Address | 0x0000 | STATION ADDRESS, 6 th octet: This field holds the sixth octet of the station Address. The sixth octet is stored in 23:16 and defaults to '0x00'. |
| | 15-8 | Station Address | | STATION ADDRESS, 5 th octet: This field holds the fifth octet of the station Address. The fifth octet is stored in 31:24 and defaults to '0x00'. |

Table 20: MAC IPG / IFG Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-------------------------------|--------|--|
| 0x00008 | 6-0 | Back to Back inter packet gap | 0x5060 | FULL DUPLEX INTER-PACKET-GAP: Sets the minimum interpacket gap between back-to-back transmitted packets in full duplex mode. Program this field to the number of bit times of IPG desired, from 0x0C to 0x7F. The default setting of 0x60 (96d) represents the standard minimum IPG of 96 bit times. |
| | 7 | Reserved | | |
| | 15-8 | Minimum IFG Enforcement | | MINIMUM IFG ENFORCEMENT: Sets the minimum number of bit times of interframe gap that is enforced between received frames. A frame following an undersized IFG is dropped. Set the register to the desired IFG in bit times plus 0x40. The default setting of 0x50 enforces a minimum IFG of 16 bit times. Range is from 0x40 to 0xFF. |
| 0x0000a | 6-0 | IPGR2 | 0x4060 | HALF DUPLEX INTER-PACKET-GAP (IPGR2): Sets the minimum interpacket gap for half duplex mode. IPG2 is the time between the end of a received packet and the start of a transmitted packet, or the time between two transmitted packets, as measured at the SMII interface of the EtherMap-3. Set the register to the number of desired bit times plus 0x04. The range of values for IPGR2 is from 0x1C to 0x7F and defaults to 0x60. |
| | 7 | Reserved | | |
| | 14-8 | IPGR1 | | NON-BACK-TO-BACK INTER-PACKET-GAP PART 1 (IPGR1): Sets the carrierSense window referenced in IEEE 802.3/4.2.3.2.1 'Carrier Deference'. If carrier is detected during the timing of IPG1, the MAC defers to carrier. If, however, carrier becomes active after IPG1, the MAC continues timing to the end of IPG2 and transmits, knowingly causing a collision, thus ensuring fair access to medium. To set the register, use the equation: $IPGR1 = IPG2 - IPG1 - 0x0C$ where IPGR1 is the register value, IPG1 is the carrierSense window in bit times and IPG2 is the total IPG in bit times (not the IPGR2 register value) The range of values for IPG1 is from 0 to IPG2. The register default is 0x40. To follow the two-thirds/one-thirds (96/64) guideline: $96 - 64 - 12 = 20 = 0x14$. |
| | 15 | Reserved | | |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 21: MAC Half Duplex Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|-------|---|--------|--|
| 0x0000c | 9-0 | Collision Window | 0xF037 | COLLISION WINDOW: Sets the collision window which is the number of slot times from the beginning of transmission during which collisions can occur in properly configured networks. Set the register to the frame byte count at the end of the desired window. The default of 0x37 yields the standard 512 slot window (frame count of 55 bytes plus the preamble and SFD). Range is from 0 to 0x3F. |
| | 11-10 | Reserved | | |
| | 15-12 | Retransmission Maximum | | RETRANSMISSION MAXIMUM: Sets the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The default of 0xF is the standard attemptLimit of 16. Range is from 0 to 0xF. |
| 0x0000e | 0 | Excessive Defer | 0x00A1 | EXCESSIVE DEFER: Setting this bit will configure the TX MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the TX MAC to abort the transmission of a packet that has been excessively deferred. Its default is '1'. |
| | 1 | No Backoff | | NO BACKOFF: Setting this bit will configure the TX MAC to immediately re-transmit following a collision. Clearing this bit will cause the TX MAC to follow the binary exponential back off rule. Its default is '0'. |
| | 2 | Back Pressure No Backoff | | BACK PRESSURE NO BACKOFF: Setting this bit will configure the TX MAC to immediately re-transmit, following a collision, during back pressure operation. Clearing this bit will cause the TX MAC to follow the binary exponential back off rule. Its default is '0'. |
| | 3 | ALTERNATE BINARY EXPONENTIAL BACK-OFF ENABLE | | ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE: Setting this bit will configure the Tx MAC to use the ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION register value instead of the 802.3 standard of ten, as described on page 135 . Clearing this bit will cause the Tx MAC to follow the standard binary exponential back off rule. Its default is '0'. |
| | 7-4 | ALTERNATE BINARY EXPONENTIAL BACK-OFF TRUNCATION: | | ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION: This field is used when ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE is set. The value programmed is substituted for the Ethernet standard value of ten. Its default is '0xA'. |
| | 15-8 | Reserved | | |

Table 22: MAC Maximum Frame Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|----------------------|--------|--|
| 0x00010 | 15-0 | Maximum Frame Length | 0x0600 | MAXIMUM FRAME LENGTH: This field resets to 0x0600 (1536d), which represents the maximum frame size in both the transmit and receive directions. If a different maximum length restriction is desired, program this 16-bit field. |

Table 23: MAC Test Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|--------------------|--------|---|
| 0x0001c | 0 | Shortcut Slot Time | 0x0000 | SHORTCUT SLOT TIME: This bit allows the slot time counter to expire regardless of the current count. This bit is for testing purposes only. Its default is '0'. |
| | 1 | Test Pause | | TEST PAUSE: Setting this bit allows the MAC to be paused via the host interface for testing purposes. Its default is '0'. |
| | 2 | Reserved | | |
| | 3 | Maximum Backoff | | MAXIMUM BACKOFF: Setting this bit will cause the MAC to backoff for the maximum possible length of time. This test bit is used to predict back-off times in Half Duplex mode. Its default is '0'. |
| | 15-4 | Reserved | | |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Tables 24 through 29 - MII Management Interface (used for MAC0 only)

Table 24: MAC MII Mgmt Configuration Registers

| Address | Bit | HW Symbol | Init | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|---------------------------|--|--------|--|-------------------|-------|-------|-------|---------------------------|---|---|---|---------------------------|---|---|---|---------------------------|---|---|---|---------------------------|---|---|---|----------------------------|---|---|---|----------------------------|---|---|---|----------------------------|---|---|---|----------------------------|---|---|---|
| 0x00020 | 2-0 | Mgmt Clock Select | 0x0000 | <p>MGMT CLOCK SELECT: This field determines the clock frequency of the Mgmt Clock (MDC), according to the following table:</p> <table border="1"> <thead> <tr> <th>Mgmt Clock Select</th> <th>Bit 2</th> <th>Bit 1</th> <th>Bit 0</th> </tr> </thead> <tbody> <tr> <td>Source Clock divided by 4</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Source Clock divided by 4</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Source Clock divided by 6</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Source Clock divided by 8</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Source Clock divided by 10</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>Source Clock divided by 14</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>Source Clock divided by 20</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Source Clock divided by 28</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Its default is '000'.</p> | Mgmt Clock Select | Bit 2 | Bit 1 | Bit 0 | Source Clock divided by 4 | 0 | 0 | 0 | Source Clock divided by 4 | 0 | 0 | 1 | Source Clock divided by 6 | 0 | 1 | 0 | Source Clock divided by 8 | 0 | 1 | 1 | Source Clock divided by 10 | 1 | 0 | 0 | Source Clock divided by 14 | 1 | 0 | 1 | Source Clock divided by 20 | 1 | 1 | 0 | Source Clock divided by 28 | 1 | 1 | 1 |
| | Mgmt Clock Select | Bit 2 | | Bit 1 | Bit 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Source Clock divided by 4 | 0 | | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Source Clock divided by 4 | 0 | | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Source Clock divided by 6 | 0 | | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Source Clock divided by 8 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Source Clock divided by 10 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Source Clock divided by 14 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Source Clock divided by 20 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Source Clock divided by 28 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | Preamble Sup- pression | <p>PREAMBLE SUPPRESSION: Setting this bit causes the MII MGMT to suppress preamble generation and reduce the Mgmt cycle from 64 clocks to 32 clocks. This is in accordance with IEEE 802.3/22.2.4.4.2. Clearing this bit causes the MII Mgmt to perform Mgmt read/write cycles with the 32 clocks of preamble. Its default is '0'.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | PhyInc | <p>PHY Increment: Automatically increments PHY address in Scan mode. Default is '0' (off).</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15-6 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x00022 | 14-0 | Reserved | 0x0000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 15 | Reset MII Mgmt | | <p>RESET MII MGMT: Setting this bit resets the MII Mgmt. Clearing this bit allows the MII Mgmt to perform Mgmt read/write cycles as requested via the Host Interface. Its default is '0'.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 25: MAC MII Mgmt Command Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------|--------|--|
| 0x00024 | 0 | Read Cycle | 0x0000 | <p>READ CYCLE: This bit causes the MII Mgmt to perform a single Read cycle when transitioned from 0 to 1. The Read data is returned in Register 0x00030 (MII Mgmt Status). Its default is '0'.</p> |
| | 1 | Scan Cycle | | <p>SCAN CYCLE: This bit causes the MII Mgmt to perform Read cycles continuously. This is useful for monitoring Link Fail for example. Its default is '0'.</p> |
| | 15-2 | Reserved | | |

Table 26: MAC MII Mgmt Address Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|-------|------------------|--------|---|
| 0x00028 | 4-0 | Register Address | 0x0000 | REGISTER ADDRESS: This field represents the 5-bit Register Address field of Mgmt cycles. Up to 32 registers can be accessed. Its default is 'TX'. |
| | 7-5 | Reserved | | |
| | 12-8 | Phy Address | | PHY ADDRESS: This field represents the 5-bit PHY Address field of Mgmt cycles. Up to 31 PHYs can be Addressed (0 is Reserved). Its default is '0x00'. |
| | 15-13 | Reserved | | |

Table 27: MAC MII Mgmt Control Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------------|--------|---|
| 0x0002c | 15-0 | MII Mgmt Control | 0x0000 | MII MGMT CONTROL (PHY Control): When written, an MII Mgmt write cycle is performed using the 16-bit data and the pre-configured PHY and Register Addresses from the MII Mgmt Address Register (0x00028). Its default is '0x0000'. |

Table 28: MAC MII Mgmt Status Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------------|--------|--|
| 0x00030 | 15-0 | MII Mgmt Status | 0x0000 | MII MGMT STATUS (PHY STATUS): Following an MII Mgmt Read Cycle, the 16-bit data can be read from this location. Its default is '0x0000'. |

Table 29: MAC MII Mgmt Indicators Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------|--------|---|
| 0x00034 | 0 | Busy | 0x0000 | BUSY: When '1' is returned - indicates MII Mgmt block is currently performing an MII Mgmt Read or Write cycle. |
| | 1 | Scanning | | SCANNING: When '1' is returned - indicates a scan operation (continuous MII Mgmt Read cycles) is in progress. |
| | 2 | Not Valid | | NOT VALID: When '1' is returned - indicates MII Mgmt Read cycle has not completed and the Read Data is not yet valid. |
| | 15-3 | Reserved | | |



ETHERNET MAC REGISTERS

Note: Throughout all the following sections of the memory map, we will use the suffix "d" for registers which indicate a defect, "a" for registers which indicate an alarm, "c" for control registers, "rpc" for performance counters. Also we use suffix "x" to index the eight MAC's.

Tables 30 through 34 - Configuration, Alarms and Interrupts of the Ethernet MACs

Table 30: MAC Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-------------------|--------|--|
| 0x1d340 | 7-0 | AUTOZ | 0x00FF | MAC: Automatic zero Addressed Statistics counter value for the MAC 1: all statistics counters saturate and are cleared on read 0: all statistics counters roll-over and are not cleared on read One bit per MAC (LSB for MAC0, ..., MSB for MAC7) |
| 0x1d342 | 7-0 | STEN | 0x0000 | MAC: Statistics enable 1: Statistics are enabled 0: Statistics are disabled One bit per MAC (LSB for MAC0, ..., MSB for MAC7) |
| 0x1d344 | 1-0 | cINRT_SOTERN_CORE | 0x0001 | Alarm latching configuration for the MAC alarm group (Table 33) Criteria used to create latched alarms from the raw (unlatched) alarms. 00: positive level 01: rising edge (default) 10: falling edge 11: rising or falling edge |
| 0x1d346 0x1d34c 0x1d352 0x1d358 0x1d35e 0x1d364 0x1d36a 0x1d370 | 15-0 | rHWPT_x | 0xFFFF | Flow Control: High Pause Time Value for MAC0-7 when exceeding the set high watermark value. The contents of this register are inserted into the outgoing PAUSE frame in the pause_time field. Recommended value for GMII mode is 0x3A98. Recommended value for SMII mode is 0x012C. |
| 0x1d348 0x1d34e 0x1d354 0x1d35a 0x1d360 0x1d366 0x1d36c 0x1d372 | 15-0 | rLWPT_x | 0x0000 | Flow Control: Low Pause Time Value for MAC0-7 when receding below the low watermark value. The contents of this register are inserted into the outgoing PAUSE frame in the pause_time field. Recommended value for both SMII and GMII modes is 0x0000. |
| 0x1d34a 0x1d350 0x1d356 0x1d35c 0x1d362 0x1d368 0x1d36e 0x1d374 | 15-0 | rHIPSE_x | 0xBEEB | Flow Control: Internal local PAUSE timer value for the MAC0-7. After being loaded with the value in the rHWPT_x register, the internal pause timer is decremented until it reaches this value, so a smaller value in this register results in a longer time between sampling the Tx FIFO depth. Recommended value for GMII mode is 0x2710. Recommended value for SMII mode is 0x0032. |

Table 31: MAC Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x1d300 | 7-0 | CARRYx | 0x0000 | Carry overflow alarm for the MAC0-7 0: no carry overflow 1: carry overflow alarm One bit per MAC (LSB for MAC0, ..., MSB for MAC7) |

Table 32: MAC Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------------|--------|---|
| 0x1d320 | 7-0 | MaCARRYx | 0x00FF | Carry overflow alarm mask for the MAC0-7 1: alarm is masked 0: alarm is not masked One bit per MAC (LSB for MAC0, ..., MSB for MAC7) |
| 0x1d322 | 0 | MaMAC_Global_Interrupt | 0x0001 | Global interrupt mask for the MAC part 1: interrupt is masked 0: interrupt is not masked |

Table 33: MAC Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x1d310 | 7-0 | L1CARRYx | 0x0000 | Carry overflow latched alarm for the MAC0-7 1: alarm is latched. Cleared on read 0: no alarm is latched One bit per MAC (LSB for MAC0, ..., MSB for MAC7) |

Table 34: MAC Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|--------|--|
| 0x1d330 | 0 | MAC_CARRY_Interrupt | 0x0000 | Global Carry alarm interrupt for the MAC 1: interrupt is masked 0: interrupt is not masked |
| 0x1d332 | 0 | MAC_Global_Interrupt | 0x0000 | Global alarm interrupt for the MAC 1: interrupt is masked 0: interrupt is not masked |



TX ENCAPSULATION REGISTERS

Tables 35 through 47 - Configuration, Status and Alarms of the Encapsulation Block

Table 35: Encapsulation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|----------------|--------|--|
| 0x1fc00 0x1ffe0 0x101e0 0x105e0 0x109e0 0x10de0 0x111e0 0x115e0 | 1-0 | ctENCAPx | 0x0008 | Transmit Side Encapsulation mode selection for MAC0-7 00: LAPS (default) 01: LAPF 10: GFP 11: PPP |
| | 2 | ctTSCRDX | | Tx Encapsulation: LAPS/PPP scrambling control for MAC0-7 0: Enable scrambling for LAPS/PPP frame. (Default) 1: Disable scrambling for LAPS/PPP frame. |
| | 3 | ctFCSx | | Tx Encapsulation: FCS enabling for MAC0-7 (LAPS/LAPF) 0: FCS calculation disabled and the FCS field octets are not inserted. 1: FCS calculation enabled and the FCS field octets are inserted. (Default) |
| | 4 | ctFCSEx | | Tx Encapsulation: FCS error insertion for MAC0-7 (LAPS/LAPF/GFP) 0: FCS is transmitted without any inserted errors. (Default) 1: FCS is transmitted with errors inserted. |
| | 5 | ctABTGx | | Tx Encapsulation: force abort generation for MAC0-7 (LAPS/GFP/PPP) 0: no action 1: Frame(s) currently in transmission are aborted (i.e., while held at '1', will cause continuous aborts). In GFP mode an error is inserted in the Payload FCS field. In LAPS/PPP mode 0x7D is transmitted, followed by 0x7E. Notes: 1) This bit is a level type. 2) When FCS is enabled, a packet is transmitted with inverted FCS. 3) If asserted and deasserted between packets, the next packet is not aborted. 4) If asserted during GFP Idle frame, 1, 2, 3 or all 4 bytes of the IDLE frame may be inverted. 5) In PPP mode, the first aborted packet will contain two abort indications. |
| | 6 | ctOFFx | | Tx Encapsulation: suspend frame mapping in SONET/SDH for MAC0-7 (LAPS/LAPF/GFP) 0: Encapsulated frames are mapped to SONET/SDH tributaries for transmission. (Default) 1: Encapsulated frames are not mapped to SONET/SDH tributaries for transmission. Instead only flags (LAPS/LAPF) or idle frames (GFP) are mapped to SONET/SDH tributaries. |
| | 7 | ctPSCRDX | | Tx Encapsulation: GFP payload scrambling control for MAC0-7 (GFP) 0: Enable scrambling of GFP Payload area only. (Default) 1: Disable scrambling of GFP Payload area. |
| 0x1fc02 | 0 | END_INIT_MICRO | 0x0000 | End of microprocessor Initialization Must be set to '1' after completion of the device initialization phase. This bit is automatically cleared after a hard reset is provided to the device. This bit only needs to be set once after the chip has been reset by a hard reset or through the RESETH bit. It does not need to be modified afterwards to change configuration bits on the fly. See "Encapsulation/Decapsulation" on page 139 section for changing Encapsulation/Decapsulation registers on the fly. Only a hard reset or the RESETH bit can clear this bit. |
| 0x1fc04 0x1ffe2 0x101e2 0x105e2 0x109e2 0x10de2 0x111e2 0x115e2 | 15-0 | rTMAXFLx | 0x0640 | Tx LAPS/LAPF/GFP/PPP: Max frame length for MAC0-7 Configures the maximum number of bytes per frame, including the FCS bytes, that will be accepted from a MAC for encapsulation. Frames which exceed this length are discarded and corresponding alarms and counters are triggered Default is 0x640 (decimal 1600). |

Table 35: Encapsulation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|---------------|--------|---|
| 0x1fc06 0x1ffe4 0x101e4 0x105e4 0x109e4 0x10de4 0x111e4 0x115e4 | 0 | ctSCRINITx | 0x0000 | Tx LAPS/GFP/PPP: scrambler initial value for MAC0-7 0: on reset, initialize the 43-bit shift register to all zeros (default). 1: on reset, initialize the 43-bit shift register to all ones. |
| 0x1fc08 0x1ffe6 0x101e6 0x105e6 0x109e6 0x10de6 0x111e6 0x115e6 | 0 | ctFCSINITALLx | 0x0001 | Tx LAPS/LAPF/GFP/PPP: initial value of FCS generation registers for MAC0-7 0: on reset, initialize the FCS generation shift register to all zeros. 1: on reset, initialize the FCS generation shift register to all ones (default). |
| 0x1fc0a 0x1ffe8 0x101e8 0x105e8 0x109e8 0x10de8 0x111e8 0x115e8 | 0 | ctFCSSWAPINx | 0x0000 | Tx LAPS/LAPF/GFP/PPP: Bit swapping of FCS generation input for MAC0-7 At the input to the FCS generator, all data bytes over which the FCS is calculated, can be bit swapped (i.e., MSB <--> LSB). 0: data bytes are NOT modified (default). 1: data bytes are bit swapped. |
| 0x1fc0c 0x1ffea 0x101ea 0x105ea 0x109ea 0x10dea 0x111ea 0x115ea | 0 | ctFCSSWAPOUTx | 0x0000 | Tx LAPS/LAPF/GFP/PPP: Bit swapping of FCS generation output for MAC0-7 At the output of the FCS generator, all data bytes over which the FCS was calculated and the FCS bytes, can be bit swapped (i.e., MSB <--> LSB). 0: data bytes and FCS bytes are NOT modified (default). 1: data bytes and FCS bytes are bit swapped. |
| 0x1fc0e 0x1ffec 0x101ec 0x105ec 0x109ec 0x10dec 0x111ec 0x115ec | 0 | ctHECINITALLx | 0x0000 | Tx GFP: HEC generation initial value for MAC0-7 In GFP mode, this bit is used to control the initial value of the HEC generation shift register. 0: on reset, initialize the HEC generation register to all zeros (default). 1: on reset, initialize the HEC generation register to all ones. |
| 0x1fc10 0x1fee 0x101ee 0x105ee 0x109ee 0x10dee 0x111ee 0x115ee | 0 | ctHECSWAPINx | 0x0000 | Tx GFP/PPP: Bit swapping of HEC generation input for MAC0-7 In GFP mode, at the input to the HEC generator, all bytes over which the HEC is to be calculated can be bit swapped (i.e., MSB <--> LSB). 0: header bytes are NOT modified (default). 1: header bytes are bit swapped. |
| 0x1fc12 0x1fff0 0x101f0 0x105f0 0x109f0 0x10df0 0x111f0 0x115f0 | 0 | ctHECSWAPOUTx | 0x0000 | Tx GFP: Bit swapping of HEC generation output for MAC0-7 In GFP mode, at the output of the HEC generator, all bytes over which the HEC was calculated, and the HEC bytes, can be bit swapped (i.e., MSB <--> LSB). 0: header bytes and HEC bytes are NOT modified. 1: header bytes and HEC bytes are bit swapped. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 35: Encapsulation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---|-----|-----------|--------|--|
| 0x1fc14 0x1ff2 0x101f2 0x105f2 0x109f2 0x10df2 0x111f2 0x115f2 | 0 | cTCTLRSTx | 0x0000 | Tx LAPS/LAPF/GFP/PPP: Resets the Control Frame buffer for MAC0-7 Writing a 1 to this bit causes the Control Frame buffer to discard its present contents. The Control Frame buffer empty alarm will be set for the corresponding MAC (aTCTLXx). |

Table 36: Encapsulation Block - LAPS Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------|--------|--|
| 0x1fda0 0x1ffb0 0x101b0 0x105b0 0x109b0 0x10db0 0x111b0 0x115b0 | 0 | cTFLAGx | 0x0003 | Tx LAPS/LAPF/PPP: number of flag insertions between LAPS/LAPF frames for MAC0-7 0: Single flag is present between frames (i.e., a shared flag). 1: Two flags are present between frames. (Default). |
| | 2-1 | cTACSELx | | Tx LAPS: ADDRESS and CONTROL field insertion management for MAC0-7 00: ADDRESS and CONTROL field contents are fixed to zero 01: ADDRESS = 0x04 and CONTROL = 0x03 (Default) 10: Reserved 11: ADDRESS and CONTROL field contents inserted from rTACFDx register |
| | 3 | cTSAPIx | | Tx LAPS: SAPI field insertion for MAC0-7 0: SAPI field contents inserted from rTSAPFDx register 1: SAPI field contents are fixed to zero |
| | 4 | cTLPPDUx | | Tx LAPS: enable LAPS frame mapping SONET/SDH for MAC0-7 0: All LAPS frames are mapped into the SONET/SDH stream. 1: LAPS frames containing Ethernet frames from the MACs are not mapped. LAPS control frames from the host continue to be mapped. |
| 0x1fda2 0x1ffb2 0x101b2 0x105b2 0x109b2 0x10db2 0x111b2 0x115b2 | 15-0 | rTACFDx | 0x0403 | Tx LAPS: Configurable ADDRESS and CONTROL field contents for MAC0-7 Upper byte (Bits 15-8) = Content of the ADDRESS field. Default set to 0x04. Lower byte (Bits 7-0) = Content of the CONTROL field. Default set to 0x03. |
| 0x1fda4 0x1ffb4 0x101b4 0x105b4 0x109b4 0x10db4 0x111b4 0x115b4 | 15-0 | rTSAPFDx | 0xFE01 | Tx LAPS: Configurable SAPI field contents for MAC0-7 Upper byte (Bits 15-8) = Content of the first SAPI octet field. Default set to 0xFE. Lower byte (Bits 7-0) = Content of the second SAPI octet field. Default set to 0x01. |

Table 37: Encapsulation Block - LAPF Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|--|
| 0x1fd80 0x1ff80 0x10180 0x10580 0x10980 0x10d80 0x11180 0x11580 | 0 | cTFECNx | 0x0000 | Tx LAPF: Setting of FECN field for MAC0-7 0: Transmit FECN bit set to 0. (Default) 1: Transmit FECN bit set to 1. |
| | 1 | ctBECNx | | Tx LAPF: Setting of BECN field for MAC0-7 0: Transmit BECN bit set to 0. (Default) 1: Transmit BECN bit set to 1. |
| | 2 | ctDEx | | Tx LAPF: Setting of DE field for MAC0-7 0: Transmit DE bit set to 0. (Default) 1: Transmit DE bit set to 1. |
| | 3 | ctLFCNOPSELx | | Tx LAPF: ADDRESS, CONTROL, OUI, NLPID and PID fields insertion control for MAC0-7 0: ADDRESS, CONTROL, OUI, NLPID and PID field content insertion enabled. (Default) ADDRESS field contents taken from rTDLCIx, cTCRx, cTFECNx, ctBECNx and ctDEx registers. CONTROL field contents taken from rTLFCNTLx register. NLPID field contents taken from rTNLPIDx register. OUI field contents taken from rTOULx register. PID field contents taken from rTPIDx register. 1: ADDRESS, CONTROL, NLPID, OUI and PID field contents insertion is disabled. These fields are all set to zero. |
| | 4 | ctLFPADx | | Tx LAPF: PAD field insertion control for MAC0-7 0: PAD field insertion enabled and field contents are taken from the rTPADx register. Only one pad field octet is inserted regarding to the alignment of payload information to a two octet boundary (even length frame). 1: PAD field insertion disabled. No insertion of PAD field in LAPF frame. |
| | 5 | cTCRx | | Tx LAPF: Setting of Command/Response (C/R) field for MAC0-7 0: Transmit C/R bit set to 0. (Default) 1: Transmit C/R bit set to 1. |
| | 6 | ctLFPDUx | | Tx LAPF: LAPF frame mapping enable into SONET/SDH stream for MAC0-7 |
| 0x1fd82 0x1ff82 0x10182 0x10582 0x10982 0x10d82 0x11182 0x11582 | 9-0 | rTDLCIx | 0x0010 | Tx LAPF: Configurable DLCI field contents for MAC0-7 Range 0x010 to 0x3DF: Indicates DLCI field contents when insertion is enabled. Default is 0x010. |
| 0x1fd84 0x1ff84 0x10184 0x10584 0x10984 0x10d84 0x11184 0x11584 | 7-0 | rTLFCNTLx | 0x0003 | Tx LAPF: Configurable CONTROL field contents for MAC0-7 Range 0x00-0xFF: Indicates CONTROL field contents when insertion is enabled. Default is 0x03. |
| 0x1fd86 0x1ff86 0x10186 0x10586 0x10986 0x10d86 0x11186 0x11586 | 7-0 | rTPADx | 0x0000 | Tx LAPF: Configurable PAD field contents for MAC0-7 Range 0x00-0xFF: Indicates PAD field contents when insertion is enabled. Default is 0x00. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 37: Encapsulation Block - LAPF Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------|--------|--|
| 0x1fd88 0x1ff88 0x10188 0x10588 0x10988 0x10d88 0x11188 0x11588 | 7-0 | rTNLPIDx | 0x0080 | Tx LAPF: Configurable NLPID field contents for MAC0-7 Range 0x00-0xFF: Indicates NLPID field contents when insertion is enabled. Default is 0x80. |
| 0x1fd8a 0x1ff8a 0x1018a 0x1058a 0x1098a 0x10d8a 0x1118a 0x1158a | 7-0 | rTOUIx(1) | 0x0000 | Tx LAPF: Configurable OUI field contents (MSB bits) for MAC0-7 Range 0x00-0xFF: Indicates OUI (MSB bits) field contents when insertion is enabled. Default is 0x00. |
| 0x1fd8c 0x1ff8c 0x1018c 0x1058c 0x1098c 0x10d8c 0x1118c 0x1158c | 15-0 | rTOUIx(0) | 0x80C2 | Tx LAPF: Configurable OUI field contents (LSB bits) for MAC0-7 Range 0x0000-0xFFFF: Indicates OUI (LSB bits) field contents when insertion is enabled. Default is 0x80C2. |
| 0x1fd8e 0x1ff8e 0x1018e 0x1058e 0x1098e 0x10d8e 0x1118e 0x1158e | 15-0 | rTPIDx | 0x0007 | Tx LAPF: Configurable PID field contents for MAC0-7 Range 0x0000-0xFFFF: Indicates PID field contents when insertion is enabled. Default is 0x0007. |

Table 38: Encapsulation Block - GFP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---|------|-----------|--------|---|
| 0x1fcc0 0x1fd0 0x101d0 0x105d0 0x109d0 0x10dd0 0x111d0 0x115d0 | 2-0 | cPTIx | 0x0100 | Tx GFP: Configurable PTI field contents for MAC0-7 Range 0x0-0x7: Indicates contents of the PTI field for GFP Client Data frames only. Default is 0x0. |
| | 3 | cPFIx | | Tx GFP: Payload FCS indicator control for MAC0-7 0: The PFI bit within the GFP Payload Header is set to zero (0). GFP Payload FCS field is not inserted. (Default) 1: The PFI bit within the GFP Payload Header is set to one (1). GFP Payload FCS field is inserted. |
| | 7-4 | cEXIx | | Tx GFP: Configurable EXI field contents for MAC0-7 Range 0x0-0xF: Indicates contents of the EXI field within the GFP Payload header. Default is 0x0. |
| | 15-8 | cUPIx | | Tx GFP: Configurable UPI field contents for MAC0-7 Range 0x00-0xFF: Indicates contents of the UPI field for GFP Client Data frames only. Default is 0x01. |

Table 38: Encapsulation Block - GFP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---|-------|-------------|----------------|---|
| 0x1fcc2 0x1ffd2 0x101d2 0x105d2 0x109d2 0x10dd2 0x111d2 0x115d2 | 7-0 | cFECIDx | 0x0000 | Tx GFP: Configurable CID field contents for MAC0-7 Range 0x00-0xFF: Indicates contents of the CID field within the GFP Extension header when using GFP Linear frame structure. Default is 0x00. |
| | 15-8 | cSPAREx | | Tx GFP: Configurable SPARE field contents for MAC0-7 Range 0x00-0xFF: Indicates contents of the SPARE field within the GFP Extension header when using GFP Linear frame structure. Default is 0x00. |
| 0x1fcc4 0x1ffd4 0x101d4 0x105d4 0x109d4 0x10dd4 0x111d4 0x115d4 | 0 | cTCHecERRx | 0x0000 | Tx GFP: Core header HEC error insertion control for MAC0-7 0: Disable cHEC error insertion. (Default) 1: A single cHEC error is inserted by inverting all the bits in the calculated cHEC field. This bit self-clears after the errored frame is transmitted. |
| | 1 | cTtHEcERRx | | Tx GFP: Type header HEC error insertion control for MAC0-7 0: Disable tHEC error insertion. (Default) 1: A single tHEC error is inserted by inverting all the bits in the calculated tHEC field. This bit self-clears after the errored frame is transmitted. |
| | 2 | cTEHEcERRx | | Tx GFP: Extension header HEC error insertion control for MAC0-7 0: Disable eHEC error insertion. (Default) 1: A single eHEC error is inserted by inverting all the bits in the calculated eHEC field. This bit self-clears after the errored frame is transmitted. |
| | 3 | cTCSRx | | Tx GFP: Core header scrambling control for MAC0-7: 0: Enable scrambling of GFP Core header only. (Default) 1: Disable scrambling of GFP Core header only. |
| | 4 | cTGFPtXCSFx | | Tx GFP: CSF frame transmit mode control for MAC0-7 0: Disable GFP CSF frame transmit mode. (Default) 1: Enable GFP CSF frame transmit mode. One CSF frame is transmitted every 100 ms, with interim GFP idle frames. Client data frames are not transmitted. |
| | 5 | cTGFPpDUx | | TxGFP: GFP frame mapping enable into SONET/SDH stream for MAC0-7 0: All GFP frames are mapped into the SONET/SDH stream. 1: GFP frames containing Ethernet frames from the MACs are not mapped. Client management/control frames from the host continue to be mapped. |
| 0x1fcc6 0x1ffd6 0x101d6 0x105d6 0x109d6 0x10dd6 0x111d6 0x115d6 | 3-0 | CIDTablex_0 | see Note below | Tx GFP: CID table word 0 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 7-4 | CIDTablex_1 | | Tx GFP: CID table word 1 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 11-8 | CIDTablex_2 | | Tx GFP: CID table word 2 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 15-12 | CIDTablex_3 | | Tx GFP: CID table word 3 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| Note: Write all 0s to all 8 registers before configuring CID table to ensure that unused VCGs have 0 in their TX CID table. | | | | |



Table 38: Encapsulation Block - GFP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---|-------|-------------|----------------|---|
| 0x1fcc8 0x1ffd8 0x101d8 0x105d8 0x109d8 0x10dd8 0x111d8 0x115d8 | 3-0 | CIDTablex_4 | see Note below | Tx GFP: CID table word 4 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 7-4 | CIDTablex_5 | | Tx GFP: CID table word 5 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 11-8 | CIDTablex_6 | | Tx GFP: CID table word 6 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| | 15-12 | CIDTablex_7 | | Tx GFP: CID table word 7 for MAC0-7 (used in linear mode with cEXI = 1) Bit 3: 0 = This entry of the table is not valid (Default); 1 = This entry of the table is valid. Bits 2-0: (Range 0x0-0x7) Indicates the number of the selected MAC port. (Default=0x0) |
| Note: Write all 0s to all 8 registers before configuring CID table to ensure that unused VCGs have 0 in their TX CID table. | | | | |

Table 39: Encapsulation Block - PPP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|--|---------------|---|--|
| 0x1fce0 0x1ff40 0x10140 0x10540 0x10940 0x10d40 0x11140 0x11540 | 1-0 | cTPFCSx | 0x00A7 | Tx PPP: FCS generation mode for MAC0-7 00: disable FCS generation 01: Reserved 10: enable 16-bit FCS generation. Two FCS bytes are inserted. 11: enable 32-bit FCS generation. Four FCS bytes are inserted. (default) |
| | 3-2 | cTPPACSELx | | Tx PPP: Address and control field insertion for MAC0-7 00: Disable insertion: all address and control fields are set to zero. 01: Fixed insertion (default): The address field is inserted as 0xFF, the control field is inserted as 0x03. 10: Reserved 11: Programmable insertion: address and control fields are inserted from the rTPPACFDx register. |
| | 4 | cTPPPIx | | Tx PPP: Protocol field insertion for MAC0-7 0: enabled (default): protocol fields are inserted from the rTPPFDx register. 1: disabled: protocol fields are set to zero. |
| | 5 | cTBCPFLGFx | | Tx PPP: BCP flag F value for MAC0-7 0: insert 0. 1: insert 1. (default) |
| | 6 | cTBCPFLG0x | | Tx PPP: BCP flag 0 value for MAC0-7 0: insert 0. (default) 1: insert 1. |
| | 7 | cTBCPFLGZx | | Tx PPP: BCP flag Z value for MAC0-7 0: insert 0. 1: insert 1. (default) |
| | 8 | cTBCPFLGBx | | Tx PPP: BCP flag B value for MAC0-7 0: insert 0. (default) 1: insert 1. |
| | 9 | cTBPDUX | | Tx PPP: Frame mapping enable into SONET/SDH for MAC0-7 0: All PPP frames are mapped into the SONET/SDH stream (default). 1: Only LCP/NCP-BCP frames from the host are mapped. |
| | 10 | cTBCPPDCALCx | | Tx PPP: Control bit for Payload or entire frame padding 0: calculation of the number of padding octets on payload only (default) 1: calculation of the number of padding octets on the whole frame (Header + payload + FCS) |
| | 0x1fce2 0x1ff42 0x10142 0x10542 0x10942 0x10d42 0x11142 0x11542 | 1-0 | | rTBCPPDMODEx |
| 3-2 | | rTBCPPDALIGNx | Tx PPP: Octet alignment boundary configuration for MAC0-7 Configures the alignment boundary when using Fixed or Self-describing padding mode. 00: 2 octet alignment boundary (default). 01: 4 octet alignment boundary. 10: 8 octet alignment boundary. 11: 16 octet alignment boundary. | |
| 7-4 | | cTBCPPDMPVx | Reserved | |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 39: Encapsulation Block - PPP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------|--------|---|
| 0x1fce4 0x1ff44 0x10144 0x10544 0x10944 0x10d44 0x11144 0x11544 | 7-0 | rTBCPPADx | 0x0100 | Tx PPP: pad value for MAC0-7 Contents of the PPP PAD bytes when fixed padding is used. Default is 0x00. Values of 0x7D or 0x7E will result in incorrect byte stuffing and should be avoided. |
| 0x10944 0x10d44 0x11144 0x11544 | 15-8 | rTBCPMACx | | |
| 0x1fce6 0x1ff46 0x10146 0x10546 0x10946 0x10d46 0x11146 0x11546 | 15-0 | rTPPACFDx | 0xFF03 | Tx PPP: Address and control field values for MAC0-7 15-8: Address field. Default is 0xFF. 7-0: Control field. Default is 0x03. |
| 0x1fce8 0x1ff48 0x10148 0x10548 0x10948 0x10d48 0x11148 0x11548 | 15-0 | rTPPFDx | 0x0031 | Tx PPP: Protocol field values for MAC0-7 15-8: First protocol byte. Default is 0x00. 7-0: Second protocol byte. Default is 0x31. |

Table 40: Encapsulation Block - Control Frame Buffers (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------------------|-----|--------------------------|--------|---|
| 0x1fd00- 0x1fd7e | 8-0 | rTCTL_x_0- rTCTL_x_63 | 0x0000 | Tx Control Frame buffer for MAC0 to MAC7 Each control buffer can carry up to 64 bytes. |
| 0x1fe00- 0x1fe7e | | | | Msb bit of each word indicates if the byte (8 lsb bits of each word) is carrying or not control frame information (msb=1 means carrying, msb=0 means not carrying). |
| 0x10000- 0x1007e | | | | |
| 0x10400- 0x1047e | | | | |
| 0x10800- 0x1087e | | | | |
| 0x10c00- 0x10c7e | | | | |
| 0x11000- 0x1107e | | | | |
| 0x11400- 0x1147e | | | | |

Table 41: Encapsulation Block - Status (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------|--------|--|
| 0x1fdb0 0x1ffc8 0x101c8 0x105c8 0x109c8 0x10dc8 0x111c8 0x115c8 | 0 | stCTLBx | 0x0000 | Tx status: LMI buffer full for MAC0-7 Indicates the status of the Tx Control Frame Buffer for each respective MAC (rTCTL_x_n). The host should poll this bit before writing to the frame buffer. 0: Empty 1: Full |

Table 42: Encapsulation Block - Status Registers (RO)

| Address | Bit | HW Symbol | Init | Description |
|---|-----|-------------------|--------|--|
| 0x1fdb4 0x1ffc 0x101cc 0x105cc 0x109cc 0x10dcc 0x111cc 0x115cc | 0 | ENC_RST_END_INITx | 0x0000 | Tx Status: Reset Complete for MAC0-7 A one indicates the Encapsulation Block for each respective MAC has completed its initialization after receiving a hard or a soft reset. |

The following performance counters can be accessed in saturating mode or roll-over mode, depending on the state of the cCROV control bit. In saturating mode, counters do not count past their terminal count and are cleared to zero when read. In roll-over mode, counters roll-over to zero after reaching their terminal count, and are not cleared when read.

Table 43: Encapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|-------------------|--------|---|
| 0x1fc80 0x1ff00 0x10100 0x10500 0x10900 0x10d00 0x11100 0x11500 | 15-0 | rpcTGFPBYTEx_LSB | 0x0000 | Tx GFP: GFP byte counter for MAC0-7 - LSB Counts the total number of bytes in GFP frame payloads transmitted to SONET/SDH. This counter does not include the count of Host inserted GFP Client Management control frames. This counter does include the count of all fields of a GFP frame (including the Ethernet MAC frame). |
| 0x1fc82 0x1ff02 0x10102 0x10502 0x10902 0x10d02 0x11102 0x11502 | 15-0 | rpcTGFPBYTEx_MSB | 0x0000 | Tx GFP: GFP byte counter for MAC0-7 - MSB This counter does not include the count of Host inserted GFP Client Management control frames. This counter does include the count of all fields of a GFP frame (including the Ethernet MAC frame). |
| 0x1fc84 0x1ff04 0x10104 0x10504 0x10904 0x10d04 0x11104 0x11504 | 15-0 | rpcTGFPFRAMEx_LSB | 0x0000 | Tx GFP: GFP payload counter for MAC0-7 - LSB Counts the total number of GFP frame payloads transmitted to SONET/SDH. This counter does not include the count of Host inserted GFP Client Management control frames. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 43: Encapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|---------------------|--------|--|
| 0x1fc86 0x1ff06 0x10106 0x10506 0x10906 0x10d06 0x11106 0x11506 | 15-0 | rpcTGFPFRAMEx_MSB | 0x0000 | Tx GFP: GFP payload counter for MAC0-7 - MSB This counter does not include the count of Host inserted GFP Client Management control frames. |
| 0x1fc88 0x1ff08 0x10108 0x10508 0x10908 0x10d08 0x11108 0x11508 | 15-0 | rpcTLAPSBYTEx_LSB | 0x0000 | Tx LAPS: LAPS byte counter for MAC0-7 - LSB Counts the total number of bytes in LAPS frame payloads transmitted to SONET/SDH. This counter does not include the count of Host inserted LAPS Control frames. This counter does include the count of all fields of a LAPS frame (including the Ethernet MAC frame). |
| 0x1fc8a 0x1ff0a 0x1010a 0x1050a 0x1090a 0x10d0a 0x1110a 0x1150a | 15-0 | rpcTLAPSBYTEx_MSB | 0x0000 | Tx LAPS: LAPS byte counter for MAC0-7 - MSB This counter does not include the count of Host inserted LAPS Control frames. This counter does include the count of all fields of a LAPS frame (including the Ethernet MAC frame). |
| 0x1fc8c 0x1ff0c 0x1010c 0x1050c 0x1090c 0x10d0c 0x1110c 0x1150c | 15-0 | rpcTLAPSFFRAMEx_LSB | 0x0000 | Tx LAPS: LAPS frame counter for MAC0-7 - LSB Counts the total number of LAPS frames transmitted to SONET/SDH. This counter does not include the count of Host inserted LAPS Control frames. |
| 0x1fc8e 0x1ff0e 0x1010e 0x1050e 0x1090e 0x10d0e 0x1110e 0x1150e | 15-0 | rpcTLAPSFFRAMEx_MSB | 0x0000 | Tx LAPS: LAPS frame counter for MAC0-7 - MSB This counter does not include the count of Host inserted LAPS Control frames. |
| 0x1fc90 0x1ff10 0x10110 0x10510 0x10910 0x10d10 0x11110 0x11510 | 15-0 | rpcTLAPFBYTEx_LSB | 0x0000 | Tx LAPF: LAPF byte counter for MAC0-7 - LSB Counts the total number of bytes in LAPF frame payloads transmitted to SONET/SDH. This counter does not include the count of Host inserted LAPF LMI frames. This counter does include the count of all fields of a LAPF frame (including the Ethernet MAC frame). |
| 0x1fc92 0x1ff12 0x10112 0x10512 0x10912 0x10d12 0x11112 0x11512 | 15-0 | rpcTLAPFBYTEx_MSB | 0x0000 | Tx LAPF: LAPF byte counter for MAC0-7 - MSB This counter does not include the count of Host inserted LAPF LMI frames. This counter does include the count of all fields of a LAPF frame (including the Ethernet MAC frame). |

Table 43: Encapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|--------------------|--------|---|
| 0x1fc94 0x1ff14 0x10114 0x10514 0x10914 0x10d14 0x11114 0x11514 | 15-0 | rpcTLAPFFRAMEx_LSB | 0x0000 | Tx LAPF: LAPF frame counter for MAC0-7 - LSB Counts the total number of LAPF frames transmitted to SONET/SDH. This counter does not include the count of Host inserted LAPF LMI frames. |
| 0x1fc96 0x1ff16 0x10116 0x10516 0x10916 0x10d16 0x11116 0x11516 | 15-0 | rpcTLAPFFRAMEx_MSB | 0x0000 | Tx LAPF: LAPF frame counter for MAC0-7 - MSB This counter does not include the count of Host inserted LAPF LMI frames. |
| 0x1fc98 0x1ff18 0x10118 0x10518 0x10918 0x10d18 0x11118 0x11518 | 15-0 | rpcTPPBYTEx_LSB | 0x0000 | Tx PPP: PPP byte counter for MAC0-7 - LSB Counts the total number of bytes in PPP frame payloads transmitted to SONET/SDH. This counter does not include the count of Host inserted PPP LCP/NCP-BCP frames. This counter does include the count of all fields of a PPP frame (including the Ethernet MAC frame). |
| 0x1fc9a 0x1ff1a 0x1011a 0x1051a 0x1091a 0x10d1a 0x1111a 0x1151a | 15-0 | rpcTPPBYTEx_MSB | 0x0000 | Tx PPP: PPP byte counter for MAC0-7 - MSB This counter does not include the count of Host inserted PPP LCP/NCP-BCP frames. This counter does include the count of all fields of a PPP frame (including the Ethernet MAC frame). |
| 0x1fc9c 0x1ff1c 0x1011c 0x1051c 0x1091c 0x10d1c 0x1111c 0x1151c | 15-0 | rpcTPPFRAMEx_LSB | 0x0000 | Tx PPP: PPP frame counter for MAC0-7 - LSB Counts the total number of PPP frames transmitted to SONET/SDH. This counter does not include the count of Host inserted PPP LCP/NCP-BCP frames. |
| 0x1fc9e 0x1ff1e 0x1011e 0x1051e 0x1091e 0x10d1e 0x1111e 0x1151e | 15-0 | rpcTPPFRAMEx_MSB | 0x0000 | Tx PPP: PPP frame counter for MAC0-7 - MSB This counter does not include the count of Host inserted PPP LCP/NCP-BCP frames. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 44: Encapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|--|
| 0x1fdb8 0x1ffa0 0x101a0 0x105a0 0x109a0 0x10da0 0x111a0 0x115a0 | 0 | aTGFP CSFx | 0x0000 | Tx GFP: CSF indication alarm for MAC0-7 1: CSF frame mode is enabled. (i.e., While cTGFP TXCSFx=1, this alarm is constantly set. It does not clear while IDLE frames are transmit in between the CSF frames.) 0: on expiry of 100 ms period |
| | 1 | aTGFP MERRx | | Tx GFP: Incomplete Ethernet frame alarm for MAC0-7 1: While in the middle of an Ethernet frame transmission, no further bytes of that frame are available. 0: Follow-on frame is complete and correct. Note: The alarm will typically occur when a TXFIFO overflow occurs and control bit cTRSTRAM=1. |
| | 2 | aTGFP MAXERx | | Tx GFP: Max frame length error MAC0-7 1: frame length is higher than rTMAXFLx(15:0) register 0: after next correct frame (less than the limit) |
| | 3 | aTLFFERRx | | Tx LAFP: FIFO error for MAC0-7 1: underflow/overflow of the TX FIFO during middle of transfer 0: on TX FIFO reset after the alarm entry |
| | 4 | aTLF MAXERx | | Tx LAFP: Max frame length error for MAC0-7 1: frame length is higher than rTMAXFLx(15:0) register 0: after next correct frame (less than the limit) |
| | 5 | aTLPFERRx | | Tx LAPS: FIFO error alarm for MAC0-7 1: underflow/overflow of the TX FIFO during middle of transfer 0: on TX FIFO reset after the alarm entry |
| | 6 | aTMAXERx | | Tx LAPS: Max frame length error for MAC0-7 1: frame length is higher than rTMAXFLx(15:0) register 0: after next correct frame (less than the limit) |
| | 7 | aTPPFERRx | | Tx PPP: FIFO error for MAC0-7 1: underflow/overflow of the TX FIFO during middle of transfer 0: on TX FIFO reset after the alarm entry |
| | 8 | aTPP MAXERx | | Tx PPP: Max frame length error for MAC0-7 1: frame length is higher than rTMAXFLx(15:0) register 0: after next correct frame (less than the limit) |
| | 9 | aTPPMPVDROPx | | Tx PPP: Padding error for MAC0-7 1: number of padding bytes exceeds the value in the rTBCPPDMPV(7:4) register 0: after next correct frame |
| | 10 | aTCTLXx | | Tx LAPS/LAFP/GFP/PPP: Control Frame buffer empty alarm for MAC0-7 1: Control Frame buffer is empty 0: Control Frame buffer is full |
| | 11 | COUNT_ENCx | | Count status Bit (Perf Mon counter is saturated) for MAC0-7 1: when any of the performance counters of each encapsulation block (associated to each MAC) has reached its maximum value in the saturating mode only 0: after being read by the microprocessor |

Table 45: Encapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------------------|--------|--|
| 0x1fdc0 0x1ffa8 0x101a8 0x105a8 0x109a8 0x10da8 0x111a8 0x115a8 | 0 | MaTGFP CSFx | 0x07FF | Tx GFP: CSF indication alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 1 | MaTGFP MERRx | | Tx GFP: Incomplete Ethernet frame alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 2 | MaTGFP MAXERx | | Tx GFP: Max frame length error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 3 | MaTLFFERRx | | Tx LAFP: FIFO error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 4 | MaTLF MAXERx | | Tx LAFP: Max frame length error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 5 | MaTLPFERRx | | Tx LAPS: FIFO error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 6 | MaTMAXERx | | Tx LAPS: Max frame length error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 7 | MaTPPFERRx | | Tx PPP: FIFO error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 8 | MaTPP MAXERx | | Tx PPP: Max frame length error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 9 | MaTPP MPVDROPx | | Tx PPP: Padding error alarm mask for MAC0-7 1: masked (default) 0: not masked |
| | 10 | MaTCTLXx | | Tx LAPS/LAFP/GFP/PPP: Control Frame buffer empty alarm mask for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdc2 | 7-0 | MaENCx_Lapf_Interrupt | 0x00FF | Tx LAFP: Mask interrupt for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdc4 | 7-0 | MaENCx_Laps_Interrupt | 0x00FF | Tx LAPS: Mask interrupt for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdc6 | 7-0 | MaENCx_Gfp_Interrupt | 0x00FF | Tx GFP: Mask interrupt for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdc8 | 7-0 | MaENCx_Ppp_Interrupt | 0x00FF | Tx PPP: Mask interrupt for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdca | 7-0 | MaENCx_Ctl_Interrupt | 0x00FF | Tx CTL: Mask interrupt for MAC0-7 1: masked (default) 0: not masked |
| 0x1fdcc | 0 | MaGlobalTxLapf | 0x0001 | Tx LAFP: Global interrupt mask 1: interrupt for LAFP alarms for all MAC is masked (default) 0: interrupt for LAFP alarms for all MAC is not masked |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 45: Encapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------------------|--------|--|
| 0x1fdce | 0 | MaGlobalTxLaps | 0x0001 | Tx LAPS: Global interrupt mask 1: interrupt for LAPS alarms for all MAC is masked (default) 0: interrupt for LAPS alarms for all MAC is not masked |
| 0x1fdd0 | 0 | MaGlobalTxGfp | 0x0001 | Tx GFP: Global interrupt mask 1: interrupt for GFP alarms for all MAC is masked (default) 0: interrupt for GFP alarms for all MAC is not masked |
| 0x1fdd2 | 0 | MaGlobalTxPpp | 0x0001 | Tx PPP: Global interrupt mask 1: interrupt for PPP alarms for all MAC is masked (default) 0: interrupt for PPP alarms for all MAC is not masked |
| 0x1fdd4 | 0 | MaGlobalTxCTL | 0x0001 | Tx CTL: global interrupt mask 1: interrupt for CTL alarms for all MAC is masked (default) 0: interrupt for CTL alarms for all MAC is not masked |
| 0x1fdd6 | 0 | MaENCAP_20M_Interrupt | 0x0001 | Tx: Global interrupt mask 1: interrupt for all alarms for all MAC is masked (default) 0: interrupt for all alarms for all MAC is not masked |
| 0x1fdd8 0x1fdda 0x1fddc 0x1fdde 0x1fde0 0x1fde2 0x1fde4 0x1fde6 | 0 | MCOUNT_ENCx | 0x0001 | Count status Bit mask for MAC0-7 1: Count status bit for each MAC is masked (default) 0: Count status for each MAC is not masked |
| 0x1fde8 | 0 | MCOUNT_ENC_20M | 0x0001 | Global count status Bit mask 1: Global count status bit for all MAC is masked (default) 0: Global count status for all MAC is not masked |

Table 46: Encapsulation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------------------|--------|--|
| 0x1fc40 0x1ff60 0x10160 0x10560 0x10960 0x10d60 0x11160 0x11560 | 0 | Encapx_Lapf_Interrupt | 0x0000 | Transmit LAPF alarm interrupt for MAC0-7 1: interrupt for all LAPF alarms for each MAC 0: no interrupt |
| 0x1fc42 0x1ff62 0x10162 0x10562 0x10962 0x10d62 0x11162 0x11562 | 0 | Encapx_Laps_Interrupt | 0x0000 | Transmit LAPS alarm interrupt for MAC0-7 1: interrupt for all LAPS alarms for each MAC 0: no interrupt |
| 0x1fc44 0x1ff64 0x10164 0x10564 0x10964 0x10d64 0x11164 0x11564 | 0 | Encapx_Gfp_Interrupt | 0x0000 | Transmit GFP alarm interrupt for MAC0-7 1: interrupt for all GFP alarms for each MAC 0: no interrupt |

Table 46: Encapsulation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|------------------------|--------|---|
| 0x1fc46 0x1ff66 0x10166 0x10566 0x10966 0x10d66 0x11166 0x11566 | 0 | Encapx_Ppp_Interrupt | 0x0000 | Transmit PPP alarm interrupt for MAC0-7 1: interrupt for all PPP alarms for each MAC 0: no interrupt |
| 0x1fc48 0x1ff68 0x10168 0x10568 0x10968 0x10d68 0x11168 0x11568 | 0 | Encapx_Ctl_Interrupt | 0x0000 | Transmit CTL alarm interrupt for MAC0-7 1: interrupt for all CTL alarms for each MAC 0: no interrupt |
| 0x1fc4a | 0 | TxLapf_Interrupt | 0x0000 | Global transmit LAPF alarm interrupt 1: interrupt for all LAPF alarms for all MAC 0: no interrupt |
| 0x1fc4c | 0 | TxLaps_Interrupt | 0x0000 | Global transmit LAPS alarm interrupt 1: interrupt for all LAPS alarms for all MAC 0: no interrupt |
| 0x1fc4e | 0 | TxGfp_Interrupt | 0x0000 | Global transmit GFP alarm interrupt 1: interrupt for all GFP alarms for all MAC 0: no interrupt |
| 0x1fc50 | 0 | TxPpp_Interrupt | 0x0000 | Global transmit PPP alarm interrupt 1: interrupt for all PPP alarms for all MAC 0: no interrupt |
| 0x1fc52 | 0 | TxCtl_Interrupt | 0x0000 | Global transmit CTL alarm interrupt 1: interrupt for all CTL alarms for all MAC 0: no interrupt |
| 0x1fc54 | 0 | COUNT_Interrupt | 0x0000 | Global Transmit Latched count status bit interrupt 1: interrupt for all latched count status bits 0: no interrupt |
| 0x1fc56 | 0 | ENCAP_20M_Interrupt | 0x0000 | Global transmit encapsulation alarm interrupt 1: interrupt for all alarms for all MAC before mask 0: no interrupt |
| 0x1fc58 | 0 | ENCAP_Global_Interrupt | 0x0000 | Global masked transmit encapsulation alarm interrupt 1: interrupt for all alarms for all MAC after mask 0: no interrupt |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 47: Encapsulation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|----------------|--------|---|
| 0x1fdbc 0x1ffc0 0x101c0 0x105c0 0x109c0 0x10dc0 0x111c0 0x115c0 | 0 | L1aTGFPFSFx | 0x0000 | Tx GFP: Latched CSF indication alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aTGFPFMERRx | | Tx GFP: Latched incomplete Ethernet frame alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aTGFPMAXERx | | Tx GFP: Latched max frame length error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aTLFFERRx | | Tx LAPF: Latched FIFO error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aTLFMAXERx | | Tx LAPF: Latched max frame length error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aTLPFERRx | | Tx LAPS: Latched FIFO error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 6 | L1aTMAXERx | | Tx LAPS: Latched max frame length error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 7 | L1aTPPFERRx | | Tx PPP: Latched FIFO error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 8 | L1aTPPMAXERx | | Tx PPP: Latched max frame length error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 9 | L1aTPPMPVDROPx | | Tx PPP: Latched padding error for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 10 | L1aTCTLXx | | Tx LAPS/LAPF/GFP/PPP: Latched Control Frame buffer empty alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 11 | LCOUNT_ENCx | | Transmit Latched count status bit alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |

RX DECAPSULATION REGISTERS

Tables 48 through 61 - Configuration, Status and Alarms of the Decapsulation Block

Table 48: Decapsulation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|---|
| 0x1eac0 0x11980 0x11d80 0x12180 0x12580 0x12980 0x12d80 0x13180 | 1-0 | cRDECAPx | 0x0000 | Receive side Decapsulation mode selection for MAC0-7 00: see cRHDLcX bit below 01: LAPF 10: GFP 11: Disabled (i.e., no decapsulation is used and block is not used). |
| 0x1eac2 0x11982 0x11d82 0x12182 0x12582 0x12982 0x12d82 0x13182 | 0 | cRFCMODEx | 0x0000 | SONET-to-Ethernet direction: Handling of PAUSE received from SONET/SDH side for MACs 0-7 0: PAUSE frames received from SONET/SDH are discarded. (Default) 1: PAUSE frames received from SONET/SDH are not discarded and passed onto the Ethernet line side. |
| 0x1eac4 0x11984 0x11d84 0x12184 0x12584 0x12984 0x12d84 0x13184 | 0 | cRHDLcX | 0x0000 | Rx HDLC encapsulation mode for MAC0-7 Effective only when cRDECAPx = 00. 0: LAPS (default) 1: PPP |
| 0x1eac6 0x11986 0x11d86 0x12186 0x12586 0x12986 0x12d86 0x13186 | 0 | cRCTLBRSTx | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Control frame buffer reset for MAC0-7 0: reset is not active 1: reset is active |
| 0x1eaca 0x1198a 0x11d8a 0x1218a 0x1258a 0x1298a 0x12d8a 0x1318a | 0 | cRFCSSWAPINx | 0x0000 | 0: data provided as protocol stated 1: data swapped (MSB<-> LSB of the protocol) |
| 0x1eacc | 1-0 | cINRT_GRPOL | 0x0001 | Alarm latching configuration for the HOL alarm group (Table 58) Criteria used to create latched alarms from the raw (unlatched) alarms. 00: positive level 01: rising edge 10: falling edge 11: rising or falling edge |



Table 48: Decapsulation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|--------------|--------|--|
| 0x1eace 0x1198c 0x11d8c 0x1218c 0x1258c 0x1298c 0x12d8c 0x1318c | 15-0 | rRMAXFLx | 0x0640 | Rx LAPS/LAPF/GFP/PPP: Max frame length for MAC0-7 Configures the maximum number of bytes per frame, including the FCS bytes, that will be accepted by a MAC. Frames which exceed this length are discarded and corresponding alarms and counters are triggered Default is 0x640 (decimal 1600). |
| 0x1ead0 0x1198e 0x11d8e 0x1218e 0x1258e 0x1298e 0x12d8e 0x1318e | 15-0 | rRCTRLMASKAx | 0xFFFF | mask for filtering LAPS, GFP and PPP LCP/Control frames for channel x LAPS: Mask (per bit basis) in addition to the rSAPFDx register to check the SAPI field. GFP: Mask (per bit basis) in addition to the rRGFPCPx register to check the PTI, PFI, EXI and UPI fields PPP: Mask (per bit basis) in addition to the comparison with 0xC021 to detect the LCP control frame. 1: Mask is not active 0: Mask is active |
| 0x1ead2 0x11990 0x11d90 0x12190 0x12590 0x12990 0x12d90 0x13190 | 15-0 | rRCTRLMASKBx | 0xFFFF | mask for filtering PPP NCP/control frames for channel x Mask (per bit basis) in addition to the comparison with 0x8031 to detect the NCP control frame. 1: Mask is not active 0: Mask is active |

Table 49: Decapsulation Block - LAPS Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|------------|--------|--|
| 0x1ebf0 0x11870 0x11c70 0x12070 0x12470 0x12870 0x12c70 0x13070 | 0 | cRSCRDx | 0x022C | Rx LAPS: Descrambling control for MAC0-7 0: Enable descrambling. (Default) 1: Disable descrambling. |
| | 1 | cRFLAGx | | Rx LAPS: Flag detection for MAC0-7 0: At least two flags to be detected between two consecutive LAPS frames. (Default) 1: At least a single flag to be detected between two consecutive LAPS frames (i.e., shared flag detection). |
| | 2 | cRFCSx | | Rx LAPS: FCS enable for MAC0-7 0: FCS checking disabled (assume no FCS octets are present) 1: FCS checking enabled. (Default) |
| | 4-3 | cRACSELx | | Rx LAPS: ADDRESS and CONTROL checking for MAC0-7 00: ADDRESS and CONTROL field contents checking is disabled 01: ADDRESS and CONTROL field contents checking with fixed values. ADDRESS field content is always checked against 0x04 and CONTROL field content is always checked against 0x03. (Default) 10: Reserved 11: ADDRESS and CONTROL field contents checked against the rRACFDx register. |
| | 5 | cRSAPIx | | Rx LAPS: SAPI checking for MAC0-7 0: SAPI field contents checking is disabled 1: SAPI field contents checked against the rRSAPFDx register. (Default) |
| | 6 | cRMMAEx | | Rx LAPS: ADDRESS, CONTROL or SAPI mismatch for MAC0-7 0: LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is discarded. (Default) 1: LAPS frame with mismatched ADDRESS or CONTROL or SAPI field contents is not discarded. |
| | 7 | cRLPABTGx | | Rx LAPS: Receive Frame abort control for MAC0-7 0: No action. (Default) 1: Current frame being received is aborted. |
| | 8 | cRLPFCSErx | | Rx LAPS: FCS discard control for MAC0-7 To be used only when FCS checking is enabled as per cRFCSx register. 0: received LAPS framed with FCS errors are discarded (default) 1: received LAPS frames with FCS errors are NOT discarded |
| | 9 | cRLPPDUx | | Rx LAPS: Decapsulation disable for MAC0-7 0: decapsulation of LAPS frames enabled 1: disabled except for Control frames |
| 0x1ebf2 0x11872 0x11c72 0x12072 0x12472 0x12872 0x12c72 0x13072 | 7-0 | rRLPMINFLx | 0x0006 | Rx LAPS: Min LAPS frame size received for MAC0-7 0x06 - 0xFF: Minimum number of octets in a received LAPS frame between the opening and closing flags. For LAPS frames received with less than six octets, an alarm aRLPSSHTERx is generated. Decapsulated frames that are less than 5 bytes won't pass through the MAC. |
| 0x1ebf4 0x11874 0x11c74 0x12074 0x12474 0x12874 0x12c74 0x13074 | 15-0 | rRACFDx | 0x0403 | Rx LAPS: ADDRESS and CONTROL field contents for MAC0-7 Upper byte (Bits 15-8) = Content of the ADDRESS field. Default is 0x04. Lower byte (Bits 7-0) = Content of the CONTROL field. Default is 0x03. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 49: Decapsulation Block - LAPS Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------|--------|---|
| 0x1ebf6 0x11876 0x11c76 0x12076 0x12476 0x12876 0x12c76 0x13076 | 15-0 | rRSAPFDx | 0xFE01 | Rx LAPS: SAPI field contents for MAC0-7 Upper byte (Bits 15-8) = Content of the first SAPI octet field. Default is 0xFE. Lower byte (Bits 7-0) = Content of the second SAPI octet field. Default is 0x01. |
| 0x1ebf8 0x11878 0x11c78 0x12078 0x12478 0x12878 0x12c78 0x13078 | 15-0 | rRLPCPx | 0x0000 | Rx LAPS: LAPS control frame filter Only LAPS control frames with SAPI Protocol field values matching this register are sent to the host. |

Table 50: Decapsulation Block - LAPF Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|---------------|--------|--|
| 0x1ea80 0x119a0 0x11da0 0x121a0 0x125a0 0x129a0 0x12da0 0x131a0 | 0 | cRLFFLAGx | 0x00A0 | Rx LAPF: Flag detection for MAC0-7 0: At least two flags to be detected between two consecutive LAPF frames. (Default) 1: At least a single flag to be detected between two consecutive LAPF frames (i.e., shared flag detection). |
| | 1 | cRLFACNOPSELx | | Rx LAPF: ADDRESS and CONTROL and OUI and NLPID and PID field contents checking control for MAC0-7 0: ADDRESS and CONTROL and OUI and NLPID and PID field contents checking enabled. (Default) ADDRESS field contents are checked against rRLFADRx CONTROL field contents are checked against rRLFCNTLx OUI field contents are checked against rROUIx NLPID field contents are checked against rRNLPIDx PID field contents are checked against rRPIDx 1: ADDRESS and CONTROL and OUI and NLPID and PID field contents checking disabled. |
| | 2 | cRLMIDLCIx | | Rx LAPF: LMI frame DLCI value selection for MAC0-7 0: DLCI = 0 to be checked to filter LMI frame. (Default) 1: DLCI = 1023 to be checked to filter LMI frame. |
| | 3 | cRLFPADx | | Rx LAPF: LAPF PAD contents checking for MAC0-7 0: LAPF PAD field contents checked against the rRPADx register. (Default) 1: LAPF PAD field contents checking is disabled. |
| | 4 | cRLFMMAEx | | Rx LAPF: ADDRESS or CONTROL or OUI or NLPID or PID or PAD field contents mismatch discard frame control for MAC0-7 0: LAPF frame with mismatched ADDRESS or CONTROL or OUI or NLPID or PID or PAD field contents is discarded. 1: LAPF frame with mismatched ADDRESS or CONTROL or OUI or NLPID or PID or PAD field contents is not discarded. (Default) |
| | 5 | cRLFFCSx | | Rx LAPF: FCS enable for MAC0-7 0: LAPF FCS checking disabled and assume the two FCS field octets are not present. (Default) 1: LAPF FCS checking enabled. |
| | 6 | cRLFFCSERx | | Rx LAPF: FCS discard for MAC0-7 0: Received LAPF frames with FCS error are discarded. 1: Received LAPF frames with FCS error are not discarded. (Default) |
| | 7 | cRLFPDUx | | Rx LAPF: LAPF frame types for MAC0-7 0: All LAPF frame types received frames from SONET/SDH are allowed to be decapsulated. 1: Only LAPF LMI frames matching the cRLMIDLCIx register are allowed to be decapsulated. (Default) |
| 0x1ea82 0x119a2 0x11da2 0x121a2 0x125a2 0x129a2 0x12da2 0x131a2 | 7-0 | rRLFMINFLx | 0x0003 | Rx LAPF: Min. LAPF frame size received for MAC0-7 0x03 - 0xFF: Minimum number of octets in a received LAPF frame between the ADDRESS field and closing flag. For LAPF frames received with less than three octets, an alarm aRLFSSERx is generated. Decapsulated frames that are less than 5 bytes won't pass through the MAC. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 50: Decapsulation Block - LAMP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------|--------|--|
| 0x1ea84 0x119a4 0x11da4 0x121a4 0x125a4 0x129a4 0x12da4 0x131a4 | 15-0 | rRLFADRx | 0x0401 | Rx LAMP: ADDRESS field contents for MAC0-7 Upper byte (bits 15-8) = Contents of the Upper DLCI (bits 15-10) and C/R (bit 9) and EA (bit 8) fields. Default set to 0x04. Lower Byte (bits 7-0) = Contents of the Lower DLCI (bits 7-4) and FECN (bit 3) and BECN (bit 2) and DE (bit 1) and EA (bit 0) fields. Default set to 0x01. |
| 0x1ea86 0x119a6 0x11da6 0x121a6 0x125a6 0x129a6 0x12da6 0x131a6 | 7-0 | rRLFCNTLx | 0x0003 | Rx LAMP: CONTROL field contents for MAC0-7 Range 0x00-0xFF: Indicates CONTROL field contents when checking is enabled. Default set to 0x03. |
| 0x1ea88 0x119a8 0x11da8 0x121a8 0x125a8 0x129a8 0x12da8 0x131a8 | 7-0 | rRPADx | 0x0000 | Rx LAMP: PAD field contents for MAC0-7 Range 0x00-0xFF: Indicates PAD field contents when checking is enabled. Default set to 0x00. |
| 0x1ea8a 0x119aa 0x11daa 0x121aa 0x125aa 0x129aa 0x12daa 0x131aa | 7-0 | rRNLPIDx | 0x0080 | Rx LAMP: NLPID field contents for MAC0-7 Range 0x00-0xFF: Indicates NLPID field contents when checking is enabled. Default set to 0x80. |
| 0x1ea8c 0x119ac 0x11dac 0x121ac 0x125ac 0x129ac 0x12dac 0x131ac | 7-0 | rROUIx(1) | 0x0000 | Rx LAMP: OUI field contents (MSB bits) for MAC0-7 Range 0x00-0xFF: Indicates OUI field (MSB bits) contents when checking is enabled. Default set to 0x00. |
| 0x1ea8e 0x119ae 0x11dae 0x121ae 0x125ae 0x129ae 0x12dae 0x131ae | 15-0 | rROUIx(0) | 0x80C2 | Rx LAMP: OUI field contents (LSB bits) for MAC0-7 Range 0x0000-0xFFFF: Indicates OUI field (LSB bits) contents when checking is enabled. Default set to 0x80C2. |
| 0x1ea90 0x119b0 0x11db0 0x121b0 0x125b0 0x129b0 0x12db0 0x131b0 | 15-0 | rRPIDx | 0x0007 | Rx LAMP: PID field contents for MAC0-7 Upper byte (bits 15-8) = Contents of the first PID octet field. Default set to 0x00. Lower Byte (bits 7-0) = Contents of the second PID octet field. Default set to 0x07. |

Table 51: Decapsulation Block - Control Buffer Status (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------|--------|---|
| 0x1ebe0 0x11860 0x11c60 0x12060 0x12460 0x12860 0x12c60 0x13060 | 0 | sRCTLBx | 0x0000 | Rx LAPF/LAPS/PPP/GFP: Control buffer full for MAC0-7 0: Control buffer is empty (Host read access is disabled) 1: Control buffer contains a single complete Control frame (Host read access is enabled). Once the Control frame is read, the Host needs to clear this bit in order to detect the arrival of another LMI frame. |

Table 52: Decapsulation Block - Link Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------|--------|---|
| 0x1ebe8 0x11868 0x11c68 0x12068 0x12468 0x12868 0x12c68 0x13068 | 0 | sLNKSTSx | 0x0000 | Rx LAPF: Link status for MAC0-7 0: LAPF link is DOWN. (Default) 1: LAPF link is UP. |
| | 1 | Reserved | | Reserved |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 53: Decapsulation Block - GFP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-------------|--------|---|
| 0x1eb40 0x119f0 0x11df0 0x121f0 0x125f0 0x129f0 0x12df0 0x131f0 | 0 | cRCDSCRx | 0x0800 | Rx GFP: Core header descrambling disable for MAC0-7 0: Enable descrambling of GFP Core header only. (Default) 1: Disable descrambling of GFP Core header only. |
| | 1 | cRCORDISx | | Rx GFP: Core header single-bit error correction control for MAC0-7 0: Enable Single bit error correction and all frames with single bit error corrected are passed. Frames with multiple-bit errors are discarded. (Default) 1: Disable Single bit error correction. All frames with errors are discarded. |
| | 2 | cRTHECSx | | Rx GFP: Type header single-bit error correction control for MAC0-7 0: Enable single bit error correction and all frames with single bit error corrected are passed. Frames with multiple-bit errors are discarded. (Default) 1: Disable single bit error correction. All frames with errors are discarded. |
| | 3 | cREHECSx | | Rx GFP: Extension header single-bit error correction control for MAC0-7 0: Enable single bit error correction and all frames with single bit error corrected are passed. Frames with multiple-bit errors are discarded. (Default) 1: Disable single bit error correction. All frames with errors are discarded. |
| | 4 | cRPSCRDX | | Rx GFP: Payload Area descrambling control for MAC0-7 0: Enable descrambling of GFP Payload area only. (Default) 1: Disable descrambling of GFP Payload area only. |
| | 7-5 | cRDELTAx | | Rx GFP: Re-synchronization control for MAC0-7 0x0-0x7: Indicates values of DELTA to be used in the GFP delineation process. (Default=0x1) |
| | 8 | cRGFPABTGx | | Rx GFP: Receive Frame abort control for MAC0-7 0: No action. (Default) 1: Current frame being received is aborted. |
| | 9 | cRGFPFCSErx | | Rx GFP: FCS discard for MAC0-7 0: Received GFP frames with FCS error are discarded. (Default) 1: Received GFP frames with FCS error are not discarded. |
| | 10 | cRGFPHDRx | | Rx GFP: NULL/LINEAR header processing control for MAC0-7 0: Only NULL extension header frame are processed. Other frame types are discarded. (Default) 1: Only LINEAR extension header frame are processed. Other frame types are discarded |
| | 11 | cRGFPDU0 | | Rx GFP: Decapsulation disable for MAC0-7 0: decapsulation of frames enabled 1: disabled except for Control frames |
| 0x1eb42 0x119f2 0x11df2 0x121f2 0x125f2 0x129f2 0x12df2 0x131f2 | 7-0 | cRGFPCIDx0 | 0x0000 | Rx GFP: CID value 0 for VCG0-7 0x00-0xFF: CID value #0 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID field value. |
| | 15-8 | cRGFPCIDx1 | | Rx GFP: CID value 1 for VCG0-7 0x00-0xFF: CID value #1 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. |
| 0x1eb44 0x119f4 0x11df4 0x121f4 0x125f4 0x129f4 0x12df4 0x131f4 | 7-0 | cRGFPCIDx2 | 0x0000 | Rx GFP: CID value 2 for VCG0-7 0x00-0xFF: CID value #2 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. |
| | 15-8 | cRGFPCIDx3 | | Rx GFP: CID value 3 for VCG0-7 0x00-0xFF: CID value #3 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. |

Table 53: Decapsulation Block - GFP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|---------------------|----------------------------------|--------|--|
| 0x1eb46 0x119f6 0x11df6 0x121f6 0x125f6 0x129f6 0x12df6 0x131f6 | 7-0 15-8 | cRGFPCIDx4 cRGFPCIDx5 | 0x0000 | Rx GFP: CID value 4 for VCG0-7 0x00-0xFF: CID value #4 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. Rx GFP: CID value 5 for VCG0-7 0x00-0xFF: CID value #5 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. |
| 0x1eb48 0x119f8 0x11df8 0x121f8 0x125f8 0x129f8 0x12df8 0x131f8 | 7-0 15-8 | cRGFPCIDx6 cRGFPCIDx7 | 0x0000 | Rx GFP: CID value 6 for VCG0-7 0x00-0xFF: CID value #6 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. Rx GFP: CID value 7 for VCG0-7 0x00-0xFF: CID value #7 (among the list of allowed eight CID values) per VCG to be compared with the actual received CID value. |
| 0x1eb4a 0x119fa 0x11dfa 0x121fa 0x125fa 0x129fa 0x12dfa 0x131fa | 7-0 | cLECIDx | 0x00FF | Rx GFP: Local-end CID field configuration for MAC0-7 0x00-0xFF: Indicates a unique local-end CID value assigned to a local MAC port. (Default=0x00) |
| 0x1eb4c 0x119fc 0x11dfc 0x121fc 0x125fc 0x129fc 0x12dfc 0x131fc | 15-0 | rRGFPCPx | 0x8000 | Rx GFP: Control frame filter GFP Client Management/Control Frames with Type field values matching this register are forwarded to the host. Default is 0x9000. bits 15-13: PTI field bit 12: PFI field bits 11-8: EXI field bits 7-0: UPI field |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 54: Decapsulation Block - PPP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|--|
| 0x1eba0 0x11840 0x11c40 0x12040 0x12440 0x12840 0x12c40 0x13040 | 0 | cRPACMMAEEx | 0x48B2 | Rx PPP: ADDRESS and CONTROL discard control for MAC0-7 0: discard PPP frames with mismatched ADDRESS or CONTROL fields (default) 1: NO discard of mismatched frames |
| | 2-1 | cRPACSELx | | Rx PPP: ADDRESS and CONTROL checking for MAC0-7 00: ADDRESS and CONTROL field contents checking is disabled 01: ADDRESS and CONTROL field contents checking with fixed values. ADDRESS field content is always checked against 0xFF and CONTROL field content is always checked against 0x03. (Default) 10: Reserved 11: ADDRESS and CONTROL field contents checked against the rRPACFDx register. |
| | 3 | cRPCRCSx | | Rx PPP: FCS algorithm for MAC0-7 0: CRC-32 (default) 1: CRC-16 |
| | 4 | cRPFCSx | | Rx PPP: FCS enable for MAC0-7 0: FCS checking disabled (assume no FCS octets are present) 1: FCS checking enabled (default) |
| | 5 | cRPFGx | | Rx PPP: Flag field matching for MAC0-7 0: disabled 1: BCP Flag fields are matched against the rRPFGFDx register (default) |
| | 6 | cRPFGMAEEx | | Rx PPP: Flag field discard control for MAC0-7 0: discard PPP frames with mismatched Flag fields (default) 1: NO discard of mismatched frames |
| | 7 | cRPMACx | | Rx PPP: Type field matching for MAC0-7 0: disabled 1: BCP Type fields are matched against the rRPMACFDx register (default) |
| | 8 | cRPMACMAEEx | | Rx PPP: Type field discard control for MAC0-7 0: discard PPP frames with mismatched Type fields (default) 1: NO discard of mismatched frames |
| | 9 | cRPPPABTGx | | Rx PPP: Receive Frame abort control for MAC0-7 0: No action. (Default) 1: Current frame being received is aborted. |
| | 10 | cRPPPCSERx | | Rx PPP: FCS discard for MAC0-7 0: Received PPP frames with FCS error are discarded. (default) 1: Received PPP frames with FCS error are not discarded. |
| | 11 | cRPPROTx | | Rx PPP: Protocol field matching for MAC0-7 0: disabled 1: Protocol fields are matched against the rRPPROTFDx register (default) |
| | 12 | cRPPROTMAEEx | | Rx PPP: Protocol Field discard control for MAC0-7 0: discard PPP frames with mismatched Protocol fields (default) 1: NO discard of mismatched frames |
| | 13 | cRBCPPDMODEx | | Rx PPP: Padding mode for PPP/BCP frames for MAC0-7 0: disabled (default) 1: Fixed padding mode is used |
| | 14 | cRBPDUX | | Rx PPP: Frame decapsulation enable for MAC0-7 0: All PPP frames are decapsulated from the SONET/SDH stream. 1: PPP frames with protocol field = 0x0031 are NOT decapsulated. LCP/NCP-BCP frames for the host continue to be decapsulated (default). |

Table 54: Decapsulation Block - PPP Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|------------|--------|--|
| 0x1eba2 0x11842 0x11c42 0x12042 0x12442 0x12842 0x12c42 0x13042 | 15-0 | rRPACFDx | 0xFF03 | Rx PPP: ADDRESS and CONTROL values for MAC0-7 bits 15-8: ADDRESS field bits 7-0: CONTROL field |
| 0x1eba4 0x11844 0x11c44 0x12044 0x12444 0x12844 0x12c44 0x13044 | 3-0 | rRPFPGFDx | 0x000A | Rx PPP: BCP Flag field match register for MAC0-7 bit 3 is the expected F bit, bit 2 is the expected 0 bit, bit 1 is the expected Z bit, and bit 0 is the expected B bit. |
| 0x1eba6 0x11846 0x11c46 0x12046 0x12446 0x12846 0x12c46 0x13046 | 15-0 | rRPLCPx | 0xC021 | Rx PPP: LCP frame filter for MAC0-7 Only LCP Frames with PPP Protocol field values matching this register are forwarded to the host. Default is 0xC021. |
| 0x1eba8 0x11848 0x11c48 0x12048 0x12448 0x12848 0x12c48 0x13048 | 7-0 | rRPMACFDx | 0x0101 | Rx PPP: BCP Type field match register for MAC0-7 Rx GFP: GFP UPI field match register for MAC0-7 In GFP mode, client data frames with mismatched Type header UPI fields are discarded and the RGFPeERRx alarm is asserted. |
| 0x1ebaa 0x1184a 0x11c4a 0x1204a 0x1244a 0x1284a 0x12c4a 0x1304a | 15-0 | rRPNCPx | 0x8031 | Rx PPP: NCP-BCP frame filter for MAC0-7 Only NCP-BCP Frames with PPP Protocol field values matching this register are forwarded to the host. Default is 0x8031. |
| 0x1ebac 0x1184c 0x11c4c 0x1204c 0x1244c 0x1284c 0x12c4c 0x1304c | 7-0 | rRPPMINFLx | 0x0006 | Rx PPP: min frame length for MAC0-7 Indicates the minimum number of octets that must be present in a received frame (between two flags). Frames smaller than this length but greater than 4 (16-bit FCS) or 6 (32-bit FCS) are not discarded, but trigger appropriate alarms and counters. Default is 0x04 for 16-bit FCS, 0x06 for 32-bit FCS. |
| 0x1ebae 0x1184e 0x11c4e 0x1204e 0x1244e 0x1284e 0x12c4e 0x1304e | 15-0 | rRPPROTFDx | 0x0031 | Rx PPP: Protocol field match register for MAC0-7 bits 15-8: first octet of Protocol field bits 7-0: second octet of Protocol field |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 55: Decapsulation Block - LMI Buffers (RO)

| Address | Bit | HW Symbol | Init | Description |
|----------------------|-----|-------------|--------|--|
| 0x1e900 – 0x1e97e | 8-0 | rRLMlx_[64] | 0x0000 | Rx LAPF: LMI buffers 0 through 63 for MAC0-7 Note: Each Address Buffer Utilizes bits 8-0. Each MAC has 64 Bytes x 8 bits of storage for a single LAPF LMI frame. The MSB bit (bit 8), when set to '1' of each byte, indicates that this byte (bits 7-0) is part of the LAPF LMI frame. This holds true up to the first byte where the MSB bit (bit 8) is set to 0. All bytes after and including the byte with the MSB bit (bit 8) set to 0, should be ignored by the Host. |
| 0x11900 – 0x1197e | | | | |
| 0x11d00 – 0x11d7e | | | | |
| 0x12100 – 0x1217e | | | | |
| 0x12500 – 0x1257e | | | | |
| 0x12900 – 0x1297e | | | | |
| 0x12d00 – 0x12d7e | | | | |
| 0x13100 – 0x1317e | | | | |

Table 56: Decapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---|-----|-------------|--------|---|
| Note: the GFP decapsulation alarms are only updated when: 1) at least one tributary is assigned to the VCG, AND 2) None of the tributaries assigned to the VCG have SONET/SDH failures such as SSF, DEG, AIS, PLM, UNEQ or LOM. | | | | |
| 0x1ebc0 0x11800 0x11c00 | 0 | aLNKSTSDWNx | 0x0000 | Rx LAPF: link down alarm for MAC0-7 0: no alarm 1: detection of the transition from link up to link down |
| 0x12000 0x12400 0x12800 | 1 | aLNKSTSUPx | | Rx LAPF: link up alarm for MAC0-7 0: no alarm 1: detection of the transition from link down to link up |
| 0x12c00 0x13000 | 2 | aRLFABTDx | | Rx LAPF: abort indication for MAC0-7 0: no alarm. 1: detection of an aborted frame. Cleared on the next valid frame. |
| | 3 | aRLFFCERx | | Rx LAPF: FCS error for MAC0-7 0: no alarm 1: detection of a frame with FCS error. Cleared on the next valid frame |
| | 4 | aRLFFSERx | | Rx LAPF: frame size error for MAC0-7 0: no alarm 1: detection of a frame with length less than 3 bytes. Cleared on the next valid frame |
| | 5 | aRLFMAXERx | | Rx LAPF: max frame size error for MAC0-7 0: no alarm 1: detection of a frame with length higher than rRMAXFLx register |
| | 6 | aRLFMINERx | | Rx LAPF: min frame size error for MAC0-7 0: no alarm 1: detection of a frame with length lower than rRMINFLx register |
| | 7 | aRLFMMx | | Rx LAPF: frame mismatch error for MAC0-7 0: no alarm 1: detection of a frame with error on Address, Control, NLPID, OUI, PAD or PID field. Cleared on the next valid frame. |

Table 56: Decapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---|-----|-------------|--------|---|
| 0x1ebc2 0x11802 0x11c02 | 0 | aRLPSABTDx | 0x0000 | Rx LAPS: abort indication for MAC0-7 0: no alarm. 1: detection of an aborted frame. Cleared on the next valid frame. |
| 0x12002 0x12402 0x12802 0x12c02 0x13002 | 1 | aRLPSFCSErx | | Rx LAPS: FCS error for MAC0-7 0: no alarm 1: Detection of a LAPS frame with FCS error. Cleared on the next valid frame |
| | 2 | aRLPSFMMx | | Rx LAPS: frame mismatch error for MAC0-7 0: no alarm 1: detection of a frame with error on Address, Control or SAPI field. Cleared on the next valid frame. |
| | 3 | aRLPSMINERx | | Rx LAPS: min frame size error for MAC0-7 0: no alarm 1: detection of a frame with length lower than rRLPMINFLx register |
| | 4 | aRLPSSHTErx | | Rx LAPS: frame size error for MAC0-7 0: no alarm 1: detection of a frame with length less than 6 bytes. Cleared on the next valid frame |
| | 5 | aRLPSMAXERx | | Rx LAPS: max frame size error for MAC0-7 0: no alarm 1: detection of a frame with length higher than rRMAXFLx register |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 56: Decapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|----------------|--------|--|
| 0x1ebc4 0x11804 0x11c04 0x12004 0x12404 0x12804 0x12c04 0x13004 | 0 | aRGFPCIDERRx | 0x0000 | Rx GFP: frame CID error for MAC0-7 0: no alarm 1: detection of an unsupported value of CID. Cleared on the next valid frame with correct CID value or an IDLE frame. |
| | 1 | aRGFPEHECERRx | | Rx GFP: eHEC error for MAC0-7 0: no alarm 1: detection of a single bit error on the eHEC. Cleared on the reception of a frame with no error on eHEC or reception of an IDLE frame. |
| | 2 | aRGFPEXIERRx | | Rx GFP: EXI error for MAC0-7 0: no alarm 1: detection of a mismatch of the EXI value with the cRGFPHDRx register. Cleared on the next valid frame. |
| | 3 | aRGFFPCSERx | | Rx GFP: Payload area FCS error for MAC0-7 0: no alarm 1: detection of a frame with Payload FCS error. Cleared on the next valid frame. |
| | 4 | aRGFFFECSFx | | Rx GFP: Far end CSF indication for MAC0-7 0: no alarm 1: detection of a CSF indication. Cleared on receipt of the first valid GFP Client data frame, or after failing to receive 3 CSF indications in 3 seconds. |
| | 5 | aRGFPHUNTx | | Rx GFP: Hunt state alarm for MAC0-7 0: state machine is in a state different from HUNT 1: state machine is in a HUNT state |
| | 6 | aRGFPLOFx | | Rx GFP: loss of frame delineation alarm for MAC0-7 0: no alarm 1: while in SYNC state, when a core header with multiple-bit errors is detected or a single-bit error detected and transitions to the HUNT state. Cleared on entering in SYNC state |
| | 7 | aRGFPMAXERx | | Rx GFP: Max length error for MAC0-7 0: no alarm 1: detection of a frame with length higher than rRMAXFLx register |
| | 8 | aRGFPMCHECERRx | | Rx GFP: Multiple Bit error for MAC0-7 0: no alarm 1: detection of multiple-bit errors in the core header while in HUNT, PRE-SYNC or SYNC states. Cleared on reception of a frame without multiple-bit errors in the core header or reception of an IDLE frame. |
| | 9 | aRGFPPRESYNcx | | Rx GFP: PRESYNC state alarm for MAC0-7 0: state machine is in a state different from PRESYNC 1: state machine is in a PRESYNC state |
| | 10 | aRGFPPTIERRx | | Rx GFP: PTI error for MAC0-7 0: no alarm 1: detection of a received PTI value different from 000 or 100. Cleared on correct received PTI value or on reception of GFP IDLE frame. |
| | 11 | aRGFPSCHECERRx | | Rx GFP: single Bit error for MAC0-7 0: no alarm 1: while in SYNC state, when a core header with single-bit errors is detected while in HUNT or PRESYNC or SYNC states. Cleared on reception of no single-bit error frame or GFP IDLE frame reception |

Table 56: Decapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------------|--------|---|
| 0x1ebc4 0x11804 0x11c04 0x12004 0x12404 0x12804 0x12c04 0x13004 | 12 | aRGFPSYNcx | 0x0000 | Rx GFP: SYNC state alarm for MAC0-7 0: state machine is in a state different from SYNC 1: state machine is in a SYNC state |
| 0x12004 0x12404 | 13 | aRGFPTECERRx | | Rx GFP: Type header check error for MAC0-7 |
| 0x12804 0x12c04 0x13004 | 14 | aRGFPeERRx | | Rx GFP: UPI error for MAC0-7 |
| 0x1ebc6 0x11806 0x11c06 0x12006 0x12406 0x12806 0x12c06 0x13006 | 0 | aRGFPFECSFCIDx0 | 0x0000 | Rx GFP: Far end CSF indication 0 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #0 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| 0x12806 0x12c06 0x13006 | 1 | aRGFPFECSFCIDx1 | | Rx GFP: Far end CSF indication 1 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #1 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 2 | aRGFPFECSFCIDx2 | | Rx GFP: Far end CSF indication 2 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #2 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 3 | aRGFPFECSFCIDx3 | | Rx GFP: Far end CSF indication 3 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #3 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 4 | aRGFPFECSFCIDx4 | | Rx GFP: Far end CSF indication 4 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #4 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 5 | aRGFPFECSFCIDx5 | | Rx GFP: Far end CSF indication 5 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #5 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 6 | aRGFPFECSFCIDx6 | | Rx GFP: Far end CSF indication 6 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #6 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| | 7 | aRGFPFECSFCIDx7 | | Rx GFP: Far end CSF indication 7 per matching CID alarm for MAC0-7 0: no alarm 1: detection of a matching CID value #7 and far end CSF indication. Cleared on reception of CID matching value or after failing to receive 3 CSF indications in 3000 ms. |
| 0x1ebca 0x1180a 0x11c0a 0x1200a 0x1240a 0x1280a 0x12c0a 0x1300a | 0 | aRCTLRXx | 0x0000 | Rx LAPS/LAPF/GFP/PPP: Host frame received alarm for MAC0-7 |
| | 1 | aRCTLBERRx | | Rx LAPS/LAPF/GFP/PPP: Control Frame Buffer Overflow for MAC0-7 |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 56: Decapsulation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|--|
| 0x1ebcc 0x1180c 0x11c0c 0x1200c 0x1240c 0x1280c 0x12c0c 0x1300c | 0 | COUNT_DECAPx | 0x0000 | Rx decapsulation: count status Bit for MAC0-7 1: when any of the performance counters of each decapsulation block (associated to each VCG) has reached its maximum value in the saturating mode only 0: after being read by the microprocessor |

Table 57: Decapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|--------------|--------|---|
| 0x1ea00 0x119c0 0x11dc0 0x121c0 0x125c0 0x129c0 0x12dc0 0x131c0 | 0 | MaLNKSTSDWNx | 0x00FF | Rx LAPF: link down alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaLNKSTSUPx | | Rx LAPF: link up alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaRLFABTDx | | Rx LAPF: abort indication mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaRLFFCERx | | Rx LAPF: FCS error mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaRLFFSERx | | Rx LAPF: frame size error mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 5 | MaRLFMAXERx | | Rx LAPF: max frame size error mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 6 | MaRLFMINERx | | Rx LAPF: min frame size error mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 7 | MaRLFMMx | | Rx LAPF: frame mismatch error mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1ea02 0x119c2 0x11dc2 0x121c2 0x125c2 0x129c2 0x12dc2 0x131c2 | 0 | MaRLPSABTDx | 0x003F | Rx LAPS: abort indication mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaRLPSFCSErX | | Rx LAPS: FCS error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaRLPSFMMx | | Rx LAPS: frame mismatch error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaRLPSMINERx | | Rx LAPS: min frame size error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaRLPSSHTErX | | Rx LAPS: frame size error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 5 | MaRLPSMAXERx | | Rx LAPS: max frame size error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |

Table 57: Decapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-----------------|--------|---|
| 0x1ea04 0x119c4 0x11dc4 0x121c4 0x125c4 0x129c4 0x12dc4 0x131c4 | 0 | MaRGFPCIDERRx | 0x7FFF | Rx GFP: frame CID error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaRGFPEHECERRx | | Rx GFP: eHEC error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaRGFPEXIERRx | | Rx GFP: EXI error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaRGFPFCSErx | | Rx GFP: Payload area FCS error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaRGFPFECSEfx | | Rx GFP: Far end CSF indication mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 5 | MaRGFPHUNTx | | Rx GFP: Hunt state alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 6 | MaRGFPLOFfx | | Rx GFP: loss of frame delineation alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 7 | MaRGFPMAXERx | | Rx GFP: Maximum length error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 8 | MaRGFPMCHECERRx | | Rx GFP: Multiple Bit error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 9 | MaRGFPRESYNcx | | Rx GFP: PRESYNC state alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 10 | MaRGFPPTIERRx | | Rx GFP: PTI error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 11 | MaRGFPSCHECERRx | | Rx GFP: single Bit error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 12 | MaRGFPSYNcx | | Rx GFP: SYNC state alarm mask for MAC0 1: alarm is masked (default) 0: alarm is not masked |
| | 13 | MaRGFPTHECERRx | | Rx GFP: Type header check error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 14 | MaRGFPUPIERRx | | Rx GFP: UPI error alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 57: Decapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|------------------------|--------|--|
| 0x1ea06 0x119c6 0x11dc6 0x121c6 0x125c6 0x129c6 0x12dc6 0x131c6 | 0 | MaRGFPFECSCIDx0 | 0x00FF | Rx GFP: Far end CSF indication 0 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaRGFPFECSCIDx1 | | Rx GFP: Far end CSF indication 1 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaRGFPFECSCIDx2 | | Rx GFP: Far end CSF indication 2 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaRGFPFECSCIDx3 | | Rx GFP: Far end CSF indication 3 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaRGFPFECSCIDx4 | | Rx GFP: Far end CSF indication 4 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 5 | MaRGFPFECSCIDx5 | | Rx GFP: Far end CSF indication 5 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 6 | MaRGFPFECSCIDx6 | | Rx GFP: Far end CSF indication 6 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| | 7 | MaRGFPFECSCIDx7 | | Rx GFP: Far end CSF indication 7 per matching CID alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1ea08 0x119c8 0x11dc8 0x121c8 0x125c8 0x129c8 0x12dc8 0x131c8 | 0 | MaRPACMMx | 0x01FF | Rx PPP: Address or Control field mismatch error alarm mask for MAC0-7 |
| | 1 | MaRPFMMx | | Rx PPP: BCP Flags field Mismatch Error alarm mask for MAC0-7 |
| | 2 | MaRPMACMMx | | Rx PPP: BCP MAC Type field Mismatch Error alarm mask for MAC0-7 |
| | 3 | MaRPPABTDx | | Rx PPP: Abort Indication alarm mask for MAC0-7 |
| | 4 | MaRPPFCSErX | | Rx PPP: FCS Error alarm mask for MAC0-7 |
| | 5 | MaRPPMAXERx | | Rx PPP: Max Frame Size Error alarm mask for MAC0-7 |
| | 6 | MaRPPMINERx | | Rx PPP: Min Frame Size Error alarm mask for MAC0-7 |
| | 7 | MaRPPSHTERx | | Rx PPP: Frame Size Error alarm mask for MAC0-7 |
| | 8 | MaRPPROTMMx | | Rx PPP: PPP Protocol field Mismatch Error alarm mask for MAC0-7 |
| 0x1ea0a 0x119ca 0x11dca 0x121ca 0x125ca 0x129ca 0x12dca 0x131ca | 0 | MaRCTRLRx | 0x0003 | Rx LAPS/LAPF/GFP/PPP: Host frame received alarm mask |
| | 1 | MaRCTRLBERRx | | Rx LAPS/LAPF/GFP/PPP: Control Frame Buffer Overflow alarm mask |
| 0x1ea0c | 7-0 | MaEGENx_Lapf_Interrupt | 0x00FF | Rx LAPF: Interrupt mask for MAC0-7 1: interrupt for all LAPF alarms of each MAC is masked (default) 0: interrupt for all LAPF alarms of each MAC is not masked |
| 0x1ea0e | 7-0 | MaEGENx_Laps_Interrupt | 0x00FF | Rx LAPS: Interrupt mask for MAC0-7 1: interrupt for all LAPS alarms of each MAC is masked (default) 0: interrupt for all LAPS alarms of each MAC is not masked |
| 0x1ea10 | 7-0 | MaEGENx_Gfp_Interrupt | 0x00FF | Rx GFP: Interrupt mask for MAC0-7 1: interrupt for all GFP alarms of each MAC is masked (default) 0: interrupt for all GFP alarms of each MAC is not masked |

Table 57: Decapsulation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------|--------|--|
| 0x1ea12 | 7-0 | MaEGENx_GfpCid_Interrupt | 0x00FF | Rx LAPF: CID interrupt mask for MAC0-7 1: interrupt for all CID alarms of each MAC is masked (default) 0: interrupt for all CID alarms of each MAC is not masked |
| 0x1ea14 | 7-0 | MaEGENx_Ppp_Interrupt | 0x00FF | Rx PPP: Interrupt alarm mask for MAC0-7 1: interrupt for all PPP alarms of each MAC is masked (default) 0: interrupt for all PPP alarms of each MAC is not masked |
| 0x1ea16 | 7-0 | MaEGENx_CtlRx_Interrupt | 0x00FF | Rx LAPS/LAPF/GFP/PPP: Host Interrupt alarm mask for MAC0-7 1: interrupt for all frames to the host from each MAC is masked (default) 0: interrupt for all frames to the host from each MAC is not masked |
| 0x1ea18 | 7-0 | MCOUNT_DECAPx | 0x00FF | Rx Decapsulation: Global count status Bit mask 1: count status is masked (default) 0: count status is not masked |
| 0x1ea1a | 0 | MaGlobalRxLapf | 0x0001 | Rx LAPF: Global interrupt mask 1: interrupt for all LAPF alarms of all MAC is masked (default) 0: interrupt for all LAPF alarms of all MAC is not masked |
| 0x1ea1c | 0 | MaGlobalRxLaps | 0x0001 | Rx LAPS: Global interrupt mask 1: interrupt for all LAPS alarms of all MAC is masked (default) 0: interrupt for all LAPS alarms of all MAC is not masked |
| 0x1ea1e | 0 | MaGlobalRxGfp | 0x0001 | Rx GFP: Global interrupt mask 1: interrupt for all GFP alarms of all MAC is masked (default) 0: interrupt for all GFP alarms of all MAC is not masked |
| 0x1ea20 | 0 | MaGlobalRxGfpCid | 0x0001 | Rx GFP: Global CID interrupt mask 1: interrupt for all CID alarms of all MAC is masked (default) 0: interrupt for all CID alarms of all MAC is not masked |
| 0x1ea22 | 0 | MaGlobalRxPpp | 0x0001 | Rx PPP: Global interrupt mask 1: interrupt for all PPP alarms of all MAC is masked (default) 0: interrupt for all PPP alarms of all MAC is not masked |
| 0x1ea24 | 0 | MaGlobalRxCtl | 0x0001 | Rx LAPS/LAPF/GFP/PPP: Global Host Frame Interruption for MAC0 1: interrupt for all frames to the host from MAC0 is masked (default) 0: interrupt for all frames to the host from MAC0 is not masked |
| 0x1ea26 | 0 | MaDECAP_100M_Interrupt | 0x0001 | Rx: Global mask interrupt 1: interrupt of all Decapsulation blocks (all modes) is masked (default) 0: interrupt of all Decapsulation blocks (all modes) is not masked |
| 0x1ea28 | 0 | MCOUNT_DECAP_100M | 0x0001 | Global count status Bit mask for physical block SDRAM controller 1: count status bit of all decapsulation blocks is masked (default) 0: count status bit of all decapsulation blocks is not masked |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 58: Decapsulation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|---------------|--------|--|
| 0x1eb60 0x11820 0x11c20 0x12020 0x12420 0x12820 0x12c20 0x13020 | 0 | L1aLNKSTSDWNx | 0x0000 | Rx LAPF: link status down latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aLNKSTSUPx | | Rx LAPF: link status up latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aRLFABTDx | | Rx LAPF: abort indication latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aRLFFCERx | | Rx LAPF: FCS error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aRLFFSERx | | Rx LAPF: frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aRLFMAXERx | | Rx LAPF: max frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 6 | L1aRLFMINERx | | Rx LAPF: min frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 7 | L1aRLFMMx | | Rx LAPF: frame mismatch error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| 0x1eb62 0x11822 0x11c22 0x12022 0x12422 0x12822 0x12c22 0x13022 | 0 | L1aRLPSABTDx | 0x0000 | Rx LAPS: abort indication latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aRLPSFCSErx | | Rx LAPS: FCS error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aRLPSFMMx | | Rx LAPS: frame mismatch error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aRLPSMINERx | | Rx LAPS: min frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aRLPSSHTErx | | Rx LAPS: frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aRLPSMAXERx | | Rx LAPS: max frame size error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |

Table 58: Decapsulation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|------------------|--------|---|
| 0x1eb64 0x11824 0x11c24 0x12024 0x12424 0x12824 0x12c24 0x13024 | 0 | L1aRGFPCIDERRx | 0x0000 | Rx GFP: frame CID error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aRGFPEHECERRx | | Rx GFP: extension header check error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aRGFPEXIERRx | | Rx GFP: EXI error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aRGFPFCSERx | | Rx GFP: Payload area FCS check error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aRGFPFECFSx | | Rx GFP: Far end CSF indication latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aRGFPHUNTx | | Rx GFP: Hunt state latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 6 | L1aRGFPLOFx | | Rx GFP: loss of frame delineation latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 7 | L1aRGFPMAXERx | | Rx GFP: Maximum length error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 8 | L1aRGFPMCHECERRx | | Rx GFP: Multiple Bit error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 9 | L1aRGFPRESYNcx | | Rx GFP: PRESYNC state latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 10 | L1aRGFPPTIERRx | | Rx GFP: PTI error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 11 | L1aRGFPSCHECERRx | | Rx GFP: single Bit error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 12 | L1aRGFPSYNcx | | Rx GFP: SYNC state latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 13 | L1aRGFPTHECERRx | | Rx GFP: Type header check error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 14 | L1aRGFPUPIERRx | | Rx GFP: UPI error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 58: Decapsulation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|-------------------|--------|--|
| 0x1eb66 0x11826 0x11c26 0x12026 0x12426 0x12826 0x12c26 0x13026 | 0 | L1aRGFPFECSFCIDx0 | 0x0000 | Rx GFP: Far end CSF indication 0 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aRGFPFECSFCIDx1 | | Rx GFP: Far end CSF indication 1 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aRGFPFECSFCIDx2 | | Rx GFP: Far end CSF indication 2 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aRGFPFECSFCIDx3 | | Rx GFP: Far end CSF indication 3 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aRGFPFECSFCIDx4 | | Rx GFP: Far end CSF indication 4 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aRGFPFECSFCIDx5 | | Rx GFP: Far end CSF indication 5 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 6 | L1aRGFPFECSFCIDx6 | | Rx GFP: Far end CSF indication 6 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 7 | L1aRGFPFECSFCIDx7 | | Rx GFP: Far end CSF indication 7 per matching CID latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| 0x1eb68 0x11828 0x11c28 0x12028 0x12428 0x12828 0x12c28 0x13028 | 0 | L1aRPACMMx | 0x0000 | Rx PPP: Address or Control field mismatch error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 1 | L1aRPFMMx | | Rx PPP: BCP Flags field Mismatch Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 2 | L1aRPMACMMx | | Rx PPP: BCP MAC Type field Mismatch Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 3 | L1aRPPABTDx | | Rx PPP: Abort Indication latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 4 | L1aRPPFCSErx | | Rx PPP: FCS Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 5 | L1aRPPMAXERx | | Rx PPP: Max Frame Size Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 6 | L1aRPPMINERx | | Rx PPP: Min Frame Size Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 7 | L1aRPPSHTERx | | Rx PPP: Frame Size Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| | 8 | L1aRPPROTMMx | | Rx PPP: PPP Protocol field Mismatch Error latched alarm for MAC0-7 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |

Table 58: Decapsulation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|---------------|--------|--|
| 0x1eb6a 0x1182a 0x11c2a 0x1202a 0x1242a 0x1282a 0x12c2a 0x1302a | 0 | L1aRCTRLRx | 0x0000 | Rx LAPS/LAPF/GFP/PPP: Host frame received latched alarm 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| 0x1202a 0x1242a 0x1282a 0x12c2a 0x1302a | 1 | L1aRCTLBERRx | | Rx LAPS/LAPF/GFP/PPP: Control Frame Buffer Overflow latched alarm 1: alarm is latched (clear on read) for each MAC 0: no alarm is latched |
| 0x1eb6c 0x1182c 0x11c2c 0x1202c 0x1242c 0x1282c 0x12c2c 0x1302c | 0 | LCOUNT_DECAPx | 0x0000 | Rx de-encapsulation: latched status Bit count for MAC0-7 1: status bit count is latched for each MAC 0: status bit count is not latched for each MAC |

Table 59: Decapsulation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|------------------|--------|--|
| 0x1eb00 0x119d0 0x11dd0 0x121d0 0x125d0 0x129d0 0x12dd0 0x131d0 | 0 | Lapf_Interrupt | 0x0000 | Rx LAPF: Interruption for MAC0-7 1: interrupt for all LAPF alarms for each MAC 0: no interrupt |
| 0x1eb02 0x119d2 0x11dd2 0x121d2 0x125d2 0x129d2 0x12dd2 0x131d2 | 0 | Laps_Interrupt | 0x0000 | Rx LAPS: Interruption for MAC0-7 1: interrupt for all LAPS alarms for each MAC 0: no interrupt |
| 0x1eb04 0x119d4 0x11dd4 0x121d4 0x125d4 0x129d4 0x12dd4 0x131d4 | 0 | Gfp_Interrupt | 0x0000 | Rx GFP: Interruption for MAC0-7 1: interrupt for all GFP alarms for each MAC 0: no interrupt |
| 0x1eb06 0x119d6 0x11dd6 0x121d6 0x125d6 0x129d6 0x12dd6 0x131d6 | 0 | GfpCid_Interrupt | 0x0000 | Rx GFP: CID Interruption for MAC0-7 1: interrupt for all CID alarms for each MAC 0: no interrupt |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 59: Decapsulation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|------------------------|--------|--|
| 0x1eb08 0x119d8 0x11dd8 0x121d8 0x125d8 0x129d8 0x12dd8 0x131d8 | 0 | Ppp_Interrupt | 0x0000 | Rx PPP: Interruption for MAC0-7 1: interrupt for all PPP alarms for each MAC 0: no interrupt |
| 0x1eb0a 0x119da 0x11dda 0x121da 0x125da 0x129da 0x12dda 0x131da | 0 | CtlRx_Interrupt | 0x0000 | Rx LAPS/LAPF/GFP/PPP: Control Frame Interruption for MAC0-7 1: interrupt for all Control Frames to the host for each MAC 0: no interrupt |
| 0x1eb0c | 0 | RxLapf_Interrupt | 0x0000 | Rx LAPF: global Interruption 1: interrupt for all LAPF alarms for ALL MACs 0: no interrupt |
| 0x1eb0e | 0 | RxLaps_Interrupt | 0x0000 | Rx LAPS: global Interruption 1: interrupt for all LAPS alarms for ALL MACs 0: no interrupt |
| 0x1eb10 | 0 | RxGfp_Interrupt | 0x0000 | Rx GFP: global Interruption 1: interrupt for all GFP alarms for ALL MACs 0: no interrupt |
| 0x1eb12 | 0 | RxGfpCid_Interrupt | 0x0000 | Rx GFP: global CID Interruption 1: interrupt for all CID alarms for ALL MACs 0: no interrupt |
| 0x1eb14 | 0 | RxPpp_Interrupt | 0x0000 | Rx PPP: global Interruption 1: interrupt for all PPP alarms for ALL MACs 0: no interrupt |
| 0x1eb16 | 0 | RCtlRx_Interrupt | 0x0000 | Rx LAPS/LAPF/GFP/PPP: Global Host Frame Interruption 1: interrupt for all frames to the host for ALL MACs 0: no interrupt |
| 0x1eb18 | 0 | COUNT_Interrupt | 0x0000 | Rx Global Latched count status bit interruption |
| 0x1eb1a | 0 | DECAP_100M_Interrupt | 0x0000 | Rx Decapsulation Interruption 1: interrupt for all decapsulation blocks 0: no interrupt |
| 0x1eb1c | 0 | DECAP_Global_Interrupt | 0x0000 | Rx Global Decapsulation masked Interruption 1: interrupt after mask for all decapsulation blocks 0: no interrupt |

The following performance counters can be accessed in saturating mode or roll-over mode, depending on the state of the cCROV control bit. In saturating mode, counters do not count past their terminal count and are cleared to zero when read. In roll-over mode, counters roll-over to zero after reaching their terminal count, and are not cleared when read.

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|------------|--------|---|
| 0x1e800 0x11880 0x11c80 0x12080 0x12480 0x12880 0x12c80 0x13080 | 15-0 | rpcRMAXERx | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Payload max length violation counter for MAC0-7 |

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------------|--------|--|
| 0x1e802 0x11882 0x11c82 0x12082 0x12482 0x12882 0x12c82 0x13082 | 15-0 | rpcRMINERx | 0x0000 | Rx LAPF/LAPS/PPP: Payload min length violation counter for MAC0-7 |
| 0x1e804 0x11884 0x11c84 0x12084 0x12484 0x12884 0x12c84 0x13084 | 15-0 | rpcRFCSErX | 0x0000 | Rx LAPF/LAPS/GFP/PPP: FCS error counter for MAC0-7 For LAPS/PPP/LAPF, this register counts all LAPS/PPP/LAPF frames received (including control frames destined for the Host) with a FCS error. For GFP, this register counts all GFP frames received (not including control frames destined for the Host) with a FCS error (when payload FCS check is enabled). |
| 0x1e806 0x11886 0x11c86 0x12086 0x12486 0x12886 0x12c86 0x13086 | 15-0 | rpcRFRAMEx_LSB | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Frame Payloads counter for MAC0-7 - LSB This counter does not include the frame count of received LAPS/GFP/LAPF/PPP control frames that are destined for the Host. |
| 0x1e808 0x11888 0x11c88 0x12088 0x12488 0x12888 0x12c88 0x13088 | 15-0 | rpcRFRAMEx_MSB | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Frame Payloads counter for MAC0-7 - MSB This counter does not include the frame count of received LAPS/GFP/LAPF/PPP control frames that are destined for the Host. |
| 0x1e80a 0x1188a 0x11c8a 0x1208a 0x1248a 0x1288a 0x12c8a 0x1308a | 15-0 | rpcRBYTEx_LSB | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Payload byte counter for MAC0-7 - LSB Counts all bytes sent from the decapsulation block to the MAC to be transmitted out the Ethernet port (does not include any encapsulation frame header bytes). This counter does not include the byte count of received LAPS/GFP/LAPF/PPP control frames that are destined for the Host. |
| 0x1e80c 0x1188c 0x11c8c 0x1208c 0x1248c 0x1288c 0x12c8c 0x1308c | 15-0 | rpcRBYTEx_MSB | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Payload byte counter for MAC0-7 - MSB Counts all bytes sent from the decapsulation block to the MAC to be transmitted out the Ethernet port (does not include any encapsulation frame header bytes). This counter does not include the byte count of received LAPS/GFP/LAPF/PPP control frames that are destined for the Host. |
| 0x1e80e 0x1188e 0x11c8e 0x1208e 0x1248e 0x1288e 0x12c8e 0x1308e | 15-0 | rpcRLSPPPADDERx | 0x0000 | Rx LAPS/PPP: Address field mismatch counter for MAC0-7 |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|-------------------|--------|--|
| 0x1e810 0x11890 0x11c90 0x12090 0x12490 0x12890 0x12c90 0x13090 | 15-0 | rpcRLSPPPCNTERx | 0x0000 | Rx LAPS/PPP: Control field mismatch counter for MAC0-7 |
| 0x1e812 0x11892 0x11c92 0x12092 0x12492 0x12892 0x12c92 0x13092 | 15-0 | rpcRLSPPPDSTUFERx | 0x0000 | Rx LAPS/PPP: Byte de-stuffing violations counter for MAC0-7 This counter includes all received LAPS/PPP control frames detected with byte de-stuffing violations. |
| 0x1e814 0x11894 0x11c94 0x12094 0x12494 0x12894 0x12c94 0x13094 | 15-0 | rpcRLFABTDx | 0x0000 | Rx LAPF: Aborted frame counter for MAC0-7 |
| 0x1e816 0x11896 0x11c96 0x12096 0x12496 0x12896 0x12c96 0x13096 | 15-0 | rpcRLFADDERx | 0x0000 | Rx LAPF: Address field mismatch counter for MAC0-7 |
| 0x1e818 0x11898 0x11c98 0x12098 0x12498 0x12898 0x12c98 0x13098 | 15-0 | rpcRLFBADx | 0x0000 | Rx LAPF: Invalid frame counter for MAC0-7 This counter includes all received LAPF LMI frames detected as invalid. |
| 0x1e81a 0x1189a 0x11c9a 0x1209a 0x1249a 0x1289a 0x12c9a 0x1309a | 15-0 | rpcRLFCNTERx | 0x0000 | Rx LAPF: Control field mismatch counter for MAC0-7 |
| 0x1e81c 0x1189c 0x11c9c 0x1209c 0x1249c 0x1289c 0x12c9c 0x1309c | 15-0 | rpcRLFDLCIERx | 0x0000 | Rx LAPF: DLCI field mismatch counter for MAC0-7 |

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|----------------|--------|--|
| 0x1e81e 0x1189e 0x11c9e 0x1209e 0x1249e 0x1289e 0x12c9e 0x1309e | 15-0 | rpcRLFDSTUFERx | 0x0000 | Rx LAPF: Bit de-stuffing violations counter for MAC0-7 This counter includes all received LAPF LMI frames detected with bit de-stuffing violations. |
| 0x1e820 0x118a0 0x11ca0 0x120a0 0x124a0 0x128a0 0x12ca0 0x130a0 | 15-0 | rpcRLFFLAGERx | 0x0000 | Rx LAPF: Flag error counter for MAC0-7 This counter includes all received LAPF LMI frames detected with Flag errors. |
| 0x1e822 0x118a2 0x11ca2 0x120a2 0x124a2 0x128a2 0x12ca2 0x130a2 | 15-0 | rpcRLFLMlx | 0x0000 | Rx LAPF: LMI frame counter for MAC0-7 |
| 0x1e824 0x118a4 0x11ca4 0x120a4 0x124a4 0x128a4 0x12ca4 0x130a4 | 15-0 | rpcRLFNLPIDERx | 0x0000 | Rx LAPF: NLPID field mismatch counter for MAC0-7 |
| 0x1e826 0x118a6 0x11ca6 0x120a6 0x124a6 0x128a6 0x12ca6 0x130a6 | 15-0 | rpcRLFOUIERx | 0x0000 | Rx LAPF: OUI field mismatch counter for MAC0-7 |
| 0x1e828 0x118a8 0x11ca8 0x120a8 0x124a8 0x128a8 0x12ca8 0x130a8 | 15-0 | rpcRLFPIDERx | 0x0000 | Rx LAPF: PID field mismatch counter for MAC0-7 |
| 0x1e82a 0x118aa 0x11caa 0x120aa 0x124aa 0x128aa 0x12caa 0x130aa | 15-0 | rpcRLPSABTDx | 0x0000 | Rx LAPS: Aborted frame counter for MAC0-7 |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|----------------|--------|---|
| 0x1e82c 0x118ac 0x11cac 0x120ac 0x124ac 0x128ac 0x12cac 0x130ac | 15-0 | rpcRLPSBADx | 0x0000 | Rx LAPS: Invalid frame counter for MAC0-7 This counter includes all received LAPS control frames detected as invalid. |
| 0x1e82e 0x118ae 0x11cae 0x120ae 0x124ae 0x128ae 0x12cae 0x130ae | 15-0 | rpcRLPSFLAGERx | 0x0000 | Rx LAPS: Flag error counter for MAC0-7 This counter includes all received LAPS control frames detected with Flag errors. |
| 0x1e830 0x118b0 0x11cb0 0x120b0 0x124b0 0x128b0 0x12cb0 0x130b0 | 15-0 | rpcRLPSSAPIERx | 0x0000 | Rx LAPS: SAPI field mismatch counter for MAC0-7 |
| 0x1e832 0x118b2 0x11cb2 0x120b2 0x124b2 0x128b2 0x12cb2 0x130b2 | 15-0 | rpcRLPSHOSTx | 0x0000 | Rx LAPS: LAPS Control frame Payload counter for MAC0-7 |
| 0x1e834 0x118b4 0x11cb4 0x120b4 0x124b4 0x128b4 0x12cb4 0x130b4 | 15-0 | rpcRPAUSEx | 0x0000 | Rx Decapsulation: Receive PAUSE frame counter for MAC0-7 In the SONET/SDH-to-Ethernet direction, this register counts the number of PAUSE frames received destined for the MAC0-7 (after the decapsulation process). |
| 0x1e836 0x118b6 0x11cb6 0x120b6 0x124b6 0x128b6 0x12cb6 0x130b6 | 15-0 | rpcRGFPCHECERx | 0x0000 | Rx GFP: cHEC error counter for MAC0-7 Counts the number of GFP frames received that are detected with a single-bit error within the Core header (i.e., cHEC field) only. |
| 0x1e838 0x118b8 0x11cb8 0x120b8 0x124b8 0x128b8 0x12cb8 0x130b8 | 15-0 | rpcRGFPCIDERx | 0x0000 | Rx GFP: CID mismatch counter for MAC0-7 Counts the number of GFP frames received that are detected with a CID mismatch/unsupported value in the CID field only. |

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|------------------|--------|---|
| 0x1e83a 0x118ba 0x11cba 0x120ba 0x124ba 0x128ba 0x12cba 0x130ba | 15-0 | rpcRGFPDATAx_LSB | 0x0000 | Rx GFP: GFP Client Data frame counter for MAC0-7 - LSB Counts the number of GFP Client Data frames received that are detected with a valid/supported GFP Client Data frame type. |
| 0x1e83c 0x118bc 0x11cbc 0x120bc 0x124bc 0x128bc 0x12cbc 0x130bc | 15-0 | rpcRGFPDATAx_MSB | 0x0000 | Rx GFP: GFP Client Data frame counter for MAC0-7 - MSB Counts the number of GFP Client Data frames received that are detected with a valid/supported GFP Client Data frame type. |
| 0x1e83e 0x118be 0x11cbe 0x120be 0x124be 0x128be 0x12cbe 0x130be | 15-0 | rpcRGFPEHECERx | 0x0000 | Rx GFP: eHEC Single-bit error counter for MAC0-7 Counts the number of GFP frames received that are detected with a single-bit error within the Extension header (i.e., eHEC field) only. |
| 0x1e840 0x118c0 0x11cc0 0x120c0 0x124c0 0x128c0 0x12cc0 0x130c0 | 15-0 | rpcRGFPEHECMERx | 0x0000 | Rx GFP: eHEC Multi-bit error counter for MAC0-7 Counts the number of GFP frames received that are detected with Multi-bit errors within the Extension header (i.e., eHEC field) only. |
| 0x1e842 0x118c2 0x11cc2 0x120c2 0x124c2 0x128c2 0x12cc2 0x130c2 | 15-0 | rpcRGFPEXIERx | 0x0000 | Rx GFP: GFP EXI field mismatch counter for MAC0-7 Counts all GFP frames received that are detected with a mismatch on the EXI field contents (i.e., value of EXI is not equal to NULL or LINEAR). |
| 0x1e844 0x118c4 0x11cc4 0x120c4 0x124c4 0x128c4 0x12cc4 0x130c4 | 15-0 | rpcRGFPIDLERx | 0x0000 | Rx GFP: GFP IDLE frame error counter for MAC0-7 Counts all GFP IDLE frames received that are detected with an error. |
| 0x1e846 0x118c6 0x11cc6 0x120c6 0x124c6 0x128c6 0x12cc6 0x130c6 | 15-0 | rpcRGFPMGTx | 0x0000 | Rx GFP: GFP Client Management frame counter for MAC0-7 Counts the number of GFP Client Management frames received that are detected with a valid/supported GFP Client Management frame type (i.e., presently only CSF indication type is supported). |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|------------------|--------|--|
| 0x1e848 0x118c8 0x11cc8 0x120c8 0x124c8 0x128c8 0x12cc8 0x130c8 | 15-0 | rpcRGFPPTIERx | 0x0000 | Rx GFP: GFP PTI field mismatch counter for MAC0-7 Counts all GFP frames received that are detected with a mismatch on the PTI field contents (i.e., value of PTI is not equal to Client Data or Management frame). |
| 0x1e84a 0x118ca 0x11cca 0x120ca 0x124ca 0x128ca 0x12cca 0x130ca | 15-0 | rpcRGFPHECERx | 0x0000 | Rx GFP: tHEC Single-bit error counter for MAC0-7 Counts the number of GFP frames received (not destined for the Host, i.e., GFP Client Management frames) that are detected with a single-bit error within the Type header (i.e., tHEC field) only. |
| 0x1e84c 0x118cc 0x11ccc 0x120cc 0x124cc 0x128cc 0x12ccc 0x130cc | 15-0 | rpcRGFPHECMERx | 0x0000 | Rx GFP: tHEC Multi-bit error counter for MAC0-7 Counts the number of GFP frames received (not destined for the Host, i.e., GFP Client management frames) that are detected with Multi-bit errors within the Type header (i.e., tHEC field) only. |
| 0x1e84e 0x118ce 0x11cce 0x120ce 0x124ce 0x128ce 0x12cce 0x130ce | 15-0 | rpcRGFPUPIERx | 0x0000 | Rx GFP: GFP UPI field mismatch counter for MAC0-7 Counts all GFP frames received that are detected with a mismatch on the UPI field contents (value of UPI field is not equal to rRPMACFDx register). |
| 0x1e850 0x118d0 0x11cd0 0x120d0 0x124d0 0x128d0 0x12cd0 0x130d0 | 15-0 | rpcRPPPFLAGERx | 0x0000 | Rx PPP: Flag error counter for MAC0-7 This counter includes all received PPP LCP/NCP-BCP frames detected with Flag errors. |
| 0x1e852 0x118d2 0x11cd2 0x120d2 0x124d2 0x128d2 0x12cd2 0x130d2 | 15-0 | rpcRPPPROTEx | 0x0000 | Rx PPP: Protocol field mismatch counter for MAC0-7 |
| 0x1e854 0x118d4 0x11cd4 0x120d4 0x124d4 0x128d4 0x12cd4 0x130d4 | 15-0 | rpcRPPPMACTYPERx | 0x0000 | Rx PPP: BCP TYPE field mismatch counter for MAC0-7 |

Table 60: Decapsulation Block - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|--|------|-------------|--------|--|
| 0x1e856 0x118d6 0x11cd6 0x120d6 0x124d6 0x128d6 0x12cd6 0x130d6 | 15-0 | rpcRPPPLCPx | 0x0000 | Rx PPP: LCP frame counter for MAC0-7 |
| 0x1e858 0x118d8 0x11cd8 0x120d8 0x124d8 0x128d8 0x12cd8 0x130d8 | 15-0 | rpcRPPNCPx | 0x0000 | Rx PPP: NCP-LCP frame counter for MAC0-7 |
| 0x1e85a 0x118da 0x11cda 0x120da 0x124da 0x128da 0x12cda 0x130da | 15-0 | rpcRPPBADx | 0x0000 | Rx PPP: Invalid frame counter for MAC0-7 This counter includes all received PPP LCP/NCP-BCP frames detected as invalid. |
| 0x1e85c 0x118dc 0x11cdc 0x120dc 0x124dc 0x128dc 0x12cdc 0x130dc | 15-0 | rpcRPPABTDx | 0x0000 | Rx PPP: Aborted frame counter for MAC0-7 |

Table 61: Decapsulation Block - Status (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|----------------------------|---|--------|--|
| 0x1eb80 0x119e0 0x11de0 0x121e0 0x125e0 0x129e0 0x12de0 0x131e0 | 0 1 2 3 4 5 | sRMAXERx sRMINERx sRFCSErX sRLSPPPADDERx sRLSPPPCnTERx sRLSPPPDSTUFERx | 0x0000 | Rx LAPF/LAPS/GFP/PPP: Status for payload max length violation counter for MAC0-7 Rx LAPF/LAPS/PPP: Status for payload min length violation counter for MAC0-7 Rx LAPF/LAPS/GFP/PPP: Status for FCS error counter for MAC0-7 Rx LAPS/PPP: Status for Address field mismatch counter for MAC0-7 Rx LAPS/PPP: Status for Control field mismatch counter for MAC0-7 Rx LAPS/PPP: Status for Byte destuffing violations counter for MAC0-7 |
| 0x1eb82 0x119e2 0x11de2 0x121e2 0x125e2 0x129e2 0x12de2 0x131e2 | 0 1 2 3 4 | sRLPSABTDx sRLPSBADx sRLPSFLAGERx sRLPSSAPIERx sRLPSHOSTx | 0x0000 | Rx LAPS: Status for aborted frame counter for MAC0-7 Rx LAPS: Status for invalid frame counter for MAC0-7 Rx LAPS: Status for flag error counter for MAC0-7 Rx LAPS: Status for SAPI field mismatch counter for MAC0-7 Rx LAPS: Status for LAPS Control frame counter for MAC0-7 |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 61: Decapsulation Block - Status (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|-----|----------------------------|--------|---|
| 0x1eb84 0x119e4 0x11de4 0x121e4 0x125e4 0x129e4 0x12de4 0x131e4 | 0 | sRLFABTDx | 0x0000 | Rx LAPP: Status for aborted frame counter for MAC0-7 |
| | 1 | sRLFADDERx | | Rx LAPP: Status for address field mismatch counter for MAC0-7 |
| | 2 | sRLFBADx | | Rx LAPP: Status for invalid frame counter for MAC0-7 |
| | 3 | sRLFCNTERx | | Rx LAPP: Status for control field mismatch counter for MAC0-7 |
| | 4 | sRLFDLCIERx | | Rx LAPP: Status for DLCI field mismatch counter for MAC0-7 |
| | 5 | sRLFDSTUFERx | | Rx LAPP: Status for bit destuffing violations counter for MAC0-7 |
| | 6 | sRLFFLAGERx | | Rx LAPP: Status for flag error counter for MAC0-7 |
| | 7 | sRLFLMIx | | Rx LAPP: Status for LMI frame counter for MAC0-7 |
| | 8 | sRLFNLPIDERx | | Rx LAPP: Status for NLPID field mismatch counter for MAC0-7 |
| | 9 | sRLFOUIERx | | Rx LAPP: Status for OUI field mismatch counter for MAC0-7 |
| | 10 | sRLFPIDERx | | Rx LAPP: Status for PID field mismatch counter for MAC0-7 |
| 0x1eb86 0x119e6 0x11de6 0x121e6 0x125e6 0x129e6 0x12de6 0x131e6 | 0 | sRGFPCHECERx | 0x0000 | Rx GFP: Status for cHEC single bit error counter for MAC0-7 |
| | 1 | sRGFPCIDERx | | Rx GFP: Status for CID mismatch counter for MAC0-7 |
| | 2 | sRGFPEHECERx | | Rx GFP: Status for eHEC single bit error counter for MAC0-7 |
| | 3 | sRGFPEHECMERx | | Rx GFP: Status for eHEC multibit error counter for MAC0-7 |
| | 4 | sRGFPEXIERx | | Rx GFP: Status for EXI mismatch counter for MAC0-7 |
| | 5 | sRGFPIDLERx | | Rx GFP: Status for IDLE frame error counter for MAC0-7 |
| | 6 | sRGFPMGTx | | Rx GFP: Status for valid client management frame counter for MAC0-7 |
| | 7 | sRGFPPTIERx | | Rx GFP: Status for PTI mismatch counter for MAC0-7 |
| | 8 | sRGFPTHECERx | | Rx GFP: Status for tHEC single bit error counter for MAC0-7 |
| | 9 | sRGFPTHECMERx | | Rx GFP: Status for tHEC multi-bit error counter for MAC0-7 |
| | 10 | sRGFPUPIERx | | Rx GFP: Status for UPI mismatch counter for MAC0-7 |
| 0x1eb88 0x119e8 0x11de8 0x121e8 0x125e8 0x129e8 0x12de8 0x131e8 | 0 | sRPPPFLAGERx | 0x0000 | Rx PPP: Flag error status for MAC0-7 |
| | 1 | sRPPPPROTERx | | Rx PPP: Protocol field mismatch status for MAC0-7 |
| | 2 | sRPPPMACTYPERx | | Rx PPP: BCP MAC TYPE field mismatch status for MAC0-7 |
| | 3 | sRPPP LCPx | | Rx PPP: LCP frame status for MAC0-7 |
| | 4 | sRPPPNCPx | | Rx PPP: NCP-LCP frame status for MAC0-7 |
| | 5 | sRPPPBADx | | Rx PPP: Invalid frame status for MAC0-7 |
| | 6 | sRPPPBATDx | | Rx PPP: Abort frame status for MAC0-7 |
| 0x1eb8a 0x119ea 0x11dea 0x121ea 0x125ea 0x129ea 0x12dea 0x131ea | 0 | MACx_LAPS_Status_Lvl3 | 0x0000 | Rx LAPS: merge all the LAPS performance status for MAC0-7 |
| | 1 | MACx_LAPF_Status_Lvl3 | | Rx LAPP: merge all the LAPP performance status for MAC0-7 |
| | 2 | MACx_PPP_Status_Lvl3 | | Rx PPP: merge all the PPP performance status for MAC0-7 |
| | 3 | MACx_GFP_Status_Lvl3 | | Rx GFP: merge all the GFP performance status for MAC0-7 |
| | 4 | MACx_CmnPerf_Status_Lvl3 | | Rx: merge all the common performance status for MAC0-7 |
| | 5 | sHOLDROPOVFX | | Rx: Status for Dropped frame in case of overflow for channel x |
| | 6 | sRPAUSEx | | Rx: Status for total number of receive PAUSE frame for channel x |
| 0x1eb8c | 7-0 | MAC0-7_PerfCnt_Status_Lvl2 | 0x0000 | Rx: merge all the level 2 performance status for MAC0-7 |

SDRAM CONTROL REGISTERS

Table 62 - SDRAM Control and SDRAM Interface Configuration

Table 62: SDRAM Control - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|----------------------|--------|---|
| 0x1d600 | 0 | SDRAMINIT | 0x00B8 | SDRAM Initialization start Bit 0: no action 1: restart the initialization of the SDRAM. Must be cleared at the end of the initialization. |
| | 2-1 | SDRAM_CFG | | SDRAM configuration 8MB/16MB/32MB 00: 8MB 01: 16 MB 10: 32 MB 11: Reserved |
| | 5-3 | SDRAM_TRFC | | SDRAM CTRL: TRFC timing, Auto refresh period range 0 to 7 (unit = number of periods at 10 ns +1) default value = 7 (means 8 periods at 10 ns) |
| | 7-6 | SDRAM_TRP | | SDRAM CTRL: TRP timing. Precharge command period range 0 to 3 (unit = number of periods at 10 ns +1). This control bit MUST be left at the default value = 2 (means 3 periods at 10 ns). |
| 0x1d602 | 10-0 | MBR_VALUE | 0x0031 | SDRAM CTRL: Mode Register default value. Default must be 0 and 000 and 011 and 0 and 001 which means CAS latency 3, burst length = 2 and sequential burst access. |
| 0x1d604 | 15-0 | SDRARP | 0x009B | SDRAM CTRL: SDRAM Auto Refresh Period in 8 SYCLK period. Default is 155 (24 μs/row). Must be set to 78 (decimal) for 12 μs/row. |
| 0x1d606 | 7-0 | SDRINIT_AR_MBR | 0x0008 | SDRAM CTRL: Number of Auto-refresh cycle performed during Initialization. Default value = 8. Note: A configured value of 'n' will provide 'n+1' AUTO REFRESH cycles during the initialization period. |
| 0x1d608 | 15-0 | SDRTINIT | 0x0064 | SDRAM CTRL: Power up initialization delay in unit of 200 cycles of clock to the SDRAM i.e., in unit of 100 cycles of SYCLK. Default is 100. |
| 0x1d60a | 15-0 | RAMC_MB_WINDOWS_ETRC | 0x0007 | SDRAM CTRL: SDRAM arbitration windows for Ethernet input client. This register must be written with 0x0009 for GMII mode. The default value of 0x0007 is used for SMII mode. |
| 0x1d60c | 15-0 | RAMC_MB_WINDOWS_SHTC | 0x0003 | SDRAM CTRL: SDRAM arbitration windows for SONET transmit client. This register must be written with 0x0001 for GMII mode. The default value of 0x0003 is used for SMII mode. |
| 0x1d60e | 15-0 | RAMC_MB_WINDOWS_ETTC | 0x0001 | SDRAM CTRL: SDRAM arbitration windows for Ethernet output client. |
| 0x1d610 | 15-0 | RAMC_MB_WINDOWS_SHRC | 0x0001 | SDRAM CTRL: SDRAM arbitration windows for SONET receive client. This register must be written with 0x0002 for STS-3c/VC-4 mode or GMII mode. The default value of 0x0001 is used for all other modes. |
| 0x1d612 | 15-0 | RAMC_MB_WINDOWS_DFRC | 0x0001 | SDRAM CTRL: SDRAM arbitration windows for HOL input client. |
| 0x1d614 | 15-0 | RAMC_MB_WINDOWS_DFTC | 0x0002 | SDRAM CTRL: SDRAM arbitration windows for HOL output client. This register must be written with 0x0001 for GMII mode. The default value of 0x0002 is used for SMII mode. |

Note: Follow procedure defined in ["Configuration Changes/Initialization"](#) on page 184 to change any register in [Table 62](#).

Table 63 and 64 - Microprocessor Access to the SDRAM (Indirect Access)**Table 63: SDRAM - Access Control Registers (RW)**

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------|--------|---|
| 0x1d630 | 15-0 | UP_Addr2RdLSB | 0x0000 | SDRAM CTRL: LSB Address for microprocessor RD access to the SDRAM |
| 0x1d632 | 6-0 | UP_Addr2RdMSB | 0x0000 | SDRAM CTRL: MSB Address for microprocessor RD access to the SDRAM |
| 0x1d634 | 15-0 | UP_Addr2WrLSB | 0x0000 | SDRAM CTRL: LSB Address for microprocessor WR access to the SDRAM |
| 0x1d636 | 6-0 | UP_Addr2WrMSB | 0x0000 | SDRAM CTRL: MSB Address for microprocessor WR access to the SDRAM |
| 0x1d638 | 15-0 | UP_Data2WrLSB | 0x0000 | SDRAM CTRL: LSB data from the microprocessor to be written to SDRAM |
| 0x1d63a | 15-0 | UP_Data2WrMSB | 0x0000 | SDRAM CTRL: MSB data from the microprocessor to be written to SDRAM |
| 0x1d63c | 0 | UP_WrAddr2Rd | 0x0000 | SDRAM CTRL: Read Address field is ready |
| 0x1d63e | 0 | UP_WrAddr2Wr | 0x0000 | SDRAM CTRL: Write Address field is ready |

Table 64: SDRAM - Access Results Registers (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|--------------|--------|---|
| 0x1d620 | 15-0 | UP_DataRdLSB | 0x0000 | SDRAM CTRL: LSB read data by microprocessor access to the SDRAM |
| 0x1d622 | 15-0 | UP_DataRdMSB | 0x0000 | SDRAM CTRL: MSB read data by microprocessor access to the SDRAM |

TX VIRTUAL CONCATENATION REGISTERS

Tables 65 through 75 - Configuration, Status and Alarms of the Transmit (Ethernet to SONET) Virtual Concatenation Block

Table 65: Tx Virtual Concatenation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x1ec80 | 0 | cSNTSDH | 0x0000 | Tx VCAT: SONET/SDH configuration 0: SONET (Default) 1: SDH |
| 0x1ec82 | 1-0 | cTHOVC3_3 | 0x0000 | Tx VCAT: STS-1/VC-3 #3 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #3 is used in low order to carry selected VT1.5/VC-11 01: AU-3 C is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #3 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #3 is used in low order to carry VT-2/VC-12 01: AU-3 C is used to carry VT-2/VC-12 10: Reserved 11: STS-1/TUG-3 #3 (with its TU-3/VC-3) is used in high order |
| | 3-2 | cTHOVC3_2 | | Tx VCAT: STS-1/VC-3 #2 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #2 is used in low order to carry selected VT1.5/VC-11 01: AU-3 B is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #2 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #2 is used in low order to carry VT-2/VC-12 01: AU-3 B is used to carry VT-2/VC-12 10: Reserved 11: STS-1/TUG-3 #2 (with its TU-3/VC-3) is used in high order |
| | 5-4 | cTHOVC3_1 | | Tx VCAT: STS-1/VC-3 #1 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #1 is used in low order to carry selected VT1.5/VC-11 01: AU-3 A is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #1 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #1 is used in low order to carry VT-2/VC-12 01: AU-3 A is used to carry VT-2/VC-12 10: Reserved 11: STS-1/TUG-3 #1 (with its TU-3/VC-3) is used in high order |
| | 6 | cTHOVC4 | | Tx VCAT: VC-4/STS-3c configuration 0: Configured for non VC-4/STS-3c mode (i.e., when using sub-structured containers/tributaries) 1: Configured for VC-4/STS-3c mode |
| 0x1ec84 | 7-0 | cTVC4MAC | 0x0000 | Tx VCAT: 10/100 port to be mapped into VC-4/STS3c bit mapped register to indicate the MAC associated to the VC-4/STS-3c in case of configuration in VC-4/STS-3c. bit 0 is associated to port 1 bit 7 is associated to port 8 Only a single bit of this register may be set to 1. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 65: Tx Virtual Concatenation Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description | | | | | | | |
|----------------------|------------|----------------|--------|--|------|------------|-----|------|-----|-------|-----|
| 0x1ec86 – 0x1ec94 | 1-0 | cTVCG_x | 0x0000 | Tx VCAT: configuration for VCG0-7 00: VCG used in ITU/ANSI low order virtual concatenation 01: VCG used in non standard ITU/ANSI low order virtual concatenation and in non LCAS 10: Reserved 11: VCG used in ITU/ANSI high order virtual concatenation | | | | | | | |
| | 2 | cTLCAS_x | | Tx VCAT: LCAS configuration for VCG0-7 0: VCG in non LCAS mode 1: VCG in LCAS mode | | | | | | | |
| | 9-3 | cTMST_VT_x | | Tx VCAT: LCAS tributary selection configuration for VCG0-7. Number of tributary which carries the MST and RS_ACK per VCG. For non-LCAS, set bits 9,8 to 0b11. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bits</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>9-8</td> <td>AU-3</td> </tr> <tr> <td>7-5</td> <td>TUG-2</td> </tr> <tr> <td>4-3</td> <td>TU-1</td> </tr> </tbody> </table> <p>Note: If the VCG is not used, set bits 9-8 to 0b11.</p> | Bits | Assignment | 9-8 | AU-3 | 7-5 | TUG-2 | 4-3 |
| Bits | Assignment | | | | | | | | | | |
| 9-8 | AU-3 | | | | | | | | | | |
| 7-5 | TUG-2 | | | | | | | | | | |
| 4-3 | TU-1 | | | | | | | | | | |
| 0x1ec96 | 7-0 | cTFCRSTx | 0x00FF | Tx VCAT: frame count reset for VCG0-7 0: in low order, frame count is increasing normally / in high order MF11/MF12 are increasing normally 1: frame count (low order) or MF12 set to 0. MF11 is not affected. | | | | | | | |
| 0x1ec98 | 7-0 | cTVCG_SRSTx | 0x0000 | Tx VCAT: LCAS VCG0-7 soft reset (only used in LCAS mode). When set to 1, the LCAS state machine corresponding to the VCG is reset. If any members are assigned to the corresponding VCG, they must be configured back to the global pool before releasing the reset. The member control bits are cTLOPOOL_x and cTHOPOOL_x. | | | | | | | |
| 0x1ec9a | 1-0 | cINRT_GRPTX20M | 0x0001 | Alarm latching configuration for Tables 47 and 69 Criteria used to create latched alarms from the raw (unlatched) alarms. 00: positive level 01: rising edge (default) 10: falling edge 11: rising or falling edge | | | | | | | |

Table 66: Tx Virtual Concatenation Block - LCAS Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|---------------|--------|---|
| 0x1ed00 – 0x1eda6 | 0 | aTLCPRD1_x | 0x0000 | LO: Tx LCAS ADD Period1 alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm on expiry of timeout counter. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 1 | aTLCASADDED_x | | LO: Tx LCAS ADD successful alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: when the member has been added and its state machine goes to NORM state 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 2 | aTLCASREM_x | | LO: Tx LCAS REMOVE successful alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: when the member has been removed and its state machine goes from NORM to IDLE state. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 3 | aTLCASDNU_x | | LO: Tx LCAS DNU alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: when MST = FAIL for the member while in NORM/EOS state. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 4 | aTLCASDNUOK_x | | LO: Tx LCAS DNU OK alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: when MST = OK to change member from DNU to NORM/EOS state. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| 0x1eda8 – 0x1edac | 0 | aTLCPRD1_x | 0x0000 | HO: Tx LCAS ADD Period1 alarm for the STS-1/VC-3 1_3 1: alarm on expiry of timeout counter. 0: no alarm |
| | 1 | aTLCASADDED_x | | HO: Tx LCAS ADD successful alarm for the STS-1/VC-3 1_3 1: when the member has been added and its state machine goes to NORM state 0: no alarm |
| | 2 | aTLCASREM_x | | HO: Tx LCAS RE MOVE successful alarm for the STS-1/VC-3 1_3 1: when the member has been removed and its state machine goes from NORM to IDLE state. 0: no alarm |
| | 3 | aTLCASDNU_x | | HO: Tx LCAS DNU alarm for the STS-1/VC-3 1_3 1: when MST = FAIL for the member while in NORM/EOS state. 0: no alarm |
| | 4 | aTLCASDNUOK_x | | HO: Tx LCAS DNU OK successful alarm for the STS-1/VC-3 1_3 1: when MST = OK to change member from DNU to NORM/EOS state. 0: no alarm |
| 0x1edae | 7-0 | aTLOPRD2_x | 0x0000 | Tx LCAS ADD Period2 alarm for the VCG 0_7 1: alarm on expiry of timeout counter. 0: no alarm |
| 0x1edb0 | 7-0 | aTHOPRD2_x | 0x0000 | Tx LCAS ADD Period2 alarm for the VCG 0_7 1: alarm on expiry of timeout counter. 0: no alarm |
| 0x1edb2 | 7-0 | aTLOPRD3_x | 0x0000 | Tx LO REMOVE Period3 alarm for the VCG 0_7 1: alarm on expiry of timeout counter. 0: no alarm |
| 0x1edb4 | 7-0 | aTHOPRD3_x | 0x0000 | Tx HO REMOVE Period3 alarm for the VCG0-7 1: alarm on expiry of timeout counter. 0: no alarm |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 67: VT/VC Address Offsets

| AU-3 # | TUG-2 # | TU-1 # | VT/VC # (VT1.5/VC-11) | VT/VC # (VT2/VC-12) | Address Offset (Hex) |
|--------|---------|--------|--------------------------|------------------------|----------------------|
| 1 | 1 | 1 | 0 | 0 | 00 |
| 1 | 1 | 2 | 1 | 1 | 02 |
| 1 | 1 | 3 | 2 | 2 | 04 |
| 1 | 1 | 4 | 3 | Not Used | 06 |
| 1 | 2 | 1 | 4 | 3 | 08 |
| 1 | 2 | 2 | 5 | 4 | 0A |
| 1 | 2 | 3 | 6 | 5 | 0C |
| 1 | 2 | 4 | 7 | Not Used | 0E |
| 1 | 3 | 1 | 8 | 6 | 10 |
| 1 | 3 | 2 | 9 | 7 | 12 |
| 1 | 3 | 3 | 10 | 8 | 14 |
| 1 | 3 | 4 | 11 | Not Used | 16 |
| 1 | 4 | 1 | 12 | 9 | 18 |
| 1 | 4 | 2 | 13 | 10 | 1A |
| 1 | 4 | 3 | 14 | 11 | 1C |
| 1 | 4 | 4 | 15 | Not Used | 1E |
| 1 | 5 | 1 | 16 | 12 | 20 |
| 1 | 5 | 2 | 17 | 13 | 22 |
| 1 | 5 | 3 | 18 | 14 | 24 |
| 1 | 5 | 4 | 19 | Not Used | 26 |
| 1 | 6 | 1 | 20 | 15 | 28 |
| 1 | 6 | 2 | 21 | 16 | 2A |
| 1 | 6 | 3 | 22 | 17 | 2C |
| 1 | 6 | 4 | 23 | Not Used | 2E |
| 1 | 7 | 1 | 24 | 18 | 30 |
| 1 | 7 | 2 | 25 | 19 | 32 |
| 1 | 7 | 3 | 26 | 20 | 34 |
| 1 | 7 | 4 | 27 | Not Used | 36 |
| 2 | 1 | 1 | 28 | 21 | 38 |
| 2 | 1 | 2 | 29 | 22 | 3A |
| 2 | 1 | 3 | 30 | 23 | 3C |
| 2 | 1 | 4 | 31 | Not Used | 3E |
| 2 | 2 | 1 | 32 | 24 | 40 |
| 2 | 2 | 2 | 33 | 25 | 42 |
| 2 | 2 | 3 | 34 | 26 | 44 |
| 2 | 2 | 4 | 35 | Not Used | 46 |
| 2 | 3 | 1 | 36 | 27 | 48 |
| 2 | 3 | 2 | 37 | 28 | 4A |
| 2 | 3 | 3 | 38 | 29 | 4C |
| 2 | 3 | 4 | 39 | Not Used | 4E |
| 2 | 4 | 1 | 40 | 30 | 50 |
| 2 | 4 | 2 | 41 | 31 | 52 |
| 2 | 4 | 3 | 42 | 32 | 54 |
| 2 | 4 | 4 | 43 | Not Used | 56 |
| 2 | 5 | 1 | 44 | 33 | 58 |
| 2 | 5 | 2 | 45 | 34 | 5A |
| 2 | 5 | 3 | 46 | 35 | 5C |
| 2 | 5 | 4 | 47 | Not Used | 5E |

Table 67: VT/VC Address Offsets

| AU-3 # | TUG-2 # | TU-1 # | VT/VC # (VT1.5/VC-11) | VT/VC # (VT2/VC-12) | Address Offset (Hex) |
|--------|---------|--------|--------------------------|------------------------|----------------------|
| 2 | 6 | 1 | 48 | 36 | 60 |
| 2 | 6 | 2 | 49 | 37 | 62 |
| 2 | 6 | 3 | 50 | 38 | 64 |
| 2 | 6 | 4 | 51 | Not Used | 66 |
| 2 | 7 | 1 | 52 | 39 | 68 |
| 2 | 7 | 2 | 53 | 40 | 6A |
| 2 | 7 | 3 | 54 | 41 | 6C |
| 2 | 7 | 4 | 55 | Not Used | 6E |
| 3 | 1 | 1 | 56 | 42 | 70 |
| 3 | 1 | 2 | 57 | 43 | 72 |
| 3 | 1 | 3 | 58 | 44 | 74 |
| 3 | 1 | 4 | 59 | Not Used | 76 |
| 3 | 2 | 1 | 60 | 45 | 78 |
| 3 | 2 | 2 | 61 | 46 | 7A |
| 3 | 2 | 3 | 62 | 47 | 7C |
| 3 | 2 | 4 | 63 | Not Used | 7E |
| 3 | 3 | 1 | 64 | 48 | 80 |
| 3 | 3 | 2 | 65 | 49 | 82 |
| 3 | 3 | 3 | 66 | 50 | 84 |
| 3 | 3 | 4 | 67 | Not Used | 86 |
| 3 | 4 | 1 | 68 | 51 | 88 |
| 3 | 4 | 2 | 69 | 52 | 8A |
| 3 | 4 | 3 | 70 | 53 | 8C |
| 3 | 4 | 4 | 71 | Not Used | 8E |
| 3 | 5 | 1 | 72 | 54 | 90 |
| 3 | 5 | 2 | 73 | 55 | 92 |
| 3 | 5 | 3 | 74 | 56 | 94 |
| 3 | 5 | 4 | 75 | Not Used | 96 |
| 3 | 6 | 1 | 76 | 57 | 98 |
| 3 | 6 | 2 | 77 | 58 | 9A |
| 3 | 6 | 3 | 78 | 59 | 9C |
| 3 | 6 | 4 | 79 | Not Used | 9E |
| 3 | 7 | 1 | 80 | 60 | A0 |
| 3 | 7 | 2 | 81 | 61 | A2 |
| 3 | 7 | 3 | 82 | 62 | A4 |
| 3 | 7 | 4 | 83 | Not Used | A6 |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 68: Tx Virtual Concatenation Block - LCAS Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|----------------|--------|--|
| 0x1ef00 – 0x1efa6 | 0 | MaTLCPRD1_x | 0x001F | LO: Tx LCAS ADD Period1 alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 1 | MaTLCASADDED_x | | LO: Tx LCAS ADD successful alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 2 | MaTLCASREM_x | | LO: Tx LCAS REMOVE successful alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 3 | MaTLCASDNU_x | | LO: Tx LCAS DNU alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 4 | MaTLCASDNUOK_x | | LO: Tx LCAS DNU OK alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| 0x1efa8 – 0x1efac | 0 | MaTLCPRD1_x | 0x001F | HO: Tx LCAS ADD Period1 alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaTLCASADDED_x | | HO: Tx LCAS ADD successful alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaTLCASREM_x | | HO: Tx LCAS REMOVE successful alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaTLCASDNU_x | | HO: Tx LCAS DNU alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaTLCASDNUOK_x | | HO: Tx LCAS DNU OK alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| 0x1efae | 7-0 | MaTLOPRD2_x | 0x00FF | Tx LO ADD Period2 alarm mask for the VCG0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1efb0 | 7-0 | MaTHOPRD2_x | 0x00FF | Tx HO ADD Period2 alarm mask for the VCG0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1efb2 | 7-0 | MaTLOPRD3_x | 0x00FF | Tx LO REMOVE Period3 alarm mask for the VCG0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1efb4 | 7-0 | MaTHOPRD3_x | 0x00FF | Tx HO REMOVE Period3 alarm mask for the VCG0-7 1: alarm is masked (default) 0: alarm is not masked |

Table 68: Tx Virtual Concatenation Block - LCAS Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|---------------------------|--------|--|
| 0x1efb6 | 0 | MaVCT_LOPRD1_Interrupt | 0x001F | LO: Interrupt mask - Tx LCAS ADD Period1 alarm 1: interrupt is masked for all Tx LCAS ADD Period1 alarms (all members) (default) 0: interrupt is not masked |
| | 1 | MaVCT_LOADEDDED_Interrupt | | LO: Interrupt mask - Tx LCAS ADD successful alarm 1: interrupt is masked for all Tx LCAS ADD alarms (all members) (default) 0: interrupt is not masked |
| | 2 | MaVCT_LOREM_Interrupt | | LO: Interrupt mask - Tx LCAS REMOVE successful alarm 1: interrupt is masked for all Tx LCAS REMOVE alarms (all members) (default) 0: interrupt is not masked |
| | 3 | MaVCT_LODNU_Interrupt | | LO: Interrupt mask -Tx LCAS DNU alarm 1: interrupt is masked for all Tx LCAS DNU alarms (all members) (default) 0: interrupt is not masked |
| | 4 | MaVCT_LODNUOK_Interrupt | | LO: Interrupt mask -Tx LCAS DNU OK alarm 1: interrupt is masked for all Tx LCAS DNU OK alarms (all members) (default) 0: interrupt is not masked |
| 0x1efb8 | 0 | MaVCT_HOPRD1_Interrupt | 0x001F | HO: Interrupt mask -Tx LCAS ADD Period1 alarm 1: interrupt is masked for all Tx LCAS ADD Period1 alarms (all members) (default) 0: interrupt is not masked |
| | 1 | MaVCT_HOADDED_Interrupt | | HO: Interrupt mask -Tx LCAS ADD successful alarm 1: interrupt is masked for all Tx LCAS ADD alarms (all members) (default) 0: interrupt is not masked |
| | 2 | MaVCT_HOREM_Interrupt | | HO: Interrupt mask -Tx LCAS REMOVE successful alarm 1: interrupt is masked for all Tx LCAS REMOVE alarms (all members) (default) 0: interrupt is not masked |
| | 3 | MaVCT_HODNU_Interrupt | | HO: Interrupt mask -Tx LCAS DNU alarm 1: interrupt is masked for all Tx LCAS DNU alarm (all members) (default) 0: interrupt is not masked |
| | 4 | MaVCT_HODNUOK_Interrupt | | HO: Interrupt mask -Tx LCAS DNU OK alarm 1: interrupt is masked for all Tx LCAS DNU OK alarm (all members) (default) 0: interrupt is not masked |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 69: Tx Virtual Concatenation Block - LCAS Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|-----------------|--------|--|
| 0x1ee00 – 0x1eea6 | 0 | L1aTLCPRD1_x | 0x0000 | LO: Tx LCAS ADD Period1 latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 1 | L1aTLCASADDED_x | | LO: Tx LCAS ADD successful latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 2 | L1aTLCASREM_x | | LO: Tx LCAS REMOVE successful latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 3 | L1aTLCASDNU_x | | LO: Tx LCAS DNU latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 4 | L1aTLCASDNUOK_x | | LO: Tx LCAS DNU OK latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| 0x1eea8 – 0x1eeac | 0 | L1aTLCPRD1_x | 0x0000 | HO: Tx LCAS ADD Period1 latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 1 | L1aTLCASADDED_x | | HO: Tx LCAS ADD successful latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 2 | L1aTLCASREM_x | | HO: Tx LCAS REMOVE successful latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 3 | L1aTLCASDNU_x | | HO: Tx LCAS DNU latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 4 | L1aTLCASDNUOK_x | | HO: Tx LCAS DNU OK latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| 0x1eeae | 7-0 | L1aTLOPRD2_x | 0x0000 | Tx LO ADD Period2 latched alarm for the VCG0-7 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| 0x1eeb0 | 7-0 | L1aTHOPRD2_x | 0x0000 | Tx HO ADD Period2 latched alarm for the VCG0-7 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| 0x1eeb2 | 7-0 | L1aTLOPRD3_x | 0x0000 | Tx LO REMOVE Period3 latched alarm for the VCG0-7 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| 0x1eeb4 | 7-0 | L1aTHOPRD3_x | 0x0000 | Tx HO REMOVE Period3 latched alarm for the VCG0-7 1: alarm is latched (clear on read) for each member 0: no alarm is latched |

Table 70: Tx Virtual Concatenation Block - LCAS Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|---------------------------|--------|--|
| 0x1ec00 | 0 | VCT_LOPRD1_Interrupt | 0x0000 | LO: Tx LCAS ADD Period1 alarm interrupt 1: interrupt for all Tx LCAS ADD Period1 alarm (all members) 0: no interrupt |
| | 1 | VCT_LOADDED_Interrupt | | LO: Tx LCAS ADD successful alarm interrupt 1: interrupt for all Tx LCAS ADD successful alarm (all members) 0: no interrupt |
| | 2 | VCT_LOREM_Interrupt | | LO: Tx LCAS REMOVE successful alarm interrupt 1: interrupt for all Tx LCAS remove successful alarm (all members) 0: no interrupt |
| | 3 | VCT_LODNU_Interrupt | | LO: Tx LCAS DNU alarm interrupt 1: interrupt for all Tx LCAS DNU alarm (all members) 0: no interrupt |
| | 4 | VCT_LODNUOK_Interrupt | | LO: Tx LCAS DNU OK alarm interrupt 1: interrupt for all Tx LCAS DNU OK alarm (all members) 0: no interrupt |
| | 5 | VCT_TXLCASLO_Interrupt | | LO: Tx LCAS alarm interrupt 1: interrupt for all Tx LCAS alarm (all members) 0: no interrupt |
| 0x1ec02 | 0 | VCT_HOPRD1_Interrupt | 0x0000 | HO: Tx LCAS ADD Period1 alarm interrupt 1: interrupt for all Tx LCAS ADD Period1 alarm (all members) 0: no interrupt |
| | 1 | VCT_HOADEDED_Interrupt | | HO: Tx LCAS ADD successful alarm interrupt 1: interrupt for all Tx LCAS ADD successful alarm (all members) 0: no interrupt |
| | 2 | VCT_HOREM_Interrupt | | HO: Tx LCAS REMOVE successful alarm interrupt 1: interrupt for all Tx LCAS REMOVE successful alarm (all members) 0: no interrupt |
| | 3 | VCT_HODNU_Interrupt | | HO: Tx LCAS DNU alarm interrupt 1: interrupt for all Tx LCAS DNU alarm (all members) 0: no interrupt |
| | 4 | VCT_HODNUOK_Interrupt | | HO: Tx LCAS DNU OK alarm interrupt 1: interrupt for all Tx LCAS DNU OK alarm (all members) 0: no interrupt |
| | 5 | VCT_TXLCASHO_Interrupt | | HO: Tx LCAS alarm interrupt 1: interrupt for all Tx LCAS alarm (all members) 0: no interrupt |
| 0x1ec04 | 0 | VCT_TXLOPRD2VCG_Interrupt | 0x0000 | Tx LO Period2 alarm interrupt 1: interrupt for all Tx LO Period2 alarm (all members) 0: no interrupt |
| | 1 | VCT_TXHOPRD2VCG_Interrupt | | Tx HO Period2 alarm interrupt 1: interrupt for all Tx HO Period2 alarm (all members) 0: no interrupt |
| 0x1ec06 | 0 | VCT_TXLOPRD3VCG_Interrupt | 0x0000 | Tx LO REMOVE Period3 alarm interrupt 1: interrupt for all Tx LO REMOVE Period3 alarm (all members) 0: no interrupt |
| | 1 | VCT_TXHOPRD3VCG_Interrupt | | Tx HO REMOVE Period3 alarm interrupt 1: interrupt for all Tx HO REMOVE Period3 alarm (all members) 0: no interrupt |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 71: Tx Virtual Concatenation Block - Low Order Tributary Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|------|------------|--------|---|
| 0x13500 – 0x135a6 | 1-0 | cTLOPOOL_x | 0x07E0 | 00: This low order tributary is assigned to a GLOBAL POOL of resources. (Default) 01: This low order tributary is assigned to a NON-LCAS POOL of resources. 10: This low order tributary is assigned to a LCAS IDLE POOL of resources. 11: This low order tributary is assigned to a LCAS ACTIVE POOL of resources. See Table 67 for per VT/VC Address Offsets. |
| | 4-2 | cTLOVCG_x | 0x07E0 | These 3 bits determine the VCG to which the select low order tributary has been assigned. Eight VCGs are available. (Default = 000). See Table 67 for per VT/VC Address Offsets. |
| | 10-5 | cTLOSQ_x | 0x07E0 | When in low order virtual concatenation, these 6 bits are used to configure/assign a sequence indicator value (i.e., SQ field) for the select low order tributary per VCG to be inserted in the extended overhead multiframe. In LCAS mode, these bits are configured only by the LCAS state machine. In non-LCAS mode, these bits are configured only by the host. (Default = 111111). See Table 67 for per VT/VC Address Offsets. |

Table 72: Tx Virtual Concatenation Block - High Order Tributary Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|------|------------|--------|--|
| 0x13400 – 0x13404 | 1-0 | cTHOPOOL_x | 0x1FE0 | 00: This high order tributary is assigned to a GLOBAL POOL of resource. (Default) 01: This high order tributary is assigned to a NON-LCAS POOL of resources. 10: This high order tributary is assigned to a LCAS IDLE POOL of resources. 11: This high order tributary is assigned to a LCAS ACTIVE POOL of resources. |
| | 4-2 | cTHOVCG_x | | These 3 bits determine the VCG to which the select high order tributary has been assigned. Eight VCGs are available. (Default=000) |
| | 12-5 | cTHOSQ_x | | When in high order virtual concatenation, these 8 bits are used to configure/assign a sequence indicator value (i.e., SQ field) for the select high order tributary per VCG to be inserted in the extended overhead multiframe. In LCAS mode, these bits are accessed only by the LCAS state machine. In non-LCAS mode, these bits are accessed only by the host. (Default = 11111111) |

Table 73: Tx Virtual Concatenation Block - LCAS Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|---------------|--------|--|
| 0x18800 – 0x188a6 | 0 | cTLOK4VCEN_x | 0x0000 | Tx LO: K4/Z7 Bit 2 enable in LCAS mode for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 See Table 74 for per VT/VC Address Offsets. |
| | 1 | cTLOCRCERR_x | | Tx LO: CRC initialization in LCAS mode for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4. A zero initializes the register to 0 for normal operation. A one initializes the register to 1 and causes CRC errors to be generated. See Table 74 for per VT/VC Address Offsets. |
| 0x188a8 – 0x188ac | 0 | cTHOH4VCEN_x | 0x0000 | Tx HO: H4 byte enable in LCAS mode for the STS-1/VC-3 1_3 |
| | 1 | cTHO_CRCERR_x | | Tx HO: CRC initialization in LCAS mode for the STS-1/VC-3 1_3. A zero initializes the register to 0 for normal operation. A one initializes the register to 1 and causes CRC errors to be generated. |
| 0x18a00 – 0x18aa6 | 9-0 | cTLOLCPRD1_x | 0x03FF | Tx LO LCAS: Terminal count of timeout counter when adding a member for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 (time unit = ms) See Table 67 for per VT/VC Address Offsets. |
| 0x18aa8 – 0x18aac | 9-0 | cTHOLCPRD1_x | 0x03FF | Tx HO LCAS: Terminal count of timeout counter when adding a member for STS-1/VC-3 1_3 (time unit = ms) |
| 0x1d7e0 – 0x1d7ee | 9-0 | cTLCPRD2_x | 0x03FF | Tx LCAS: Terminal count of timeout counter used for detection of RS_ACK after ADD for VCG0-7 (time unit = ms) |

Table 73: Tx Virtual Concatenation Block - LCAS Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|------------|--------|---|
| 0x1d200 – 0x1d20e | 9-0 | cTLCPRD3_x | 0x03FF | Tx LCAS: Terminal count of timeout counter used for detection of RS_ACK after REM for VCG0-7 (time unit = ms) |

Table 74: VT/VC Address Offsets (cTLOK4VCEN_x and cTLOCRCERR_x Only)

| AU-3 # | TUG-2 # | TU-1 # | VT/VC # (VT1.5/VC-11) | VT/VC # (VT2/VC-12) | Address Offset (Hex) |
|--------|---------|--------|--------------------------|------------------------|----------------------|
| 1 | 1 | 1 | 0 | 0 | 00 |
| 1 | 1 | 2 | 1 | 1 | 2A |
| 1 | 1 | 3 | 2 | 2 | 54 |
| 1 | 1 | 4 | 3 | Not Used | 7E |
| 1 | 2 | 1 | 4 | 3 | 06 |
| 1 | 2 | 2 | 5 | 4 | 30 |
| 1 | 2 | 3 | 6 | 5 | 5A |
| 1 | 2 | 4 | 7 | Not Used | 84 |
| 1 | 3 | 1 | 8 | 6 | 0C |
| 1 | 3 | 2 | 9 | 7 | 36 |
| 1 | 3 | 3 | 10 | 8 | 60 |
| 1 | 3 | 4 | 11 | Not Used | 8A |
| 1 | 4 | 1 | 12 | 9 | 12 |
| 1 | 4 | 2 | 13 | 10 | 3C |
| 1 | 4 | 3 | 14 | 11 | 66 |
| 1 | 4 | 4 | 15 | Not Used | 90 |
| 1 | 5 | 1 | 16 | 12 | 18 |
| 1 | 5 | 2 | 17 | 13 | 42 |
| 1 | 5 | 3 | 18 | 14 | 6C |
| 1 | 5 | 4 | 19 | Not Used | 96 |
| 1 | 6 | 1 | 20 | 15 | 1E |
| 1 | 6 | 2 | 21 | 16 | 48 |
| 1 | 6 | 3 | 22 | 17 | 72 |
| 1 | 6 | 4 | 23 | Not Used | 9C |
| 1 | 7 | 1 | 24 | 18 | 24 |
| 1 | 7 | 2 | 25 | 19 | 4E |
| 1 | 7 | 3 | 26 | 20 | 78 |
| 1 | 7 | 4 | 27 | Not Used | A2 |
| 2 | 1 | 1 | 28 | 21 | 02 |
| 2 | 1 | 2 | 29 | 22 | 2C |
| 2 | 1 | 3 | 30 | 23 | 56 |
| 2 | 1 | 4 | 31 | Not Used | 80 |
| 2 | 2 | 1 | 32 | 24 | 08 |
| 2 | 2 | 2 | 33 | 25 | 32 |
| 2 | 2 | 3 | 34 | 26 | 5C |
| 2 | 2 | 4 | 35 | Not Used | 86 |
| 2 | 3 | 1 | 36 | 27 | 0E |
| 2 | 3 | 2 | 37 | 28 | 38 |
| 2 | 3 | 3 | 38 | 29 | 62 |
| 2 | 3 | 4 | 39 | Not Used | 8C |
| 2 | 4 | 1 | 40 | 30 | 14 |
| 2 | 4 | 2 | 41 | 31 | 3E |
| 2 | 4 | 3 | 42 | 32 | 68 |
| 2 | 4 | 4 | 43 | Not Used | 92 |
| 2 | 5 | 1 | 44 | 33 | 1A |
| 2 | 5 | 2 | 45 | 34 | 44 |
| 2 | 5 | 3 | 46 | 35 | 6E |
| 2 | 5 | 4 | 47 | Not Used | 98 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 74: VT/VC Address Offsets (cTLOK4VCEN_x and cTLOCRCERR_x Only)

| AU-3 # | TUG-2 # | TU-1 # | VT/VC # (VT1.5/VC-11) | VT/VC # (VT2/VC-12) | Address Offset (Hex) |
|--------|---------|--------|--------------------------|------------------------|----------------------|
| 2 | 6 | 1 | 48 | 36 | 20 |
| 2 | 6 | 2 | 49 | 37 | 4A |
| 2 | 6 | 3 | 50 | 38 | 74 |
| 2 | 6 | 4 | 51 | Not Used | 9E |
| 2 | 7 | 1 | 52 | 39 | 26 |
| 2 | 7 | 2 | 53 | 40 | 50 |
| 2 | 7 | 3 | 54 | 41 | 7A |
| 2 | 7 | 4 | 55 | Not Used | A4 |
| 3 | 1 | 1 | 56 | 42 | 04 |
| 3 | 1 | 2 | 57 | 43 | 2E |
| 3 | 1 | 3 | 58 | 44 | 58 |
| 3 | 1 | 4 | 59 | Not Used | 82 |
| 3 | 2 | 1 | 60 | 45 | 0A |
| 3 | 2 | 2 | 61 | 46 | 34 |
| 3 | 2 | 3 | 62 | 47 | 5E |
| 3 | 2 | 4 | 63 | Not Used | 88 |
| 3 | 3 | 1 | 64 | 48 | 10 |
| 3 | 3 | 2 | 65 | 49 | 3A |
| 3 | 3 | 3 | 66 | 50 | 64 |
| 3 | 3 | 4 | 67 | Not Used | 8E |
| 3 | 4 | 1 | 68 | 51 | 16 |
| 3 | 4 | 2 | 69 | 52 | 40 |
| 3 | 4 | 3 | 70 | 53 | 6A |
| 3 | 4 | 4 | 71 | Not Used | 94 |
| 3 | 5 | 1 | 72 | 54 | 1C |
| 3 | 5 | 2 | 73 | 55 | 46 |
| 3 | 5 | 3 | 74 | 56 | 70 |
| 3 | 5 | 4 | 75 | Not Used | 9A |
| 3 | 6 | 1 | 76 | 57 | 22 |
| 3 | 6 | 2 | 77 | 58 | 4C |
| 3 | 6 | 3 | 78 | 59 | 76 |
| 3 | 6 | 4 | 79 | Not Used | A0 |
| 3 | 7 | 1 | 80 | 60 | 28 |
| 3 | 7 | 2 | 81 | 61 | 52 |
| 3 | 7 | 3 | 82 | 62 | 7C |
| 3 | 7 | 4 | 83 | Not Used | A6 |

Table 75: Tx Virtual Concatenation Block - Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------------------|------|------------|-------------------|---|
| 0x18c00 – 0x18ca6 | 1-0 | sTLOPOOL_x | Not Applicable | 00: Indicates low order tributary is assigned to the GLOBAL POOL of resources. 01: Indicates low order tributary is assigned to the NON-LCAS POOL of resources. 10: Indicates low order tributary is assigned to the LCAS IDLE POOL of resources. 11: Indicates low order tributary is assigned to the LCAS ACTIVE POOL of resources. See Table 67 for per VT/VC Address Offsets. |
| | 4-2 | sTLOVCG_x | | When in low order virtual concatenation, indicates to which VCG the low order tributary has been assigned. Only eight VCGs are available. See Table 67 for per VT/VC Address Offsets. |
| | 8-5 | sTLOCTRL_x | | When in low order virtual concatenation, indicates the status of tributary state (i.e., the CTRL field transmitted) in both LCAS and non-LCAS modes. See Table 67 for per VT/VC Address Offsets. |
| | 14-9 | sTLOSQ_x | | When in low order virtual concatenation, indicates the status of the assigned SEQUENCE INDICATOR value for the select low order tributary per VCG. See Table 67 for per VT/VC Address Offsets. |
| 0x18ca8 0x18cac 0x18cb0 | 7-0 | sTHOSQ_x | 0x0000 | When in high order virtual concatenation, indicates the assigned SEQUENCE INDICATOR (SQ) value for the select high order tributary per VCG. |
| 0x18caa 0x18cae 0x18cb2 | 1-0 | sTHOPOOL_x | 0x0000 | 00: Indicates high order tributary is assigned to a GLOBAL POOL of resources. 01: Indicates high order tributary is assigned to a NON-LCAS POOL of resources. 10: Indicates high order tributary is assigned to a LCAS IDLE POOL of resources. 11: Indicated high order tributary is assigned to a LCAS ACTIVE POOL of resources. |
| | 4-2 | sTHOVCG_x | | When in high order virtual concatenation, indicates to which VCG the high order tributary has been assigned. Only eight VCGs are available. |
| | 8-5 | sTHOCTRL_x | | When in high order virtual concatenation, indicates the status of tributary state (i.e., the CTRL field transmitted) in both LCAS and non-LCAS modes. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

RX VIRTUAL CONCATENATION REGISTERS

Tables 76 through 85 - Configuration, Status and Alarm of the Receive (SONET to Ethernet) Virtual Concatenation Block

Table 76: Rx Virtual Concatenation Block - General Configuration Registers (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1f000 | 1-0 | cINRT_GRPRX20M | 0x0001 | Alarm latching configuration for Receive LCAS alarm group (Table 79) Criteria used to create latched alarms from the raw (unlatched) alarms. 00: positive level 01: rising edge (default) 10: falling edge 11: rising or falling edge |
| 0x1f002 | 0 | HINTEN | 0x0000 | Enable of the interrupt signal 0: general interrupt signal is disabled 1: general interrupt is enabled |
| 0x1f004 | 1-0 | cRHOVC3_3 | 0x0000 | Rx VCAT: STS-1/VC-3 #3 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #3 is used in low order to carry selected VT1.5/VC-11 01: AU-3 C is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #3 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #3 is used in low order to carry VT-2/VC-12 01: AU-3 C is used to carry VT2/VC-12 10: Reserved 11: STS-1/TUG-3 #3 (with its TU-3/VC-3) is used in high order |
| | 3-2 | cRHOVC3_2 | | Rx VCAT: STS-1/VC-3 #2 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #2 is used in low order to carry selected VT1.5/VC-11 01: AU-3 B is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #2 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #2 is used in low order to carry VT-2/VC-12 01: AU-3 B is used to carry VT2/VC-12 10: Reserved 11: STS-1/TUG-3 #2 (with its TU-3/VC-3) is used in high order |
| | 5-4 | cRHOVC3_1 | | Rx VCAT: STS-1/VC-3 #1 configuration <u>cSNTSDH = '0'</u> 00: STS-1/TUG-3 #1 is used in low order to carry selected VT1.5/VC-11 01: AU-3 A is used to carry VT1.5/VC-11 10: Reserved 11: STS-1/TUG-3 #1 (with its STS-1SPE / VC-3) is used in high order <u>cSNTSDH = '1'</u> 00: STS-1/TUG-3 #1 is used in low order to carry VT-2/VC-12 01: AU-3 A is used to carry VT2/VC-12 10: Reserved 11: STS-1/TUG-3 #1 (with its TU-3/VC-3) is used in high order |
| | 6 | cRHOVC4 | | Rx VCAT: STS3c/VC-4 configuration 0: Configured for non VC-4/STS-3c mode (i.e., when using sub-structured containers/tributaries) 1: Configured for VC-4/STS-3c mode |

Table 76: Rx Virtual Concatenation Block - General Configuration Registers (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|--------------|--------|--|
| 0x1f006 | 7-0 | cRVC4MAC | 0x0000 | Rx VCAT: 10/100 port to extract data from VC-4/STS3c bit mapped register to indicate the MAC associated to the VC-4/STS-3c in case of configuration in VC-4/STS-3c. bit 0 is associated to port 1 bit 7 is associated to port 8 Only a single bit of this register may be set to 1. |
| 0x1f008 – 0x1f016 | 1-0 | cRVCG_x | 0x0000 | Rx: VCG0-7 configuration 00: VCG used in ITU/ANSI low order virtual concatenation 01: VCG used in non standard ITU/ANSI low order virtual concatenation and in non LCAS 10: Reserved 11: VCG used in ITU/ANSI high order virtual concatenation |
| | 2 | cRLCAS_x | | Rx: LCAS/NON LCAS configuration for the VCG0-7 0: VCG in non LCAS mode 1: VCG in LCAS mode |
| | 5-3 | TX_VCG_x | | Rx: VCG0-7 to carry the MST_OK Used in LCAS mode only Number of VCG which carry the MST |
| | 6 | cRLCCRCRST_x | | LCAS CRC reset value for VCG0-7 |
| 0x1f018 – 0x1f026 | 9-0 | rMAXDELVCG_x | 0x0200 | Maximum differential delay value for the VCG0-7 <u>In low order:</u> 3 MSB bits represent the max allowed value of differential delay by step of 16 ms 000: 0 ms 001: 16 ms 010: 32 ms (default) 011: 48 ms <u>In high order:</u> All 10 bits are used to represent the max allowed value of differential delay by step of 125 µs. 0x0000: 0 ms 0x0001: 125 µs ... 0x0180: 48 ms |
| 0x1f028 | 0 | cRFREEZEMFI | 0x0000 | Freeze the multiFrame-count registers to their current value. 0: MultiFrame-count status registers are continuously updated with the value received in the multiFrame. 1: MultiFrame-count status registers are not internally updated. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 77: Rx Virtual Concatenation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----------|-----------------|--------|--|
| 0x1f100 – 0x1f1a6 | 0 | aLOSQM_x | 0x0000 | Rx LO: Loss of Sequence Indicator for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: The received debounced sequence indicator (RLOACSQx) does not match the expected SQ value (cRLOSQ register) in non LCAS mode. If the N incoming tributaries have sequence indicators ordered from 0 to N-1, the decapsulation block will still pass traffic even if this alarm is asserted. Cleared on matching SQ value. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 1 | aRLOLCSCRCE_x | | Rx LO: LCAS CRC error for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: The received frame has error in CRC in LCAS mode only. Cleared on matching CRC value. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 2 | aRLOLCASADDED_x | | Rx LO: LCAS ADD successful for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: A member was successfully added to the OK state. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 3 | aRLOLCASFAIL_x | | Rx LO: LCAS FAIL alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: A defect condition occurred and the member goes from OK to FAIL. 0: no alarm See Table 67 for per VT/VC Address Offsets. |
| | 4 | aRLOLCASREM_x | | Rx LO: LCAS REMOVE successful for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 See Table 67 for per VT/VC Address Offsets. |
| 0x1f1a8 – 0x1f1ac | 0 | aHOSQM_x | 0x0000 | Rx HO: Loss of Sequence Indicator for the STS-1/VC-3 1_3 1: The received debounced SQ (RHOACSQx) does not match with the expected SQ value (cRHOSQ register) in non LCAS mode. Cleared on matching SQ value. 0: no alarm |
| | 1 | aRHOLCSCRCE_x | | Rx HO: LCAS CRC error for the STS-1/VC-3 1_3 1: The received frame has error in CRC in LCAS mode only. Cleared on matching CRC value. 0: no alarm |
| | 2 | aRHOLCASADDED_x | | Rx HO: LCAS ADD successful for the STS-1/VC-3 1_3 1: A member was successfully added to the OK state. 0: no alarm |
| | 3 | aRHOLCASFAIL_x | | Rx HO: LCAS FAIL alarm for the STS-1/VC-3 1_3 1: A defect condition occurred and the member goes from OK to FAIL. 0: no alarm |
| | 4 | aRHOLCASREM_x | | Rx HO: LCAS REMOVE successful for the STS-1/VC-3 1_3 1: A member is successfully removed and goes to the IDLE state. 0: no alarm |
| 0x1f1ae | even bits | aHOLOA_x | 0x0000 | Rx HO: Group Loss of Alignment for VCG0 (bit 0) through VCG7 (bit 14) 1: Differential delay calculated over received members of VCGx exceeds rMAXDELVCGx. 0: Differential delay calculated over received members of VCGx does not exceed rMAXDELVCGx. |
| | odd bits | aHOLOA_AlVT_x | | Rx HO: Global LOA for VCG0 (bit 1) through VCG7 (bit 15) 1: Differential delay calculated over all received containers exceeds rMAXDELVCGx. 0: Differential delay calculated over all received containers does not exceed rMAXDELVCGx. |

Table 77: Rx Virtual Concatenation Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----------|----------------|--------|--|
| 0x1f1b0 | even bits | aLOLOA_x | 0x0000 | Rx LO: Group Loss of Alignment for VCG0 (bit 0) through VCG7 (bit 14) Indicates if payload carrying members of a VCG (CTRL is NORM or EOS) have differential delay larger than the limit configured by rMAXDELVCG. 1: Differential delay for VCGx exceeds limit. 0: Differential delay for VCGx does not exceed limit. |
| | odd bits | aLOLOA_AIIVT_x | | Rx LO: Global LOA for VCG0 (bit 1) through VCG7 (bit 15) Indicates if all members associated with a VCG (including members carrying ADD, DNU or IDLE) have differential delay larger than the limit configured by rMAXDELVCG. 1: Differential delay for VCGx exceeds limit. 0: Differential delay for VCGx does not exceed limit. |
| 0x1f1b2 | 7-0 | aRXFIFO_x | 0x0000 | Rx FIFO overflow for the VCG0-7 1: The SDRAM FIFO is in overflow state (not in VC-4 mode). 0: no overflow (not in VC-4 mode) |
| 0x1f1b4 | 7-0 | aRHOLCASGIDM_x | 0x0000 | Rx HO: GID mismatch alarm for VCG0-7 |
| 0x1f1b6 | 7-0 | aRLOLCASGIDM_x | 0x0000 | Rx LO: GID mismatch alarm for VCG0-7 |

Table 78: Rx Virtual Concatenation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----|------------------|--------|--|
| 0x1f300 – 0x1f3a6 | 0 | MaLOSQM_x | 0x001F | Rx LO: Loss of Sequence Indicator alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 1 | MaRLOLCSCRCE_x | | Rx LO: LCAS CRC error alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 2 | MaRLOLCASADDED_x | | Rx LO: LCAS ADD successful alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 3 | MaRLOLCASFAIL_x | | Rx LO: LCAS FAIL alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |
| | 4 | MaRLOLCASREM_x | | Rx LO: LCAS REMOVE successful alarm mask for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is masked (default) 0: alarm is not masked See Table 67 for per VT/VC Address Offsets. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 78: Rx Virtual Concatenation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----------|------------------|--------|---|
| 0x1f3a8 – 0x1f3ac | 0 | MaHOSQM_x | 0x001F | Rx HO: loss of Sequence Indicator alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 1 | MaRHOLCSCRCE_x | | Rx HO: LCAS CRC error alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 2 | MaRHOLCASADDED_x | | Rx HO: LCAS ADD successful alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 3 | MaRHOLCASFAIL_x | | Rx HO: LCAS FAIL alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| | 4 | MaRHOLCASREM_x | | Rx HO: LCAS REMOVE successful alarm mask for the STS-1/VC-3 1_3 1: alarm is masked (default) 0: alarm is not masked |
| 0x1f3ae | even bits | MaHOLOA_x | 0xFFFF | Rx HO: Group LOA alarm mask for VCG0 (bit 0) - VCG7 (bit 14) 1: alarm is masked (default) 0: alarm is not masked |
| | odd bits | MaHOLOA_AIIVT_x | | Rx HO: Global LOA alarm mask for VCG0 (bit 1) - VCG7 (bit 15) 1: alarm is masked (default) 0: alarm is not masked |
| 0x1f3b0 | even bits | MaLOLOA_x | 0xFFFF | Rx LO: Group LOA alarm mask for VCG0 (bit 0) - VCG7 (bit 14) 1: alarm is masked (default) 0: alarm is not masked |
| | odd bits | MaLOLOA_AIIVT_x | | Rx LO: Global LOA alarm mask for VCG0 (bit 1) - VCG7 (bit 15) 1: alarm is masked (default) 0: alarm is not masked |
| 0x1f3b2 | 7-0 | MaRXFIFO_x | 0x00FF | Rx FIFO overflow alarm mask for the VCG 0_7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1f3b4 | 7-0 | MaRHOLCASCIDM_x | 0x00FF | Rx HO: GID mismatch alarm mask for the VCG 0_7 |
| 0x1f3b6 | 7-0 | MaRLOLCASCIDM_x | 0x00FF | Rx LO: GID mismatch alarm mask for the VCG 0_7 |

Table 78: Rx Virtual Concatenation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------|--------|---|
| 0x1f3b8 | 0 | MaVCR_LOSQM_Interrupt | 0x00FF | Rx LO Loss of sequence indicator alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 1 | MaVCR_LOCRCE_Interrupt | | Rx LO: LCAS CRC error alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 2 | MaVCR_LOADDED_Interrupt | | Rx LO: LCAS ADD successful alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 3 | MaVCR_LOFAIL_Interrupt | | Rx LO: LCAS FAIL alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 4 | MaVCR_LOREM_Interrupt | | Rx LO: LCAS REMOVE successful alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 5 | MaVCR_RXLCASLO_Interrupt | | Rx LO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 6 | MaVCT_TXLCASLO_Interrupt | | Tx LO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 7 | MaRXTXLCASLO_Interrupt | | Rx/TX LO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3ba | 0 | MaVCR_HOSQM_Interrupt | 0x00FF | Rx HO Loss of sequence indicator alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 1 | MaVCR_HOCRCE_Interrupt | | Rx HO: LCAS CRC error alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 2 | MaVCR_HOADDED_Interrupt | | Rx HO: LCAS ADD successful alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 3 | MaVCR_HOFAIL_Interrupt | | Rx HO: LCAS FAIL alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 4 | MaVCR_HOREM_Interrupt | | Rx HO: LCAS REMOVE successful alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 5 | MaVCR_RXLCASHO_Interrupt | | Rx HO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 6 | MaVCT_TXLCASHO_Interrupt | | Tx HO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 7 | MaRXTXLCASHO_Interrupt | | Rx/TX HO LCAS alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 78: Rx Virtual Concatenation Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------------------|--------|--|
| 0x1f3bc | 0 | MaVCR_LOLOA_Interrupt | 0x001F | Rx LO loss of alignment alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 1 | MaVCR_LOLCASGIDM_Interrupt | | Rx LO GID mismatch alarm interrupt mask |
| | 2 | MaVCT_TXLOPRD2VCG_Interrupt | | Tx LO PRD2 VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 3 | MaVCT_TXLOPRD3VCG_Interrupt | | Tx LO PRD3 VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 4 | MaVCR_LOVCG_Interrupt | | Rx/Tx LO VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3be | 0 | MaVCR_HOLOA_Interrupt | 0x001F | Rx HO loss of alignment alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 1 | MaVCR_HOLCASGIDM_Interrupt | | Rx HO GID mismatch alarm interrupt mask |
| | 2 | MaVCT_TXHOPRD2VCG_Interrupt | | Tx HO PRD2 VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 3 | MaVCT_TXHOPRD3VCG_Interrupt | | Tx HO PRD3 VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| | 4 | MaVCR_HOVCG_Interrupt | | Rx/Tx HO VCG alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3c0 | 0 | MaVCR_RXFIFO_Interrupt | 0x0001 | Rx FIFO overflow alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3c2 | 0 | MaRXTXLO_Interrupt | 0x0001 | Rx/Tx LO alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3c4 | 0 | MaRXTXHO_Interrupt | 0x0001 | Rx/Tx HO alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |
| 0x1f3c6 | 0 | MaRXTXHOLO_Interrupt | 0x0001 | Rx/Tx HO/LO alarm interrupt mask 1: interrupt is masked (default) 0: interrupt is not masked |

Table 79: Rx Virtual Concatenation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|-----------|-------------------|--------|--|
| 0x1f200 – 0x1f2a6 | 0 | L1aLOSQM_x | 0x0000 | Rx LO: Loss of Sequence Indicator latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 1 | L1aRLOLCSCRCE_x | | Rx LO: LCAS CRC error latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 2 | L1aRLOLCASADDED_x | | Rx LO: LCAS ADD successful latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 3 | L1aRLOLCASFAIL_x | | Rx LO: LCAS FAIL latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| | 4 | L1aRLOLCASREM_x | | Rx LO: LCAS remove successful latched alarm for the STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 1: alarm is latched (clear on read) for each member 0: no alarm is latched See Table 67 for per VT/VC Address Offsets. |
| 0x1f2a8 – 0x1f2ac | 0 | L1aHOSQM_x | 0x0000 | Rx HO: Loss of Sequence Indicator latched alarm for the STS-1/VC-3 1_3, TUG-2 8 and TU-1 5 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 1 | L1aRHOLCSCRCE_x | | Rx HO: LCAS CRC error latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 2 | L1aRHOLCASADDED_x | | Rx HO: LCAS ADD successful latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 3 | L1aRHOLCASFAIL_x | | Rx HO: LCAS FAIL latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| | 4 | L1aRHOLCASREM_x | | Rx HO: LCAS REMOVE successful latched alarm for the STS-1/VC-3 1_3 1: alarm is latched (clear on read) for each member 0: no alarm is latched |
| 0x1f2ae | even bits | L1aHOLOA_x | 0x0000 | Rx HO Group Loss of alignment latched alarm for VCG0 (bit 0) - VCG7 (bit 14) 1: alarm is latched (clear on read) for each VCG 0: no alarm is latched |
| | odd bits | L1aHOLOA_AIIVT_x | | Rx HO Global Loss of alignment latched alarm for VCG0 (bit 1) - VCG7 (bit 15) 1: alarm is latched (clear on read) for each VCG 0: no alarm is latched |
| 0x1f2b0 | even bits | L1aLOLOA_x | 0x0000 | Rx LO Group Loss of alignment latched alarm for VCG0 (bit 0) - VCG7 (bit 14) 1: alarm is latched (clear on read) for each VCG 0: no alarm is latched |
| | odd bits | L1aLOLOA_AIIVT_x | | Rx LO Global Loss of alignment latched alarm for VCG0 (bit 1) - VCG7 (bit 15) 1: alarm is latched (clear on read) for each VCG 0: no alarm is latched |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 79: Rx Virtual Concatenation Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x1f2b2 | 7-0 | L1aRXFIFO_x | 0x00FF | Rx FIFO overflow latched alarm for the VCG0-7 (not in VC-4 mode) 1: alarm is latched (clear on read) for each VCG 0: no alarm is latched |
| 0x1f2b4 | 7-0 | L1aRHOLCASGIDM_x | 0x0000 | Rx HO: GID mismatch latched alarm for the VCG0-7 |
| 0x1f2b6 | 7-0 | L1aRLOLCASGIDM_x | 0x0000 | Rx LO: GID mismatch latched alarm for the VCG0-7 |

Table 80: Rx Virtual Concatenation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------------|--------|---|
| 0x1f080 | 0 | VCR_LOSQM_Interrupt | 0x0000 | Rx LO loss of sequence indicator alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 1 | VCR_LOCRCE_Interrupt | | Rx LO LCAS CRC error alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 2 | VCR_LOADDED_Interrupt | | Rx LO LCAS ADD successful alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 3 | VCR_LOFAIL_Interrupt | | Rx LO LCAS FAIL alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 4 | VCR_LOREM_Interrupt | | Rx LO LCAS REMOVE successful alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 5 | VCR_RXLCASLO_Interrupt | | Rx LCAS LO alarm interrupt 1: interrupt for all alarms in Low order in Rx and for all members 0: no interrupt |
| | 6 | RXTXLCASLO_Interrupt | | Rx/Tx LCAS LO alarm interrupt 1: interrupt for all alarms in Low order in Rx and Tx and for all members 0: no interrupt |
| 0x1f082 | 0 | VCR_HOSQM_Interrupt | 0x0000 | Rx HO loss of sequence indicator alarm interrupt |
| | 1 | VCR_HOCRCE_Interrupt | | Rx HO LCAS CRC error alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 2 | VCR_HOADEDED_Interrupt | | Rx HO LCAS ADD successful alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 3 | VCR_HOFAIL_Interrupt | | Rx HO LCAS FAIL alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 4 | VCR_HOREM_Interrupt | | Rx HO LCAS REMOVE successful alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 5 | VCR_RXLCASHO_Interrupt | | Rx HO LCAS alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 6 | RXTXLCASHO_Interrupt | | Rx/Tx LCAS HO alarm interrupt 1: interrupt for all members 0: no interrupt |

Table 80: Rx Virtual Concatenation Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------|--------|--|
| 0x1f084 | 0 | VCR_LOLOA_Interrupt | 0x0000 | Rx LO loss of alignment alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 1 | VCR_HOLOA_Interrupt | | Rx HO loss of alignment alarm interrupt 1: interrupt for all members 0: no interrupt |
| | 2 | VCR_LOLCASGIDM_Interrupt | | Rx LO GID mismatch alarm interrupt |
| | 3 | VCR_HOLCASGIDM_Interrupt | | Rx HO GID mismatch alarm interrupt |
| | 4 | VCR_LOVCG_Interrupt | | Rx LO VCG alarm interrupt 1: interrupt for all VCG 0: no interrupt |
| | 5 | VCR_HOVCG_Interrupt | | Rx HO VCG alarm interrupt 1: interrupt for all VCG 0: no interrupt |
| 0x1f086 | 0 | VCR_RXFIFO_Interrupt | 0x0000 | Rx FIFO overflow alarm interrupt 1: interrupt for all Rx FIFO overflow alarms (not in VC-4 mode) 0: no interrupt |
| 0x1f088 | 0 | RXTXHO_Interrupt | 0x0000 | Rx/TX LCAS HO alarm interrupt 1: interrupt for all RX and Tx LCAS High order alarms 0: no interrupt |
| 0x1f08a | 0 | RXTXLO_Interrupt | 0x0000 | Rx/Tx LO alarm interrupt 1: interrupt for all RX/TX LCAS Low order alarms 0: no interrupt |
| 0x1f08c | 0 | RXTXHOLO_Interrupt | 0x0000 | Rx/Tx LO/HO alarm interrupt 1: interrupt for all RX and Tx LCAS High order and low order alarms 0: no interrupt |
| 0x1f08e | 0 | RXTXConc_Interrupt | 0x0000 | Rx/TX virtual concatenation alarm interrupt 1: interrupt for all alarms in Virtual concatenation Rx and Tx 0: no interrupt |

Table 81: Rx Virtual Concatenation Block - Low Order Tributary Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|------|----------------|--------|---|
| 0x13900 – 0x139a6 | 1-0 | cRLOPOOL_x | 0x07E0 | 00: This low order tributary is assigned to a GLOBAL POOL of resources. (Default) 01: This low order tributary is assigned to a NON-LCAS POOL of resources. 10: This low order tributary is assigned to a LCAS IDLE POOL of resources. 11: This low order tributary is assigned to a LCAS ACTIVE POOL of resources. See Table 67 for per VT/VC Address Offsets. |
| | 4-2 | cRLOVCG_x | 0x07E0 | These 3 bits determine the VCG to which the select low order tributary has been assigned. Only eight VCGs are available. (Default = 000). See Table 67 for per VT/VC Address Offsets. |
| | 10-5 | cRLOSQ_x | 0x07E0 | When in low order virtual concatenation, these 6 bits are used to configure/assign a SEQUENCE INDICATOR value for the select low order tributary per VCG. In LCAS mode, these bits are accessed only by the LCAS state machine. In non-LCAS mode, these bits are accessed only by the host. (Default = 111111). See Table 67 for per VT/VC Address Offsets. |
| | 11 | cRLOFMSTFAIL_x | 0x07E0 | Rx LO configuration for the Rx STS-1/VC-3 1, TUG-2 1 and TU-1 1: LCAS MST force FAIL option. See Table 67 for per VT/VC Address Offsets. |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 82: Rx Virtual Concatenation Block - High Order Tributary Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|-------------------------------|------|----------------|--------|--|
| 0x13800 0x13802 0x13804 | 1-0 | cRHOPOOL_x | 0x1FE0 | 00: This high order tributary is assigned to a GLOBAL POOL of resources. (Default) 01: This high order tributary is assigned to a NON-LCAS POOL of resources. 10: This high order tributary is assigned to a LCAS IDLE POOL of resources. 11: This high order tributary is assigned to a LCAS ACTIVE POOL of resources. |
| | 4-2 | cRHOVCG_x | | These 3 bits determine the VCG to which the select high order tributary has been assigned. Only eight VCGs are available. (Default=000) |
| | 12-5 | cRHOSQ_x | | Rx HO configuration per STS-1/VC-3 1: Sequence indicator configuration |
| | 13 | cRHOFMSTFAIL_x | | Rx HO configuration per STS-1/VC-3 1: LCAS MST force FAIL option |

Table 83: Rx Virtual Concatenation Block - Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------------------|------|-------------|--------|---|
| 0x18e00 – 0x18ea6 | 1-0 | sRLOPOOL_x | 0x0000 | 00: Indicates low order tributary is assigned to the GLOBAL POOL of resources. 01: Indicates low order tributary is assigned to the NON-LCAS POOL of resources. 10: Indicates low order tributary is assigned to the LCAS IDLE POOL of resources. 11: Indicates low order tributary is assigned to the LCAS ACTIVE POOL of resources. See Table 67 for per VT/VC Address Offsets. |
| | 4-2 | sRLOVCG_x | | When in low order virtual concatenation, indicates to which VCG the low order tributary has been assigned. Only eight VCGs are available. See Table 67 for per VT/VC Address Offsets. |
| | 8-5 | sRLOCTRL_x | | When in low order virtual concatenation, indicates the state of received control word (i.e., CTRL field), for the member, in both LCAS and non-LCAS modes extracted from the extended overhead multiframe. If member is not provisioned or during a SONET fail event, this register field is not updated. See Table 67 for per VT/VC Address Offsets. |
| | 14-9 | sRLOSQ_x | | When in low order virtual concatenation, indicates the state of the received sequence indicator value (i.e., SQ field) for the member and extracted from the extended overhead multiframe. If member is not provisioned or during a Sonet fail event, this register field is not updated See Table 67 for per VT/VC Address Offsets. |
| 0x18ea8 0x18eac 0x18eb0 | 7-0 | sRHOSQ_x | 0x0000 | When in high order virtual concatenation, indicates the assigned SEQUENCE INDICATOR (SQ) value for the select high order tributary per VCG. During a SONET/SDH fail event, this register field is not updated. |
| 0x18eaa 0x18eae 0x18eb2 | 1-0 | sRHOPOOL_x | 0x0000 | 00: Indicates high order tributary is assigned to a GLOBAL POOL of resources. 01: Indicates high order tributary is assigned to a NON-LCAS POOL of resources. 10: Indicates high order tributary is assigned to a LCAS IDLE POOL of resources. 11: Indicated high order tributary is assigned to a LCAS ACTIVE POOL of resources. |
| | 4-2 | sRHOVCG_x | | When in high order virtual concatenation, indicates to which VCG the high order tributary has been assigned. Only eight VCGs are available. |
| | 8-5 | sRHOCCTRL_x | | When in high order virtual concatenation, indicates the state of received control word (i.e., CTRL field), for the member, in both LCAS and non-LCAS modes. If member is not provisioned or during a Sonet fail event, this register field is not updated. |

Table 84: Rx Virtual Concatenation Block - Frame Counter Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|------|------------|--------|--|
| 0x19000 – 0x190a6 | 4-0 | sRLOMFI_x | 0x0000 | Rx LO status of the MFI for STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 in low order (range 0 to 31) See Table 67 for per VT/VC Address Offsets. |
| | 9-5 | sRLOFC_x | | Rx LO status of the Frame count for STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 in low order (range 0 to 31) See Table 67 for per VT/VC Address Offsets. |
| 0x190a8 – 0x190ac | 3-0 | sRHOMFI1_x | 0x0000 | Rx HO status of the MFI1 field for STS-1/VC-3 1_3 (range 0 to 15) |
| | 11-4 | sRHOMFI2_x | | Rx HO status of the MFI2 field for STS-1/VC-3 1_3 (range 0 to 255) |

Table 85: Rx Virtual Concatenation Block - Differential Delay Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|-------------------|------|--------------|--------|---|
| 0x19200 – 0x192a6 | 5-0 | rRLOACSQ_x | 0x0000 | Rx LO recovered Sequence Indicator value for STS-1/VC-3 1_3, TUG-2 1_7 and TU-1 1_4 Value of the SQ indicator after debounce filter, to be compared with the expected SQ value See Table 67 for per VT/VC Address Offsets. |
| 0x192a8 – 0x192ac | 7-0 | rRHOACSQ_x | 0x0000 | Rx HO recovered sequence indicator value for STS-1/VC-3 1_3 Value of the SQ indicator after debounce filter, to be compared with the expected SQ value |
| 0x192ae – 0x192bc | 11-0 | rDIFDELVCG_x | 0x0000 | Rx differential delay for the VCG 0_7 Value of the calculated differential delay per VCG until 128 ms in LO and HO. <u>Low order</u> 4 LSB bits from 0000 to 1000, by step of 16 ms 0000: 0 ms 0001: 16 ms ... 0111: 112 ms 1000: 128 ms <u>High order</u> 11 LSB bits (from 0x000 to 0x400) are used by step of 125 µs but with a maximum value of 128 ms. |



ETHERNET TO SONET HANDLING REGISTERS

Tables 86 through 90 - Configuration and Status of the Ethernet Frame Format Block (Output of the Ethernet MAC)

Table 86: Ethernet Frame Format Block - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|----------------------|-----|-----------------|--------|--|
| 0x1d6a0 | 7-0 | cTFCMODE | 0x0000 | Full Duplex mode: Pause Frame filtering in the Ethernet-to-SONET direction for MACs 0-7. Regardless of whether received Pause Frames are used to stop outgoing Ethernet traffic, this bit determines if Pause Frames are passed on to SONET/SDH. 1: Pause Frames are passed on to SONET 0: Pause Frames are dropped after the MAC Block (not encapsulated) |
| 0x1d6a2 | 1-0 | cINRT_GRP125M | 0x0001 | Alarm latching configuration for the physical block 125MHz |
| 0x1d6a4 – 0x1d6b2 | 0 | cRXTMODEx (0-7) | 0x0000 | Rx encapsulation discard frame enable for the MAC(0-7) |

Table 87: Ethernet Frame Format Block - Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x1d698 | 7-0 | aTETHERRx | 0x0000 | Transmit errored Ethernet frame alarm for MAC0-7 0: no alarm 1: An errored Ethernet frame is detected by the MAC. Cleared on the next valid frame. |

Table 88: Ethernet Frame Format Block - Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------------|--------|---|
| 0x1d680 | 7-0 | MaTETHERRx | 0x00FF | Transmit errored Ethernet frame alarm mask for MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x1d682 | 0 | MaESA_Global_Interrupt | 0x0001 | Global interrupt mask for all the TETHER alarm of all the MAC 1: interrupt is masked (default) 0: interrupt is not masked |

Table 89: Ethernet Frame Format Block - Latched Alarms (RR)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|--|
| 0x1d69c | 7-0 | L1aTETHERRx | 0x0000 | Transmit errored Ethernet frame latched alarm for MAC0-7 0: no alarm is latched 1: alarm is latched. Clear on read |

Table 90: Ethernet Frame Format Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|--------|--|
| 0x1d688 | 0 | ESA_TETHER_Interrupt | 0x0000 | Transmit errored Ethernet frame alarm interrupt 1: interrupt before mask 0: no interrupt |
| 0x1d68a | 0 | ESA_Global_Interrupt | 0x0000 | ESA global alarm interrupt 1: global interrupt for all the L1aTETHER latched alarms 0: no global interrupt |

Table 91 through 103 - Ethernet Buffering and Flow Control in Transmit (Ethernet to SONET) and Receive (SONET to Ethernet) Paths

Table 91: SONET to Ethernet - General Configuration and Watermarks (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|-----------------|--------|---|
| 0x19680 | 7-0 | cHOLTXMACCRC | 0x00FF | Ethernet FCS discard for the 8 MACs. For each MAC, if '1' is selected, the LAN CRC of the incoming packets is kept; if '0' is selected, the LAN CRC is discarded. |
| 0x19682 | 0 | cHOLTRSTRAM | 0x0000 | SDRAM reset mode in case of HOL FIFO overflow. This bit affects all 8 MAC channels. 1: After an HOL FIFO (Ethernet packet buffering before the output) overflow, the FIFO is reset to empty. 0: After overflow, enough recent packets are discarded to bring the HOL FIFO fill level below the high watermark. |
| 0x19686 0x1968e 0x19696 0x1969e 0x196a6 0x196ae 0x196b6 0x196be | 7-0 | rHOLHWTMK_MSB_x | 0x00FF | HOL flow control: High watermark MSB for the MAC0-7 (See Note 1). |
| 0x19688 0x19690 0x19698 0x196a0 0x196a8 0x196b0 0x196b8 0x196c0 | 15-0 | rHOLHWTMK_LSB_x | 0xFFFF | HOL flow control: High watermark LSB for the MAC0-7 (See Note 1). |
| 0x1968a 0x19692 0x1969a 0x196a2 0x196aa 0x196b2 0x196ba 0x196c2 | 7-0 | rHOLLWTMK_MSB_x | 0x00FF | HOL flow control: Low watermark MSB for the MAC0-7 (See Note 1). |
| 0x1968c 0x19694 0x1969c 0x196a4 0x196ac 0x196b4 0x196bc 0x196c4 | 15-0 | rHOLLWTMK_LSB_x | 0xFFFF | HOL flow control: Low watermark LSB for the MAC0-7 (See Note 1). |

Note:

1. The allowed ranges for the High/Low HOL watermark registers depends on the SDRAM configuration (SDRAM_CFG bit) and the selection of GMII/SMII mode, as shown in the table below:



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Allowed Range for High/Low HOL Watermark Registers

| Mode | Memory Allocated to Each FIFO | Minimum Value for rHOLLWTMK_MSB_x, rHOLLWTMK_LSB_x | Maximum Value for rHOLHWTMK_MSB_x, rHOLHWTMK_LSB_x | Recommended default value |
|------------------|-------------------------------|--|--|---------------------------|
| SDRAM 8MB, SMII | 256 kB | 0000 0020 | 0000 FFFF | 0000 7FFF |
| SDRAM 8MB, GMII | 2MB | 0000 0020 | 0007 FFFF | 0003 FFFF |
| SDRAM 16MB, SMII | 512 kB | 0000 0020 | 0001 FFFF | 0000 FFFF |
| SDRAM 16MB, GMII | 4MB | 0000 0020 | 000F FFFF | 0007 FFFF |
| SDRAM 32MB, SMII | 1 MB | 0000 0020 | 0003 7FFF | 0001 FFFF |
| SDRAM 32MB, GMII | 8 MB | 0000 0020 | 001F FFFF | 000F FFFF |

Comments:

1. In the watermark registers, one step of 1 HEX corresponds to four bytes in the HOL FIFO. For example, if you lower the HOL watermark by a hex value of "1", the HOL FIFO threshold will be lowered by four bytes.
2. For the High HOL watermark, the maximum allowed value corresponds to the whole allocated FIFO space minus one 32 bit word (4 bytes).

Table 92: SONET to Ethernet - SDRAM Alarms (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------|--------|---|
| 0x19640 | 7-0 | aHOLFIFOx | 0x0000 | SDRAM overflow alarm for MAC0-7. If this overflow occurs, the number of dropped frames is determined by the difference between the decapsulation frame counter and the MAC frame counter. |
| 0x19642 | 7-0 | aHOLPTRRAMERRx | 0x0000 | SDRAM pointer error alarm for MAC0-7 |
| 0x19644 | 0 | COUNT_DFTC_100M | 0x0000 | Count status bit for the DFTC block |

Table 93: SONET to Ethernet - SDRAM Alarm and Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------------------------|--------|---|
| 0x19600 | 7-0 | MaHOLFIFOx | 0x00FF | SDRAM overflow alarm mask for the MAC0-7 |
| 0x19602 | 7-0 | MaHOLPTRRAMERRx | 0x00FF | SDRAM pointer error alarm mask for the MAC0-7 |
| 0x19604 | 0 | MCOUNT_DFTC_100M | 0x0001 | Mask of the count status bit for the DFTC block |
| 0x19606 | 0 | MaDFTC_HOLPTRRAMERR_Interrupt | 0x0001 | SDRAM pointer error alarm mask interrupt |
| 0x19608 | 0 | MaDFTC_HOLFIFO_Interrupt | 0x0001 | SDRAM overflow alarm mask interrupt |
| 0x1960a | 0 | MaDFTC_100M_Interrupt | 0x0001 | SDRAM controller block alarm mask interrupt |

Table 94: SONET to Ethernet - SDRAM Latched Alarms RR)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x19650 | 7-0 | L1aHOLFIFOx | 0x0000 | SDRAM overflow latched alarm for the MAC0-7 |
| 0x19652 | 7-0 | L1aHOLPTRRAMERRx | 0x0000 | SDRAM pointer error latched alarm for the MAC0-7 |
| 0x19654 | 0 | LCOUNT_DFTC_100M | 0x0000 | Latched count status bit for the DFTC block |

Table 95: SONET to Ethernet - SDRAM Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------------------|--------|----------------------------------|
| 0x19660 | 0 | DFTC_HOLFIFO_Interrupt | 0x0000 | SDRAM interrupt |
| 0x19662 | 0 | DFTC_HOLPTRRAMERR_Interrupt | 0x0000 | SDRAM pointer error interrupt |
| 0x19664 | 0 | DFTC_100M_Interrupt | 0x0000 | SDRAM controller block interrupt |
| 0x19666 | 0 | DFTC_Global_Interrupt | 0x0000 | DFTC global interrupt |

Table 96: SONET to Ethernet - SDRAM Performance Counters (RR)

| Address | Bit | HW Symbol | Init | Description |
|--|------|---------------|--------|--|
| 0x19620 0x19622 0x19624 0x19626 0x19628 0x1962a 0x1962c 0x1962e | 15-0 | rpcRSTHOLRAMx | 0x0000 | Reset MAC0-7 SDRAM part performance counter (overflow) |

Table 97: SONET to Ethernet - SDRAM FIFO Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------------|--------|--|
| 0x19678 | 7-0 | HOL_HWTMK_Detectx | 0x0000 | High Watermark status for HOL SDRAM part |
| 0x1967a | 7-0 | HOL_LWTMK_Detectx | 0x0000 | Low Watermark status for HOL SDRAM part |

Table 98: Ethernet to SONET - Flow Control Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|--------------|--------|---|
| 0x19800 0x19808 0x19810 0x19818 0x19820 0x19828 0x19830 0x19838 | 7-0 | rHWTMK_MSB_x | 0x00FF | Flow control: High watermark MSB for the MAC0-7 value by step of 32 bit word <u>MAC 0 to 7 in SMII (recommended value is 0x0000)</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x001FFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x003FFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x007FFF <u>MAC 0 in GMII (recommended value is 0x0000)</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x00FFFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x01FFFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x03FFFF |
| 0x19802 0x1980a 0x19812 0x1981a 0x19822 0x1982a 0x19832 0x1983a | 15-0 | rHWTMK_LSB_x | 0xFFFF | Flow control: High watermark LSB for the MAC0-7 value by step of 32 bit word <u>MAC 0 to 7 in SMII (recommended value is 0x186A)</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x001FFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x003FFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x007FFF <u>MAC 0 in GMII (recommended value is 0xC350)</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x00FFFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x01FFFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x03FFFF |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 98: Ethernet to SONET - Flow Control Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|--|------|---------------|--------|--|
| 0x19804 0x1980c 0x19814 0x1981c 0x19824 0x1982c 0x19834 0x1983c | 7-0 | rLWTMK_MSB_x | 0x00FF | Flow control: Low watermark MSB for the MAC0-7 value by step of 32 bit word <u>MAC 0 to 7 in SMII</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x001FFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x003FFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x007FFF <u>MAC 0 in GMII</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x00FFFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x01FFFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x03FFFF |
| 0x19806 0x1980e 0x19816 0x1981e 0x19826 0x1982e 0x19836 0x1983e | 15-0 | rLWTMK_LSB_x | 0xFFFF | Flow control: Low watermark LSB for the MAC0-7 value by step of 32 bit word <u>MAC 0 to 7 in SMII</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x001FFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x003FFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x007FFF <u>MAC 0 in GMII</u> SDRAM 8Mb: range for all the watermark from 0x000020 to 0x00FFFF SDRAM 16Mb: range for all the watermark from 0x000020 to 0x01FFFF SDRAM 32Mb: range for all the watermark from 0x000020 to 0x03FFFF |
| 0x19840 | 7-0 | cTXMACCRC | 0x00FF | Ethernet FCS discard for all the 8 MAC 0: LAN FCS is discarded before encapsulation 1: LAN FCS is kept during encapsulation One bit per MAC (LSB for MAC0, MSB for MAC7) |
| 0x19842 | 1-0 | cINRT_GRP100M | 0x0001 | Alarm latching configuration for the SDRAM alarm group (Table 101) Criteria used to create latched alarms from the raw (unlatched) alarms. 00: positive level 01: rising edge (default) 10: falling edge 11: rising or falling edge |
| 0x19844 | 0 | cTRSTRAM | 0x0000 | TxFIFO reset mode after overflow. This bit affects all 8 MAC channels. 1: After a TxFIFO overflow, the FIFO is reset to empty. 0: After TxFIFO overflow, enough recent packets are discarded to bring the TxFIFO fill level below the high watermark. |

Table 99: SDRAM Controller Alarm (Tx and Rx) (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x198c0 | 7-0 | aTXFIFOx | 0x0000 | TX FIFO overflow alarm for the MAC0-7 0: no alarm 1: TX FIFO overflow is detected. If the fifo resets to empty (cTRSTRAM bit is 1) then this alarm clears after 10 clock cycles, otherwise it clears after the FIFO depth falls below the high watermark. If this overflow occurs, the number of dropped frames is determined by the difference between the MAC frame counter and encapsulation frame counter. |
| 0x198c2 | 7-0 | aPTRRAMERRx | 0x0000 | SDRAM integrity alarm for the TX FIFO. Corruption at this interface could cause the TX FIFO to incorrectly determine it is above its high watermark, causing pause frames to continuously be sent. If this alarm is detected, a per channel soft reset should be considered. |
| 0x198c4 | 0 | aRXFIFOVC4 | 0x0000 | RX FIFO overflow alarm in VC-4 mode 0: no alarm 1: RXFIFO overflow is detected. Cleared on the RXFIFO reset |
| 0x198c6 | 0 | aLOSSDCLK | 0x0000 | Loss of Drop Clock alarm 0: no alarm 1: detection of the loss of DCLK input. Cleared on the recovery of the DCLK |

Table 99: SDRAM Controller Alarm (Tx and Rx) (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------|--------|---|
| 0x198c8 | 0 | COUNT_SHTC_100M | 0x0000 | Count status Bit for the SDRAM controller 0: no rpcRSTSDRAMx is overflowed 1: count status bit when one of the rpcRSTSDRAMx is overflowed |

Table 100: SDRAM Controller (Tx and Rx Direction) (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------------|--------|---|
| 0x198e0 | 7-0 | MaTXFIFOx | 0x00FF | TX FIFO overflow alarm mask for the MAC0-7 1: alarm is masked (default) 0: alarm is not masked |
| 0x198e2 | 7-0 | MaPTRRAMERRx | 0x00FF | TX RAM pointer error alarm mask for the MAC0-7 |
| 0x198e4 | 0 | MCOUNT_SHTC_100M | 0x0001 | Mask of the count status Bit for the 100MHz block 1: alarm is masked (default) 0: alarm is not masked |
| 0x198e6 | 0 | MaRXFIFOVC4 | 0x0001 | RX FIFO overflow alarm mask 1: alarm is masked (default) 0: alarm is not masked |
| 0x198e8 | 0 | MaLOSSDCLK | 0x0001 | Loss of Drop Clock alarm mask 1: alarm is masked (default) 0: alarm is not masked |
| 0x198ea | 0 | MaSHTC_PTRRAMERR_Interrupt | 0x0001 | TX RAM pointer error alarm mask interrupt |
| 0x198ec | 0 | MaSHTC_TXFIFO_Interrupt | 0x0001 | TX FIFO overflow alarm mask interrupt 1: interrupt for all the MAC is masked (default) 0: interrupt is not masked |
| 0x198ee | 0 | MaSHTC_100M_Interrupt | 0x0001 | SDRAM controller block alarm mask interrupt 1: general interrupt for all the alarms of Table 101 are masked (default) 0: general interrupt for all the alarms of Table 101 are not masked |

Table 101: SDRAM Controller (Tx and Rx Directions) (RR)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|---|
| 0x198d0 | 7-0 | L1aTXFIFOx | 0x0000 | TX FIFO overflow latched alarm for the MAC0-7 1: alarm is latched. Cleared on read 0: no alarm is latched |
| 0x198d2 | 7-0 | L1aPTRRAMERRx | 0x0000 | TX RAM pointer error latched alarm for the MAC0-7 1: alarm is latched. Cleared on read 0: no alarm is latched Corruption at the SDRAM interface could cause the TxFIFO to incorrectly determine it is above its high watermark, causing pause frames to continuously be sent. If this alarm is detected, a per channel soft reset should be considered (TX_RESETSx). |
| 0x198d4 | 0 | LCOUNT_SHTC_100M | 0x0000 | Latched count status bit for the SDRAM controller |
| 0x198d6 | 0 | L1aRXFIFOVC4 | 0x0000 | RX FIFO overflow latched alarm (VC-4 mode only) 1: alarm is latched. Cleared on read 0: no alarm is latched |
| 0x198d8 | 0 | L1aLOSSDCLK | 0x0000 | Loss of Drop Clock latched alarm 1: alarm is latched. Cleared on read 0: no alarm is latched |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 102: Ethernet to SONET, SDRAM Output - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------|--------|--|
| 0x198f8 | 0 | SHTC_TXFIFO_Interrupt | 0x0000 | TX FIFO interrupt 1: interrupt is active for all the TXFIFO 0: no interrupt |
| 0x198fa | 0 | SHTC_PTRRAMERR_Interrupt | 0x0000 | Reserved |
| 0x198fc | 0 | SHTC_100M_Interrupt | 0x0000 | SDRAM controller block interrupt before the mask MaSHTC_100M_interrupt 1: interrupt is active for the physical block 100M 0: no interrupt |
| 0x198fe | 0 | SHTC_Global_Interrupt | 0x0000 | SHTCL global interrupt after the mask MaSHTC_100M_interrupt 1: interrupt is active for the physical block 100M 0: no interrupt |

Table 103: Ethernet to SONET, SDRAM Output - Performance Counters

| Address | Bit | HW Symbol | Init | Description |
|----------------------|------|--------------|--------|---|
| 0x19880 – 0x1988e | 15-0 | rpcRSTSDRAMx | 0x0000 | In the Ethernet-to-SONET/SDH direction, this register counts the number of times the SDRAM TXFIFO area (for channel 0-7) is reset when the TXFIFO is in overflow condition. (RR when the perf counters are in saturating mode and not RR when the perf counters are in roll over mode) |

TX MAPPER BLOCK REGISTERS

Tables 104 through 107 - Configuration, Status and Interrupt handling of the Transmit Mapper Block

Table 104: Mapper Block - Reset (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------------------|--------|---|
| 0x1d288 | 0 | VTMD_CONF_ResetCounters | 0x0000 | VTMAPPER: reset counters 0: no reset state 1: reset counters in the transmit path |

Table 105: Mapper Block - Interrupt Configuration (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------------|--------|--|
| 0x1d28a | 0 | VTMD_Global_Interrupt | 0x0000 | Global interrupt of the VTMAPPER 1: interrupt (SONET/SDH side) is active 0: no interrupt |

Table 106: Mapper Block - Interrupt Mask (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x1d28c | 0 | MaVTMD_Interrupt | 0x0001 | VTMAPPER interrupt mask 1: VTMAPPER interrupt is masked. 0: VTMAPPER interrupt is not masked |

Table 107: Mapper and Demapper Block - Status (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------------------|--------|---|
| 0x1d28e | 0 | VTMD_CONF_DeviceInitialized | 0x0000 | Status of the end of Initialization of the design 0: Design is not initialized (need END_INIT_MICRO asserted after the 1: Design is initialized |

Tables 108 through 118 - Configuration of the Transmit Mapper Block

Table 108: Mapper Block - Timing Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|--------------------|--------|--|
| 0x13c40 | 11-0 | PulseDelay | 0x0000 | Defines the pulse delay that is needed to let a frame arrive in the Tx Combus Interface one frame after the request from the Combus is received. Set to 0x2C0. |
| 0x13c42 | 0 | AU_Mode | 0x0001 | Defines the AU mode: AU-3 (0) or AU-4 (1) |
| 0x13c44 | 0 | AU4_HO_VC4_Payload | 0x0000 | Defines what is in a VC-4 in AU-4 mode (TRUE is a C4 container, FALSE is substructured) |
| 0x13c46 | 1-0 | VC3_XConnect_0 | 0x0024 | Anticipate the timing of the L3 Xconnect |
| | 3-2 | VC3_XConnect_1 | | |
| | 5-4 | VC3_XConnect_2 | | |



Table 109: Mapper Block - TUG-3/VC-3 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------------|-------|--------|---|
| 0x13c00 | 0 | AU4_TUG3_Mode | 0 | 0x0000 | Defines what is in a TUG-3: TU-3 (0) or TUG-2 (1) |
| 0x13c02 | 1 | VC3_PayloadType | 1 | | Defines what is in a VC-3: TUG-2 (0) or C3 (1) |
| 0x13c04 | | | 2 | | |

Table 110: Mapper Block - TUG-2 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|--------------|-------|--------|--|
| 0x13c80 | 0 | TUG2_Is_TU12 | 0 | 0x0000 | Defines if a TUG-2 contains 4 TU-11's (0) or 3 TU-12's (1) |
| 0x13c82 | | | 1 | | |
| ... | | | ... | | |
| 0x13ca8 | | | 20 | | |

Table 111: Mapper Block - Pointer Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|------------------|-------|--------|---|
| 0x13d00 | 0 | PointerValueZero | 0 | 0x0001 | Select the value of the TU-11/TU-12 pointers: zero (1), or to 78/105 (0). |
| 0x13d02 | | | 1 | | |
| ... | | | ... | | |
| 0x13da6 | | | 83 | | |

Table 112: Mapper Block - General Configuration, Low Order (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|---------------------|--------|---|
| 0x1a400 | 0 | AU_Mode | 0x0006 | Selects AU-3 (0) or AU-4 (1) mode when in Low Order Mode. |
| | 1 | UseDefaultMapping | | Use default mapping for the Tx LO cross connect (ignore LOMP_MAPRAM when set). |
| | 2 | UpperMAPRAMValid | | Select Tx LO cross connect bank read by hardware. Software can only write to the inactive bank. |
| | 3 | ReadUpperMAPRAMBank | | Select Tx LO cross connect bank accessed by software. |

Table 113: Mapper Block - TUG-2 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|---|
| 0x1a500 | 0 | isTU12 | 0 | 0x0000 | Sets if a TUG-2 contains 4 TU-11's (0) or 3 TU-12's (1) |
| 0x1a502 | | | 1 | | |
| ... | | | ... | | |
| 0x1a528 | | | 20 | | |

Table 114: Mapper Block - POH Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|--------------------|-------|--------|---|
| 0x1a800 | 0 | BIP2_Error | 0 | 0x004A | Test: BIP-2 error insertion |
| 0x1a808 | 1 | PointerZeroValue | 1 | | Flags if V1/V2 pointer value is 0 or 78/105 |
| ... | ... | ... | ... | | Force VT/TU AIS |
| 0x1aa98 | 2 | SendVTAIS | 83 | | Force unequipped |
| | 3 | SendUneq | | | Select normal (0) or supervisory (1) unequipped |
| | 4 | UneqSelect | | | Sets an unidirectional signal VC |
| | 5 | SendUnidirectional | | | Single (1) or three (0) Bit RDI selection |
| | 6 | SingleRDI | | | |

Table 114: Mapper Block - POH Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-------|-----------------|---------------------|---|---|
| 0x1a802 0x1a80a ... 0x1aa9a | 7-0 | Ext_SignalLabel | 0 1 ... 83 | 0x0000 | The value of the transmitted extended signal label |
| 0x1a804 0x1a80c ... 0x1aa9c | 1-0 | REI_Source | 0 1 | 0x000A | Select REI source, POH RAM (00), POH Port (01), or Alarm Indication Port (10=default) |
| | 3-2 | RDI_Source | ... 83 | | Select RDI source, POH RAM (00), POH Port (01), or Alarm Indication Port (10=default) |
| | 5-4 | Ext_TSL_Source | | | Select Extended signal label source, POH RAM (00), or POH Port (01) |
| | 7-6 | LO_VC_Source | | | Select LO Virtual Concatenation control packet, POH RAM (00=default), POH Port (01), or Pass Through (11) |
| | 9-8 | APS_Source | | | Select APS source, POH RAM (00=default), or POH Port (01) |
| | 11-10 | DL_Source | | Select Data Link source, POH RAM (00=default), or POH Port (01) | |
| 0x1a806 0x1a80e ... 0x1aa9e | 1-0 | J2_Source | 0 1 | 0x0000 | Select J2 source, POH RAM (00=default), or POH Port (01) |
| | 3-2 | N2_Source | ... 83 | | Select N2/Z6 source, POH RAM (00=default), or POH Port (01) |

Table 115: Mapper Block - Cross Connect Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-------------|---------------------|--------|---|
| 0x1a600 0x1a602 ... 0x1a6a6 | 6-0 | MAPRAM_data | 0 1 ... 83 | 0x0000 | Transmit low order cross connect map. Disabled if UseDefaultMapping is true. |

Table 116: Mapper Block - V4 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|--------------|---------------------|--------|----------------------|
| 0x1a000 0x1a002 ... 0x1a0a6 | 7-0 | V4_ByteValue | 0 1 ... 83 | 0x0000 | Value of the V4 byte |

Table 117: Mapper Block - POH Byte Values (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|---------------|-----------------------|--------|-----------------------|
| 0x1b000 0x1b002 ... 0x1bd1e | 7-0 | POH_ByteValue | 0 1 ... 1679 | 0x0000 | Value of the POH byte |

See below for detailed offsets. The index of the VT/TU (0..83) in these arrays is according to the klm numbering (see Transmit Low Order Path Termination section of data sheet) $index = (k-1)*28 + (l-1)*4 + (m-1)$.

| Offset | Index | Description | Offset | Index | Description |
|--------|-------|--------------------|--------|-------|-------------|
| 0x000 | 0 | J2 Message Byte 0 | 0xa80 | 0 | V5 Byte |
| 0x002 | | J2 Message Byte 1 | 0xa82 | | N2/Z6 Byte |
| ... | | ... | 0xa84 | | K4/Z7 Byte |
| 0x01e | | J2 Message Byte 15 | 0xa86 | | not used |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

| Offset | Index | Description | Offset | Index | Description |
|--------|-------|--------------------|--------|-------|-------------|
| 0x020 | 1 | J2 Message Byte 0 | 0xa88 | 1 | V5 Byte |
| 0x022 | | J2 Message Byte 1 | 0xa8a | | N2/Z6 Byte |
| ... | | ... | 0xa8c | | K4/Z7 Byte |
| 0x03e | | J2 Message Byte 15 | 0xa8e | | not used |
| ... | | | ... | | |
| 0xa60 | 83 | J2 Message Byte 0 | 0xd18 | 83 | V5 Byte |
| 0xa62 | | J2 Message Byte 1 | 0xd1a | | N2/Z6 Byte |
| ... | | ... | 0xd1c | | K4/Z7 Byte |
| 0xa7e | | J2 Message Byte 15 | 0xd1e | | not used |

Table 118: Mapper Block - Bypass Control (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|---|
| 0x1a440 0x1a442 0x1a444 | 0 | ByPass | 0 1 2 | 0x0000 | Enables the POH processing bypass for an AU-3 |
| 0x1a480 0x1a482 0x1a484 | 0 | ByPass | 0 1 2 | 0x0000 | Enables the pointer processing bypass for an AU-3 |
| 0x1a4c0 0x1a4c2 0x1a4c4 | 0 | ByPass | 0 1 2 | 0x0000 | Enables the cross connect ByPass for an AU-3 |

RX DEMAPPER BLOCK REGISTERS

Tables 119 through 131 - Configuration, Status and Alarms for the Receive Demapper Block

Table 119: Demapper Block - General Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------------------|---------------------|--------|---|
| 0x1c670 | 0 | Check_SS | | 0x0001 | Activate SS Bit checking |
| 0x1c672 | 0 | Reserved | | 0x0006 | Reserved: this bit must be 0 for correct operation. |
| | 1 | UseDefaultMapping | | | Use default mapping for the Rx LO cross connect (ignore LODMP_MAPRAM when set). |
| | 2 | Active_MAPRAM_Bank_ID | | | Select Rx LO cross connect bank read by hardware. Software can only write to the inactive bank. |
| 0x1c674 | 0 | Bank_ID_MAPRAM | | 0x0000 | Select Rx LO cross connect bank accessed by software. |
| 0x1c400 0x1c402 ... 0x1c4a6 | 6-0 | MAPRAM_Data | 0 1 ... 83 | 0x0000 | Receive low order cross connect map. Disabled if UseDefaultMapping is true. |

Table 120: Demapper Block - Bypass Control (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|---------------------------------------|
| 0x1c600 0x1c602 0x1c604 | 0 | ByPass | 0 1 2 | 0x0000 | Enables the cross connect ByPass |
| 0x1c620 0x1c622 0x1c624 | 0 | ByPass | 0 1 2 | 0x0000 | Enables the pointer processing ByPass |

Table 121: Demapper Block - TUG-2 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------|---------------------|--------|------------------------|
| 0x1c680 0x1c682 ... 0x1c6a8 | 0 | isTU12 | 0 1 ... 20 | 0x0000 | TUG-2 contains TU-12's |

Table 122: Demapper Block - Performance Counters Shadow Registers (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|----------------|---------------------|--------|-----------------------------------|
| 0x1c800 0x1c804 ... 0x1c94c | 4-0 | PosJustCounter | 0 1 ... 83 | 0x0000 | Number of Positive Justifications |
| 0x1c802 0x1c806 ... 0x1c94e | 4-0 | NegJustCounter | 0 1 ... 83 | 0x0000 | Number of Negative Justifications |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 123: Demapper Block - Alarm Control (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|---|
| 0x1c660 | 0 | TSF_Inhibits_AIS | 0x003F | Trail Signal Failure inhibits AIS alarms |
| | 1 | TSF_Inhibits_LOP | | Trail Signal Failure inhibits LOP alarms |
| | 2 | PLM_Inhibits_AIS | | Payload Mismatch inhibits AIS alarms |
| | 3 | PLM_Inhibits_LOP | | Payload Mismatch inhibits LOP alarms |
| | 4 | LOM_Inhibits_AIS | | Loss Of MultiFrame inhibits AIS alarms |
| | 5 | LOM_Inhibits_LOP | | Loss Of MultiFrame inhibits LOP alarms |
| 0x1c662 | 0 | Reserved | 0x0002 | Reserved: this bit must be 0 for correct operation. |
| | 2-1 | IntEventControl | | Controls latching on raising and falling edges. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 4-3 | PM_EventControl | | Controls latching on raising and falling edges 00: PM disabled 01: Rising edge 10: Falling edge 11: Both edges |

Table 124: Demapper Block - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x1c640 | 0 | Interrupt | 0x0000 | Interrupt generated by Ptr Processor latched alarms |
| 0x1c642 | 0 | PM | 0x0000 | Summary for Performance Monitoring |
| 0x1c644 | 0 | FM | 0x0000 | Summary for Fault Monitoring |

Table 125: Demapper Block - Alarms (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|--|
| 0x1c700 | 0 | AIS_Detected | 0 | 0x0000 | Low Order Pointer Processor AIS defect |
| 0x1c702 | 1 | LossOfPointer | 1 | | Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1c7a6 | | | 83 | | |

Table 126: Demapper Block - Latched Alarms (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|--|
| 0x1ca00 | 0 | AIS_Detected | 0 | 0x0000 | Low Order Pointer Processor AIS defect |
| 0x1ca02 | 1 | LossOfPointer | 1 | | Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1caa6 | | | 83 | | |

Table 127: Demapper Block - Alarm Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---|
| 0x1cb00 | 0 | AIS_Detected | 0 | 0x0003 | Mask for the Low Order Pointer Processor AIS defect |
| 0x1cb02 | 1 | LossOfPointer | 1 | | Mask for the Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1cba6 | | | 83 | | |

Table 128: LODMP_Ptr_DefectCorrelations_LP (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|--|
| 0x1cc00 | 0 | AIS_Detected | 0 | 0x0000 | Low Order Pointer Processor AIS defect |
| 0x1cc02 | 1 | LossOfPointer | 1 | | Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1cca6 | | | 83 | | |

Table 129: LODMP_Ptr_DefectCorrelations_PM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|--|
| 0x1cd00 | 0 | AIS_Detected | 0 | 0x0000 | Low Order Pointer Processor AIS defect |
| 0x1cd02 | 1 | LossOfPointer | 1 | | Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1cda6 | | | 83 | | |

Table 130: LODMP_Ptr_DefectCorrelations_FM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|--|
| 0x1ce00 | 0 | AIS_Detected | 0 | 0x0000 | Low Order Pointer Processor AIS defect |
| 0x1ce02 | 1 | LossOfPointer | 1 | | Low Order Pointer Processor LOP defect |
| ... | | | ... | | |
| 0x1cea6 | | | 83 | | |

Table 131: Demapper Block - POH Byte Monitors (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--|
| 0x1cf00 | 7-0 | Data | 0 | 0x0000 | TU-11/VT1.5 or TU-12/VT2 V1 Pointer byte |
| 0x1cf02 | | | 1 | | |
| ... | | | ... | | |
| 0x1cfa6 | | | 83 | | |
| 0x1c000 | 7-0 | Data | 0 | 0x0000 | TU-11/VT1.5 or TU-12/VT2 V2 Pointer byte |
| 0x1c002 | | | 1 | | |
| ... | | | ... | | |
| 0x1c0a6 | | | 83 | | |
| 0x1c200 | 7-0 | Data | 0 | 0x0000 | TU-11/VT1.5 or TU-12/VT2 V4 byte |
| 0x1c202 | | | 1 | | |
| ... | | | ... | | |
| 0x1c2a6 | | | 83 | | |

Tables 132 through 154 - Configuration, Status and Alarms of the Low Order POH Monitor

Table 132: LO POH Monitor - Bypass Control (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|-------------------------------|
| 0x148e0 | 0 | ByPass | 0 | 0x0000 | Activate POH Processor bypass |
| 0x148e2 | | | 1 | | |
| 0x148e4 | | | 2 | | |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 133: LO POH Monitor - J2 Trace Message Handling

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------|-----------------------|--------|---------------------------------|
| 0x14900 0x14902 ... 0x1491e | 7-0 | J2_Byte | 0 1 ... 15 | 0x0000 | Received TTI Message byte (RO) |
| 0x14980 0x14982 ... 0x1499e | 7-0 | J2_Byte | 0 1 ... 15 | 0x0000 | Accepted TTI Message byte (RO) |
| 0x16000 0x16002 ... 0x16a7e | 7-0 | J2_Byte | 0 1 ... 1343 | 0x0000 | Expected TTI Message bytes (RW) |

Table 134: LO POH Monitor - POH Byte Monitors (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------|---------------------|--------|----------------|
| 0x17800 0x17808 ... 0x17a98 | 7-0 | V5 | 0 1 ... 83 | 0x0000 | V5 POH byte |
| 0x17802 0x1780a ... 0x17a9a | 7-0 | J2 | 0 1 ... 83 | 0x0000 | J2 POH byte |
| 0x17804 0x1780c ... 0x17a9c | 7-0 | N2 | 0 1 ... 83 | 0x0000 | N2/Z6 POH byte |
| 0x17806 0x1780e ... 0x17a9e | 7-0 | K4 | 0 1 ... 83 | 0x0000 | K4/Z7 POH byte |

Table 135: LO POH Monitor - Accepted Values (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|---------------|---------------------|--------|-----------------------------|
| 0x14000 0x14004 ... 0x1414c | 2-0 | TSL_Accepted | 0 1 ... 83 | 0x0000 | Accepted TSL (V5) bits |
| 0x14002 0x14006 ... 0x1414e | 7-0 | ETSL_Accepted | 0 1 ... 83 | 0x0000 | Accepted E-TSL (K4/Z7) byte |

Table 136: LO POH Monitor - Expected Values (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|--------------|---------------------|--------|------------------------|
| 0x14400 0x14404 ... 0x1454c | 2-0 | TSL_Expected | 0 1 ... 83 | 0x0000 | Expected TSL (V5) bits |

Table 136: LO POH Monitor - Expected Values (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|-----------------------------|
| 0x14402 | 7-0 | ETSL_Expected | 0 | 0x0000 | Expected E-TSL (K4/Z7) byte |
| 0x14406 | | | 1 | | |
| ... | | | ... | | |
| 0x1454e | | | 83 | | |

Table 137: LO POH Monitor - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----------------|---|--------|--|
| 0x148d0 | 7-0 | ResetCounters | 0x0000 | Reset Performance Counters when writing 0x91 (Write Only) |
| 0x14880 | 0 | Reserved | 0x0004 | Reserved: this field must be FALSE (0) for correct operation. |
| | 1 | ShadowRegister_Enable | | Enable Performance monitor shadow registers |
| | 3-2 | IntEventControl | | Mode to latch defects for Interrupt. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 5-4 | PM_EventControl | | Mode to latch defects for Fault/Performance monitoring 00: PM disabled 01: Rising edge 10: Falling edge 11: Both edges |
| 0x14800 | 0 | VC4hasC4 | 0x19A8 | High order VC-4 frame contains C-4 data |
| | 2-1 | RDI_NrOfIntervals | | Specify number of intervals before accepting RDI bit: 3 (00), 5 (01) or 10 (10) |
| | 6-3 | ERDI_NrOfIntervals | | Specify number of intervals before accepting E-RDI bits (5 to 10) |
| | 10-7 | TSL_NrOfIntervals | | Specify number of intervals before accepting TSL bits (3 to 10) |
| | 14-11 | ETSL_NrOfIntervals | | Specify number of intervals before accepting E-TSL byte (3 to 10) |
| 0x14802 | 3-0 | J2_NrOfFramesToSetTim | 0x0035 | Specify number of mismatching multiframes to set TIM defect |
| | 7-4 | J2_NrOfFramesToResetTim | | Specify number of matching multiframes to reset TIM defect |
| | 8 | J2_Report_Enable | | Enable J2 reporting |
| | 15-9 | J2_Report_Channel | | Channel number for J2 reporting |
| 0x14804 | 0 | AIS_SSF_Disable | 0x0000 | Disable SSF defect in generation of consequent action for AIS |
| | 1 | AIS_IncAIS_Disable | | Disable AIS (V5) defect in generation of consequent action for AIS |
| | 2 | AIS_UNEQ_Disable | | Disable UNEQ defect in generation of consequent action for AIS |
| | 3 | AIS_TIM_Disable | | Disable TIM defect in generation of consequent action for AIS |
| | 4 | TSF_SSF_Disable | | Disable SSF defect in generation of consequent action for TSF |
| | 5 | TSF_UNEQ_Disable | | Disable UNEQ defect in generation of consequent action for TSF |
| | 6 | TSF_TIM_Disable | | Disable TIM defect in generation of consequent action for TSF |
| | 7 | TSF_IncAIS_Disable | | Disable AIS (V5) defect in generation of consequent action for TSF |
| | 8 | RDI_SSF_Disable | | Disable SSF defect in generation of consequent action for RDI |
| | 9 | RDI_UNEQ_Disable | | Disable UNEQ defect in generation of consequent action for RDI |
| | 10 | RDI_TIM_Disable | | Disable TIM defect in generation of consequent action for RDI |
| | 11 | RDI_PLM_Disable | | Disable PLM defect in generation of consequent action for RDI |
| | 12 | LOM_LOM_Disable | | Disable LOM defect in generation of consequent action for LOM |
| 13 | PLM_PLM_Disable | Disable PLM defect in generation of consequent action for PLM | | |

Bits in register 0x14804 disable consequent actions when they are set to one. See [Mapper/Demapper Consequent Actions per Block](#) beginning on [page 390](#) for more details. In general, consequent actions should always be enabled. Specifically, if the SSF, UNEQ, AIS, LOM or PLM actions are disabled (bits 0,1,2,4,5,7,12 or 13 set to one), it is possible to observe sink side traffic loss during LCAS deprovisioning.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 138: LO POH Monitor - Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------------------------|-------|-----------------------------|---------------|--------|---|---|
| 0x17c00 0x17c08 ... | 0 | Unidirectional | 0 1 ... | 0x0000 | Enables the unidirectional option. If the unidirectional mode is active, the POH monitor reports FarEndBlockErrorCounter = 0 and clears all received RDI defects. Default value = false | |
| 0x17e98 | 1 | InsertAIS | 83 | | | Force AIS insertion |
| | 2 | ERDI_Disable | | | | Disable K4/Z7 E-RDI processing |
| 0x17c02 0x17c0a ... | 0 | J2_ExtiMessage | 0 | 0x0000 | J2 TTI 16 byte message or repeating non-specific byte mode | |
| 0x17e9a | 1 | J2_TimEnable | 1 ... | | | Enable J2 TIM monitoring |
| | | | 83 | | | |
| 0x17c04 0x17c0c ... | 10-0 | BIP2_DEG_SetThreshold | 0 | 0x1001 | Specify error threshold to set degraded interval | |
| 0x17e9c | 14-11 | BIP2_DEG_SetNrOfIntervals | 1 ... | | | Specify number of degraded intervals to set signal degrade defect |
| | | | 83 | | | |
| 0x17c06 0x17c0e ... | 10-0 | BIP2_DEG_ClearThreshold | 0 | 0x1001 | Specify error threshold to clear degraded interval | |
| 0x17e9e | 14-11 | BIP2_DEG_ClearNrOfIntervals | 1 ... | | | Specify number of not-degraded intervals to clear signal degrade defect |
| | | | 83 | | | |

Table 139: LO POH Monitor - Channel Status (RO)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------------------------|-----|-------------------------|---------------|--------|---|--|
| 0x14a00 0x14a02 ... | 0 | PohRamWriteInSecondBank | 0 1 ... | 0x0000 | Writing bytes to Second POH RAM register bank | |
| 0x14aa6 | | | 83 | | | |

Table 140: LO POH Monitor - Channel Report (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------|--------|---|
| 0x148c0 | 0 | J2_Stable_1 | 0x0000 | Stable J2 TTI repeating non-specific byte |
| | 1 | J2_Stable_16 | | Stable J2 TTI 16-byte message |

Table 141: LO POH Monitor - Channel Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------------------------|-----|-------------|-------|--------|--|
| 0x14c00 0x14c02 ... | 0 | CI_SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x14ca6 | 1 | V5_DEG | 1 | | V5 Signal Degrade defect |
| | 2 | V5_AIS | ... | | V5 Alarm Indication Signal defect |
| | 3 | V5_PLM | 83 | | V5 Payload Mismatch defect |
| | 4 | V5_UNEQ | | | V5 Unequipped signal defect |
| | 5 | V5_RFI | | | V5 Remote Failure Indication defect |
| | 6 | V5_RDI | | | V5 Remote Defect Indication defect |
| | 7 | K4_ERDI_C | | | K4/Z7 Enhanced-RDI Connectivity defect |
| | 8 | K4_ERDI_P | | | K4/Z7 Enhanced-RDI Payload defect |
| | 9 | K4_ERDI_S | | | K4/Z7 Enhanced-RDI Server defect |
| | 10 | K4_LOM | | | K4/Z7 Loss Of Multiframe defect |
| | 11 | J2_TIM | | | J2 Trace Identifier Mismatch defect |
| | 12 | J2_TTI_ZERO | | | J2 TTI all-zero repeating byte defect |

Table 142: LO POH Monitor - Defect Correlations (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|------------------------------------|----------------------------------|
| 0x14e00 | 0 | SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x14e02 | 1 | DEG | 1 | | Degraded Signal defect |
| ... | ... | ... | ... | | |
| 0x14ea6 | 2 | AIS | 83 | | ALarm Indication Signal defect |
| | 3 | PLM | | | Payload Mismatch defect |
| | 4 | UNEQ | | | Unequipped signal defect |
| | 5 | RFI | | | Remote Failure Indication defect |
| | 6 | RDI | | | Remote Defect Indication defect |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity defect |
| | 8 | ERDI_P | | | Enhanced-RDI payload defect |
| | 9 | ERDI_S | | | Enhanced-RDI server defect |
| | 10 | LOM | | | Loss Of Multiframe defect |
| | 11 | TIM | | | Trace Identifier Mismatch defect |
| | 12 | TTI_ZERO | | TTI all-zero repeating byte defect | |

Table 143: LO POH Monitor - Latched Defects (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|------------------------------------|----------------------------------|
| 0x15000 | 0 | SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x15002 | 1 | DEG | 1 | | Degraded Signal defect |
| ... | ... | ... | ... | | |
| 0x150a6 | 2 | AIS | 83 | | ALarm Indication Signal defect |
| | 3 | PLM | | | Payload Mismatch defect |
| | 4 | UNEQ | | | Unequipped signal defect |
| | 5 | RFI | | | Remote Failure Indication defect |
| | 6 | RDI | | | Remote Defect Indication defect |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity defect |
| | 8 | ERDI_P | | | Enhanced-RDI payload defect |
| | 9 | ERDI_S | | | Enhanced-RDI server defect |
| | 10 | LOM | | | Loss Of Multiframe defect |
| | 11 | TIM | | | Trace Identifier Mismatch defect |
| | 12 | TTI_ZERO | | TTI all-zero repeating byte defect | |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 144: LO POH Monitor - Defect Correlations Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|----------------------------------|----------------------------------|
| 0x15200 | 0 | SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x15202 | 1 | DEG | 1 | | Degraded Signal defect |
| ... | ... | ... | ... | | |
| 0x152a6 | 2 | AIS | 83 | | ALarm Indication Signal defect |
| | 3 | PLM | | | Payload Mismatch defect |
| | 4 | UNEQ | | | Unequipped signal defect |
| | 5 | RFI | | | Remote Failure Indication defect |
| | 6 | RDI | | | Remote Defect Indication defect |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity defect |
| | 8 | ERDI_P | | | Enhanced-RDI payload defect |
| | 9 | ERDI_S | | | Enhanced-RDI server defect |
| | 10 | LOM | | | Loss Of Multiframe defect |
| | 11 | TIM | | Trace Identifier Mismatch defect | |

Table 145: LO POH Monitor - PM Defect Correlations Monitor (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|----------------------------------|----------------------------------|
| 0x15400 | 0 | SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x15402 | 1 | DEG | 1 | | Degraded Signal defect |
| ... | ... | ... | ... | | |
| 0x154a6 | 2 | AIS | 83 | | ALarm Indication Signal defect |
| | 3 | PLM | | | Payload Mismatch defect |
| | 4 | UNEQ | | | Unequipped signal defect |
| | 5 | RFI | | | Remote Failure Indication defect |
| | 6 | RDI | | | Remote Defect Indication defect |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity defect |
| | 8 | ERDI_P | | | Enhanced-RDI payload defect |
| | 9 | ERDI_S | | | Enhanced-RDI server defect |
| | 10 | LOM | | | Loss Of Multiframe defect |
| | 11 | TIM | | Trace Identifier Mismatch defect | |

Table 146: LO POH Monitor - FM Defect Correlations Monitor (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|----------------------------------|----------------------------------|
| 0x15600 | 0 | SSF | 0 | 0x0000 | Server Signal Fail defect |
| 0x15602 | 1 | DEG | 1 | | Degraded Signal defect |
| ... | ... | ... | ... | | |
| 0x156a6 | 2 | AIS | 83 | | ALarm Indication Signal defect |
| | 3 | PLM | | | Payload Mismatch defect |
| | 4 | UNEQ | | | Unequipped signal defect |
| | 5 | RFI | | | Remote Failure Indication defect |
| | 6 | RDI | | | Remote Defect Indication defect |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity defect |
| | 8 | ERDI_P | | | Enhanced-RDI payload defect |
| | 9 | ERDI_S | | | Enhanced-RDI server defect |
| | 10 | LOM | | | Loss Of Multiframe defect |
| | 11 | TIM | | Trace Identifier Mismatch defect | |

Table 147: LO POH Monitor - Defect Correlations Mask (R/W)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|----------------------------------|--------------------------------|
| 0x15800 | 0 | SSF | 0 | 0x1FFF | Server Signal Fail mask |
| 0x15802 | 1 | DEG | 1 | | Degraded Signal Defect mask |
| ... | ... | ... | ... | | |
| 0x158a6 | 2 | AIS | 83 | | ALarm Indication Signal mask |
| | 3 | PLM | | | Payload Mismatch mask |
| | 4 | UNEQ | | | Unequipped signal mask |
| | 5 | RFI | | | Remote Failure Indication mask |
| | 6 | RDI | | | Remote Defect Indication mask |
| | 7 | ERDI_C | | | Enhanced-RDI connectivity mask |
| | 8 | ERDI_P | | | Enhanced-RDI payload mask |
| | 9 | ERDI_S | | | Enhanced-RDI server mask |
| | 10 | LOM | | | Loss Of Multiframe mask |
| | 11 | TIM | | | Trace Identifier Mismatch mask |
| | 12 | TTI_ZERO | | TTI all-zero repeating byte mask | |

Table 148: LO POH Monitor - Defect Correlations Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----------------------------|--|--------|---|
| 0x148a0 | 0 | UNEQ_SSF_Inhibit_Disable | 0x0000 | Disable SSF defect in generation of defect correlation for UNEQ |
| | 1 | UNEQ_TIM_Disable | | Disable TIM defect in generation of defect correlation for UNEQ |
| | 2 | UNEQ_TTIZERO_Disable | | Disable TTIZERO defect in generation of defect correlation for UNEQ |
| | 3 | TIM_SSF_Inhibit_Disable | | Disable SSF defect in generation of defect correlation for TIM |
| | 4 | TIM_UNEQ_Inhibit_Disable | | Disable UNEQ defect in generation of defect correlation for TIM |
| | 5 | TIM_TTIZERO_Inhibit_Disable | | Disable TTIZERO defect in generation of defect correlation for TIM |
| | 6 | DEG_SSF_Inhibit_Disable | | Disable SSF defect in generation of defect correlation for DEG |
| | 7 | DEG_TIM_Inhibit_Disable | | Disable TIM defect in generation of defect correlation for DEG |
| | 8 | RDI_SSF_Inhibit_Disable | | Disable SSF defect in generation of defect correlation for RDI |
| | 9 | RDI_UNEQ_Inhibit_Disable | | Disable UNEQ defect in generation of defect correlation for RDI |
| | 10 | RDI_TIM_Inhibit_Disable | | Disable TIM defect in generation of defect correlation for RDI |
| | 11 | RDI_TTIZERO_Inhibit_Disable | | Disable TTIZERO defect in generation of defect correlation for RDI |
| | 12 | RFI_SSF_Inhibit_Disable | | Disable SSF defect in generation of defect correlation for RFI |
| | 13 | RFI_UNEQ_Inhibit_Disable | | Disable UNEQ defect in generation of defect correlation for RFI |
| | 14 | RFI_TIM_Inhibit_Disable | | Disable TIM defect in generation of defect correlation for RFI |
| 15 | RFI_TTIZERO_Inhibit_Disable | Disable TTIZERO defect in generation of defect correlation for RFI | | |
| 0x148a2 | 0 | SSF_IncAIS_Disable | 0x0000 | Disable AIS (V5) defect in generation of defect correlation for SSF |
| | 1 | PLM_TSF_Inhibit_Disable | | Disable TSF defect in generation of defect correlation for PLM |
| | 2 | LOM_TSF_Inhibit_Disable | | Disable TSF defect in generation of defect correlation for LOM |
| | 3 | LOM_PLM_Inhibit_Disable | | Disable PLM defect in generation of defect correlation for LOM |
| | 4 | TTIZERO_SSF_Inhibit_Disable | | Disable SSF defect in generation of defect correlation for TTIZERO |



Table 149: LO POH Monitor - Defect Correlations Summary (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-------------|-------|--------|---|
| 0x15a00 | 0 | LatchForInt | 0 | 0x0000 | Defect Correlations summary Latched For Interrupt per channel |
| 0x15a02 | 1 | PM | 1 | | |
| ... | | | ... | | |
| 0x15aa6 | 2 | FM | 83 | | Defect Correlations summary for Fault Monitoring per channel |

Table 150: LO POH Monitor - Defect Correlations Summary Mask (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--|
| 0x15c00 | 0 | Mask | 0 | 0x0001 | Defect Correlations summary mask per channel |
| 0x15c02 | | | 1 | | |
| ... | | | ... | | |
| 0x15ca6 | | | 83 | | |

Table 151: LO POH Monitor - Defect Correlations Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x14840 | 0 | Interrupt | 0x0000 | Defect Correlations group summary for Interrupt generation |
| 0x14842 | 0 | PM | 0x0000 | Defect Correlations group summary for Performance monitoring |
| 0x14844 | 0 | FM | 0x0000 | Defect Correlations group summary for Fault monitoring |

Table 152: LO POH Monitor - Performance Monitor One Second Latch (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--|
| 0x15e00 | 0 | NDS | 0 | 0x0000 | Near-End Defect second, TSF occurrence per one second interval |
| 0x15e02 | 1 | FDS | 1 | | |
| ... | | | ... | | Far-End Defect second, RDI occurrence per one second interval |
| 0x15ea6 | | | 83 | | |

Table 153: LO POH Monitor - Performance Counters (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|------|-------------------------------|-------|--------|---|
| 0x17000 | 10-0 | BIP2_NearEndBlockErrorCounter | 0 | 0x0000 | BIP-2 Near-End Block Errors per one second interval |
| 0x17008 | | | 1 | | |
| ... | | | ... | | |
| 0x17298 | | | 83 | | |
| 0x17002 | 11-0 | BIP2_ErrorCounter | 0 | 0x0000 | BIP-2 Errors per one second interval |
| 0x1700a | | | 1 | | |
| ... | | | ... | | |
| 0x1729a | | | 83 | | |
| 0x17004 | 10-0 | REI_FarEndBlockErrorCounter | 0 | 0x0000 | REI Far-End Block Errors per one second interval |
| 0x1700c | | | 1 | | |
| ... | | | ... | | |
| 0x1729c | | | 83 | | |

Table 154: LO POH Monitor - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|------|-------------------------------|-------|--------|---|
| 0x17400 | 10-0 | BIP2_NearEndBlockErrorCounter | 0 | 0x0000 | BIP-2 Near-End Block Errors per one second interval |
| 0x17408 | | | 1 | | |
| ... | | | ... | | |
| 0x17698 | | | 83 | | |

Table 154: LO POH Monitor - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|------|-----------------------------|---------------------|--------|--|
| 0x17402 0x1740a ... 0x1769a | 11-0 | BIP2_ErrorCounter | 0 1 ... 83 | 0x0000 | BIP-2 Errors per one second interval |
| 0x17404 0x1740c ... 0x1769c | 10-0 | REI_FarEndBlockErrorCounter | 0 1 ... 83 | 0x0000 | REI Far-End Block Errors per one second interval |

Tables 155 through 162 - Configuration, Status and Alarms of the Low Order Tx Alarm Indication (RING) Port

Table 155: Tx LO Ring Port - General Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|---------------------------------------|--|---------------------|--------|---|
| 0x18100 0x18102 ... 0x181a6 | 0 1 2 | SelectInterface ResetChannel Extend_RDI | 0 1 ... 83 | 0x0000 | Select per low order path the internal (0) or external (1) interface. Resets an entire channel Use extended 3-bit RDI |
| 0x18060 | 0 1 | ClockEdge DisableAP | | 0x0000 | Sets the rising (0) or the falling (1) edge of the clock as active edge Disables the entire Alarm Indication Port |
| 0x18070 | 7-0 8 9 10 12-11 14-13 | ResetCounters Reserved SaturateCounters ShadowRegister_Enable IntEventCtrl PM_EventCtrl | | 0x0800 | Reset the event counters Reserved: this field must be FALSE (0) for correct operation. Sets counters to either saturating or wrap-around Enables the performance counter mode with shadow counters Chooses when to latch the events or defects for interrupt: 00 - level controlled 01 - rising edge 10 - falling edge 11 - both edges Chooses when to latch the defects for PM/FM (Disable PM/FM (00), rising edge (01), falling edge (10), both edges (11)) |

Table 156: Tx LO Ring Port - Event Latch (COW-1)

| Address | Bit | HW Symbol | Init | Description |
|---------|--------|--|--------|---|
| 0x18080 | 0 1 | CRC_Error_Internal_li CRC_Error_External_li | 0x0000 | Latch for interrupt signals for CRC_Error of both interface |

Table 157: Tx LO Ring Port - Performance Counters (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------------|--------|--|
| 0x18020 | 15-0 | pCRC_Error_Internal | 0x0000 | Performance counter for CRC errors of the internal ring port |
| 0x18022 | 15-0 | pCRC_Error_External | 0x0000 | Performance counter for CRC errors of the external ring port |

Table 158: Tx LO Ring Port - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------------|--------|--|
| 0x18040 | 15-0 | pCRC_Error_Internal | 0x0000 | Performance counter for CRC errors of the internal ring port |
| 0x18042 | 15-0 | pCRC_Error_External | 0x0000 | Performance counter for CRC errors of the external ring port |



Table 159: Tx LO Ring Port - Defects

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------|--------|---|
| 0x180c0 | 0 | cLOC_Internal | 0x0000 | Defect correlations for the LOC defects (RO) |
| | 1 | cLOC_External | | |
| 0x180c2 | 0 | LOC_Internal_li | 0x0000 | Latch for interrupt signals for the LOC defects (COW-1) |
| | 1 | LOC_External_li | | |
| 0x180c4 | 0 | LOC_Internal_lp | 0x0000 | Latch for PM/FM signals for the LOC defects (COW-0) |
| | 1 | LOC_External_lp | | |
| 0x180c6 | 0 | LOC_Internal_pm | 0x0000 | Performance monitoring signals for the LOC defects (RO) |
| | 1 | LOC_External_pm | | |
| 0x180c8 | 0 | LOC_Internal_fm | 0x0000 | Fault monitoring signals for the LOC defects (RO) |
| | 1 | LOC_External_fm | | |

Table 160: Tx LO Ring Port - Interrupt Mask (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|--------|---|
| 0x18090 | 0 | CRC_Error_Internal_m | 0x0003 | Interrupt masks for the CRC Error latch for interrupt signals |
| | 1 | CRC_Error_External_m | | |
| 0x180a0 | 0 | LOC_Internal_m | 0x0003 | Interrupt masks for the LOC latch for interrupt signals |
| | 1 | LOC_External_m | | |

Table 161: Tx LO Ring Port - Event Interrupt (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x180b0 | 0 | GeneralInterrupt | 0x0001 | General Interrupt signal for the Tx LO Alarm Indication Port |

Table 162: Tx LO Ring Port - Defect Interrupt (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x18000 | 0 | GeneralInterrupt | 0x0001 | General Interrupt signal for the Tx LO Alarm Indication Port |

Table 163 - Configuration of the Low Order Rx Alarm Indication (RING) Port

Table 163: Rx LO Ring Port - Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d7c0 | 0 | InsertCRCError | 0x0000 | Insert a CRC error when a CRC4 is calculated |
| 0x1d7c2 | 0 | ClockEdge | 0x0000 | Sets the rising (0) or falling (1) edge as active edge |

Tables 164 through 166 - Configuration and Status of the general Low Order Interrupt Controller

Table 164: LO Interrupt Controller - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------------|----------------|--|
| 0x1d2c4 | 0 | TXAP_CorrDefect_Interrupt | Not Applicable | Interrupt of the per channel defects coming from the TX Alarm Indication Port. Default value: TRUE |
| | 1 | TXAP_Event_Interrupt | | Interrupt of the per channel events coming from the TX Alarm Indication Port. Default value: TRUE |
| | 2 | LODMP_POH_CorrDefect_Interrupt | | Interrupt coming from the POH monitor of the LO Demapper. Default value: TRUE |
| | 3 | LODMP_PTR_CorrDefect_Interrupt | | Interrupt coming from the PTR processor of the LO Demapper. Default value: TRUE |

Table 165: LO Interrupt Controller - Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------------|--------|--|
| 0x1d2c6 | 0 | TXAP_CorrDefect_Interrupt | 0x000F | Interrupt of the per channel defects coming from the TX Alarm indication Port. Default value: TRUE |
| | 1 | TXAP_Event_Interrupt | | Interrupt of the per channel events coming from the TX Alarm Indication Port. Default value: TRUE |
| | 2 | LODMP_POH_CorrDefect_Interrupt | | Interrupt coming from the POH monitor of the LO Demapper. Default value: TRUE |
| | 3 | LODMP_PTR_CorrDefect_Interrupt | | Interrupt coming from the PTR processor of the LO Demapper. Default value: TRUE |

Table 166: LO Interrupt Controller - Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x1d2c0 | 0 | Interrupt | 0x0000 | Interrupt summary for the whole VTMAPPER block |

Table 167 - Configuration of the High Order Rx Alarm Indication (RING) Port

Table 167: Rx HO Ring Port - Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d7d0 | 0 | InsertCRCError | 0x0000 | Insert a CRC error when a CRC4 is calculated |
| 0x1d7d2 | 0 | ClockEdge | 0x0000 | Sets the rising (0) or falling (1) edge as active edge |

Tables 168 through 176 - Configuration, Status and Alarms of the High Order Tx Alarm Indication (RING) Port

Table 168: Tx HO Ring Port - Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------------|---------------------|--------|---|
| 0x19a00 | 0 | ClockEdge | | 0x0000 | Sets the rising (0) or the falling (1) edge of the clock as active edge |
| 0x19a02 | 0 | DisableAP | | 0x0000 | Disables the entire Alarm Indication Port |
| 0x19a80 0x19a88 ... 0x19af8 | 0 | SelectInterface | 0 1 ... 15 | 0x0000 | Select per high order path the internal (0) or external (1) interface. |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 168: Tx HO Ring Port - Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|--------------|---------------------|--------|--------------------------|
| 0x19a82 0x19a8a ... 0x19afa | 0 | ResetChannel | 0 1 ... 15 | 0x0000 | Resets an entire channel |
| 0x19a84 0x19a8c ... 0x19afc | 0 | Extend_RDI | 0 1 ... 15 | 0x0000 | Use extended RDI |

Table 169: Tx HO Ring Port - Counter Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-------|-----------------------|--------|---|
| 0x19a30 | 7-0 | ResetCounters | 0x0800 | Reset the event counters |
| | 8 | Reserved | | Reserved: this field must be FALSE (0) for correct operation. |
| | 9 | SaturateCounters | | Sets counters to either saturating or wrap-around |
| | 10 | ShadowRegister_Enable | | Enables the performance counter mode with shadow counters |
| | 12-11 | IntEventCtrl | | Chooses when to latch the events or defects for interrupt: 00 - level controlled 01 - rising edge 10 - falling edge 11 - both edges |
| | 14-13 | PM_EventCtrl | | Chooses when to latch the defects for PM/FM (Disable PM/FM (00), rising edge (01), falling edge (10), both edges (11)) |

Table 170: Tx HO Ring Port - Event Latch (COW-1)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------------|--------|---|
| 0x19a38 | 0 | CRC_Error_Internal_li | 0x0000 | Latch for interrupt signals for CRC_Error of both interface |
| | 1 | CRC_Error_External_li | | |

Table 171: Tx HO Ring Port - Performance Counters (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------------|--------|--|
| 0x19a10 | 15-0 | pCRC_Error_Internal | 0x0000 | Performance counter for CRC errors of the internal ring port |
| 0x19a12 | 15-0 | pCRC_Error_External | 0x0000 | Performance counter for CRC errors of the external ring port |

Table 172: Tx HO Ring Port - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|---------------------|--------|--|
| 0x19a20 | 15-0 | pCRC_Error_Internal | 0x0000 | Performance counter for CRC errors of the internal ring port |
| 0x19a22 | 15-0 | pCRC_Error_External | 0x0000 | Performance counter for CRC errors of the external ring port |

Table 173: Tx HO Ring Port - Defects

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------|--------|---|
| 0x19a60 | 0 | cLOC_Internal | 0x0000 | Defect correlations for the LOC defects (RO) |
| | 1 | cLOC_External | | |
| 0x19a62 | 0 | LOC_Internal_li | 0x0000 | Latch for interrupt signals for the LOC defects (COW-1) |
| | 1 | LOC_External_li | | |

Table 173: Tx HO Ring Port - Defects

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------------|--------|---|
| 0x19a64 | 0 | LOC_Internal_lp | 0x0000 | Latch for PM/FM signals for the LOC defects (COW-0) |
| | 1 | LOC_External_lp | | |
| 0x19a66 | 0 | LOC_Internal_pm | 0x0000 | Performance monitoring signals for the LOC defects (RO) |
| | 1 | LOC_External_pm | | |
| 0x19a68 | 0 | LOC_Internal_fm | 0x0000 | Fault monitoring signals for the LOC defects (RO) |
| | 1 | LOC_External_fm | | |

Table 174: Tx HO Ring Port - Interrupt Mask (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|--------|---|
| 0x19a40 | 0 | CRC_Error_Internal_m | 0x0003 | Interrupt masks for the CRC Error latch for interrupt signals |
| | 1 | CRC_Error_External_m | | |
| 0x19a48 | 0 | LOC_Internal_m | 0x0003 | Interrupt masks for the LOC latch for interrupt signals |
| | 1 | LOC_External_m | | |

Table 175: Tx HO Ring Port - General Interrupt (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x19a50 | 0 | GeneralInterrupt | 0x0001 | General Interrupt signal for the Tx LO Alarm Indication Port |

Table 176: Tx HO Ring Port - Defect Interrupt (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|--------|--|
| 0x19a58 | 0 | GeneralInterrupt | 0x0001 | General Interrupt signal for the Tx LO Alarm Indication Port |

Tables 177 through 209 - Configuration, Status and Alarms of the High Order POH Monitor

Table 177: HO POH Monitor - Received-64 Byte Trace Message (RO)

| Offset | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|-----|-----------|-------|--------|-------------|
| 0x00-0x7e (increments by 0x02) | 7-0 | ByteValue | 0-63 | 0x0000 | RAM Byte |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|-------------|------------|
| Base Address | 0x1f780 | 0x1da00 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 178: HO POH Monitor - Received 16-Byte Trace Message (RO)

| Offset | Bit | HW Symbol | Index | Init | Description |
|-----------------------------------|-----|-----------|-------|--------|-------------|
| 0x00-0x1e (increments by 0x02) | 7-0 | ByteValue | 0-15 | 0x0000 | Ram Byte |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|--------------------|-------------------|
| Base Address | 0x1f6c0 | 0x1dc00 |

Table 179: HO POH Monitor - Accepted Bytes (RO)

| Offset | Bit | HW Symbol | Index | Init | Description |
|-----------------------------------|-----|-----------|-------|--------|-------------|
| 0x00-0x7e (increments by 0x02) | 7-0 | ByteValue | 0-63 | 0x0000 | Ram Byte |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|--------------------|-------------------|
| Base Address | 0x1f400 | 0x1db00 |

Table 180: HO POH Monitor - Expected J1 Bytes (RW)

| Offset | Bit | HW Symbol | Index | Init | Description |
|-----------------------------------|-----|-----------|-------|--------|-------------|
| 0x00-0x7e (increments by 0x02) | 7-0 | ByteValue | 0-63 | 0x0000 | Ram Byte |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f500 | 0x1de00 | 0x1de80 | 0x1df00 |

Table 181: HO POH Monitor - Expected C2 Bytes (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|-------------|
| 0 | 7-0 | ByteValue | 0x0000 | Ram Byte |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f750 | 0x1dcb0 | 0x1dcb2 | 0x1dcb4 |

Table 182: HO POH Monitor - Received POH Bytes (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------------------|
| 0 | 7-0 | J1 | 0x0000 | J1 byte of the previously received VC |
| 2 | 7-0 | B3 | 0x0000 | B3 byte of the previously received VC |
| 4 | 7-0 | C2 | 0x0000 | C2 byte of the previously received VC |
| 6 | 7-0 | G1 | 0x0000 | G1 byte of the previously received VC |

Table 182: HO POH Monitor - Received POH Bytes (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|--|
| 8 | 7-0 | F2 | 0x0000 | F2 byte of the previously received VC |
| a | 7-0 | H4 | 0x0000 | H4 byte of the previously received VC |
| c | 7-0 | F3 | 0x0000 | F3/Z3 byte of the previously received VC |
| e | 7-0 | K3 | 0x0000 | K3/Z4 byte of the previously received VC |
| 10 | 7-0 | N1 | 0x0000 | N1/Z5 byte of the previously received VC |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f640 | 0x1d800 | 0x1d820 | 0x1d840 |

Table 183: HO POH Monitor - Accepted POH Bytes (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------------------|
| 0 | 7-0 | C2 | 0x0000 | Accepted C2 byte (debounced value) |
| 2 | 7-0 | K3 | 0x0000 | Accepted K3/Z4 byte (debounced value) |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f738 | 0x1dc60 | 0x1dc64 | 0x1dc68 |

Table 184: HO POH Monitor - Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-------------------|--------|--|
| 0 | 2-0 | POHMon_Mode | 0x0000 | This field must be 0x0000 for correct VC-3 operation, and 0x0006 for correct VC-4 operation. |
| 2 | 0 | J1_Report_Enable | 0x0000 | Enable J1 TTI message reporting |
| | 2-1 | J1_Report_Channel | | VC that is used for reporting J1. Numbering starts at 00. Example: for the first VC-3 you write '00' to bit 1 and 2 (and '1' to bit 0) |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|-------------|------------|
| Base Address | 0x1f740 | 0x1dc40 |

Table 185: HO POH Monitor - Loopback Control (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1f754 | 0 | LoopBackActive | 0x0000 | Controls Ethernet/Local Side loopback from Add to Drop Telecom bus. Default value: disabled (0). |

Table 186: HO POH Monitor - Channel Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|----------------|--------|--|
| 0 | 0 | Unidirectional | 0x0000 | Enables the unidirectional option. If the uni-directional option is active, the POH monitor reports FarEndBlockErrorCounter = 0 and clear all received RDI defects. Default value: FALSE |
| | 1 | Bypass | | Bypasses the channel. No action is done on the data flow. Default value: FALSE |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Table 186: HO POH Monitor - Channel Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----------|---|--------|--|
| 2 | 0 | J1_ExTiMessage | 0x01A8 | Selects between repeating non-specific byte (value: FALSE) and other message formats (value: TRUE). Default value: FALSE |
| | 1 | J1_ExTi64 | | Selects between 64-byte trace message (value: TRUE) and 16-byte trace message (value: FALSE). Default value: FALSE |
| | 2 | J1_TimEnable | | Enable TIM Detection. Default value: FALSE |
| | 6-3 | J1_NrOfFramesToSetTim | | Number of consecutive mismatched multiframes to set TIM. Default value: 5 |
| | 10-7 | J1_NrOfFramesToResetTim | | Number of consecutive matched multiframes to clear TIM. Default value: 3 |
| 4 | 6-0 | J1_CRC_Seed | 0x0000 | CRC Seed value for the J1 CRC check. Default value: 0x0 |
| | 7 | J1_CRCEnable | | Enables CRC check. Default value: FALSE |
| 6 | 3-0 | J1_NrOfFramesToSetStable64 | 0x0043 | Number of consecutive matched multiframes to set Stable64. Default value: 3 |
| | 7-4 | J1_NrOfFramesToSetStable16 | | Number of consecutive matched multiframes to set Stable16. Default value: 4 |
| 8 | 12-0 | B3_SetThreshold | 0x0001 | Number of errored blocks that may occur in an interval to be considered as a BAD interval. Default value: 1 |
| a | 12-0 | B3_ClearThreshold | 0x0001 | Number of errored blocks that may occur in an interval to be considered as a GOOD interval. Default value: 1 |
| c | 3-0 | B3_SetNrOfIntervals | 0x0022 | Number of consecutive BAD intervals to declare a degraded signal defect. Default value: 2 |
| | 7-4 | B3_ClearNrOfIntervals | | Number of consecutive GOOD intervals to clear the degraded signal defect. Default value: 2 |
| e | 3-0 | G1_AcceptNrOfIntervals | 0x0005 | Number of consecutive frames to debounce G1. Default value: 5 |
| 10 | 1-0 | H4_MultiFrameType | 0x0014 | Type of H4_Multiframe that the H4 Finite State Machine (FSM) looks for. Default value: H4_MF_NONE (00). Possible values: H4_MF_NONE (00), H4_MF_LO (01), H4_MF_VC (10) |
| | 5-2 | H4_MsToSetLOM | | Number of ms that the OOM (OOM1 or OOM2) state must persist tot declare the LOM defect. Default value: 5 |
| 12 | 0 | AIS_SSF_Disable | 0x0000 | Disables AIS insertion on SSF. Default value: FALSE |
| | 1 | AIS_TIM_Disable | | Disables AIS insertion due to the TIM defect. Default value: FALSE |
| | 2 | AIS_IncAIS_Disable | | Disables AIS insertion due to Incoming AIS defect. Default value: FALSE |
| | 3 | AIS_UNEQ_Disable | | Disables AIS insertion due to UNEQ defect. Default value: FALSE |
| | 4 | TSF_TIM_Disable | | Disables TSF action due to TIM defect. Default: FALSE |
| | 5 | TSF_IncAIS_Disable | | Disables TSF action due to Incoming AIS defect. Default value: FALSE |
| | 6 | TSF_UNEQ_Disable | | Disables TSF action due to UNEQ defect. Default value: FALSE |
| | 7 | PLM_PLM_Disable | | Disables PLM action due to PLM defect. Default value: FALSE |
| | 8 | RDI_SSF_Disable | | Disables RDI action due to SSF defect. Default value: FALSE |
| | 9 | RDI_UNEQ_Disable | | Disables RDI action due to UNEQ defect. Default value: FALSE |
| | 10 | RDI_TIM_Disable | | Disables RDI action due to TIM defect. Default value: FALSE |
| | 11 | RDI_PLM_Disable | | Disables RDI action due to PLM defect. Default value: FALSE |
| | 12 | LOM_LOM_Disable | | Disables LOM action due to LOM defect. Default value: FALSE |
| 13 | InsertAIS | Software forced AIS insertion. Default value: FALSE | | |

Bits in register 0x14804 disable consequent actions when they are set to one. See [Mapper/Demapper Consequent Actions per Block](#) beginning on [page 390](#) for more details. In general, consequent actions should always be enabled. Specifically, if the SSF, UNEQ, AIS, LOM or PLM actions are disabled (bits 0,2,3,5,6,7 or 12 set to one), it is possible to observe sink side traffic loss during LCAS deprovisioning.

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f680 | 0x1d900 | 0x1d920 | 0x1d940 |

Table 187: HO POH Monitor - Channel Status (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-------------------------|--------|--|
| 0 | 0 | PohRamWriteInSecondBank | 0x0000 | Indicates if the received POH bytes are written into the second RAM bank |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f758 | 0x1dcc0 | 0x1dcc2 | 0x1dcc4 |

Table 188: HO POH Monitor - Channel Defects (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|------------|--------|----------------------------------|
| 0 | 0 | CI_SSF | 0x0000 | Incoming SSF defect |
| | 1 | J1_TIM | | TIM defect |
| | 2 | J1_TTIZERO | | TTIZero defect |
| | 3 | J1_CRC | | CRC defect |
| | 4 | B3_DEG | | Degraded signal defect |
| | 5 | C2_PLM | | PLM defect |
| | 6 | C2_UNEQ | | UNEQ defect |
| | 7 | C2_VC_AIS | | Incoming AIS defect |
| | 8 | G1_RDI | | Incoming RDI defect |
| | 9 | G1_RDI_S | | Incoming Server RDI defect |
| | 10 | G1_RDI_C | | Incoming Connectivity RDI defect |
| | 11 | G1_RDI_P | | Incoming Payload RDI defect |
| | 12 | H4_LOM | | LOM defect |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f75c | 0x1dcd0 | 0x1dcd2 | 0x1dcd4 |

Table 189: HO POH Monitor - J1 Message Status (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|--------------|--------|--|
| 0 | 0 | J1_Stable_1 | 0x0000 | Indication that the J1 trail message contains a stable1 message |
| | 1 | J1_Stable_16 | | Indication that the J1 trail message contains a stable16 message |
| | 2 | J1_Stable_64 | | Indication that the J1 trail message contains a stable64 message |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|--------------------|-------------------|
| Base Address | 0x1f760 | 0x1dc50 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 190: HO POH Monitor - Defects (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------|
| 0 | 0 | SSF | 0x0000 | SSF Correlated defect |
| | 1 | TIM | | TIM Correlated defect |
| | 2 | TTIZERO | | TTIZERO Correlated defect |
| | 3 | CRC | | CRC Correlated defect. |
| | 4 | DEG | | DEG Correlated defect. |
| | 5 | PLM | | PLM Correlated defect. |
| | 6 | UNEQ | | UNEQ Correlated defect. |
| | 7 | IncAIS | | IncAIS Correlated defect. |
| | 8 | RDI | | RDI Correlated defect. |
| | 9 | RDI_S | | RDI_S Correlated defect. |
| | 10 | RDI_C | | RDI_C Correlated defect. |
| | 11 | RDI_P | | RDI_P Correlated defect. |
| | 12 | LOM | | LOM Correlated defect. |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f764 | 0x1dce0 | 0x1dce2 | 0x1dce4 |

Table 191: HO POH Monitor - Latched Defects (R/COW-1)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------|
| 0 | 0 | SSF | 0x0000 | SSF Correlated defect |
| | 1 | TIM | | TIM Correlated defect |
| | 2 | TTIZERO | | TTIZERO Correlated defect |
| | 3 | CRC | | CRC Correlated defect. |
| | 4 | DEG | | DEG Correlated defect. |
| | 5 | PLM | | PLM Correlated defect. |
| | 6 | UNEQ | | UNEQ Correlated defect. |
| | 7 | IncAIS | | IncAIS Correlated defect. |
| | 8 | RDI | | RDI Correlated defect. |
| | 9 | RDI_S | | RDI_S Correlated defect. |
| | 10 | RDI_C | | RDI_C Correlated defect. |
| | 11 | RDI_P | | RDI_P Correlated defect. |
| | 12 | LOM | | LOM Correlated defect. |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f768 | 0x1dcf0 | 0x1dcf2 | 0x1dcf4 |

Table 192: HO POH Monitor - Defect Masks (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---|
| 0 | 0 | SSF | 0x1FFF | Mask setting for the SSF correlated defect. Default value: TRUE |
| | 1 | TIM | | Mask setting for the TIM correlated defect. Default value: TRUE |
| | 2 | TTIZERO | | Mask setting for the TTIZERO correlated defect. Default value: TRUE |
| | 3 | CRC | | Mask setting for the CRC correlated defect. Default value: TRUE |
| | 4 | DEG | | Mask setting for the DEG correlated defect. Default value: TRUE |
| | 5 | PLM | | Mask setting for the PLM correlated defect. Default value: TRUE |
| | 6 | UNEQ | | Mask setting for the UNEQ correlated defect. Default value: TRUE |
| | 7 | IncAIS | | Mask setting for the IncAIS correlated defect. Default value: TRUE |
| | 8 | RDI | | Mask setting for the RDI correlated defect. Default value: TRUE |
| | 9 | RDI_S | | Mask setting for the RDI_S correlated defect. Default value: TRUE |
| | 10 | RDI_C | | Mask setting for the RDI_C correlated defect. Default value: TRUE |
| | 11 | RDI_P | | Mask setting for the RDI_P correlated defect. Default value: TRUE |
| | 12 | LOM | | Mask setting for the LOM correlated defect. Default value: TRUE |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f76c | 0x1dd00 | 0x1dd02 | 0x1dd04 |

Table 193: HO POH Monitor - Defects Latched For PMFM (R/COW-0)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------|
| 0 | 0 | SSF | 0x0000 | SSF Correlated defect |
| | 1 | TIM | | TIM Correlated defect |
| | 2 | TTIZERO | | TTIZERO Correlated defect |
| | 3 | CRC | | CRC Correlated defect. |
| | 4 | DEG | | DEG Correlated defect. |
| | 5 | PLM | | PLM Correlated defect. |
| | 6 | UNEQ | | UNEQ Correlated defect. |
| | 7 | IncAIS | | IncAIS Correlated defect. |
| | 8 | RDI | | RDI Correlated defect. |
| | 9 | RDI_S | | RDI_S Correlated defect. |
| | 10 | RDI_C | | RDI_C Correlated defect. |
| | 11 | RDI_P | | RDI_P Correlated defect. |
| | 12 | LOM | | LOM Correlated defect. |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f770 | 0x1dd10 | 0x1dd12 | 0x1dd14 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 194: HO POH Monitor - Defects PM (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------|
| 0 | 0 | SSF | 0x0000 | SSF Correlated defect |
| | 1 | TIM | | TIM Correlated defect |
| | 2 | TTIZERO | | TTIZERO Correlated defect |
| | 3 | CRC | | CRC Correlated defect. |
| | 4 | DEG | | DEG Correlated defect. |
| | 5 | PLM | | PLM Correlated defect. |
| | 6 | UNEQ | | UNEQ Correlated defect. |
| | 7 | IncAIS | | IncAIS Correlated defect. |
| | 8 | RDI | | RDI Correlated defect. |
| | 9 | RDI_S | | RDI_S Correlated defect. |
| | 10 | RDI_C | | RDI_C Correlated defect. |
| | 11 | RDI_P | | RDI_P Correlated defect. |
| | 12 | LOM | | LOM Correlated defect. |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f774 | 0x1dd20 | 0x1dd22 | 0x1dd24 |

Table 195: HO POH Monitor - Defects FM (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------|
| 0 | 0 | SSF | 0x0000 | SSF Correlated defect |
| | 1 | TIM | | TIM Correlated defect |
| | 2 | TTIZERO | | TTIZERO Correlated defect |
| | 3 | CRC | | CRC Correlated defect. |
| | 4 | DEG | | DEG Correlated defect. |
| | 5 | PLM | | PLM Correlated defect. |
| | 6 | UNEQ | | UNEQ Correlated defect. |
| | 7 | IncAIS | | IncAIS Correlated defect. |
| | 8 | RDI | | RDI Correlated defect. |
| | 9 | RDI_S | | RDI_S Correlated defect. |
| | 10 | RDI_C | | RDI_C Correlated defect. |
| | 11 | RDI_P | | RDI_P Correlated defect. |
| | 12 | LOM | | LOM Correlated defect. |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f778 | 0x1dd30 | 0x1dd32 | 0x1dd34 |

Table 196: HO POH Monitor - Defect Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------------------------|--------|--|
| 0 | 0 | SSF_IncAIS_Disable | 0x0000 | Disables the contribution of dC2_VC_AIS to cSSF. Default value: FALSE |
| | 1 | UNEQ_SSF_Inhibit_Disable | | Disables the inhibition of dC2_UNEQ by CI_SSF. Default value: FALSE |
| | 2 | UNEQ_TIM_Disable | | Disables the inhibition of dC2_UNEQ by dJ1_TIM. Default value: FALSE |
| | 3 | UNEQ_TTIZERO_Disable | | Disables the inhibition of dC2_UNEQ by dJ1_TTIZERO. Default value: FALSE |
| | 4 | TIM_SSF_Inhibit_Disable | | Disables the inhibition of dJ1_TIM by CI_SSF. Default value: FALSE |
| | 5 | TIM_UNEQ_Inhibit_Disable | | Disables the inhibition of dJ1_TIM by dC2_UNEQ. Default value: FALSE |
| | 6 | TIM_TTIZERO_Inhibit_Disable | | Disables the inhibition of dJ1_TIM by dJ1_TTIZERO. Default value: FALSE |
| | 7 | TTIZERO_SSF_Inhibit_Disable | | Disables the inhibition of dJ1_TTIZERO by CI_SSF. Default value: FALSE |
| | 8 | CRC_SSF_Inhibit_Disable | | Disables the inhibition of dJ1_CRC by CI_SSF. Default value: FALSE |
| | 9 | CRC_UNEQ_Inhibit_Disable | | Disables the inhibition of dJ1_CRC by dC2_UNEQ. Default value: FALSE |
| | 10 | CRC_TTIZERO_Inhibit_Disable | | Disables the inhibition of dJ1_CRC by dJ1_TTIZERO. Default value: FALSE |
| | 11 | DEG_SSF_Inhibit_Disable | | Disables the inhibition of dB3_DEG by CI_SSF. Default value: FALSE |
| | 12 | DEG_TIM_Inhibit_Disable | | Disables the inhibition of dB3_DEG by dJ1_TIM. Default value: FALSE |
| | 13 | PLM_TSF_Inhibit_Disable | | Disables the inhibition of dC2_PLM by AI_TSF. Default value: FALSE |
| 2 | 0 | RDI_SSF_Inhibit_Disable | 0x0000 | Disables the inhibition of dG1_RDI, dG1_RDI_S, dG1_RDI_P and dG1_RDI_C by CI_SSF. Default value: FALSE |
| | 1 | RDI_UNEQ_Inhibit_Disable | | Disables the inhibition of dG1_RDI, dG1_RDI_S, dG1_RDI_P and dG1_RDI_C by dC2_UNEQ. Default value: FALSE |
| | 2 | RDI_TIM_Inhibit_Disable | | Disables the inhibition of dG1_RDI, dG1_RDI_S, dG1_RDI_P and dG1_RDI_C by CI_SSF. Default value: FALSE |
| | 3 | RDI_TTIZERO_Inhibit_Disable | | Disables the inhibition of dG1_RDI, dG1_RDI_S, dG1_RDI_P and dG1_RDI_C by CI_SSF. Default value: FALSE |
| | 4 | LOM_TSF_Inhibit_Disable | | Disables the inhibition of dH4_LOM by AI_TSF. Default value: FALSE |
| | 5 | LOM_PLM_Inhibit_Disable | | Disables the inhibition of dH4_LOM by dC2_PLM. Default value: FALSE |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f748 | 0x1dc80 | 0x1dc84 | 0x1dc88 |

Table 197: HO POH Monitor - Defect Summary (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-------------|--------|---|
| 0 | 0 | LatchForInt | 0x0000 | Per channel latch Bit for interrupt summary |
| | 1 | PM | | Per channel PM summary |
| | 2 | FM | | Per channel FM summary |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f77c | 0x1dd40 | 0x1dd42 | 0x1dd44 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 198: HO POH Monitor - Defect Summary Mask (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---|
| 0 | 0 | Mask | 0x0001 | Mask Bit for the latch Bit for interrupt summary per channel. Default value: TRUE |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f600 | 0x1dd50 | 0x1dd52 | 0x1dd54 |

Table 199: HO POH Monitor - Defect Group Summary (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---|
| 0 | 0 | Interrupt | 0x0000 | Latch for interrupt summary for the per channel defects |
| 2 | 0 | PM | 0x0000 | PM summary for the per channel defects |
| 4 | 0 | FM | 0x0000 | FM summary for the per channel defects |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|-------------|------------|
| Base Address | 0x1f700 | 0x1dd60 |

Table 200: HO POH Monitor - APS Event (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|-----------------------|
| 0 | 0 | K3_APS | 0x0000 | K3_APS event detected |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f608 | 0x1dd70 | 0x1dd72 | 0x1dd74 |

Table 201: HO POH Monitor - Latched APS Event (R/COW-1)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---------------------------------|
| 0 | 0 | K3_APS | 0x0000 | K3_APS event detected (latched) |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f610 | 0x1dd80 | 0x1dd82 | 0x1dd84 |

Table 202: HO POH Monitor - APS Event Mask (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|-------------------|
| 0 | 0 | K3_APS | 0x0001 | K3_APS event mask |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f618 | 0x1dd90 | 0x1dd92 | 0x1dd94 |

Table 203: HO POH Monitor - APS Interrupt (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---|
| 0 | 0 | Interrupt | 0x0000 | Interrupt summary of the K3_APS event of all channels |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|--------------------|-------------------|
| Base Address | 0x1f620 | 0x1dc58 |

Table 204: HO POH Monitor - Performance Counters (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|------|-----------------------------|--------|------------------------------|
| 0 | 12-0 | B3_NearEndBlockErrorCounter | 0x0000 | Near End Block Error Counter |
| 2 | 15-0 | G1_FarEndBlockErrorCounter | 0x0000 | Far End Block Error Counter |
| 4 | 15-0 | B3_BIP_ErrorCounter | 0x0000 | Near End Bip Error Counter |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f710 | 0x1ddc0 | 0x1ddc8 | 0x1ddd0 |

Table 205: HO POH Monitor - Performance Counters One Second Latch (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|----------------------|
| 0 | 0 | NDS | 0x0000 | TSF one second latch |
| | 1 | FDS | | RDI one second latch |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f628 | 0x1dda0 | 0x1dda2 | 0x1dda4 |

Table 206: HO POH Monitor - Performance Counter Shadow Registers (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|------|-----------------------------|--------|------------------------------|
| 0 | 12-0 | B3_NearEndBlockErrorCounter | 0x0000 | Near End Block Error Counter |
| 2 | 15-0 | G1_FarEndBlockErrorCounter | 0x0000 | Far End Block Error Counter |
| 4 | 15-0 | B3_BIP_ErrorCounter | 0x0000 | Near End Bip Error Counter |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1f720 | 0x1dde0 | 0x1dde8 | 0x1ddf0 |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 207: HO POH Monitor - Performance Counter Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|---------------------------------|--------|---|
| 0 | 0 | G1_CountBlockErrorsNotBitErrors | 0x0001 | Enables counting of block errors for the far end block error counters Bit errors. Default value: TRUE |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1f630 | 0x1ddb0 | 0x1ddb2 | 0x1ddb4 |

Table 208: HO POH Monitor - Counter Reset (WO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|---------------|--------|--|
| 0 | 7-0 | ResetCounters | 0x0000 | Reset all performance counters of the block when 0x91 is written to this Address. Default value: 0x0 |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|-------------|------------|
| Base Address | 0x1f638 | 0x1dca0 |

Table 209: HO POH Monitor - PMFM Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------------------|--------|--|
| 0 | 0 | Reserved | 0x0006 | Reserved: this field must be FALSE (0) for correct operation. |
| | 1 | ShadowRegister_Enable | | Enables the shadowing of the performance counters. Default value: TRUE |
| | 3-2 | IntEventControl | | Interrupt latch condition. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 5-4 | PM_EventControl | | PM,FM latch condition. Default value: PM_DISABLED. Possible values: PM_DISABLED (00), PM_RISING_EDGE (01), PM_FALLING_EDGE (10), PM_BOTH_EDGES (11) |

| | VC-4/STS-3c | VC-3/STS-1 |
|--------------|-------------|------------|
| Base Address | 0x1f730 | 0x1dca8 |

Tables 210 through 222 - Configuration, Status and Alarms of the TU-3 PTR Tracker

Table 210: TU-3 PTR Tracker - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------------|--------|--|
| 0x19c00 | 0 | Reserved | 0x000A | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Configure on which transitions the Interrupt latching occurs. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 4-3 | PMFMEventControl | | Configure on which transitions the PM/FM latching occurs 00: PM/FM disabled 01: Rising edge 10: Falling edge 11: Both edges |
| 0x19c02 | 7-0 | ResetPerfCounters | 0x0000 | Reset all performance counters by writing 0x91 to this register |

Table 211: TU-3 PTR Tracker - Per Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|--------------------|--------------------------|---|--------|--|
| 0x19c80 | 0 | AUG1_Format | 0 | 0x0001 | Timeslot belongs to either AU-3 (0) or AU-4 (1) ^a |
| 0x19c90 | 1 | TUG3_Format | 1 | | |
| 0x19ca0 | | | 2 | | |
| 0x19c82 | 1-0 | SS_Reference | 0 | 0x000E | Pointer Interpreter FSM will expect these Bits as SS-Bits |
| 0x19c92 | 2 | SS_Check_Enable | 1 | | If enabled, received SS-Bits are also checked by the Pointer Interpreter FSM against the SS_Reference Bits |
| 0x19ca2 | 3 | AIS2LOP_Enable | 2 | | If enabled, AIS to LOP transition is possible |
| 0x19c84 | 0 | InsertAIS_On_PLM_Disable | 0 | 0x0000 | If FALSE, AIS will be inserted when PLM is detected |
| 0x19c94 | 1 | InsertAIS_On_LOP_Disable | 1 | | If FALSE, AIS will be inserted when LOP is detected |
| 0x19ca4 | 2 | InsertAIS_On_AIS_Disable | 2 | | If FALSE, AIS will be inserted when AIS is detected |
| | 3 | InsertAIS_On_TSF_Disable | | | If FALSE, AIS will be inserted when TSF is detected |
| | 4 | SSF_On_PLM_Disable | | | If FALSE, SSF will be asserted when PLM is detected |
| | 5 | SSF_On_LOP_Disable | | | If FALSE, SSF will be asserted when LOP is detected |
| | 6 | SSF_On_AIS_Disable | | | If FALSE, SSF will be asserted when AIS is detected |
| 7 | SSF_On_TSF_Disable | | If FALSE, SSF will be asserted when TSF is detected | | |
| 0x19c86 | 0 | TSF_Inhibits_AIS | 0 | 0x0007 | If TRUE, TSF inhibits generation of Correlated AIS Defect |
| 0x19c96 | 1 | PLM_Inhibits_AIS | 1 | | If TRUE, PLM inhibits generation of Correlated AIS Defect |
| 0x19ca6 | 2 | PLM_Inhibits_LOP | 2 | | If TRUE, PLM inhibits generation of Correlated LOP Defect |
| 0x19c88 | 0 | SW_InsertAIS | 0 | 0x0000 | Force AIS Insertion through software; only valid in AU-4/VC-4/TUG-3/TU-3 format |
| 0x19c98 | 1 | | 1 | | |
| 0x19ca8 | 2 | | 2 | | |

a. See [Table 1, "TU-3 Pointer Tracker/Retimer Modes,"](#) on page 96

b. See [Table 1, "TU-3 Pointer Tracker/Retimer Modes,"](#) on page 96

Table 212: TU-3 PTR Tracker - Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c10 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c12 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c14 | | | 2 | | |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 213: TU-3 PTR Tracker - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c20 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c22 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c24 | | | 2 | | |

Table 214: TU-3 PTR Tracker - Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c30 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c32 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c34 | | | 2 | | |

Table 215: TU-3 PTR Tracker - Defects PM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c40 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c42 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c44 | | | 2 | | |

Table 216: TU-3 PTR Tracker - Defects FM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c50 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c52 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c54 | | | 2 | | |

Table 217: TU-3 PTR Tracker - Defect Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|---------------|-------|--------|---------------------------------|
| 0x19c60 | 0 | LossOfPointer | 0 | 0x0000 | LossOfPointer Correlated Defect |
| 0x19c62 | 1 | AIS_Detected | 1 | | AIS Correlated Defect |
| 0x19c64 | | | 2 | | |

Table 218: TU-3 PTR Tracker - Defect Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x19c70 | 2-0 | LatchForInt | 0x0000 | Per Channel Latched For Interrupt Defect Summary |
| 0x19c72 | 2-0 | PM | 0x0000 | Per Channel Performance Monitoring Defect Summary |
| 0x19c74 | 2-0 | FM | 0x0000 | Per Channel Fault Monitoring Defect Summary |

Table 219: TU-3 PTR Tracker - Defect Summary Mask (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|----------------|---|
| 0x19cc0 | 2-0 | LatchForInt | Not Applicable | Per Channel Latched For Interrupt Defect Summary |
| 0x19cc2 | 2-0 | PM | | Per Channel Performance Monitoring Defect Summary |
| 0x19cc4 | 2-0 | FM | | Per Channel Fault Monitoring Defect Summary |

Table 220: TU-3 PTR Tracker - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--------------------------------------|
| 0x19cd0 | 0 | Interrupt | 0x0000 | Latched For Interrupt Defect Summary |

Table 220: TU-3 PTR Tracker - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---------------------------------------|
| 0x19cd2 | 0 | PM | 0x0000 | Performance Monitoring Defect Summary |
| 0x19cd4 | 0 | FM | 0x0000 | Fault Monitoring Defect Summary |

Table 221: TU-3 PTR Tracker - Performance Counters (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|--------------|-------------|--------|---|
| 0x19ce0 0x19ce4 0x19ce8 | 7-0 | NegJustCount | 0 1 2 | 0x0000 | Raw count of incoming TU-3 Pointer Negative Justifications (Decrements) |
| 0x19ce2 0x19ce6 0x19cea | 7-0 | PosJustCount | 0 1 2 | 0x0000 | Raw count of incoming TU-3 Pointer Positive Justifications (Increments) |

Table 222: TU-3 PTR Tracker - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|--------------|-------------|--------|--|
| 0x19cf0 0x19cf4 0x19cf8 | 7-0 | NegJustCount | 0 1 2 | 0x0000 | One second count of incoming TU-3 Pointer Negative Justifications (Decrements) |
| 0x19cf2 0x19cf6 0x19cfa | 7-0 | PosJustCount | 0 1 2 | 0x0000 | One second count of incoming TU-3 Pointer Positive Justifications (Increments) |

Tables 223 and 224 - Configuration of TU-3 Cross Connect

Table 223: Transmit VC-3/STS-1/TUG-3 Time Slot Interchange (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|------------|-------------|--------|--|
| 0x1d700 0x1d708 0x1d710 | 1-0 | SourceSlot | 0 1 2 | 0x0000 | Selection of the source timeslot for this output timeslot. Range: 0 to 2. Default value: 0 |
| 0x1d702 0x1d70a 0x1d712 | 1-0 | SourceBus | 0 1 2 | 0x0000 | Selection of the source bus for this output timeslot. Default value: 0 |
| 0x1d704 0x1d70c 0x1d714 | 0 | ForceUneq | 0 1 2 | 0x0001 | Force unequipped on this output timeslot. Default value: TRUE |
| 0x1d706 0x1d70e 0x1d716 | 0 | ForceAIS | 0 1 2 | 0x0000 | Force AIS on this output timeslot. Default value: FALSE |

Table 224: Receive VC-3/STS-1/TUG-3 Time Slot Interchange (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|------------|-------------|--------|--|
| 0x1d720 0x1d728 0x1d730 | 1-0 | SourceSlot | 0 1 2 | 0x0000 | Selection of the source timeslot for this output timeslot. Range 0 to 2. Default value: 0 |
| 0x1d722 0x1d72a 0x1d732 | 1-0 | SourceBus | 0 1 2 | 0x0000 | Selection of the source bus for this output timeslot: 0x0001 selects the bus from the Level 3 retimer, 0x0002 selects the not substructured VC-4 bypass. |



Table 224: Receive VC-3/STS-1/TUG-3 Time Slot Interchange (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|---|
| 0x1d724 0x1d72c 0x1d734 | 0 | ForceUneq | 0 1 2 | 0x0001 | Force unequipped on this output timeslot. Default value: TRUE |
| 0x1d726 0x1d72e 0x1d736 | 0 | ForceAIS | 0 1 2 | 0x0000 | Force AIS on this output timeslot. Default value: FALSE |

Tables 225 through 237 - Configuration, Status and Alarms of the TU-3 PTR Generator

Table 225: TU-3 PTR Generator - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------------|--------|---|
| 0x19e40 | 0 | Reserved | 0x000A | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Configure on which transitions the Interrupt latching occurs. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 4-3 | PMFMEventControl | | Configure on which transitions the PM/FM latching occurs 00: PM/FM disabled 01: Rising edge 10: Falling edge 11: Both edges |
| 0x19e42 | 7-0 | ResetPerfCounters | 0x0000 | Reset all performance counters by writing 0x91 to this register |
| 0x19e44 | 9-0 | AU4_FixedPointer | 0x0000 | Set AU-4 pointer used in AU3_TO_AU4 mode |

Table 226: TU-3 PTR Generator - Per Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|--------------------------------|-------|--------|--|
| 0x19ee0 0x19ee8 0x19ef0 | 2-0 | ConversionType | 0 | 0x0000 | Configure mapping per VC-3/STS-1/TUG-3 time slot. ^a |
| 0x19ee2 0x19eea 0x19ef2 | 1-0 | SS_Reference | 0 | 0x0002 | Use this reference to fill in SS Bits in TU-3 pointer |
| 0x19ee4 0x19eec 0x19ef4 | 0 | InsertAIS_On_FifoError_Disable | 0 | 0x0000 | Disable AIS Insertion when FIFO error is detected |
| | 1 | InsertAIS_On_SSF_Disable | | | Disable AIS Insertion when incoming SSF is detected |
| 0x19ee6 0x19eee 0x19ef6 | 0 | SW_InsertAIS | 0 | 0x0000 | Force AIS Insertion through software |

a. See Table 2, "TU-3 Pointer Generator Modes," on page 96

Table 227: TU-3 PTR Generator - Defects (RO)

| Address | Bit | HW Symbol | SW symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-----------|-------------|--------|--------------------------------------|
| 0x19e50 0x19e52 0x19e54 | 0 | FifoError | Defects | 0 1 2 | 0x0000 | Fifo Over- or Underflow has occurred |

Table 228: TU-3 PTR Generator - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x19e60 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x19e62 | | | 1 | | |
| 0x19e64 | | | 2 | | |

Table 229: TU-3 PTR Generator - Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x19e70 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x19e72 | | | 1 | | |
| 0x19e74 | | | 2 | | |

Table 230: TU-3 PTR Generator - Defects PM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x19e80 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x19e82 | | | 1 | | |
| 0x19e84 | | | 2 | | |

Table 231: TU-3 PTR Generator - Defects FM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x19e90 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x19e92 | | | 1 | | |
| 0x19e94 | | | 2 | | |

Table 232: TU-3 PTR Generator - Defect Mask (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x19ea0 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x19ea2 | | | 1 | | |
| 0x19ea4 | | | 2 | | |

Table 233: TU-3 PTR Generator - Defect Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x19eb0 | 2-0 | LatchForInt | 0x0000 | Per Channel Latched For Interrupt Defect Summary |
| 0x19eb2 | 2-0 | PM | 0x0000 | Per Channel Performance Monitoring Defect Summary |
| 0x19eb4 | 2-0 | FM | 0x0000 | Per Channel Fault Monitoring Defect Summary |

Table 234: TU-3 PTR Generator - Defect Summary Mask (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|----------------|---|
| 0x19ec0 | 2-0 | LatchForInt | Not Applicable | Per Channel Latched For Interrupt Defect Summary |
| 0x19ec2 | 2-0 | PM | | Per Channel Performance Monitoring Defect Summary |
| 0x19ec4 | 2-0 | FM | | Per Channel Fault Monitoring Defect Summary |

Table 235: TU-3 PTR Generator - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--------------------------------------|
| 0x19ed0 | 0 | Interrupt | 0x0000 | Latched For Interrupt Defect Summary |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 235: TU-3 PTR Generator - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---------------------------------------|
| 0x19ed2 | 0 | PM | 0x0000 | Performance Monitoring Defect Summary |
| 0x19ed4 | 0 | FM | 0x0000 | Fault Monitoring Defect Summary |

Table 236: TU-3 PTR Generator - Performance Counters (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|--------------|-------------|--------|---|
| 0x19e00 0x19e04 0x19e08 | 7-0 | NegJustCount | 0 1 2 | 0x0000 | Count of outgoing TU-3 Pointer Negative Justifications (Decrements) |
| 0x19e02 0x19e06 0x19e0a | 7-0 | PosJustCount | 0 1 2 | 0x0000 | Count of outgoing TU-3 Pointer Positive Justifications (Increments) |

Table 237: TU-3 PTR Generator - Performance Counter Shadow Registers (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|--------------|-------------|--------|---|
| 0x19e20 0x19e24 0x19e28 | 7-0 | NegJustCount | 0 1 2 | 0x0000 | Count of outgoing TU-3 Pointer Negative Justifications (Decrements) |
| 0x19e22 0x19e26 0x19e2a | 7-0 | PosJustCount | 0 1 2 | 0x0000 | Count of outgoing TU-3 Pointer Positive Justifications (Increments) |

Tables 238 through 242 - Configuration of High Order (VC-3 and VC-4) POH Generator

Table 238: HO POH Generator - Channel Control (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|--------------|--------|---|
| 0 | 0 | ForceAIS | 0x0000 | Forces insertion of AIS in the corresponding channel |
| | 1 | ForceUneq | | Forces insertion of Unequipped in the corresponding channel |
| | 2 | ForceSupUneq | | Forces insertion of Supervisory Unequipped in the corresponding channel |
| | 3 | PassPOH | | When set the incoming channel is passed untouched |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1d058 | 0x1f960 | 0x1f962 | 0x1f964 |

Table 239: HO POH Generator - Configuration (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-------|-------------------|--------|---|
| 0 | 0 | J1_Length64 | 0x0000 | When set the length of the TTI message inserted in J1 is 64 bytes |
| | 1 | B3_Masking | | When set the B3 Byte is masked with the value in the POH RAM |
| | 2 | G1_UniDirectional | | When set the Unidirectional option is activated |
| | 3 | OneBitRDI | | When set the RDI is encoded in 1 Bit |
| | 5-4 | G1_REI_Control | | Select the source of the G1 REI, POH RAM (00=default), POH port (01) or Alarm Indication Port (10) |
| | 7-6 | G1_RDI_Control | | Select the source of the G1 RDI, POH RAM (00=default), POH port (01) or Alarm Indication Port (10) |
| | 8 | G1_SPARE_Control | | Select the source of the G1 SPARE Bit, POH RAM (0=default) or POH port (1) |
| | 9 | F2_Control | | Select the source of the F2 Byte, POH RAM (0=default) or POH port (1) |
| | 11-10 | H4_Control | | Select the source of the H4 Byte, POH RAM (00=default), POH port (01), pass through (10), or generate (11). |
| | 12 | F3_Control | | Select the source of the F3/Z3 Byte, POH RAM (0=default) or POH port (1) |
| | 13 | K3_Control | | Select the source of the K3/Z4 Byte, POH RAM (0=default) or POH port (1) |
| | 14 | N1_Control | | Select the source of the N1/Z5 Byte, POH RAM (0=default) or POH port (1) |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1d040 | 0x1f900 | 0x1f902 | 0x1f904 |

Table 240: HO POH Generator - J1 Message Bytes (RW)

| Offset | Bit | HW Symbol | Index | Init | Description |
|----------------------------------|-----|-----------|-------|--------|---|
| 0x00-0x7e (increment by 0x02) | 7-0 | value | 0-63 | 0x0000 | TTI-message byte for insertion in the J1 location |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1d080 | 0x1fa00 | 0x1fa80 | 0x1fb00 |

Table 241: HO POH Generator - POH Insertion Values (RW)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|--|
| 0 | 7-0 | B3 | 0x0000 | Mask used on the B3 byte if B3_Masking is enabled. |
| 2 | 7-0 | C2 | 0x0000 | Signal label to be inserted. |
| 4 | 7-0 | G1 | 0x0000 | Value used when G1 is inserted out of RAM |
| 6 | 7-0 | F2 | 0x0000 | Value used when F2 is inserted out of RAM |
| 8 | 7-0 | H4 | 0x0000 | Value used when H4 is inserted out of RAM |
| a | 7-0 | F3 | 0x0000 | Value used when F3/Z3 is inserted out of RAM |
| c | 7-0 | K3 | 0x0000 | Value used when K3/Z4 is inserted out of RAM |
| e | 7-0 | N1 | 0x0000 | Value used when N1/Z5 is inserted out of RAM |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|--------------------|----------------------|----------------------|----------------------|
| Base Address | 0x1d000 | 0x1f800 | 0x1f810 | 0x1f820 |



Table 242: HO POH Generator - POH Port Monitors (RO)

| Offset | Bit | HW Symbol | Init | Description |
|--------|-----|-----------|--------|---|
| 0 | 7-0 | G1 | 0x0000 | Value received from the POH Port for insertion in G1 |
| 2 | 7-0 | F2 | 0x0000 | Value received from the POH Port for insertion in F2 |
| 4 | 7-0 | H4 | 0x0000 | Value received from the POH Port for insertion in H4 |
| 6 | 7-0 | F3 | 0x0000 | Value received from the POH Port for insertion in F3/Z3 |
| 8 | 7-0 | K3 | 0x0000 | Value received from the POH Port for insertion in K3/Z4 |
| a | 7-0 | N1 | 0x0000 | Value received from the POH Port for insertion in N1/Z5 |

| | VC-4/STS-3c | VC-3/STS-1 #1 | VC-3/STS-1 #2 | VC-3/STS-1 #3 |
|--------------|-------------|---------------|---------------|---------------|
| Base Address | 0x1d060 | 0x1f980 | 0x1f990 | 0x1f9a0 |

Tables 243 through 250 - Configuration, Status and Alarms of the TU-3 Retimer

Table 243: TU-3 Retimer - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|------------------|--------|---|
| 0x1e5a0 | 0 | Reserved | 0x0002 | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Configure on which transitions Latching For Interrupt occurs. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| 0x1e5a2 | 0 | DisableSequencer | 0x0001 | Turn off Sequencer (For instance when writing to program RAM) |
| 0x1e5a4 | 11-0 | FrameOffset | 0x0000 | Configure offset of Frame Start to FrameRefPulse. Set to 0x97D. |

Table 244: TU-3 Retimer - Per Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|--------------------------|-------|--------|---|
| 0x1e5c0 | 1 | InsertAIS_On_SSF_Disable | 0 | 0x0000 | Disable AIS Insertion when incoming SSF is detected |
| 0x1e5c4 | | | 1 | | |
| 0x1e5c8 | | | 2 | | |
| 0x1e5c2 | 0 | SW_InsertAIS | 0 | 0x0000 | Force AIS Insertion through software |
| 0x1e5c6 | | | 1 | | |
| 0x1e5ca | | | 2 | | |

Table 245: TU-3 Retimer - Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x1e400 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x1e402 | | | 1 | | |
| 0x1e404 | | | 2 | | |

Table 246: TU-3 Retimer - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--------------------------------------|
| 0x1e440 | 0 | FifoError | 0 | 0x0000 | Fifo Over- or Underflow has occurred |
| 0x1e442 | | | 1 | | |
| 0x1e444 | | | 2 | | |

Table 247: TU-3 Retimer - Defect Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|--------------------------------------|
| 0x1e480 0x1e482 0x1e484 | 0 | FifoError | 0 1 2 | 0x0000 | Fifo Over- or Underflow has occurred |

Table 248: TU-3 Retimer - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--------------------|
| 0x1e580 | 0 | Interrupt | 0x0000 | Summary of Defects |

Table 249: TU-3 Retimer - Sequencer Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|------|-----------------|----------------------|--------|--|
| 0x1e500 0x1e504 ... 0x1e510 | 0 | Const(1) | 0 1 ... 4 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e502 0x1e506 ... 0x1e512 | 15-0 | Const(0) | 0 1 ... 4 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e4c0 0x1e4c4 | 0 | Const(1) | 0 1 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e4c2 0x1e4c6 | 15-0 | Const(0) | 0 1 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e4c0 0x1e4c4 | 0 | Const(1) | 0 1 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e4c2 0x1e4c6 | 15-0 | Const(0) | 0 1 | 0x0000 | Constants which are used in Sequencer calculations |
| 0x1e600 0x1e602 ... 0x1e7fe | 15-0 | InstructionWord | 0 1 ... 255 | 0x0000 | Instruction Word for Sequencer Program RAM |

Table 250: TU-3 Retimer - Sequencer Data (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|--------------------------------------|------|--------------|----------------------|--------|---|
| 0x1e000 0x1e004 ... 0x1e3fc | 9-0 | DataWord_MSB | 0 1 ... 255 | 0x0000 | MSB of DataWord from Sequencer Data RAM |
| 0x1e002 0x1e006 ... 0x1e3fe | 15-0 | DataWord_LSB | 0 1 ... 255 | 0x0000 | LSB of DataWord from Sequencer Data RAM |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Tables 251 through 258 - Configuration, Status and Alarms of the AU-3/4 Retimer

Table 251: AU-3/4 Retimer - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------------|--------|---|
| 0x1d438 | 0 | Reserved | 0x0002 | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Configure on which transitions Latching For Interrupt occurs. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| 0x1d43a | 11-0 | FrameOffset | 0x0000 | Configure offset of Frame Start to FrameRefPulse. Set to 0x97A. |

Table 252: AU-3/4 Retimer - Per Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|--------|--|-------------|--------|--|
| 0x1d440 0x1d448 0x1d450 | 0 | AUG1_Format | 0 1 2 | 0x0001 | Timeslot belongs to either AU-3 (0) or AU-4 (1) |
| 0x1d442 0x1d44a 0x1d452 | 0 1 | InsertAIS_On_FifoError_Disable InsertAIS_On_SSF_Disable | 0 1 2 | 0x0000 | Disable AIS Insertion when FIFO error is detected Disable AIS Insertion when incoming SSF is detected |
| 0x1d444 0x1d44c 0x1d454 | 0 | SW_InsertAIS | 0 1 2 | 0x0000 | Force AIS Insertion through software |
| 0x1d446 0x1d44e 0x1d456 | 0 | JustCountReset | 0 1 2 | 0x0000 | Reset Pos/NegJustCount for this channel |

Table 253: AU-3/4 Retimer - Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|--------------------------------------|
| 0x1d400 0x1d402 0x1d404 | 0 | FifoError | 0 1 2 | 0x0000 | Fifo Over- or Underflow has occurred |

Table 254: AU-3/4 Retimer - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|--------------------------------------|
| 0x1d410 0x1d412 0x1d414 | 0 | FifoError | 0 1 2 | 0x0000 | Fifo Over- or Underflow has occurred |

Table 255: AU-3/4 Retimer - Defect Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------|-------------|--------|--------------------------------------|
| 0x1d420 0x1d422 0x1d424 | 0 | FifoError | 0 1 2 | 0x0000 | Fifo Over- or Underflow has occurred |

Table 256: AU-3/4 Retimer - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--------------------------------------|
| 0x1d430 | 0 | Interrupt | 0x0000 | Latched For Interrupt Defect Summary |

Table 257: AU-3/4 Retimer - Ptr Leak Reset Value (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|------|--------------------|-------------|--------|---|
| 0x1d460 0x1d464 0x1d468 | 15-0 | SlowLeakResetValue | 0 1 2 | 0x0000 | Reset Value of Counter determining outgoing Pointer Movement spacing while the FifoDepth is in the Slow Leak Zone. A unit corresponds to two frames |
| 0x1d462 0x1d466 0x1d46a | 15-0 | FastLeakResetValue | 0 1 2 | 0x0000 | Reset Value of Counter determining outgoing Pointer Movement spacing while the FifoDepth is in the Fast Leak Zone. A unit corresponds to two frames |

Table 258: AU-3/4 Retimer - Performance Counters (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|------|--------------|-------------|--------|---|
| 0x1d470 0x1d474 0x1d478 | 15-0 | PosJustCount | 0 1 2 | 0x0000 | Count of outgoing (generated) Positive Pointer Movements (Increments) |
| 0x1d472 0x1d476 0x1d47a | 15-0 | NegJustCount | 0 1 2 | 0x0000 | Count of outgoing (generated) Negative Pointer Movements (Decrements) |

Tables 259 through 261 - Configuration and Status of the General High Order Interrupt Controller

Table 259: HO Interrupt Controller - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|----------------------------|---|----------------|---|
| 0x1d2e4 | 0 | R4POH_Event_Interrupt | Not Applicable | Interrupt of the per channel events coming from the RX_VC4_POH Monitor. Default value: TRUE |
| | 1 | R4POH_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_VC4_POH Monitor. Default value: TRUE |
| | 2 | R3POH_Event_Interrupt | | Interrupt of the per channel events coming from the RX_VC3_POH Monitor. Default value: TRUE |
| | 3 | R3POH_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_VC3_POH Monitor. Default value: TRUE |
| | 4 | RTU3_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_TU3_PTR. Default value: TRUE |
| | 5 | L3RTM_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the L3RTM Default value: TRUE |
| | 6 | TXAP_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX alarm indication port Default value: TRUE |
| | 7 | TXAP_Event_Interrupt | | Interrupt of the per channel events coming from the TX alarm indication port Default value: TRUE |
| | 8 | TTU3_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX_TU3_PTR Default value: TRUE |
| 9 | AURTM_CorrDefect_Interrupt | Interrupt of the per channel defects coming from the AU Retimer Default value: TRUE | | |



Table 260: HO Interrupt Controller - Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------------|--------|---|
| 0x1d2e6 | 0 | R4POH_Event_Interrupt | 0x03FF | Interrupt of the per channel events coming from the RX_VC4_POH Monitor. Default value: TRUE |
| | 1 | R4POH_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_VC4_POH Monitor. Default value: TRUE |
| | 2 | R3POH_Event_Interrupt | | Interrupt of the per channel events coming from the RX_VC3_POH Monitor. Default value: TRUE |
| | 3 | R3POH_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_VC3_POH Monitor. Default value: TRUE |
| | 4 | RTU3_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX_TU3_PTR. Default value: TRUE |
| | 5 | L3RTM_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the L3RTM Default value: TRUE |
| | 6 | TXAP_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX alarm indication port Default value: TRUE |
| | 7 | TXAP_Event_Interrupt | | Interrupt of the per channel events coming from the TX alarm indication port Default value: TRUE |
| | 8 | TTU3_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX_TU3_PTR Default value: TRUE |
| | 9 | AURTM_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the AU Retimer Default value: TRUE |

Table 261: HO Interrupt Controller - Interrupt Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x1d2e0 | 0 | Interrupt | 0x0000 | Interrupt summary for the whole C3_TO_AUG1 block |

Tables 262 through 280 - Configuration, Status and Alarms of the Rx Combust Interface

Table 262: Rx Combust Interface - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|------------------|----------------|---|
| 0x1d578 | 0 | Reserved | Not Applicable | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Configure on which transitions Latching For Interrupt occurs. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 4-3 | PMFMEventControl | | Configure on which transitions Latching For PM/FM occurs 00: PM/FM disabled 01: Rising edge 10: Falling edge 11: Both edges |
| | 5 | ActiveEdge | | Select the edge on which data and timing from the Combust are sampled: falling (1) or rising (0) edge. The rising edge is default. |
| | 9-6 | TimingDelay | | Configure expected Delay between Timing and Data on Combust |
| 0x1d57a | 0 | ParityEven | 0x0000 | If TRUE, Parity is assumed to be even; else it is assumed to be odd |
| | 1 | ParityMode | | Parity is calculated either over Data only (0), or over Data and Timing (1) |

Table 263: Rx Combus Interface - Per Channel Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------------|-------------|--------|--|
| 0x1d510 0x1d514 0x1d518 | 0 | AU_Mode | 0 1 2 | 0x0000 | Select AU-4 (1) or AU-3 (0) format |
| 0x1d512 0x1d516 0x1d51a | 0 | V1_PulsePresent | 0 1 2 | 0x0001 | Indicates if V1-pulse is present on the Combus |

Table 264: Rx Combus Interface - Per Channel Status (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|------|-----------|--------|--------|-----------------------------------|
| 0x1d520 0x1d522 0x1d524 | 7-0 | H1_Byte | 0 | 0x0000 | Received AU-level H1 Pointer Byte |
| | 15-8 | H2_Byte | 1 2 | | Received AU-level H2 Pointer Byte |

Table 265: Rx Combus Interface - Defects (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d57c | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM. Recovery can take from 6 to 15 frames after any offending alarms clear. |
| | 1 | ParityError | | Parity Error detected |

Table 266: Rx Combus Interface - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d57e | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM. Recovery can take from 6 to 15 frames after any offending alarms clear. |
| | 1 | ParityError | | Parity Error detected |

Table 267: Rx Combus Interface - Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d500 | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM. Recovery can take from 6 to 15 frames after any offending alarms clear. |
| | 1 | ParityError | | Parity Error detected |

Table 268: Rx Combus Interface - Defects PM (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d504 | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM. Recovery can take from 6 to 15 frames after any offending alarms clear. |
| | 1 | ParityError | | Parity Error detected |

Table 269: Rx Combus Interface - Defects FM (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|--|
| 0x1d508 | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM. Recovery can take from 6 to 15 frames after any offending alarms clear. |
| | 1 | ParityError | | Parity Error detected |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 270: Rx Combus Interface - Defect Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|---------------------------------|
| 0x1d50c | 0 | C1_LossOfFrame | 0x0000 | Loss of Frame in C1 Locking FSM |
| | 1 | ParityError | | Parity Error detected |

Table 271: Rx Combus Interface - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---------------------------------------|
| 0x1d528 | 0 | Interrupt | 0x0000 | Latched For Interrupt Defect Summary |
| 0x1d52a | 0 | PM | 0x0000 | Performance Monitoring Defect Summary |
| 0x1d52c | 0 | FM | 0x0000 | Fault Monitoring Defect Summary |

Table 272: Rx Combus Interface - Per Channel Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------|-----|----------------|-------|--------|---------------------------------|---|
| 0x1d530 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM | |
| 0x1d532 | 1 | V1_LossOfFrame | | | 1 | Loss of Frame in V1 Locking FSM |
| 0x1d534 | 2 | AIS_Detected | | | 2 | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 273: Rx Combus Interface - Per Channel Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------|-----|----------------|-------|--------|---------------------------------|---|
| 0x1d538 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM | |
| 0x1d53a | 1 | V1_LossOfFrame | | | 1 | Loss of Frame in V1 Locking FSM |
| 0x1d53c | 2 | AIS_Detected | | | 2 | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 274: Rx Combus Interface - Per Channel Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------|-----|----------------|-------|--------|---------------------------------|---|
| 0x1d540 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM | |
| 0x1d542 | 1 | V1_LossOfFrame | | | 1 | Loss of Frame in V1 Locking FSM |
| 0x1d544 | 2 | AIS_Detected | | | 2 | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 275: Rx Combus Interface - Per Channel Defects PM (RO)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------|-----|----------------|-------|--------|---------------------------------|---|
| 0x1d548 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM | |
| 0x1d54a | 1 | V1_LossOfFrame | | | 1 | Loss of Frame in V1 Locking FSM |
| 0x1d54c | 2 | AIS_Detected | | | 2 | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 276: Rx Combus Interface - Per Channel Defects FM (RO)

| Address | Bit | HW Symbol | Index | Init | Description | |
|---------|-----|----------------|-------|--------|---------------------------------|---|
| 0x1d550 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM | |
| 0x1d552 | 1 | V1_LossOfFrame | | | 1 | Loss of Frame in V1 Locking FSM |
| 0x1d554 | 2 | AIS_Detected | | | 2 | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 277: Rx Combus Interface - Per Channel Defect Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x1d558 | 0 | J1_LossOfFrame | 0 | 0x0000 | Loss of Frame in J1 Locking FSM |
| 0x1d55a | 1 | V1_LossOfFrame | 1 | | Loss of Frame in V1 Locking FSM |
| 0x1d55c | 2 | AIS_Detected | 2 | | AIS Detected through monitoring of AU H1/H2 Pointer Bytes |

Table 278: Rx Combus Interface - Per Channel Defect Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x1d560 | 2-0 | LatchForInt | 0x0000 | Per Channel Latched For Interrupt Defect Summary |
| 0x1d562 | 2-0 | PM | 0x0000 | Per Channel Performance Monitoring Defect Summary |
| 0x1d564 | 2-0 | FM | 0x0000 | Per Channel Fault Monitoring Defect Summary |

Table 279: Rx Combus Interface - Per Channel Defect Summary Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x1d568 | 2-0 | LatchForInt | 0x0000 | Per Channel Latched For Interrupt Defect Summary |
| 0x1d56a | 2-0 | PM | 0x0000 | Per Channel Performance Monitoring Defect Summary |
| 0x1d56c | 2-0 | FM | 0x0000 | Per Channel Fault Monitoring Defect Summary |

Table 280: Rx Combus Interface - Per Channel Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---------------------------------------|
| 0x1d570 | 0 | Interrupt | 0x0000 | Latched For Interrupt Defect Summary |
| 0x1d572 | 0 | PM | 0x0000 | Performance Monitoring Defect Summary |
| 0x1d574 | 0 | FM | 0x0000 | Fault Monitoring Defect Summary |



DATA SHEET

EtherMap-3 Plus
TXC-04236

Tables 281 through 302 - Configuration, Status and Alarms of the Tx Combust Interface

Table 281: Tx Combust Interface - General Configuration (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|--------------|---|--------|--|
| 0x184c8 | 0 | Reserved | 0x48A2 | Reserved: this field must be FALSE (0) for correct operation. |
| | 2-1 | IntEventControl | | Interrupt latch condition. Default value: INT_RISING_EDGE. Possible values: INT_LEVEL (00), INT_RISING_EDGE (01), INT_FALLING_EDGE (10), INT_BOTH_EDGES (11) |
| | 4-3 | PMFMEventControl | | PM/FM Latch condition. Default value: PM_DISABLED (00). Possible values: PM_DISABLED (00), PM_RISING_EDGE (01), PM_FALLING_EDGE (10), PM_BOTH_EDGES (11) |
| | 5 | ActiveEdge | | Select active edge of the timing on the Combust: This control is used in: a) Add bus timing slave. The inputs AC1J1V1 and ASPE are sampled on the falling edge of ACLK (bit set to '1') or rising edge (bit set to '0'). b) Drop bus timing. The inputs DC1J1V1 and DSPE are sampled on the falling edge of DCLK (bit set to '1') or rising edge (bit set to '0'). The falling edge is default active. |
| | 6 | LoopBackActive | | Controls SONET/SDH Line Side loopback from Drop to Add Telecom bus. Default value: disabled (0). |
| | 10-7 | TimingDelay | | Timing Delay: Delay between timing and data on the Combust. Default value: 1. Possible values: 0 .. 15 |
| | 11 | AddInd_ActLow | | This bit must always be written with a 1. |
| | 12 | ParityMode | | Parity mode of the calculated parity. The parity can be calculated over the data only (0) or in timing source mode over the data and the SPE and C1J1V1 timing signals (1). Default value is data only. |
| | 13 | ParityEven | | Indication whether the calculated parity is even. Default value: FALSE |
| 14 | C1_LOF_HighZ | Setting to enable tristating the bus during C1_LOF. Default value: TRUE | | |

Table 282: Tx Combust Interface - AUG1 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|---|
| 0x184cc | 0 | AU_Mode | 0 | 0x0000 | Selects the AU Mode of this AUG1 on the Combust: AU-3 (0) or AU-4 (1). Default value is AU-3. |

Table 283: Tx Combust Interface - AU-3 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|-------------------------------|-----|-----------------|-------------|--------|---|
| 0x184e8 0x184ea 0x184ec | 0 | J1_LOF_HighZ | 0 1 2 | 0x003F | Enable tristating the bus during J1_LOF. For AU-4, this must be set for every AU-3. Default value: TRUE |
| | 1 | V1_LOF_HighZ | | | Enable tristating the bus during V1_LOF. For AU-4, this must be set for every AU-3. Default value: TRUE |
| | 2 | FifoError_HighZ | | | Enable Tristating the bus during FifoError. For AU-4, this must be set for every AU-3. Default value: TRUE |
| | 3 | HighZ_AU3 | | | Tristate forcing of the AU-3. For AU-4, this must be set for every AU-3. Default value: TRUE (See "Telecom Bus Tributary Activation/Tri-State Control" on page 191) |
| | 4 | HighZ_TUG3 | | | Tristate forcing of the TUG-3. Default value: TRUE (See "Telecom Bus Tributary Activation/Tri-State Control" on page 191) |
| | 5 | V1_PulsePresent | | | Indicates if the V1 Pulse is present on the Combust |

Table 284: Tx Combust Interface - TUG-2 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|---|
| 0x18480 | 0 | IsTU12 | 0 | 0x0002 | Indication if the TUG-2 contains TU-11 containers. Default value: FALSE. When TRUE, the TUG-2 contains TU-12 containers |
| 0x18482 | | | 1 | | |
| ... | 1 | HighZ | ... | | Tristate setting of the TUG-2. Default value: TRUE (See "Telecom Bus Tributary Activation/Tri-State Control" on page 191) |
| 0x184a8 | | | 20 | | |

Table 285: Tx Combust Interface - TU-11/TU-12 Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------|-------|--------|--|
| 0x18500 | 0 | HighZ | 0 | 0x0001 | Tristate setting for the TU-11/TU-12. Default value: TRUE (See "Telecom Bus Tributary Activation/Tri-State Control" on page 191) |
| 0x18502 | | | 1 | | |
| ... | | | ... | | |
| 0x185a6 | | | 83 | | |

Table 286: Tx Combust Interface - Defects (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|----------------|---|
| 0x184d0 | 0 | C1_LossOfFrame | Not Applicable | C1_LossOfFrame alarm for the C1 locking FSM |

Table 287: Tx Combust Interface - Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|----------------|---|
| 0x184d4 | 0 | C1_LossOfFrame | Not Applicable | C1_LossOfFrame alarm for the C1 locking FSM. Recovery can occur 6 to 15 frames after any offending alarms are cleared up. |

Table 288: Tx Combust Interface - Defect Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|----------------|---|
| 0x184d8 | 0 | C1_LossOfFrame | Not Applicable | C1_LossOfFrame alarm for the C1 locking FSM |

Table 289: Tx Combust Interface - Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|--------|---|
| 0x184dc | 0 | C1_LossOfFrame | 0x0000 | C1_LossOfFrame alarm for the C1 locking FSM. Recovery can occur 6 to 15 frames after any offending alarms are cleared up. |

Table 290: Tx Combust Interface - Defects PM (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|----------|---|
| 0x184e0 | 0 | C1_LossOfFrame | see Note | C1_LossOfFrame alarm for the C1 locking FSM. Recovery can occur 6 to 15 frames after any offending alarms are cleared up. |

Note: If ONESEC is not present then the initial value is 0x0000. If ONESEC is present, then the initial value is 0x0001.

Table 291: Tx Combust Interface - Defects FM (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------|----------|---|
| 0x184e4 | 0 | C1_LossOfFrame | see Note | C1_LossOfFrame alarm for the C1 locking FSM. Recovery can occur 6 to 15 frames after any offending alarms are cleared up. |

Note: If ONESEC is not present then the initial value is 0x0000. If ONESEC is present, then the initial value is 0x0001.



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 292: Tx Combust Interface - Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x184f0 | 0 | Interrupt | 0x0000 | Latch for interrupt summary for the global defects. |
| 0x184f2 | 0 | PM | 0x0000 | PM summary for the global defects |
| 0x184f4 | 0 | FM | 0x0000 | FM summary for the global defects |

Table 293: Tx Combust Interface - Per Channel Defects (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x184f8 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x184fa | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x184fc | 2 | FifoError | 2 | | FifoError |

Table 294: Tx Combust Interface - Per Channel Defects Latched For Interrupt (R/COW-1)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x18400 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x18402 | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x18404 | 2 | FifoError | 2 | | FifoError |

Table 295: Tx Combust Interface - Per Channel Defect Masks (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x18410 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x18412 | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x18414 | 2 | FifoError | 2 | | FifoError |

Table 296: Tx Combust Interface - Per Channel Defects Latched For PMFM (R/COW-0)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x18420 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x18422 | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x18424 | 2 | FifoError | 2 | | FifoError |

Table 297: Tx Combust Interface - Per Channel Defects PM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x18430 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x18432 | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x18434 | 2 | FifoError | 2 | | FifoError |

Table 298: Tx Combust Interface - Per Channel Defects FM (RO)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|----------------|-------|--------|---|
| 0x18440 | 0 | J1_LossOfFrame | 0 | 0x0000 | J1 Loss Of Frame for the J1 locking FSM |
| 0x18442 | 1 | V1_LossOfFrame | 1 | | V1 Loss Of Frame for the V1 locking FSM |
| 0x18444 | 2 | FifoError | 2 | | FifoError |

Table 299: Tx Combust Interface - Per Channel Defect Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-------------|--------|---|
| 0x18450 | 2-0 | LatchForInt | 0x0000 | Per channel latch for interrupt summary |
| 0x18452 | 2-0 | PM | 0x0000 | Per channel PM summary |
| 0x18454 | 2-0 | FM | 0x0000 | Per channel FM summary |

Table 300: Tx Combust Interface - Per Channel Defect Summary Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x184c0 | 2-0 | Mask | 0x0007 | Mask setting for every per channel latched Bit for interrupt of the per channel summary. Default: TRUE (1) |

Table 301: Tx Combust Interface - Per Channel Defect Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x18460 | 0 | Interrupt | 0x0000 | Latch for interrupt summary for the per channel defects |
| 0x18462 | 0 | PM | 0x0000 | PM summary for the per channel defects |
| 0x18464 | 0 | FM | 0x0000 | FM summary for the per channel defects |

Table 302: Tx Combust Interface - Defect Configuration (RW)

| Address | Bit | HW Symbol | Index | Init | Description |
|---------|-----|-----------------------------|-------|--------|---|
| 0x18470 | 0 | J1LOF_C1LOF_Inhibit_Disable | 0 | 0x0000 | Disables the inhibition of J1_LossOfFrame by C1_LossOfFrame. Default value: FALSE |
| 0x18472 | | | 1 | | |
| 0x18474 | | | 2 | | |
| | 1 | V1LOF_C1LOF_Inhibit_Disable | | | Disables the inhibition of V1_LossOfFrame by C1_LossOfFrame. Default value: FALSE |
| | 2 | V1LOF_J1LOF_Inhibit_Disable | | | Disables the inhibition of V1_LossOfFrame by J1_LossOfFrame. Default value: FALSE |

Tables 303 through 305 - Configuration and Status of the General Combust Interface Interrupt Controller

Table 303: Combust Interrupt Controller - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------------------|----------------|--|
| 0x1d784 | 0 | RXCB_Global_CorrDefect_Interrupt | Not Applicable | Interrupt of the global defects coming from the RX Combust. Default value: TRUE |
| | 1 | RXCB_PerChannel_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX Combust. Default value: TRUE |
| | 2 | TXCB_Global_CorrDefect_Interrupt | | Interrupt of the global defects coming from the TX Combust. Default value: TRUE |
| | 3 | TXCB_PerChannel_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX Combust. Default value: TRUE |



DATA SHEET

**EtherMap-3 Plus
TXC-04236**

Table 304: Combus Interrupt Controller - Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|--------------------------------------|--------|---|
| 0x1d786 | 0 | RXCB_Global_CorrDefect_Interrupt | 0x000F | Interrupt of the global defects coming from the RX Combus. Default value: TRUE |
| | 1 | RXCB_PerChannel_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the RX Combus. Default value: TRUE |
| | 2 | TXCB_Global_CorrDefect_Interrupt | | Interrupt of the global defects coming from the TX Combus. Default value: TRUE |
| | 3 | TXCB_PerChannel_CorrDefect_Interrupt | | Interrupt of the per channel defects coming from the TX Combus. Default value: TRUE |

Table 305: Combus Interrupt Controller - Interrupt Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|--|
| 0x1d780 | 0 | Interrupt | 0x0000 | Interrupt summary for the whole Combus block |

Tables 306 through 308 - Configuration and Status of the General VTMAPPER Interrupt Controller

Table 306: Mapper Interrupt Controller - Interrupts (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|----------------|--|
| 0x1d7a4 | 0 | COMBUS_Interrupt | Not Applicable | Interrupt coming from the Combus core. |
| | 1 | C3_TO_AUG1_Interrupt | | Interrupt coming from the C3_TO_AUG1 core. |
| | 2 | VTMP_Interrupt | | Interrupt coming from the VTMAPPER core. |

Table 307: Mapper Interrupt Controller - Interrupt Masks (RW)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|----------------------|--------|---|
| 0x1d7a6 | 0 | COMBUS_Interrupt | 0x0007 | Mask for the interrupt coming from the Combus core. Default value: TRUE |
| | 1 | C3_TO_AUG1_Interrupt | | Mask for the interrupt coming from the C3_TO_AUG1 core. Default value: TRUE |
| | 2 | VTMP_Interrupt | | Mask for the interrupt coming from the VTMAPPER core. Default value: TRUE |

Table 308: Mapper Interrupt Controller - Interrupt Group Summary (RO)

| Address | Bit | HW Symbol | Init | Description |
|---------|-----|-----------|--------|---|
| 0x1d7a0 | 0 | Interrupt | 0x0000 | Interrupt summary for the whole VTMAPPER_TOP core |

Table 309: Reserved Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------|--------|-------------|
| 0x00006 | 15-0 | Reserved | 0x0000 | |
| 0x00012 | 15-0 | Reserved | 0x0000 | |
| 0x00014 | 15-0 | Reserved | 0x20D7 | |
| 0x00016 | 15-0 | Reserved | 0x0108 | |
| 0x00018 | 15-0 | Reserved | 0x0000 | |
| 0x0001a | 15-0 | Reserved | 0x0000 | |
| 0x0001e | 15-0 | Reserved | 0x0000 | |
| 0x00026 | 15-0 | Reserved | 0x0000 | |

Table 309: Reserved Registers

| Address | Bit | HW Symbol | Init | Description |
|---------|------|-----------|--------|------------------------------|
| 0x0002a | 15-0 | Reserved | 0x0000 | |
| 0x0002e | 15-0 | Reserved | 0x0000 | |
| 0x00032 | 15-0 | Reserved | 0x0000 | |
| 0x00036 | 15-0 | Reserved | 0x0000 | |
| 0x00038 | 15-0 | Reserved | 0x0000 | Must be set to 0x0000 |
| 0x0003a | 15-0 | Reserved | 0x0100 | Must be set to 0x0100 |
| 0x0003e | 15-0 | Reserved | 0x0000 | |
| 0x00044 | 15-0 | Reserved | 0x0000 | |
| 0x11988 | 15-0 | Reserved | 0x0000 | |
| 0x11d88 | 15-0 | Reserved | 0x0000 | |
| 0x12188 | 15-0 | Reserved | 0x0000 | |
| 0x12588 | 15-0 | Reserved | 0x0000 | |
| 0x12988 | 15-0 | Reserved | 0x0000 | |
| 0x12d88 | 15-0 | Reserved | 0x0000 | |
| 0x13188 | 15-0 | Reserved | 0x0000 | |
| 0x19670 | 15-0 | Reserved | 0x0000 | |
| 0x19684 | 15-0 | Reserved | 0x003C | |
| 0x19846 | 15-0 | Reserved | 0x003C | |
| 0x198f0 | 15-0 | Reserved | 0x0000 | |
| 0x1d050 | 15-0 | Reserved | 0x0000 | Must be set to 0x0006 |
| 0x1d240 | 15-0 | Reserved | 0x0088 | |
| 0x1d242 | 15-0 | Reserved | 0x0064 | |
| 0x1d244 | 15-0 | Reserved | 0x017A | |
| 0x1d246 | 15-0 | Reserved | 0x0011 | |
| 0x1d248 | 15-0 | Reserved | 0x000C | |
| 0x1d280 | 15-0 | Reserved | 0x0000 | |
| 0x1d282 | 15-0 | Reserved | 0x0000 | |
| 0x1d284 | 15-0 | Reserved | 0x0000 | |
| 0x1d286 | 15-0 | Reserved | 0x0000 | |
| 0x1d690 | 15-0 | Reserved | 0x0000 | |
| 0x1d692 | 15-0 | Reserved | 0x0000 | |
| 0x1eac8 | 15-0 | Reserved | 0x0000 | |
| 0x1ebce | 15-0 | Reserved | 0x0000 | |
| 0x1f0c0 | 15-0 | Reserved | 0x0000 | |
| 0x1f0c2 | 15-0 | Reserved | 0x0000 | |
| 0x1f0c4 | 15-0 | Reserved | 0x0000 | |
| 0x1f0c6 | 15-0 | Reserved | 0x0000 | |
| 0x1f0c8 | 15-0 | Reserved | 0x0000 | |
| 0x1f0ca | 15-0 | Reserved | 0x0000 | |
| 0x1f0cc | 15-0 | Reserved | 0x0000 | |
| 0x1f0ce | 15-0 | Reserved | 0x0000 | |
| 0x1f0d0 | 15-0 | Reserved | 0x0000 | |
| 0x1f940 | 15-0 | Reserved | 0x0000 | |

ALARMS, PERFORMANCE AND FAULT MONITORING

This section details out the Alarm/Status and Performance Monitoring features for the EtherMap-3 *Plus* device. The general features are described herein, with specific listing of all Alarms, Performance Counters appearing in the relevant sections.

TERMINOLOGY

System Alarm (Raw, Unlatched Alarm)

A signal that traces in real time, the evolution of a system property (a system fault, statistic, or any other characteristic that needs monitoring) when appropriately enabled. This signal, then can be monitored for purposes of corrective action or for the purposes of status reporting.

Note that the terms System Alarm, Raw Alarm or Unlatched Alarm may be used interchangeably.

Alarm Event

A transition in the state of a System Alarm.

Note that there can be two types of transitions in a System Alarm - a rising edge, or a falling edge corresponding to 'Alarm Entry' or 'Alarm Exit' respectively.

Latched Alarm

A Latched Alarm for a given Unlatched Alarm, is the associated latched memory for the occurrence of an alarm event (of a single type, or either type) in the unlatched alarm signal. This permits processing of the system alarm without real-time constraints. The active transition or level, which leads to setting of the Latched Alarm, in general may be software configurable.

Secondary Alarm Inhibition

The process of filtering to provide data reduction and unnecessary generation of interrupts, when an alarm event that is at a higher hierarchy leads to the generation of multiple lower order alarms (in other words, lower order alarm events are triggered as a secondary effect). This filtering mechanism (termed herein as 'Secondary Alarm Inhibition) prevents redundant data processing and also the unnecessary interrupt burden that may affect adversely the functioning of the system.

The Alarm Inhibition function may be built at the Unlatched Alarm level, or, if GR-253 style reporting requirements need to be supported, then the Alarm Inhibition may be built at the Latched Alarm level.

Interrupt Mask

If interrupt generation is a function of a given Latched Alarm, there will be a corresponding dedicated Interrupt Mask bit, that may be set up to disable the particular interrupt. These bits will be software readable and writable.

Performance and Fault Monitoring (PM and FM)

An Unlatched Alarm may have associated with it a corresponding PM/FM feature, that allows a System to monitor the long term evolution of the particular alarm, in a convenient manner.

As an example, a System may wish to monitor if a defect occurred over only a single unit time interval, or, if the defect persisted over several unit time intervals with respect to a certain particular alarm, or a group of alarms. The unit time interval may be 1-second, or any other, as laid down by applicable standards (if any), or as required to implement a specified Performance and Fault Monitoring System.

Performance Monitoring (PM)

The 1-second PM output bit associated with an unlatched alarm indicates the occurrence of an alarm event over the immediately preceding 1-second interval.

Fault Monitoring (FM)

The 1-second FM output bit associated with an unlatched alarm indicates that the unlatched alarm was continuously asserted, without any alarm events taking place, over the duration of at least the immediately preceding 1-second interval.

1-Second Clock

The 1-second clock defines 1-second time intervals to serve as a time reference for the PM/FM scheme (see ONESEC [page 43](#)). This clock typically, may be provided from external sources to TranSwitch devices, and is also used to synchronize the external polling mechanism that would query the PM/FM registers on the TranSwitch device.

Performance Counters

Certain alarm events or parameters are counted for System Performance Monitoring. The counter width (in bits) depends on the event being counted, and time-intervals (that is, estimated maximum counts) between reads. The Performance Counters may adopt one of two schemes:

A. Counters that either roll-over or saturate. Here 'roll-over' means that after the terminal count is reached, the counter wraps around, and continues to count from zero; 'saturate' means that after terminal count is reached, the counter stops incrementing, and freezes at the terminal count.

B. Counters that clear on 1-second boundaries, with existing counts over the 1-second interval transferred to 1-second counter shadow registers (also on the 1-second boundaries). The main event counters are cleared by the microprocessor writing 0's to the counter, or at 1-second boundaries.

UNLATCHED ALARMS

All Unlatched alarms are memory mapped and available to be read out from Read-Only type registers for the actual status.

The Unlatched alarm signal is high only when asserted.

Unlatched Alarms can be both frame based, like SONET/SDH Performance Alarms, or, independent of framing, such as Loss of Signal alarms, or Buffer overflow/underflow alarms etc.

Inhibition of Secondary Unlatched Alarm Generation

The generation of Secondary Unlatched Alarm may be inhibited dynamically, depending on system alarm hierarchy to prevent unnecessary automatic reporting of secondary alarms which arise as a consequence of some primary root cause alarm (the particular inhibiting conditions for a given device). This process is known as 'Defect Correlation' in [G806]. Defect correlation will also inhibit the generation of unnecessary interrupts at a lower layer. Refer figures 6.1 and 6.2 in [G806], that illustrate the process of Alarm Supervision and Defect Correlation at each atomic function. Each atomic function generates AIS as appropriate, based on locally detected defects only. Upstream AIS or upstream TSF/SSF signals are inputs to the atomic function. The defect correlation process in [G806] terminology is described as

$$c(\text{defect}) \leftarrow d(\text{defect}) \text{ AND } (\text{not}(\text{inhibition_condition}) \text{ AND } (\text{inhibition_enabled}))$$

There are two components for the inhibition function:

- 1) Active high Alarm Inhibition condition based on upstream or primary or root cause alarms; (Active_Hi_Alarm_Inhibition_cond). This includes possibly an upstream TSF/SSF.
- 2) Static, software configurable bit INHIB_alarm_name_EN, that enables such a correlation. Note that provision for the INHIB_alarm_name_EN control bit is optional. On power up, or on a HW reset, this control bit is set up with a zero. The presence of this control gives the system the flexibility to implement defect correlation.

The correlated defect (Unlatched Alarm generated after being operated on by the inhibition function) gives rise to two possible sets of latched alarm event bits, discussed below.

LATCHED ALARMS

Every Unlatched alarm bit (Alarm_name) has a corresponding Latched Alarm bit for interrupt generation (called LAlarm_name, if there is no associated PM/FM).

If there is Performance and Fault Monitoring associated with an unlatched alarm, then there are two separate Latched Alarm bits: (1) One for generating hardware/software interrupts (called L1Alarm_name); and (2) another to be used for PM/FM circuits (called L2Alarm_name) for PM and FM functionality. It should be noted that it is not necessary for PM/FM to be associated with every unlatched alarm, while a latched alarm must exist for every unlatched alarm.

The purpose of the Latched Alarm(s) is two-fold:

1. To generate a Hardware or Software interrupt to flag the occurrence of an alarm event to the external Host Processor.
2. To derive the Performance and Fault Monitoring (PM/FM) conditions.

The L1Alarm_name bits are latched read-only (R(L)), cleared on a microprocessor read (or on a system reset).

The L2Alarm_name bits, for PM/FM, are Read/Write, cleared either by the microprocessor writing a zero to this bit, or on 1-second clock boundaries (or on system reset).

The general scheme for latched alarm processing is shown below.

LATCHED ALARM BITS FOR INTERRUPT GENERATION (LALARM_NAME/L1ALARM_NAME)

The EtherMap-3 Plus is capable of latching according to the states given in the following table. INRT(1-0) (actual Symbol names are cINRT_GRP125M (Table 48, on page 236), cINRT_GRP100M (Table 98, on page 298), cINRT_GRPTX20M (Table 65, on page 270), cINRT_GRPRX20M (Table 76, on page 283) and cINRT_SOTERN_CORE (Table 30, on page 217)) are global configuration bits for the group of latched alarm bits for interrupt generation (labelled as LAlarm_name in systems without PM/FM, for example LLOS; and labelled as L1Alarm_name in systems with PM/FM, for example L1LOS). The case for level triggering is included for completeness; most TranSwitch devices are doing away with that option.

At minimum, all TranSwitch devices are configurable for the positive edge only and positive/negative edge events. The negative edge only and the level triggering events are additional optional features of particular devices. For devices that do not incorporate these options, the INRT(1-0) = (0,0) or (1,0) settings are invalid.

Table 310: Latched Alarm Bit (L1Alarm_name) Transition Selection

| INRT1 | INRT0 | Action |
|-------|-------|---|
| 0 | 0 | All Latched Alarm bits (event bits) latch on the positive level (i.e., true state) of the Unlatched Alarm. When a Latched Alarm bit position is cleared, it re-latches if the Unlatched Alarm is still active (true). (This mode is no longer favored in TranSwitch devices; the only purpose of its inclusion is when PM/FM is not provided, this may be one option of monitoring a persistent fault). |
| 0 | 1 | All Latched Alarm bits (event bits) latch on the positive transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm goes inactive and then active again. This is expected to be the most frequently used mode for the Latched Alarm bits. |
| 1 | 0 | All Latched Alarm bits (event bits) latch on the negative transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm goes active and then inactive again. The purpose of these bits is added flexibility, in configuring all events for alarm exit conditions. |
| 1 | 1 | All Latched Alarm bits (event bits) latch on either the positive or negative transition of an Unlatched Alarm. When a Latched Alarm bit position is cleared, it remains reset unless the alarm transitions again. |

Software access to this set of latched alarm bits is as follows:

Normal operation: Latched Read Only, and clears on a microprocessor read, or on global resets.

All L /L1Alarm_name values are readable by Software, before application of masking.

The following diagram of Figure 59 illustrates the above described options.

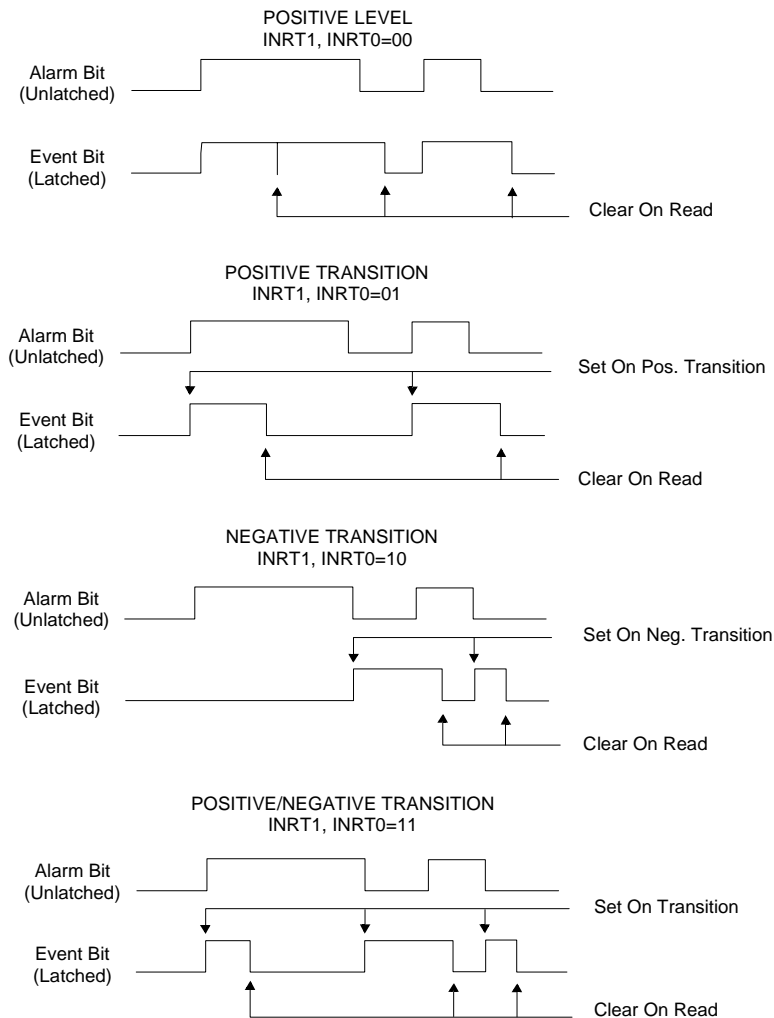


Figure 59. Latched Alarm Bit (L1Alarm_name) Transitions

LATCHED ALARM MASKING BITS (MALARM_NAME)

Each latched alarm L/L1Alarm_name has its own static masking bit that is software configurable, and is named MAlarm_name. The latched alarm combined with the state of the mask bit may generate an interrupt. These individual interrupts are grouped at various levels of hierarchy (with masking provided at each level) and finally be consolidated at a top level software polling register. Depending on individual device requirements, there could also be a single global interrupt mask bit.

The hardware interrupt capability is enabled by writing a 1 into the HINTEN control bit. When disabled, the hardware interrupt indication INT/IRQ lead is tri-stated (for a device/chip-level output) or, at the IP core level, the o_INT/IRQ signal is in the inactive state, even when a latched indication (event) bit is set. A software polling bit and the hardware interrupt state (when enabled by writing a 1 to HINTEN) indication occurs when one or

more bit locations in the interrupt mask bit locations are written with a '0', and the corresponding latched alarm occurs. Note that the polarity of the INT/ $\overline{\text{IRQ}}$ output signal for the Intel/Motorola processor interface is selectable by selecting the appropriate microprocessor interface (not in the scope of the present specification). Please note that setting of a mask bit to 0 enables the actions by an alarm.

The Hardware interrupt state is exited when any one (or more) of the following occurs:

HINTEN control bit is written with a 0

Alarm Mask bit is written with a 1

Latched alarm bit position is cleared

The Software Polling indication is zero when any one (or more) of the following occurs:

Alarm Mask bit is written with a 1

Latched alarm bit position is cleared

Please note that a latched alarm will re-latch if the alarm is active for a positive level transition.

SECONDARY LATCHED ALARM INHIBITION

The process of 'Defect Correlation' in [G806] (refer Section 3.2.1 for references to Defect Correlation), maybe done at the Latched Alarm level. This process is optional to the process described in Section 3.2.1. Note the difference: the process in Section 3.2.1 suppresses generation of the Unlatched alarms, whereas, this process allows the Unlatched alarm to be generated.

The Latched Alarm is inhibited dynamically, depending on system alarm hierarchy to prevent unnecessary automatic latching of secondary alarms which arise as a consequence of some primary root cause alarm.

The above inhibits the generation of unnecessary interrupts, while at the same time, allow the monitoring of the secondary alarms for optional report generation, as certain standards require, since the Unlatched alarms are readable, and their generation is not suppressed (As an example of such a standard, the BellCore/TelCordia GR-253, Sept. 2000: Section 6.2.1.8.4, R6-293 and R6-294, may be cited).

There are three components for the function:

1) Active high Alarm Inhibition condition based on upstream or primary or root cause alarms; (Active_Hi_Alarm_Inhibition_cond).

2) Static, software configurable bit INHIB_alarm_name_EN, that enables such an inhibit (Note that provision for the INHIB_alarm_name_EN control bit is optional). On power up, or on a HW reset, this control bit is set up with a zero.

3) Delayed release of Unlatched alarm signal for interrupt generation when the inhibition condition for the secondary latched alarm is removed ('off-delay' timer). This blocks the generated secondary alarm for sufficiently long duration so that its delayed exit after the exit of the Primary alarm is kept from actuating the secondary latched event. For example, for a VT Demapper, the VT AIS alarm exit could take 3 SONET/SDH multiframes, or 1.5 milliseconds to integrate. If an Upstream AIS alarm is used to inhibit the VT AIS alarm, the inhibit function could stay in effect for 1.5 ms after the Upstream AIS alarm exits.

The Unlatched Alarm when not blocked by the inhibition function, gives rise to two possible sets of latched alarm event bits, discussed above and below.



LATCHED ALARM BITS FOR PM/FM (L2ALARM_NAME), PERFORMANCE MONITORING (PM BITS; PALARM_NAME) AND FAULT MONITORING (FM BITS; FALARM_NAME)

The Latched Alarm bits for PM/FM are capable of latching according to the states given in the following table. LPF(1-0) are global configuration bits for the group of latched event bits for PM/FM. These bits are named L2Alarm_name, corresponding to the Unlatched Alarm, Alarm_name. Also, the corresponding PM and FM bits are named PAlarm_name and FAlarm_name (as an example, the PM/FM bits for the OOF alarm is called POOF and FOOF respectively).

Software access to this set of latched event bits:

Normal mode: Latched Read Only; Writable for 0's only. These latched event bits for PM/FM are cleared by writing them with a zero by the microprocessor, or, on 1-second clock rising edges, or on global resets. Writing 1's have no effect.

Masking does not apply to these bits. However, inhibition does apply.

PM/FM registers have a hierarchy that is identical to the basic system alarm hierarchy, that governs the interrupt hierarchy.

Note that 1-second interval boundaries are used to determine the state of a given Alarm or event over the immediately preceding 1-second interval; whether an alarm persisted for multiple seconds; to obtain 1-second performance counts; and to operate the 1-second Performance and Fault Monitoring registers, and Performance Counter shadow registers. The 1-second clock may be an external input, that is distributed globally throughout the device, or, obtained inside the device as a derivative of some other external reference input. The 1-second clock input is synchronized with respect to the time base that the Host microprocessor uses to initiate the 1-second reads. It is extremely important that this be so since otherwise, PM/FM data and performance counts may be lost.

The table below shows the action of these control bits, in selection of the active transition in the main unlatched alarm for setting the latched event bits:

Table 311: Latched Alarm Bit (L2Alarm_name) Transition Selection

| LPF1 | LPF0 | Action |
|------|------|---|
| 0 | 0 | Latched status bits for PM/FM disabled. |
| 0 | 1 | Latched status indication sets on positive alarm transition. |
| 1 | 0 | Latched status indication sets on negative alarm transition. |
| 1 | 1 | Latched status indication sets on both positive and negative alarm transitions. |

The PM/FM latched event bit and the main unlatched alarm together set up the PM/FM indication bits as shown in the following timing diagrams, for all the three active options of the LPF(1-0).

The PM/FM 1-second shadow registers are enabled with the control bit SRGEN set to 1. This control bit also enables the 1-second PM Counter shadow registers if applicable. Note that the PM/FM registers can be cleared either by the microprocessor writing zeros to these locations of the memory map, or on the rising edges of the 1-second clock.

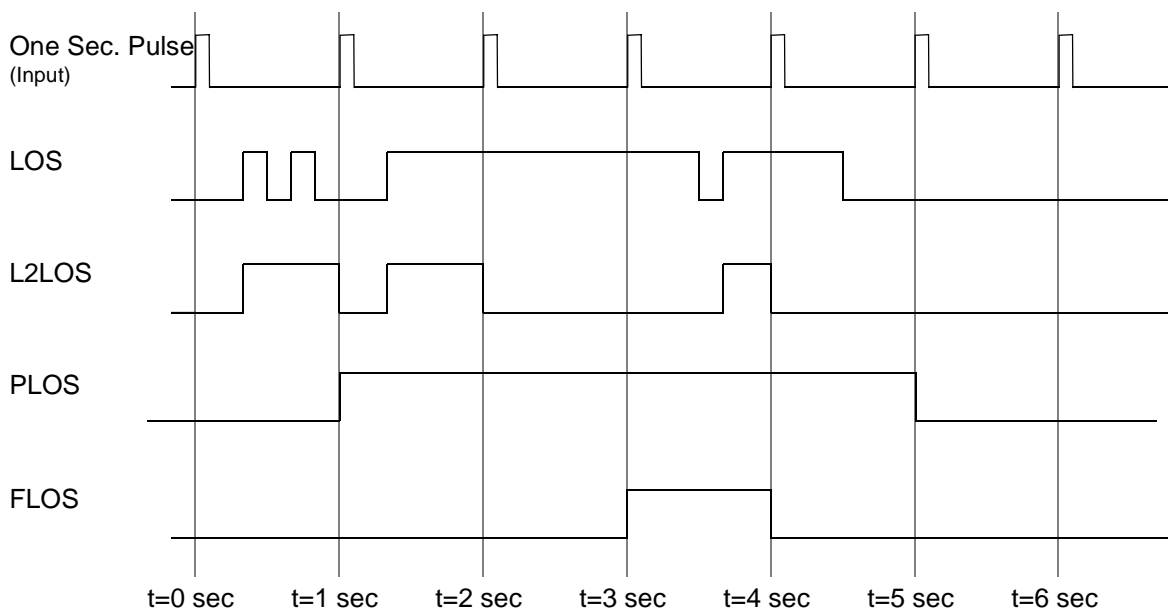
Positive Edge Events

The following diagram shows the case for the rising edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 01, the transition from 0 to 1 of the LOS alarm will cause the L2LOS bit to latch. (The alarm status can be determined by reading periodically the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place).

Assume that the PM/FM shadow registers are enabled. Then on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate (a) the Unlatched Alarm entered in the preceding 1-second interval, OR (b) the current unlatched alarm was active for at least the entire preceding 1-second interval. In addition, the FM indication bit FLOS is set if the alarm is active, but the transition to the active state did not occur in the last 1-second interval (i.e., the alarm has persisted for longer than 1-second). The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, $LOS + L2LOS = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, $LOS \& \overline{L2LOS} = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the transition having occurred in the immediately previous interval. Hence, the combination $PLOS \& \overline{FLOS} = 1$ is interpreted as an alarm entry in the immediately previous interval; and $FLOS = 1$ shows a persistent fault.



Note 1: For this example, latched events are set only on positive event transitions.

Note 2: $PLOS = LOS + L2LOS$ evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: $FLOS = LOS \& \overline{L2LOS}$ evaluated at 1-second boundaries (where '&' is a logical and, and \overline{X} is a logical inversion).

Figure 60. Positive Edge Event - PM/FM Signal Generation

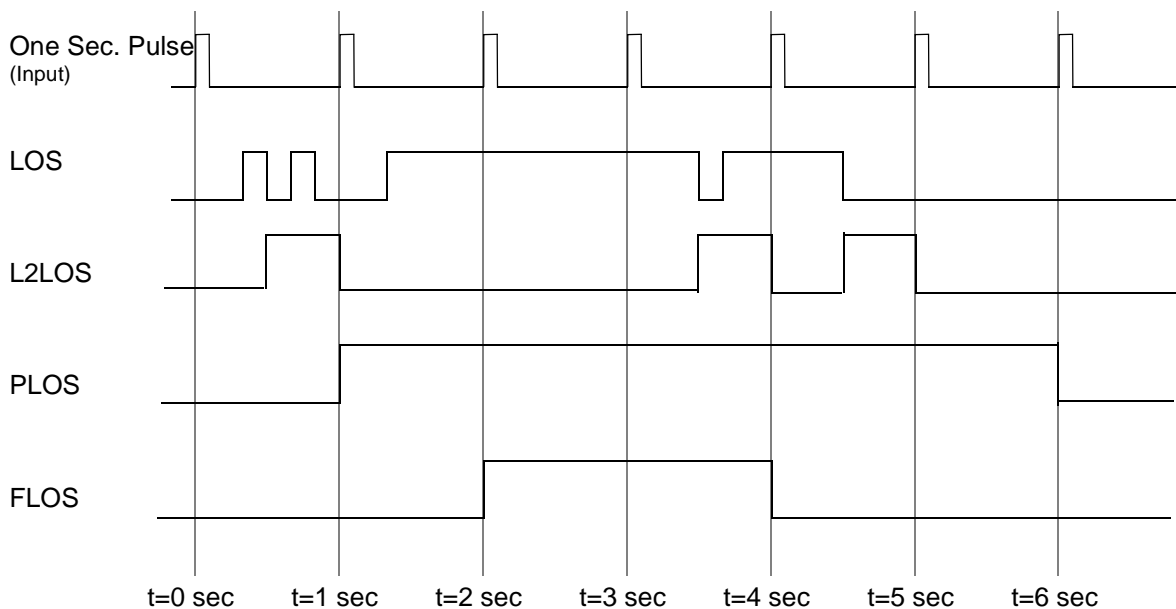
Negative Edge Events

The following diagram shows the case for the falling edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 10, the transition from 1 to 0 of the LOS alarm causes the L2LOS bit to latch. The L2LOS alarm event now signifies an alarm exit. As in the previous case for the rising edge transition, the alarm status can be determined by periodically reading the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place.

Assume that the PM/FM shadow registers are enabled. Then, on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate either: (a) the Unlatched Alarm exited in the preceding 1-second interval, or (b) the current unlatched alarm was active for at least the entire preceding 1-second interval. For the negative transition case, the FM indication bit FLOS is set if the alarm is active, AND the alarm did not clear in the last 1-second interval. The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, $LOS + L2LOS = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, $LOS \& \overline{L2LOS} = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the negative edge transition having occurred in the immediately previous interval. Hence, for the NEG EDGE event, the combination $PLOS \& \overline{FLOS} = 1$ is interpreted as the alarm LOS cleared in the immediately previous interval; and $FLOS = 1$ shows a persistent fault, or the unlatched alarm occurred in the previous interval.



Note 1: For this example, latched events are set only on negative event transitions.

Note 2: $PLOS = LOS + L2LOS$ evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: $FLOS = LOS \& \overline{L2LOS}$ evaluated at 1-second boundaries (where '&' is a logical and, and \overline{X} is a logical inversion).

Figure 61. Negative Edge Event - PM/FM Signal Generation

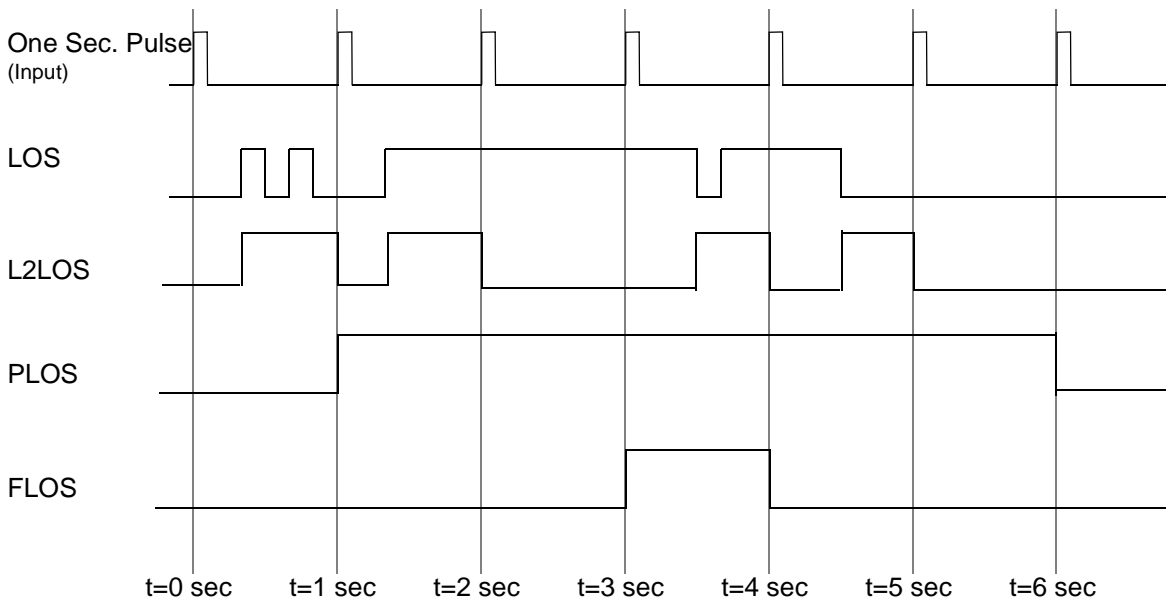
Positive or Negative Edge Events

The following diagram shows the case for the rising or falling edge transition in the example Unlatched Alarm, Loss of Signal (LOS). Assuming that control bits LPF(1-0) = 11, the transition from 1 to 0, or, from 0 to 1, of the LOS alarm causes the L2LOS bit to latch. The L2LOS event now signifies either an alarm entry or exit. The alarm status can, as in the previous cases, be determined by reading periodically the unlatched alarm status bit, until it becomes 0, indicating that recovery has taken place.

Assume that the PM/FM shadow registers are enabled. Then, as before (for the rising edge only or falling edge only cases), on rising edges of the input 1-second clock, the PM indication bit PLOS is set to indicate either: (a) there was an alarm event, either entry or exit, in the Unlatched Alarm in the previous 1-second interval; OR (b) the Unlatched Alarm has been asserted over the past 1-second interval. For the positive or negative transition case, the FM indication bit FLOS is set if the alarm is active, AND the alarm did not enter or clear in the last 1-second interval (i.e., the alarm has persisted for longer than 1-second). The rising edge of the 1-second pulse is also reset the latched event bit position L2LOS independent of the microprocessor.

Note that PLOS is set on rising edge of the 1-second clock, when, $LOS + L2LOS = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that even if the duration of the fault event is much smaller than the 1-second interval, the PLOS signal captures it.

Note also that FLOS is set on rising edge of the 1-second clock, when, $LOS \& \overline{L2LOS} = 1$, evaluated just prior to the time L2LOS is reset to 0. This ensures that FLOS is set on a 1-second edge, only if the unlatched alarm was active, without the transition having occurred in the immediately previous interval. Hence, for the POS or NEG EDGE event, the combination $PLOS \& \overline{FLOS} = 1$ is interpreted as the alarm LOS entered or cleared in the immediately previous interval; and $FLOS = 1$ shows a persistent fault, with the unlatched alarm transition, positive or negative, NOT having occurred in the previous interval.



Note 1: For this example, latched events are set on positive or negative event transitions.

Note 2: $PLOS = LOS + L2LOS$ evaluated at 1-second boundaries (where '+' is a logical or).

Note 3: $FLOS = LOS \& \overline{L2LOS}$ evaluated at 1-second boundaries (where '&' is a logical and, and \overline{X} is a logical inversion).

Figure 62. Positive/Negative Edge Event - PM/FM Signal Generation

OVERALL ALARM GENERATION AND PM/FM PROCESS DIAGRAM

The following is a signal flow diagram that illustrates the process of generating the L1Alarm_name and L2Alarm_name bits from the common starting input of the Unlatched Alarm (Alarm_name). The diagram is based on the Alarm inhibition process. Included is a basic view of the logic diagram used for setting the software polling bits and the hardware interrupt (where & is an “and” function, and + is an “or” function), using the L1Alarm_name, and the corresponding Mask bit. Note the diagram shows a simplified situation, without any hierarchies. The ‘Off Delay’ is the time for which the inverter output is held low after the alarm inhibition condition is removed (when INHIB_Alarm_name_EN = 1). A clock together with a counter could be used to realize this delay; the clock is such that counter sizes are minimized, while providing the appropriate level of granularity, so that the smallest required delay can be realized efficiently. The PM/FM Bit generation starting from the L2Alarm_name bit is included. Note that both the L1Alarm_name and the L2Alarm_name bits are subject to the same inhibiting condition.

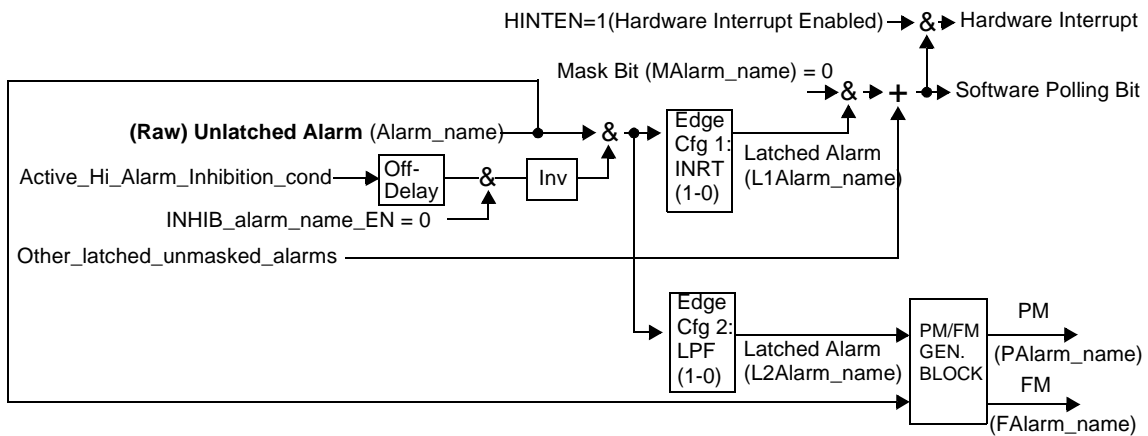


Figure 63. Alarm, Interrupt and PM/FM Generation Process

If the Alarm Inhibition function is adopted, then the signal simplifies as follows:

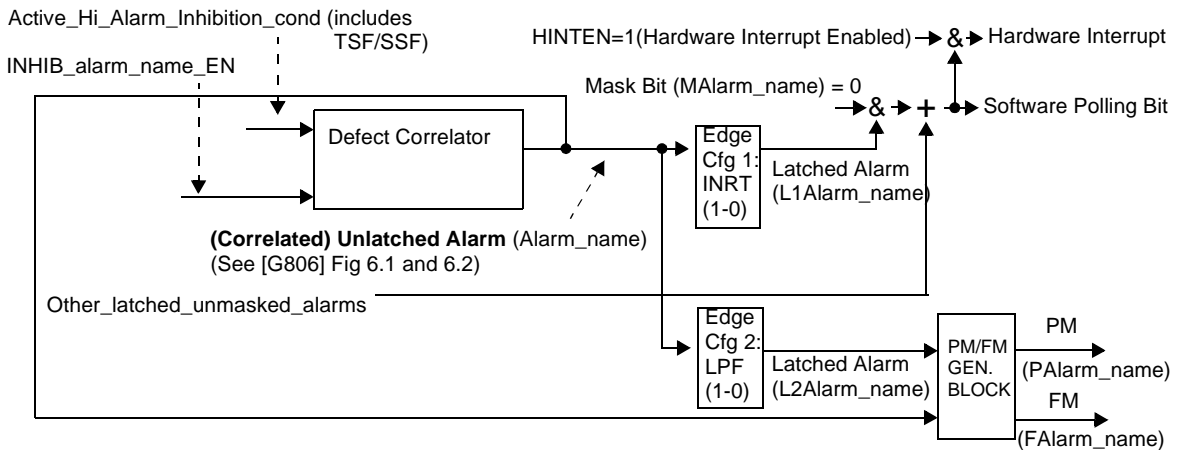


Figure 64. Alarm, Interrupt and PM/FM Generation Process (Inhibition Function)

PERFORMANCE COUNTERS

Performance Counters in the EtherMap-3 Plus device use two different schemes, as dictated by their respective functions:

Scheme A - Counters with Roll-Over/Saturation Option

These performance counters are configurable to be either saturating or non-saturating.

When the performance counters are configured to be saturating, the counters stop at their maximum count. In the saturating mode, counts that occur during a micro read cycle, are held off and the counter updates later. A saturating counter is reset to zero on a microprocessor read cycle.

When the performance counters are configured to be non-saturating they roll over to 0 on the next count after the maximum count is reached (i.e., all ones). In this mode, the counters do not clear on a microprocessor read cycle, but continue to count. When a "reset counters" operation is performed, these performance counters are set to an all-zeros value.

This type of counter is used in the following two areas:

The Encapsulation and Decapsulation blocks, with performance counters described in Tables 43 and 60. Control bit CROV (0x194a6, Table 10) selects between saturate and roll-over.

The Ethernet MAC blocks, with performance counters described in Tables 13, 14 and 15. Control bit AUTOZ (0x1d340, Table 30) selects between saturate and roll-over.

All performance counters may be reset simultaneously by writing a 91H to top level register RESETC.

All counters in the device that can be read by the microprocessor, are of the 'Read/Write' type, and for test purposes, the microprocessor is able to write any value to them.

A status alarm bit COUNT with an associated interrupt mask bit MCOUNT is provided. The COUNT status bit is set when any of the performance counters has reached its maximum value in the saturating mode of operation only. When a microprocessor reads the saturated counter, the counter is cleared, but the latched alarm (LCOUNT) is not cleared unless read and cleared separately.

Scheme B - Performance Counters with 1-second Shadow Register Option

The differences from scheme A, are:

1. There are designated bits (1 bit for each counter) available, that take up counter overflow, for each counter.
2. In the event that a terminal count is reached, the overflow bit is used as an indicator. There is no equivalent of the CROV configuration bit as in the case of scheme A.
3. The Counters can only be cleared by the rising edge of a 1-second interval boundary, or, if the microprocessor writes 0's to the counters. The counters are reset to all 0's.
4. At the 1-second boundary, the contents of the Performance counter are transferred, along with the overflow indication bit, to a 1-second shadow register for the particular counter, after which the counter is cleared. Thus, the 1-second shadow register for the performance counter updates only on 1-second boundaries.
5. The 1-second shadow registers are enabled with the common shadow register enable control bit, SRGEN.
6. There is no equivalent of the COUNT alarm, for saturated counter operation, as with Scheme A.

Clearing/Resetting of Performance Counters in Scheme B, is accomplished in a manner similar to that of Scheme A.

The shadow register holds its count during a microprocessor read cycle. However, the main Performance Counters may be updated internally on a coincident 1-second boundary, for a count update.

This type of counter is used in the TX Mapper and Rx DeMapper block.

ALARM FEATURE COMBINATIONS

Each defined system alarm or event, have associated with it one of the following groups of features:

Group 1:

- A main unlatched alarm signal (Alarm_name).
- A Latched Alarm Indication an Unlatched Alarm, for the purpose of status and interrupt generation (L1Alarm_name).
- Latched Alarm Interrupt Mask bit (MAalarm_name).

Group 2:

- Features Group 1.
- A Latched Alarm Indication for an Unlatched Alarm, for the purpose of 1-second Performance and Fault Monitoring (L2Alarm_name).
- 1-second PM bit (PAalarm_name).
- 1-second FM bit (FAalarm_name).

Group 3:

- Features Group 1.
- Performance Counter.

Group 4:

- Features Group 2.
- Performance Counter.

Group 5:

- Performance Counter Only; Note that there may be Performance Counters that are not associated with any alarm (for example, SONET/SDH Pointer Justification Counters).

Group 6:

- A Latched Alarm Indication for the main unlatched system alarm or event, for the purpose of 1-second Performance and Fault Monitoring (Alarm 2).
- 1-second PM bit.
- 1-second FM bit.
- Performance Counter.

It is the responsibility of the individual device's specification to completely specify for each alarm, the following:

1. Group of features applicable.
2. Main Unlatched Alarm Entry Condition, with standard reference if applicable.
3. Main Unlatched Alarm Exit Condition, with standard reference if applicable.

4. Alarm Action.
5. Hierarchical position of the alarm, that is what secondary alarms and Performance Counter(s) are inhibited on its occurrence.
6. The decision to implement a Scheme A or Scheme B Performance Counters (on a per counter basis, if applicable).
7. Inhibition Definition, Inhibition Extension Times, and Enable control bits as applicable.

SYSTEM ALARM, INTERRUPT, AND PM/FM HIERARCHY

The System Alarm and Interrupt Hierarchy are device specific, and aimed towards providing a convenient software interrupt nesting, so that poll times are considerably reduced. The PM/FM registers follow a similar hierarchy, only difference being that the PM/FM bits are not subject to masking (they are subject to inhibition however).

In general, the Alarm and Interrupt Hierarchy follow one or more of the following grouping schemes:

- Protocol Layers, example for SONET/SDH devices, Section Layer, Line/HO Path Layer, LO Path Layer.
- Channel Numbers (example, alarms/masks grouped based on VT numbers for HDM, or channel numbers for framers, etc.).
- Alarm Functionality (e.g., global alarm for a VT LOP condition).
- Receive/Transmit or other special hierarchical groupings).

Each latched alarm bit has a mask bit. In addition, depending on the grouping chosen, each hierarchical level has a consolidated Latched Alarm and associated Mask; may also have PM/FM bits, depending on Alarm Feature Group specified.

The software polling interrupt register provides a way to have the processor poll a register in memory (provided the proper interrupt mask disable bits are set) to indicate the alarms that causes the interrupt or the alarms that are set without having to read all the alarm registers until the active alarm is found.

There is also a hierarchical alarm inhibition scheme that may be implemented, based on needs and standards. The diagram of [Figure 65](#) below illustrates how an alarm and interrupt hierarchy is to be achieved:

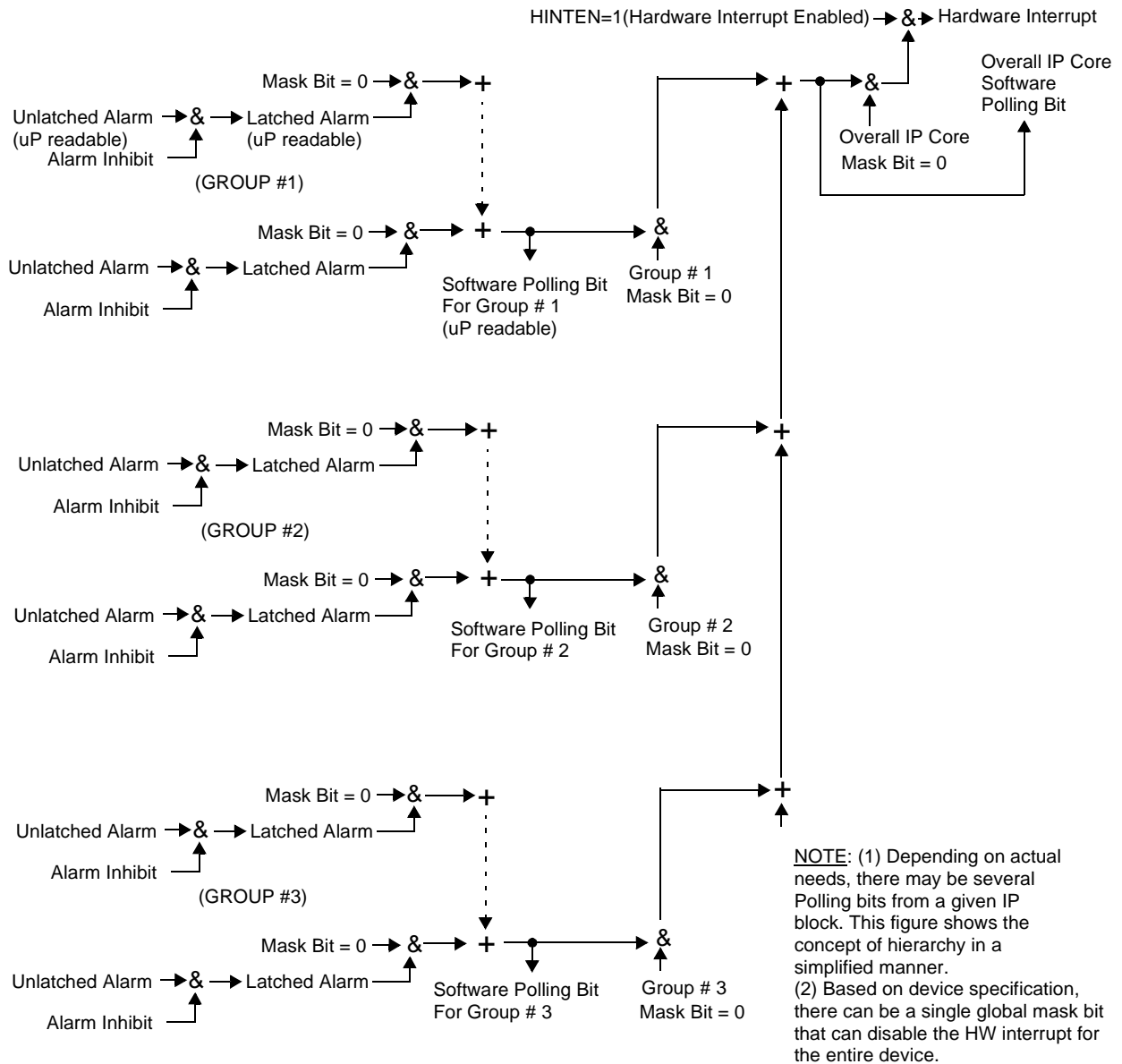


Figure 65. Alarm Interrupt Hierarchy

ALARM INTERRUPT TREE

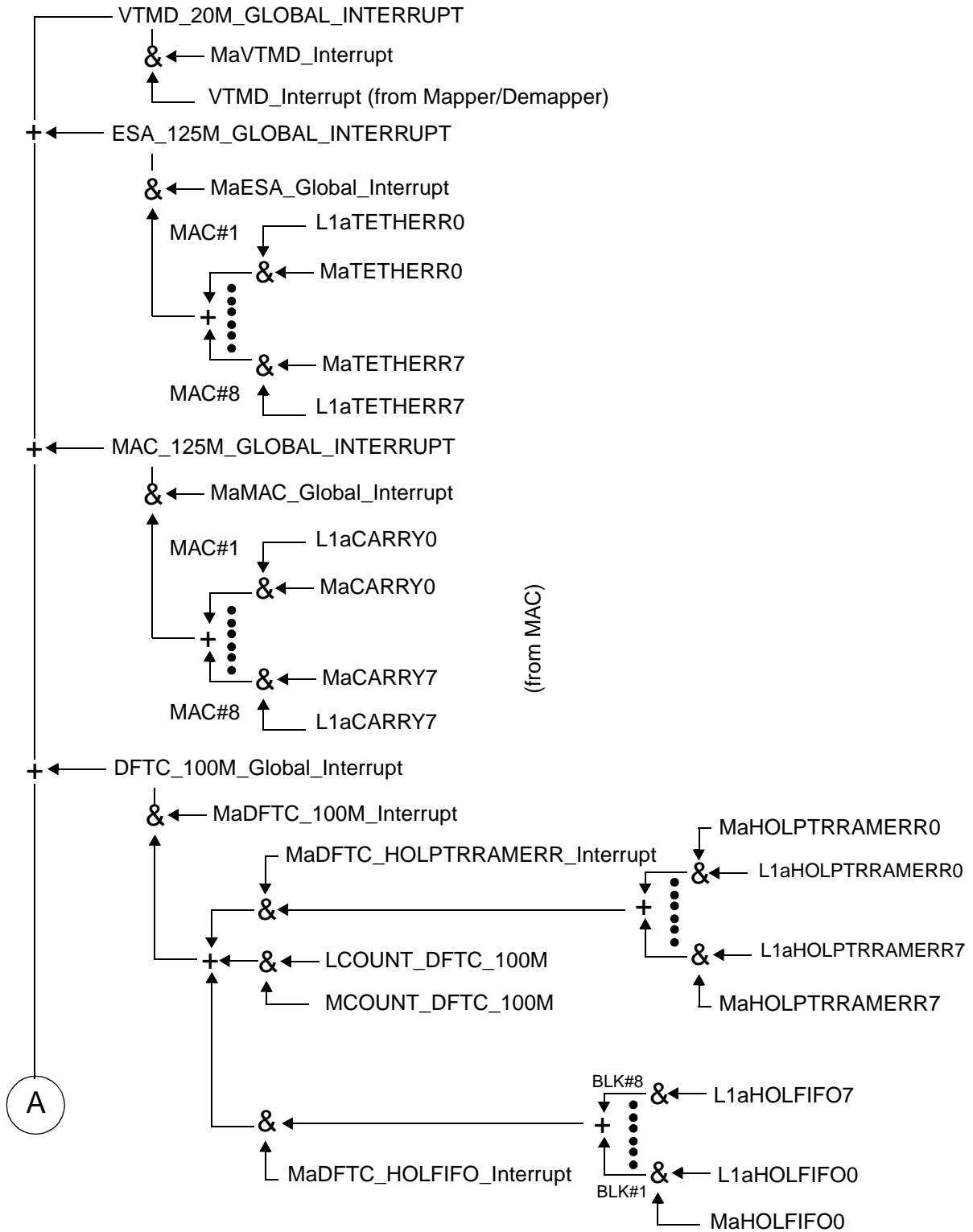


Figure 66. Alarm Interrupt Tree Part A

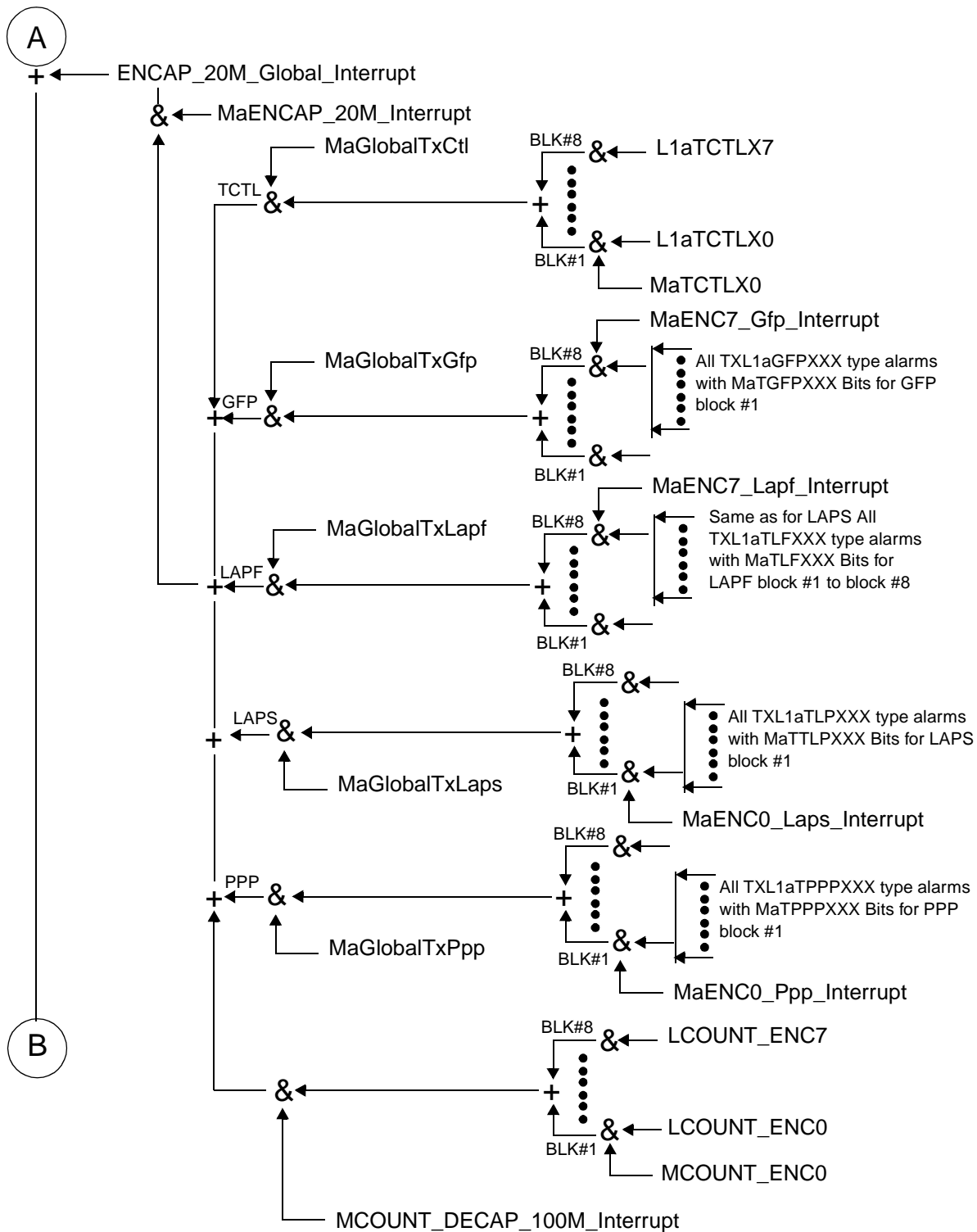


Figure 67. Alarm Interrupt Tree Part A to Part B

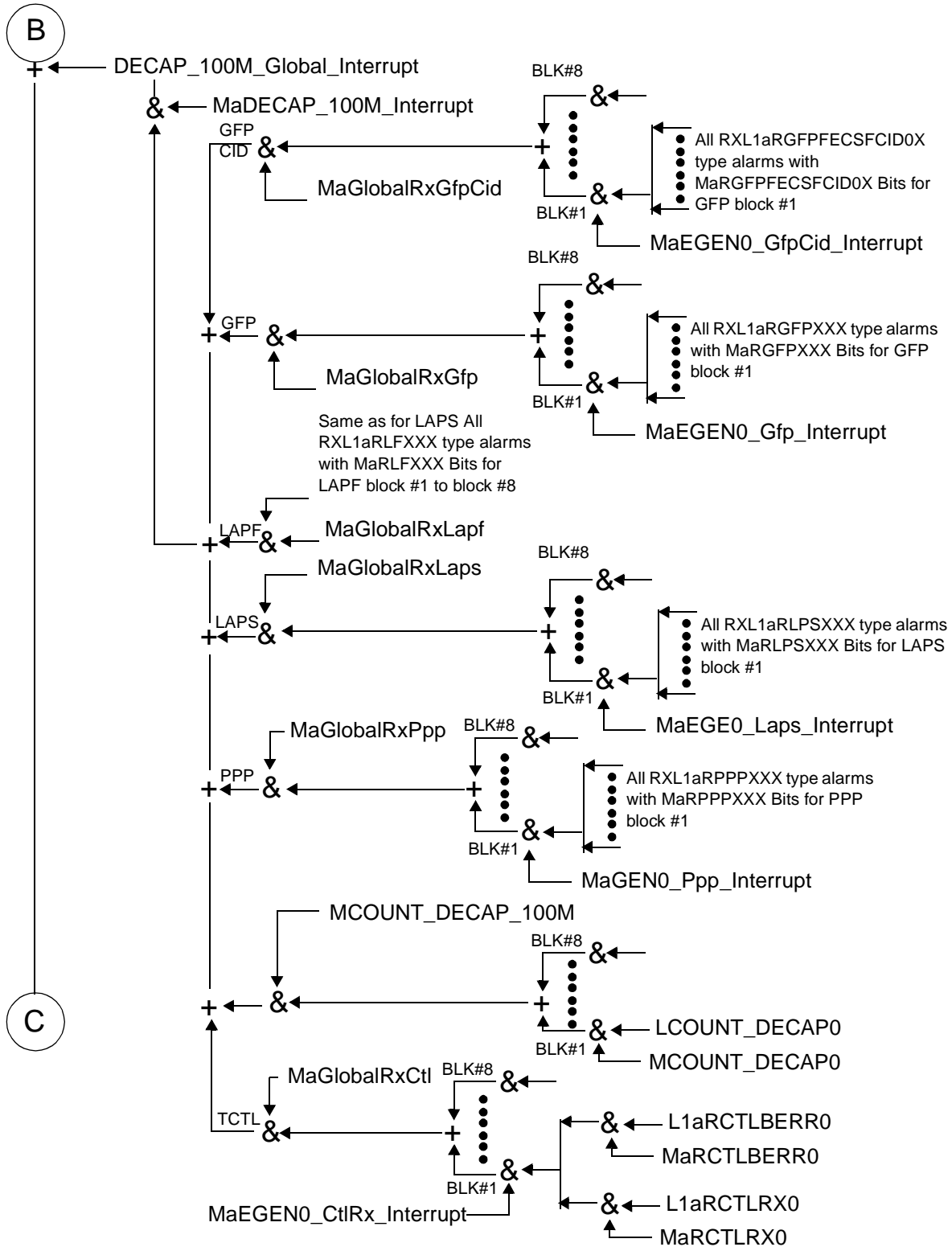


Figure 68. Alarm Interrupt Tree Part B to Part C

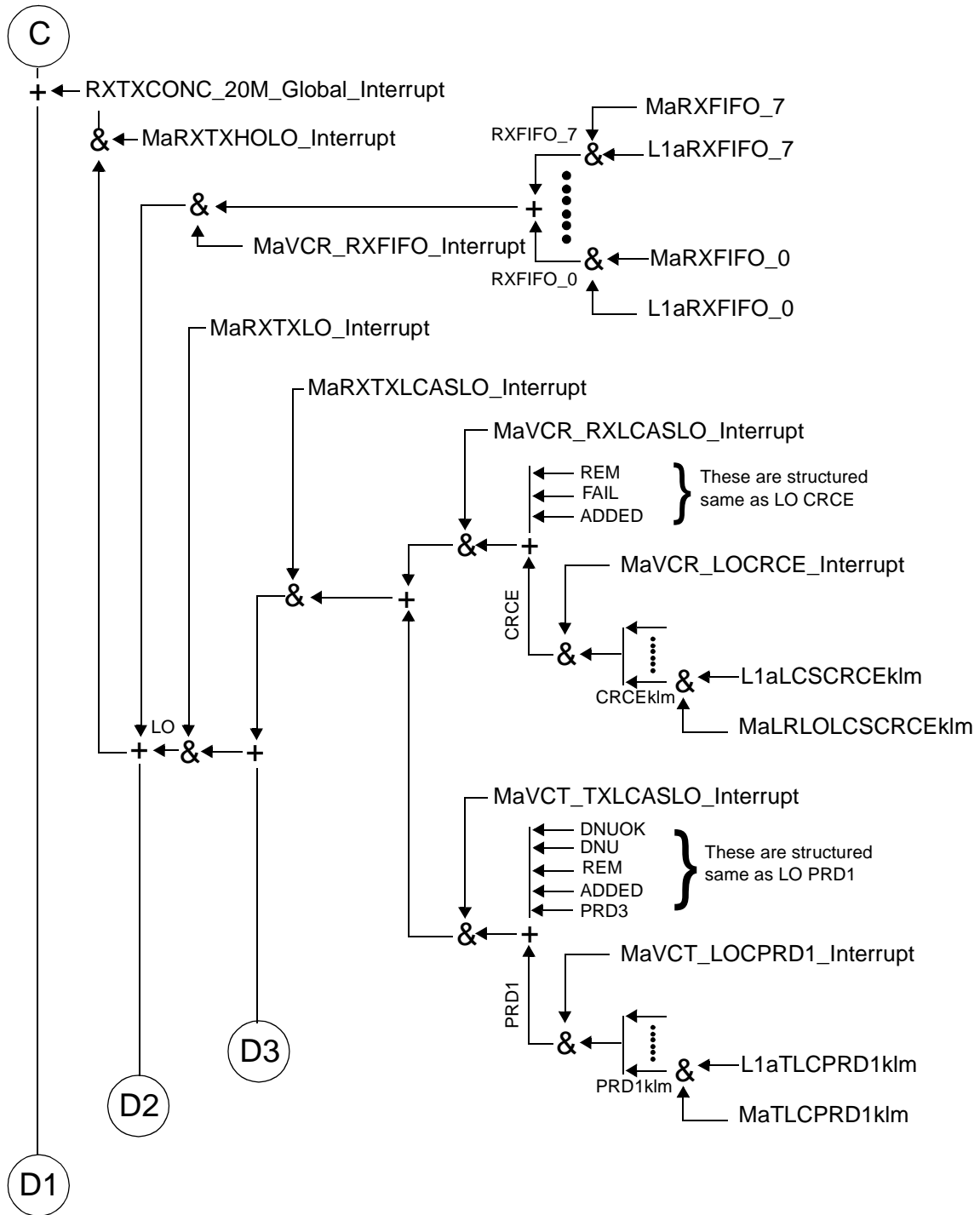


Figure 69. Alarm Interrupt Tree Part C to Parts D1, D2 and D3

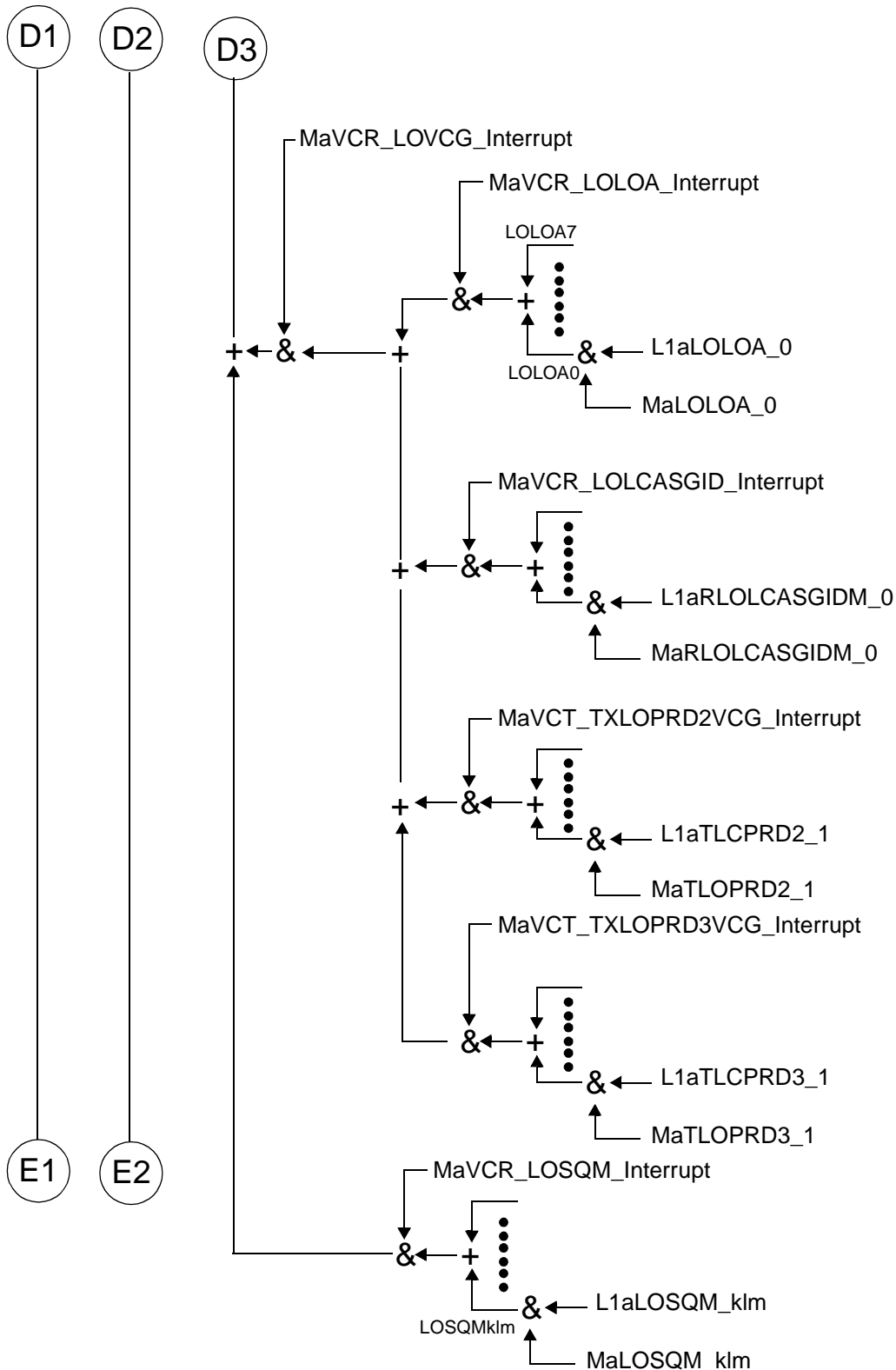


Figure 70. Alarm Interrupt Tree Parts D1, D2 and D3 to Parts E1 and E2

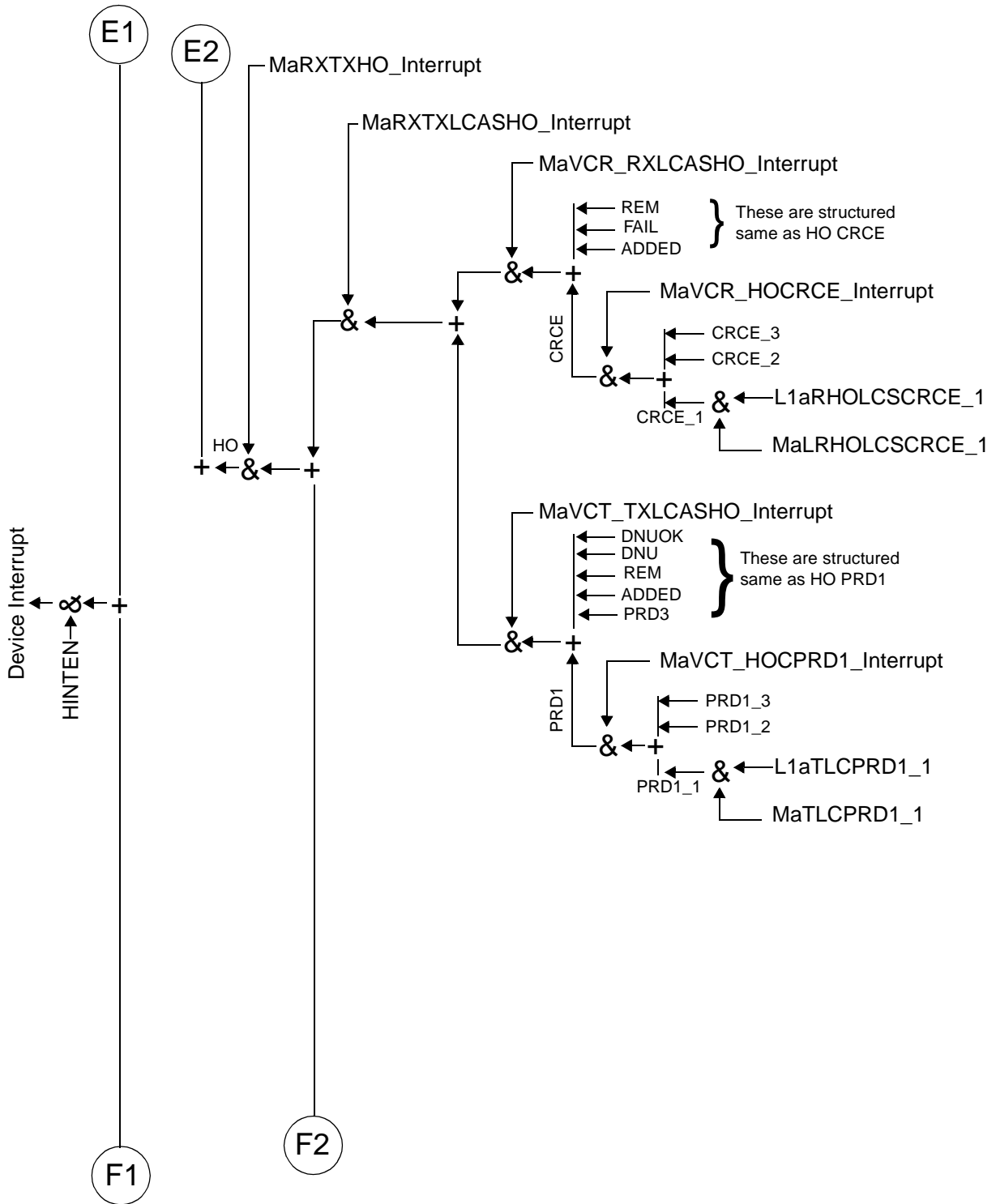


Figure 71. Alarm Interrupt Tree Parts E1 and E2 to Parts F1 and F2

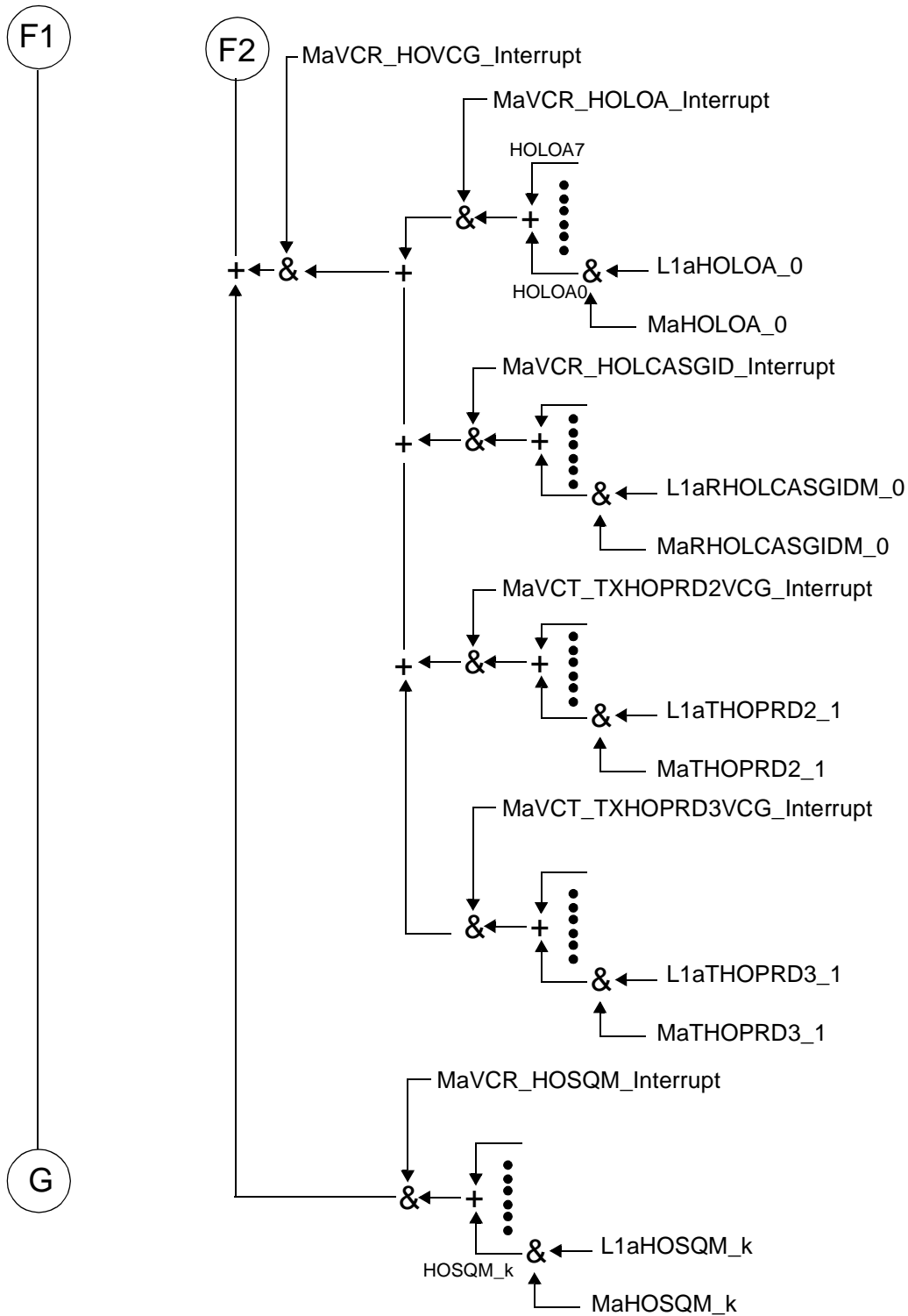


Figure 72. Alarm Interrupt Tree Parts F1 and F2 to Part G

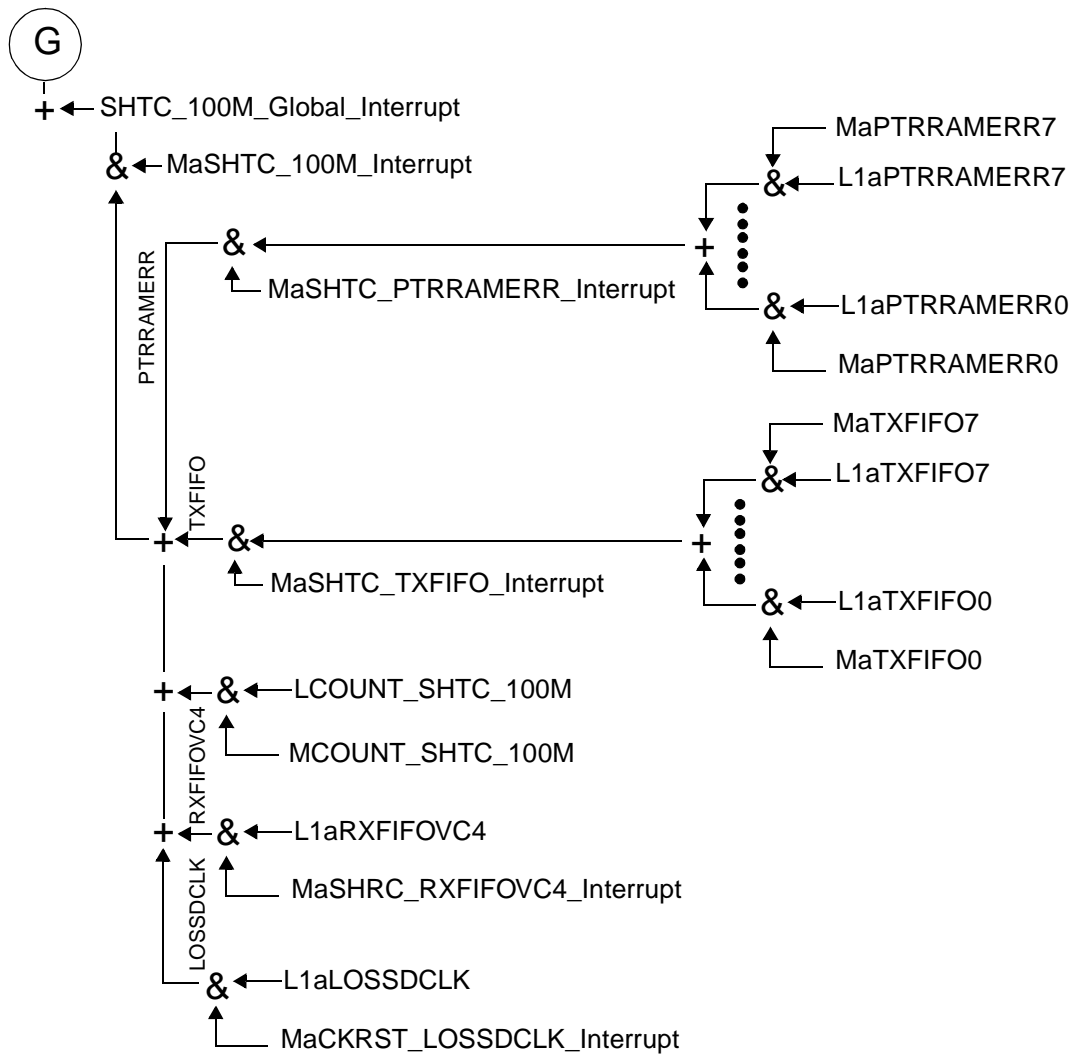


Figure 73. Alarm Interrupt Tree Part G

REGISTER TREE

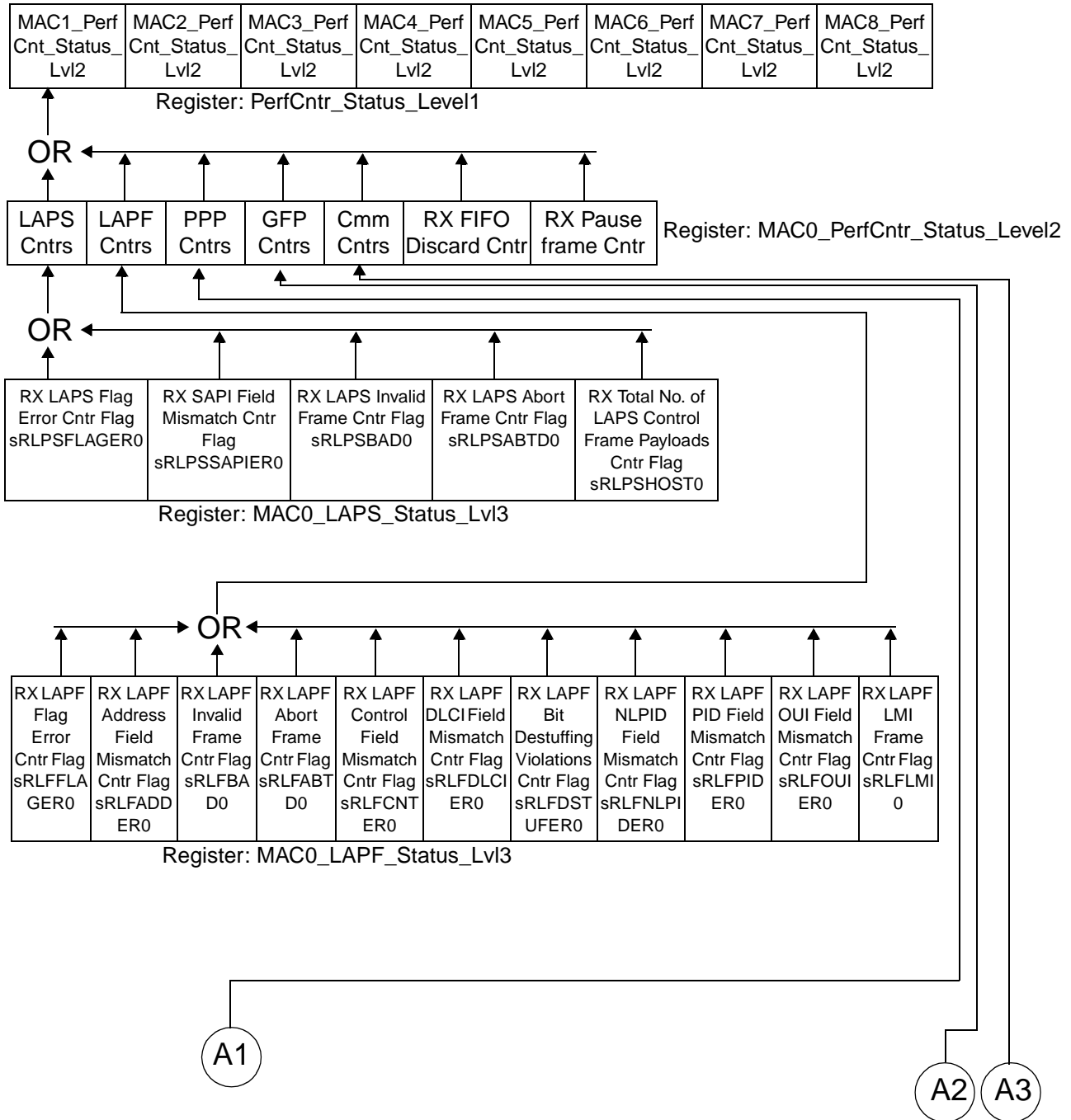


Figure 74. Register Tree Parts A1, A2 and A3

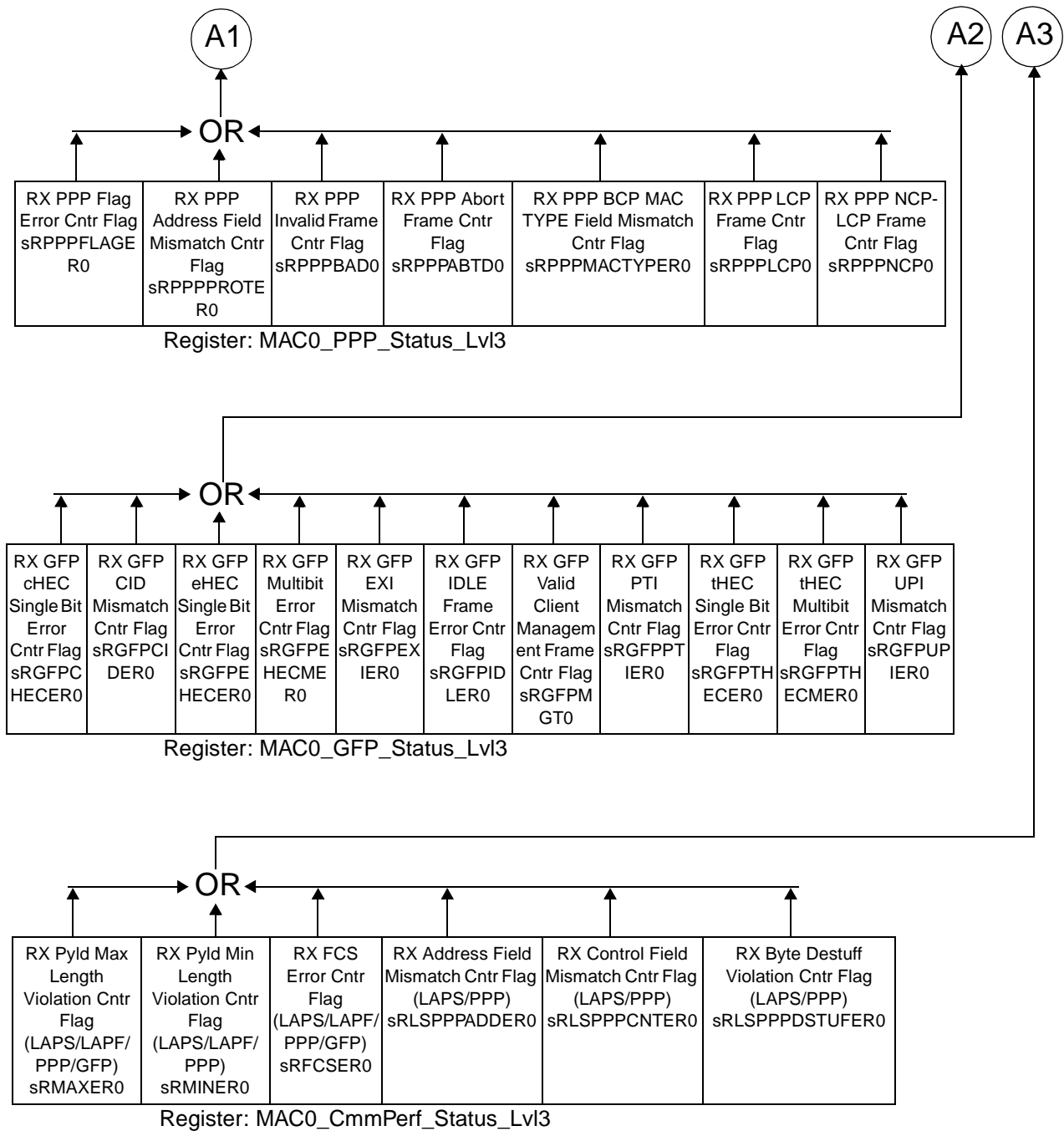


Figure 75. Register Tree Parts A1, A2 and A3 (continued)

MAPPER/DEMAPPER PERFORMANCE MONITORING

Pointer Adjustment Counters per Level 3 High Order path:

- Incoming Positive Pointer Adjustment Count,
- Incoming Negative Pointer Adjustment Count.

Pointer Adjustment Counters per Low Order path:

- Incoming Positive Pointer Adjustment Count,
- Incoming Negative Pointer Adjustment Count.

POH counters per High Order Path:

- B3 Near-End Errored BIP Count,
- B3 Near-End Errored Block Count,
- G1 Far-End Error Count, configurable to count either REI errors or errored blocks,
- Near-End Defect Second,
- Far-End Defect Second.

POH counters per Low Order Path:

- V5 Near-End Errored BIP Count,
- V5 Near-End Errored Block Count,
- V5 Far-End Errored Block Count,
- Near-End Defect Second,
- Far-End Defect Second.

All performance counters are one second shadow registers and at the one second boundary, the contents of each performance counter is latched into its one second shadow register, after which the performance counter is cleared. These one second shadow registers will hold their value during the entire period between two subsequent one second boundaries.

The one second shadow registers are available for software read-only access. All performance counters are saturating: counting will stop when the maximum count value is reached. All errored BIP and Block counters are dimensioned to cover the maximum count value during a one second interval meaning they can never reach saturation.

Mapper/Demapper Interrupt Tree

- [lo] ranges from 0 to 83 (84 low order channels)
- [ho] ranges from 0 to 2 (3 high order channels)
- [aip] ranges from 0 to 1 (internal and external alarm indication port)

VTMP_TOP_IC (Mapper/Demapper Top Level)

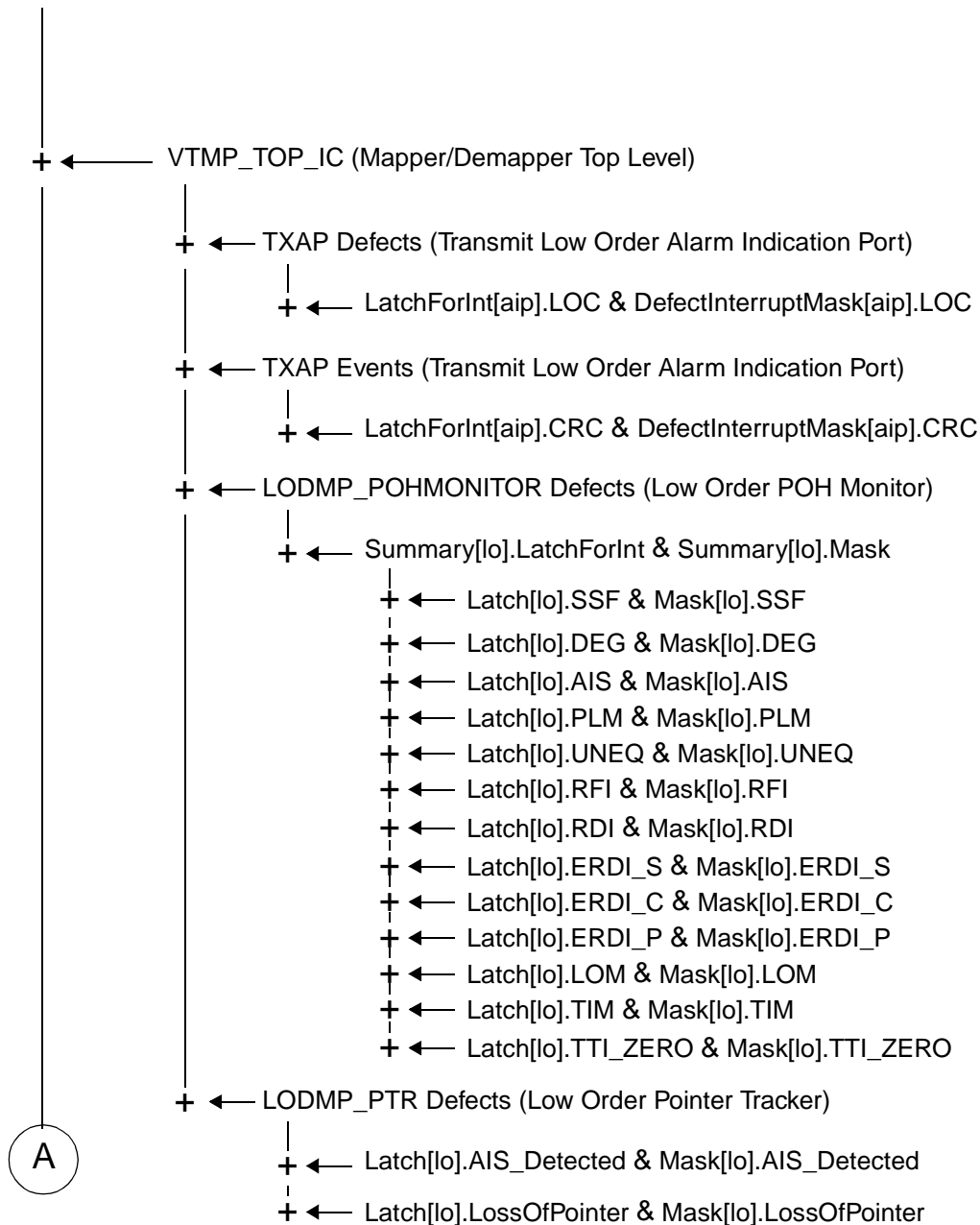


Figure 76. Mapper/Demapper Interrupt Tree Part A

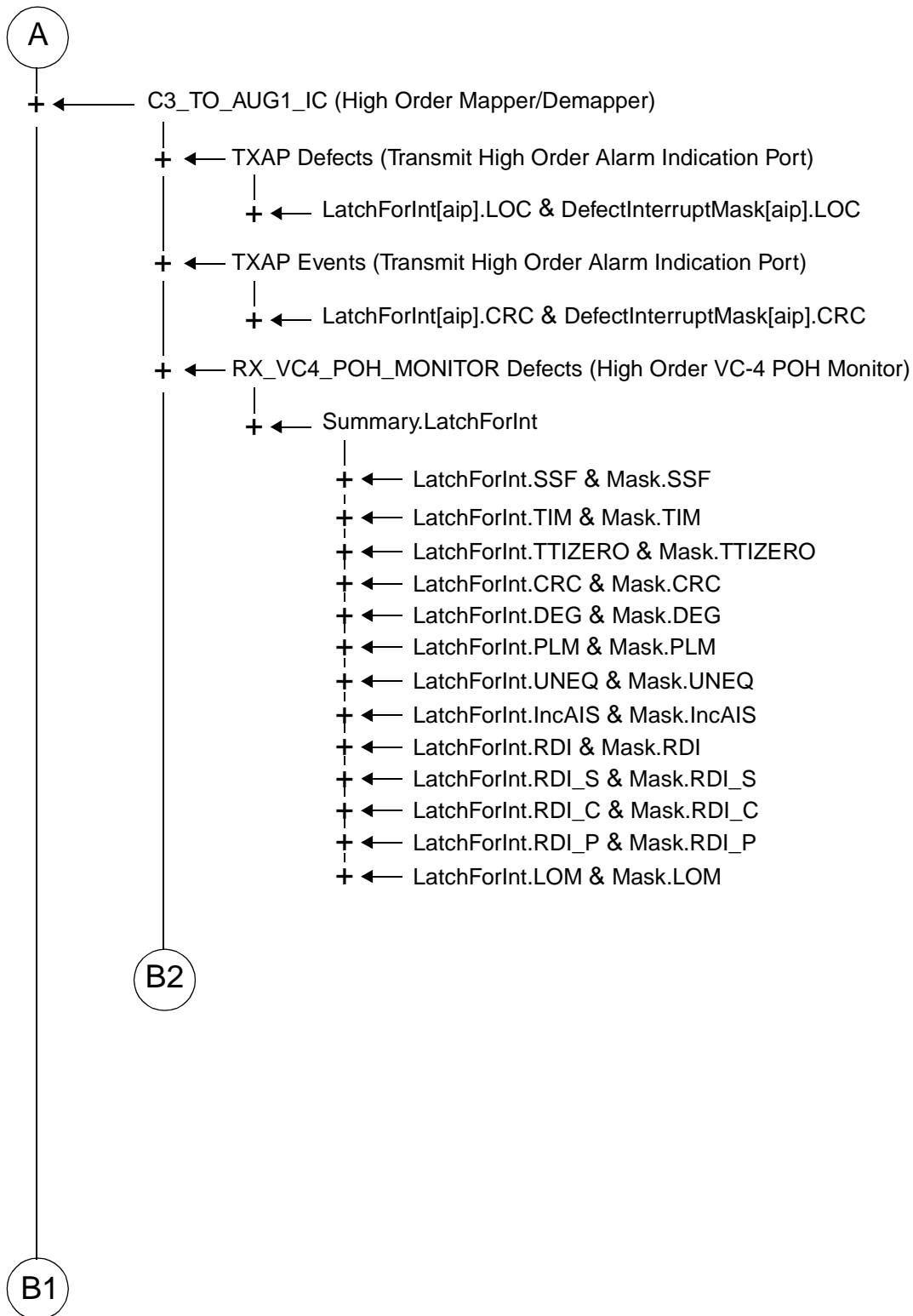


Figure 77. Mapper/Demapper Interrupt Tree Part A to Parts B1 and B2

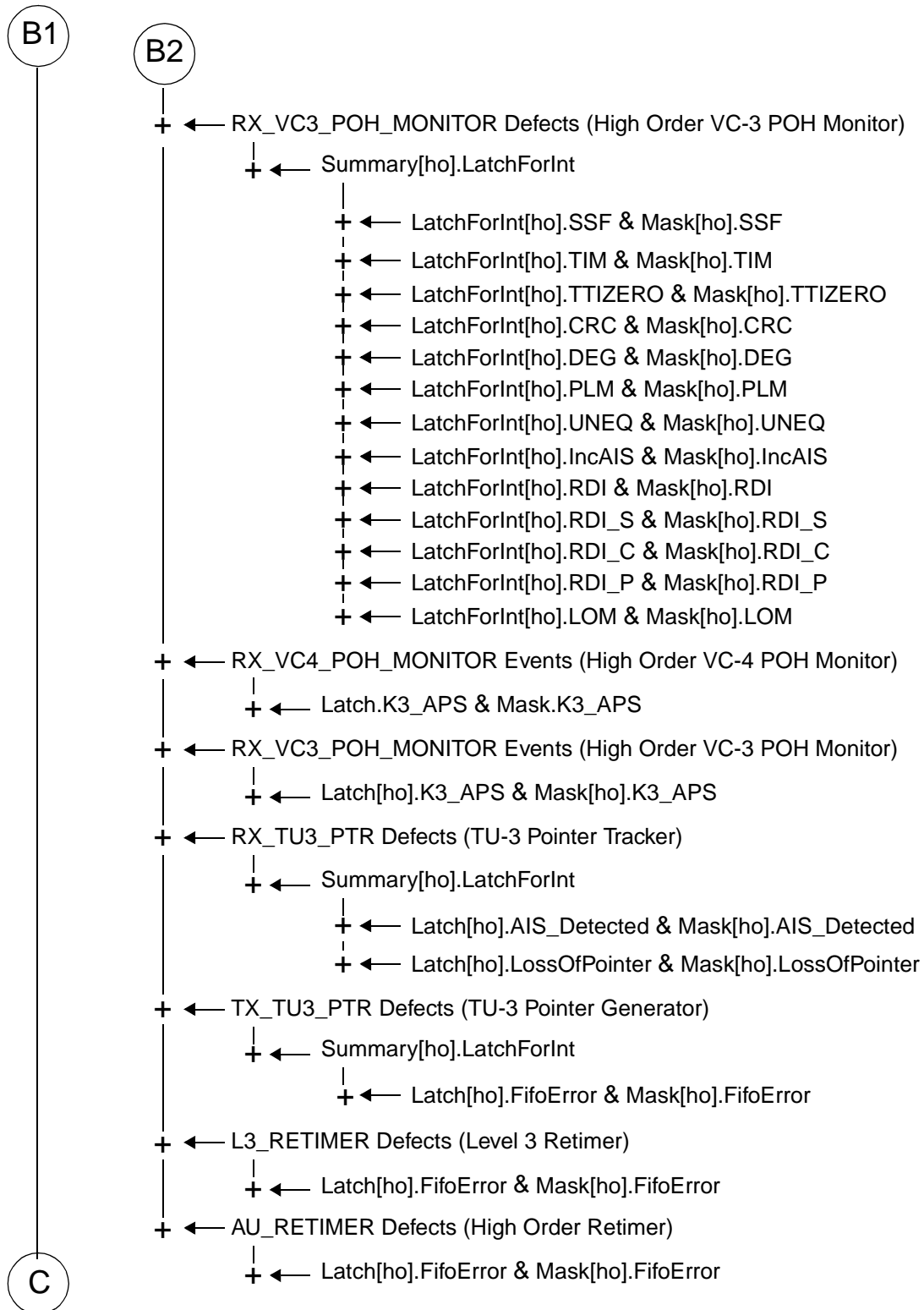


Figure 78. Mapper/Demapper Interrupt Tree Parts B1 and B2 to Part C

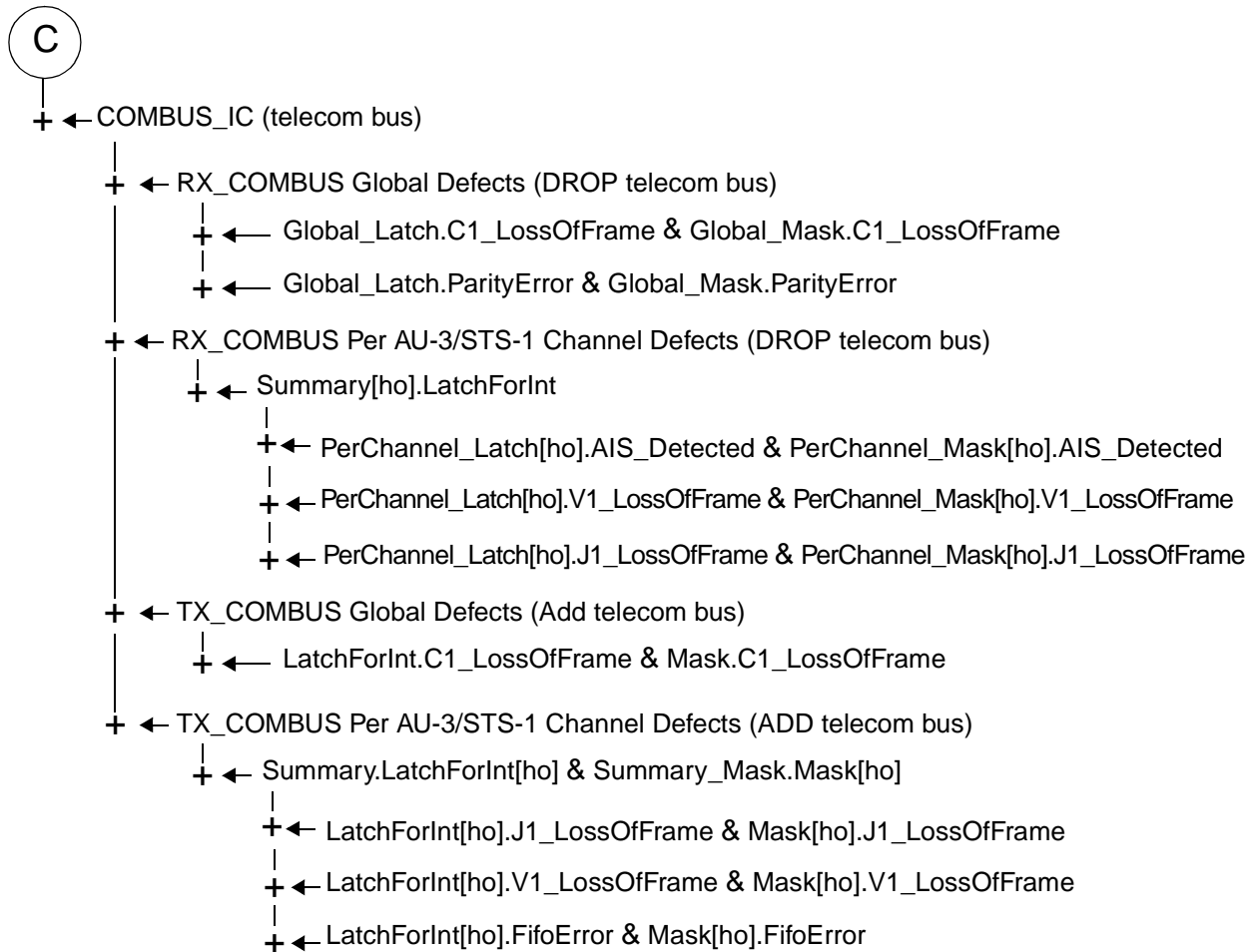


Figure 79. Mapper/Demapper Interrupt Tree Part C

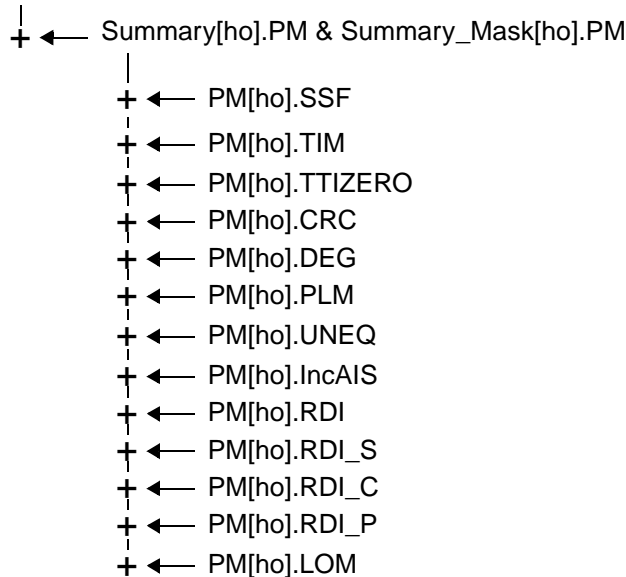
- [lo] ranges from 0 to 83 (84 low order channels)
- [ho] ranges from 0 to 2 (3 high order channels)
- [aip] ranges from 0 to 1 (internal and external alarm indication port)

Mapper/Demapper PM/FM Tree per Block

RX_VC3_POH_MONITOR (High Order VC-3/STS-1 POH Monitor):

- [ho] ranges from 0 to 2 (3 high order channels)

GroupSummary.PM



GroupSummary.FM

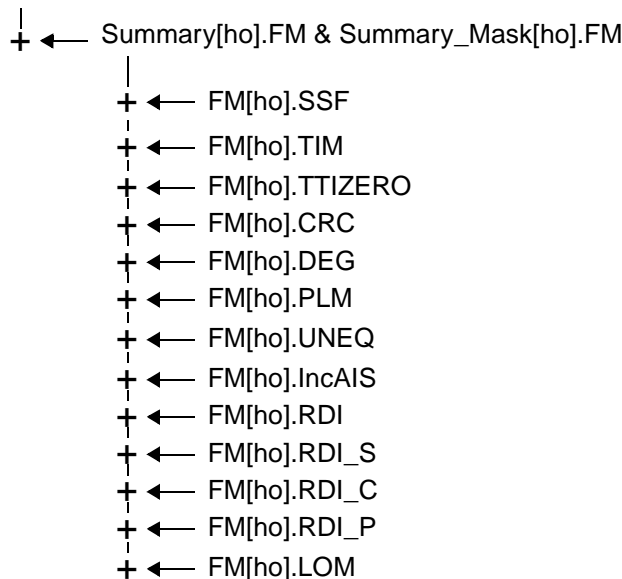
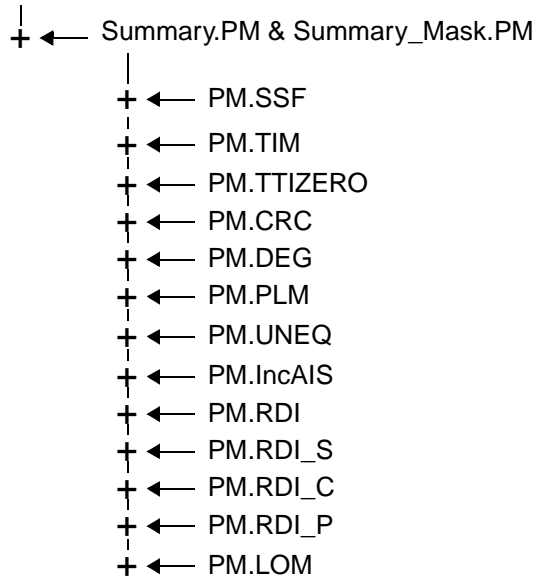


Figure 80. Mapper/Demapper RX_VC3_POH_MONITOR PM/FM Trees

RX VC4 POH MONITOR (High Order VC-4/STS-3c POH Monitor):

GroupSummary.PM



GroupSummary.FM

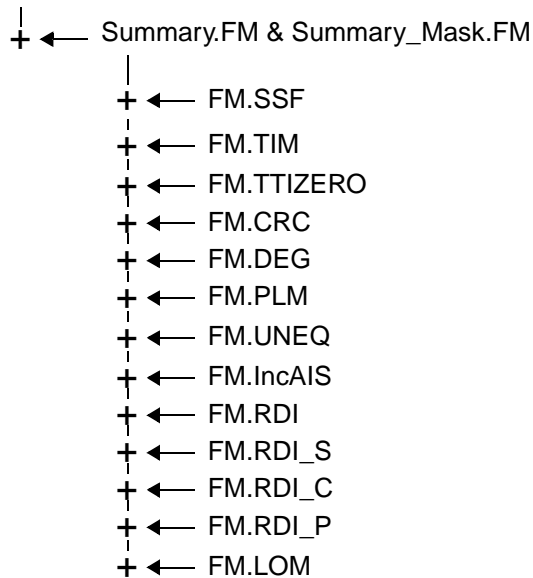
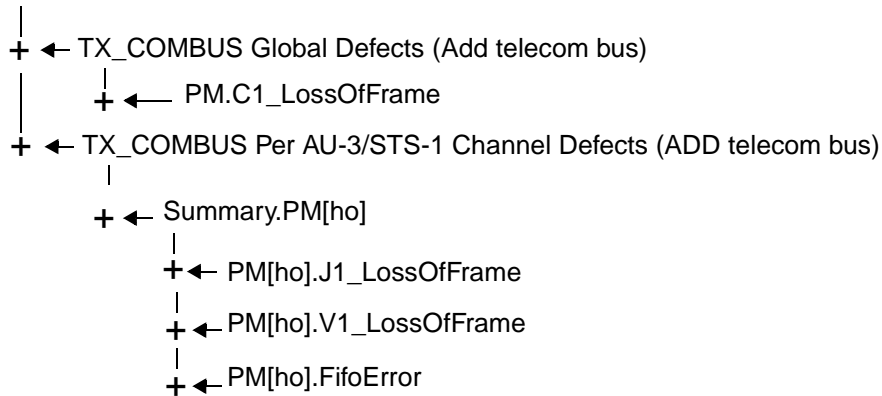


Figure 81. Mapper/Demapper RX VC-4 POH MONITOR PM/FM Trees

TX COMBUS (Transmit ADD Telecom bus):

- [ho] ranges from 0 to 2 (3 high order channels)

GroupSummary.PM



GroupSummary.FM

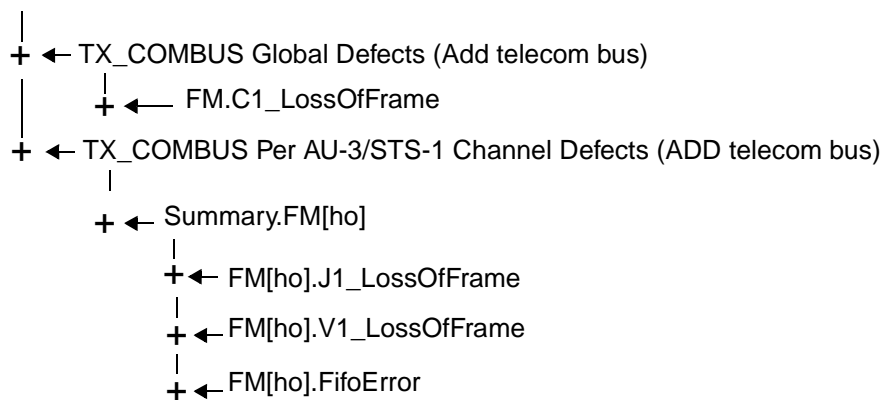


Figure 82. Mapper/Demapper TX COMBUS PM/FM Trees

RX TU3 PTR (TU-3 Pointer Tracker):

- [ho] ranges from 0 to 2 (3 high order channels)

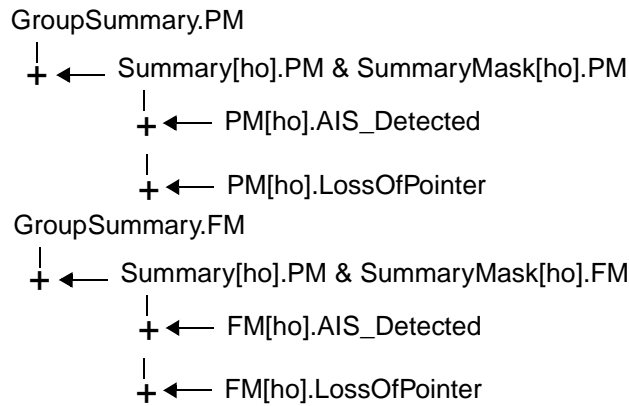


Figure 83. Mapper/Demapper RX_TU3_PTR PM/FM Trees

TX TU3 PTR (TU-3 Pointer Generator):

- [ho] ranges from 0 to 2 (3 high order channels)

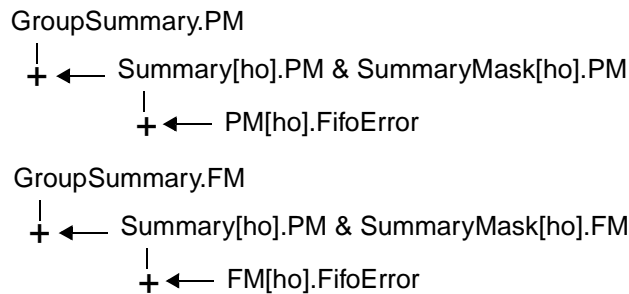
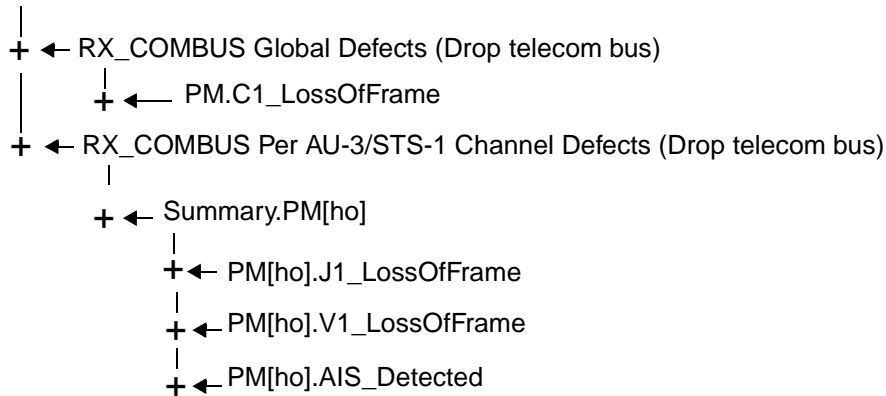


Figure 84. Mapper/Demapper TX_TU3_PTR PM/FM Trees

RX COMBUS (Receive DROP Telecom Bus):

- [ho] ranges from 0 to 2 (3 high order channels)

GroupSummary.PM



GroupSummary.FM

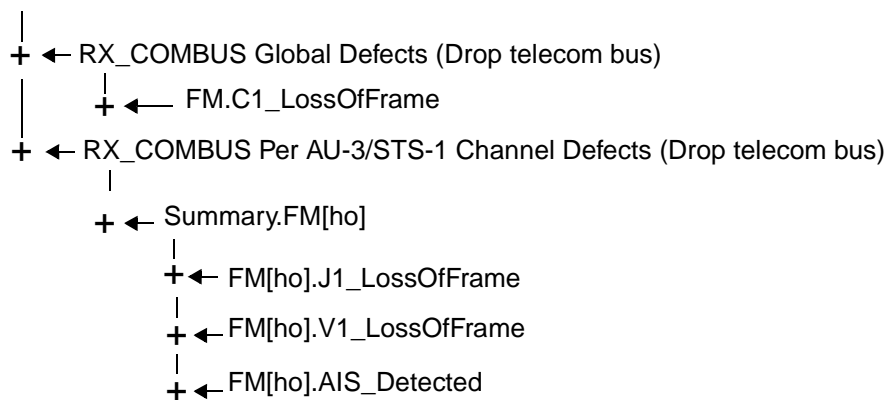


Figure 85. Mapper/Demapper RX COMBUS PM/FM Trees

LODMP_POHMONITOR (Low Order POH Monitor):

- [Io] ranges from 0 to 83 (84 low order channels)

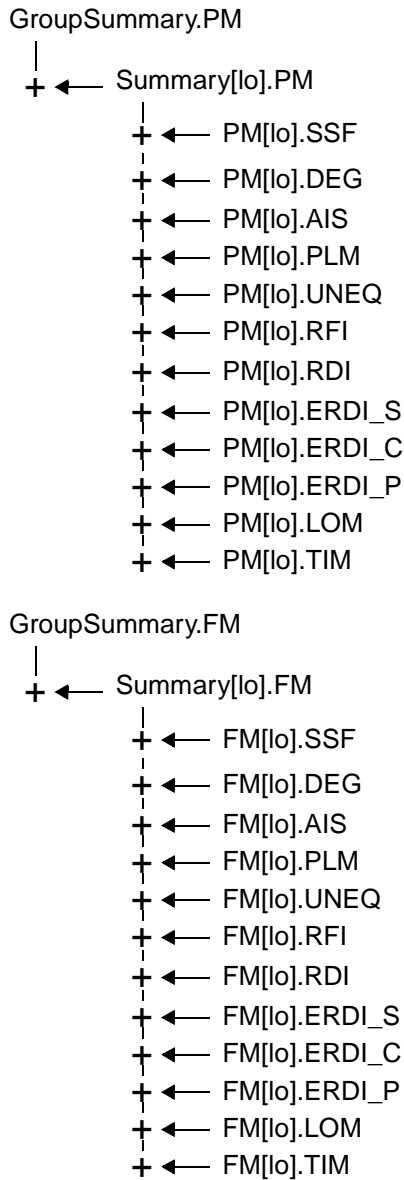


Figure 86. Mapper/Demapper LODMP_POHMONITOR PM/FM Trees

LODMP_Ptr (Low Order Pointer Tracker):

- [lo] ranges from 0 to 83 (84 low order channels)

Summary.PM

|
+ ← PM[lo].AIS_Detected

|
+ ← PM[lo].LossOfPointer

Summary.FM

|
+ ← FM[lo].AIS_Detected

|
+ ← FM[lo].LossOfPointer

Figure 87. Mapper/Demapper LODMP_Ptr PM/FM Trees

Mapper/Demapper Consequent Actions per Block

RX_VC4_POH_MONITOR (High Order VC-4/STS-3c POH Monitor):

The High Order VC-4/STS-3c POH Monitor will insert AIS per high order path according to the following expression:

aAIS = dAIS and not AIS_IncAIS_Disable
or dSSF and not AIS_SSF_Disable
or dUNEQ and not AIS_UNEQ_Disable
or dTIM and not AIS_TIM_Disable
or InsertAIS

The High Order VC-4/STS-3c POH Monitor will insert RDI per high order path towards the RX high order path Alarm Indication Port according to the following expressions:

aRDI-S = dSSF and not RDI_SSF_Disable
or InsertAIS

aRDI-C = dUNEQ and not RDI_UNEQ_Disable
or dTIM and not RDI_TIM_Disable

aRDI = aRDI-S
or aRDI-C

aRDI-P = dPLM and not RDI_PLM_Disable

The High Order VC-4/STS-3c POH Monitor will forward the dPLM and dLOM indications to the subsequent adaptation blocks (low order pointer processors or virtual concatenation receiver blocks) depending on the configured SDH/SONET mapping:

aPLM = dPLM and not PLM_PLM_Disable
aLOM = dLOM and not LOM_LOM_Disable

RX VC3 POH MONITOR (High Order VC-3/STS-1 POH Monitor):

- [ho] ranges from 0 to 2 (3 high order channels)

The High Order VC-3/STS-1 POH Monitor will insert AIS per high order path according to the following expression:

$$\begin{aligned}
 \mathbf{aAIS}_{[ho]} &= \mathbf{dAIS}_{[ho]} \text{ and not } \mathbf{AIS_IncAIS_Disable}_{[ho]} \\
 &\text{or } \mathbf{dSSF}_{[ho]} \text{ and not } \mathbf{AIS_SSF_Disable}_{[ho]} \\
 &\text{or } \mathbf{dUNEQ}_{[ho]} \text{ and not } \mathbf{AIS_UNEQ_Disable}_{[ho]} \\
 &\text{or } \mathbf{dTIM}_{[ho]} \text{ and not } \mathbf{AIS_TIM_Disable}_{[ho]} \\
 &\text{or } \mathbf{InsertAIS}_{[ho]}
 \end{aligned}$$

The High Order VC-3/STS-1 POH Monitor will insert RDI per high order path towards the RX high order path Alarm Indication Port according to the following expressions:

$$\begin{aligned}
 \mathbf{aRDI-S}_{[ho]} &= \mathbf{dSSF}_{[ho]} \text{ and not } \mathbf{RDI_SSF_Disable} \\
 &\text{or } \mathbf{InsertAIS}_{[ho]}
 \end{aligned}$$

$$\begin{aligned}
 \mathbf{aRDI-C}_{[ho]} &= \mathbf{dUNEQ}_{[ho]} \text{ and not } \mathbf{RDI_UNEQ_Disable} \\
 &\text{or } \mathbf{dTIM}_{[ho]} \text{ and not } \mathbf{RDI_TIM_Disable}
 \end{aligned}$$

$$\begin{aligned}
 \mathbf{aRDI}_{[ho]} &= \mathbf{aRDI-S}_{[ho]} \\
 &\text{or } \mathbf{aRDI-C}_{[ho]}
 \end{aligned}$$

$$\mathbf{aRDI-P}_{[ho]} = \mathbf{dPLM}_{[ho]} \text{ and not } \mathbf{RDI_PLM_Disable}$$

The High Order VC-3/STS-1 POH Monitor will forward the dPLM and dLOM indications to the subsequent adaptation blocks (low order pointer processors or virtual concatenation receiver blocks) depending on the configured SDH/SONET mapping:

$$\begin{aligned}
 \mathbf{aPLM}_{[ho]} &= \mathbf{dPLM}_{[ho]} \text{ and not } \mathbf{PLM_PLM_Disable} \\
 \mathbf{aLOM}_{[ho]} &= \mathbf{dLOM}_{[ho]} \text{ and not } \mathbf{LOM_LOM_Disable}
 \end{aligned}$$

RX TU3 PTR (TU-3 Pointer Tracker):

- [tu3] ranges from 0 to 2 (3 high order channels)

The TU-3 pointer tracker will insert AIS per TU-3 towards the high order VC-3 POH monitors according to the following expression:

aAIS_[tu3] = dAIS_[tu3] and not InsertAIS_On_AIS_Disable
or dLOP_[tu3] and not InsertAIS_On_LOP_Disable
or dPLM and not InsertAIS_On_PLM_Disable (from High Order VC-4 POH Monitor)

LODMP Ptr (Low Order Pointer Tracker):

- [lo] ranges from 0 to 83 (84 low order channels)

The low order pointer tracker will insert AIS per low order path towards the low order POH monitors according to the following expression:

aAIS_[lo] = dAIS_[lo]
or dLOP_[lo]
or dPLM (from High Order POH Monitor)
or dLOM (from High Order POH Monitor)

LODMP_POHMONITOR (Low Order POH Monitor):

- [lo] ranges from 0 to 83 (84 low order channels)

The Low Order POH Monitor will insert AIS per low order path according to the following expression:

$$\begin{aligned}
 \mathbf{aAIS}_{[lo]} &= \mathbf{dAIS}_{[lo]} \text{ and not } \mathbf{AIS_IncAIS_Disable} \\
 &\text{or } \mathbf{dSSF}_{[lo]} \text{ and not } \mathbf{AIS_SSF_Disable} \\
 &\text{or } \mathbf{dUNEQ}_{[lo]} \text{ and not } \mathbf{AIS_UNEQ_Disable} \\
 &\text{or } \mathbf{dTIM}_{[lo]} \text{ and not } \mathbf{AIS_TIM_Disable} \\
 &\text{or } \mathbf{InsertAIS}_{[lo]}
 \end{aligned}$$

The Low Order POH Monitor will insert RDI per low order path towards the RX low order path Alarm Indication Port according to the following expressions:

$$\begin{aligned}
 \mathbf{aRDI-S}_{[lo]} &= \mathbf{dSSF}_{[lo]} \text{ and not } \mathbf{RDI_SSF_Disable} \\
 &\text{or } \mathbf{InsertAIS}_{[lo]}
 \end{aligned}$$

$$\begin{aligned}
 \mathbf{aRDI-C}_{[lo]} &= \mathbf{dUNEQ}_{[lo]} \text{ and not } \mathbf{RDI_UNEQ_Disable} \\
 &\text{or } \mathbf{dTIM}_{[lo]} \text{ and not } \mathbf{RDI_TIM_Disable}
 \end{aligned}$$

$$\begin{aligned}
 \mathbf{aRDI}_{[lo]} &= \mathbf{aRDI-S}_{[lo]} \\
 &\text{or } \mathbf{aRDI-C}_{[lo]}
 \end{aligned}$$

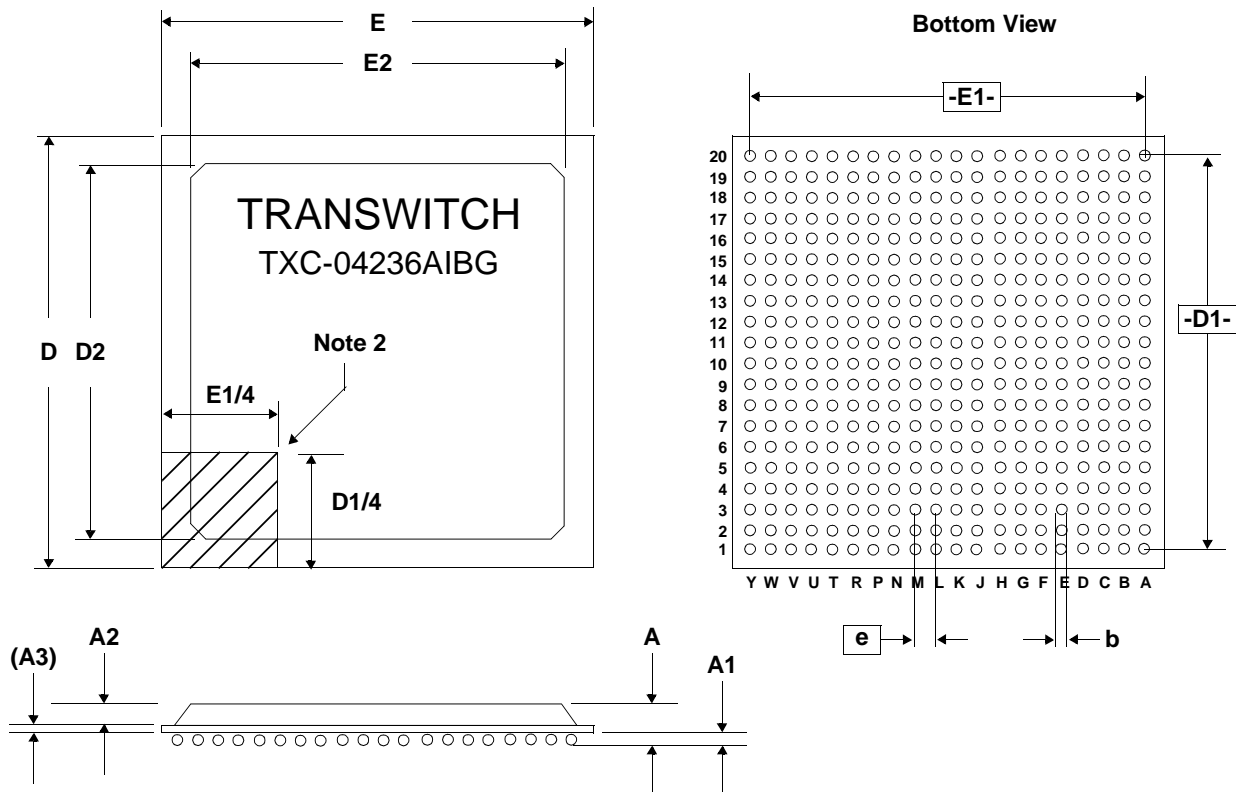
$$\mathbf{aRDI-P}_{[lo]} = \mathbf{dPLM}_{[lo]} \text{ and not } \mathbf{RDI_PLM_Disable}$$

The Low Order POH Monitor will forward the dPLM and dLOM indications to the subsequent adaptation blocks (virtual concatenation receiver blocks) depending on the configured SDH/SONET mapping:

$$\begin{aligned}
 \mathbf{aPLM}_{[lo]} &= \mathbf{dPLM}_{[lo]} \text{ and not } \mathbf{PLM_PLM_Disable} \\
 \mathbf{aLOM}_{[lo]} &= \mathbf{dLOM}_{[lo]} \text{ and not } \mathbf{LOM_LOM_Disable}
 \end{aligned}$$

PACKAGE INFORMATION

The EtherMap-3 Plus device is packaged in a 400-lead plastic ball grid array (PBGA) suitable for surface mounting, as illustrated in Figure 88.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.

| Dimension (Note 1) | Min | Max |
|--------------------|-------|-------|
| A (Nom.) | 2.33 | |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 (Nom.) | 0.56 | |
| b (Ref.) | 0.76 | |
| D | 27.00 | |
| D1 (Nom.) | 24.13 | |
| D2 | 24.95 | 25.70 |
| E | 27.00 | |
| E1 (Nom.) | 24.13 | |
| E2 | 24.95 | 25.70 |
| e (Ref.) | 1.27 | |

Figure 88. EtherMap-3 Plus TXC-04236 Package Diagram



ORDERING INFORMATION

Part Number: TXC-04236AIBG 400-lead plastic ball grid array package

RELATED PRODUCTS

TXC-03453, TL3M Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-04222, TEMx28 Device (28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-06103, PHAST-3N Device (SDH/SONET STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06212, PHAST-12E Device (Programmable, High-Performance ATM/Packet/Transmission SONET/SDH Terminator for Level 12). A highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher-order multiplexing, and transmission applications. This PHAST-12 device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06312, PHAST-12N Device (STM-4/OC-12 SDH/SONET Overhead Terminator with Telecom Bus Interface). The PHAST-12N is a highly integrated SDH/SONET overhead terminator device designed for TDM payload mappings. A single PHAST-12N can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line.

TXC-06603, POP-12 Device (OC-12 SONET/SDH Path Overhead Processor, Retimer, and Cross Connect). The POP-12 integrates VC-3/VC-4 POH processing, AU-3/AU-4 pointer processing retiming, and VC-3/VC-4 cross connect for four Telecom Bus interfaces into one package. It provides an interface to high density mapper applications when used with the TranSwitch PHAST-12E (TXC-06212), and mapper and framer devices. The POP-12 device is designed to provide a seamless interface to the PHAST-12E device.

TXC-06712, EtherPHAST-48 Device (OC-48 SONET/SDH Ethernet Mapper). The EtherPHAST-48 Device is a highly integrated, STS-48/STM-16 rate SONET/SDH device, for mapping of IEEE 802.3 100/1000 Mbps Ethernet and block encoded Fibre Channel, FICON, ESCON and DVB-ASI into SONET/SDH Transport.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications
Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor
Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org



IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

**Publication Services of International
Telecommunication Union
Telecommunication Standardization Sector**
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

**DODSSP Standardization Documents
Ordering Desk**
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

**TTC Standard Publishing Group of the
Telecommunication Technology Committee**
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated EtherMap-3 Plus TXC-04236 Data Sheet that have significant differences relative to the previous and now superseded EtherMap-3 Plus TXC-04236 Data Sheet.

Updated EtherMap-3 Plus TXC-04236 Data Sheet: *PRELIMINARY* Edition 3, July 2004

Previous EtherMap-3 Plus TXC-04236 Data Sheet: *PRELIMINARY* Edition 2, March 2004

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

| <u>Page Number of Updated Data Sheet</u> | <u>Summary of the Change</u> |
|--|---|
| All | Changed edition number and date. |
| 2 - 14 | Updated Table of Contents, List of Figures and List of Tables. |
| 19 | Changed Data Processing/Flow section. |
| 22 | Changed 10/100/1000 Mbit/s Ethernet Media Access Controller (MAC) Block section. |
| 23 | Added SONET/SDH Mapping section. Changed Mapper Block section. |
| 25 | Changed Demapper Block section. |
| 47 | Changed Conditions column for Parameter Moisture Exposure Level in the Absolute Maximum Ratings and Environmental Limitations (Referenced to VSS) table. Changed Note 3 below the table. |
| 48 | Changed Note 1 below the table. |
| 55, 57 | Changed Max value for Symbol $t_{D(3)}$. |
| 58 | Changed the diagram of Figure 10 . |
| 59 | Changed the diagram of Figure 11 . |
| 86 | Modified for Symbol $t_{D(4)}$ in Figure 35 . |
| 116 | Changed sixth and sixteenth bullets. |
| 119 | Changed sixth and sixteenth bullets. Changed Configuration for Virtual concatenation and LCAS section. |
| 124 | Changed sentence "The value 0x0300 represents...". Changed heading to VCG Tributary Assignments (Adding and Removing Members) and made changes to this section. Added title Dynamic Mapping and Virtual Concatenation Changes . |
| 131 | Changed heading to Ethernet Support and added sub-heading SMII and GMII Interfaces . |
| 133 | Changed last two bulleted sections of Ethernet MAC Blocks section. |
| 134 | Added Ethernet Frame Size section. |
| 136 | Changed Flow Control Operation section. |
| 139 | Added heading Setting the Encapsulation Mode . Added heading Changing the Encapsulation Mode and changed the content of this section. |
| 186 | Changed Microprocessor Controlled Hardware Reset section. |
| 200 | Changed Descriptions for Symbols RESETH, TX_RESETSx, RX_RESETSx and cCROV in Table 10 . Changed Description for Symbol VersionMask in Table 12 . |
| 206 | Changed Bit 3 of register 0x0003c to Reserved in Table 16 . |

| <u>Page Number of Updated Data Sheet</u> | <u>Summary of the Change</u> |
|---|--|
| 210 | Changed Descriptions for Symbols Synchronized Enable and Synchronized Received Enable in Table 18 . |
| 215 | Changed Description for Symbol Read Cycle in Table 25 . |
| 216 | Changed Description for Symbol MII Mgmt Control in Table 27 . |
| 217 | Changed Descriptions for Symbols rHWPT_x, rLWPT_x and rHISPSE_x in Table 30 . |
| 247 | Added Note at the top of Table 56 . |
| 249 | Changed Description for Symbol aRGFPFECsFx in Table 56 . |
| 270 | Changed Descriptions for Symbols cTHOVC3_3, cTHOVC3_2 and cTHOVC3_1 in Table 65 . |
| 283 | Changed Descriptions for Symbols cRHOVC3_3, cRHOVC3_2 and cRHOVC3_1 in Table 76 . |
| 285 | Changed Description for Symbol aLOSQM_x in Table 77 . |
| 286 | Changed Descriptions for Symbols aLOLOA_x and aLOLOA_AIIvT_x in Table 77 . |
| 293 | Changed Descriptions for Symbols sRLOPOOL_x, sRLOVCG_x, sRLOCTRL_x, sRLOSQ_x, sRHOSQ_x, sRHOPOOL_x, sRHOVCG_x and sRHOCtrl_x in Table 83 . |
| 295 | Changed Description for Symbol cTFCMODEx in Table 86 . |
| 299 | Changed Description for Symbol cTRSTRAM in Table 98 . Changed Description for Symbol aTXFIFOx in Table 99 . |
| 300 | Changed Description for Symbol L1aPTRRAMERRx in Table 101 . |
| 303 | Changed Table 112 heading. Changed Description for Symbol AuMode in Table 112 . |
| 310 | Added note at bottom of Table 137 . |
| 323 | Added note at bottom of Table 186 . |
| 364 | Modified fifth paragraph under Scheme A - Counters with Roll-Over/Saturation Option . |
| 370 | Changed the diagram of Figure 68 . |
| 398 | Added List of Data Sheet Changes section. |

- NOTES -

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- NOTES -

