QT1M Device
Quad T1 Mapper
TXC-04251

DATA SHEET

FEATURES

- Add/drop four 1.544 Mbit/s signals from an STS-1, an STS-3/AU-3, or an STM-1 VC-4
- Independent add and drop bus timing modes
- Selectable AMI or B8ZS positive/negative rail or NRZ T1 interface. Performance counter provided for coding violations
- Digital desynchronizer reduces systemic jitter in the presence of multiple pointer movements. A register is also provided to control the internal FIFO leak rate
- Drop buses are monitored for parity, loss of clock, upstream AIS and H4 multiframe errors
- Performance counters are provided for VT/TU pointer movements, BIP-2 errors and Far End Block Errors (FEBEs)
- VT/TUs are monitored for Loss Of Pointer, New Data Flags (NDFs), AIS, Remote Defect Indication (RDI), and size errors (S-bits)
- V5 Byte Signal Label Mismatch and Unequipped detection
- T1 facility and line loopbacks, generation of BIP-2 and FEBE errors, and send RDI capability
- Multiplexed microprocessor bus interface with interrupt capability
- IEEE 1149.1 standard boundary scan
- 160-pin plastic quad flat package

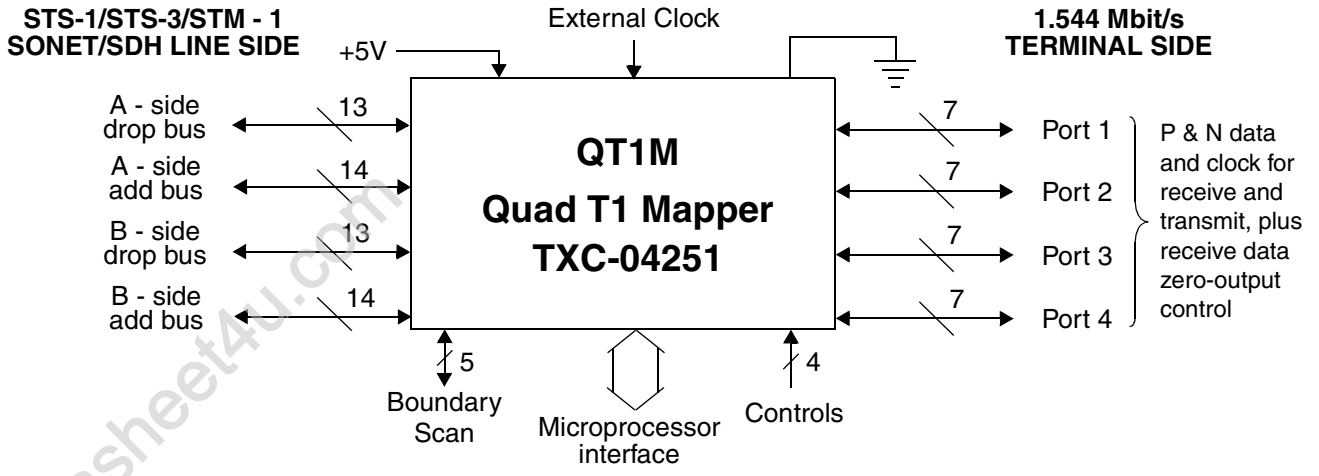
DESCRIPTION

The Quad T1 Mapper device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Four T1 1.544 Mbit/s signals are mapped to and from asynchronous 1.5 Virtual Tributaries (VT1.5s) or Tributary Unit-11s (TU-11s). The QT1M interfaces to a multiple-segment, byte-parallel SONET/SDH-formatted bus at the 19.44 Mbit/s byte rate for STS-3/STM-1 operation or at the 6.48 Mbit/s byte rate for STS-1 operation. The T1 1.544 Mbit/s signals can be either AMI/B8ZS positive/negative rail- or NRZ-formatted signals. The QT1M provides performance counters, alarm detection, and the ability to generate errors and Alarm Indication Signals (AIS). T1 facility and line loopback capabilities are also provided.

The bus interface can connect to other TranSwitch devices, such as the STM-1/STS-3/STS-3c Overhead Terminator (SOT-3), TXC-03003B, to form an STS-3/STM-1 add/drop or terminal system.

APPLICATIONS

- STS-1/STS-3/STM-1 to 1.544 Mbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STS-1/STS-3/STM-1 termination terminal mode multiplexer
- STS-1/STS-3/STM-1 test equipment



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LIST OF FIGURES

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BLOCK DIAGRAM

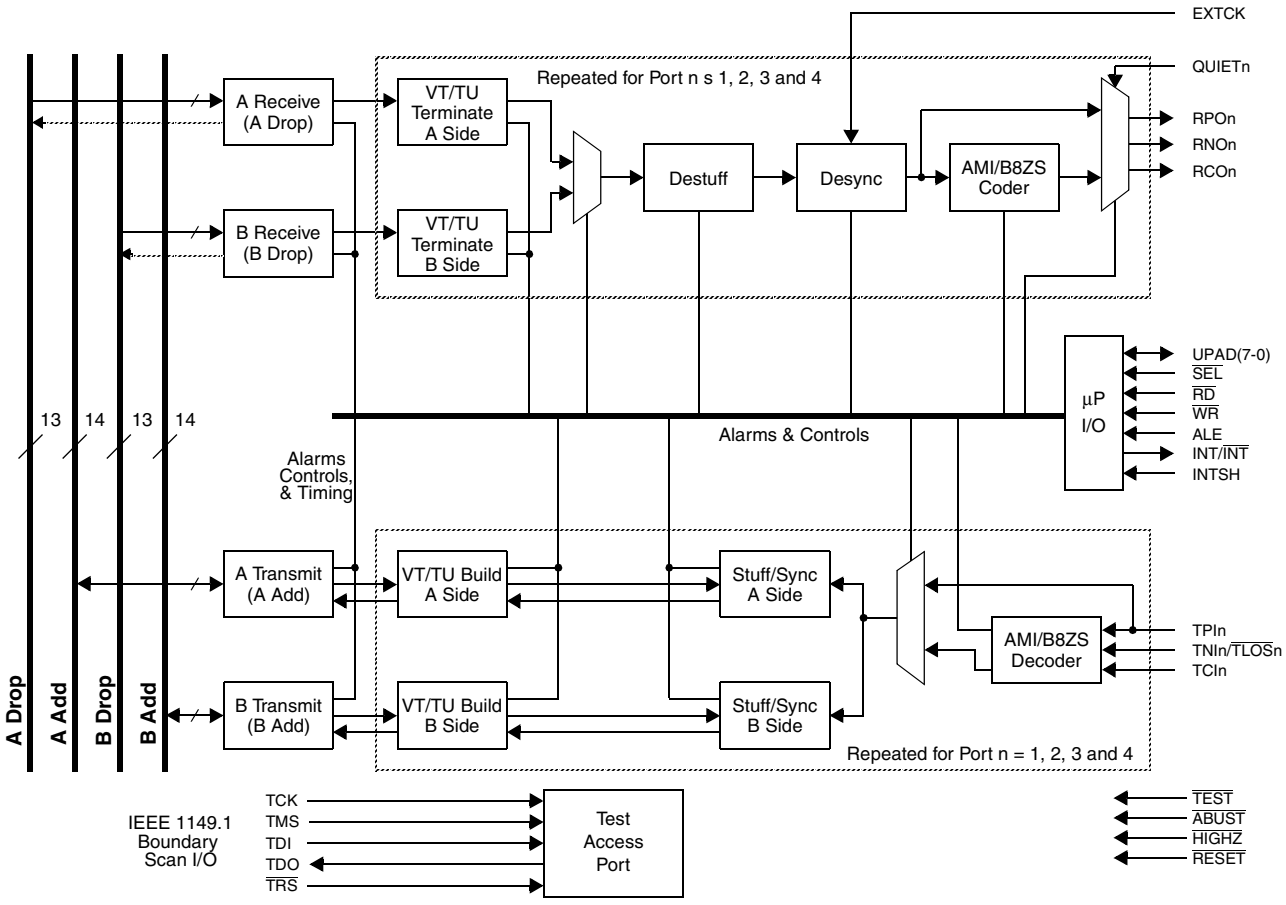


Figure 1. QT1M TXC-04251 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram for the Quad T1 Mapper is shown in Figure 1. The Quad T1 Mapper interfaces to four buses, designated as A Drop, B Drop, A Add, and B Add. The four buses run at the STS-3/STM-1 rate of 19.44 Mbyte/s, or at the STS-1 rate of 6.48 Mbyte/s. For North American applications, the asynchronous T1 signals are carried in floating Virtual Tributary 1.5s (VT1.5s) in a Synchronous Transport Signal -1 (STS-1), or in STS-1s that are carried in a Synchronous Transport Signal - 3 (STS-3). For ITU applications, the T1 signals are carried in floating mode Tributary Unit -11s (TU-11s) in the STM-1 Virtual Container -4 structure (VC-4) using Tributary Unit Group -3 (TUG-3), or in the STM-1 Virtual Container -3 structure (VC-3) using Tributary Unit Group -2 (TUG-2) mapping schemes. Four T1 signals can be dropped from one bus (A Drop or B Drop), or from both of the drop buses, to the T1 lines. Four asynchronous T1 signals are formatted into VT1.5s or TUs and are added to either of the add buses, or both, depending upon the mode of operation. When the Quad T1 Mapper is configured for drop bus timing, the add buses are, by definition, byte- and multiframe-synchronous with their like-named drop buses, but are delayed by one byte time because of internal processing. For example, if a byte in the STM-1 Virtual Container -4 structure (VC-4) using Tributary Unit Group -3 (TUG-3), VT1.5/TU-11 is to be added to the A Add bus, the time of its placement on the bus is derived from the A Drop

bus timing, and from software instructions specifying which VT/TU number is being dropped/added. When the device is configured for add bus timing, the add bus, parity, and add indicator signals are derived from the add clock, C1J1V1 and SPE signals.

The A Receive block is identical to the B Receive block. The VT/TU Terminate block is repeated 8 times, two for each port (A and B sides). The Destuff, Desync, and AMI/B8ZS Coder Blocks are repeated four times, one for each port. The interface between a drop bus and Receive block consists of 12 input leads (pins), and an optional output lead: a byte clock, byte-wide data, a C1J1 indicator which may be carrying a V1 indication making the signal a C1J1V1 indicator, an SPE indicator, and an odd parity bit for the last-named three signals. Parity is selectable by control bits for even parity and for the data byte only. The output lead is an optional VT/TU select indicator signal. The Drop C1J1V1 signal is used in conjunction with the Drop SPE signal to determine the location of the various pulses. The C1 pulse identifies the location of the C1 byte when the SPE signal is low. A single J1 pulse identifies the starting location of the J1 byte in the VC-4 format, when the SPE signal is high. Three J1 pulses are provided for the STS-3 format, each identifying the starting location of the J1 byte in each of the STS-1 signals.

The Quad T1 Mapper can operate with a V1 pulse in the C1J1V1 signal, or it can use an internal H4 detector for determining the location of the V1 pulse. The V1 pulse location is used to determine the location of the pointer byte V1. For STM-1 VC-4 operation, if the C1J1V1 signal is used, a single V1 pulse must occur three drop bus clock cycles every four frames following the J1 pulse. For STS-3 operation, three V1 pulses must be present every four frames. Each of the three V1 pulses must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte location is six clock cycles after the V1 pulse.

For STS-1 operation, one V1 must be present if the C1J1V1 signal is used. The V1 pulse must occur on the next clock cycle after J1, and when the SPE signal is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the STS-1) in the POH bytes. In the next column (first clock cycle) the VTs start. Thus, the V1 pulse identifies the starting location of the first V1 byte in the signal. The rest of the V1 bytes for the 21 VT1.5/TU-11s are aligned regarding their starting point with respect to the V1 pulse.

Each bus is monitored for parity errors, loss of clock, H4 multiframe alignment if selected, and an upstream SONET/SDH AIS indication. The Quad T1 Mapper can monitor either the TOH E1 bytes or the H1/H2 bytes for an AIS indication. Which E1 byte and H1/H2 bytes are selected is a function of the VT/TU selected.

Each VT/TU Terminate block (A and B side) performs pointer processing based on the location of the V1 and V2 bytes. The pointer bytes are monitored for loss of pointer, VT AIS indication, and NDF. The pointer tracking process is based on the latest ETSI standard, which also meets ANSI/Bellcore requirements. Pointer increments and decrements are also counted, and the SS-bits are monitored for the correct value. This block also monitors the various alarms found in the V5 and Z7 bytes, including signal label mismatch detection, unequipped status detection, BIP-2 parity error detection and error counter, FEBE counter, and the RDI indications.

A control bit for each port selects the VT/TU from either the A Drop or B Drop bus. The VT/TU is destuffed in the Destuff block using majority logic rules for the three sets of three justification control bits to determine if the two S-bits are data bits or frequency justification bits.

The Desync block removes the effects on the T1 output of systemic jitter that might occur because of signal mappings and pointer movements in the network. The Desync block contains two parts, a pointer leak buffer, and a T1 loop buffer. The pointer leak buffer can accept up to five consecutive pointer movements, and can adjust the effect over time. The T1 Loop Buffer consists of a digital loop filter, which is designed to track the frequency of the received T1 signal and to remove both transmission and stuffing jitter.

An option for each port provides either NRZ data and clock, or an AMI- or B8ZS-encoded positive and negative rail signal for the T1 interface. Transmit data (towards the T1 line), for all four channels, can be clocked out on either rising or falling edges of the clock. In addition, control bits are provided for forcing the data and clock signals to a high impedance state. A control lead is provided for forcing the output leads to the 0 state.

In the add direction, the Quad T1 Mapper accepts clock and either NRZ data or AMI - or B8ZS-encoded positive and negative rail signals. Data, for all four channels, can be clocked in on either a negative or rising edge of the clock. In the NRZ mode, an external loss of clock indication input signal can be provided. For the rail signal, coding violations are counted, and the signal monitored for loss of signal. A T1AIS detector is also provided.

The data signal is written into a FIFO in one of the eight Stuff/Sync Blocks. Threshold modulation is used for the frequency justification process. Timing information from the drop bus or add bus is used to read the FIFO and perform the VT/TU justification process. This block permits the tracking of the incoming T1 signal having an average frequency offset as high as 120 ppm, and up to 5 UI of peak-to-peak jitter. Since the Quad T1 Mapper supports a ring architecture, two sets of blocks are provided for each port. The VT/TU selection is the same for both blocks. A control bit, and transmit line alarms, can generate a T1AIS.

The eight VT/TU Blocks format the VT/TU into a STS-1, STS-3 or STM-1 structure for the asynchronous 1544 kbit/s signals, as shown in Figure 2. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 78. Transmit access is provided for the 8 overhead communications channel bits (O-bits) via the microprocessor. The microprocessor also writes the signal label, and the values of the J2, Z6, and Z7 bytes. The Far End Block Error (FEBE) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated. Control bits are provided for generating unequipped status, generating VT/TU AIS, and inserting FEBE and BIP-2 errors. The ability to generate Null Pointer Indicators (NPIs) is also provided for the STM-1 VC-4 format.

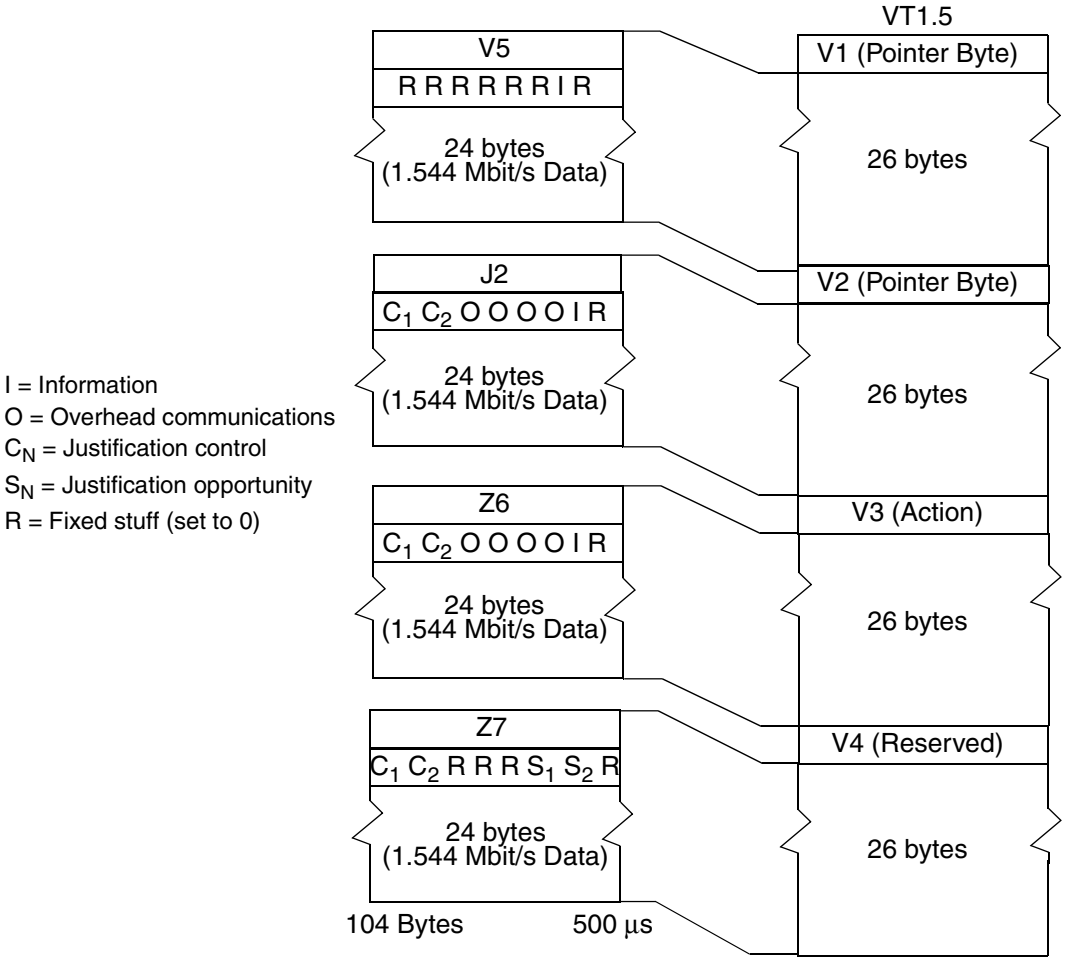
The A Transmit block is identical to the B Transmit block. The interface between an add bus and a Transmit block consists of three input pins and eleven output pins, when the add bus timing mode is selected. The input pins are a byte clock, a C1J1V1 indicator, and an SPE indicator. The output pins are byte-wide data, a parity indicator, an add indicator, and an optional VT/TU selection indicator signal. The Add C1J1V1 signal is used in conjunction with the Add SPE signal to determine the location of the various pulses. An option is provided in which the drop side V1 reference pulse, either from the drop bus C1J1V1 indicator or from the H4 multiframe detector, may be used as the add side V1 reference pulse.

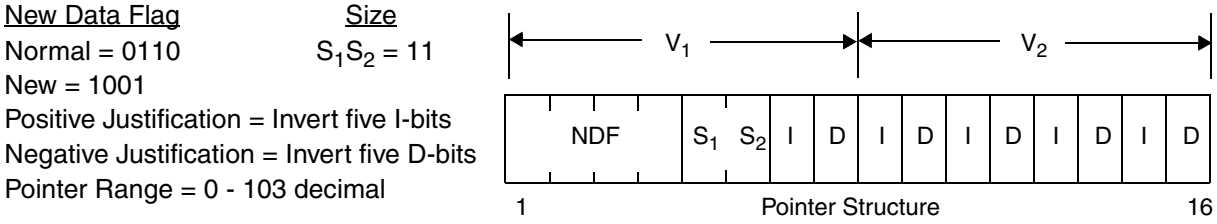
When drop bus timing is selected, the output pins are byte-wide data, a parity indicator, an add indicator, and an optional VT/TU selection indicator signal. The add bus clock, SPE and C1J1V1 signals are disabled.

The microprocessor interface consists of a multiplexed address/data bus. Interrupt capability is also provided. The alarms that cause the interrupt can be set on positive, negative, or positive or negative transitions, and on positive levels. Interrupt mask bits are provided for register byte locations, and some defined bits.

Control bits are provided which enable a T1 facility or line loopback. Because of the complexity of the SONET/SDH interface and the two timing modes, SONET/SDH loopback of the VT/TUs is not supported.

The Boundary Scan Interface block provide a five-pin Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external I/O pins from the TAP for board and component test.





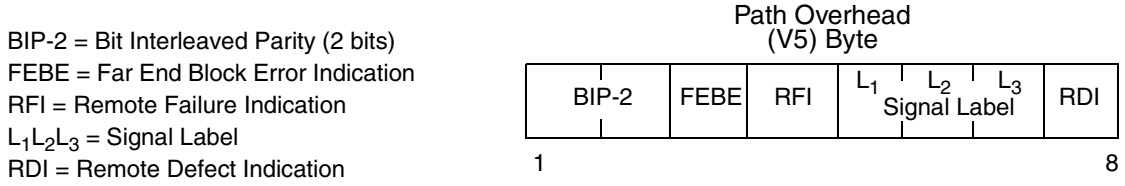


Figure 2. 1544 kbit/s Mapping

PIN DIAGRAM

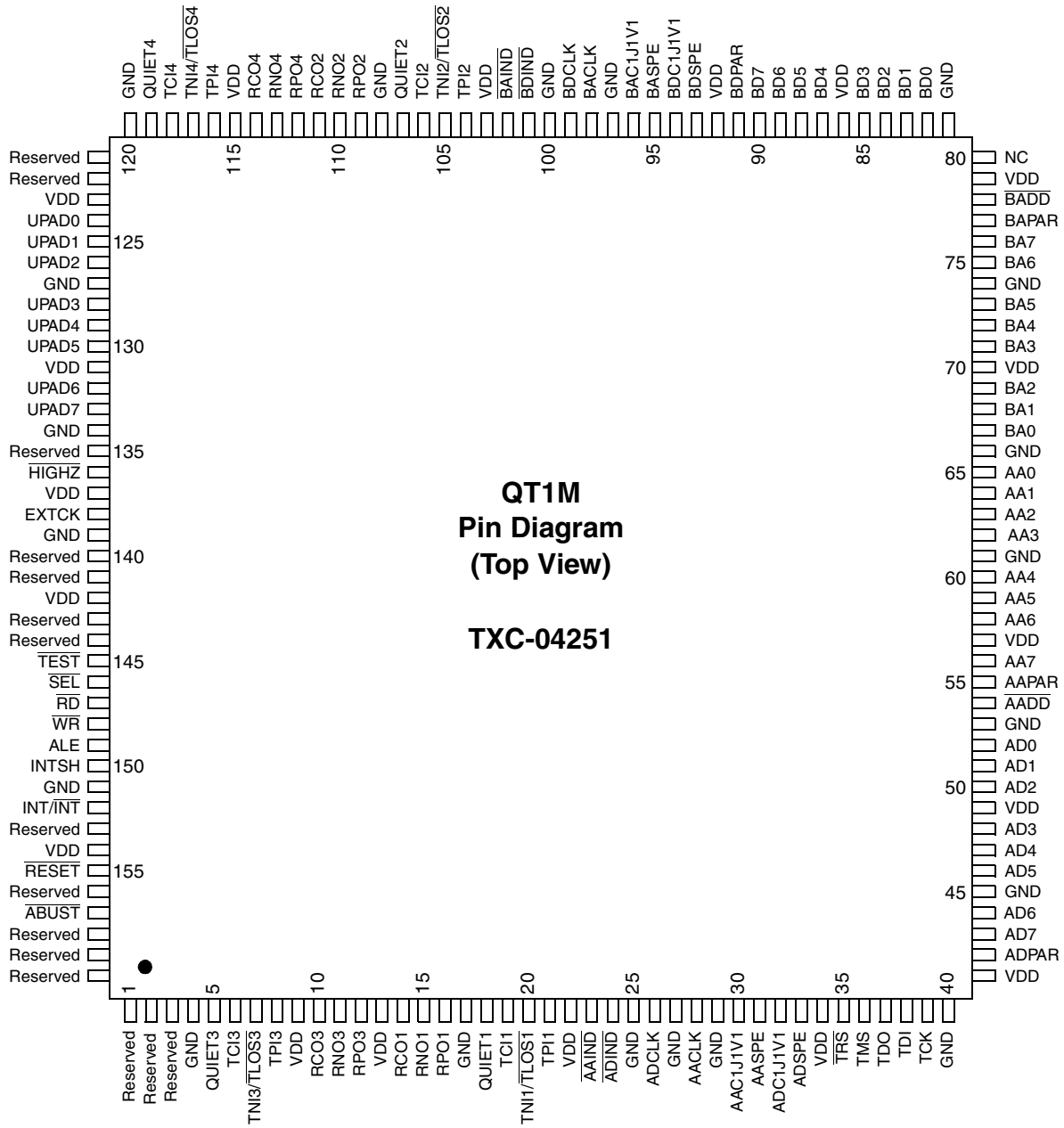


Figure 3. QT1M TXC-04251 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY, GROUND, NO CONNECT AND RESERVED

Symbol	Pin No.	I/O/P *	Type	Name/Function
VDD	9, 13, 22, 34, 41, 49, 57, 70, 79, 86, 92, 103, 115, 123, 131, 137, 142, 154	P		**VDD:** +5 volt supply voltage, ±5%.
GND	4, 17, 25, 27, 29, 40, 45, 53, 61, 66, 74, 81, 97, 100, 108, 120, 127, 134, 139, 151	P		**Ground:** 0 volt reference.
NC	80			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. NC pins may be used for manufacturing test purposes, and/or may be assigned to functions in future versions of the device. Connection of these pins may impair performance or even cause damage to the device, and could prevent the substitution of future device versions in the application.
Reserved	1, 2, 3, 121, 122 135, 140, 141 143, 144, 153 156, 158 - 160			**Reserved:** Reserved pins permit the connection of leads for input/output signals which are not used/provided by the QT1M device. Such signals may be used/provided by other pin-compatible devices that could be substituted in QT1M applications, particularly future versions of the QT1M device which have additional features requiring the use of these pins.

* I = Input; O = Output; P = Power; T = Tristate

A DROP AND A ADD BUS I/O

Symbol	Pin No.	I/O/P	Type *	Name/Function
ADCLK	26	I	TTLs	**A Drop Bus Clock:** This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. A Drop bus byte-wide data (AD7-AD0), the parity bit (ADPAR), SPE indication (ADSPE), and the C1J1V1 indication (ADC1J1) are clocked in on falling edges of this clock. This clock may also be used for timing and deriving the like-named add bus byte-wide data, add and VT/TU indications, and parity bits. The add bus signals are clocked out on rising edges of the clock during the time slots that correspond to the selected VT/TU.
ADPAR	42	I	TTL	**A Drop Bus Parity Bit:** An odd parity bit input signal representing the parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus. Control bits are provided which enable even parity to be calculated (control bit DPE is 1), and for the data byte only (control bit PDDO is 1).

* See Input, Output and Input/Output Parameters section for Type definitions.

Symbol	Pin No.	I/O/P	Type *	Name/Function
AD(7-0)	43, 44, 46, 47, 48, 50, 51, 52	I	TTL	**A Drop Bus Data Byte:** Byte-wide data that corresponds to the STS-3/STM-1/STS-1 signal from the drop bus. The first bit received (dropped) corresponds to bit 7.
ADSPE	33	I	TTL	**A Drop Bus SPE Indicator:** A signal that is active high during each byte of the STS-3/STM-1/STS-1 payload, and low during Transport Overhead times.
ADC1J1V1	32	I	TTL	**A Drop Bus C1J1V1 Indications:** An active high timing signal that carries STS-3/STM-1/STS-1 starting frame and SPE information. This signal works in conjunction with the ADSPE signal. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal, and the C1 byte in the STS-1 signal, when ADSPE is low. The J1 signal identifies the starting location of the J1 signal when ADSPE is high. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{ADIND}}$	24	O	CMOS 4mA	**A Drop Bus VT/TU Selection Indication:** Enabled when control bit ADnEN is written with a 1. An active low signal that is clocked out for the time slots determined by VT/TU selection (VTNn register) for each port.
AACLK	28	I	TTLs	**A Add Bus Clock:** When the add bus timing mode is selected, this input must be provided for add bus timing. This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication (AASPE), and the C1J1V1 indication (AAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (AA7-AA0), add indicator ($\overline{\text{AADD}}$), and parity bit (AAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected VT/TU. When drop bus timing is selected, this input is disabled.
AAPAR	55	O(T)	CMOS 4mA	**A Add Bus Parity Bit:** An odd parity output signal that is calculated over the byte-wide add data. This tristate pin is only active when there is data being added to the add bus. When control bit APE is 1 even parity is calculated.
AA(7-0)	56, 58, 59, 60, 62, 63, 64, 65	O(T)	CMOS 4mA	**A Add Bus Data Byte:** Byte-wide data that corresponds to the selected VT/TU.
AASPE	31	I	TTL	**A Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STS-3/STM-1/STS-1 payload, and low during Transport Overhead byte times.

Symbol	Pin No.	I/O/P	Type *	Name/Function
AAC1J1V1	30	I	TTL	**A Add Bus C1J1V1 Indications:** When the add bus timing mode is selected, this signal must be provided for add bus timing. An active high timing signal that carries STS-3/STM-1/STS-1 starting frame and SPE information. This signal works in conjunction with the AASPE signal. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal, and the C1 byte in the STS-1 signal, when AASPE is low. The J1 signal identifies the starting location of the J1 signal when AASPE is high. The J1 signal identifies the location of the J1 byte. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{AAIND}}$	23	O	CMOS 4mA	**A Add Bus VT/TU Selection Indication:** Enabled when control bit AAnEN is written with a 1. An active low signal that is clocked out for the time slots determined by VT/TU selection (VTNn register) for each port.
$\overline{\text{AADD}}$	54	O	CMOS 4mA	**A Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the A Add bus is valid. It identifies the location of all of the VT/TU time slots being selected. When control bit ADDI is 1, the indicator is active high instead of low.

B DROP AND B ADD BUS I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
BDCLK	99	I	TTLs	**B Drop Bus Clock:** This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. B Drop bus byte-wide data (BD7-BD0), the parity bit (BDPAR), SPE indication (BDSPE), and the C1J1V1 indication (BDC1J1) are clocked in on falling edges of this clock. This clock may also be used for timing and deriving the like-named add bus byte-wide data, add and VT/TU indications, and parity bits. The add bus signals are clocked out on rising edges of the clock during the time slots that correspond to the selected VT/TU.
BDPAR	91	I	TTL	**B Drop Bus Parity Bit:** An odd parity bit input signal representing the parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus. Control bits are provided which enable even parity to be calculated (control bit DPE is 1), and for the data byte only (control bit PDDO is 1).
BD(7-0)	90, 89, 88, 87, 85, 84, 83, 82	I	TTL	**B Drop Bus Data Byte:** Byte-wide data that corresponds to the STS-3/STM-1/STS-1 signal from the drop bus. The first bit received (dropped) corresponds to bit 7.

Symbol	Pin No.	I/O/P	Type	Name/Function
BDSPE	93	I	TTL	**B Drop Bus SPE Indicator:** A signal that is active high during each byte of the STS-3/STM-1/STS-1 payload, and low during Transport Overhead times.
BDC1J1V1	94	I	TTL	**B Drop Bus C1J1V1 Indications:** An active high timing signal that carries STS-3/STM-1/STS-1 starting frame and SPE information. This signal works in conjunction with the BDSPE signal. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal, and the C1 byte in the STS-1 signal, when BDSPE is low. The J1 signal identifies the starting location of the J1 signal when BDSPE is high. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{BDIND}}$	101	O	CMOS 4mA	**B Drop Bus VT/TU Selection Indication:** Enabled when control bit BDnEN is written with a 1. An active low signal that is clocked out for the time slots determined by VT/TU selection (VTNn register) for each port.
BACLK	98	I	TTLs	**B Add Bus Clock:** When the add bus timing mode is selected, this input must be provided for add bus timing. This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication (BASPE), and the C1J1V1 indication (BAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (BA7-BA0), add indicator ($\overline{\text{BADD}}$), and parity bit (BAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected VT/TU. When drop bus timing is selected, this input is disabled.
BAPAR	77	O(T)	CMOS 4mA	**B Add Bus Parity Bit:** An odd parity output signal that is calculated over the byte-wide add data. This tristate pin is only active when there is data being added to the add bus. When control bit APE is 1, even parity is calculated.
BA(7-0)	76, 75, 73, 72, 71, 69, 68, 67	O(T)	CMOS 4mA	**B Add Bus Data Byte:** Byte-wide data that corresponds to the selected VT/TU.
BASPE	95	I	TTL	**B Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STS-3/STM-1/STS-1 payload, and low during Transport Overhead byte times.

Symbol	Pin No.	I/O/P	Type	Name/Function
BAC1J1V1	96	I	TTL	**B Add Bus C1J1V1 Indications:** When the add bus timing mode is selected, this signal must be provided for add bus timing. An active high timing signal that carries STS-3/STM-1/STS-1 starting frame and SPE information. This signal works in conjunction with the BASPE signal. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal, and the C1 byte in the STS-1 signal, when BASPE is low. The J1 signal identifies the starting location of the J1 signal when BASPE is high. The J1 signal identifies the location of the J1 byte. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{BAIND}}$	102	O	CMOS 4mA	**B Add Bus VT/TU Selection Indication:** Enabled when control bit BAnEN is written with a 1. An active low signal that is clocked out for the time slots determined by VT/TU selection (VTNn register) for each port.
$\overline{\text{BADD}}$	78	O	CMOS 4mA	**B Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the B Add bus is valid. It identifies the location of all of the VT/TU time slots being selected. When control bit ADDI is 1, the indicator is active high instead of low**.**

PORT n LINE INTERFACE (n = 1, 2, 3 or 4)

Symbol	Pin No.	I/O/P	Type	Name/Function
RCOn (n=1-4)	14, 111, 10, 114	O(T)	CMOS 4mA	**Receive Port n Output Clock:** A 1.544 MHz clock output. Data is normally clocked out on rising edges of this clock. When control bit RCKI is 1, data is clocked out on falling edges of this clock. When control bit RnEN is 0, this pin is forced to a high impedance state.
RPOn (n=1-4)	16, 109, 12, 112	O(T)	CMOS 4mA	**Receive Port n Data Positive Rail or NRZ:** When control bit BYPASn is 0, positive rail data is provided on this lead. When control bit BYPASn is 1, an NRZ signal is provided on this pin. When control bit RnEN is 0, this pin is forced to a high impedance state.
RNOn (n=1-4)	15, 110, 11, 113	O(T)	CMOS 4mA	**Receive Port n Data Negative Rail:** When control bit BYPASn is 0, negative rail data is provided on this pin. When control bit RnEN is 0, or control bit BYPASn is 1, this pin is forced to a high impedance state.
TCIn (n=1-4)	19, 106, 6, 118	I	TTLs	**Transmit Port n Input Clock:** A 1.544 MHz clock input. Data is normally clocked in on falling edges of this clock. When control bit TCKI is 1, data is clocked in on the rising edges of this clock.
TPIn (n=1-4)	21, 104, 8, 116	I	TTL	**Transmit Port n Data Positive Rail or NRZ:** When control bit BYPASn is 0, positive rail input data is provided on this pin. When control bit BYPASn is 1, an NRZ signal is provided on this pin.

Symbol	Pin No.	I/O/P	Type	Name/Function
TNIn/ $\overline{\text{TLOSn}}$ (n=1-4)	20, 105, 7, 117	I	TTL	**Transmit Port n Data Negative Rail/External Loss Of Signal:** When control bit BYPASn is 0, negative rail input data is provided on this pin. When control bit BYPASn is 1, this pin may be used to input an active low external loss of signal indicator from the line interface device.
QUIETn (n=1-4)	18, 107, 5, 119	I	TTL	**Quiet Port n:** A high forces the RPOn and RNOn pins to the 0 state for either a rail or NRZ interface, overriding control bit RnEN. A low allows the state of the RPOn and RNOn pins to be controlled by RnEN.

MICROPROCESSOR BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
UPAD(7-0)	133, 132, 130, 129, 128, 126, 125, 124	I/O	TTL 8mA	**Address/Data Bus:** These pins constitute the time-multiplexed address and data bus for accessing the registers which reside in the memory map of the Quad T1 Mapper. UPAD7 is the most significant bit. High is logic 1.
$\overline{\text{SEL}}$	146	I	TTLs	**Select:** A low signal generated by the microprocessor for accessing the memory map registers for control, status, and alarm information.
$\overline{\text{RD}}$	147	I	TTLs	**Read:** A low signal generated by the microprocessor for reading the registers which reside in the memory map. The memory map is selected by placing a low on the select pin.
$\overline{\text{WR}}$	148	I	TTLs	**Write:** A low signal generated by the microprocessor for writing to the registers which reside in the memory map. The memory map is selected by placing a low on the select pin.
ALE	149	I	TTLs	**Address Latch Enable:** An active high signal generated by the microprocessor for holding an address stable during a read/write cycle.
INT/$\overline{\text{INT}}$	152	O(T)	TTL 8mA	**Interrupt:** A high or low on this output pin signals an interrupt request to the microprocessor. The polarity of this signal is determined by the state of the INTSH pin.
INTSH	150	I	TTL	**Interrupt Sense High Selection:** A high on this pin causes the interrupt sense to be high when an interrupt occurs. A low causes the interrupt sense to be low when an interrupt occurs.

CONTROLS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{TEST}}$	145	I	TTLs	**TranSwitch Test Bit:** A high must be placed on this pin.
EXTCK	138	I	CMOS	**External Reference Clock:** This clock is used for desynchronizer operation and other purposes. The clock frequency must be 48.6360 MHz (+/- 32 ppm over life) and the clock duty cycle must be 50 +/- 10%.
$\overline{\text{RESET}}$	155	I	TTLs	**Hardware Reset:** When an active low pulse is applied to this pin for a minimum of 150 nanoseconds after power is applied, this pulse clears all performance counters and alarms, resets the control bits (except those bits that force a high impedance state for the add buses), and initializes the internal FIFOs. The microprocessor must write the control bit states for normal operation**.**
$\overline{\text{HIGHZ}}$	136	I	TTLs	**High Impedance Select:** A low forces all output pins to the high impedance state for testing purposes**.**
$\overline{\text{ABUST}}$	157	I	TTLs	**Add Bus Timing Select:** An active low selects the A and B Add bus clock, SPE and C1J1V1 input signals for deriving timing for the A and B Add buses. An active high selects the like-named drop bus for deriving timing (e.g., A Drop bus for A Add bus). This control pin is disabled when a 1 is written to control bit SBTEN.

BOUNDARY SCAN INTERFACE SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	39	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock:** This signal is used to shift data into TDI on the rising edge, and out of TDO on the falling edge. The maximum clock frequency is 10 MHz.
TMS	36	I	TTLp	**IEEE 1149.1 Test Port Mode Select:** TMS is sampled on the rising edge of TCLK, and is used to place the Test Access Port controller into various states as defined in IEEE 1149.1. This input has an internal pull-up to VDD.
TDI	38	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked into this pin on the rising edge of TCK. This input has an internal pull-up to VDD.
TDO	37	O	TTL 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this pin on the falling edge of TCLK. When inactive, this 3-state output will be put into its high impedance state.
$\overline{\text{TRS}}$	35	I	TTLp	**IEEE 1149.1 Test Port Reset Pin:** This pin will asynchronously reset the Test Access Port (TAP) controller. This lead must be held low, asserted low, or pulsed low (for a minimum duration of 50 ns) to reset the TAP controller upon QT1M power-up. This input has an internal pull-up to VDD.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.5	+6.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, non-condensing	RH		100	%	Note 2
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended or warranted.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient	--	--	23.0	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}	160	175	215	mA	STS-1 (see Note 1)
P_{DD}	760	875	1130	mW	STS-1 (see Note 1)
I_{DD}	212	245	295	mA	STS-3 (see Note 1)
P_{DD}	1010	1225	1550	mW	STS-3 (see Note 1)
I_{DD}	215	250	300	mA	STM-1 (see Note 1)
P_{DD}	1020	1250	1575	mW	STM-1 (see Note 1)

Note 1: All values assume no more than 15 pF loading.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			1.65	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			±1.0	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTLs

Parameter	Min	Typ	Max	Unit	Test Conditions
VT- Negative going, threshold voltage			0.8	V	
VT+ Positive going, threshold voltage	2.0			V	
Input leakage current			1.0	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
Vhys Hysteresis (VT+ - VT-)	0.3		0.7	V	

INPUT PARAMETERS FOR TTLp, INPUT PADS WITH INTERNAL 25 µA PULL UP *

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			25	µA	$V_{DD} = 5.25$
Input capacitance		5.1		pF	

* Note: TTLp inputs can be disabled for device testing by applying a low to the $\overline{\text{TEST}}$ pin (pin 145).

OUTPUT PARAMETERS FOR CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
I_{OZ} (HIGHZ output current)			±10.0	µA	

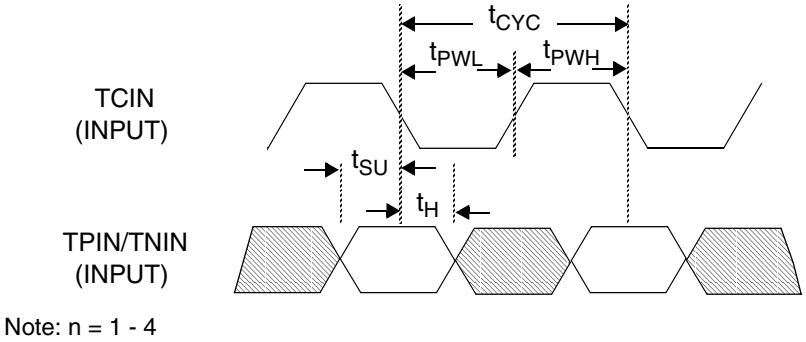
INPUT/OUTPUT PARAMETERS FOR TTL 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
INPUT LEAKAGE CURRENT			±1.0	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

TIMING CHARACTERISTICS

Detailed timing diagrams for the QT1M device are illustrated in Figures 4 through 12, with values of the timing intervals tabulated below each timing diagram. All output times are measured with a maximum 45 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or at voltage levels of $(V_{OH} + V_{OL})/2$ for output signals.

Figure 4. Ports 1, 2, 3 and 4 DS1 Transmit Timing

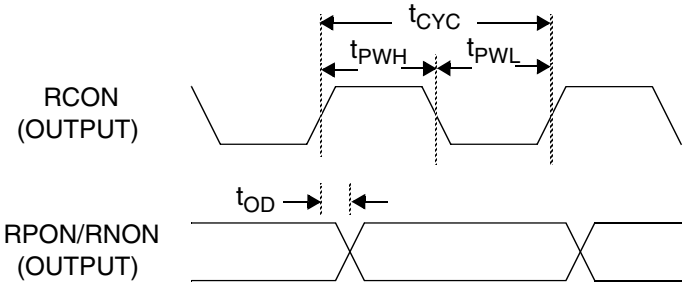


Note: n = 1 - 4

Note: TCIn is shown for TCLKI = 0, where data are clocked in on falling edges. Data are clocked in on rising edges when TCLKI =1. For NRZ operation, TNIn may be used to input an external loss of signal indication. Otherwise, this pin must be held high.

Parameter	Symbol	Min	Typ	Max	Unit
TCIn Clock period	t_{CYC}	560	647.7		ns
TCIn clock low time	t_{PWL}	280			ns
TCIn clock high time	t_{PWH}	280			ns
TPIn/TNIn data set-up time before TCIn↓	t_{SU}	10			ns
TPIn/TNIn data hold time after TCIn↓	t_H	4.0			ns

Figure 5. Ports 1, 2, 3 and 4 DS1 Receive Timing

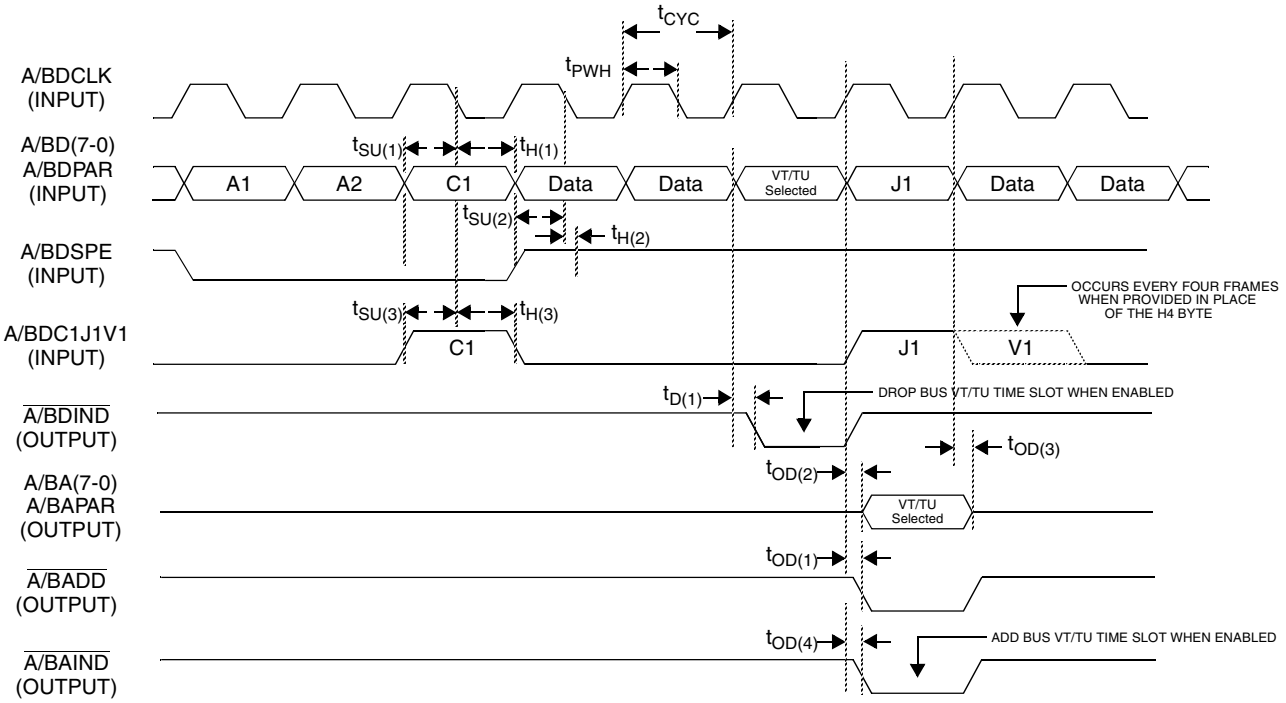


Note: n = 1 - 4

Note: RCOn is shown for RCLKI=0, where data are clocked out on rising edges. Data are clocked out on falling edges when RCLKI=1.

Parameter	Symbol	Min	Typ	Max	Unit
RCOn clock period	t_{CYC}	637		658	ns
RCOn clock low time	t_{PWL}	318		329	ns
RCOn clock high time	t_{PWH}	318		329	ns
RPOn/RNOn data delay from RCOn↑	t_{OD}	0.0		5.0	ns

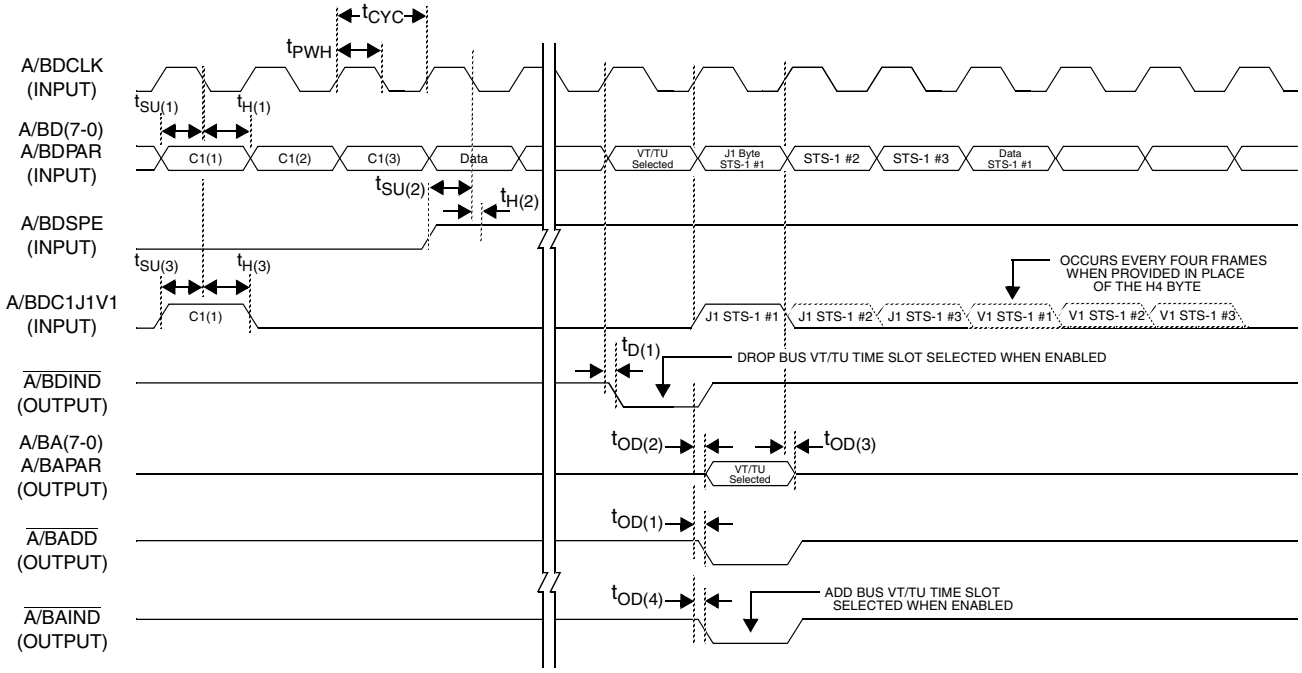
Figure 6. STS-1 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus



Note: For illustration purposes, a single VT/TU (VT number 28) is shown. The V1 pulse may or may not be present. If the V1 pulse is not present, the H4 byte must be provided. The delay of data from D(7-0) to A(7-0) is one byte time. An additional byte time of delay in A(7-0) is provided when control bit ABD is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		154.32		ns
DLCK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
D(7-0), DPAR data set up time before DCLK↓	$t_{SU(1)}$	4.0			ns
D(7-0), DPAR data hold time after DCLK↓	$t_{H(1)}$	5.0			ns
DSPE set up time before DCLK↓	$t_{SU(2)}$	4.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
DC1J1V1 set up time before DCLK↓	$t_{SU(3)}$	4.0			ns
DC1J1V1 hold time after DCLK↓	$t_{H(3)}$	5.0			ns
$\overline{DIND}$ drop bus indication output delay from DCLK ↑	$t_{D(1)}$	6.0		19	ns
A(7-0), APAR data out (from tristate) delay from DCLK↑	$t_{OD(2)}$	6.0		19	ns
A(7-0), APAR data to tristate delay from DCLK↑	$t_{OD(3)}$	6.0		20	ns
$\overline{ADD}$ add indicator delayed from DCLK↑	$t_{OD(1)}$	6.0		19	ns
$\overline{AIND}$ add bus indication output delay from DCLK↑	$t_{OD(4)}$	6.0		20	ns

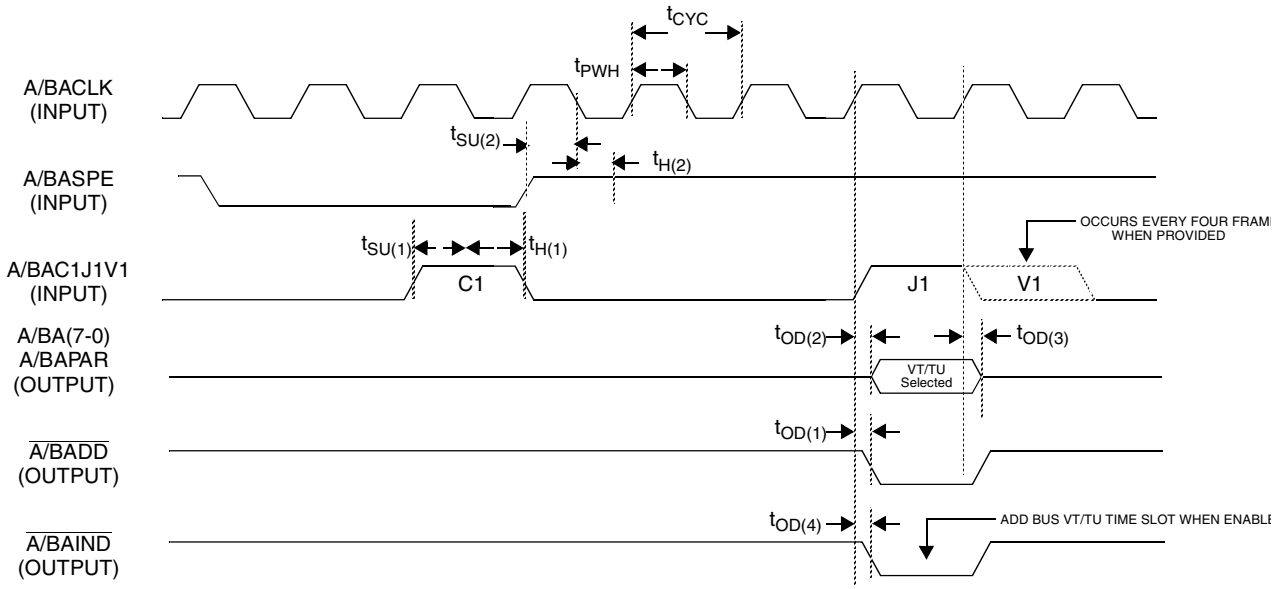
Figure 7. STS-3/STM-1 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus



Note: A single VT/TU is shown for illustration purposes. It also shows the VT/TU selection for the drop bus and add bus (number 28 in STS-1 number 3). The format is a AU-3/STS-3. For VC-4 operation, one J1 pulse and one optional V1 pulse are present. The delay of data from D(7-0) to A(7-0) is one byte time. An additional byte time of delay in A(7-0) is provided when control bit ABD is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
D(7-0), DPAR data set up time before DCLK↓	$t_{SU(1)}$	10			ns
D(7-0), DPAR data hold time after DCLK↓	$t_{H(1)}$	5.0			ns
DSPE set up time before DCLK↓	$t_{SU(2)}$	10			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
DC1J1V1 set up time before DCLK↓	$t_{SU(3)}$	10			ns
DC1J1V1 hold time after DCLK↓	$t_{H(3)}$	5.0			ns
$\overline{DIND}$ drop bus indication output delay from DCLK↑	$t_{D(1)}$	6.0		19	ns
A(7-0), APAR data out (from tristate) delay from DCLK↑	$t_{OD(2)}$	6.0		20	ns
A(7-0), APAR data to tristate delay from DCLK↑	$t_{OD(3)}$	6.0		20	ns
$\overline{ADD}$ add indicator delayed from DCLK↑	$t_{OD(1)}$	6.0		19	ns
$\overline{AIND}$ add bus indication output delay from DCLK↑	$t_{OD(4)}$	6.0		20	ns

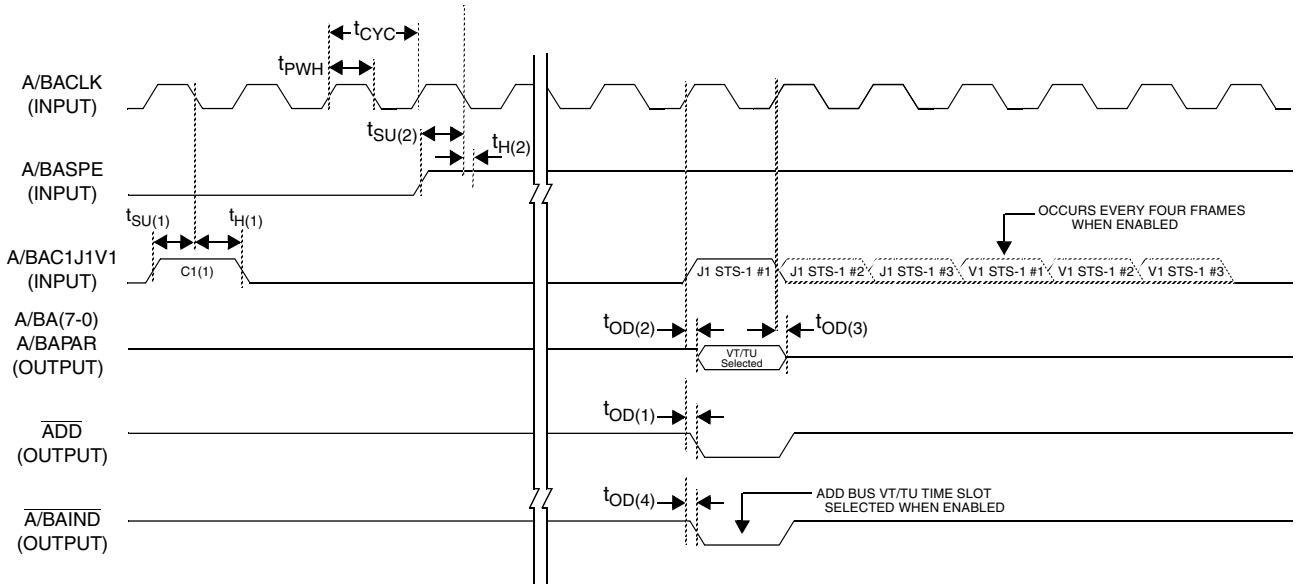
Figure 8. STS-1 A/B Add Bus Signals, Timing Derived from Add Bus



Note: For illustration purposes, a single VT/TU is shown. The location of this VT/TU corresponds to VT/TU number 28. An additional byte time of delay in A(7-0) is provided when control bit ABD is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		154.32		ns
ACLK duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
AC1J1V1 set up time before ACLK↓	$t_{SU(1)}$	10			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$	5.0			ns
ASPE set up time before ACLK↓	$t_{SU(2)}$	10			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
A(7-0), APAR data out (from tristate) delay from ACLK↑	$t_{OD(2)}$	6.0		19	ns
A(7-0), APAR data to tristate delay from ACLK↑	$t_{OD(3)}$	6.0		20	ns
$\overline{ADD}$ add indicator delayed from ACLK ↑	$t_{OD(1)}$	6.0		19	ns
$\overline{AIND}$ add bus indication output delay from ACLK↑	$t_{OD(4)}$	6.0		20	ns

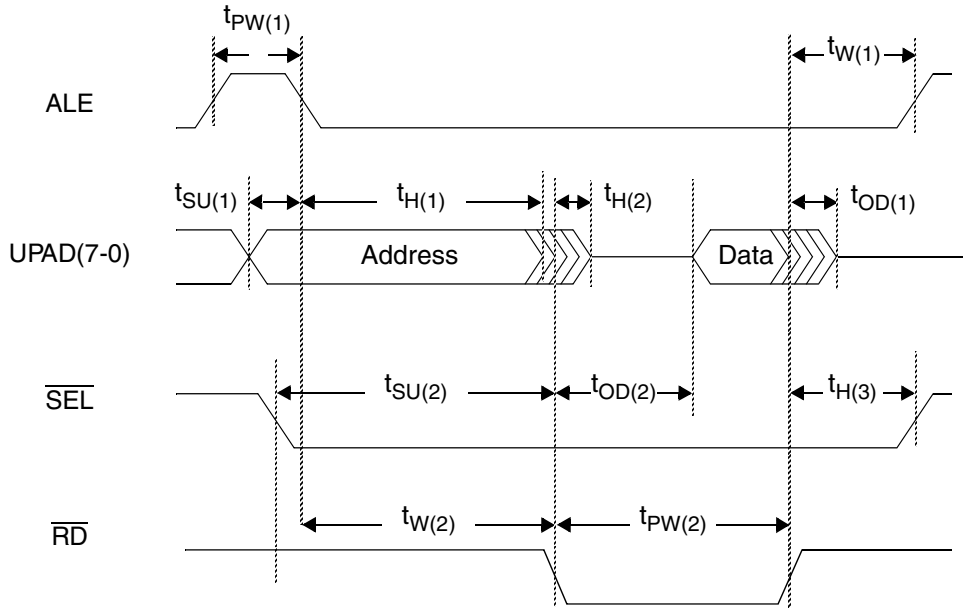
Figure 9. STS-3/STM-1 A/B Add Bus Signals, Timing Derived from Add Bus



Note: A single VT/TU is shown for illustration purposes. It also shows the VT/TU selection for the drop bus and add bus (number 28 in STS-1 number 3). The format is a AU-3/STS-3. For VC-4 operation, one J1 pulse and one optional V1 pulse are present. An additional byte time of delay in A(7-0) is provided when control bit ABD is written with a 1.

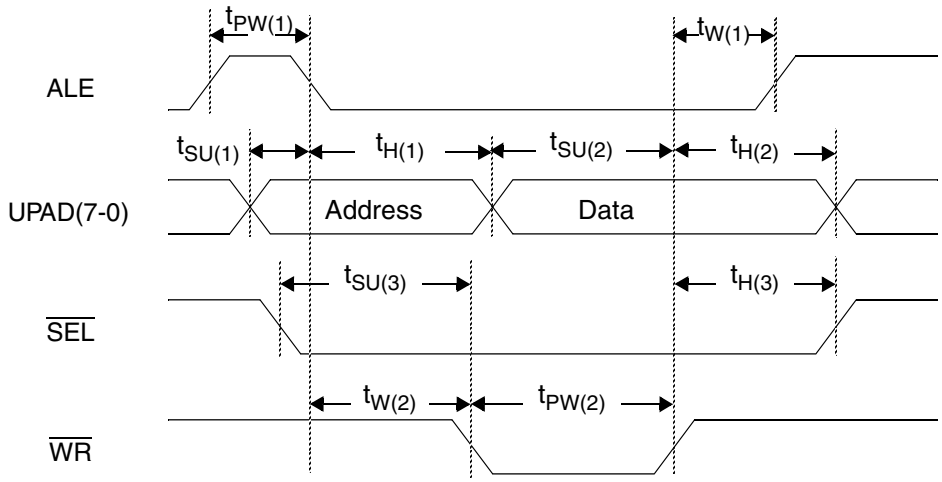
Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
AC1J1V1 set up time before ACLK↓	$t_{SU(1)}$	10			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$	5.0			ns
ASPE set up time before ACLK↓	$t_{SU(2)}$	10			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
A(7-0), APAR data out (from tristate) delay from ACLK↑	$t_{OD(2)}$	6.0		19	ns
A(7-0), APAR data to tristate delay from ACLK↑	$t_{OD(3)}$	6.0		19	ns
$\overline{ADD}$ add indicator delayed from ACLK↑	$t_{OD(1)}$	6.0		20	ns
$\overline{AIND}$ add bus indication output delay from ACLK↑	$t_{OD(4)}$	6.0		20	ns

Figure 10. Microprocessor Read Cycle Timing



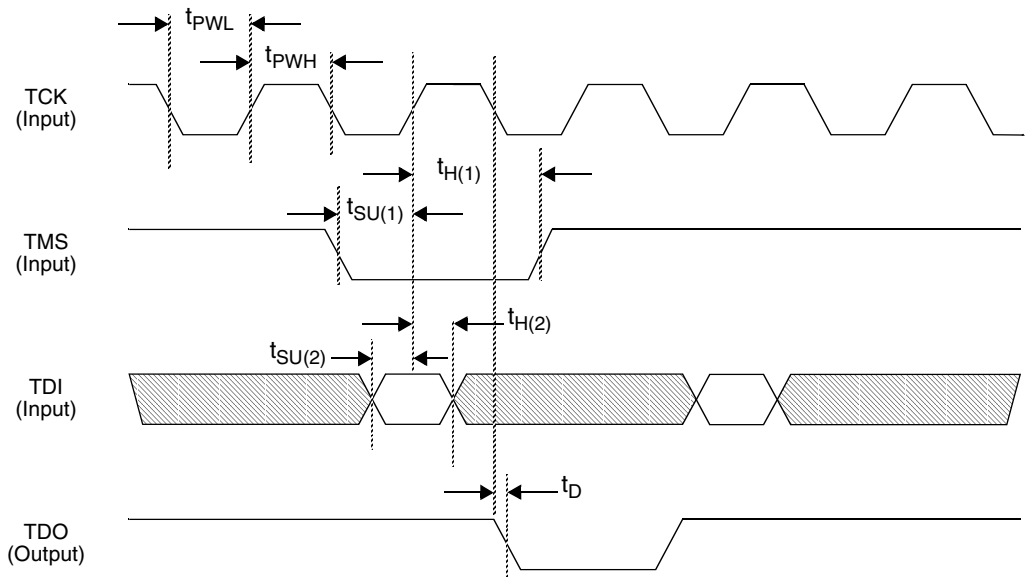
Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
UPAD(7-0) address set-up time before ALE↓	$t_{SU(1)}$	5.0			ns
UPAD(7-0) address hold time after ALE↓	$t_{H(1)}$	3.0			ns
UPAD(7-0) data available delay after $\overline{RD}$↓	$t_{OD(2)}$	5.0		17	ns
UPAD(7-0) data delay to tristate after $\overline{RD}$↑	$t_{OD(1)}$	2.0		8.0	ns
ALE wait time after $\overline{RD}$↑	$t_{W(1)}$	0.0			ns
$\overline{SEL}$ set-up before $\overline{RD}$↓	$t_{SU(2)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{RD}$↑	$t_{H(3)}$	0.0			ns
$\overline{RD}$ wait after ALE↓	$t_{W(2)}$	20			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	45			ns

Figure 11. Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
ALE wait after $\overline{WR}\uparrow$	$t_{W(1)}$	0.0			ns
UPAD(7-0) address set-up time before ALE$\downarrow$	$t_{SU(1)}$	5.0			ns
UPAD(7-0) address hold time after ALE$\downarrow$	$t_{H(1)}$	3.0			ns
UPAD(7-0) data set-up time before $\overline{WR}\uparrow$	$t_{SU(2)}$	3.0			ns
UPAD(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	16			ns
$\overline{SEL}$ set-up time before $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{WR}$ wait after ALE$\downarrow$	$t_{W(2)}$	20			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	45			ns

Figure 12. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time before TCK↑	$t_{SU(1)}$	5.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	6.0	-	ns
TDO delay from TCK↓	t_D	-	11	ns

OPERATION

The following sections detail the internal operation of the Quad T1 Mapper.

BUS INTERFACE MODES

The Quad T1 Mapper supports the following bus modes of operation:

- Drop Mode
- Single Unidirectional Ring Mode
- Multiplexer Mode
- Dual Unidirectional Ring Mode

Drop Mode

In the drop mode of operation, a VT/TU is terminated from either the A or B Drop bus to the receive output of one of the four ports, without a return path in the transmit direction.

Single Unidirectional Ring Mode

In the single unidirectional ring mode of operation, a VT/TU is dropped from the A (or B) Drop bus, with the return path the A (or B) Add bus. Timing for the VT/TU to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Multiplexer Mode

In the multiplexer mode of operation, a VT/TU is dropped from the A (or B) Drop bus, with the return path the B (or A) Add bus. Timing for the VT/TU to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Dual Unidirectional Ring Mode

In the dual unidirectional ring mode of operation, a VT/TU is dropped from the A (or B) Drop bus, with the return path both the A and B Add buses. Timing for the VT/TU to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

BUS MODE SELECTION

VT/TU Bus mode selection is performed by the control bits defined in the table shown below. The n represents the port number (1-4). Note: Both the A and B Add buses power up in the high impedance state. A 1 must be written to control bits AAHZE and BAHZE for normal add bus operation. If a channel is not assigned a valid VT number, the TnSEL(1-0) bits for that channel must be set to 00.

Mode Type	TnSEL1	TnSEL0	RnSEL	DROP from Bus	ADD to Bus
Dropping only, from A	0	0	0	A	Drop-only
Dropping only, from B	0	0	1	B	Drop-only
Single unidirectional ring	0	1	0	A	A
Single unidirectional ring	0	1	1	B	B
Multiplexer, A in, B out	1	0	0	A	B
Multiplexer B in, A out	1	0	1	B	A
Dual unidirectional ring	1	1	0	A	A and B
Dual unidirectional ring	1	1	1	B	B and A

Bus Mode Selection for Port n

SONET/SDH ADD/DROP MULTIPLEXING FORMAT SELECTIONS

The control bit settings for format selection are given in the table shown below. When the STS-1 format is selected, the buses are configured to operate at a bus rate of 6.48 Mbyte/s, instead of 19.44 Mbyte/s for VC-4/AU-3/STS-3 formats.

Format	MOD1	MOD0
STS-1 Format	0	0
STS-3 Format	0	1
STM-1 AU-3 Format	1	0
STM-1 TUG-3/VC-4 Format	1	1

Format Selection

ADD/DROP VT/TU SELECTION

Each of the four T1 ports has the ability to select and transmit a VT1.5 (VT/TU) in either or both (or neither) add bus segment (A Add bus and B Add bus). The VT1.5 (TU) number selection register labels, which consist of seven bits, are given in the following table. The VT/TU selected is valid for both the dropped (received) and added (transmitted) VT/TU. Note: If the VT selection is set to zero, the TnSEL(1-0) bits for that channel must be set to 00.

Locations 4CH (port 1), 7CH (port 2), ACH (port 3), DCH (port 4)

Bit	6	5	4	3	2	1	0	
AU-3/TUG-3 or STS-1 ID			VT/TU Group Number			VT/TU Number		Meaning
0	0		0	0	0	0	0	No VT/TU Selected
0	0							STS-1
0	1							AU-3/TUG-3 A, STS-1 #1
1	0							AU-3/TUG-3 B, STS-1 #2
1	1							AU-3/TUG-3 C, STS-1 #3
			0	0	1			VT/TU Group Number 1
			0	1	0			VT/TU Group Number 2
			0	1	1			VT/TU Group Number 3
			1	0	0			VT/TU Group Number 4
			1	0	1			VT/TU Group Number 5
			1	1	0			VT/TU Group Number 6
			1	1	1			VT/TU Group Number 7
						0	0	VT/TU Number 1
						0	1	VT/TU Number 2
						1	0	VT/TU Number 3
						1	1	VT/TU Number 4

VT/TU Selection

UNEQUIPPED PAYLOAD GENERATION

The QT1M is capable of sending an Unequipped Channel or Unequipped Supervisory Channel in all add modes of operation. A channel which has either the UCHnE bit or the USCHnE and UCHnE bits set in the Port Provisioning Registers will add an Unequipped Channel or Unequipped Supervisory Channel for the VT/TU selected. An Unequipped Channel has a VT/TU Pointer consisting of a valid NDF, size bits equal to 11, and a fixed pointer value of 78. The remaining VT Overhead bytes and the payload are sent as zeros. The Unequipped Supervisory Channel has an identical pointer to the Unequipped Channel, but sends a valid J2 byte, and valid BIP-2 bits and RDI-bit in V5, and valid RDI-bits in Z7. The V5 RDI and Z7 RDI bits can be set to zero by other control bits if they are not required. There are some differences in operation between the multiplex mode and the other Add/Drop modes based on the UEAME bit in register address 14H. The following table describes these differences.

*UCHnE	*USCHnE	**UEAME	Add/Drop Mode	Drop From	A-add	B-add
0	X	X	Multiplexed	A	High-Z	Normal
				B	Normal	High-Z
			Single Unidirectional Ring	A	Normal	High-Z
				B	High-Z	Normal
			Bidirectional Ring	A	Normal	Normal
				B	Normal	Normal
			Drop Only	A	High-Z	High-Z
				B	High-Z	High-Z
1	0	0	Multiplexed	A	**Unequipped	Normal
				B	Normal	**Unequipped
			Single Unidirectional Ring	A	Unequipped	High-Z
				B	High-Z	Unequipped
			Bidirectional Ring	A	Unequipped	Unequipped
				B	Unequipped	Unequipped
			Drop Only	A	High-Z	High-Z
				B	High-Z	High-Z
		1	Multiplexed	A	High-Z	**Unequipped
				B	**Unequipped	High-Z
			Single Unidirectional Ring	A	Unequipped	High-Z
				B	High-Z	Unequipped
			Bidirectional Ring	A	Unequipped	Unequipped
				B	Unequipped	Unequipped
			Drop Only	A	High-Z	High-Z
				B	High-Z	High-Z

* Note: For UCHnE=1 and USCHnE=1, substitute all occurrences of “Unequipped” in the table with “Unequipped Supervisory”.

** Note: Only multiplexed mode is effected by the UEAME control bit. All other modes operate independently of the state of the UEAME bit.

BUS TIMING

Timing for adding a VT/TU to the add bus is derived from the like-named drop bus, or from the like-named add bus. Bus timing may be selectable using a pin, or through software. Upon power-up or a device reset, the SBTEN (Software Bus Timing Enable) control bit is reset to 0. To enable the software to control timing, the SBTEN control bit must be first written with a 1, which will override the state placed on the $\overline{\text{ABUST}}$ pin. When SBTEN is 1, bus timing (add or drop bus timing) is controlled by the DRPBT control bit. The various states associated with the bus timing selection are shown in the table below.

$\overline{\text{ABUST}}$ pin	SBTEN	DRPBT*	Action
Low	0	X	Add bus timing selected.
High	0	X	Drop bus timing selected.
X	1	0	Add bus timing selected. $\overline{\text{ABUST}}$ pin disabled.
X	1	1	Drop bus timing selected. $\overline{\text{ABUST}}$ pin disabled.

* Note: X = Don't Care

Bus Timing Selection

DROP BUS MULTIFRAME ALIGNMENT

V1 byte alignment in the receive direction (from the drop bus) is established by using the H4 byte or the V1 reference pulse in the ADC1J1V1 and BDC1J1V1 signal. Depending on the format, one or three V1 pulses will be present in this signal. When the H4 byte is used to establish V1 byte alignment, the V1 pulse does not have to be present in the ADC1J1V1 or BDC1J1V1 signal. Writing a 1 to control bit DV1SEL selects the V1 pulse in the ADC1J1V1 and BDC1J1V1 signal to be used to establish the V1 byte location reference, while a 0 selects the H4 byte as the multiframe detector for establishing the V1 reference. The H4 multiframe detection circuits are disabled when the V1 pulse is used in place of the H4 byte.

For STM-1 VC-4 operation, a single V1 pulse must occur three drop bus clock cycles every four frames following the J1 pulse. For STS-3/STM-1 AUG3 operation, three V1 pulses must be present every four frames. Each V1 pulse must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte occurs six clock cycles after the V1 pulse.

For STS-1 operation, one V1 pulse must be present. The V1 pulse must occur on the next clock cycle after J1, and when the SPE signal is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the STS-1) in the POH bytes. The next column (first clock cycle) defines the VTs starting location. Thus, the V1 pulse identifies the starting location of the first V1 byte in the signal. The rest of the V1 bytes for the 28 VT1.5s are aligned regarding their starting point with respect to the V1 pulse. The timing relationships between J1, V1, and other signals are shown in the Timing Characteristics section.

The H4 byte is used to identify the location of the V1 byte as shown in Figure 13 below:

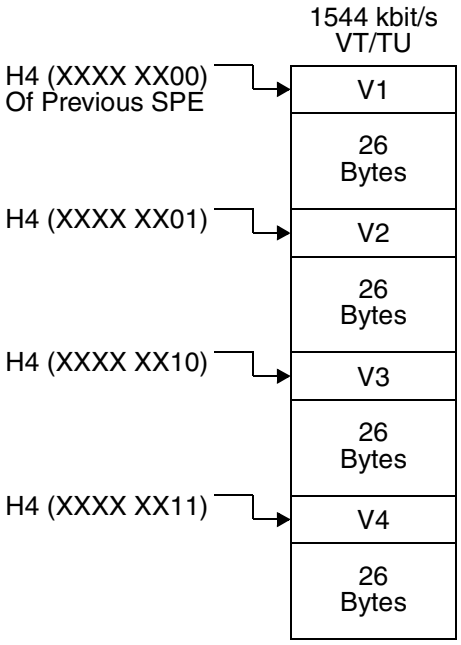


Figure 13. H4 Byte Floating VT Mode Bit Allocation

The H4 byte is monitored for multiframe alignment when enabled. Loss of multiframe alignment is declared (AnDH4E, BnDH4E) if two or more H4 byte values differ from those of a 2-bit counter for two consecutive multiframes. Recovery occurs when four consecutive sequential H4 byte values are detected once.

ADD BUS MULTIFRAME ALIGNMENT

When drop bus timing is selected, add bus V1 alignment is based on using the drop bus V1 pulse (A/BDC1J1V1), or the V1 reference signal that is generated by the H4 multiframe detectors in the drop bus side. When add bus timing is selected, V1 byte alignment for the add bus is established by using the V1 pulses that must be present in the A/BAC1J1V1 signal, when a 0 is written to control bit DV1REF.

When add bus timing is selected, the drop bus V1 reference from either the A/BDC1J1V1 signal, or from the internal V1 reference signal generated by the H4 multiframe detector in the drop bus direction, may also be used as the add bus V1 reference when control bit DV1REF is written with a 1. If the V1 pulse is present in the A/BAC1J1V1 signal it is ignored. This feature is common for the three AU-3/STS-1 signals. Extreme care must be taken when using this V1 selection mode to prevent add bus V1 byte alignment slips.

The control bit selection for V1 byte alignment is given in the Table below.

Bus Timing Mode	DV1SEL	DV1REF *	Action
Drop bus timing selected	0	X	Drop bus A/B H4 multiframe detector determines dropped VT/TU V1 byte starting location, and added VT/TU V1 byte starting location. V1 pulse in drop bus A/BDC1J1V1 signal ignored.
Drop bus timing selected	1	X	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped VT/TU V1 byte starting location, and added VT/TU V1 byte starting location. A/B drop bus H4 multiframe detector disabled.
Add bus timing selected	0	0	Drop bus A/B H4 multiframe detector determines dropped VT/TU V1 byte starting location. V1 pulse in drop bus A/BDC1J1V1 signal ignored. Add bus V1 alignment determined by the V1 pulse in the add bus A/BAC1J1V1 signal.
Add bus timing selected	1	0	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped VT/TU starting location. Drop bus H4 multiframe detector disabled. Add bus V1 alignment determined by the V1 pulse in the add bus A/BAC1J1V1 signal.
Add bus timing selected	0	1	Drop bus A/B H4 multiframe detector determines dropped VT/TU V1 byte starting location. V1 pulse in drop bus A/BDC1J1V1 or add bus A/BAC1J1V1 signals are ignored. Add bus V1 alignment determined by the internal V1 pulse generated by the drop bus A/B H4 byte detector.
Add bus timing selected	1	1	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped VT/TU V1 byte starting location, A/B Drop bus H4 multiframe detector disabled. V1 pulse in add bus A/BAC1J1V1 signal is ignored. Add bus V1 alignment determined by the V1 pulse in the add bus A/BAC1J1V1 signal.

* Note: X = Don't care

Add Bus V1 Reference Selection

PERFORMANCE COUNTERS

All performance counters are saturating, with the counters stopping at their maximum count. A counter is reset when it is read by the microprocessor. The performance counters for port n are also reset when a 1 is written to control bit RnSETC. This bit is self-clearing, and does not require the microprocessor to write a 0 into its location. Counts that occur during the read cycle are held and updated afterwards. For a 16-bit counter, the low order byte must be read first, followed by reading the high order byte.

ALARM STRUCTURE

All alarm indications are reported as latched (events) and as unlatched bit states. The alarm event bits will latch on the positive, negative, or positive and negative transitions of the alarm. The selection will also control the interrupt indication. The event transition is controlled by the selection bits IPOS and INEG.

A control bit is also provided that allows a positive level of the alarm to latch the event bits (latched bit positions) in an alarm register. In this mode, if the alarm is active during a read cycle, the latched alarm bit position clears, and will set immediately after the completion of the read cycle. This mode can activated by writing a 0 to control bit LATEN. A 0 written into this control bit will also disable the alarm transition (and interrupt) selection bits IPOS and INEG.

INTERRUPT STRUCTURE

Interrupt indication and interrupt mask registers are provided, as illustrated below. Status bits in the interrupt indication register indicate the status of latched alarm event bits in registers associated with that status bit, provided the corresponding interrupt mask bit is set for that status bit. The hardware interrupt indication is enabled when control bit HWDIE is 1. A global software interrupt indication bit (INT) is also provided. The hardware interrupt pin (INT/$\overline{\text{INT}}$) is a three-state 8 mA PAD, with a sense option to be active positive or negative. Should they be required, additional mask bits are provided in the memory map for disabling alarms for the status registers associated with port n. These additional mask bit locations must be initialized with FF hex. The interrupt works in the following manner. Assume that the hardware interrupt enable control bit HWDIE is 1, the alarm mask bits are a 1, the IPOS and LATEN bits are 1, and the INEG bit is 0.

The positive transition of an alarm causes the alarm status (event) bit in alarm register n (where n is port 1, 2, 3 or 4) to latch. This causes a software interrupt indication and hardware interrupt to occur. The microprocessor reads the interrupt indication register to determine the alarm registers to be read for that alarm. The microprocessor then reads the latched alarm registers that correspond to the interrupt indication bit and interrupt mask bit. The read cycle determines what alarm has been set. The completion of the read cycle clears the event (latched) alarm register and releases the hardware and software interrupt indication (INT).

If there is more than one alarm in more than one alarm register, each of the corresponding event (latched) alarm registers must be read before the interrupt is released. In addition, the hardware and software interrupt may be released by writing a 0 to the interrupt mask bit that corresponds to interrupt indication register. A second level of mask bits is also provided, if required. If the alarm remains active during the read cycle, the latched alarm bit position will not re-latch. The unlatched alarm registers should be read to check for alarm persistence. If an alarm has recovered (i.e., is in the off state) prior to the read cycle, and during the read cycle of the register that contains the alarm, the alarm occurs again, it will not result in a latched alarm indication.

Interrupt Registers

Interrupt Indication Register (Address 20H)

INT	0	ASIDE	BSIDE	PORT4	PORT3	PORT2	PORT1

Interrupt Mask Register (Address 21H)

0	0	ASMSK	BSMSK	P4MSK	P3MSK	P2MSK	P1MSK

Additional Interrupt Mask Registers (Addresses 17H, 18H, 19H)

RPT4A	RPT4B	RPT3A	RPT3B	RPT2A	RPT2B	RPT1A	RPT1B
TFIFO4A	TFIFO4B	TFIFO3A	TFIFO3B	TFIFO2A	TFIFO2B	TFIFO1A	TFIFO1B
TPORT4	TPORT3	TPORT2	TPORT1	RFIFO4	RFIFO3	RFIFO2	RFIFO1

Interrupt Indication ASIDE Registers (Addresses 22H, 24H)

A Side Drop/Add Alarms (ASIDE)

ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
0	0	0	0	0	A3DH4E	A2DH4E	A1DH4E

Interrupt Indication BSIDE Registers (Addresses 26H, 28H)

B Side Drop/Add Alarms (BSIDE)

BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
0	0	0	0	0	B3DH4E	B2DH4E	B1DH4E

Interrupt Indication PORTn Registers (Addresses 30H, 3AH, 44H for Port 1)

Port n Alarms (PORTn)

AnAIS	AnLOP	AnSIZE	AnNDF	AnRDI	AnRFI	AnUNEQ	AnSLER
BnAIS	BnLOP	BnSIZE	BnNDF	BnRDI	BnRFI	BnUNEQ	BnSLER
RnFFE	0	0	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS

Interrupt and Alarm Control Bit Summary

IPOS	INEG	HWDIE	LATEN	Interrupt Mask Bit	Action on an Alarm
0	0	0	1	X	No alarm event indication, or interrupt register indication.
X	X	X	0	0	Alarm event register sets on positive levels of an alarm; no software or hardware interrupt indications.
X	X	0	0	1	Alarm event register sets, and software interrupt indication occurs, on positive levels of the alarm; no hardware interrupt.
X	X	1	0	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive levels of the alarm.
1	0	X	1	0	Alarm event register sets on positive transitions of the alarm; no software or hardware interrupt indications.
1	0	0	1	1	Alarm event register sets, and software interrupt indication occurs, on positive transitions of the alarm; no hardware interrupt.
1	0	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive transitions of the alarm.
0	1	X	1	0	Alarm event register sets on negative transitions of the alarm; no software or hardware interrupt indications.
0	1	0	1	1	Alarm event register sets, and software interrupt indication occurs, on negative transitions of the alarm; no hardware interrupt.
0	1	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on negative transitions of the alarm.
1	1	X	1	0	Alarm event register sets on positive and/or negative transitions of the alarm; no software or hardware interrupt indications.
1	1	0	1	1	Alarm event register sets, and software interrupt indication occurs, on positive and/or negative transitions of the alarm; no hardware interrupt.
1	1	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive and/or negative transitions of alarm.

Note: X = Don't Care

SONET/SDH AIS DETECTION

The Quad T1 Mapper can detect an upstream AIS condition using the TOH H1/H2 (pointer) bytes or the TOH E1 (order wire) byte. When control bit SE1AIS is 0, the H1/H2 bytes are monitored for an upstream AIS condition. When the MOD control bits select the VC-4/TUG-3 format, the H11 and H21 bytes only are monitored for AIS. The monitoring of AIS in the two other H1n/H2n bytes is disabled. When the MOD control bits select the STS-3 or AU-3 format, each set of the three H1/H2 bytes per A Drop and B Drop buses are monitored for an AIS indication. Each of the three H1/H2 pointer bytes corresponds to the like-numbered AU-3/STS-1 signal. When the MOD control bits select the STS-1 format, the H1/H2 bytes per A Drop and B Drop buses are monitored for an AIS indication.

If all ones are detected in the H1/H2 bytes (whose location is determined by the C1 pulse) for three consecutive frames, the alarm bits AnUAISI (A bus detected H1/H2 or E1 byte upstream AIS) or BnUAISI (B bus detected H1/H2 or E1 byte upstream AIS) will set. Recovery occurs when a normal NDF (bits 1 through 4) in H1 is detected for three consecutive frames. A normal NDF is defined as a 0110 (and also a 1110, 0010, 0100, or 0111). The H1/H2 byte AIS detection circuits (when selected) for both the A and B Drop buses are disabled by writing a 0 to control bit HEAISE.

When control bit SE1AIS is 1, the E1n bytes are monitored for an upstream AIS condition. When the MOD control bits select the VC-4/TUG-3 format, the E11 byte in both buses is monitored for AIS. The detection of the upstream AIS indication in the E12 and E13 bytes is disabled. When the MOD control bits select the AU-3/STS-3 format, each of the three E1n bytes in the A and B Drop buses are monitored for AIS. Each of the three E1n bytes corresponds to the like-numbered AU-3/STS-1 signal. For STS-1 operation, the single E1 byte is checked for the upstream AIS indication.

Majority logic is used to determine if an E1n byte is carrying an upstream AIS indication. If 5 or more ones (at least 5 bits equal to 1 out of the 8 bits) are detected once in a A/B Drop bus E1n byte (whose locations are determined by the C1 pulse), the alarm bits AnUAISI (A bus detected H1/H2 or E1 Byte AIS) or BnUAISI (B bus detected H1/H2 or E1 Byte AIS) is set. Recovery occurs when 4 or more zeros (at least 4 bits equal to 0 out of the 8 bits) are detected one or more times. The E1n byte AIS detection circuits (when selected) for both the A and B Drop buses is disabled by writing a 0 to control bit HEAISE.

VT/TU POINTER TRACKING

The starting location of the V1 byte is determined by either the V1 pulses in the A/BC1J1V1 signals or the H4 multiframe detection circuits. The VT/TU pointer bit assignment for the V1 and V2 bytes is shown below. The alignment is necessary to determine the starting locations of the V5 byte and the other bytes that are carrying the 1544 kbit/s format.

	V1 Byte								V2 Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	SS-bits		I	D	I	D	I	D	I	D	I	D

I = Increment Bit
D = Decrement Bit
N = New Data Flag Bit
(enabled = 1001 or 0001/1101/1011/1000, normal or disabled = 0110 or 1110/0010/0100/0111)
Negative Justification: Inverted 5 D-bits and accept majority rule
Positive Justification: Inverted 5 I-bits and accept majority rule
SS-bits (VT Size) = 11 for 1544 kbit/s,

Pointer Bytes Bit Assignment

The pointer value is a binary number with a range of 0 to 103 for the 1544 kbit/s format. The pointer offset indicates the offset from the V2 byte to the first byte in the VT1.5 mapping. The pointer bytes are not counted in the offset calculation. The pointer offset arrangement for this format is shown below.

1544 kbit/s TU-11/VT1.5

V1
78
79-102
103
V2
0
1-24
25
V3
26
27-50
51
V4
52
53-76
77

VT/TU Pointer Offset Locations

Eight independent pointer-tracking state machines are used in the Quad T1 Mapper, one for each of the four ports 1, 2, 3, and 4, and also for both buses, the A bus and B bus. The pointer tracking algorithm is illustrated in Figure 14. The pointer tracking state machine is based on the pointer tracking machine found in the latest ETSI requirements, and is also valid for both Bellcore and ANSI. When control bit PTALTE is 0, the transition from AIS to LOP is disabled (shown dotted), which is required in Bellcore recommendations.

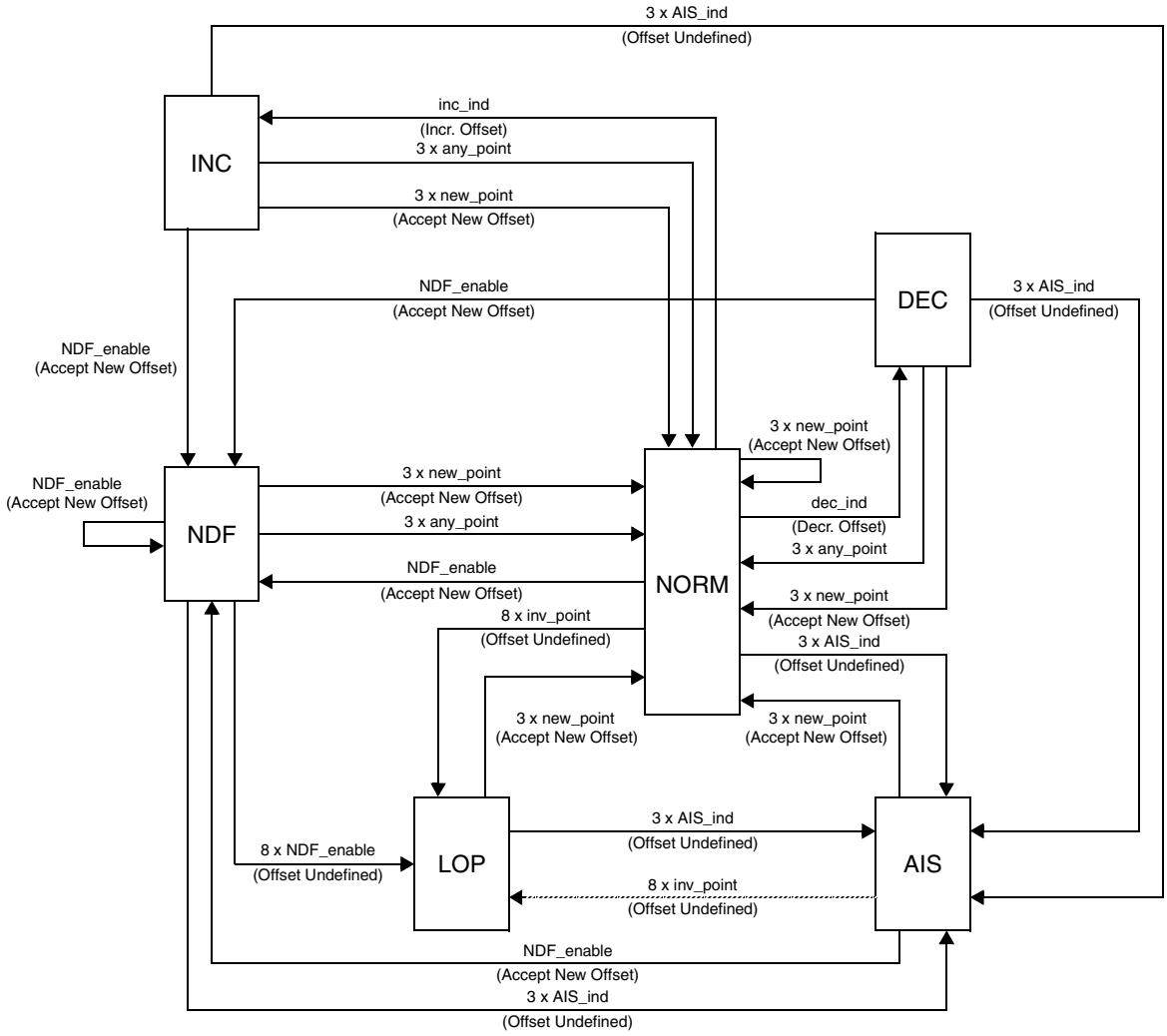
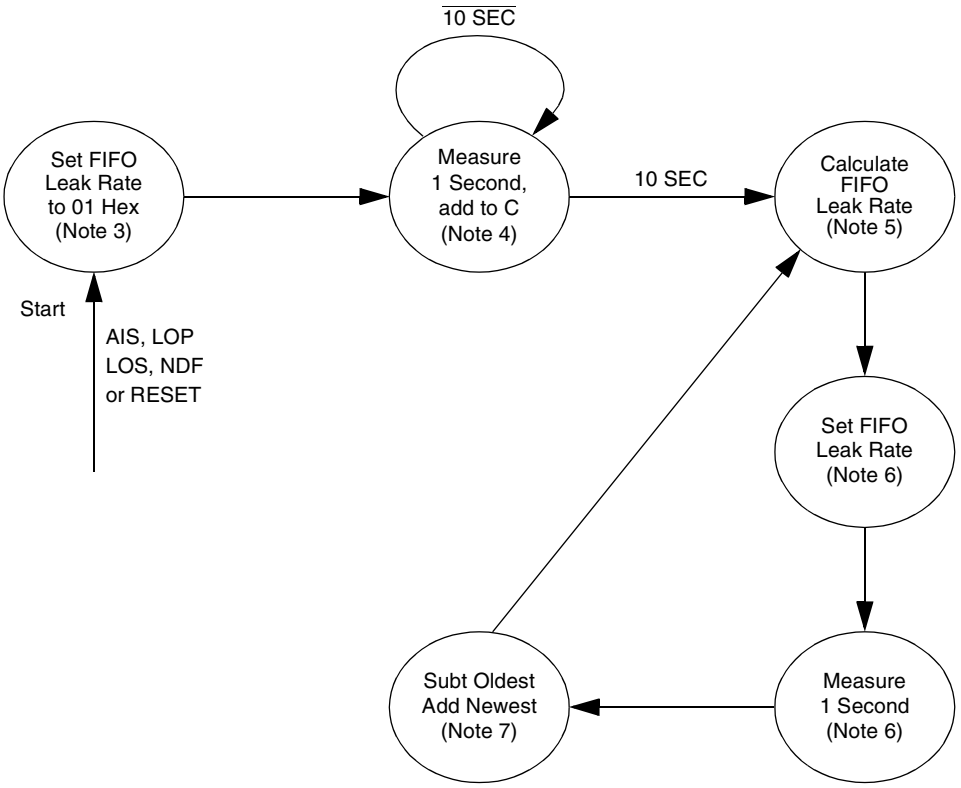


Figure 14. VT/TU Pointer Tracking State Machine

POINTER LEAK RATE CALCULATIONS



Notes:

1. The procedure described in Notes 2 through 8 below must be performed independently for each of the four ports of the QT1M device.
2. The procedure shown in the diagram above uses a ten-second sliding window with a resolution of one second.
3. The initial FIFO Leak Rate Register value (in memory map address 49H, 79H, A9H, or D9H) must first be set to 01 Hex (reset value).
4. Measure ten consecutive one-second samples from the Positive and Negative Stuff Counters being used. Store all ten difference values, i.e.,
   S_1 = POS STUFF COUNT1 - NEG STUFF COUNT1,
   S2 = POS STUFF COUNT2 - NEG STUFF COUNT2, and so on through
   S10 = POS STUFF COUNT10 - NEG STUFF COUNT10.
   There are eight pairs of stuff counters in the QT1M; care should be taken to use the pair appropriate to the programmed configuration of the device. The counters are located at addresses 32H, 62H, 92H and C2H (for the A-Side) and 3C, 6C, 9C, and CC (for the B-Side).
5. Calculate the leak rate (L.R.) using the following equation:
   L.R. = Hex [Int [1180 / C]], where
   C = ABS [S1 + S2 + ... + S10].
   Then, if L.R. < 1, let L.R = 1,
   or if L.R. > 255, let L.R = 255.
6. Set the FIFO Leak Rate Register (address 49H, 79H, A9H, or D9H) with the value between 1 and 255 calculated above, then take another one-second sample (e.g., S11).
7. Recalculate the value of 'C' by subtracting the oldest sample and adding the newest, and calculate a new leak rate, as described in Note 5 (e.g., using S2 through S11).
8. Continue to repeat the steps described in Notes 5, 6 and 7 until AIS, LOP, LOS or NDF is received or until you reset the QT1M.

REMOTE DEFECT INDICATIONS (RDI)

V5 and Z7 Byte Coding

Bits 5, 6 and 7 in the Z7 byte, in conjunction with bit 8 in the V5 byte, provide a detection scheme which is compliant with earlier versions of the RDI standard and also with enhanced VT/TU RDI capability. The enhanced version of RDI allows the user to differentiate between server, payload, and connectivity defects. Bit 8 in V5 is set equal to bit 5 in Z7. Bit 7 in Z7 is set to the inverse of bit 6 of Z7, which allows it to distinguish the enhanced version of RDI from the old version of RDI. It should be noted that when bits 6 and 7 in Z7 are either 01 or 10, the RDI indication is also influenced by Bit 8 of V5, as shown in the table below. When bits 6 and 7 are either 00 or 11, then RDI is determined solely by bit 8 in V5. This allows detection of an RDI originating from older equipment that generates the RDI in the V5 byte. The following table lists the RDI defect indications carried in the V5 and Z7 bytes.

Bit 8 V5 Bit 5 Z7	Bit 6 Z7	Bit 7 Z7	Definition
0	0	0	No defect indications (when RDIEN=0).
0	0	1	No defect indications (when RDIEN=1).
0	1	0	Remote Payload Defect - Path Label Mismatch - Loss of Multiframe.
0	1	1	No defect indications.
1	0	0	Remote defect (old equipment).
1	0	1	Remote Server Defect - Loss of Pointer - VT AIS detected - Upstream AIS detected (E1 or H1/H2 Bytes).
1	1	0	Remote Connectivity Defect - Unequipped Signal Label
1	1	1	Remote defect (old equipment).

RDI Bit Assignment

Detection and Recovery

The RDI alarms are defined in the table below. The number of consecutive events for detection and recovery is controlled by V5AL10. The value of five is selected when the V5AL10 control bit is 0, and the value of ten is selected when the V5AL10 control bit is 1.

AnRDIC BnRDIC	AnRDIP BnRDIP	AnRDIS BnRDIS	Action
0	0	1	Remote Server Defect Indication, and old equipment RDI indication (Bit 8 in the V5 byte).
0	1	0	Remote Payload Defect Indication.
1	0	0	Remote Connectivity Indication.

RDI Alarm Definition

Remote Defect Indications Generation

An RDI is sent for the following unlatched alarm conditions in the V5 and Z7 overhead bytes of the VT added to the A or B Add bus, depending on the states of the RnSEL (active bus selected), TnSEL1 and TnSEL0 (bus enabled) control bits. The following examples apply to port 1, but corresponding examples for ports 2 through 4 may be constructed by substituting the port number digit for the 1-digit in the bit symbols (except DV1SEL).

- When RDI enable (RDIEN) is 1, a remote payload defect indication is sent for:
    - A/B Drop H4 Error (A1DH4E, B1DH4E), when DV1SEL is 0
    - Mismatch signal label (A1SLER, B1SLER)

- When RDI enable (RDIEN) is 1, a remote server defect indication is sent for:
    - Loss of Pointer (A1LOP, B1LOP)
    - VT AIS (A1AIS, B1AIS)
    - A/B Drop Bus Upstream AIS in H1/H2 or the E1 byte (AnUAISI, BnUAISI), and HEAISE is 1 (where n represents the STS-1 or TUG in which the VT/TU has been selected).

- When RDI enable (RDIEN) is 1, a remote connectivity defect indication is sent for:
    - Unequipped signal label (A1UNEQ, B1UNEQ) and UQAE is 1

- When RDI enable (RDIEN) is 0, the microprocessor can control RDI generation:
    - Microprocessor writes a 1 to T1RDIS to generate remote server defect indication.
    - Microprocessor writes a 1 to T1RDIP to generate remote payload defect indication.
    - Microprocessor writes a 1 to T1RDIC to generate remote connectivity defect indication.

Note: The microprocessor may send an RDI by writing to the above control bits at any time, including the add only mode. To prevent contention between the internal logic and full microprocessor control, the RDIEN control bit should be written with a 0 when microprocessor control is intended. The three control bits TnRDIS, TnRDIP and TnRDIC may only be activated one at a time, since activation of two or more at the same time can cause decode errors.

OVERHEAD COMMUNICATIONS BIT ACCESS

Microprocessor access is provided for the eight overhead communications bits (O-bits) carried in the two justification control (JC) bytes in the multiframe format, e.g., in a 1544 kbit/s VT/TU, shown partially below. The bits in the justification control byte are numbered 1 through 8, starting with C1.

	Other Bytes							
	J2 Byte							
JC Byte 1	C1	C2	O	O	O	O	R	R
	24 Bytes - Information							
	V3 Byte							
	Z6 Byte							
JC Byte 2	C1	C2	O	O	O	O	R	R
	Other Bytes							

O-bit Placement in a 1544 kbit/s VT/TU

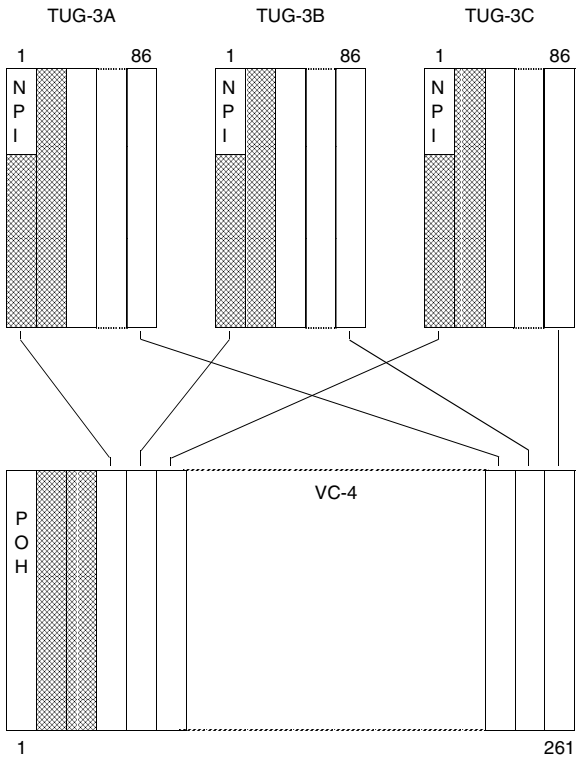
In the receive direction, the eight O-bits are stored in eight 8-bit registers (A and B for each of 4 ports) and these registers are updated each frame. The two O-bit nibbles that form a byte in the registers for receiving and transmitting are from the same multiframe. Bits 3 through 0 in an O-bit register correspond to bits 3 through 6 (C1C2 OOOO RR) in the first justification control byte, and bits 7 through 4 in an O-bit register correspond to bits 3 through 6 in the second justification control byte, as shown below.

	Second Justification Control Byte				First Justification Control Byte			
Bit	3	4	5	6	3	4	5	6
Register	7	6	5	4	3	2	1	0

O-bit Assignment Memory Map

TUG-3 NULL POINTER INDICATOR

For STM-1 TUG-3 format, the Quad T1 Mapper has the option to generate and transmit a Null Pointer Indicator (NPI) for one or more of the TUG-3s, as shown below.



NPI Structure

Three control bits (NPIA, NPIB and NPIC) are provided for selecting one or more of the TUG-3 NPIs. The three control bits are enabled when the MOD1 and MOD0 control bits are 11 (TUG-3/VC-4 format). The NPI consists of three bytes, starting with row 1. The table below shows the bit assignment for the first two bytes.

Bit	1	2	3	4	5	6	7	8
Row 1	1	0	0	1	0	0	1	1
Row 2	1	1	1	0	0	0	0	0

NPI Bit Assignment

The third byte (and the other 6 bytes in the column) are assigned as fixed stuff. Bytes which are designated as stuff (cross-hatched) will be in the high impedance state.

T1 LOOPBACK CAPABILITY

The Quad T1 Mapper provides two types of T1 loopbacks, facility and line (i.e., at the facility side and at the line side). Facility loopback per port is enabled when a 1 is written to control bit FnLBK. The internal transmit NRZ clock and data output signals are looped back as the receive clock and data input signals as shown in Figure 15, and remain available at the output pins. The receive clock and data signals at the input are disabled.

Line loopback per port is enabled when a 1 is written to control bit LnLBK. The receive clock and data output signals (rail) are looped back as the transmit data and clock signals (rail), as shown in Figure 15. The receive line rail or NRZ clock and data output signals are provided at the receive interface. The transmit clock and data signals (rail or NRZ) at the input are disabled.

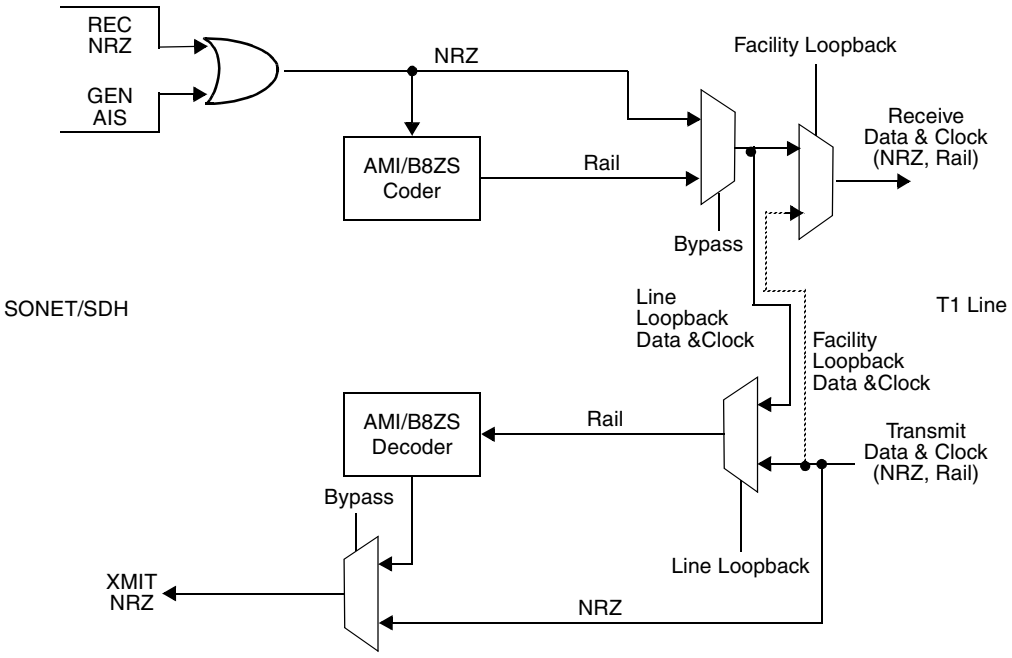


Figure 15. Facility and Line Loopbacks

RESETS

The Quad T1 Mapper has several reset options. These include a full hardware and software device reset, partial software resets, and counter software resets. All of the software reset bits are self-clearing and do not require a 0 to be written to a register location after the reset is applied by setting the bit to 1. Upon power-up, when the RESET bit (bit 7 in 15 hex) is written with a 1, or an active low is placed on the $\overline{\text{RESET}}$ pin (pin 155), the add bus data and the port T1 interfaces are forced to a high impedance state until the device is initialized or reinitialized. The AAHZE, BAHZE, and RnEN control bits must be written with zeros in order to enable the bus and line interfaces. In addition, the $\overline{\text{AAIND}}$, $\overline{\text{BAIND}}$, $\overline{\text{AADD}}$ and $\overline{\text{BADD}}$ pins are forced off. All performance counters are reset, and the alarms (except AnLOP, BnLOP) are reset. The control bits are also forced to zero, and the various FIFOs are recentered. A hardware reset can only be applied after the clocks are stable, and must be present for a minimum of 150 nanoseconds.

Writing 1 to a RnSETS software reset control bit for any of the ports resets the performance counters, re-centers the FIFO, and clears the alarms, except the AnLOP, BnLOP alarms, which will set for port n. The loss of pointer alarms will recover when a valid pointer is received. The control bits will not be reset.

Writing 1 to a RnSETC counter reset control bit for any of the ports resets the performance counters for that port. This feature allows the performance measurements to start at the same time for a port.

Writing 1 to control bits RESTAB or RESTBB resets the alarms for each of the two buses, A side and B side.

DATA THROUGHPUT DELAY

On the Receive side (SONET/SDH to T1) the mapper delay in T1 bit times will run from a nominal delay of 85 to 90 clocks, up to a maximum of 200 clocks with the Leak and Desynchronizer FIFOs near the saturation point. When using Bypass or AMI, there will be an eleven or ten clock nominal reduction in those figures, as the calculations were payload with the assumption of B8ZS encoding, which gives the maximum delay.

On the Transmit side (T1 to SONET/SDH) the maximum delay is approximately 85 clocks with a nominal delay of around 40 to 45 T1 bit times. The delay is less for AMI or NRZ than for B8ZS decoding.

BOUNDARY SCAN

Introduction

The Boundary Scan Interface block provide a five-pin Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external I/O pins from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. As shown in Figure 16, one cell of a boundary scan register is assigned to each input or output pin to be observed or tested (bidirectional pins may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output pins. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 12. The TDI, TMS and $\overline{TRS}$ pins have internal pull-up resistors. The pull-up is implemented with an active device which may be disabled for certain test situations by putting a low on the $\overline{TEST}$ input pin (pin 145). The normal state (i.e., power-up) is for the device to be active, and the inputs to be held high in the absence of external stimulus. The TDO is a tristate output, and the normal state is the high impedance state. It is driven only during the *Shift_DR* and *Shift_IR* states of the TAP controller state machine.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 16. The boundary scan function can be reset and disabled by holding pin $\overline{TRS}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the QT1M device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation[1]

The maximum frequency the QT1M device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface pins are shown in Figure 12.

The QT1M device performs the following four boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the QT1M device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The IDCODE test instruction (101) allows the loading of the internal device Identification Register, and the shifting of its contents through the Boundary Scan Register without interfering with normal device operation. The contents of the ID Register are 0109B0D7 (hex).

The BYPASS test instruction (111) provides the ability to bypass the QT1M boundary scan and instruction registers.

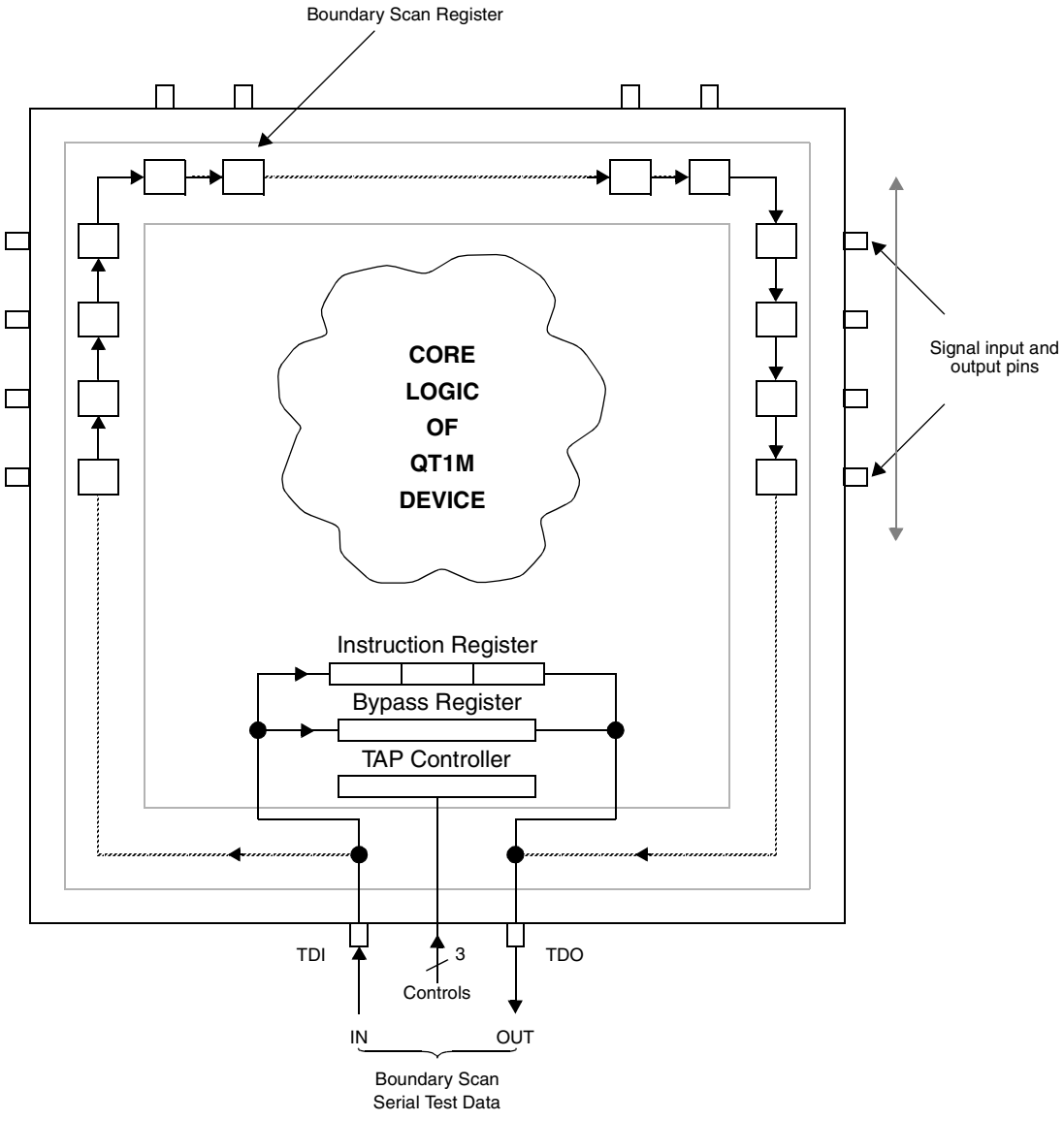
During the *Capture_IR* state of the TAP controller state machine, 001 is loaded into the 3-bit instruction register.

1. The BSDL file for this device contains further information regarding the operation of the TAP. This file is available upon request from the Applications Engineering department of TranSwitch.

Boundary Scan Reset

Specific control of the $\overline{TRS}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the QT1M.

Figure 16. Boundary Scan Schematic



Boundary Scan Chain

There are 143 scan cells in the QT1M boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function. The notes numbered 1 through 5 appear at the end of the table.

Scan Cell #	Direction	Pin #	Pin Name	Comments
0	Input [1]	33	ADSPE	A Drop SPE Indicator
1	Input	32	ADC1J1V1	A Drop C1J1V1 Indicator
2	Input	31	AASPE	A Add SPE Indicator
3	Input	30	AAC1J1V1	A Add C1J1V1 Indicator
4	Input	28	AACLK	A Add Clock In
5	Input	26	ADCLK	A Drop Clock In
6	2-State	24	$\overline{\text{ADIND}}$	A Drop Bus VT Slot Indicator
7	2-State	23	$\overline{\text{AAIND}}$	A Add Bus VT Slot Indicator
8	Input	21	TPI1	Port 1 Positive Rail In
9	Input	20	TNI1/$\overline{\text{TLOS1}}$	Port 1 Neg. Rail In/LOS In
10	Input	19	TCI1	Port 1 Transmit Clock In
11	Input	18	QUIET1	Quiet Port 1
12	3-State [2]	16	RPO1	Port 1 Positive Rail Out
13	Control [3]	--	rn1_enb	Output Enable for 15
14	3-State	15	RNO1	Port 1 Negative Rail Out
15	Control	--	rcp1_enb	Output Enable for 14, 16
16	3-State	14	RCO1	Port 1 Receive Clock Out
17	3-State	12	RPO3	Port 3 Positive Rail Out
18	Control	--	rn3_enb	Output Enable for 11
19	3-State	11	RNO3	Port 3 Negative Rail Out
20	Control	--	rcp3_enb	Output Enable for 10, 12
21	3-State	10	RCO3	Port 3 Receive Clock Out
22	Input	8	TPI3	Port 3 Positive Rail In
23	Input	7	TNI3/$\overline{\text{TLOS3}}$	Port 3 Neg. Rail In/LOS In
24	Input	6	TCI3	Port 3 Transmit Clock In
25	Input	5	QUIET3	Quiet Port 3
26	--	3	Reserved	Unused: Observe-only Cell
27	--	2	N.C.	Unused: Observe-only Cell
28	--	1	Reserved	Unused: Observe-only Cell
29	--	160	Reserved	Unused: Observe-only Cell
30	--	159	Reserved	Unused: Observe-only Cell
31	--	158	Reserved	Unused: Observe-only Cell
32	Input	157	$\overline{\text{ABUST}}$	A/B Add Bus Timing Select
33	--	156	Reserved	Unused: Observe-only Cell
34	Input	155	$\overline{\text{RESET}}$	Low-Active Device Reset
35	--	153	Reserved	Unused: Observe-only Cell
36	3-State	152	INT/$\overline{\text{INT}}$	Interrupt Out-Polarity Selectable

Scan Cell #	Direction	Pin #	Pin Name	Comments
37	Control	--	hwint_enb	Output Enable for 152
38	Input	150	INTSH	Interrupt Sense High
39	Input	149	ALE	CPU Interface Add. Lat. En.
40	Input	148	$\overline{WR}$	CPU Interface Write Line
41	Input	147	$\overline{RD}$	CPU Interface Read Line
42	Input	146	$\overline{SEL}$	CPU Interface Select Line
43	Input	145	$\overline{TEST}$	
44	--	144	Reserved	Unused: Observe-only Cell
45	--	143	Reserved	Unused: Observe-only Cell
46	--	141	Reserved	Unused: Observe-only Cell
47	--	140	Reserved	Unused: Observe-only Cell
48	Input	138	EXTCK	External 48.6360 MHz Clock
49	Input [4]	136	$\overline{HIGHZ}$	Observe & Control
50	--	135	Reserved	Unused: Observe-only Cell
51	Input [5]	133	UPAD7	CPU Address/Data Bus
52	3-State [5]	133	UPAD7	CPU Address/Data Bus
53	Input [5]	132	UPAD6	CPU Address/Data Bus
54	Control [5]	--	Cado67_enb	Output Enable for 132, 133
55	3-State [5]	132	UPAD6	CPU Address/Data Bus
56	Input	130	UPAD5	CPU Address/Data Bus
57	3-State	130	UPAD5	CPU Address/Data Bus
58	Input	129	UPAD4	CPU Address/Data Bus
59	Control	--	Cado45_enb	Output Enable for 129, 130
60	3-State	129	UPAD4	CPU Address/Data Bus
61	Input	128	UPAD3	CPU Address/Data Bus
62	3-State	128	UPAD3	CPU Address/Data Bus
63	Input	126	UPAD2	CPU Address/Data Bus
64	Control	--	Cado23_enb	Output Enable for 126, 128
65	3-State	126	UPAD2	CPU Address/Data Bus
66	Input	125	UPAD1	CPU Address/Data Bus
67	3-State	125	UPAD1	CPU Address/Data Bus
68	Input	124	UPAD0	CPU Address/Data Bus
69	Control	--	Cado01_enb	Output Enable for 124, 125
70	3-State	124	UPAD0	CPU Address/Data Bus
71	--	122	Reserved	Unused: Observe-only Cell
72	--	121	N.C.	Unused: Observe-only Cell
73	Input	119	QUIET4	Quiet Port 4
74	Input	118	TCI4	Port 4 Transmit Clock In
75	Input	117	TNI4/$\overline{TLOS4}$	Port 4 Neg. Rail In/LOS In
76	Input	116	TPI4	Port 4 Positive Rail In

Scan Cell #	Direction	Pin #	Pin Name	Comments
77	3-State	114	RCO4	Port 4 Receive Clock Out
78	3-State	113	RNO4	Port 4 Negative Rail Out
79	Control	--	rn4_enb	Output Enable for 113
80	Control	--	rcp4_enb	Output Enable for 112, 114
81	3-State	112	RPO4	Port 4 Positive Rail Out
82	3-State	111	RCO2	Port 2 Receive Clock Out
83	3-State	110	RNO2	Port 2 Negative Rail Out
84	Control	--	rn2_enb	Output Enable for 110
85	Control	--	rcp2_enb	Output Enable for 109, 111
86	3-State	109	RPO2	Port 2 Position Rail Out
87	Input	107	QUIET2	Quiet Port 2
88	Input	106	TCI2	Port 2 Transmit Clock In
89	Input	105	TNI2/$\overline{\text{TLOS2}}$	Port 2 Neg. Rail In/LOS In
90	Input	104	TPI2	Port 2 Positive Rail In
91	2-State	102	$\overline{\text{BAIND}}$	B Add Bus VT Slot Indicator
92	2-State	101	$\overline{\text{BDIND}}$	B Drop Bus VT Slot Indicator
93	Input	99	BDCLK	B Drop Clock In
94	Input	98	BACLK	B Add Clock In
95	Input	96	BAC1J1V1	B Add C1J1V1 Indicator
96	Input	95	BASPE	B Add SPE Indicator
97	Input	94	BDC1J1V1	B Drop C1J1V1 Indicator
98	Input	93	BDSPE	B Drop SPE Indicator
99	Input	91	BDPAR	B Drop Parity Bit
100	Input	90	BD7	B Drop Bus Data
101	Input	89	BD6	B Drop Bus Data
102	Input	88	BD5	B Drop Bus Data
103	Input	87	BD4	B Drop Bus Data
104	Input	85	BD3	B Drop Bus Data
105	Input	84	BD2	B Drop Bus Data
106	Input	83	BD1	B Drop Bus Data
107	Input	82	BD0	B Drop Bus Data
108	2-State	78	$\overline{\text{BADD}}$	B Add Data Present
109	3-State	77	BAPAR	B Add Parity Bit
110	3-State	76	BA7	B Add Bus Data
111	Control	--	Ba6p_enb	Output Enable for 75, 76, 77
112	3-State	75	BA6	B Add Bus Data
113	3-State	73	BA5	B Add Bus Data
114	3-State	72	BA4	B Add Bus Data
115	Control	--	Ba35_enb	Output Enable for 71, 72, 73
116	3-State	71	BA3	B Add Bus Data

Scan Cell #	Direction	Pin #	Pin Name	Comments
117	3-State	69	BA2	B Add Bus Data
118	3-State	68	BA1	B Add Bus Data
119	Control	--	Ba02_enb	Output Enable for 67, 68, 69
120	3-State	67	BA0	B Add Bus Data
121	3-State	65	AA0	A Add Bus Data
122	3-State	64	AA1	A Add Bus Data
123	Control	--	Aa02_enb	Output Enable for 63, 64, 65
124	3-State	63	AA2	A Add Bus Data
125	3-State	62	AA3	A Add Bus Data
126	3-State	60	AA4	A Add Bus Data
127	Control	--	Aa35_enb	Output Enable for 59, 60, 62
128	3-State	59	AA5	A Add Bus Data
129	3-State	58	AA6	A Add Bus Data
130	3-State	56	AA7	A Add Bus Data
131	3-State	55	AAPAR	A Add Parity Bit
132	Control	--	Aa6p_enb	Output Enable for 55, 56, 58
133	Output	54	$\overline{\text{AADD}}$	A Add Data Present
134	Input	52	AD0	A Drop Bus Data
135	Input	51	AD1	A Drop Bus Data
136	Input	50	AD2	A Drop Bus Data
137	Input	48	AD3	A Drop Bus Data
138	Input	47	AD4	A Drop Bus Data
139	Input	46	AD5	A Drop Bus Data
140	Input	44	AD6	A Drop Bus Data
141	Input	43	AD7	A Drop Bus Data
142	Input	42	ADPAR	A Drop Parity Bit

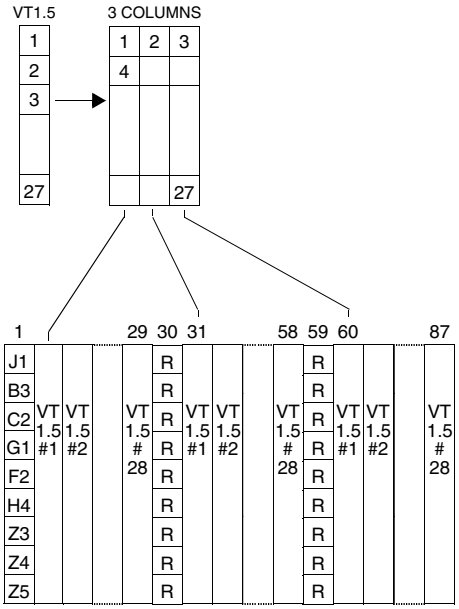
Notes:

1. Input Pins have Observe-Only Boundary Scan Cells unless otherwise noted.
2. 3-State Outputs indicate signals which can, in normal circuit functioning, be Active (High/Low), Inactive (Low/High), or in a High Impedance State. This varies from the 2-State Outputs, which although they use tristateable Output Buffers, are always either High or Low only regardless of their Active polarity. These outputs can be put in a High Impedance State only by applying a Low logic level to the $\overline{\text{HIGHZ}}$ input signal which puts all Output Pins in such a state.
3. Where BSR Cells have “Control” in the Direction column, it signifies that this cell is for observation and control of an Output Enable of a 3-State Output or Bidirectional Pin. The Comments column will list the Pin number(s) of the signal(s) that it controls. All output enables are active when low (‘0’), and all Bidirectional controls drive out when low (‘0’).
4. The $\overline{\text{HIGHZ}}$ Signal is a special case of Input in that its only function is to disable all output pins on the device for testing purposes. This input pin has an Observe and Control BS Cell which allows it to be Preloaded via the SAMPLE/PRELOAD command with a High Logic (“1”). This value, which is loaded into the Registered Parallel Output of the BS Cell during the Update DR state, is applied to the signal during the EXTEST, in much the same way that Controls (Enables) for Bidirectional Signals or 3-State Outputs are handled.
5. Bidirectional Pins have two BSR cells, one Observe-Only BS Cell for the Input and an Observe & Control BS Cell for the Output. In addition there will be a Control & Observe Cell for the direction control pin, although in most cases these serve two or more pins.

MULTIPLEX FORMAT AND MAPPING INFORMATION

STS-1 VT1.5 (1.544 Mbit/s) Multiplex Format

The following diagram and table illustrate the mapping of the 28 VT1.5s into a STS-1 SPE. Column 1 is assigned to carry the path overhead bytes.



STS-1 SPE

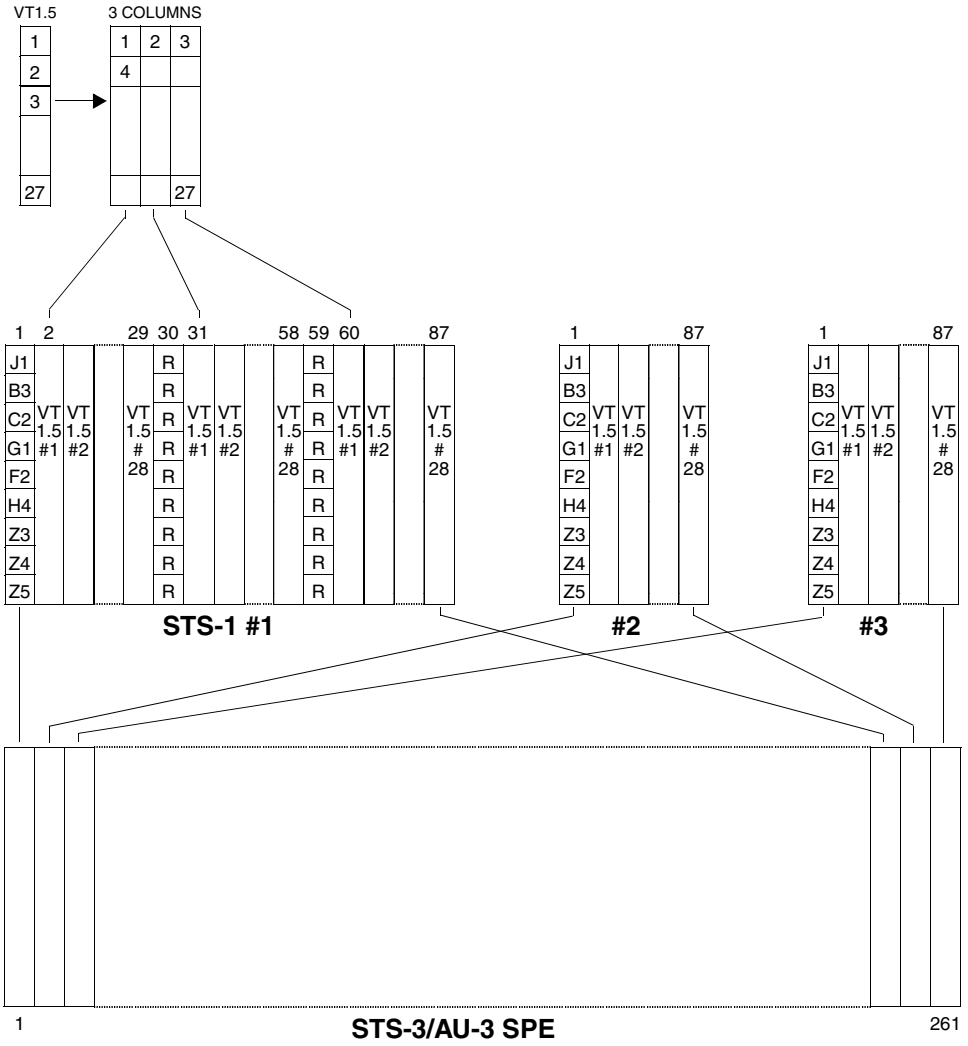
STS-1 Mapping

VT#	4CH (Port 1), 7CH (Port 2), ACH (Port 3) and DCH (Port 4) Registers							VT1.5 Column Numbers*
	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	No VT Selected
1	0	0	0	0	1	0	0	2, 31, 60
2	0	0	0	1	0	0	0	3, 32, 61
3	0	0	0	1	1	0	0	4, 33, 62
4	0	0	1	0	0	0	0	5, 34, 63
5	0	0	1	0	1	0	0	6, 35, 64
6	0	0	1	1	0	0	0	7, 36, 65
7	0	0	1	1	1	0	0	8, 37, 66
8	0	0	0	0	1	0	1	9, 38, 67
9	0	0	0	1	0	0	1	10, 39, 68
10	0	0	0	1	1	0	1	11, 40, 69
11	0	0	1	0	0	0	1	12, 41, 70
12	0	0	1	0	1	0	1	13, 42, 71
13	0	0	1	1	0	0	1	14, 43, 72
14	0	0	1	1	1	0	1	15, 44, 73
15	0	0	0	0	1	1	0	16, 45, 74
16	0	0	0	1	0	1	0	17, 46, 75
17	0	0	0	1	1	1	0	18, 47, 76
18	0	0	1	0	0	1	0	19, 48, 77
19	0	0	1	0	1	1	0	20, 49, 78
20	0	0	1	1	0	1	0	21, 50, 79
21	0	0	1	1	1	1	0	22, 51, 80
22	0	0	0	0	1	1	1	23, 52, 81
23	0	0	0	1	0	1	1	24, 53, 82
24	0	0	0	1	1	1	1	25, 54, 83
25	0	0	1	0	0	1	1	26, 55, 84
26	0	0	1	0	1	1	1	27, 56, 85
27	0	0	1	1	0	1	1	28, 57, 86
28	0	0	1	1	1	1	1	29, 58, 87

* Note: Columns 30 and 59 carry fixed stuff bytes. Column 1 is assigned for the POH bytes.

STS-3/AU-3 VT1.5/TU-11 (1.544 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the VT1.5/TU-11s into a STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes.



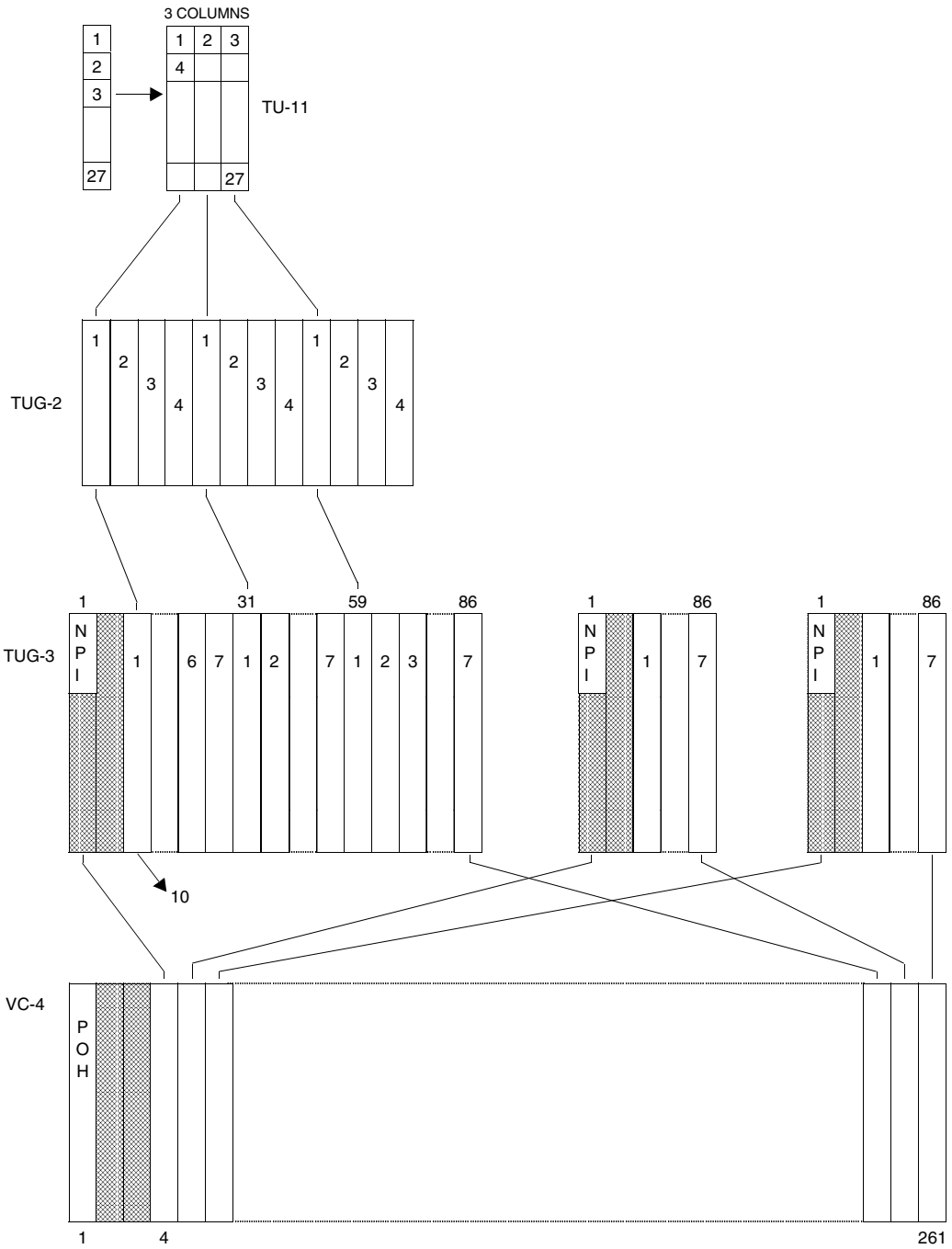
STS-3 AU-3 Mapping

VT TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VT/TU Column Numbers*
	0 0 0 0 0 0 0	No TU Selected						
1	0 1 0 0 1 0 0	4 91 178	29	1 0 0 0 1 0 0	5 92 179	57	1 1 0 0 1 0 0	6 93 180
2	0 1 0 1 0 0 0	7 94 181	30	1 0 0 1 0 0 0	8 95 182	58	1 1 0 1 0 0 0	9 96 183
3	0 1 0 1 1 0 0	10 97 184	31	1 0 0 1 1 0 0	11 98 185	59	1 1 0 1 1 0 0	12 99 186
4	0 1 1 0 0 0 0	13 100 187	32	1 0 1 0 0 0 0	14 101 188	60	1 1 1 0 0 0 0	15 102 189
5	0 1 1 0 1 0 0	16 103 190	33	1 0 1 0 1 0 0	17 104 191	61	1 1 1 0 1 0 0	18 105 192
6	0 1 1 1 0 0 0	19 106 193	34	1 0 1 1 0 0 0	20 107 194	62	1 1 1 1 0 0 0	21 108 195
7	0 1 1 1 1 0 0	22 109 196	35	1 0 1 1 1 0 0	23 110 197	63	1 1 1 1 1 0 0	24 111 198
8	0 1 0 0 1 0 1	25 112 199	36	1 0 0 0 1 0 1	26 113 200	64	1 1 0 0 1 0 1	27 114 201
9	0 1 0 1 0 0 1	28 115 202	37	1 0 0 1 0 0 1	29 116 203	65	1 1 0 1 0 0 1	30 117 204
10	0 1 0 1 1 0 1	31 118 205	38	1 0 0 1 1 0 1	32 119 206	66	1 1 0 1 1 0 1	33 120 207
11	0 1 1 0 0 0 1	34 121 208	39	1 0 1 0 0 0 1	35 122 209	67	1 1 1 0 0 0 1	36 123 210
12	0 1 1 0 1 0 1	37 124 211	40	1 0 1 0 1 0 1	38 125 212	68	1 1 1 0 1 0 1	39 126 213
13	0 1 1 1 0 0 1	40 127 214	41	1 0 1 1 0 0 1	41 128 215	69	1 1 1 1 0 0 1	42 129 216
14	0 1 1 1 1 0 1	43 130 217	42	1 0 1 1 1 0 1	44 131 218	70	1 1 1 1 1 0 1	45 132 219
15	0 1 0 0 1 1 0	46 133 220	43	1 0 0 0 1 1 0	47 134 221	71	1 1 0 0 1 1 0	48 135 222
16	0 1 0 1 0 1 0	49 136 223	44	1 0 0 1 0 1 0	50 137 224	72	1 1 0 1 0 1 0	51 138 225
17	0 1 0 1 1 1 0	52 139 226	45	1 0 0 1 1 1 0	53 140 227	73	1 1 0 1 1 1 0	54 141 228
18	0 1 1 0 0 1 0	55 142 229	46	1 0 1 0 0 1 0	56 143 230	74	1 1 1 0 0 1 0	57 144 231
19	0 1 1 0 1 1 0	58 145 232	47	1 0 1 0 1 1 0	59 146 233	75	1 1 1 0 1 1 0	60 147 234
20	0 1 1 1 0 1 0	61 148 235	48	1 0 1 1 0 1 0	62 149 236	76	1 1 1 1 0 1 0	63 150 237
21	0 1 1 1 1 1 0	64 151 238	49	1 0 1 1 1 1 0	65 152 239	77	1 1 1 1 1 1 0	66 153 240
22	0 1 0 0 1 1 1	67 154 241	50	1 0 0 0 1 1 1	68 155 242	78	1 1 0 0 1 1 1	69 156 243
23	0 1 0 1 0 1 1	70 157 244	51	1 0 0 1 0 1 1	71 158 245	79	1 1 0 1 0 1 1	72 159 246
24	0 1 0 1 1 1 1	73 160 247	52	1 0 0 1 1 1 1	74 161 248	80	1 1 0 1 1 1 1	75 162 249
25	0 1 1 0 0 1 1	76 163 250	53	1 0 1 0 0 1 1	77 164 251	81	1 1 1 0 0 1 1	78 165 252
26	0 1 1 0 1 1 1	79 166 253	54	1 0 1 0 1 1 1	80 167 254	82	1 1 1 0 1 1 1	81 168 255
27	0 1 1 1 0 1 1	82 169 256	55	1 0 1 1 0 1 1	83 170 257	83	1 1 1 1 0 1 1	84 171 258
28	0 1 1 1 1 1 1	85 172 259	56	1 0 1 1 1 1 1	86 173 260	84	1 1 1 1 1 1 1	87 174 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

* Note: Columns 88, 89, 90, 175, 176, 177 are fixed stuff.

TU-11 - VC-4 Multiplex Format Mapping

The following diagram and table illustrate the mapping of TU-11s into a VC-4. The QT1M provides control bits for enabling the Null Pointer Indicators (NPIs) for the columns indicated.



TU-11 - VC-4 Multiplex Format Mapping

TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	4CH (Port 1), 7CH (Port 2), ACH (Port 3), DCH (Port 4) Registers 6 5 4 3 2 1 0	VC-4 Column Numbers
	0 0 0 0 0 0 0	No TU Selected						
1	0 1 0 0 1 0 0	10 94 178	29	1 0 0 0 1 0 0	11 95 179	57	1 1 0 0 1 0 0	12 96 180
2	0 1 0 1 0 0 0	13 97 181	30	1 0 0 1 0 0 0	14 98 182	58	1 1 0 1 0 0 0	15 99 183
3	0 1 0 1 1 0 0	16 100 184	31	1 0 0 1 1 0 0	17 101 185	59	1 1 0 1 1 0 0	18 102 186
4	0 1 1 0 0 0 0	19 103 187	32	1 0 1 0 0 0 0	20 104 188	60	1 1 1 0 0 0 0	21 105 189
5	0 1 1 0 1 0 0	22 106 190	33	1 0 1 0 1 0 0	23 107 191	61	1 1 1 0 1 0 0	24 108 192
6	0 1 1 1 0 0 0	25 109 193	34	1 0 1 1 0 0 0	26 110 194	62	1 1 1 1 0 0 0	27 111 195
7	0 1 1 1 1 0 0	28 112 196	35	1 0 1 1 1 0 0	29 113 197	63	1 1 1 1 1 0 0	30 114 198
8	0 1 0 0 1 0 1	31 115 199	36	1 0 0 0 1 0 1	32 116 200	64	1 1 0 0 1 0 1	33 117 201
9	0 1 0 1 0 0 1	34 118 202	37	1 0 0 1 0 0 1	35 119 203	65	1 1 0 1 0 0 1	36 120 204
10	0 1 0 1 1 0 1	37 121 205	38	1 0 0 1 1 0 1	38 122 206	66	1 1 0 1 1 0 1	39 123 207
11	0 1 1 0 0 0 1	40 124 208	39	1 0 1 0 0 0 1	41 125 209	67	1 1 1 0 0 0 1	42 126 210
12	0 1 1 0 1 0 1	43 127 211	40	1 0 1 0 1 0 1	44 128 212	68	1 1 1 0 1 0 1	45 129 213
13	0 1 1 1 0 0 1	46 130 214	41	1 0 1 1 0 0 1	47 131 215	69	1 1 1 1 0 0 1	48 132 216
14	0 1 1 1 1 0 1	49 133 217	42	1 0 1 1 1 0 1	50 134 218	70	1 1 1 1 1 0 1	51 135 219
15	0 1 0 0 1 1 0	52 136 220	43	1 0 0 0 1 1 0	53 137 221	71	1 1 0 0 1 1 0	54 138 222
16	0 1 0 1 0 1 0	55 139 223	44	1 0 0 1 0 1 0	56 140 224	72	1 1 0 1 0 1 0	57 141 225
17	0 1 0 1 1 1 0	58 142 226	45	1 0 0 1 1 1 0	59 143 227	73	1 1 0 1 1 1 0	60 144 228
18	0 1 1 0 0 1 0	61 145 229	46	1 0 1 0 0 1 0	62 146 230	74	1 1 1 0 0 1 0	63 147 231
19	0 1 1 0 1 1 0	64 148 232	47	1 0 1 0 1 1 0	65 149 233	75	1 1 1 0 1 1 0	66 150 234
20	0 1 1 1 0 1 0	67 151 235	48	1 0 1 1 0 1 0	68 152 236	76	1 1 1 1 0 1 0	69 153 237
21	0 1 1 1 1 1 0	70 154 238	49	1 0 1 1 1 1 0	71 155 239	77	1 1 1 1 1 1 0	72 156 240
22	0 1 0 0 1 1 1	73 157 241	50	1 0 0 0 1 1 1	74 158 242	78	1 1 0 0 1 1 1	75 159 243
23	0 1 0 1 0 1 1	76 160 244	51	1 0 0 1 0 1 1	77 161 245	79	1 1 0 1 0 1 1	78 162 246
24	0 1 0 1 1 1 1	79 163 247	52	1 0 0 1 1 1 1	80 164 248	80	1 1 0 1 1 1 1	81 165 249
25	0 1 1 0 0 1 1	82 166 250	53	1 0 1 0 0 1 1	83 167 251	81	1 1 1 0 0 1 1	84 168 252
26	0 1 1 0 1 1 1	85 169 253	54	1 0 1 0 1 1 1	86 170 254	82	1 1 1 0 1 1 1	87 171 255
27	0 1 1 1 0 1 1	89 172 256	55	1 0 1 1 0 1 1	89 173 257	83	1 1 1 1 0 1 1	90 174 258
28	0 1 1 1 1 1 1	91 175 259	56	1 0 1 1 1 1 1	92 176 260	84	1 1 1 1 1 1 1	93 177 261
	TUG-3 A			TUG-3 B			TUG-3 C	

MEMORY MAP

The QT1M memory map consists of counters and register bit positions which may be accessed by the microprocessor. The memory map segment consists of FF hex address locations. Addresses that are unused or unlisted register locations must not be accessed by the microprocessor. Unused bit positions within register locations will contain unspecified values when read, unless a 0 or 1 value is indicated in the tables below, or the address has been written by the microprocessor, in which case unused bit positions must always be set to 0. All counters saturate at full count and are cleared when they are read. Reserved registers are put in a state to ensure proper operation when the device is given a power-up reset. The memory map has the following address structure:

Device ID	00H-04H
Reserved	05H-0FH
Common Registers	10H-21H
A Bus	22H-25H
B Bus	26H-29H
Port 1	30H-5FH
Port 2	60H-8FH
Port 3	90H-BFH
Port 4	C0H-EFH
Reserved	F0H-FFH

The common memory map segment consists of the Control, Provisioning, Interrupt Indication, and Interrupt Status registers. The A bus segment consists of the A Drop and Add status registers. The B bus segment consists of the B Drop and Add status registers. Each Port n memory map segment (e.g., Port 1) consists of the Desynchronizer, Provisioning, Status, and Operations registers.

DEVICE ID

Address (Hex)	Status *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	1	1	0	1	0	1	1	1
01	R	1	0	1	1	0	0	0	0
02	R	0	0	0	0	1	0	0	1
03	R	Revision (Version) Level				0	0	0	1
04	R	Mask Level (0000)				Growth (0000)			

* Note: Status codes are R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

Address 00H, bit 0 is a fixed 1 value. The 11-bit field from address 01H, bit 3 (MSB) to address 00H, bit 1 (LSB) contains the binary equivalent of the manufacturer ID assigned to TranSwitch, which is 107 (decimal). The 16-bit field from address 03H, bit 3 (MSB) to address 01H, bit 4 (LSB) contains the binary equivalent of the manufacturer's numeric code assigned to the QT1M device (04251 decimal).

COMMON REGISTERS - CONTROLS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	R/W	MOD1	MOD0	AAHZE	BAHZE	BLOCK	NPIA	NPIB	NPIC
11	R/W	SBTEN	DRPBT	ABD	LATEN	TAISE	TCLKI	RAISE	RCLKI
12	R/W	ADDI	APE	IPOS	INEG	DISRFI	Unused	DPE	PDDO
13	R/W	HEAISE	DV1SEL	DV1REF	RDIEN	Unused	DDIND	UQAE	TOBWZ

COMMON REGISTERS - PROVISIONING

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14	R/W	Unused			UEAME	SE1AIS	V5AL10	PTALTE	HDWIE
15	W	RESET	RESTAB	RESTBB	Unused				

COMMON REGISTERS - INTERRUPT INDICATION

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	R	INT	0	ASIDE	BSIDE	PORT4	PORT3	PORT2	PORT1

COMMON REGISTERS - INTERRUPT STATUS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	R/W	RPT4A	RPT4B	RPT3A	RPT3B	RPT2A	RPT2B	RPT1A	RPT1B
18	R/W	TFIFO4A	TFIFO4B	TFIFO3A	TFIFO3B	TFIFO2A	TFIFO2B	TFIFO1A	TFIFO1B
19	R/W	TPORT4	TPORT3	TPORT2	TPORT1	RFIFO4	RFIFO3	RFIFO2	RFIFO1
21	R/W	0	0	ASMSK	BSMSK	P4MSK	P3MSK	P2MSK	P1MSK

A/B DROP AND ADD BUS REGISTERS - STATUS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
22	R(L)	ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
23	R	ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
24	R(L)	0	0	0	0	0	A3DH4E	A2DH4E	A1DH4E
25	R	0	0	0	0	0	A3DH4E	A2DH4E	A1DH4E
26	R(L)	BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
27	R	BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
28	R(L)	0	0	0	0	0	B3DH4E	B2DH4E	B1DH4E
29	R	0	0	0	0	0	B3DH4E	B2DH4E	B1DH4E

* Note: Status codes are R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

DESYNCHRONIZER CONTROL PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49 79 A9 D9	R/W	Desynchronizer Pointer Leak Rate Register - Port n							

PROVISIONING PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4A 7A AA DA	R/W	TnSEL1	TnSEL0	RnSEL	UCHnE	USCHnE	BYPASn	RnEN	TnB8ZS
4B 7B AB DB	R/W	ADnEN	BDnEN	AAnEN	BAnEN	Unused			
4C 7C AC DC	R/W	Unused	VT/TU Select (VTNn)						
4D 7D AD DD	R/W	Unused							

STATUS REGISTERS PORT n (A SIDE)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30 60 90 C0	R(L)	AnAIS	AnLOP	AnSIZE	AnNDF	AnRDIS	AnRFI	AnUNEQ	AnSLER
31 61 91 C1	R	AnAIS	AnLOP	AnSIZE	AnNDF	AnRDIS	AnRFI	AnUNEQ	AnSLER
32 62 92 C2	R	AnPJ Counter				AnNJ Counter			
33 63 93 C3	R	AnBIP2 Error Counter							
34 64 94 C4	R	AnFEBE Error Counter							
35 65 95 C5	R	Unused					An Rx Label		
4E 7E AE DE	R(L)	AnRDIP	AnRDIC	Unused					
4F 7F AF DF	R	AnRDIP	AnRDIC	Unused					
36 66 96 C6	R	An Receive J2 Byte							
37 67 97 C7	R	An Receive Z6 Byte							
38 68 98 C8	R	An Receive Z7 Byte							
39 69 99 C9	R	An Receive O-Bits							

STATUS REGISTERS PORT n (B SIDE)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3A 6A 9A CA	R(L)	BnAIS	BnLOP	BnSIZE	BnNDF	BnRDIS	BnRFI	BnUNEQ	BnSLER
3B 6B 9B CB	R	BnAIS	BnLOP	BnSIZE	BnNDF	BnRDIS	BnRFI	BnUNEQ	BnSLER
3C 6C 9C CC	R	BnPJ Counter				BnNJ Counter			
3D 6D 9D CD	R	BnBIP2 Error Counter							
3E 6E 9E CE	R	BnFEBE Error Counter							
3F 6F 9F CF	R	Unused					Bn Rx Label		

* Note: Status codes are R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5E 8E BE EE	R(L)	BnRDIP	BnRDIC	Unused					
5F 8F BF EF	R	BnRDIP	BnRDIC	Unused					
40 70 A0 D0	R	Bn Receive J2 Byte							
41 71 A1 D1	R	Bn Receive Z6 Byte							
42 72 A2 D2	R	Bn Receive Z7 Byte							
43 73 A3 D3	R	Bn Receive O-Bits							

STATUS REGISTERS PORT n (A AND B SIDES)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
44 74 A4 D4	R(L)	RnFFE	0	0	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS
45 75 A5 D5	R	RnFFE	0	0	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS
46 76 A6 D6	R	Transmit Port n Coding Violation Counter (Low Byte)							
47 77 A7 D7	R	Transmit Port n Coding Violation Counter (High Byte)							

OPERATIONS REGISTERS PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50 80 B0 E0	R/W	FnLBK	LnLBK	RnAIS	TnAIS	TnVTAIS	TnRFI	TnRDIS	TnRDIP
51 81 B1 E1	R/W	Unused							TnRDIC
52 82 B2 E2	W	RnSETS	RnSETC	Unused				TnFB2	TnFFB
53 83 B3 E3	R/W	Unused					An µP Signal Label		
54 84 B4 E4	R/W	Unused					Bn µP Signal Label		
55 85 B5 E5	R/W	Unused					Tn TX Signal Label		
56 86 B6 E6	R/W	Transmit J2 Byte Value - Port n							
57 87 B7 E7	R/W	Transmit Z6 Byte Value - Port n							
58 88 B8 E8	R/W	Transmit Z7 Byte Value - Port n							
59 89 B9 E9	R/W	Transmit O-Bits - Port n							

* Note: Status codes are R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

MEMORY MAP DESCRIPTIONS

COMMON CONTROL - PROVISIONING DESCRIPTIONS

Address	Bit	Symbol	Description
10	7 6	MOD1 MOD0	**Format Selection:** The format selection is made according to the table given below. MOD1 MOD0 Format (and rate) Selected 0 0 STS-1 Format 0 1 STS-3 Format 1 0 STM-1 AU-3 Format 1 1 STM-1 TUG-3/VC-4 Format
	5	AAHZE	**A Add Bus High Impedance Enable:** A 1 forces the A-side add bus data output to a high impedance state. Upon power-up, or on a hardware or software reset, this bit is set to a 1. Note: For normal bus operation this bit position must be written with a 0.
	4	BAHZE	**B Add Bus High Impedance Enable:** A 1 forces the B-side add bus data output to a high impedance state. Upon power-up, or on a hardware or software reset, this bit is set to a 1. Note: For normal bus operation this bit position must be written with a 0.
	3	BLOCK	**Block Count:** A 1 enables two BIP-2 errors to be counted as a single error (block) for the BIP-2 performance counters (V5 and Z7 bytes). A 0 enables two BIP-2 errors to be counted as two errors.
	2 1 0	NPIA NPIB NPIC	**Null Pointer Indicator Selection:** A 1 enables a null pointer indicator to be generated for one or more of the TUG-3s when control bit MOD1 and MOD0 are a 1 (STM-1 format). A null pointer indicator is carried in the first two bytes of column 1 in a TUG-3. A null pointer indicator is defined as a 1001 in bits 1 through 4, bits 5 and 6 are equal to 0, five ones are in bits 7 through 11, followed by five zeros in bits 12 through 16.
11	7	SBTEN	**Software Bus Timing Enable**: This bit works in conjunction with control bit DRPBT and the $\overline{\text{ABUST}}$ pin according to the following table (where X = Don't Care): SBTEN DRPBT $\overline{\text{ABUST}}$ Action 0 X Low Add bus timing selected. Add bus data derived from add bus timing signals. Software control of bus timing disabled. 0 X High Drop bus timing selected. Add bus data derived from like-named drop bus. Software control of bus timing disabled. 1 0 X Add bus timing selected. Add bus data derived from add bus timing signals. Hardware control of bus timing disabled. 1 1 X Drop bus timing selected. Add bus data derived from like-named drop bus. Hardware control of bus timing disabled. This bit is reset to 0 upon power-up and a device reset.

Address	Bit	Symbol	Description
11 (cont.)	6	DRPBT	**Drop Bus Timing:** Enabled when a 1 is written to control bit SBTEN. A 1 selects the drop bus timing mode, while a 0 selects the add bus timing mode. See table above.
	5	ABD	**Add Bus Delay:** A 0 delays the add bus data with respect to the drop bus by one clock cycle. A 1 delays the add bus data with respect to the drop bus by one additional clock cycle, for a total of two clock cycles. This bit operates in both the drop bus and add bus timing modes.
	4	LATEN	**Latch On Alarm Transitions Enable Bit:** A 1 enables the IPOS and INEG control bits at Address 12H, Bits 5 and 4. A 0 disables the states of the IPOS and INEG control bits, and causes the event alarm bits (latched alarm bits in the registers) to latch on the positive level of an alarm.
	3	TAISE	**Transmit T1 Line AIS Enable:** A common control for all four ports. A 1 enables a T1 AIS (unframed all ones) to be generated and sent when a T1 line input loss of signal, or loss of clock, occurs for port n.
	2	TCLKI	**Transmit T1 Line Clock Inversion:** A common control for the four ports. A 0 enables transmit data to be clocked in on the negative clock edges. A 1 enables data to be clocked in on the positive clock edges.

	1	RAISE	**Receive T1 Line AIS Enable:** A common control for the four ports. A 1 enables a receive T1 AIS to be sent when internal defined alarms occur for port n. A T1 AIS is an unframed all ones signal. For example, receive AIS for port 1 will be generated:
			- When R1SEL is 0 and RAISE is 1 (drop VT from A side)
			  - Loss of pointer detected (A1LOP)
			  - VT AIS detected (A1AIS)
			  - A Drop Bus Loss Of Clock (ADLOC)
			  - A Drop Bus Upstream AIS detected (AnUAISI) when HEAISE is 1.
			  - A Drop H4 Error (AnDH4E) when DV1SEL is 0
			  - Unequipped signal label (A1UNEQ) and UQAE is 1
			  - Mismatch signal label (A1SLER)
			- When R1SEL is 1 and RAISE is 1 (drop VT from B side)
			  - Loss of pointer detected (B1LOP)
			  - VT AIS detected (B1AIS)
			  - B Drop Bus Loss Of Clock (BDLOC)
			  - B Drop Bus Upstream AIS detected (BnUAISI) and HEAISE is 1
			  - B Drop H4 Error (BnDH4E) when DV1SEL is 0
			  - Unequipped signal label (B1UNEQ) and UQAE is 1
			  - Mismatch signal label (B1SLER)
			- Receive FIFO Error (R1FFE) and RAISE is 1
			- A 1 written to send receive AIS (R1AIS)
			The AIS will be sent for one multiframe when a receive FIFO error occurs. The n in AnUAISI, BnUAISI, AnDH4E and BnDH4E represents the STS-1 or TUG in which the VT/TU has been selected.

	0	RCLKI	**Receive T1 Line Clock Inversion:** A common control for the four ports. A 0 enables the T1 receive data signal to be clocked out on positive clock edges. A 1 causes T1 data to be clocked out on negative clock edges.

Address	Bit	Symbol	Description
12	7	ADDI	**Add Indicator Inversion:** A 1 causes the A and B Add bus output indicator signals ($\overline{AADD}$ and $\overline{BADD}$) to be active high instead of active low when a time slot is added to the bus.
	6	APE	**A/B Add Bus Even Parity Generated:** A 1 enables even parity to be generated, while a 0 enables odd parity to be generated. Parity is calculated over the data byte only.
	5 4	IPOS INEG	**Interrupt/Event Positive/Negative Alarm Transition Selection:** An event register bit will latch, and a software interrupt indication will occur, according to the transitions given in the table below. The appropriate interrupt mask bit must be set. A hardware interrupt occurs when the hardware interrupt bit is also enabled (control bit HDWIE is 1). These bits are disabled when a 1 is written to control bit LATEN. IPOS INEG Action 0 0 No event or interrupt indication 1 0 Event and interrupt on positive alarm transition 0 1 Event and interrupt on negative alarm transition 1 1 Event and interrupt on positive and negative alarm transitions
	3	DISRFI	**Disable RFI Interrupt:** A common control bit for all four ports. A 1 disables an RFI indication (bit 4 in V5 of the VT/TU) from causing an interrupt. A 0 enables an RFI indication to cause an interrupt.
	2	Unused	**Unused:** This bit must be written to 0.
	1	DPE	**A/B Drop Bus Even Parity Detected:** This bit works in conjunction with the PDDO control bit to determine the parity calculation in the drop direction. DPE PDDO Action 0 0 Odd parity check over drop data, SPE, and C1J1V1 for both A and B buses. 0 1 Odd parity check over drop data only. 1 0 Even parity check over drop data, SPE, and C1J1V1 for both A and B buses. 1 1 Even parity check over drop data only. Other than reporting the event, no action is taken upon parity error indication.
	0	PDDO	**A/B Drop Bus Parity Detected on Data Only:** Common control bit for both buses. A 1 causes parity to be calculated over the data byte only for both the A and B Drop buses. A 0 causes parity to be calculated over the data byte, SPE and C1J1V1 signals for both buses.
13	7	HEAISE	**A/B H1/H2 or E1 Byte AIS Enable:** Common control for both the A and B Drop buses. A 1 enables an AIS detected in either the SONET/SDH H1/H2 bytes, or in the E1 bytes to generate a receive T1 line AIS and transmit an RDI (when enabled).

Address	Bit	Symbol	Description
13 (cont.)	6	DV1SEL	**Drop Bus V1 Select:** Common control bit for both buses. A 0 selects the H4 byte to be is used as the multiframe indicator. A 1 selects the V1 pulses present in the A and B Drop bus C1J1V1 signals to be used for multiframe alignment.
	5	DV1REF	**Drop Bus V1 Reference Enable:** Common control bit for both buses. Enabled when add bus timing is selected. A 1 enables the V1 pulse from either the drop bus C1J1V1 signal or from the H4 multiframe detector to be used as the V1 reference pulse. The V1 pulse in the AAC1J1V1 and BAC1J1V1 signals is ignored.

	4	RDIEN	**Transmit Remote Defect Indication Enable:** Common control for both the A and B Add buses. A remote payload, server or connectivity defect indication is generated under the conditions described below. These examples apply to port 1, but corresponding examples for ports 2 through 4 may be constructed by substituting the port number digit for the 1-digit in the bit symbols (except DV1SEL).
			- When RDI enable (RDIEN) is 1, a remote payload defect indication is sent for:
			  - A/B Drop H4 Error (A1DH4E, B1DH4E), when DV1SEL is 0
			  - Mismatch signal label (A1SLER, B1SLER)
			- When RDI enable (RDIEN) is 1, a remote server defect indication is sent for:
			  - Loss of Pointer (A1LOP, B1LOP)
			  - VT AIS (A1AIS, B1AIS)
			  - A/B Drop Bus Upstream AIS in H1/H2 or the E1 byte (AnUAISI, BnUAISI), and HEAISE is 1 (where n represents the STS-1 or TUG in which the VT/TU has been selected).
			- When RDI enable (RDIEN) is 1, a remote connectivity defect indication is sent for:
			  - Unequipped signal label (A1UNEQ, B1UNEQ) and UQAE is 1
			- When RDI enable (RDIEN) is 0, the microprocessor can control RDI generation:
			  - Microprocessor writes a 1 to T1RDIS to generate remote server defect indication.
			  - Microprocessor writes a 1 to T1RDIP to generate remote payload defect indication.
			  - Microprocessor writes a 1 to T1RDIC to generate remote connectivity defect indication.
			Note:The microprocessor may send an RDI by writing to the above control bits at any time, including the add only mode. To prevent contention between the internal logic and full microprocessor control, the RDIEN control bit should be written with a 0 when microprocessor control is intended.

	3	Unused	**Unused:** This bit must be written to 0.
	2	DDIND	**Delay Drop Bus Indication Signal:** A 1 increases the delay of the drop bus indication signals ($\overline{\text{ADIND}}$ and $\overline{\text{BDIND}}$) by one additional clock cycle.

Address	Bit	Symbol	Description
13 (cont.)	1	UQAE	**Unequipped Alarm AIS Enable:** A common control for both the A and B Drop buses. A 1 enables a receive T1 line AIS and an RDI to be transmitted when an unequipped alarm is detected in either the A or B Drop bus signals.
	0	TOBWZ	**Transmit Overhead Bytes With Zeros:** A 0 enables bytes written into the memory map by the microprocessor to be transmitted as the J2, Z6, and overhead communications channel bytes for all four ports. A 1 forces the J2, Z6, and overhead communications channel bytes, and the unused bits (bits 1, 2, 3, 4 and 8) in the Z7 byte, to be transmitted as zeros for all four ports.

COMMON REGISTERS - PROVISIONING DESCRIPTIONS

Address	Bit	Symbol	Description
14	7-5	Unused	**Unused:** These bits must be written to 0.
	4	UEAME	**Unequipped Active Multiplex Line Enable:** A 0 enables an unequipped channel or an unequipped supervisory channel to be generated on the inactive bus in Multiplexed Mode only, according to the table given below: Drop Add Action A B Unequipped or unequipped supervisory channel can be transmitted for the VT/TU selected on the A bus. B A Unequipped or unequipped supervisory channel can be transmitted for the VT/TU selected on the B bus. A 1 enables an unequipped channel or unequipped supervisory channel to be transmitted only on the active bus for the VT/TU selected. All other modes (Unidirectional Ring Mode, and Bidirectional Ring Mode) always transmit an unequipped channel or an unequipped supervisory channel on the active bus only. See control bits UCHnE and USCHnE below (Addresses 4A, 7A, AA, and DA) for associated control functions.
	3	SE1AIS	**Select E1AIS:** A 1 disables the TOH H1/H2n AIS detection circuit and enables the AIS detection circuit for the TOH E1n bytes. A 0 enables the AIS detection circuit for the H1/H2n bytes. The n represents the STS-1 signal the VT is being carried in.
	2	V5AL10	**V5 Alarm Detection Select 10:** A 1 selects 10 consecutive RDI assertions for detection and recovery. A 0 selects 5 consecutive RDI assertions for detection and recovery.
	1	PTALTE	**Pointer Tracking AIS to LOP Transition Enabled:** A 1 enables the AIS to LOP transition in the pointer tracking state machine, as required per ETSI standards. A 0 will disable the transition per Bellcore and ANSI standards.
	0	HDWIE	**Hardware Interrupt Enable:** A 1 enables the interrupt pin to be activated when an interrupt occurs, provided the corresponding mask bit is set.

Address	Bit	Symbol	Description
15	7	RESET	**Reset:** A 1 clears all controls (except A and B high impedance bits), alarms, internal counters, performance counters, and re-centers the receive and transmit FIFOs. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	6	RESTAB	**Reset A Side Bus Alarms:** A 1 clears the alarms associated with the A side bus. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	5	RESTBB	**Reset B Side Bus Alarms:** A 1 clears the alarms associated with the B side bus. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	4-0	Unused	**Unused:** These bits must be written to 0.

COMMON REGISTERS - INTERRUPT INDICATION REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
20	7	INT	**Software Interrupt Indication:** A 1 indicates that a positive, negative, or positive and negative alarm transition has occurred. The corresponding interrupt mask bit must be set to 1 for this indication to occur.
	6	Unused	**Unused:** This bit reads out as 0.
	5	ASIDE	**A Side Interrupt Indication:** Enabled when a 1 is written into the AMSK bit. A 1 indicates that an alarm has occurred in one of the A-side alarm registers.
	4	BSIDE	**B Side Interrupt Indication:** Enabled when a 1 is written into the BMSK bit. A 1 indicates that an alarm has occurred in one of the B-side alarm registers.
	3	PORT4	**Port 4 Interrupt Indication:** Enabled when a 1 is written into the P4MSK bit. A 1 indicates that an alarm has occurred in one of the port 4 alarm registers.
	2	PORT3	**Port 3 Interrupt Indication:** Enabled when a 1 is written into the P3MSK bit. A 1 indicates that an alarm has occurred in one of the port 3 alarm registers.
	1	PORT2	**Port 2 Interrupt Indication:** Enabled when a 1 is written into the P2MSK bit. A 1 indicates that an alarm has occurred in one of the port 2 alarm registers.
	0	PORT1	**Port 1 Interrupt Indication:** Enabled when a 1 is written into the P1MSK bit. A 1 indicates that an alarm has occurred in one of the port 1 alarm registers.

COMMON REGISTERS - OPERATIONS DESCRIPTIONS

Address	Bit	Symbol	Description
17	7, 5, 3, 1	RPTnA (n=4-1)	**Receive A Side Status Interrupt Mask Bit:** A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred in an A-side alarm register (mask bits for registers 30, 60, 90, and C0) when PnMSK is set for port n. A 0 disables the A side receive alarms for port n from causing an interrupt.
	6, 4, 2, 0	RPTnB (n=4-1)	**Receive B Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred in a B-side alarm register (mask bits for registers 3A, 6A, 9A, and CA) when PnMSK is set for port n. A 0 disables the B side receive alarms for port n from causing an interrupt**.**
18	7, 5, 3, 1	TFIFOnA (n=4-1)	**Transmit FIFO Error A Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for an A-side transmit FIFO (mask bits for bit 4 in registers 44, 74, A4, and D4) when PnMSK is set for port n. A 0 disables a transmit FIFO error A side alarm for port n from causing an interrupt.
	6, 4, 2, 0	TFIFOnB (n=4-1)	**Transmit FIFO Error B Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for a B-side transmit FIFO (mask bits for bit 3 in registers 44, 74, A4, and D4) when PnMSK is set for port n. A 0 disables a transmit FIFO error B side alarm for port n from causing an interrupt.
19	7, 6, 5, 4	TPORTn (n=4-1)	**Transmit Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for one of the transmit alarms (mask bits for TnLOS (bit 2), TnLOC (bit 1) and TnDAIS (bit 0) in registers 44, 74, A4, and D4) when PnMSK is set for port n. A 0 disables a transmit alarm from causing an interrupt.
	3, 2, 1, 0	RFIFOn (n=4-1)	**Receive FIFO Error Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for a receive FIFO (mask bits for bit 7 in registers 44, 74, A4, and D4) when PnMSK is set for port n. A 0 disables a receive FIFO error alarm for port n from causing an interrupt.

Address	Bit	Symbol	Description
21	7-6	Unused	**Unused:** These bits must be written to 0.
	5	ASMSK	**A Side Interrupt Mask Bit**: A 1 enables the A Side Interrupt Indication (ASIDE).
	4	BSMSK	**B Side Interrupt Mask Bit:** A 1 enables the B Side Interrupt Indication (BSIDE).
	3	P4MSK	**Port 4 Interrupt Mask Bit**: A 1 enables the Port 4 Interrupt Indication (PORT4). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 4, when the corresponding RPT4A, RPT4B, TFIFO4A, TFIFO4B, RFIFO4 or TPORT4 mask bit is set.
	2	P3MSK	**Port 3 Interrupt Mask Bit**: A 1 enables the Port 3 Interrupt Indication (PORT3). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 3, when the corresponding RPT3A, RPT3B, TFIFO3A, TFIFO3B, RFIFO3 or TPORT3 mask bit is set.
	1	P2MSK	**Port 2 Interrupt Mask Bit**: A 1 enables the Port 2 Interrupt Indication (PORT2). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 2, when the corresponding RPT2A, RPT2B, TFIFO2A, TFIFO2B, RFIFO2 or TPORT2 mask bit is set.
	0	P1MSK	**Port 1 Interrupt Mask Bit**: A 1 enables the Port 1 Interrupt Indication (PORT1). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 1, when the corresponding RPT1A, RPT1B, TFIFO1A, TFIFO1B, RFIFO1 TPORT1 mask bit is set.

A/B DROP AND ADD BUS - STATUS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
22	7-0		Same bit definitions as in register 23 hex, except the bits are latched.
23	7	ADLOC	**A Drop Bus Loss Of Clock:** A 1 indicates that the A Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for the equivalent of 1000 ns +/- 500 ns. Recovery occurs on the first clock transition.
	6	AALOC	**A Add Bus Loss Of Clock:** A 1 indicates that the A Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add data and parity bit to a high impedance state, and the add indicator off for the duration of the alarm. An alarm occurs when the input add clock is stuck high or low for 10 or more clock cycles. Recovery occurs on the first clock transition.
	5	ADPAR	**A Drop Bus Parity Error Detected:** A 1 indicates that an even or odd parity error has been detected in the A Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	4-3	Unused	**Unused:** These bits read out as 0.
	2	A3UAISI	**A side Received Upstream AIS Indication - AU-3 C/STS-1 No. 3:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 C/STS-1 No. 3. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E13 byte for AU-3 C/STS-1 No. 3. Disabled when the format is an AU-4 VC-4, or STS-1.
	1	A2UAISI	**A side Received Upstream AIS Indication - AU-3 B/STS-1 No. 2:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 B/STS-1 No. 2. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E12 byte for AU-3 B/STS-1 No. 2. Disabled when the format is an AU-4 VC-4, or STS-1.
	0	A1UAISI	**A side Received Upstream AIS Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 A/STS-1 No. 1, or in the AU-4 VC-4 signal. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E11 byte for AU-3 A/STS-1 No. 1, AU-4 VC-4, or the STS-1 signal.
24	7-0		Same bit definitions as in register 25 hex, except the bits are latched.
25	7-3	Unused	**Unused:** These bits read out as 0.
	2	A3DH4E	**A Drop Bus Loss of H4 Indication - AU-3 C/STS-1 No. 3:** Loss of multiframe for AUG-3 C/STS-1 No. 3 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.

Address	Bit	Symbol	Description
25 (cont.)	1	A2DH4E	**A Drop Bus Loss of H4 Indication - AU-3 B/STS-1 No. 2:** Loss of multiframe for AUG-3 B/STS-1 no. 2 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	0	A1DH4E	**A Drop Bus Loss of H4 Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** Loss of multiframe for AUG-3 A/STS-1 No. 1 or AU-4 VC-4 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This bit is forced to 1 at power-up.
26	7-0		Same bit definitions as in register 27 hex, except the bits are latched.
27	7	BDLOC	**B Drop Bus Loss Of Clock:** A 1 indicates that the B Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for the equivalent of 1000 ns +/- 500 ns. Recovery occurs on the first clock transition.
	6	BALOC	**B Add Bus Loss Of Clock:** A 1 indicates that the B Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add data and parity bit to a high impedance state, and the add indicator off for the duration of the alarm. An alarm occurs when the input drop clock is stuck high or low for 10 or more clock cycles. Recovery occurs on the first clock transition.
	5	BDPAR	**B Drop Bus Parity Error Detected:** A 1 indicates that an even or odd parity error has been detected in the B Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	4-3	Unused	**Unused:** These bits read out as 0.
	2	B3UAISI	**B side Received Upstream AIS Indication - AU-3 C/STS-1 No. 3:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 C/STS-1 No. 3. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E13 byte for AU-3 C/STS-1 No. 3. Disabled when the format is a AU-4 VC-4, or STS-1.
	1	B2UAISI	**B side Received Upstream AIS Indication - AU-3 B/STS-1 No. 2:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 B/STS-1 No. 2. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E12 byte for AU-3 B/STS-1 No. 2. Disabled when the format is a AU-4 VC-4, or STS-1
	0	B1UAISI	**B side Received Upstream AIS Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 A/STS-1 No. 1, or in the AU-4 VC-4 signal. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E11 byte for AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1 signal.

Address	Bit	Symbol	Description
28	7-0		Same bit definitions as in register 29 hex, except the bits are latched.
29	7-3	Unused	**Unused:** These bits read out as 0.
	2	B3DH4E	**B Drop Bus Loss of H4 Indication - AU-3 C/STS-1 No. 3:** Loss of multiframe for AUG-3 C/STS-1 No. 3 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	1	B2DH4E	**B Drop Bus Loss of H4 Indication - AU-3 B/STS-1 No. 2:** Loss of multiframe for AUG-3 B/STS-1 No. 2 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	0	B1DH4E	**B Drop Bus Loss of H4 Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** Loss of multiframe for AUG-3 A/STS-1 No. 1 or AU-4 VC-4 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This bit is forced to 1 at power-up.

PORT n - DESYNCHRONIZER CONTROL REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
49 Port 1 79 Port 2 A9 Port 3 D9 Port 4	7-0	Pointer Leak Rate Value	**Desynchronizer Pointer Leak Rate Register - Port n:** The count written into this location is used for the internal leak rate buffer, and represents the average leak rate. A count of 1 one represents 8 frames, or 2 multiframes, in the rate of occurrence of pointer movements from the number of counts read from the positive and negative stuff counters.

PORT n - PROVISIONING REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
4A Port 1 7A Port 2 AA Port 3 DA Port 4	7 6 5	TnSEL1 TnSEL0 RnSEL	**Transmit Port n A/B Drop/Add Bus Selection:** The table below lists the selection criteria for the eight available modes of operation of port n: TnSEL1 TnSEL0 RnSEL Operating Mode 0 0 0 A Drop only 0 0 1 B Drop only 0 1 0 A Drop A Add 0 1 1 B Drop B Add 1 0 0 A Drop B Add 1 0 1 B Drop A Add 1 1 0 A Drop A and B Add 1 1 1 B Drop B and A Add If a channel is not assigned a VT number, the TnSEL(1-0) bits for that channel must be set to 00.
	4	UCHnE	**Unequipped Channel for Port n Enabled:** The UCHnE control bit works in conjunction with the USCHnE control bit (in bit position 3) according to the following table: UCHnE USCHnE Action 0 X Normal Operation. 1 0 Unequipped VT/TU generated. An unequipped VT/TU consists of a normal NDF, size bits equal to 11, a fixed pointer equal to 78, and all other bytes equal to 0. 1 1 Unequipped supervisory VT/TU generated. An unequipped supervisory VT/TU consists of a normal NDF, size bits equal to 11, a fixed pointer equal to 78, and a valid J2 byte. The V5 byte will consist of a valid BIP-2, with zeros in the signal label and in the other bits. The Z6 and Z7 bytes, and the other bytes, will be equal to 00H. Note: X = don't care (0 or 1). See the UEAME bit description and the Unequipped Payload Generation section for further explanation.
	3	USCHnE	**Unequipped Supervisory Channel for Port n Enabled:** Works in conjunction with the UCHnE bit according to the table given above. See the UEAME bit description and the Unequipped Payload Generation section for further explanation.
	2	BYPASn	**Bypass CODEC of Port n:** A 1 disables the AMI/B8ZS CODEC (coder and decoder) of port n for NRZ operation. This bit also works in conjunction with the TnB8ZS control bit, according to the following table: BYPASn TnB8ZS Action 0 0 AMI CODEC function enabled. Rail interface selected for the receive and transmit ports. 0 1 B8ZS CODEC function enabled. Rail interface selected for the receive and transmit ports. 1 X AMI/B8ZS CODEC function disabled. NRZ interface selected for the receive and transmit ports. Note: X = don't care (0 or 1).

Address	Bit	Symbol	Description
4A Port 1 7A Port 2 AA Port 3 DA Port 4 (cont.)	1	RnEN	**Receive Port n Enable:** A 1 enables the receive data (NRZ or rail) output and clock output for port n when pin QUIETn is low. A 0 forces the data and clock output pins to a high impedance state. The four bits power up and are reset to 0. A 1 must be written to these control bits to enable the port T1 outputs.
	0	TnB8ZS	**Port n B8ZS CODEC Enable:** A 1 enables the B8ZS CODEC function for port n. A 0 enables the AMI CODEC function for port n. Also refer to the table given for BYPASn.
4B Port 1 7B Port 2 AB Port 3 DB Port 4	7	ADnEN	**A Side Drop Bus Port n VT/TU Selection Output Enable:** A 1 enables the drop bus $\overline{\text{ADIND}}$ signal output. This signal will be active low for the time slots corresponding to the VT/TU selected for port n.
	6	BDnEN	**B Side Drop Bus Port n VT/TU Selection Output Enable**: A 1 enables the drop bus $\overline{\text{BDIND}}$ signal output. This signal will be active low for the time slots corresponding to the VT/TU selected for port n.
	5	AAnEN	**A Side Add Bus Port n VT/TU Selection Output Enable:** A 1 enables the add bus $\overline{\text{AAIND}}$ signal output. This signal will be active low for the time slots corresponding to the VT/TU selected for port n.
	4	BAnEN	**B Side Add Bus Port n VT/TU Selection Output Enable:** A 1 enables the add bus $\overline{\text{BAIND}}$ signal output. This signal will be active low for the time slots corresponding to the VT/TU selected for port n.
	3-0	Unused	**Unused:** These bits must be written to 0.
4C Port 1 7C Port 2 AC Port 3 DC Port 4	7	Unused	**Unused:** This bit must be written to 0.
	6-0	VTNn	**VT/TU Selection for Port n:** The seven-bit code binary code written into this location selects the VT/ TU that is to be dropped from the A or B-side drop bus, and added to the A or B-side add bus. If no VT/TU is selected, the microprocessor should either write a 1 to control bit RnAIS thereby forcing a T1 AIS, or should write a 0 to RnEN, which will tristate the port n data and clock output pins. In this case, the TnSEL(1-0) bits should be set to 00 to disable any data being added to the bus from the unassigned port.

PORT n - RECEIVE STATUS REGISTER DESCRIPTIONS

The following descriptions pertain to the status registers assigned to port n, where n = 1 to 4. There are two readable bit positions per alarm. One bit (in an odd-numbered address) indicates the detected alarm as unlatched. The second bit (in the preceding even-numbered address) provides the alarm status as an latched alarm indication. A latched bit position is set on a positive, negative, or positive/negative transition of the alarm, or a positive level of the alarm. A latched alarm is cleared on a microprocessor read cycle of its address. During a read cycle, internal logic holds any increment to a counter until the read cycle is complete, and then updates the counter afterwards.

Address	Bit	Symbol	Description
30 Port 1 60 Port 2 90 Port 3 C0 Port 4	7-0	Latched An Alarms	Same alarms as the following address locations, except these alarm states are latched.
31 Port 1 61 Port 2 91 Port 3 C1 Port 4	7	AnAIS	**A Drop Bus Port n VT/TU AIS Alarm:** A 1 indicates that an AIS has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	6	AnLOP	**A Drop Bus Port n Loss Of VT/TU Pointer Alarm:** A 1 indicates that a loss of pointer has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	5	AnSIZE	**A Drop Bus Port n VT/TU Pointer Size Error Indication:** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 11 for the VT/TU selected. The detection and recovery time is immediate.
	4	AnNDF	**A Drop Bus Port n New Data Flag Indication:** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the VT/TU selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit).
	3	AnRDIS	**A Drop Bus Port n Remote Server Defect Indication:** A 1 indicates that either a remote server defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 101), or an RDI has been detected coming from older equipment (bit 8 in V5 equals 1 when bits 6 and 7 in Z7 are equal to 00 or 11). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	AnRFI	**A Drop Bus Port n Remote Failure Indication:** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the VT/TU selected. The detection and recovery time is immediate.
	1	AnUNEQ	**A Drop Bus Port n Unequipped Indication:** A 1 indicates that an Unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 = 0) for the VT/TU selected in the A side drop bus. An unequipped signal label is equal to 000. Five or more consecutive received unequipped signal labels will cause this alarm. Recovery occurs when five or more consecutive signal labels are received not equal to 000. The following alarms will not cause an unequipped indication: - H4 alarm (AnDH4E) when DV1SEL is 0. - Loss of pointer alarm (AnLOP) - VT/TU AIS alarm (AnAIS) - Upstream AIS detected (AnAISI) when HEAISE is 1 (n is the STS-1 or AU-3 identifier).

Address	Bit	Symbol	Description
31 Port 1 61 Port 2 91 Port 3 C1 Port 4 (cont.)	0	AnSLER	**A Drop Bus Port n Signal Label Mismatch Indication:** A 1 indicates that the receive signal label (Bits 5-7 in V5) does not match the microprocessor-written signal label in the VT/TU selected for the A side drop bus. Five or more consecutive signal label mismatches (against the microprocessor-written value), or received labels not equal to 001, results in an alarm. Recovery occurs upon receipt of five or more consecutive correct signal labels, or 001 values. The following alarms will not cause a signal label mismatch indication: - All zeros (unequipped) or AIS (all ones) - H4 alarm (AnDH4E) when DV1SEL is 0. - Loss of pointer alarm (AnLOP) - VT/TU AIS alarm (AnAIS) - Upstream AIS detected (AnAISI) when HEAISE is 1 (n is the STS-1 or AU-3 identifier).
32 Port 1 62 Port 2 92 Port 3 C2 Port 4	7-4	AnPJ Counter	**A Drop Bus Port n Positive Pointer Justification Counter:** A four-bit counter that increments on a positive pointer movement for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
	3-0	AnNJ Counter	**A Drop Bus Port n Negative Pointer Justification Counter:** A four-bit counter that increments on a negative pointer movement for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
33 Port 1 63 Port 2 93 Port 3 C3 Port 4	7-0	AnBIP2 Error Counter	**A Drop Bus Port n BIP-2 Error Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the VT/TU selected. A maximum of two errors can occur each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.
34 Port 1 64 Port 2 94 Port 3 C4 Port 4	7-0	AnFEBE Error Counter	**A Drop Bus Port n FEBE Error Counter:** An 8-bit counter which counts the number of FEBE errors received (Bit 3 in V5 = 1) for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
35 Port 1 65 Port 2 95 Port 3 C5 Port 4	7-3	Unused	**Unused:** These bits read out as 0.
	2-0	An Rx Label	**A Drop Bus Port n Received Signal Label**: The three bit positions correspond to the three signal label bits in bits 5 through 7 in V5 in the VT/TU selected. This location is updated every 500 microseconds. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for an unequipped and mismatch indication. Code 1 (001) has been implemented in hardware and does not have to be written into this location.
4E Port 1 7E Port 2 AE Port 3 DE Port 4	7-0	Latched An Alarms	Same alarms as the corresponding address 4F, 7F, AF, DF bit positions, except that these alarms are latched.

Address	Bit	Symbol	Description
4F Port 1 7F Port 2 AF Port 3 DF Port 4	7	AnRDIP	**A Drop Bus Port n Remote Payload Defect Indication:** A 1 indicates that a remote payload defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 010). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	6	AnRDIC	**A Drop Bus Port n Remote Connectivity Defect Indication:** A 1 indicates that a remote connectivity defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 110). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	5-0	Unused	**Unused:** These bits read out as 0.
36 Port 1 66 Port 2 96 Port 3 C6 Port 4	7-0	An Receive J2 Byte	**A Drop Bus Port n J2 Byte**: The eight bits in this register position correspond to the J2 byte received in the VT/TU selected. Bit 7 corresponds to bit 1 in the J2 byte.
37 Port 1 67 Port 2 97 Port 3 C7 Port 4	7-0	An Receive Z6 Byte	**A Drop Bus Port n Z6 Byte**: The eight bits in this register position correspond to the Z6 byte received in the VT/TU selected. Bit 7 corresponds to bit 1 in the Z6 byte.
38 Port 1 68 Port 2 98 Port 3 C8 Port 4	7-0	An Receive Z7 Byte	**A Drop Bus Port n Z7 Byte**: The eight bits in this register position correspond to the Z7 byte received in the VT/TU selected. Bit 7 corresponds to bit 1 in the Z7 byte.
39 Port 1 69 Port 2 99 Port 3 C9 Port 4	7-0	An Receive O-Bits	**A Drop Bus Port n O-bits**: The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits received in the VT/TU selected. Bit 7 corresponds to bit 3 in the second justification control byte, while bit 0 corresponds to bit 6 in the first justification control byte. The two nibbles written into this register location will be from the same frame.
3A Port 1 6A Port 2 9A Port 3 CA Port 4	7-0	Latched Bn Alarms	Same alarms as the following address locations, except these alarm states are latched.
3B Port 1 6B Port 2 9B Port 3 CB Port 4	7	BnAIS	**B Drop Bus Port n VT/TU AIS Alarm:** A 1 indicates that an AIS has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	6	BnLOP	**B Drop Bus Port n Loss Of VT/TU Pointer Alarm:** A 1 indicates that a loss of pointer has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	5	BnSIZE	**B Drop Bus Port n Pointer Size Error Indication:** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 11 for the VT/TU selected. The detection and recovery time is immediate.
	4	BnNDF	**B Drop Bus Port n New Data Flag Indication:** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the VT/TU selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit).

Address	Bit	Symbol	Description
3B Port 1 6B Port 2 9B Port 3 CB Port 4 (cont.)	3	BnRDIS	**B Drop Bus Port n Remote Server Defect Indication:** A 1 indicates that either a remote server defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 101), or an RDI has been detected coming from older equipment (bit 8 in V5 equals 1 when bits 6 and 7 in Z7 are equal to 00 or 11). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	BnRFI	**B Drop Bus Port n Remote Failure Indication:** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the VT/TU selected. The detection and recovery time is immediate.
	1	BnUNEQ	**B Drop Bus Port n Unequipped Indication:** A 1 indicates that an Unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 = 0) for the VT/TU selected in the B side drop bus. An unequipped signal label is equal to 000. Five or more consecutive received unequipped signal labels will cause this alarm. Recovery occurs when five or more consecutive signal labels are received not equal to 000. The following alarms will not cause an unequipped indication: - H4 alarm (BnDH4E) when DV1SEL is 0. - Loss of pointer alarm (BnLOP) - VT/TU AIS alarm (BnAIS) - Upstream AIS detected (BnAISI) when HEAISE is 1 (n is the STS-1 or AU-3 identifier).
	0	BnSLER	**B Drop Bus Port n Signal Label Mismatch Indication:** A 1 indicates that the receive signal label (Bits 5-7 in V5) does not match the microprocessor-written signal label in the VT/TU selected for the B side drop bus. Five or more consecutive signal label mismatches (against the microprocessor-written value), or received labels not equal to 001, results in an alarm. Recovery occurs upon receipt of five or more consecutive correct signal labels, or 001 values. The following alarms will not cause a signal label mismatch indication: - All zeros (unequipped) or AIS (all ones) - H4 alarm (BnDH4E) when DV1SEL is 0. - Loss of pointer alarm (BnLOP) - VT/TU AIS alarm (BnAIS) - Upstream AIS detected (BnAISI) when HEAISE is 1 (n is the STS-1 or AU-3 identifier).
3C Port 1 6C Port 2 9C Port 3 CC Port 4	7-4	BnPJ Counter	**B Drop Bus Port n Positive Pointer Justification Counter:** A four-bit counter that increments on a positive pointer movement for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
	3-0	BnNJ Counter	**B Drop Bus Port n Negative Pointer Justification Counter:** A four-bit counter that increments on a negative pointer movement for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
3D Port 1 6D Port 2 9D Port 3 CD Port 4	7-0	BnBIP2 Error Counter	**B Drop Bus Port n BIP-2 Error Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the VT/TU selected. A maximum of two errors can occur each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.

Address	Bit	Symbol	Description
3E Port 1 6E Port 2 9E Port 3 CE Port 4	7-0	BnFEBE Error Counter	**B Drop Bus Port n FEBE Error Counter:** An 8-bit counter which counts the number of FEBE errors received (Bit 3 in V5 = 1) for the VT/TU selected. The counter saturates at full count and is cleared when it is read.
3F Port 1 6F Port 2 9F Port 3 CF Port 4	7-3	Unused	**Unused:** These bits read out as 0.
	2-0	Bn RX Label	**B Drop Bus Port n Received Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5 for the VT/TU selected. This location is updated every 500 microseconds. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for an unequipped and mismatch indication. Code 1 (001) has been implemented in hardware and does not have to be written into this location.
5E Port 1 8E Port 2 BE Port 3 EE Port 4	7-0	Latched Bn Alarms	Same alarms as the corresponding address 5F, 8F, BF, EF bit positions except that these alarms are latched.
5F Port 1 8F Port 2 BF Port 3 EF Port 4	7	BnRDIP	**B Drop Bus Port n Remote Payload Defect Indication:** A 1 indicates that a remote payload defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 010). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	6	BnRDIC	**B Drop Bus Port n Remote Connectivity Defect Indication:** A 1 indicates that a remote connectivity defect alarm has been detected (bits 5, 6 and 7 in Z7 are equal to 110). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	5-0	Unused	**Unused:** These bits read out as 0.
40 Port 1 70 Port 2 A0 Port 3 D0 Port 4	7-0	Bn Receive J2 Byte	**B Drop Bus Port n J2 Byte:** The eight bits in this register position correspond to the J2 byte received for the VT/TU selected. Bit 7 corresponds to bit 1 in the J2 byte.
41 Port 1 71 Port 2 A1 Port 3 D1 Port 4	7-0	Bn Receive Z6 Byte	**B Drop Bus Port n Z6 Byte:** The eight bits in this register position correspond to the Z6 byte received for the VT/TU selected. Bit 7 corresponds to bit 1 in the Z6 byte.
42 Port 1 72 Port 2 A2 Port 3 D2 Port 4	7-0	Bn Receive Z7 Byte	**B Drop Bus Port n Z7 Byte:** The eight bits in this register position correspond to the Z7 byte received for the VT/TU selected. Bit 7 corresponds to bit 1 in the Z7 byte.
43 Port 1 73 Port 2 A3 Port 3 D3 Port 4	7-0	Bn Receive O-Bits	**B Drop Bus Port n O-bits:** The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits received for the VT/TU. Bit 7 corresponds to bit 3 in the second justification control byte, while bit 0 corresponds to bit 6 in the first justification control byte. The two nibbles written into this register location will be from the same frame.
44 Port 174 Port 2 A4 Port 3 D4 Port 4	7-0	Latched Tx Alarms	Same alarms as the following address locations, except these alarm states are latched.

Address	Bit	Symbol	Description
45 Port 1 75 Port 2 A5 Port 3 D5 Port 4	7	RnFFE	**Receive Port n FIFO Error:** A 1 indicates that the receive FIFO for port 1 has overflowed or underflowed. The FIFO is reset automatically. Other than an alarm indication, no action is taken.
	6-5	Unused	**Unused:** These bits read out as 0.
	4	TAnFE	**Transmit A Add Bus Port n FIFO Error:** A 1 indicates that the A Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two frames automatically.
	3	TBnFE	**Transmit B Add Bus Port n FIFO Error:** A 1 indicates that the B Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two frames automatically.
	2	TnLOS	**Transmit Port n Loss Of Signal:** An alarm occurs when there are no signal transitions detected on the positive rail or negative rail for a period of 175 +/- 75 consecutive pulse positions. Recovery occurs when the average pulse density of at least 12.5% occurs over a period of 175 +/- 75 consecutive pulse positions. For an NRZ signal, this alarm is active when a low occurs on the external transmit loss of signal indication pin which is shared with the TNIn pin.
	1	TnLOC	**Transmit Port n Loss Of Clock:** A 1 indicates that the transmit clock (TCIn) for port n is stuck high or low for 10 or more clock cycles. Recovery occurs on the first clock transition.
	0	TnDAIS	**Transmit Port n AIS Detected:** A 1 indicates that line AIS (unframed all ones) has been detected in the bit stream for port n. Other than reporting the alarm, no action is taken.
46 Port 1 76 Port 2 A6 Port 3 D6 Port 4	7-0	Coding Violation Counter Low Order Byte	**Transmit Port n Coding Violation Counter:** Low order byte of a 16-bit saturating counter which counts the number of coding violations that have occurred in the AMI/B8ZS line code. During a read cycle internal logic holds any new count until the read cycle is complete, and then the counter is updated. This counter is cleared on reset pulse, reset counter control bit = 1, or when it is read.
47 Port 1 77 Port 2 A7 Port 3 D7 Port 4	7-0	Coding Violation Counter High Order Byte	**Transmit Port n Coding Violation Counter:** High order byte of an 16-bit saturating counter which counts the number of coding violations that have occurred in the AMI/B8ZS line codes. During a read cycle internal logic holds any new count until the read cycle is complete, and then the counter is updated. This counter is cleared on reset pulse, reset counter control bit = 1, or when it is read.

PORT n - OPERATIONS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
50 Port 1 80 Port 2 B0 Port 3 E0 Port 4	7	FnLBK	**Facility Loopback:** A 1 enables a T1 facility (side) loopback for port n. The T1 transmit clock and data output signals are looped back as the T1 receive clock and data signals. The T1 receive input signals are disabled. The T1 transmit clock and data output signals are provided at the interface.
	6	LnLBK	**Line Loopback:** A 1 enables a T1 line (side) loopback for port n. The receive T1 clock and data output signals are looped back as the T1 transmit signal. The T1 transmit clock and data input signals are disabled. The T1 receive clock and data output signals are provided at the interface.
	5	RnAIS	**Send Receive T1 Line AIS for Port n:** A 1 enables a T1 AIS (unframed all ones signal) to be inserted into the receive data stream for port n independent of the status of the internal alarms.
	4	TnAIS	**Transmit T1 Line AIS for Port n:** A 1 enables a T1 AIS (unframed all ones signal) to be inserted into the transmit data stream for port n independent of the status of the internal alarms.
	3	TnVTAIS	**Transmit VT AIS for the VT/TU Selected for Port n:** A 1 enables a VT/TU AIS to be transmitted for the VT/TU selected. A VT/TU AIS consists of all ones in the entire VT/TU, including bytes V1 through V4.
	2	TnRFI	**Transmit Port n RFI (Remote Failure Indication):** A 1 enables an RFI alarm to be transmitted (bit 4 in the V5 byte is set to 1).
	1	TnRDIS	**Transmit Port n RDIS (Remote Server Defect Indication):** A 1 enables an RDIS to be transmitted (bit 8 in the V5 byte is set to 1, and bits 5, 6 and 7 in the Z7 byte are set to 101). Neither the TnRDIP nor the TnRDIC bit should be set while bit TnRDIS is set.
	0	TnRDIP	**Transmit Port n RDIP (Remote Payload Defect Indication):** A 1 enables an RDIP to be transmitted (bit 8 in the V5 byte is set to 0, and bits 5, 6 and 7 in the Z7 byte are set to 010). Neither the TnRDIS nor the TnRDIC bit should be set while bit TnRDIP is set.
51 Port 1 81 Port 2 B1 Port 3 E1 Port 4	7-1	Unused	**Unused:** These bits must be written to 0.
	0	TnRDIC	**Transmit Port n RDIC (Remote Connectivity Defect Indication):** A 1 enables an RDIC to be transmitted (bit 8 in the V5 byte is set to 1, and bits 5, 6 and 7 in the Z7 byte are set to 110). Neither the TnRDIS nor the TnRDIP bit should be set while bit TnRDIC is set.
52 Port 1 82 Port 2 B2 Port 3 E2 Port 4	7	RnSETS	**Reset Port n Selected Functions:** A 1 will clear the alarms, reset the performance counters to 0, and re-center the FIFOs associated with port n. The control bits for port n are not reset. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	6	RnSETC	**Reset Port n Performance Counters:** A 1 resets the performance counters to 0 for port n. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.

Address	Bit	Symbol	Description
52 Port 1 82 Port 2 B2 Port 3 E2 Port 4 (cont.)	5-2	Unused	**Unused:** These bits must be written to 0.
	1	TnFB2	**Transmit Port n BIP-2 Error Mask (Force BIP-2 Error):** A 1 causes bits 1 and 2 (the BIP-2 value) in the V5 byte to be inverted from the calculated value and transmitted for one frame. This bit is self-clearing, and will reset to 0 after the single error is transmitted.
	0	TnFFB	**Transmit Port n FEBE Error Mask (Force FEBE Error):** A 1 causes bit 3 (the FEBE value) of the V5 byte to be transmitted as a 1. This control bit is self-clearing, and will reset to 0 after the V5 byte has been transmitted. Please note that if an internal FEBE is being sent, the error is sent after the last FEBE indication is sent.
53 Port 1 83 Port 2 B3 Port 3 E3 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	AnUPSL	**A Drop Bus Port n Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the VT/TU selected. Bit 2 in this register corresponds to bit 7 in the V5 byte. The bits written into this register are compared against the received signal for a mismatch signal label alarm.
54 Port 1 84 Port 2 B4 Port 3 E4 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	BnUPSL	**B Drop Bus Port n Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the VT/TU selected. Bit 2 in this register corresponds to bit 7 in the V5 byte. The bits written into this register are compared against the received signal for a mismatch signal label alarm.
55 Port 1 85 Port 2 B5 Port 3 E5 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	Tn TX Label	**Transmit Port n Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the VT/TU selected for transmission. Bit 2 in this register corresponds to bit 7 in the V5 byte.
56 Port 1 86 Port 2 B6 Port 3 E6 Port 4	7-0	Transmit J2 Byte Value	**Transmit J2 Value Port n:** The value written into this register is transmitted when control bit TOBWZ is 0. Bit 7 corresponds to bit 1 in the J2 byte.
57 Port 1 87 Port 2 B7 Port 3 E7 Port 4	7-0	Transmit Z6 Byte Value	**Transmit Z6 Value Port n:** The value written into this register is transmitted when control bit TOBWZ is 0. Bit 7 corresponds to bit 1 in the Z6 byte.
58 Port 1 88 Port 2 B8 Port 3 E8 Port 4	7-0	Transmit Z7 Byte Value	**Transmit Z7 Value Port n:** The value written into bits 7, 6, 5, 4 and 0 in this register is transmitted when control bit TOBWZ is 0. Bits 3, 2, and 1 are assigned for the RDI indicators and cannot be written to in this register. Bit 7 corresponds to bit 1 in the Z7 byte.
59 Port 1 89 Port 2 B9 Port 3 E9 Port 4	7-0	Transmit O-bits	**Transmit O Bits Port n:** The value written into this register is transmitted when control bit TOBWZ is 0. Bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte. Bits 3 through 0 correspond to bits 3 through 6 in the first justification control byte.

PACKAGE INFORMATION

The QT1M device is packaged in a 160-pin plastic quad flat package (PQFP) suitable for surface mounting, as illustrated in Figure 17.

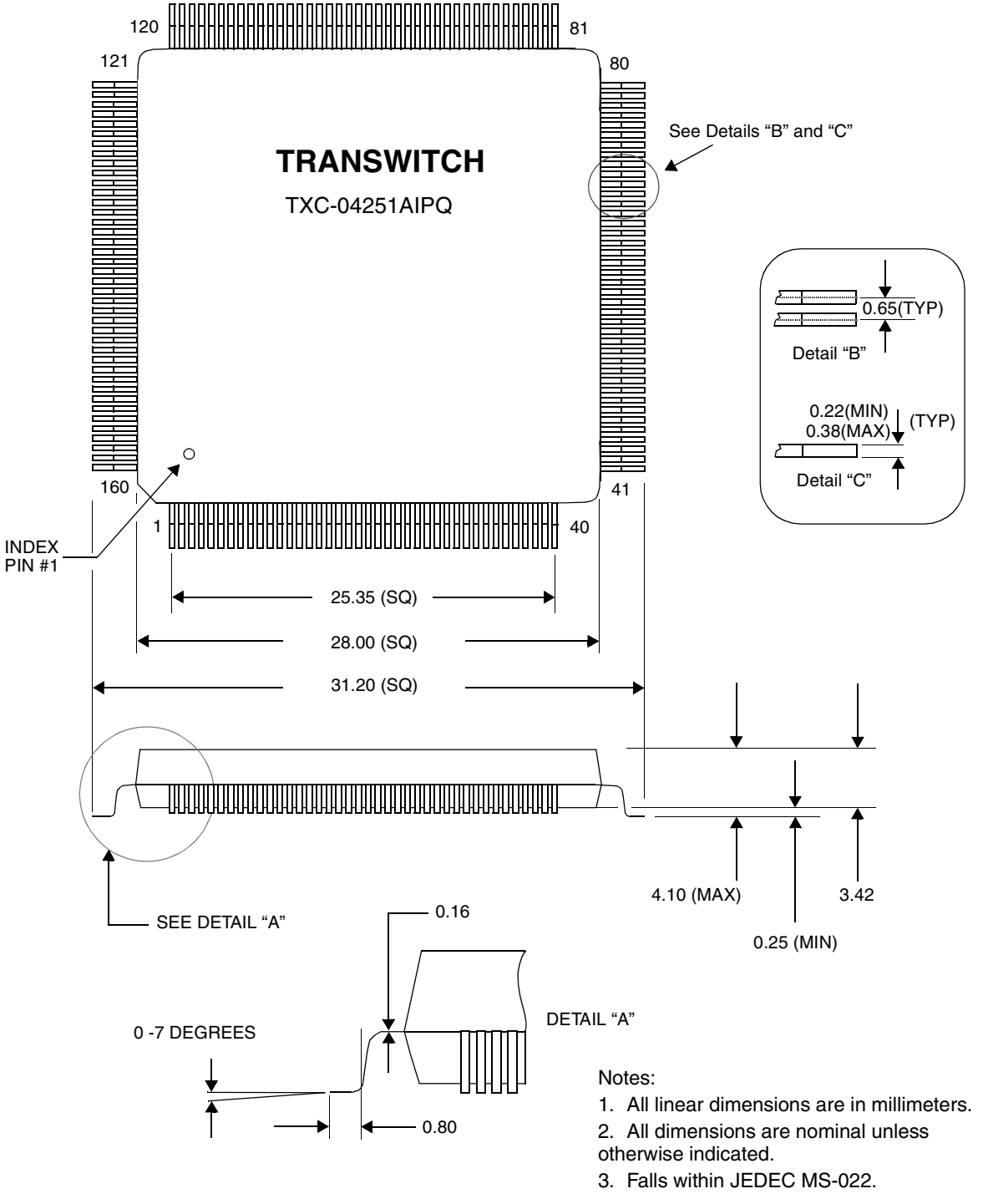


Figure 17. QT1M TXC-04251 160-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-04251AIPQ 160-pin plastic quad flat package (PQFP)

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus extended features.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). In a single device, it provides the SONET interface to any payload. Provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal.

TXC-03003B SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line, and path overhead processing for a STS-3/STS-3c/STM-1 signal. Compliant with ANSI and ITU-TSS standards.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-lead TXC-03001B SOT-1 devices, and it has a 144-lead package.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line.

TXC-03108, T1Fx8 VLSI Device (8-Channel T1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). Maps seven 1.544 Mbit/s DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 virtual tributaries carried in a SONET or SDH synchronous payload envelope.

TXC-05132, MCHDLC VLSI Device (Multi-Channel HDLC Controller). The MCHDLC VLSI device is designed to send and receive packets over 256 link channels using eight serial interfaces, each operating independently at the T1/DS1, E1 or MVIP rates, or at an unchannelized rate. It operates from a power supply of 3.3 volts.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides features similar to those of the TXC-03011 SOT-1E device, but it operates from a power supply of 3.3 volts rather than 5 volts.

TXC-06103, PHAST-3N VLSI Device (SONET STM-1, STS-3 or STS-3c Overhead Terminator). This PHAST-3N VLSI device provides a Telecom Bus interface for downstream devices. It operates from a power supply of 3.3 volts.

TXC-06112, PHAST-12 VLSI Device (Four-channel SONET STS-3c or STM-1 Overhead Terminator). This PHAST-12 VLSI device provides programmable, high performance ATM/Packet/Transmission for Level 12 applications and operates from a power supply of 3.3 volts.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: 650-949-6700
Fax: 650-949-6705
Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79
Web:
www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698
Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: 800-854-7179 (within U.S.A.)
Tel: 314-726-0444 (outside U.S.A.)
Fax: 314-726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)	Tel: 800-669-6857 (within U.S.A.) Tel: 903-769-3717 (outside U.S.A.)
3220 N Street NW, Suite 360	Fax: 508-650-1375
Washington, DC 20007	Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union	Tel: 22 730 5111
Telecommunication Standardization Sector	Fax: 22 733 7256
Place des Nations, CH 1211	Web: www.itu.int
Geneve 20, Switzerland	

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk	Tel: 215-697-2179
Building 4 / Section D	Fax: 215-697-1462
700 Robbins Avenue	Web: www.dodssp.daps.mil
Philadelphia, PA 19111-5094	

PCI SIG (U.S.A.):

PCI Special Interest Group	Tel: 800-433-5177 (within U.S.A.)
2575 NE Kathryn Street #17	Tel: 503-693-6232 (outside U.S.A.)
Hillsboro, OR 97124	Fax: 503-693-8344
	Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.	Tel: 800-521-CORE (within U.S.A.)
Attention - Customer Service	Tel: 908-699-5800 (outside U.S.A.)
8 Corporate Place	Fax: 908-336-2559
Piscataway, NJ 08854	Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee	Tel: 3 3432 1551 Fax: 3 3432 1553
2nd Floor, Hamamatsucho - Suzuki Building,	Web: www.ttc.or.jp
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo	

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated QT1M Data Sheet that have significant differences relative to the previous and now superseded QT1M Data Sheet:

Updated QT1M Data Sheet: Edition 4, March 2000

Previous QT1M Data Sheet: Edition 3, December 1997

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
2	Added 'Unequipped Payload Generation' section at page 32.
9-10	On page 10, deleted Pins No. 2 and 121 for Symbol NC and added these two pins to the Symbol Reserved row. Deleted Note 1. Made corresponding changes to Figure 3 on page 9.
16	Added second sentence to Name/Function column for Symbol $\overline{TRS}$, to specify a power-up initialization requirement.
17	Removed Operating Junction Temperature row from first table. Moved Ambient Operating Temperature row to first table from last table. Changed ESD Classification row and added Note 3 for first table. Reduced Max value of thermal resistance in second table from 41.4 to 23.0. Renamed last table.
22-23	Added signal 'A/BDPAR' for second waveform and 'A/BAPAR' for sixth waveform in Figures 6 and 7, and added sentence about data delay to Notes. Added 'DPAR' in Parameter for Symbols $t_{SU(1)}$, $t_{H(1)}$ and 'APAR' for Symbols $t_{OD(2)}$, $t_{OD(3)}$ in tables.
24-25	Added signal 'A/BAPAR' to fourth waveform in Figures 8 and 9. Added 'APAR' in Parameter for Symbols $t_{OD(2)}$ and $t_{OD(3)}$ in tables.
30-31	Added last sentence in first paragraph.
32	Added 'Unequipped Payload Generation' section.
43	Added '(when RDIEN=0)' in first row and '(when RDIEN=1)' in second row for Definition column of RDI Bit Assignment table.
50	Added 'Boundary Scan Reset' section before Figure 16.
67	Changed first sentence and added last sentence of Description for Symbol ABD.
70	Changed Description for Symbol UEAME.
76	Added last sentence to Description for Symbols TnSEL1, TnSEL0, and RnSEL. Added last sentence to Description for Symbols UCHnE and USCHnE.
77	Added last sentence to Description for Symbol VTNn.
86	Deleted reference to socket mounting. Changed Note 3 and dimension for package height to 4.10 from 4.07 in Figure 17.
87	Updated Related Products section.
88-89	Made extensive changes to Standards Documentation Sources section.
90	Replaced List of Data Sheet Changes section to show changes from Ed. 3 to Ed. 4.
93	Updated Documentation Update Registration Form.

- NOTES -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Please complete the registration form on this back cover sheet, and fax or mail it, if you wish to receive updated documentation on this TranSwitch product as it becomes available.