www.DataSheet4U.com

CUBIT-622™ Device
Multi-PHY *CellBus*® Access Device
TXC-05805

DATA SHEET

FEATURES

- 622 Mbit/s performance
- UTOPIA Level 1/2 interface (8/16-bit) with support for 64 ports
- Tandem operation for two devices, supporting dual *CellBus* cell switching in load sharing or redundancy
- Inlet-side address translation and routing header insertion
- Programmable OAM cell routing
- Outlet cell queuing, using external synchronous SRAM (SSRAM) cell buffer
- Support for spatial multicast for 256 sessions
- Support for packet discard in outlet direction
- Support for over-reservation of all VBR and UBR/GFR traffic
- *CellBus* traffic monitor mode
- Cell insertion and extraction via microprocessor interface port
- Microprocessor control port, selectable for Intel or Motorola interfaces
- Test Access Port for IEEE 1149.1 Boundary Scan
- +3.3 V and +2.5 V power supplies
- 376-lead Plastic Ball Grid Array (PBGA) package, 23 mm x 23 mm

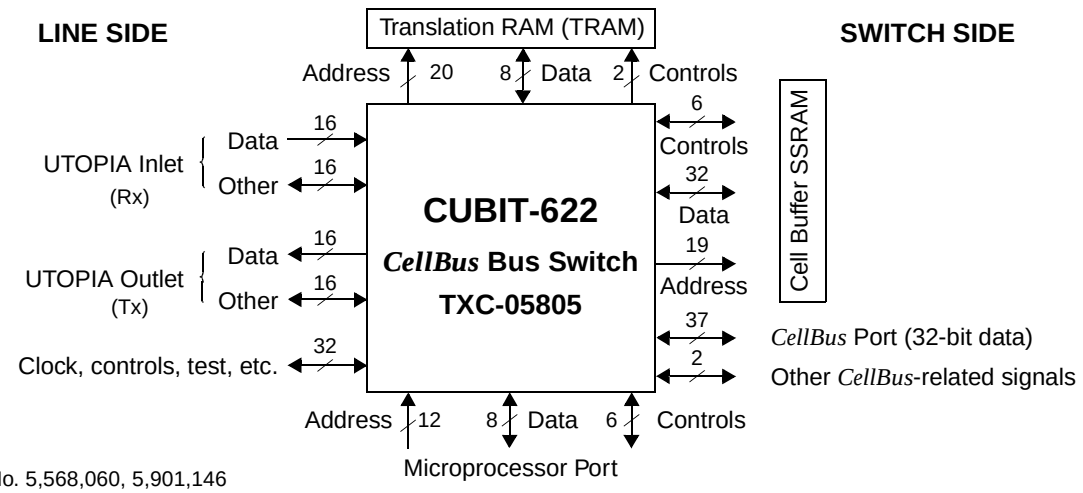
DESCRIPTION

The CUBIT-622™ device is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus*® architecture. Such systems are built from a number of CUBIT®-3, CUBIT-*Pro*, CUBIT-622 or ASPEN® devices, all interconnected by a 37-line common bus, the *CellBus*. CUBIT-622 supports unicast and multicast transfers, and has all the necessary functions for implementing a switch: cell address translation, cell routing, and outlet cell queuing.

The CUBIT-622 is designed to interface directly with UTOPIA Level 1/2, 8/16-bit compliant devices, such as the PHAST-3P (TXC-06203) and the PHAST-12E (TXC-06212). On the switch side, the CUBIT-622 interfaces directly with *CellBus* devices such as the CUBIT-*Pro* (TXC-05802B), CUBIT-3 (TXC-05804), and ASPEN (TXC-05810).

APPLICATIONS

- DSLAM Applications
- Remote access equipment
- ATM Access Multiplexers
- ATM LAN switch
- Frame Relay Switch



U.S. Patent No. 5,568,060, 5,901,146
U.S. and/or foreign patents issued or pending
Copyright © 2002 TranSwitch Corporation
CUBIT-622 is a trademark of TranSwitch Corporation
TranSwitch, TXC, CellBus, CUBIT and ASPEN are registered trademarks of TranSwitch Corporation

Document Number:
PRELIMINARY TXC-05805-MB
Ed. 5, June 2002

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

Proprietary TranSwitch Corporation Information for use Solely by its Customers

PRELIMINARY information documents contain information on products in the sampling, pre-production or early production phases of the product life cycle. Characteristic data and other specifications are subject to change. Contact Transwitch Applications Engineering for current information on this product.

DataSheet4U.com

www.DataSheet4U.com

TABLE OF CONTENTS

et4U.com
DataShee
DataSheet4U.com
DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

LIST OF FIGURES

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

BLOCK DIAGRAM

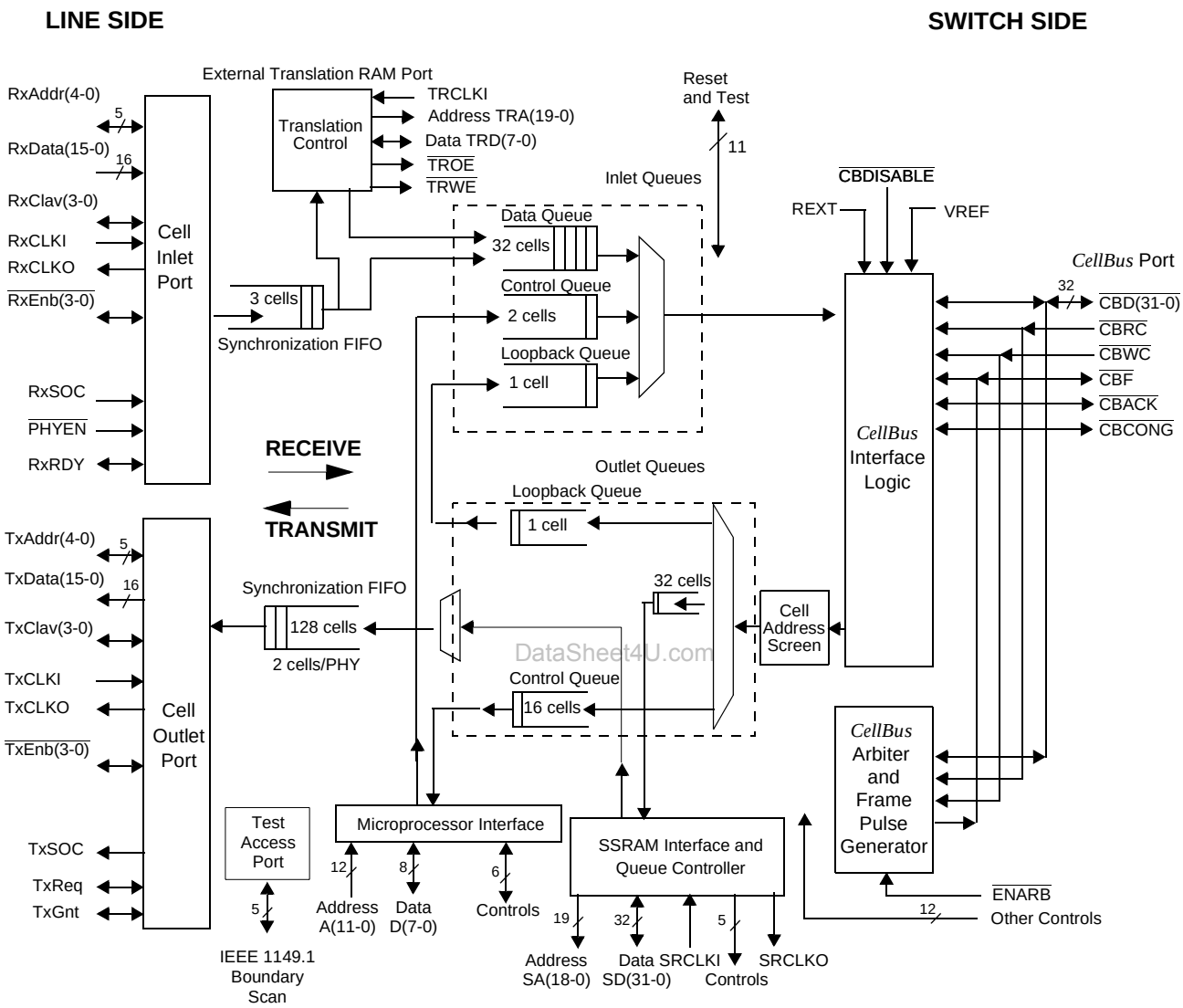


Figure 1. CUBIT-622 (TXC-05805) Block Diagram

BLOCK DIAGRAM DESCRIPTION

CELL INLET TO *CellBus* (RECEIVE DIRECTION)

A block diagram of the CUBIT-622 device is shown in Figure 1. Further information on device operation and the interfaces to external circuits is provided below in the following Operation section.

On the cell inlet side of the CUBIT-622 is circuitry associated with accepting cells from the line and passing them to the *CellBus* with an appropriate header. The Cell Inlet Port block may be set to be compatible with either the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) Level 1 or 2 interface. Incoming cells may be translated using the CUBIT-622 Translation Control block. Translation and routing header

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

tables to support this function are contained in an external static RAM (TRAM, up to 1 M x 8 bits). The configuration of the TRAM is similar to that used in the CUBIT-3 (TXC-05804). The CUBIT-622 provides support for VPI- or VPI/VCI-based translation while operating in both 8- and 16-bit modes. Operating in UTOPIA Level 2 ATM emulation mode will provide translation based on 64 ports (UNI bit set to 1) or 4 ports (UNI bit set to 0).

The CUBIT-622 also supports an external translation function where the incoming cell already carries a *CellBus* Routing Header, Tandem Routing Header, and translated outgoing VPI/VCI address. The incoming cells then pass through a FIFO data queue in the Inlet Queues block to the *CellBus* Port via the *CellBus* Interface Logic block.

When there is a cell in this 32-cell data queue, the CUBIT-622 makes a *CellBus* access request, and upon receiving a grant will send the cell to the *CellBus*, in standard *CellBus* format. In addition to data cells, the CUBIT-622 can also send control cells from the local microprocessor to the *CellBus.* Loopback cells received from the *CellBus* may also be returned to the *CellBus*, re-directed back to the originating *CellBus* device which launched the loopback cell. Both the control cells and the loopback cells have inlet queues, consisting of FIFOs with two cells and one cell, respectively. Statistics are kept for total numbers of misrouted cells, and received cells.

CellBus TO CELL OUTLET (TRANSMIT DIRECTION)

On the cell outlet side, cells of proper unicast address, broadcast address or selected multicast address, received from the *CellBus*, are recognized by the Cell Address Screen block and routed into a 32-cell FIFO queueing structure in the Outlet Queues block. The *CellBus* unicast address is unique per device, set by device straps. Each CUBIT-622 may be programmed to accept cells associated with multicast sessions. Up to 256 multicast sessions may be accepted independently by each CUBIT-622 on the *CellBus*. Each multicast session contains a list of destination ports to which a cell will be forwarded (max. all 64 ports). Control cells and loopback cells arriving from the *CellBus* are routed to the 16-cell outlet control queue, and the 1-cell outlet loopback queue, respectively.

DataSheet4U.com

The outlet data cell FIFO structure in the external SSRAM can be configured as a single bulk queue per outlet port, or it can be subdivided into four individual queues for traffic of different service types per physical port, as shown in Figure 2. The four priority-queue split is typically into CBR cells, VBR-rt (real-time) cells, VBR-nrt (non real-time) cells, and UBR/GFR cells, in decreasing order of outlet service priority. This allows for delay minimization of critical service types, and for more efficient traffic management. The queue threshold limit for each individual queue may be configured independently. The Tandem Routing Header (TRH) bits 11-4 are used for queue selection (bits 11-6 indicate port number and bits 5-4 indicate priority), while TRH bits 3-0 hold a CRC-4 to protect bits 11-4.

The CUBIT-622 supports queue over-reservation, which accommodates the traffic burstiness inherent in ATM traffic. Using this technique, a traffic burst is allowed to consume buffer space up to the specified queue threshold. However, an additional constraint is that the sum of all queues in that service category must be less than or equal to the entire class allocation. Service class limits for VBR-nrt, VBR-rt and UBR/GFR are programmable. If the sum of all buffers utilized by all queues within one of these service categories exceeds the service category limit, then cells are not enqueued. To relieve congestion when it occurs and increase system goodput, the CUBIT-622 can be configured for packet discard. Packet Discard (PD) is enabled on a global basis for the UBR/GFR queues. When an individual UBR/GFR queue limit is exceeded, the packet discard state is entered.

At the cell outlet, provisions are made for insertion of an outgoing Generic Flow Control (GFC) field and Explicit Forward Congestion Indication (EFCI) marking. Statistics are kept for discarded cells (per port).

Additionally, if enabled, the CUBIT-622 may be placed in a *CellBus* monitoring mode. In this mode, the CUBIT-622 accepts all traffic coming in from the *CellBus,* regardless of *CellBus* ID. The cells are enqueued based on *CellBus* ID. *CellBus* IDs 0-15 are enqueued in service class 0 queues for ports 0-15, and IDs 16-31 are enqueued in service class 1 queues for ports 0-15. Additionally, all multicast cells are placed in PHY 0 Service Class 2, broadcast cells are placed in PHY 1 Service Class 2, and cells that fail the CRC check(s) for the CBRH and/or TRH will be placed in a "Trash" queue, which is PHY 2 Service Class 2.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

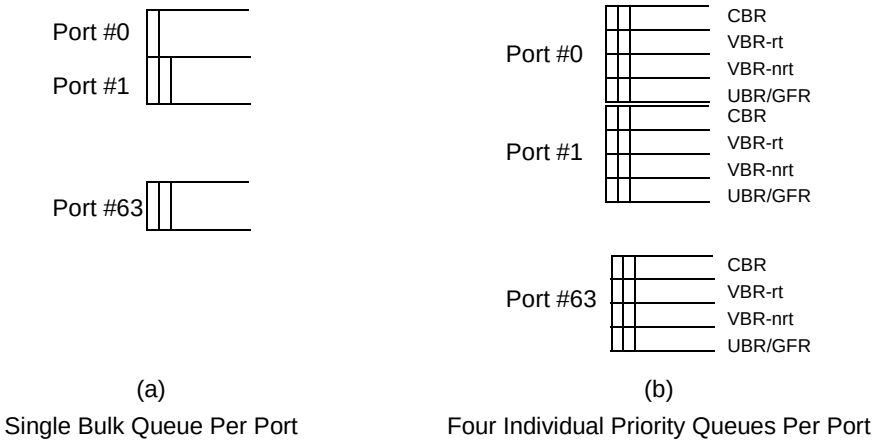


Figure 2. CUBIT-622 Outlet Queue Modes

TANDEM MODE

The Tandem Mode feature allows two CUBIT-622 devices to act as masters on the same UTOPIA bus. Each may be connected to a different *CellBus*, to enable both *CellBus* buses to be used in a load sharing application.

et4U.com

Receive Mode

DataShee

In receive mode, one device is designated the Primary UTOPIA Master. The designation is made with a lead strap. The Primary UTOPIA Master will perform all polling and PHY selection. The Secondary UTOPIA Master will monitor the address and enable lines and respond to polling with its own RDY signal to signal the Primary UTOPIA Master that it can accept a cell in its buffer. This RDY signal is asserted independent of the UTOPIA address polling and is based solely on the availability of a buffer to accept another cell. The signal is deasserted if the device cannot accept a cell. The Primary UTOPIA Master will monitor this RDY signal and will not begin the next cell transfer until RDY is asserted.

DataSheet4U.com

Both the Primary and Secondary devices will accept all cells and screen them (with a lookup) to determine if they should be forwarded to the associated *CellBus*.

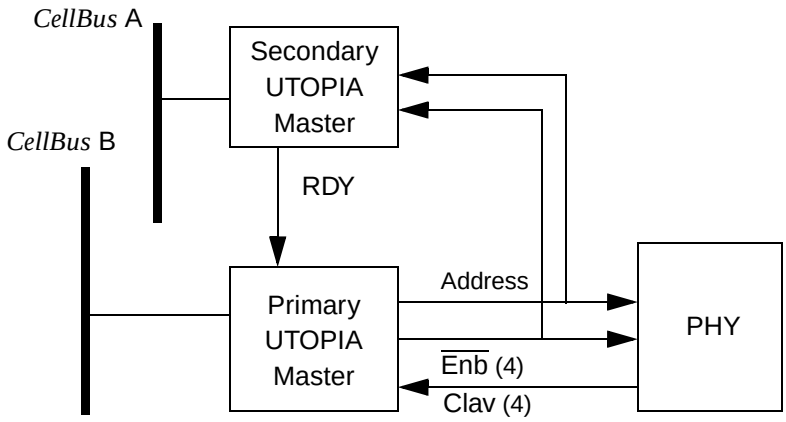


Figure 3. Tandem UTOPIA Operation - Receive Configuration

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Transmit Mode

In transmit mode, when the primary Utopia master does polling and PHY selection, the Secondary UTOPIA Master will respond with a Request (REQ signal) to indicate if it has a cell to send for a PHY that has responded positively to the polling. An arbitration mechanism in the Primary UTOPIA Master allows equal access of the Secondary and Primary devices to transmit on the UTOPIA bus. If the Primary UTOPIA Master has the bus and the Secondary UTOPIA Master asserts REQ indicating it has a cell to send, then the Secondary UTOPIA Master will be granted the bus on the next cell cycle by asserting the Grant signal. If the Primary UTOPIA Master is using the bus and the Secondary UTOPIA Master has not asserted REQ during the polling cycle then the Primary UTOPIA Master will continue to use the bus (as needed).

If the Secondary UTOPIA Master is granted the bus, the address and enable signals are asserted by the Secondary UTOPIA Master during the selection period. Grant is asserted prior to the end of the current cell transfer or as quickly as possible if no cell transfer is in progress. The Secondary UTOPIA Master monitors the polling address and Clav responses to determine which ports have cells available. The Primary UTOPIA Master tristates all enable and address lines for that cell cycle. During the cell transfer, the Secondary UTOPIA Master continues polling from the last address polled by the Primary UTOPIA Master. The Secondary UTOPIA Master again must assert the REQ signal during its cell transfer if it has a cell to send to a PHY that can accept a cell. If the Primary UTOPIA Master does not have any cells to send (to a PHY that has asserted its Clav) it will again assert the Grant signal to the Secondary UTOPIA Master prior to the end of the current cell transfer to allow it to send another cell. When the cell transfer is complete and Grant has not been asserted, the Secondary UTOPIA Master tristates the enable signals as the next cell cycle begins, controlled by the Primary UTOPIA Master. Polling resumes by the Primary UTOPIA Master from the last address polled by the Secondary UTOPIA Master. Before relinquishing the UTOPIA bus, each master asserts the address and enable signals high. A dead cycle follows during which neither master drives the bus and weak pullups maintain the signals in the high state. Control of the bus resumes during the next clock cycle.

et4U.com DataShee DataSheet4U.com

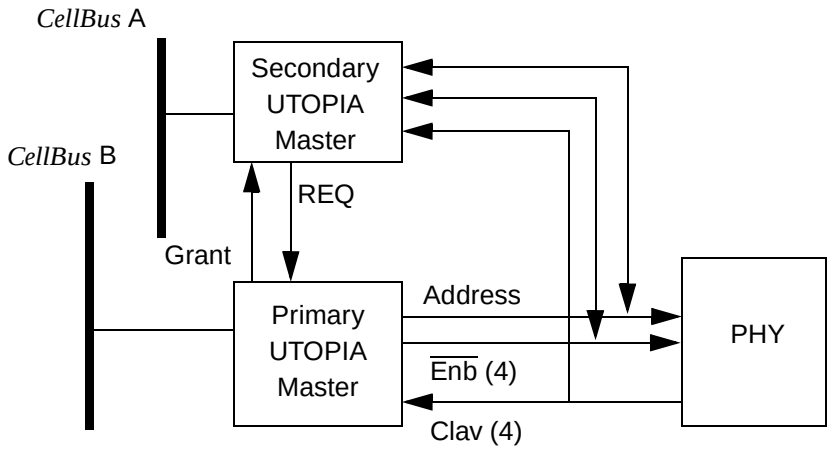


Figure 4. Tandem UTOPIA Operation - Transmit Configuration

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

OTHER INTERFACES

Microprocessor Interface

Registers are used for device configuration and indicating alarm conditions. Access to the CUBIT-622 registers is provided by the microprocessor interface, consisting of an 8-bit data bus, 12-bit address bus, and control signals. The interface can be configured for Motorola or Intel microprocessors.

UTOPIA Interface

The CUBIT-622's UTOPIA 2 port constitutes the main interface for the cell traffic between the CUBIT-622 and other physical layer devices (see Notes 1 and 2 below). The ATM Forum-compatible Level 1 and Level 2 interface can address up to 64 physical devices in ATM layer emulation (master) mode. The standard 5-bit address is used along with additional sets of four Clav and $\overline{\text{Enb}}$ signals for both transmit and receive. Multiple PHY devices may be configured for the same UTOPIA address (up to four), but each will have an individual Clav and $\overline{\text{Enb}}$ signal pair. The UTOPIA master (CUBIT-622) will poll all PHY addresses with the same address simultaneously but will receive individual responses. Only one PHY is selected for a cell transfer at a time.

CUBIT-622 supports both master and slave modes of operation. In slave mode, the CUBIT-622 emulates UTOPIA Level 2 Multi-PHY mode. However, the port based Header Translation is not supported in this mode. There are 256 VPI entries available in UNI mode and 4096 VPI entries in NNI mode, which will be shared by all ports.

Additionally, the CUBIT-622 supports cell sizes of 53 bytes and 57 bytes in 8-bit mode and 54 and 58 bytes in 16-bit interface mode when external header translation is used, i.e., where the incoming cell already carries a *CellBus* Routing Header, Tandem Routing Header, and translated outgoing VPI/VCI address. For all applications, timing and logical flow of the cell inlet/outlet is still identical to that of UTOPIA, except that potentially cell lengths differing from 53 bytes are transferred.

et4U.com DataShee DataSheet4U.com

Tandem operation is available so that two CUBIT-622 devices in ATM emulation mode can both communicate to the PHY devices and each may be connected to a different *CellBus*. The tandem operation allows for one device to be a Primary UTOPIA Master while the other device is configured as a Secondary UTOPIA Master. The Primary UTOPIA Master arbitrates the UTOPIA bus to designate which master gets to transmit on each cell cycle. Both devices must receive all traffic and process it through the normal cell address screen. This feature enables the use of two *CellBus* devices in a load sharing configuration.

Notes:

1. UTOPIA address wrap-around is not supported. It is recommended that the physical address for logical address 0 should be x0FH or less. Use of a single UTOPIA address with multiple Clav/$\overline{\text{Enb}}$ pairs is not supported. UTOPIA port assignment has a limitation of 16 ports per Clav/$\overline{\text{Enb}}$ pair.

2. The UTOPIA interface timing does not meet the specifications of the ATM Forum for the 50 MHz rate. For detailed timing specifications, refer to:

   Figure 38, Timing of UTOPIA Receive Multi-PHY (ATM Layer Emulation) (16-bit)

   Figure 44, Timing of UTOPIA Receive Multi-PHY (PHY Layer Emulation) (16-bit)

   Figure 46, Timing of UTOPIA Transmit Multi-PHY (ATM Layer Emulation) (16-bit).

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

TRAM Memory Interface

An external local memory is required by the CUBIT-622 for address translation. The CUBIT-622 integrates a complete memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a medium speed asynchronous SRAM. No external timing or control logic is required. The TRAM memory controller directly addresses up to 8 Mbits (1 Mbyte). The TRAM access time requirement is dependent on the TRAM clock (TRCLKI) speed. An access time of 14 nanoseconds or less will support the maximum UTOPIA speed.

SSRAM Memory Interface

An external local memory is required by the CUBIT-622 for cell queuing. The CUBIT-622 integrates a complete memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a high speed synchronous SRAM (SSRAM). No external timing or control logic is required. The SSRAM memory controller directly addresses up to 16 Mbits of external memory to accommodate a maximum queue size of approximately 30,000 cells. The memory controller is configured to use a 512 k x 32-bit memory at 100 MHz.

Boundary Scan (Test Access) Port

The test interface includes a five-lead Test Access Port (TAP) as the boundary scan port that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external input/output leads from the TAP for board and component test.

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

POWER UP SEQUENCING

During power up, I/O Supply Voltage ($V_{DD3.3}$) must lead the PLLPWR (2.5V). In addition, the Core Supply Voltage ($V_{DD2.5}$) needs to be brought up after I/O Supply Voltage, and can be brought up together with PLLPWR. After power up, the I/O Supply Voltage must not go below the Core Supply Voltage by more than 0.5V at any time, including power down.

OPERATION

INTRODUCTION TO *CellBus* ARCHITECTURE

This section provides only an introduction to *CellBus* bus architecture and operation. Additional technical information is provided in a TranSwitch Technical Manual, document number TXC-05802-TM1, entitled "*CellBus* Bus Technical Manual and CUBIT-*Pro* Applications", which is available as a CUBIT-*Pro* document from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

CellBus Operation

The CUBIT-622 is a versatile CMOS VLSI device for implementing ATM switching functions. Various ATM cell switching or multiplexing structures can be formed by interconnection of a number of CUBIT-622 devices (or other TranSwitch *CellBus* compatible devices) over a 37-line parallel bus with 32 data bits, the *CellBus*. Since the interconnect structure is a bus, communication among any of the devices on the *CellBus* is possible. Each cell placed onto the *CellBus* by a CUBIT-622 device can be routed either to one single CUBIT-622 device port (unicast addressing), or to multiple CUBIT-622 device ports (multicast or broadcast addressing). Depending upon the needs of an application, up to 32 CUBIT-622 devices may be interconnected on one *CellBus*. With a maximum *CellBus* frequency of 40MHz, the raw bandwidth of the 32-bit data bus exceeds 1 Gbit/s.

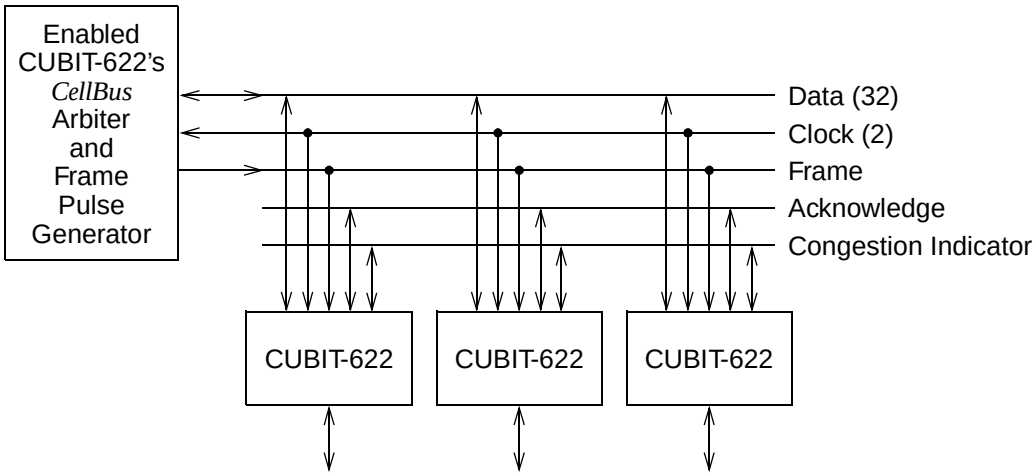


Figure 5. *CellBus* **Structure**

The *CellBus*, shown in Figure 5, is a shared bus, and can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Since multiple CUBIT-622 devices share the same *CellBus*, bus access contention must be resolved. This access contention is resolved by use of a central arbitration function. CUBIT-622s will request *CellBus* access, and the central *CellBus* Arbiter will grant access back, in response. The circuitry for a *CellBus* Arbiter and a frame pulse generator is included inside the CUBIT-622 device. Any one CUBIT-622 in a system may be enabled to perform the arbitration and frame pulse generation functions for the *CellBus* by setting its $\overline{\text{ENARB}}$ lead low.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

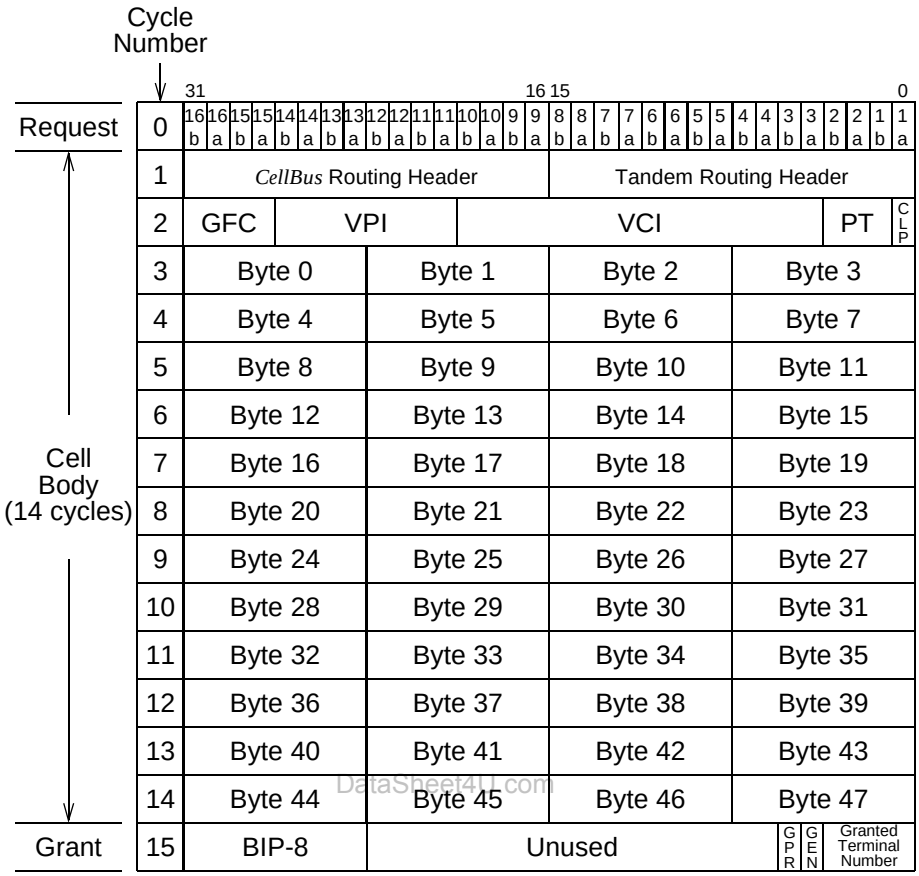


Figure 6. *CellBus* Frame Format

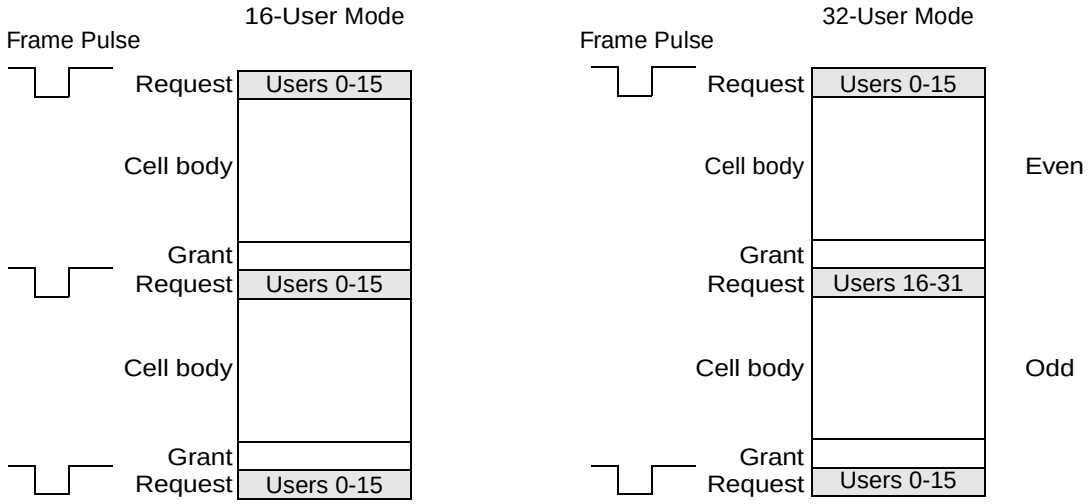
The *CellBus* has a framed format that is 16 clock cycles long and 32 bits wide, as illustrated in Figure 6. The first cycle of each frame is the Request cycle (Cycle 0), during which those CUBIT-622s which have a cell to send to the *CellBus* each make an access request by asserting one or two assigned bits on the *CellBus*. The $\overline{\text{CBF}}$, $\overline{\text{CBACK}}$ and $\overline{\text{CBCONG}}$ signals are asserted during a Request cycle. The *CellBus* ID assigned to each CUBIT-622 by device strap leads ($\overline{\text{UA(4-0)}}$) uniquely specifies which two bits it may assert during the *CellBus* Request cycle time. *CellBus* IDs 0-15 are used for 16-user systems and IDs 0-31 are used for 32-user systems (see Figure 7). For example, when leads $\overline{\text{UA(4-0)}}$ are all high, the *CellBus* ID is 0 and bits 1a and 1b are selected. By asserting one of its assigned bits, or the other, or both, access requests of three different priorities may be made (controlled via bits P1, P0 in memory address 00AH). A central *CellBus* Arbiter accepts these access requests, executes an arbitration algorithm (highest priority served first, round-robin within each priority), and issues a *CellBus* access grant during the final cycle of the frame, the Grant cycle (Cycle 15). Each grant issued by the *CellBus* Arbiter is for one CUBIT-622 to send one cell to the *CellBus*. Whichever CUBIT-622 is issued a grant during a Grant cycle will transmit its cell during the 14 Cell Body clock cycles of the next bus frame, and will also drive an 8-bit cell parity check (BIP-8) during the Grant cycle of that *CellBus* frame. Each cell sent can be of unicast, multicast, or broadcast type. CUBIT-622s will accept single-address cells routed to an address defined by their address straps, all broadcast cells, and selected multicast cells. Thus, cells may be sent from any one CUBIT-622 to any one CUBIT-622 or to multiple CUBIT-622s.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

The CUBIT-622 can be operated in either 16-user or 32-user mode, selectable via the $\overline{U32}$ lead, as shown in Figure 7. For the 16-user mode, all *CellBus* frames have an associated frame pulse ($\overline{CBF}$). However, in 32-user mode the frame is duplicated, so that an odd and even frame are provided. The distinction between these two frames is given by the location of the Request cycle relative to the frame pulse. The Request cycle in the even frame coincides with the frame pulse, whereas in the odd frame the pulse is not present. In the even frame CUBIT-622s 0-15 (lower 16 users) request access to the *CellBus*, and in the odd frame CUBIT-622s 16-31 (upper 16 users) request access to the *CellBus*. The full *CellBus* bandwidth is available to be shared among all the users on the *CellBus* in either 16 or 32-user mode.



DataSheet4U.com

Figure 7. *CellBus* **16/32-User Modes - Frame Formats**

To detect *CellBus* errors, a BIP-8 (Bit Interleave Parity byte) is calculated over the 54-byte data field that extends from the first Tandem Routing Header byte in Cycle 1 through the final payload data byte, Byte 47 in Cycle 14. The BIP-8 is generated by the transmitting CUBIT-622 using the following algorithm. The first byte of the Tandem Routing Header is exclusive-or gated with an all-ones byte, creating a starting seed value. This seed value is then exclusive-or gated with the second byte of the Tandem Routing Header. The result is then exclusive-or gated with the next byte in the cell. This process is repeated with every successive byte in the cell, through Byte 47 of the payload, and the final result is transmitted as the BIP-8 byte in cycle 15. The receiving CUBIT-622 performs the same process and compares the generated BIP-8 with the received BIP-8. If no errors are detected the receiving CUBIT-622 pulls $\overline{CBACK}$ low, acknowledging receipt of a cell. The *CellBus* Routing Header has its own CRC-4 field and is not included in the BIP-8 calculation. A cell with a BIP-8 or CRC-4 error is discarded.

There are 5 conditions in which the $\overline{CBCONG}$ signal (active low) is asserted. The first condition is when the *CellBus* outlet queue(s), Data and/or Control, is/are near full. Second, $\overline{CBCONG}$ is set when queue congestion exists on any SSRAM traffic queue (queue near full or full). This condition does not apply to multicast or broadcast cells. Third, service category congestion (VBR-rt, VBR-nrt or UBR/GFR) will set $\overline{CBCONG}$. The fourth condition is memory full in SSRAM traffic queues. This can occur if a PHY device stops accepting egress traffic from the CUBIT-622 device or when buffer over-subscription is used and the sum of the traffic queues exceeds the buffer capacity. Fifth, Packet Discard (on UBR/GFR queues) asserts $\overline{CBCONG}$.

The only signals required to operate the *CellBus* which are not sourced by a CUBIT-622 device are two transfer clocks: write clock ($\overline{CBWC}$) and read clock ($\overline{CBRC}$). These clock signals are of the same frequency, but may be slightly phase-offset to allow for reliable *CellBus* operation. The frame pulse used to define the *CellBus* frame cycle is sent out by the CUBIT-622 that has been selected to perform the arbitration function. Each CUBIT-622 contains the circuitry for both the *CellBus* Arbiter and the Frame Pulse Generator. Only one CUBIT-622 will have this circuitry enabled, by setting its control lead $\overline{ENARB}$ low.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CellBus Cell Routing

The *CellBus* architecture allows several types of cell routing from any one inlet port to the outlet ports of the CUBIT-622s on the *CellBus*:

- Point-to-Point Routing: In Unicast or Single Address cell routing a cell coming into an inlet port is transferred to a single outlet port of a specific *CellBus* device. The CUBIT-622 can also address a cell to itself, effectively implementing both the inlet and outlet ports.
- Point-to-Multipoint (Multicast): In multicast routing the cell arriving at the inlet port is sent to the subset of outlet ports that belong to the specific multicast session in each *CellBus* device on the *CellBus*.
- Point-to-Multipoint (Broadcast): A cell coming into the inlet port is routed to all of the outlet ports of all the *CellBus* devices on the *CellBus*.

For each of the routing methods the cells can be sent to different output queues according to whether the cell is used as a data cell or as control/loopback cell. Furthermore, data cells can be selected to go to one of four different data outlet queues per UTOPIA 2 outlet port: CBR queue, VBR-rt queue, VBR-nrt queue, and UBR/GFR queue.

The encoding rules for the two-byte *CellBus* Routing Header in Bits 31-16 of Cycle 1 are summarized in Figure 8.

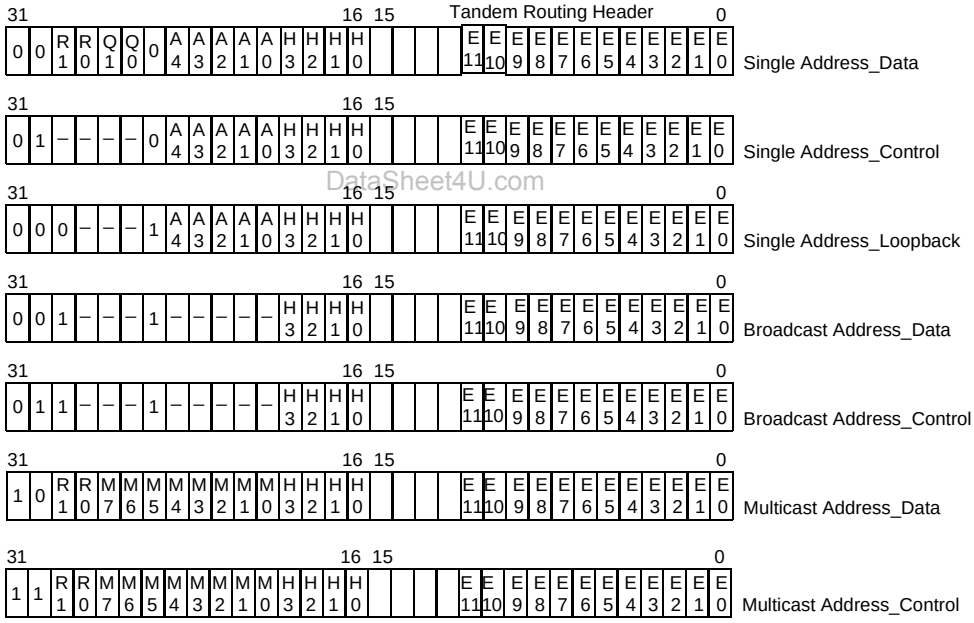


Figure 8. *CellBus* **Routing Header Formats**

<u>*CellBus* Routing Header Format</u>

The *CellBus* Routing Header contains the following fields, as shown in Figure 8:

R: Multi-PHY selector field (2 bits). Not interpreted by CUBIT-622 currently (passed through intact).

Q: Queue selection field for split-queue mode (2 bits). This field is only used to address CUBIT (TXC-05801) or CUBIT-*Pro* (TXC-05802B) devices, and is not interpreted by CUBIT-622.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

A: CUBIT-622 single address field (5 bits, for 32 addresses). A0 is the LSB. For example, A(4-0)=00000 is the address value for the CUBIT-622 whose five device identity straps $\overline{UA(4\text{-}0)}$ are all tied high (HHHHH).

M: Multicast number field (8 bits, for 256 multicast sessions). M0 is the LSB.

H: CRC-4 field. This 4-bit field H(3-0) provides *CellBus* Routing Header error protection across the *CellBus* in both directions. It is calculated over the 12-bit word (X11-X0) in bits 31-20 of the Routing Header using the following logic, where ⊕ represents logical exclusive-or:

$H3 = (\overline{X7} \oplus \overline{X9} \oplus \overline{X3} \oplus \overline{X10} \oplus \overline{X8} \oplus \overline{X5} \oplus \overline{X2})$

$H2 = (X6 \oplus X8 \oplus X2 \oplus X9 \oplus X7 \oplus X4 \oplus X1)$

$H1 = (\overline{X5} \oplus \overline{X7} \oplus \overline{X1} \oplus \overline{X8} \oplus \overline{X6} \oplus \overline{X3} \oplus \overline{X0})$

$H0 = (X8 \oplus X10 \oplus X4 \oplus X11 \oplus X9 \oplus X6 \oplus X3 \oplus X0)$

For cells arriving from the *CellBus*, the CUBIT-622 automatically calculates the corresponding CRC-4 and sets to 1 the status bit CRCF (bit 7 in register 008H) if it is not the same as that in bits H(3-0) of the received Routing Header. This status bit may be enabled to cause an interrupt signal to the microprocessor by setting to 1 the enable bit INTEN7 (bit 7 in register 009H). The CRC-4 is automatically calculated and inserted by the CUBIT-622 into cells sent to the *CellBus*.

Tandem Routing Header Format

In CUBIT-622 applications, the Tandem Routing Header bits 11-0 (Extended Queue field) are used for queue and priority selection and include cyclical redundancy protection.

E: Extended Queue field E(11-0). E(11-6) indicate port number, E(5-4) indicate priority, and E(3-0) is the CRC-4. The priority field E(5-4) is encoded as follows: CBR '00', VBR-rt '01', VBR-nrt '10', UBR/GFR '11'.

DataSheet4U.com

CellBus Status Signals and Monitoring

The CUBIT-622 provides the capability to monitor the activity on the *CellBus*. The essential signals that determine whether the *CellBus* is active (in the absence of any cell traffic) are the clock signals and the frame pulse.

The *CellBus* clocks (read and write) are generated externally to the CUBIT-622. If either of these clocks fails, the entire *CellBus* will cease operation. The CUBIT-622 provides the capability to detect the absence of clock signal for more than the equivalent of 32 processor clock (PCLK) cycles. The failure detection is performed independently for the *CellBus* Read Clock ($\overline{CBRC}$) and the *CellBus* Write Clock ($\overline{CBWC}$).

Two bits (register 005H, bits CBLORC and CBLOWC) in the CUBIT-622 memory map are used to indicate these clock loss events. Once an event is detected, the bit in register 005H will remain set to one until the microprocessor reads the register, at which point the register will be cleared. Either event can be used to generate a microprocessor interrupt provided that the corresponding bit in the interrupt enable register (address 006H, bits INTENA1 and INTENA0) is 1.

The second monitoring function concerns the detection of loss of frame. The detection mechanism looks for two consecutive missing *CellBus* frame pulses ($\overline{CBF}$) in 32-user mode ($\overline{U32}$ = Low), and four consecutive missing *CellBus* frame pulses in 16-user mode. The *CellBus* Read Clock must be present to detect Loss of Frame Pulse. If *CellBus* Read Clock is present and *CellBus* Write Clock is not, then both CBLOWC and CBLOF (in register 005H, bits 0 and 2) will be set to 1 upon loss of frame. CBLOF will generate an interrupt to the microprocessor if the corresponding interrupt enable bit is 1 (register 006H, bit 2: INTENA2).

Apart from the detection of loss of *CellBus* Read and Write clocks, the device has a recovery mechanism that re-synchronizes the device to the *CellBus* frame pulse as soon as the *CellBus* clocks are restored and stabilized to resume normal operation. In case this mechanism fails, a Software Reset must be applied. A Software Reset resets the entire device except the configuration registers in the memory map. To resume normal operation, the FIFO Pointer Table as well as the Freelist must be restored.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CellBus Traffic Monitoring

The traffic monitoring function concerns the monitoring of all *CellBus* traffic. If enabled (by setting control bit CBMON in register 100H), the CUBIT-622 accepts all traffic coming in from the *CellBus* regardless of the *CellBus* ID to which cells are addressed. The cells are enqueued based on this *CellBus* ID. *CellBus* IDs 0-15 are enqueued in service class 0 (CBR) queues for ports 0-15, and IDs 16-31 are enqueued in service class 1 (VBR-rt) queues for ports 0-15, respectively. Multicast cells are placed in PHY 0 Service class 2 and broadcast cells are placed in PHY 1 Service Class 2. If the CRC check(s) failed for the CBRH or TRH, the cell will be put in the "Trash" queue which is PHY 2 Service Class 2. This facilitates the design of *CellBus* monitoring cards for new and existing *CellBus* systems.

CUBIT-622 CELL INLET AND OUTLET PORTS

The Cell Inlet and Cell Outlet ports constitute the main interfaces for the cell traffic between the CUBIT-622 and other devices in either the upper ATM or Physical (PHY) Layers. The device supports UTOPIA Level 1 and 2 interfaces in either 8 or 16-bit mode at rates up to 50 MHz.

The CUBIT-622 can provide address translation if selected by setting control parameter InletCellSize (register 101H) to 53 bytes (8-bit wide interface) or 54 bytes (16-bit interface). If no translation is selected, the external hardware must provide the *CellBus* Routing Header, the Tandem Routing Header (optional), and the ATM cell. If translation mode is selected, the hardware is required only to provide the ATM cell and the CUBIT-622 will perform the translation based on the information programmed into the attached Translation RAM.

For all the modes the cell size is selectable via control bits InletCellSize(1-0) and OutletCellSize(1-0), as described below. This feature permits the CUBIT-622 to accommodate the requirements for different designs.

Additionally, the UTOPIA Level 1 and Level 2 (8-bit or 16-bit) modes can be selected to behave as either the master (ATM layer device) or the slave (PHY layer device). The selection between ATM and PHY layer device for the UTOPIA and 16-bit modes is made via the $\overline{\text{PHYEN}}$ lead (lead A2), where a low enables PHY layer device operation.

The CUBIT-622 allows the selection of the clock for the cell inlet/outlet operation from two different sources: the *CellBus* clock ($\overline{\text{CBRC}}$, lead AB12 and $\overline{\text{CBWC}}$, lead AA12) or the microprocessor interface clock (PCLK, lead U3). The clock selected will be used for the UTOPIA modes for which the CUBIT-622 sources the interface clock. The selection of the clock source for the cell interfaces is performed via six control bits in register 00BH: CLKS1, CLKS0 and LINEDIV(3-0). The coding for the clock selection is as follows:

CLKS1, CLKS0 = 0,0: Cell interface clock = *CellBus* clock divided by 2^{LINEDIV}

CLKS1, CLKS0 = 0,1: Reserved, do not use

CLKS1, CLKS0 = 1,0: Cell interface clock = PCLK clock divided by 2^{LINEDIV}

CLKS1, CLKS0 = 1,1: Reserved, do not use

Please note that the LINEDIV(3-0) control bits must be set to their desired values after the ONLINE control bit (bit 7 in register 00CH) has been set to 1.

Typical signal connections for the CUBIT-622 when operating in UTOPIA mode are illustrated in Figure 9 and Figure 10, for Single-PHY ATM Layer and PHY Layer cell level handshake modes, respectively. Figures 11 and 12 show the corresponding Multi-PHY configurations.

The CUBIT-622's UTOPIA port constitutes the main interface for the cell traffic between the CUBIT-622 and other devices. The ATM Forum Compliant Level 1 and Level 2 interface can address up to 16 physical devices in ATM layer emulation (master) mode.

Additionally, the CUBIT-622 supports cell sizes of 53 bytes or 57 bytes in 8-bit mode and 54 or 58 bytes in 16-bit interface mode when external header translation is used (i.e., where the incoming cell already carries a *CellBus*

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Routing Header, a Tandem Routing Header, and a translated outgoing VPI/VCI address[1]). For all applications, timing and logical flow of the cell inlet/outlet is still identical to that of UTOPIA, except that potentially cell lengths differing from 53-bytes are transferred.

The operating mode options for UTOPIA mode are selected by the device mode control bits U1, InletCellSize(1-0)/OutletCellSize(1-0), UNI, 16b and PHY0ADDR(4-0), and control input lead $\overline{\text{PHYEN}}$. The UTOPIA modes are described in more detail below. Differences between Single-PHY and Multi-PHY functions in a given mode, if any, are highlighted. In UTOPIA mode, $\overline{\text{PHYEN}}$ determines whether the CUBIT-622 emulates an ATM (master) or PHY (slave) device. U1 determines either UTOPIA Level 1 or Level 2 support. InletCellSize/OutletCellSize sets the cell size, which can vary between 53 bytes and 57 bytes in 8-bit mode. The cell sizes supported in 16-bit mode are 27 and 29 words. In UTOPIA Level 2 mode in ATM layer emulation, the ATM layer device is required to poll the various physical layer devices to determine the availability of cells which can be transferred. The polling mechanism implemented in the CUBIT-622 is round robin-based. The physical addresses are set via control bits PHY0ADDR(4-0), which set the physical address for PHY0. Addresses for ports 1-15 are in sequential order from the value in PHY0ADDR. Each physical device has an individual enable (registers A01H to A08H); when set to 0 that PHY device is not polled in Multi-PHY mode. Control bit 16b enables the CUBIT-622 to receive/transmit 16-bit wide data.

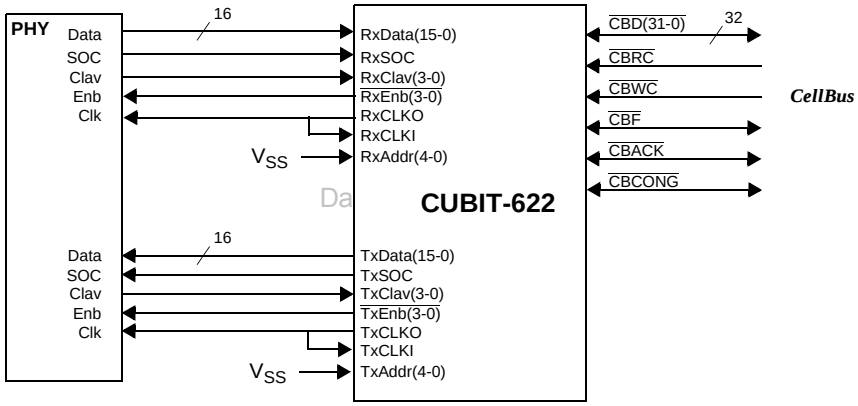


Figure 9. ATM Layer Emulation (Master Mode) - Single-PHY

1. 55-byte and 56-byte modes may not be used at the inlet because they do not allow the full 4-byte *CellBus* Routing Header to be appended.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

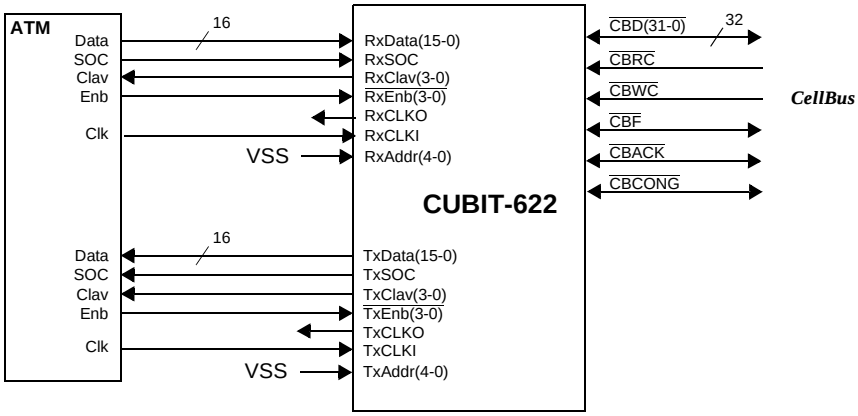


Figure 10. PHY Layer Emulation (Slave Mode) - Single-PHY

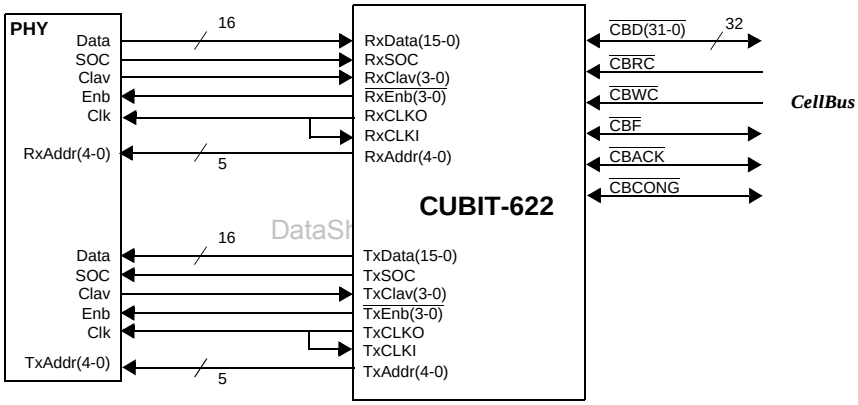


Figure 11. ATM Layer Emulation (Master Mode) - Multi-PHY

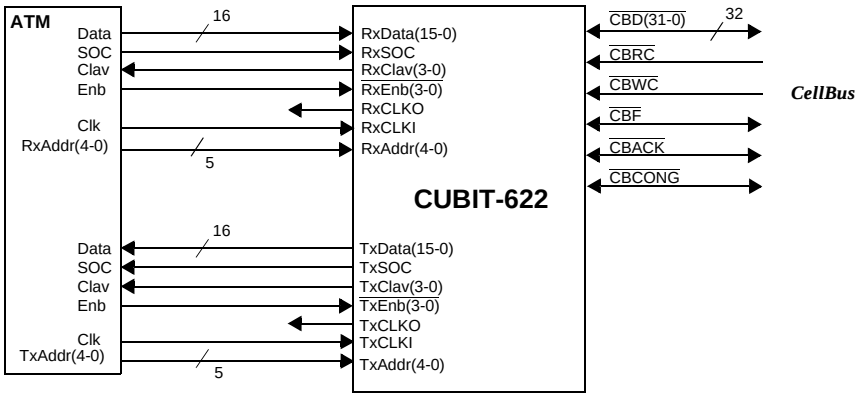


Figure 12. PHY Layer Emulation (Slave Mode) - Multi-PHY

DataSheet4U.com www.DataSheet4U.com

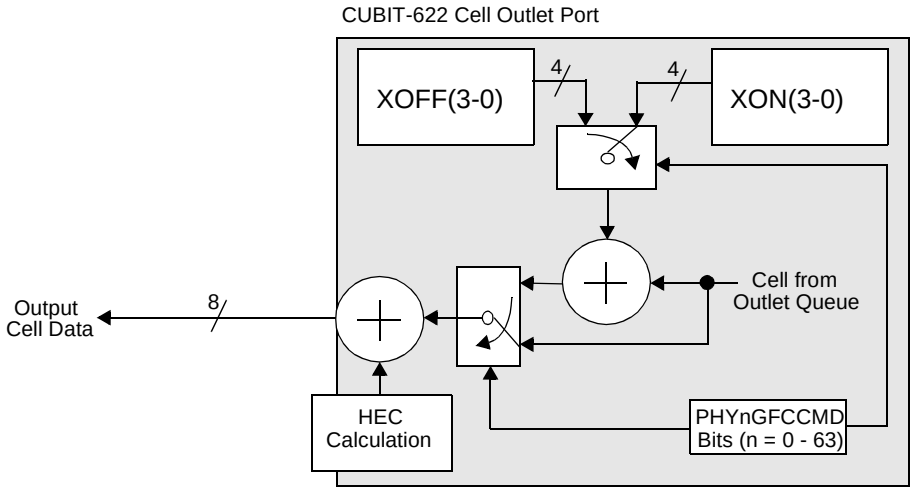
DataSheet4U.com

www.DataSheet4U.com

TRAFFIC MANAGEMENT FUNCTIONS

Dynamic Generic Flow Control (GFC) Field Insertion

The CUBIT-622 can insert the value of the first nibble of the ATM cell header in real time. The value of the GFC nibble is supplied to the CUBIT-622 via the control bits XON(3-0) and XOFF(3-0) (register 105H). The insertion of the GFC value is enabled via the control bits PHYnGFCCMD(1-0) in registers 110H to 11FH, where n = 0 - 63, as shown in Figure 13.



DataSheet4U.com

Figure 13. GFC Insertion on the Outlet Queue (PHYnGFCCMD)

When control bit 1 of PHYnGFCCMD(1-0) is set to one, then the state of either the XOFF or XON fields will be accepted during the leading rising edge of the clock for the first byte of the ATM cell header and inserted as an outgoing GFC on the following cell. Therefore the GFC value is inserted into the next outgoing cell. The setting of PHYnGFCCMD(1-0) bit 0 is used to select either the XON field or XOFF field. When set to 1, it selects the XON field. When bit 0 is set to 0, the XOFF field is inserted. There is a separate PHYnGFCCMD(1-0) for each PHY port (n = 0 - 63).

Explicit Forward Congestion Indication (EFCI)

The CUBIT-622 can notify an impending congested state by setting to one the middle bit of the Payload Type (PT) field in the ATM cell header. This Explicit Forward Congestion Indication bit (EFCI) will be asserted in the PT fields of user cells if the following two conditions occur at the same time:

a) the IFECN(3-0) bit (register 101H, bits 7-4) corresponding to the cell's given service class queue is set to 1 and

b) the queue fill level is 27 cells from the queue limit for that service class queue.

The condition is cleared when the queue clears its congestion indication; this occurs when any of the following occurs:

a) the IFECN(3-0) bit corresponding to that service class queue is reset to 0, or

b) the queue in question empties, or (for longer queues)

c) a number of cells are read out of the queue such that a threshold fill level of 54 cells from the limit is reached.

Note: The IFECN(3-0) field is encoded as follows: CBR bit 0, VBR-rt bit 1, VBR-nrt bit 2, UBR/GFR bit 3.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Packet Discard (PD)

To relieve congestion and increase system goodput when operating in packet mode, the CUBIT-622 can be configured for packet discard. Packet Discard (PD) threshold is enabled on a global basis for the UBR/GFR queues. When an individual UBR/GFR queue near limit is exceeded (queue limit - 27), PD is triggered for the UBR/GFR service class queue. While in the PD state, no cells other than EOM cells are allowed to be enqueued. The PD state for an individual UBR/GFR queue is exited when the UBR/GFR queue fill level has decreased to 50% of the queue limit.

Queue Congestion Indications

To aid in the detection of congestion conditions, three interrupts are available (QF, MNF, MF):

QF or Queue Full (Address 106H, bit 4): After a cell was written into a queue, the queue length reached its limit. This is an indication that indiscriminate cell discard will start for this queue.

MNF or Memory Not Full (Address 106H, bit 1). After a cell was read from a queue, there is space available for a cell to be enqeued.

MF or Memory Full (Address 106H, bit 0). After a cell was written into a queue, the entire memory is full. This is an indication that indiscriminate cell discard will start for all queues.

Paralleling Cell Inlet/Outlet Ports for Redundancy

If the control bit ONLINE (control register address 00CH, bit 7) is set to zero, then all of the CUBIT-622 cell outlet interface output leads will be taken to the high impedance (Hi-Z) state and the cell inlet data input leads will be disabled. Thus two CUBIT-622s may be paralleled for redundancy, each connected to a separate *CellBus*. Cells will only be accepted from, or sent to, the line by the CUBIT-622 in which ONLINE = 1. The other CUBIT-622 must have its ONLINE bit set to 0. When ONLINE is set to 0 during a cell transfer, the transfer will be completed before the output leads are set to the high impedance state.

INLET-SIDE TRANSLATION

Introduction

The translation function on the inlet side uses information stored in an external static Translation RAM (TRAM), and can provide the following functions:

Virtual Path Identifier (VPI) translation or

VPI/VCI translation (where VCI is Virtual Circuit Identifier), and

CellBus Routing Header insertion and Tandem Routing Header insertion, or

F4 flow cell routing, or

F5 flow cell routing.

VPI Routing Table Lookup for ATM Multi-PHY

All translation operations start by checking if the UNI bit is set to 1. If it is, the 6-bit port number of the connection source is used in conjunction with the cell header for header lookup by the CUBIT-622. If UNI is not set, the 2 least significant bits of the PHY address are used in conjunction with the 12-bit VPI to perform the lookup (Only ports 0 - 3 are supported in NNI mode). The lookup retrieves the VPI routing table. Within the routing table record for that VPI is control information indicating if the VPI is valid and active, and whether cells are to be routed based on VPI number alone or on VPI and VCI. [Note: For UTOPIA Level 1 operation the port number is ignored.]

Note: Tandem Routing Header insertion is required for CUBIT-3 and CUBIT-622, but not for CUBIT-*Pro*.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

If VPI-only routing is selected, a translated VPI number, accompanied by *CellBus* and Tandem Routing Headers, is retrieved from the translation record for that VPI. In this case, the VCI number of the incoming cell is not changed. If VPI translation is selected, separate routing for F4 OAM flow cells and RM-VPC cells on that VPI can be programmed, allowing selective handling of these OAM-cells and RM-cells by a *CellBus* system. F4 OAM cells are identified by the VCC when VPI-only routing is selected. VCC = 3 is used for segment OAM identification and VCC = 4 is used for end-to-end OAM identification. F5 OAM cells are identified by the PTI field = 4 for segment flows and PTI = 5 for end to end flows.

If the connection is instead programmed for VCI translation, then a two-step procedure is used to accomplish the translation. The VPI record, accessed first, indicates the size and position in memory of the VCI translation table. Using this information, and the VCI address of the cell, a VPI/VCI translation record is accessed. This translation record contains the VPI and VCI numbers to be assigned to the cell, along with the *CellBus* and Tandem Routing Headers. When VPI/VCI translation is selected, separate routing for F5 OAM flow cells and RM-VCC cells on that VCI can be programmed, allowing selective handling of these OAM-cells and RM-cells.

In both cases, the cells with the translated headers and *CellBus* and Tandem Routing Headers are forwarded to the *CellBus* in sequential order. Translation does not add delay to cells passing through the inlet side to the *CellBus*.

Translation RAM Connections

The CUBIT-622 can address up to 1M bytes of Translation RAM (TRAM), which uses external SRAM memory. The connections to the TRAM are shown in Figure 14. The TRAM access time requirement is dependent upon the Translation RAM clock speed (TRCLKI).

DataSheet4U.com

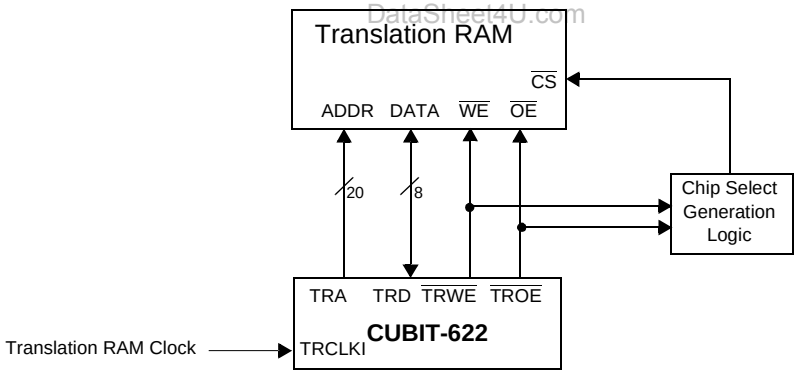


Figure 14. Translation RAM Connections

The chip select should be implemented according to the number of SRAM devices used in the design. If a single 1M x 8 SRAM is used, the memory can be permanently selected, or if a low-power application is required then the memory can be selected only when the CUBIT-622 needs to access the SRAM (use $\overline{\text{TROE}}$ and $\overline{\text{TRWE}}$, as shown in Figure 14).

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Translation RAM Control

When the CUBIT-622 device is configured to perform translation, it replaces received values of VPI or VPI and VCI numbers with new values, and adds Routing Headers to the cells forwarded to the *CellBus*. The VPI/VCI number and Routing Header information that is inserted comes from translation record entries in the TRAM. The TRAM is organized into a block of VPI records and a block of VCI records, the contents of which are established by system control.

Translation RAM Organization

The Translation RAM partitioning is shown in Figure 15. The lower portion of the TRAM contains the translation records for VPIs. When the UNI mode is enabled (control bit UNI=1 in register 00AH), the number of VPI entries available is 256 per port (max 64 ports). When NNI mode is enabled (UNI=0), 4096 VPI entries are available per port (max 4 ports).

The VP Record has six bytes. The size of the VPI memory space in NNI mode is 6 x 4096 x 4 = 98,304 bytes. For UNI mode the max size is 6 x 256 x 64 = 98,304 bytes when using UTOPIA Level 2 (Multi-PHY). The size of the VPI record space is limited by the number of ports specified in NPHY(1-0). Only the appropriate number of ports should be enabled, based on the value of NPHY. If NPHY is set to 00, only UNI ports 7-0 are supported and 12,288 bytes are required. The following table summarizes the possible size of the VPI records:

Table 1. VPI Record Size

NPHY(1-0)	# of UNI PHYs	VPI Record Size (bytes)	# of NNI PHYs	VPI Record Size (bytes)
00	8	12,288	4	98,304
01	16	24,576	N/A	
10	32	49,152	N/A	
11	64	98,304	N/A	

For UNI mode using UTOPIA Level 1 (Single-PHY) the size is 1536 bytes (6 x 256). In NNI mode for Single-PHY operation the number of bytes used for the VP records is 4,096 x 6 = 24k. When using PHY emulation mode and UNI interface, the size is 1536 bytes regardless of the use of UTOPIA Level 1 or 2 because PHY mode always emulates only a Single-PHY.

The memory space above the VPI section is the VCI translation record storage space; this is divided into a number of VCI pages. Each VCI page contains the translation records for 128, 256, 512, or 1024 VCIs.

The VC Record has eight bytes. The number of VCI records per page (VRP) depends on the settings of the VRPS(1-0) control bits in register 00EH as follows:

VRPS(1-0)=0,0: VRP is 256

VRPS(1-0)=0,1: VRP is 512

VRPS(1-0)=1,0: VRP is 1024

VRPS(1-0)=1,1: VRP is 128

The total size of the TRAM which the CUBIT-622 can support is up to 1M bytes. Hence, the number of VCI translation table pages that can be supported is a function of memory size and the state of the UNI control bit, as shown in Table 1. For example, the maximum number (M) of VCI memory pages, for maximum memory size, is as follows:

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

M = (1M - memory used for VP records) / (# VC records per page * 8)

For 4 NNI ports (NPHY(1-0) = 00) the memory used for VP records = 4096 x 6 x 4 = 96k bytes

For 16 UNI ports (NPHY(1-0) = 01), the memory used for VP records = 256 x 6 x 16 = 24k bytes

For 64 UNI ports (NPHY(1-0) = 11), the memory used for VP records = 256 x 6 x 64 = 96k bytes

The formula for computing the max number of VCI pages is as follows:

Max Number of VCI Pages = Available Memory (M)/(#VCIs/page x 8 bytes/VCI record). A sample of possible configurations is shown in Table 2, “Max Number of VCI Pages,” on page 22.

Table 2. Max Number of VCI Pages

NPHY(1-0)	Max Number of Ports (UNI/NNI)	VRPS(1-0)	# VCIs per Page	Max # of Pages
3	64	3	128	256*
3	64	0	256	256*
3	64	1	512	226
3	64	2	1024	113

et4U.com DataShee DataSheet4U.com

* Note: The maximum number of VCI pages supported is 256.

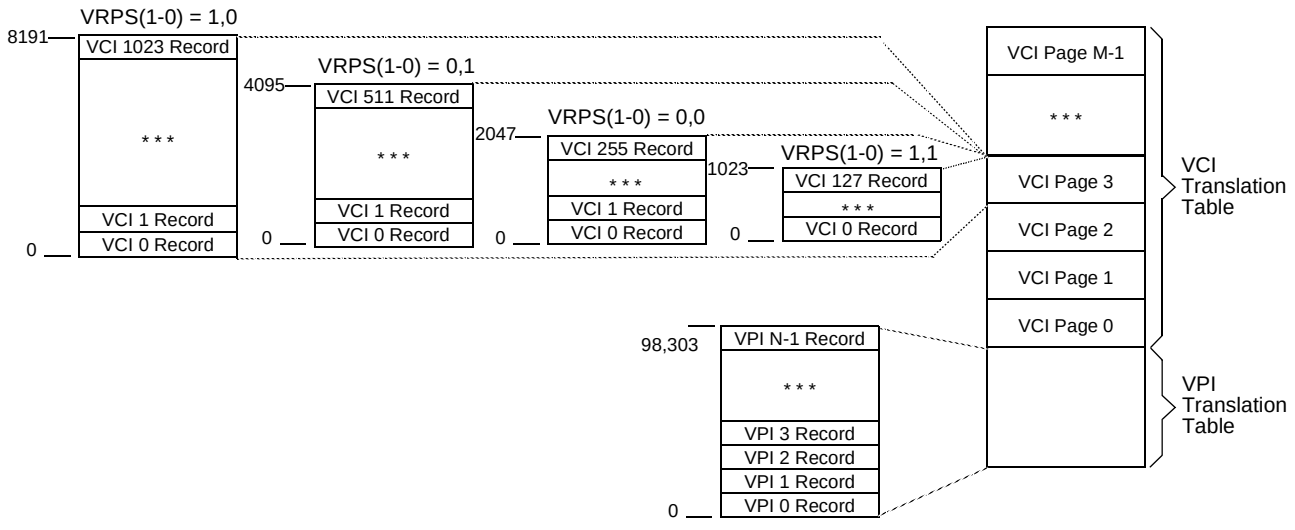


Figure 15. Translation RAM Organization

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

VCI Page 0 Organization

This page may optionally be used for OAM-cells routing, RM-cells routing, or data cells routing. The organization of VCI Page 0 is shown in Figure 16.

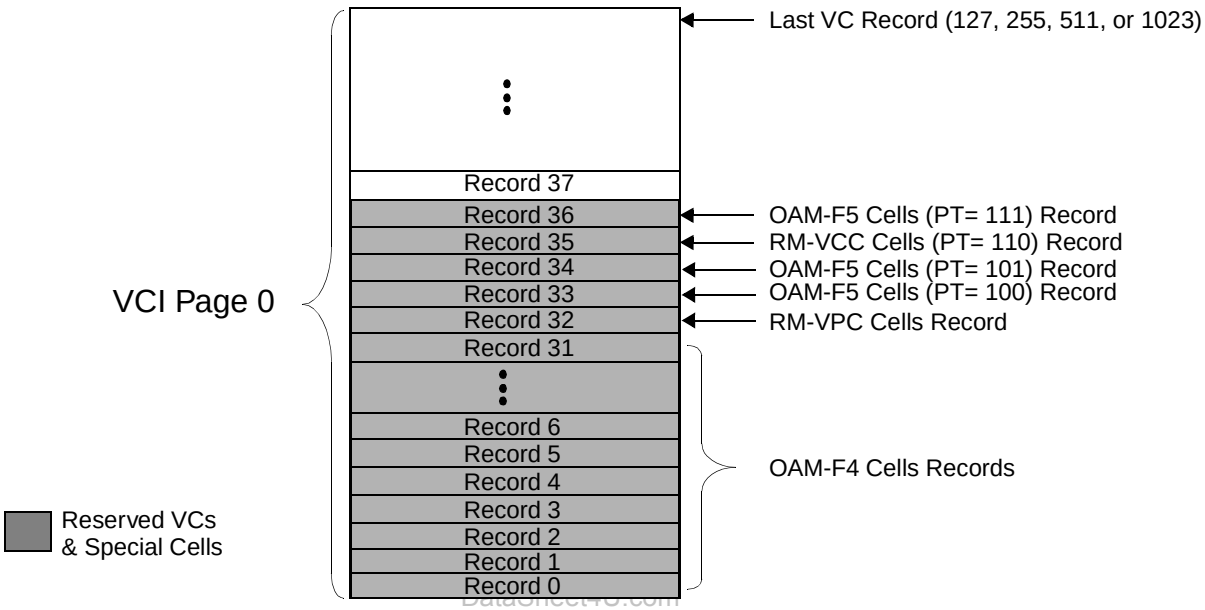


Figure 16. VCI Page 0 Organization

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Translation Procedure

For UTOPIA Level 1 (control bit U1 in register 100H set to 1) translation is performed in a two-step procedure, starting with examining the incoming VPI number. A full 8-bit (UNI=1) or 12-bit (UNI=0) VPI number may be used. The incoming VPI number is used to address a VPI translation record. If the translation is to be done on VPI only, leaving the VCI number intact, then the VPI number and routing header are contained in the VPI translation record. If VPI and VCI translation is to be done, then the VPI record contains a pointer to the location of one or more "pages" of VCI translation records. Each "page" is a set of translation records for either 128, 256, 512, or 1024 consecutive VCI numbers (depending on the settings of bits VRPS(1-0) in register 00EH). Up to sixteen such VCI pages may be assigned to any VPI. The only restriction is that the VCI pages for each VPI must be assigned in consecutive VCI address space from zero upwards. Within this assigned space, the VCI number of the incoming cell is used to address a particular VCI translation record containing the new VPI and VCI numbers and the routing header.

OAM/RM cells are routed either from the VP record or VC record that is marked for this special cell's routing, as detailed in the section below entitled "OAM-Cells and RM-Cells Record Format".

For the translation operation the CUBIT-622 uses several data structures. These data structures can be of three different types:

VP Record

VC Record

OAM/RM Record

et4U.com Each of these records contains one or more control bits in the first byte of the record (byte 0), which determines whether the routing is per VP, per VC, or per OAM/RM cell. These control bits are described next. DataShee

DataSheet4U.com

Translation Records Control Bits

Four control bits, labelled as A, P, E and I, are used in byte 0 of translation records, as described below (see also Figure 17):

Active (A) Bit:

If the A bit is set to one in a translation record, then that VPI or VCI is active. Cells received with this VPI or VCI will be translated and forwarded to the bus, unless control bit I is set to one and NOTIGN (bit 5 in register 00EH) is zero. If A is set to 0, then cells received on this VPI or VCI will be considered misrouted, unless control bit I is set to 1 and NOTIGN (bit 5 in register 00EH) is zero.

VPI Translation Enable Bit (P):

If this bit is one in a VPI translation record, then a VPI-only translation is made. If P is set to zero, a combined VPI and VCI translation is made.

OAM/RM Cell Routing Enable Bit (E):

If bit E is set to one in a VPI record, then VCIs numbered 0 through 31 of that VPI will be routed according to OAM/RM records contained in record numbers 0 through 31 of VCI page zero. Additionally, if bit E is set to one in a VPI record, then cells of that VPI with VCI = 6 and having the PT = 110 will be routed according to the OAM translation record contained in record number 32 of VCI page zero. Regular data cells (not conforming to the above rules) are routed according to the VP and/or VC record. If bit E is set to one in a VCI record, then cells of that VPI having the PT = 100, 101, 110, and 111(Payload Type Indicator, in ATM cell header) will be routed according to the OAM translation record contained in record numbers 33, 34, 35, and 36 of VCI page zero, respectively. (Note: PTI=110 and 111 are currently undefined.)

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Ignore Bit (I):

If the ignore bit is one (I=1) in an active VP or VC (i.e., A is set to 1 in the translation record) then incoming cells bearing this VP or VC number are discarded, but not counted as misrouted cells. If the control bit NOTIGN (bit 5 in register 00EH) is set to 1, then connections with I set to 1 will be treated as if I was set to 0.

For OAM/RM-cell translation records, control bits P and E are replaced by OAM/RM routing mode bits C1 and C0, as shown in Figure 21.

OAM/RM Routing Mode Bits (C1,C0):

These bits are used to determine on which VPI/VCI OAM/RM cells are routed. The possible combinations are:

C1,C0 = 0,0: the cell header is translated according to the values in the OAM/RM record.

C1,C0 = 0,1: for F4 flow this virtual path connection's (VPC) OAM cells/RM-VPC cells are not routed according to the OAM/RM record. Instead, these cells are routed according to the VP record corresponding to the incoming VP.
For F5 flow this virtual circuit connection's (VCC) OAM cells/RM-VCC cells are not routed according to the OAM/RM record. Instead, these cells are routed according to the VC record corresponding to the incoming VP/VC combination.

C1,C0 = 1,0: attach *CellBus* Routing Header (CBRH) and Tandem Routing Header (TRH) only, and preserve the incoming VP/VC combination.

C1,C0 = 1,1: reserved

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

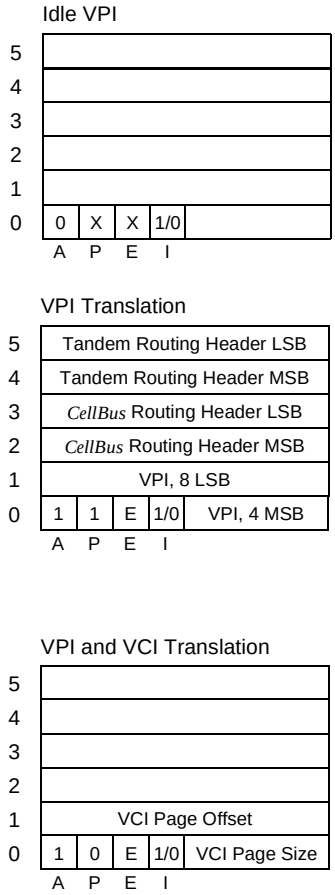
DataSheet4U.com

www.DataSheet4U.com

Translation Record Formats

VPI Translation Record Formats

VPI translation records are six bytes long, as shown in Figure 17. Each VPI may be either idle or busy. If it is busy, then each VPI may be set for VPI-only translation, or for combined VPI/VCI translation. The control bits (A, P, E and I) and Routing Headers are described in the preceding sections.



If the VPI is unused, then the MSB (Active bit, A) of relative address zero is set to zero, indicating idle. If a cell arrives with this VPI number, it is discarded and is counted as a misrouted cell. If I=1 the cell is discarded but not counted as misrouted.

If the VPI is active and is to have VPI number translation only, then the A bit is set=1, and the P bit is set=1. In this case, the VPI to be inserted on the cell is contained in the 4 LSB of relative address zero (4 MSB of new VPI), and in relative address one (8 LSB of new VPI). *CellBus* and Tandem Routing Headers are also contained in the next two or four bytes.

If the VPI is active and is set for combined VPI/VCI number translation, a reference is generated to a VCI translation record. The VPI is set active (A=1), and is set for VPI/VCI translation (P=0). The 4 LSB of relative address zero contain the VCI Page Size, which is the number of assigned VCI pages (max 16). Relative address one contains the VCI Page Offset, which indicates where among the VCI pages the first utilized page starts.

Figure 17. VPI Translation Record Formats

The calculation of the start address for the VP record is performed as follows:

$$VP\_Start\_Addr = VP\# \times 6$$

DataSheet4U.com

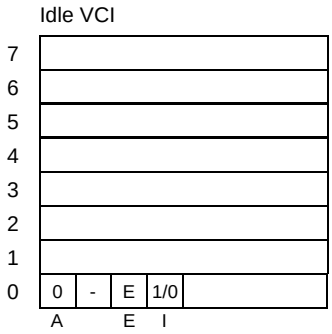
www.DataSheet4U.com

DataSheet4U.com

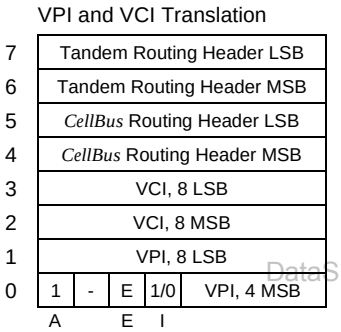
www.DataSheet4U.com

VCI Translation Record Formats

VCI translation records are eight bytes long, as shown in Figure 18. Each VCI may be either idle or busy.



If the VCI is inactive (A=0) and not Ignore (I=0), then cells arriving bearing that VCI number are discarded and counted as misrouted. If I=1, they are discarded and not counted as misrouted.



If the VCI is active (A=1), then the VPI and VCI numbers, and the *CellBus* Routing Header and Tandem Routing Header to be inserted, are read from the VCI translation record at the positions indicated.

DataSheet4U.com

Figure 18. VCI Translation Record Formats

The calculation of the start address for the VC record uses information from the VP table as well as the VCI of the incoming cell. The information required from the VP record is the VCI Page Offset (VPO). The start address of the VC record, assuming a given number of VCI records per page (VRP, determined by the control bits VRPS1 and VRPS0 in register 00EH), is calculated (in decimal format) as follows:

VC_Start_Address = VC Base Address + VPO (VC page offset) x VRP x 8 + VCI x 8

Where the VC Base Address is programmed in register addresses 015H (bits 7-0, TRAL(7-0)), 016H (bits 7-0, TRAU(7-0)) and 017H (bits 3-0, TRAL(3-0)).

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

OAM-Cells and RM-Cells Record Format

OAM/RM and reserved VC cells routing can be performed on any VP/VC combination with the appropriate programming of the E-bit in the VP or VC translation record.

Both F4 and F5 flows are supported in the CUBIT-622. Depending on which flow is routed, two algorithms are used by the CUBIT-622.

The algorithm for FF-flow is depicted in Figure 19. The PT field of the ATM cell header coming in a VP/VC that is set for VP/VC translation (with E-bit set to 1 in the VC translation record) will be checked for all possible values and routed to VCI Page 0 according to the flow shown in Figure 19.

For F4 flow a cell coming in any VP will be sent to VCI Page 0 if the VCI is within numbers 0-31 according to the algorithm shown in Figure 20.

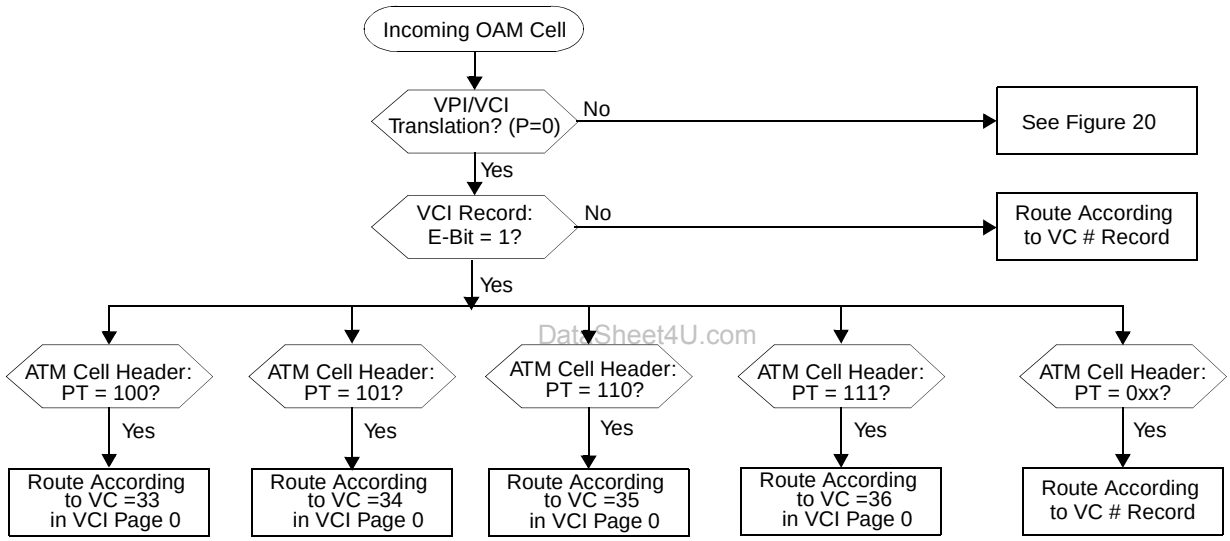


Figure 19. OAM F5 and RM-VCC Cell Routing

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

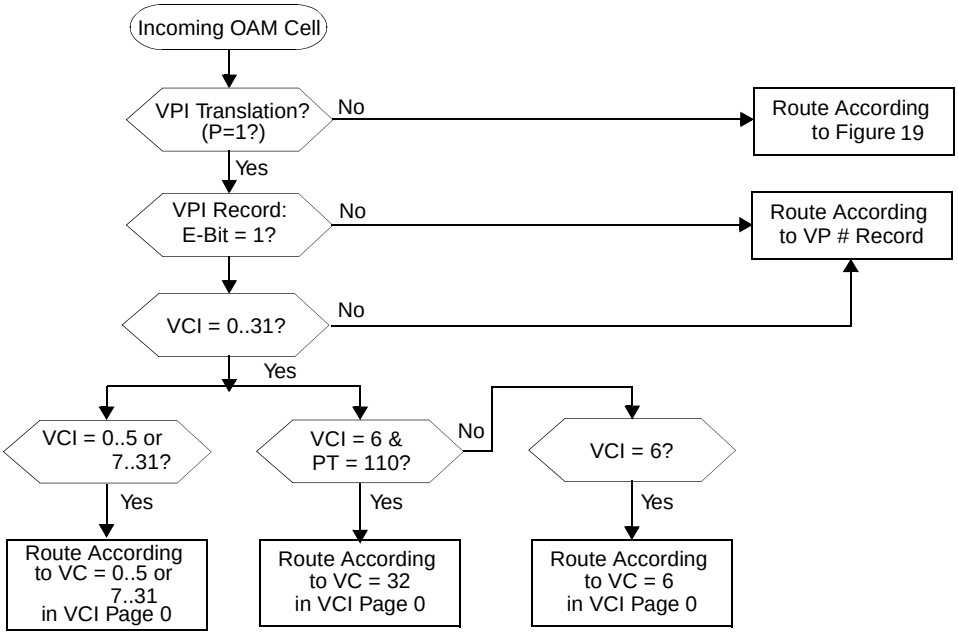
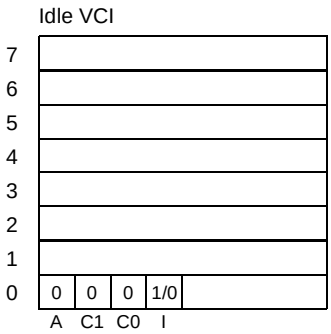


Figure 20. OAM F4 and RM-VPC Cell Routing

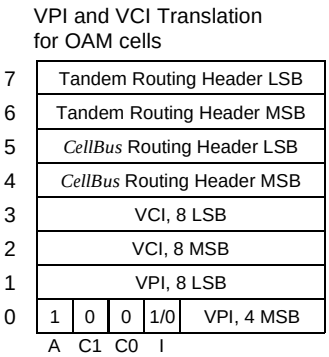
et4U.com DataShee

The corresponding formats for OAM translation records are shown in Figure 21.



If the VCI is inactive (A=0) and not Ignore (I=0), then OAM cells arriving bearing that VCI number are discarded and counted as misrouted. If I=1, they are discarded and not counted as misrouted.

The C1 and C0 bits determine the type of translation for OAM/RM cells received. The coding is explained in the "Translation Records Control Bits" section.



If the VCI is active (A=1), then the VPI and VCI numbers to be inserted in the cell, and the *CellBus* Routing Header and Tandem Routing Header to be used, are read from the OAM translation record at the positions indicated.

Note: OAM/RM Translation Records are optional. They are located in VCI page zero.

Figure 21. OAM/RM-Cells Translation Record Formats

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MULTICAST SESSION MEMORY

A multicast address data cell is sent to all CUBIT-622s, and each CUBIT-622 will check the multicast session (max 256) and lookup in its Multicast Session Table (MST) if this device should participate in the multicast session. Each of the 256 multicast session addresses has a 64-bit list of destination ports in registers 200H to 9FFH to which a cell can be forwarded (max. all 64 ports). For each bit that is set to 1 in the list corresponding to the received multicast address, the cell is forwarded to the port corresponding to that bit. Each CUBIT-622 can be configured to accept any or all of the 256 possible multicast sessions and send them to any or all of the possible 64 destination ports by setting the bit in the corresponding location in the table. The multicast process adopted is a pointer replication process as opposed to a cell duplication process. Pointers to a given multicast cell are added to their appropriate destination queues.

If any port becomes disabled, the active bit (see Table 3, “FIFO Pointer Table Map”, on page 34) corresponding to that port should be reset and then disable the UTOPIA port by resetting to zero the corresponding PHYEN bit in registers A01H to A08H. Resetting the active bit will prevent the cell from being replicated to the queue for that port.

Note: In order to update the leaves associated with a particular multicast session, eight consecutive memory addresses must be written, starting with the address corresponding to Ports 7-0 (i.e., starting with 200H for session number 0, through 9F8H for session number 255).

Multicast control cells have their own multicast session table for up to 256 sessions. Multicast control cells are only accepted by *CellBus* devices (depending on the state of the control multicast session table) and not replicated to multiple ports. These cells are sent to the Control Receive Queue for extraction to the host processor. The multicast session table memory contains 1 bit for each session and is located in address 0xB00 - 0xBFF.

et4U.com DataShee

THE *CellBus* INTERFACE

DataSheet4U.com

Thirty-seven lines comprise the *CellBus* interface, as shown in Figures 1 and 5. There are thirty-two data lines, with Frame, Acknowledge, and Congestion Indicator lines, all sourced by a CUBIT-622 device, and two Clock lines sourced by external drivers. Additional technical information for implementing a *CellBus* Bus with circuit cards plugged into backplane connectors is provided in a document entitled “TranSwitch *CellBus* Bus Reference Design Guideline for CUBIT-*Pro* Applications”, Revision 0.5 dated February 19, 1999, which is available as a CUBIT-*Pro* document from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

Operation with Internal GTL+ Transceivers

Gunning Transceiver Logic (GTL+) transceivers for *CellBus* Data, Frame, Acknowledge, and Congestion Indicator lines are contained internally in the CUBIT-622, along with two clock line GTL+ receivers. Each of the drivers has a typical current sink capability of 45 mA and is capable of driving a bus on a card or on a backplane directly. Each of the GTL+ lines is to be pulled up at each of its ends by a 50 ohm (± 5%) resistor (metal film or carbon composition) to a +1.5 V low-impedance supply. Each end of each line should have a filtering capacitor connected from the +1.5 V supply to ground, as shown in Figure 22.

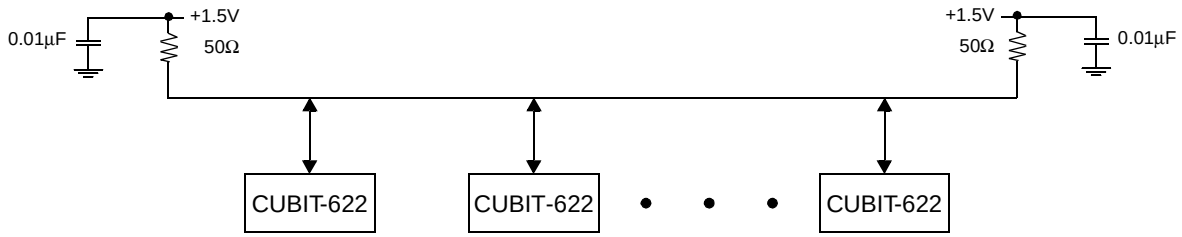


Figure 22. External Circuit Requirements for GTL+ Transceivers

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

In the CUBIT-622 lead configuration, all of the leads involved with the *CellBus* interface are aligned along one side of the package (between lead rows AB and W). This side of the package must be aligned toward the board connector, or toward the *CellBus*, with as little board trace length as possible between the leads and the connector or *CellBus*, to maximize operating speed.

Clock Source

Two GTL+ clock signals must be driven to the *CellBus* from an external source. These are the write clock, $\overline{\text{CBWC}}$, and the read clock, $\overline{\text{CBRC}}$. A phase relationship keeping the write clock between 0.5 and 4 nanoseconds behind the read clock is needed to ensure proper synchronous *CellBus* operation. When the clock driver is driven from the center of the backplane (i.e., no greater than half a backplane length from any card) a minimum phase distance of 1.0 ns or more must be maintained. When the driver is at one of the ends, a more conservative 2-4 ns minimum is required. In any *CellBus* implementation, on the backplane and on each card, care must be taken to ensure that these two lines are routed together. The capacitive and inductive loadings of the two lines should be as nearly equal as possible, to maintain performance. At the drive point, a delay line should be used to maintain a stable delay, and the read and write clock drivers must be units of the same integrated circuit package. All of these precautions will ensure the most stable clocks and permit the highest possible operating speed.

CellBus Bus Arbiter Selection

One copy of the *CellBus* Bus Arbiter circuitry is included inside each CUBIT-622 device. Enabling of the Arbiter on a particular CUBIT-622 is done by connecting the $\overline{\text{ENARB}}$ lead of that device to ground (V_{SS}). Only one Arbiter may be enabled at a time. It is the responsibility of the overall system control to decide which CUBIT-622 will have its Arbiter enabled, and to enable it. Failure of an Arbiter can be detected by using the NOGRT indications. If multiple CUBIT-622s are indicating NOGRT failures, an Arbiter failure is indicated. It is again the responsibility of system control to enable another *CellBus* Arbiter. Upon switching from one Arbiter to another, the receiving devices on the *CellBus* will automatically re-align to the new frame position within one *CellBus* frame.

OUTLET-SIDE QUEUE MANAGEMENT

The CUBIT-622 contains an external queuing mechanism, similar to that implemented in the ASPEN device (TXC-05810). An external local memory is required by the CUBIT-622 for cell queuing; there is no large internal buffering mechanism as in the CUBIT-*Pro*. The CUBIT-622 integrates a complete memory controller to support this local memory. The on-chip memory controller provides a 'glueless' interface to a high speed synchronous SRAM (SSRAM). No external timing or control logic is required. The SSRAM memory controller directly addresses up to 16 Mbits of external memory to enable a maximum queue size of greater than 30,000 cells. The memory controller is configured to use 32-bit memories.

Free List

The CUBIT-622 incorporates a data structure known as a “Free List”, which is a linked list of all available cell buffers in external SSRAM. Each buffer consists of 16 sequential 32-bit words. The data contained in the last entry (sixteenth address) of each buffer points to the address location of the beginning of the next buffer. The Free List must initially be configured by the user after the CUBIT-622 has exited the Reset state and should include all SSRAM cell buffers in a sequential linked list (i.e., buffer 0 points to buffer 1, etc.).

The “Head of Free List” is an address which corresponds to the first SSRAM memory location that will be used for cell storage. This initial Head of Free List address is contained in the Base Pointer Address BPSQS(9-0) in registers 10FH and 10EH (LSB). The Base Pointer Address is 0100H by default upon Reset. The user may change the starting location of the Free List by writing the appropriate value to the Base Pointer Address and then setting the NFL bit (bit 2 in register 100H) to 1. For instance, the Base Pointer Address may be selected to be 0000H if user-defined SSRAM storage space is not needed in lower memory.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

The pointer in the last entry of the Free List linked list must be written with 80000000H to signify the end of the list.Initialization of the Free List consists of the operations described below, where the SSRAM address numbers refer to 32-bit words.

Free List Configuration

1) Set control bit DATA/$\overline{\text{CTRL}}$ to 1 and control bit QMR/$\overline{\text{W}}$ to 0 (bits 1 and 0 in register 130H). This will configure the queue manager to perform only write operations to the SSRAM.
2) Write data (address of next buffer) corresponding to “First Link Address” using the 24-bit QMADD and 32-bit QMDATA registers (registers 131H to 133H and 134H to 137H, respectively).

QMADD	=	First Link Address location	=	BP + 0FH
QMDATA	=	Address of next buffer	=	BP + 0FH + 01H

3) Write data (address of next buffer) corresponding to “Next Link Address” using the 24-bit QMADD and 32-bit QMDATA registers (registers 131H to 133H and 134H to 137H, respectively).

QMADD	=	Next Link Address	=	BP + 0FH	+ 10H
QMDATA	=	Address of next buffer	=	BP + 0FH + 01H	+ 10H

4) Continue as in steps 2 and 3 until the last cell buffer is reached.

et4U.com DataShee

5) Write data corresponding to the Last Link Address

DataSheet4U.com

QMADD	=	Last Link Address	=	BP + 0FH + 10H X (length of Free List - 1)
QMDATA	=	End of Free List code =	80000000H	

The QMADD and QMDATA registers are defined as follows:

QMADD(23….0) = A2.A1.A0 (3-byte address) with A0 being the LSB

QMDATA(31….0) = D3. D2. D1. D0 (4 bytes of data) with D0 being the LSB

Note: Data byte D0 located at address 137H must be the last byte written to initiate the memory write. Address byte A2 located at address 133H must be the last byte written to initiate a read.

Queue Description

The outlet data cell FIFO structure can be treated as four individual queues for traffic of different service types per physical port. The four priority-queue split is typically into CBR cells, VBR-rt (real-time) cells, VBR-nrt (non real-time) cells, and UBR/GFR cells, in decreasing order of outlet service priority. This allows for delay minimization of critical service types, and for more efficient traffic management. CBR queues have higher priority than VBR-rt queues. VBR-rt queues have higher priority than VBR-nrt queues. VBR-nrt service class will have priority over UBR/GFR traffic.

The Tandem Routing Header bits 11-4 are used for queue selection (bits 11-6 indicate port number and bits 5-4 indicate priority). Note: The priority field is encoded as follows: CBR ‘00’, VBR-rt ‘01’, VBR-nrt ‘10’, UBR/GFR ‘11’.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

FIFO Pointer Table RAM (FPTRAM)

The FIFO Pointer Table (FPTRAM, see Table 3) is a data structure located within 32-bit wide memory internal to the CUBIT-622 and it contains information associated with each queue. There is one FIFO Pointer Table (FPT) associated with each outlet queue destination port. Each FPT consists of three 32-bit words located at three consecutive addresses. There are a total of 256 (64 ports x 4 queues) FPTs located between addresses 00H and 3FFH in FPTRAM. The FPT contains the Queue Limit, Cell Count, Read Pointer, and Write Pointer for each of the 256 queues.

Eight additional 32-bit wide memory locations (FPTRAM addresses 400H through 407H) are used to store the activity bits associated with each queue.

The FPT must be initialized prior to cell reception by setting the Read Pointer, Write Pointer And Cell Count all equal to zero. The Queue Limit will be loaded with the desired queue size. In addition, the selected queues must be activated by setting the appropriate queue activity bit(s) to 1.

The FPT is accessed through the Queue Manager Address and Data registers located in registers 131H to 133H and 134H to 137H respectively.

Please note that the SSRAM is also accessed via these registers. The SSRAM select bit (DATA/$\overline{\text{CTRL}}$), located in bit 1 of register 130H, is used to select either the SSRAM (1 for DATA) or the FPT (0 for $\overline{\text{CTRL}}$).

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Table 3. FIFO Pointer Table Map

Address (Hex)	Mode	PHY	Service Class	Bits 31 - 0			
0	R/W	0	0	RP(3:0)	CC(13:0)	QL(13:0)	
1	R/W			WP(16:0)		RP(18:4)	
2	R/W			Reserved			WP(18:17)
3	R/W			Reserved			
4	R/W		1	RP(3:0)	CC(13:0)	QL(13:0)	
5	R/W			WP(16:0)		RP(18:4)	
6	R/W			Reserved			WP(18:17)
7	R/W			Reserved			
8	R/W		2	RP(3:0)	CC(13:0)	QL(13:0)	
9	R/W			WP(16:0)		RP(18:4)	
0xA	R/W			Reserved			WP(18:17)
0xB	R/W			Reserved			
0xC	R/W		3	RP(3:0)	CC(13:0)	QL(13:0)	
0xD	R/W			WP(16:0)		RP(18:4)	
0xE	R/W			Reserved			WP(18:17)
0xF	R/W			Reserved			
0x10	R/W	1	0	RP(3:0)	CC(13:0)	QL(13:0)	
0x11	R/W			WP(16:0)		RP(18:4)	
0x12	R/W			Reserved			WP(18:17)
0x13	R/W			Reserved			
.....							
0x3FC	R/W	63	3	RP(3:0)	CC(13:0)	QL(13:0)	
0x3FD	R/W			WP(16:0)		RP(18:4)	
0x3FE	R/W			Reserved			WP(18:17)
0x3FF	R/W			Reserved			
0x400	R/W	31-0	0	Active Bits for PHY 31 - 0, SC0			
0x401	R/W	63-32	0	Active Bits for PHY 63 - 32, SC0			
0x402	R/W	31-0	1	Active Bits for PHY 31 - 0, SC1			
0x403	R/W	63-32	1	Active Bits for PHY 63 - 32, SC1			
0x404	R/W	31-0	2	Active Bits for PHY 31 - 0, SC2			
0x405	R/W	63-32	2	Active Bits for PHY 63 - 32, SC2			
0x406	R/W	31-0	3	Active Bits for PHY 31 - 0, SC3			
0x407	R/W	63-32	3	Active Bits for PHY 63 - 32, SC3			
0x408	R/W			Head of Free List			

where CC = cell count and QL = queue limit, WP = write pointer and RP = read pointer

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Configuration of the FPTRAM consists of the following operations.

FPTRAM Initialization:

1) Set DATA/$\overline{CTRL}$ to 0 and QMR/$\overline{W}$ to 0 (bits 1 and 0 in register 130H). This will configure the Queue Manager to perform only write operations to the FPTRAM.

2) Write first address of FPT corresponding to Port 0, Queue 0:

   QMADD = 000000H
   QMDATA = D3.D2.D1.D0

   D3 = 00H
   D2 = 00H
   D1(7..6) = 00
   D1(5..0) = QLIMIT(13..8)
   D0 = QLIMIT(7..0)

3) Write second address of FPT corresponding to Port 0, Queue 0:

   QMADD = 000001H
   QMDATA = D3.D2.D1.D0

DataSheet4U.com

   D3 = 00H
   D2 = 00H
   D1 = 00H
   D0 = 00H

4) Write third address of FPT corresponding to Port 0, Queue 0:

   QMADD = 000002H
   QMDATA = D3.D2.D1.D0

   D3 = 00H
   D2 = 00H
   D1 = 00H
   D0 = 00H

5) Continue as in steps 2, 3 and 4 for remaining 255 port/queue combinations.

Note: The following steps should only be performed once the device is ready to accept live traffic.

6) Write data corresponding to activity bits for service class 0 queues associated with ports 31 - 0.

   QMADD = 000400H
   QMDATA = D3.D2.D1.D0

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

D3 = QACTIVE(31..24)
D2 = QACTIVE(23..16)
D1 = QACTIVE(15..8)
D0 = QACTIVE(7..0)

7) Write data corresponding to activity bits for service class 0 queues associated with ports 63 - 32

QMADD = 000401H
QMDATA = D3.D2.D1.D0

D3 = QACTIVE(63..56)
D2 = QACTIVE(55..48)
D1 = QACTIVE(47..40)
D0 = QACTIVE(39..32)

8) Repeat steps 6 and 7 for service classes 1, 2 and 3.

Setting Queue Lengths

The lengths of the queues can be configured independently. The procedure for configuring a queue consists of the following steps (refer to Table 3):

1) Select the type of operation, by setting control bit DATA/$\overline{\text{CTRL}}$ (register 130H, bit 1) to 0. A write operation is selected by setting QMR/$\overline{\text{W}}$ to 0 (register 130H, bit 0), while setting the bit to 1 selects a read operation.

2) Set the QMADD Address field (registers 131H - 133H) to the queue number, and parameter to be configured. The queue numbering scheme is 0-3, port 0 queues, 4-7, port 1 queues, etc. The 2 LSBs indicate the priority queues, CBR '00', VBR-rt '01', VBR-nrt '10', UBR/GFR '11'. Note: if the operation selected is a read operation, it will be initiated by setting register 133H of the QMADD field. Completion of the read operation is signaled by the QMACK event bit in register 106H, which is set to 1 to indicate that valid data is in the QMDATA registers.

3) Set the QMDATA field (data parameters, registers 134H - 137H, 32-bit word to be written to control RAM). Each queue has three 32-bit word parameters and requires three successive word writes to 12 successive bytes, as indicated by the QMADD register. The first parameter contains the lower four bits of the read pointer (also set to 0) and two fields that are both 14-bits in length and are the instantaneous cell count for this queue, and the maximum queue depth, respectively. The second parameter is a write pointer (bits 16:0) and the upper 15 bits of a read pointer; both of these must be set to 0 initially. The third parameter is the two upper bits of the write pointer (bits 18:17). The cell count **must** be initialized to 0, and the maximum queue depth **must** be initialized to a non-zero quantity. Writing a value to register 137H initiates the write operation. Completion of the write operation is signaled by the QMACK event bit in register 106H, which sets to 1 to indicate that the data in the QMDATA registers has been stored.

4) The final step involves performing 8 more word writes that set the queues to active status. Each write process involves two parts: A) set QMADD to the appropriate register (000400H through 000407H), and B) set the appropriate QMDATA bit to 1. For example port 4, CBR would correspond to QMADD 000400H, with QMDATA set to XXXX XXXX XXXX XXXX XXXX XXXX XXX1 XXXX, where X is the previous state of the register bit. Each write operation is concluded when event bit QMACK becomes set to 1.

As part of the session tear-down procedure, there may be a need to delete non-empty queues for selected destination ports. The CUBIT-622 accommodates this using the feature DiscardPHY (registers 0D8H to 0DFH). When any of these 64 bits are set to 1, all cells destined for the corresponding ports (PHYs), which are enqueued, are discarded. Note: These registers must be written to in sequence (0D8H to 0DFH) before the discard process will begin. The event bit QD (queue deleted, bit 2 in register 106H) indicates when the discard operation has been completed.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

PHY Disable Procedure

To discard all the cells that are stored in SSRAM associated with a given port or ports, the following procedure should be followed:

1. Disable the UTOPIA port(s) by setting to 0 the PHYEN(63-0) bit(s) in registers A01H to A08H.
2. Set all the queue activity bits associated with the given port(s) to 0 in the FIFO Pointer Table (400H-407H of the FPT – see Table 3, “FIFO Pointer Table Map,” on page 34 for description of FPT access).
3. Set the corresponding DiscardPHY(63-0) bit(s) in registers 0D8H to 0DFH to 1. A write to register 0DFH, DiscardPHY(63-56), triggers the discard logic. The QD flag (register 106H) will be set to 1 and the Discard-PHY(63-0) bit(s) will be reset to 0 when the discard process has been completed.

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

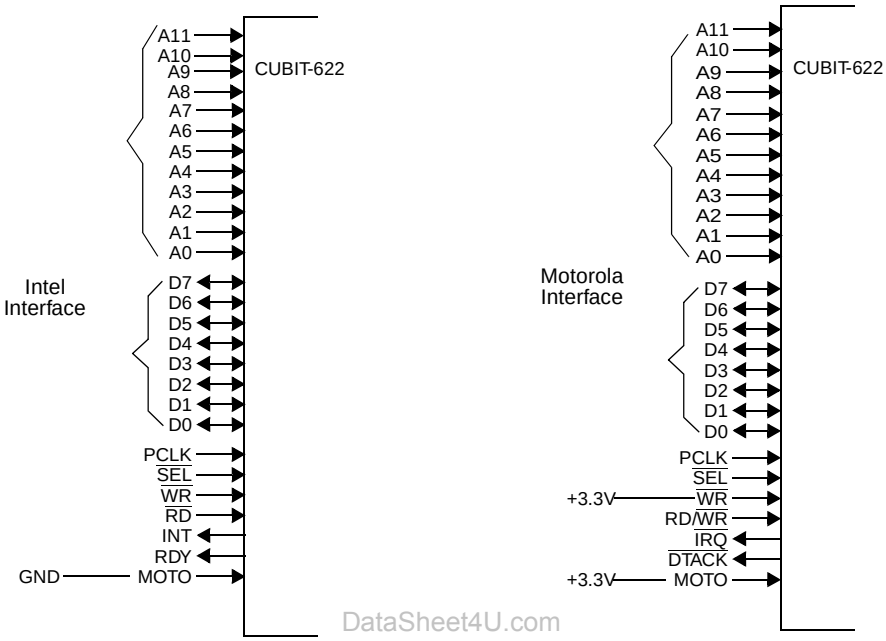
DataSheet4U.com

www.DataSheet4U.com

MICROPROCESSOR INTERFACE

General Description

The CUBIT-622 Microprocessor Port will support an input/output interface characteristic of either Intel or Motorola microprocessors, as shown in Figure 23. The interface type is selected via the lead MOTO.



DataSheet4U.com

Figure 23. Microprocessor Port Interface Connections

The connections for address A(11-0), data D(7-0), processor clock (PCLK) and select ($\overline{SEL}$) are the same for both cases. Differences are listed below.

Intel Mode

Enabled when device strap MOTO is connected to V_{SS} (ground). Connections are as shown in Figure 23. The differences to support Intel mode are:

$\overline{WR}$ lead is low to execute a write command,

$\overline{RD}$ lead is low to execute a read command,

Interrupt INT is active high,

Ready RDY is active high. When set low, it requests microprocessor wait time.

Motorola Mode

Enabled when device strap MOTO is connected to V_{DD} (+3.3V). Connections are as shown in Figure 23. The differences to support Motorola mode are:

$\overline{WR}$ lead is not used and must be pulled up to +3.3 volts,

RD/$\overline{WR}$ lead is high to execute a read command or low to execute a write command,

Interrupt $\overline{IRQ}$ is active low,

Data Transfer Acknowledge $\overline{DTACK}$ is active low. When inactive, and pulled high by an external pull-up resistor, it requests microprocessor wait time.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

32-bit FIFO-like Access

Address 134H is set aside as a word address. This address corresponds to reading/writing the FIFO pointer table (FPT, control parameters for queues), and reading/writing of the external SSRAM. Each word address is a set of four successive addresses, each of which corresponds to a byte in a word. When byte 0 is accessed, the entire word is being cached, allowing the on-chip machines to not participate in the next three accesses, and speeding up those accesses for the microprocessor. The access continues by reading/writing the second third and fourth bytes in the address region. A word access is terminated by reading from the address ending in ....11. Only one word access at a time can be initiated, and it is a requirement that the processor perform all four accesses in succession from address 00. For additional information, please see the description of the QMADD and QMDATA fields in the prior section entitled “Outlet Side Queue Management”.

To write to the FPT, set address 130H to 00H, and then write to addresses 131H to 137H. On writing to address 137H, QMDATA will be written to QMADD. Note QMDATA is the FPT word value and QMADD is the FPT RAM address.

To read from the FPT, set address 130H to 01H, and then write to addresses 131H to 133H. On writing to address 133H, QMDATA will be read from QMADD. Note QMDATA is the FPT word value and QMADD is the FPT RAM address.

To write to the SSRAM, set address 130H to 02H, and then write to addresses 131H to 137H. On writing to address 137H, QMDATA will be written to QMADDD. Note QMDATA is the provided SSRAM data value and QMADD is the SSRAM address to be written.

To read from the SSRAM, set address 130H to 03H, and then write to address 131H to 133H. On writing to address 133H, QMDATA will be read from QMADD. Note QMDATA is the retrieved SSRAM data value and QMADD is the SSRAM address to be read.

DataSheet4U.com

(Note: The read or write cycle is initiated when the last register is written, i.e., 137H for write, 133H for read.)

Interrupts

The CUBIT-622 allows the generation of interrupts based on eighteen different events. The events are latched in three status registers located at addresses 005H, 008H and 106H as shown in Figure 24, Figure 23 and Figure 26. Any of the events will generate an interrupt provided the corresponding interrupt enable bit, located in registers at addresses 006H, 009H and 107H, is set to one.

If any of the events occurs, the corresponding latched status bit will be set to one. All the status bits in a register are cleared when it is read, except for any bits for which the events still persist. Some enabled interrupts may not be cleared in the absence of the *CellBus* clocks. Such interrupts will persist until the clocks are re-applied and the register is then read. It is possible, however, to mask any interrupt regardless of the absence or presence of the *CellBus* clocks, by setting the corresponding enable bit to zero. The events reported are explained below:

1. Status register at address 005H

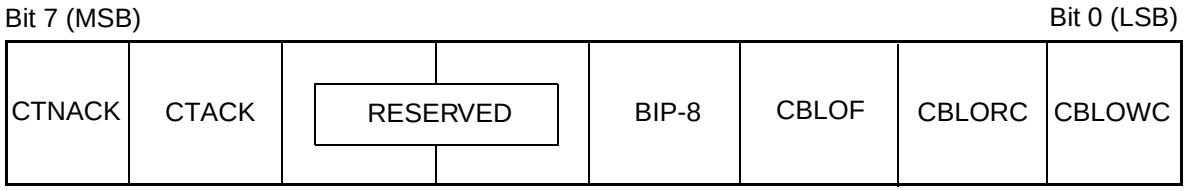


Figure 24. CUBIT-622 Status Register at Address 005H

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CTNACK:

The cell transmitted from the control queue was rejected from the *CellBus*.

CTACK:

The cell transmitted from the control queue was accepted from the *CellBus*.

BIP-8 Error:

If the BIP-8 field (Grant cycle) of the *CellBus* cell body in a cell received from the *CellBus* does not match the calculated BIP-8, this bit is set to 1 (see Figure 6).

CBLOF *CellBus* Loss of Frame Pulse Error:

In the event that the *CellBus* frame pulse is not present for more than 4 consecutive 16-cycle frames, or if the *CellBus* Write Clock is not present, this bit is set to 1.

CBLORC *CellBus* Loss of Read Clock Error:

If the *CellBus* Read Clock is not present, this bit will be set to 1.

CBLOWC *CellBus* Loss of Write Clock Error:

If the *CellBus* Write Clock is not present, this bit will be set to 1.

2. Status register at address 008H

et4U.com DataShee

Bit 7 (MSB) Bit 0 (LSB)

DataSheet4U.com

CRCF	CRQOVF	CRQCAV	INSOC	CTSENT	NOGRT	RESERVED	RESERVED

Figure 25. CUBIT-622 Status Register at Address 008H

CRCF CRC-4 Error:

If the CRC-4 field H(3-0) of the *CellBus* Routing Header in a cell received from the *CellBus* does not match the calculated CRC-4, this bit is set to 1 (see Figure 8).

CRQOVF Control Receive Queue Overflow:

When a cell arrives at the 16-cell control receive queue while it is full, the cell will be discarded and this bit will be set to 1.

CRQCAV Control Receive Queue Cell Available:

When a control cell has been received from the *CellBus* and placed in the control receive queue (registers 060H-093H) this bit will be set to 1. This bit is cleared to 0 after the microprocessor reads the last cell from the control receive queue.

INSOC Inlet False Start of Cell Detection:

In the ATM Layer Emulation UTOPIA 8-bit and 16-bit modes ($\overline{\text{PHYEN}}$ = High) modes, if signal input RxSOC is not present in the second clock cycle after $\overline{\text{RxEnb(3-0)}}$ is asserted, or if RxSOC is asserted before the end of the current cell, the INSOC bit is set to 1.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

In the PHY Layer Emulation UTOPIA 8-bit and 16-bit ($\overline{PHYEN}$ = Low) modes, if TxSOC is not present at the start of a cell, the INSOC bit is set to 1. If the ONLINE bit is set to 0 to disable cell acceptance at the cell inlet, arrival of a cell will cause INSOC to be set to 1. In order to prevent generation of false interrupts, the interrupt-enable bit for INSOC (INTEN4) should also be set to 0 when ONLINE is set to 0.

CTSENT Control Cell Sent:

When the microprocessor requests that a control cell be sent to the *CellBus*, this bit will be set to 1 after the cell has been sent.

NOGRT No Grant:

If the CUBIT-622 device has requested a *CellBus* grant and has not received it after the number of frames indicated by the TIME register (register 00FH), this bit will be set to 1.

3. Status register at address 106H

Bit 7 (MSB)							Bit 0 (LSB)
RESERVED	RESERVED	TRHCRCF	QF	QMACK	QD	MNF	MF

et4U.com

Figure 26. CUBIT-622 Status Register at Address 106H

DataShee

DataSheet4U.com

TRHCRCF Tandem Routing Header CRC-4 Error:

If the CRC field of the Tandem Routing Header in a cell received from the *CellBus* does not match the calculated CRC, this bit is set to 1 (see Figure 8).

QF Queue Full:

After a cell was written into a queue, the queue length reached its limit. When set to 1, this bit is an indication that indiscriminate cell discard will start for this queue.

QMACK Queue Manager Operation Acknowledge:

This bit is set to 1 when a Queue Manager read or write operation has been completed (see control bit QMR/$\overline{W}$ in register 130H)

QD Queue Deleted:

This bit is set to 1 when all cells destined for all ports (n) whose DiscardPHYn configuration bits are set to 1 have been discarded.

MNF Memory Not Full:

This bit is set to 1 if buffer memory is filled and then a cell is taken from the queue. It indicates that memory is now available to store another cell.

MF Memory Full:

This bit is set to 1 after a cell is written in a queue, and there is no space available in memory to enqueue another cell. This is an indication that indiscriminate cell discard will start for all queues.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CONTROL QUEUE TRANSMIT AND RECEIVE

The formats of transmit and receive control cells are shown in Figure 27. Reference to Figure 1 block diagram will be helpful for understanding how cells are handled by the inlet and outlet control queues.

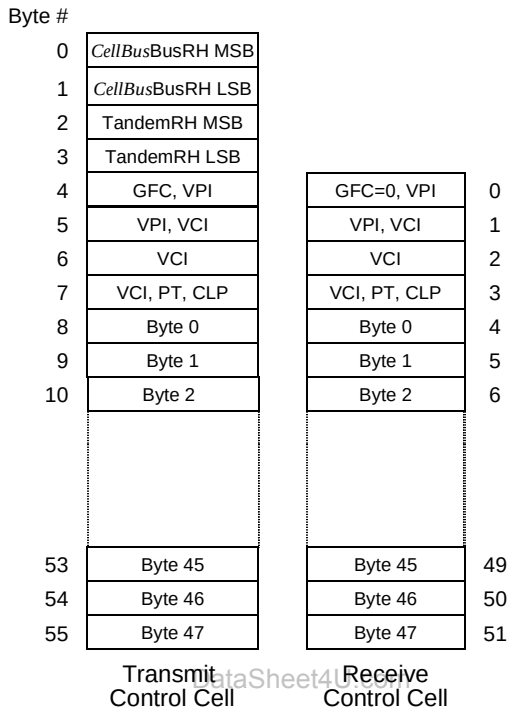


Figure 27. Transmit and Receive Control Cell Formats

A cell can be sent from the microprocessor to the *CellBus* by using the control cell transmit buffer (Inlet Control Queue in Figure 1). This ability allows the microprocessor to send any type of data, control or loopback cell to any CUBIT-622 on the *CellBus*. Before writing, the microprocessor must check the value of the CTRDY bit (Address 00AH, Bit 1). If this is a '0' the control queue can be written to. The microprocessor writes a 56-byte transmit cell with the format shown in Figure 27 to the control cell transmit buffer CTQ(0-55) (Addresses 0A0H-0D7H in the CUBIT-622 memory map). Then a 1 is written to control bit CTRDY (Address 00AH, Bit 1). The cell will be sent to the *CellBus* after any pending data cells, and the CTSENT bit (Address 008H, Bit 3) will then be set to 1 and the CTRDY bit will be reset to 0. The transmit control queue can accept up to 2 cells at a time.

A sixteen-cell FIFO buffer (Outlet Control Queue in Figure 1) is provided for reception of control cells from the *CellBus*, since control cells can arrive from several sources and may have to wait for the microprocessor to accept them from the CUBIT-622. The FIFO output is the 52-byte memory segment CRQ(0-51) at Addresses 060H-093H. When this segment acquires a received control cell the CUBIT-622 sets its interrupt bit CRQCAV to 1 (Address 008H, Bit 5). This bit may be enabled to cause an interrupt to the microprocessor (by setting interrupt enable bit INTEN5 to 1 in Address 009H, Bit 5). When an interrupt or polling process causes the microprocessor to read the interrupt event status register at Address 008H it will detect the CRQCAV indication that a control cell is available for reading. It must then read CRQ(0-51). The CUBIT-622 resets CRQCAV to 0 and places the next control cell in CRQ(0-51) whenever the next cell arrives in the FIFO from the *CellBus*.

Control cell transmission and reception may still be performed regardless of the state of control bit ONLINE (Address 00CH, Bit 7).

DataSheet4U.com

www.DataSheet4U.com

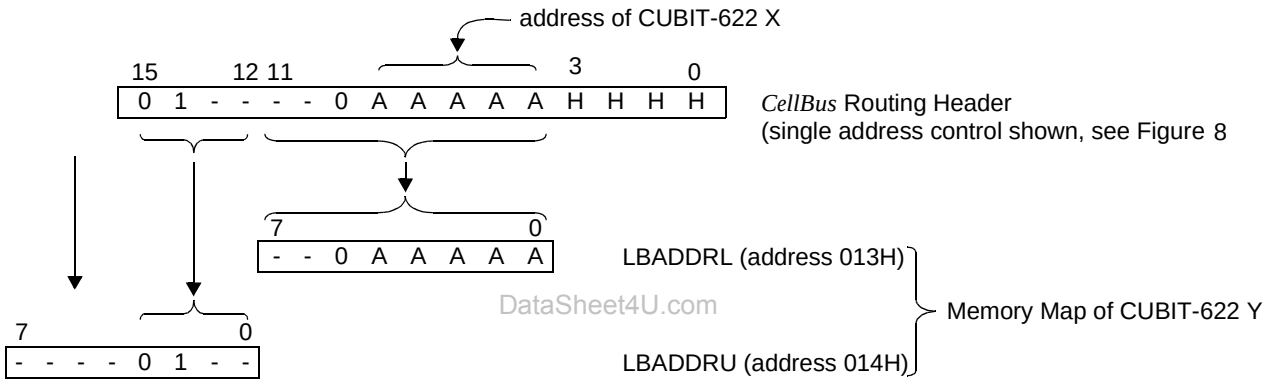
DataSheet4U.com

www.DataSheet4U.com

LOOPBACK CELL TRANSMIT, RECEIVE, AND RELAY

The loopback function is provided for diagnostic purposes. It may be used on-line (ONLINE = 1), or off-line (ONLINE = 0). A loopback path for a cell from CUBIT-622 X to CUBIT-622 Y and back to CUBIT-622 X can be set up by loading the LBADDR registers in addresses 013H and 014H of CUBIT-622 Y with the single address control *CellBus* Routing Header of CUBIT-622 X, as shown in Figure 28. The microprocessor then writes a cell with a single address loopback Routing Header for CUBIT-622 Y into the control transmit buffer (Addresses 0A0H-0D7H) of CUBIT-622 X and causes the cell to be sent. When CUBIT-622 Y receives the cell it will use the contents of LBADDR to form a new Routing Header for the cell and send it back to CUBIT-622 X. CUBIT-622 X will receive the cell and place it in the control receive buffer where it can be examined by the microprocessor.

The above description assumes that the loopback cell originates in the control transmit buffer of CUBIT-622 X, but it could also be received from the inlet port. Any of the six Routing Header formats shown in Figure 8 could actually be loaded in the LBADDRL/U registers of CUBIT-622 Y instead of the single address control *CellBus* Routing Header of CUBIT-622 X, with a corresponding change in the final destination of the loopback cell.



Note: - indicates don't care state

Figure 28. Loading the Loopback Registers

All aspects of system operation are the responsibility of the control system implemented for use of the CUBIT-3 devices. Care must be taken to ensure that no more than one CUBIT-622 is trying to set up a loopback into the same CUBIT-622, or mis-routing will ensue.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MEMORY MAP RESET STATES

The general conditions for resetting the memory map states are:

1. all input clock signals are present, and
2. the $\overline{\text{DEVHIZ}}$ and $\overline{\text{TSTMODE1}}$ input leads are high.

There are two alternative reset conditions that reset the memory map registers 005H through 1FFH and the internal memory words (FPT) to the values shown in the following table:

1. Hardware reset is applied via the $\overline{\text{RESET}}$ input lead. All registers in the device are reset, including the configuration registers (refer to the Memory Map). The reset values of the configuration registers are shown in the table below.
2. Software reset applied via software reset register (10AH). All registers in the device are reset, except the configuration registers. The device will not lose its configuration settings due to a software reset.

Address (Hex)	00A	018	01E	0A0-0D7, 0E0-0FF, 200-BFF	10D	10F	122, 126	123, 127	Others in map	FPT internal words 400-407 (Activity Bits)	Other FPT internal words
Reset Value (Hex or Bin)	40	XX (1)	XX (2)	XX (3)	10 (4)	01 (5)	XX11 1111	FF	00 (6)	00000000	XXXXXXXX (3)

Notes:

1. Reset value depends on content of location 00H in TRAM.
2. Reset value depends on state of leads $\overline{\text{U32}}$, $\overline{\text{ENARB}}$ and $\overline{\text{UA(4-0)}}$.
3. Undefined value after power-up. Pre-existing value is not affected by reset.
4. UBR/GFR limit default value is 1000H in addresses 10D and 10C.
5. Base pointer default value is 0100H in addresses 10F and 10E.
6. Except reserved addresses, which contain undefined values after power-up and hardware reset. These other addresses are unaffected by a software reset.

INITIALIZATION OF SSRAM

Initialization of the SSRAM consists of the following sequence of operations. The SSRAM must be initialized after power-up and after the CUBIT-622 has undergone either a hardware reset or a software reset.

1) Load the Base Pointer Address registers (10FH-10EH) to point to the first cell buffer in the Free List.
2) Load the Free List following the steps outlined in the descriptive section above (page 31).
3) Load the FPT following the steps outlined in the appropriate descriptive sections above (page 33).
4) Set the NFL bit (bit 2 in register 100H) to indicate that a new Free List has been loaded into the SSRAM.
5) Set activity bits to activate desired queues as described above (page 36).

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

BOUNDARY SCAN

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides absorbability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 29. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a 16-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation. The timing of the boundary scan signals is shown in Figure 58.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first.

et4U.com DataShee

Boundary Scan Support

DataSheet4U.com

The following boundary scan test instructions are supported

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- IDCODE
- HIGHZ
- CLAMP

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

IDCODE Instruction

When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

HIGHZ Instruction

The HIGHZ instruction is used to place all outputs in an inactive drive state (high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

CLAMP Instruction

The CLAMP instruction allows the state of the signals driven from the component leads to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component leads will not switch while the CLAMP instruction is selected.

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

BSDL File

A Boundary Scan Description Language (BSDL) file for the CUBIT-622 device is available for download from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

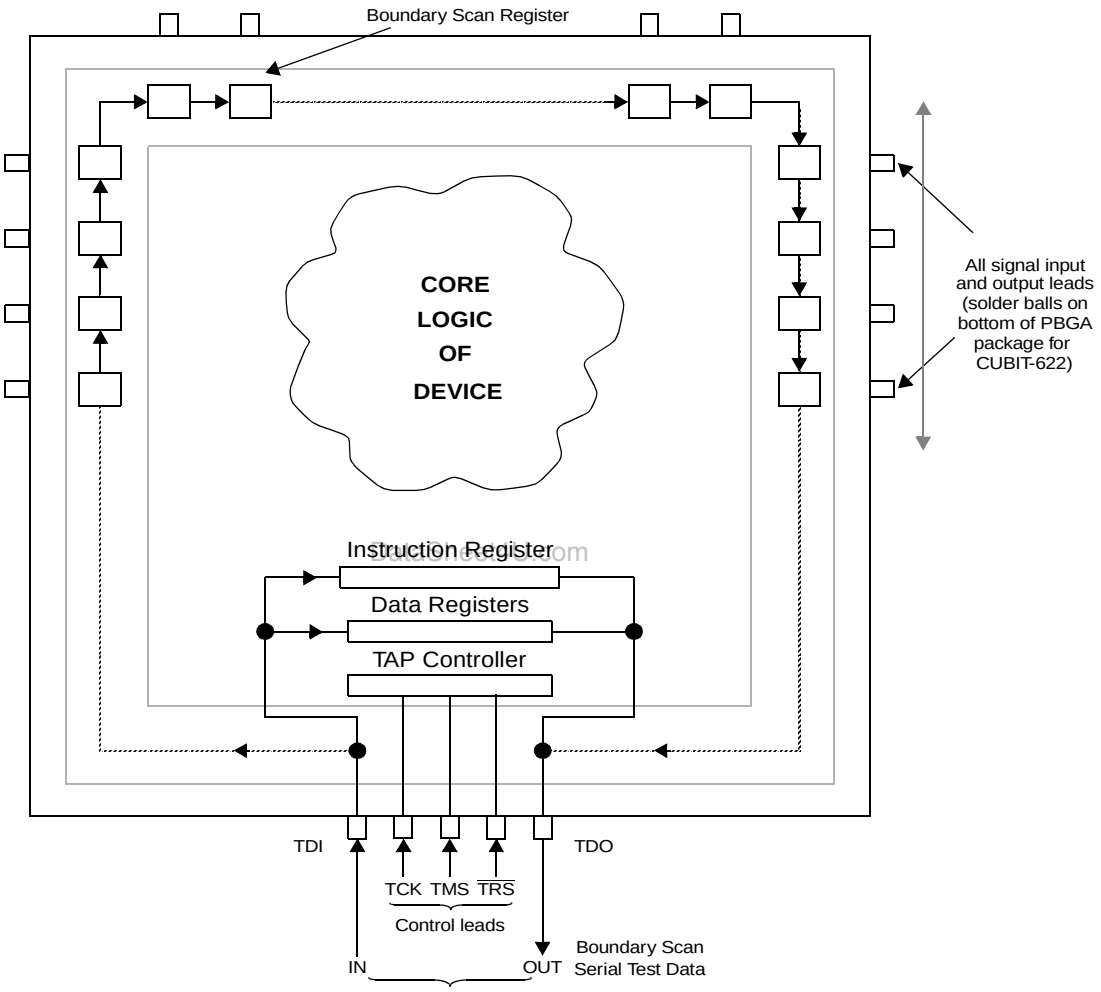


Figure 29. Boundary Scan Top-Level Block Diagram

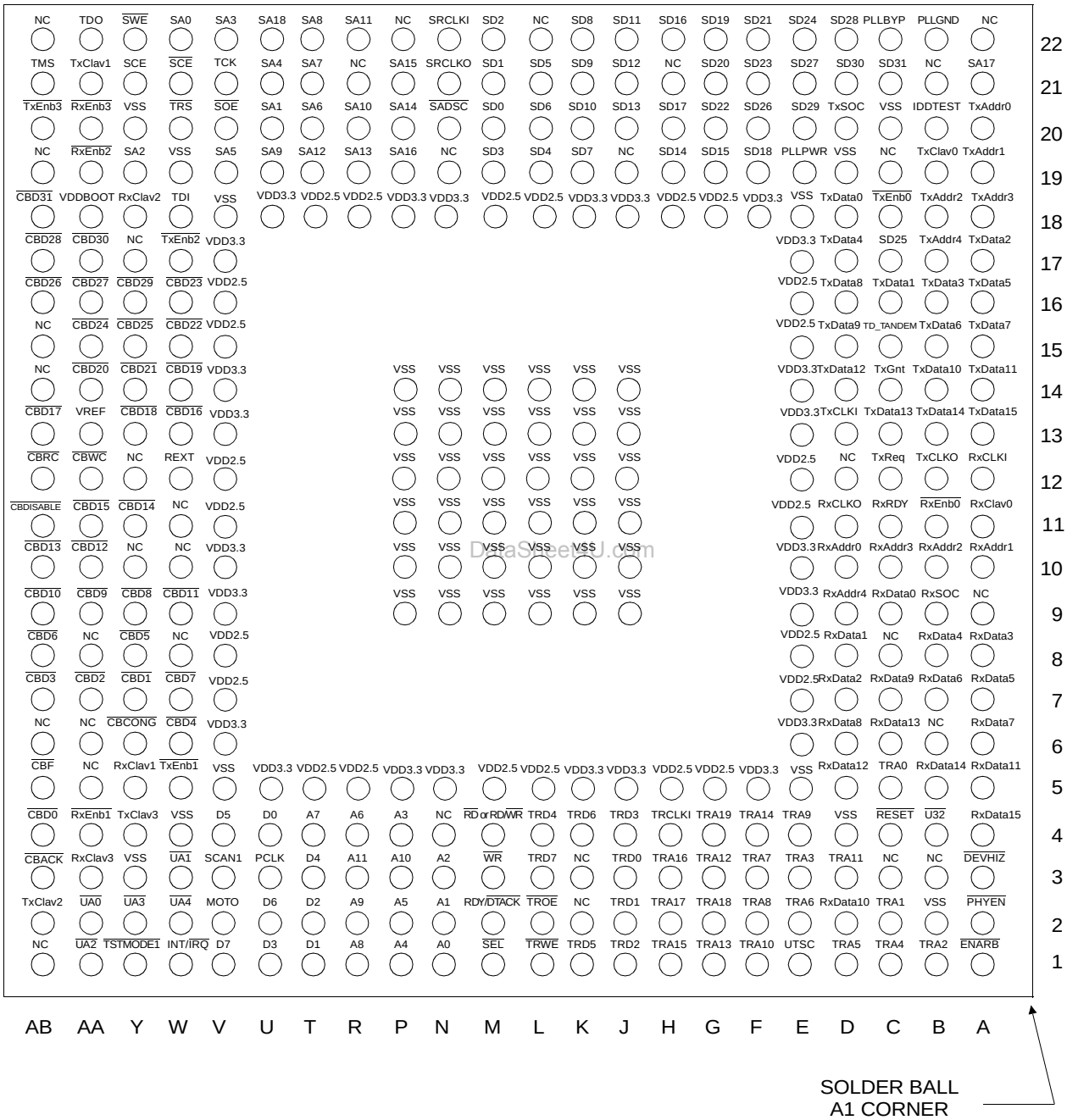
DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

LEAD DIAGRAM

Bottom view of package



Note: The dimensions of the package are shown in Figure 59.

Figure 30. CUBIT-622 TXC-05805 Lead Diagram

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT LEADS

Symbol	Lead No.	I/O/P*	Type	Name/Function
VDD2.5	E7, E8, E11, E12, E15, E16, G5, G18, H5, H18, L5, L18, M5, M18, R5, R18, T5, T18, V7, V8, V11, V12, V15, V16	P		**$V_{DD2.5}$**: +2.5 volt supply voltage, ±5%
VDD3.3	E6, E9, E10, E13, E14, E17, F5, F18, J5, J18, K5, K18, N5, N18, P5, P18, U5, U18, V6, V9, V10, V13, V14, V17	P		**$V_{DD3.3}$**: +3.3 volt supply voltage, ±5%
VSS	B2, C20, D4, D19, E5, E18, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, V5, V18, W4, W19, Y3, Y20	P		**V_{SS}**: Ground, 0 volt reference.
VDDBOOT	AA18	P		**V_{DDBOOT}:** +2.5 volt supply voltage, ± 10%, which must be present for the *CellBus* Bus disable function to work. For compatibility with existing CUBIT-*Pro* +5.0 volt V_{DDBOOT} supplies a resistive divider is required.
PLLPWR	E19	P		**PLLPWR:** +2.5 volt supply voltage, ± 10% for PLL.
PLLGND	B22	P		**PLLGND:** Ground, 0 volt reference for PLL.
NC	A9, A22, B3, B6, B21, C3, C8, C19, D12, H21, J19, K2, K3, L22, N4, N19, P22, R21, W8, W10, W11, Y10, Y12, Y17, AA5, AA6, AA8, AB1, AB6, AB14, AB15, AB19, AB22	--		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions in future upgrades of the device.

* Note: I=Input; O=Output; OD=Open Drain Output; P=Power

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CELL INLET

Symbol**	Lead No.	I/O/P	Type*	Name/Function
RxCLKI	A12	I	CMOS	**Receive UTOPIA Clock Input:** UTOPIA Interface input clock.
RxCLKO	D11	O	TTL 8mA	**Receive UTOPIA Clock Output:** UTOPIA interface output clock used only in ATM layer emulation mode.
$\overline{\text{RxEnb(3-0)}}$	AA20, AA19, AA4, B11	I/O	LVTTL/ TTL 8mA	**Receive Enable:** Input in PHY mode, output in ATM mode. Active low read enable signal for cell input. One Clav/$\overline{\text{Enb}}$ pair for every 16 PHYs.
RxClav(3-0)	AA3, Y18, Y5, A11	I/O	LVTTL/ TTL 8mA	**Receive Cell Available:** Input in ATM mode, output in PHY mode. Active high signal indicating either a cell space is available (PHY mode) or that a cell is available (ATM mode). One Clav/$\overline{\text{Enb}}$ pair for every 16 PHYs.
RxData(15-0)	A4, B5, C6, D5, A5, D2, C7, D6, A6, B7, A7, B8, A8, D7, D8, C9	I	CMOS	**Receive Data:** Input data bus
RxSOC	B9	I	CMOS	**Receive Start of Cell:** Start of Cell Indicator.
RxAddr(4-0)	D9, C10, B10, A10, D10	I/O	LVTTL/ TTL 8mA	**Receive Multi-PHY Address:** Used for polling each port to determine the availability of cell space in PHY mode, and availability of a cell for transfer in ATM mode. Input in PHY emulation mode, output in ATM emulation mode.
RxRDY	C11	I/O	LVTTL/ TTL 8mA	**Receive Ready:** Driven by the secondary UTOPIA master in tandem mode. This signal is asserted high to indicate to the primary master that the secondary can accept a cell on receive. The primary will not begin a RCV cell transfer if this signal is not asserted.

* See Input, Output and Input/Output Parameters section for Type definitions.

** Signals which are active when low or upon their falling edges are shown as negated (overlined).

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CELL OUTLET

Symbol	Lead No.	I/O/P	Type	Name/Function
TxCLKI	D13	I	CMOS	**Transmit UTOPIA Clock Input:** UTOPIA interface input clock.
TxCLKO	B12	O	TTL 8mA	**Transmit UTOPIA Clock Output:** UTOPIA interface output clock used only in ATM layer emulation mode
$\overline{\text{TxEnb(3-0)}}$	AB20, W17, W5, C18	I/O	LVTTL/ TTL 8mA	**Transmit Enable:** Input in PHY mode, output in ATM mode. Active low read enable signal for cell output. One Clav/$\overline{\text{Enb}}$ pair for every 16 PHYs.
TxClav(3-0)	Y4, AB2, AA21, B19	I/O	LVTTL/ TTL 8mA	**Transmit Cell Available:** Input in ATM mode, output in PHY mode. Active high signal indicating either a cell space is available (PHY mode) or that a cell is available (ATM mode). One Clav/$\overline{\text{Enb}}$ pair for every 16 PHYs.
TxReq	C12	I/O	LVTTL/ TTL 8mA	**UTOPIA Bus Request:** When the device is configured as a secondary controller by lead UTSC, this signal is asserted high when requesting the UTOPIA bus. This signal is monitored by the UTOPIA bus arbiter, if the device is configured as primary bus master.
TxGnt	C14	I/O	LVTTL/ TTL 8mA	**UTOPIA Bus Grant:** When configured as a primary controller by lead UTSC, this signal is asserted high when granting control of the UTOPIA bus. This signal is monitored, when the device is configured as a secondary bus controller by the UTSC lead.
TxData(15-0)	A13, B13, C13, D14, A14, B14, D15, D16, A15, B15, A16, D17, B16, A17, C16, D18	O	TTL 8mA	**Transmit Data:** Output data bus
TxSOC	D20	O	TTL 8mA	**Transmit Start of Cell:** Start of Cell Indicator.
TxAddr(4-0)	B17, A18, B18, A19, A20	I/O	LVTTL/ TTL 8mA	**Transmit Multi-PHY Address:** Used for polling each port to determine the availability of a cell in PHY emulation mode, and availability of a cell space for transfer in ATM emulation mode. Input in PHY emulation mode, output in ATM emulation mode.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

CellBus **BUS PORT**

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{CBACK}}$	AB3	I/O	GTL+	*CellBus* **Bus Acknowledge:** Active low acknowledge.
$\overline{\text{CBCONG}}$	Y6	I/O	GTL+	*CellBus* **Bus Congestion Indicator:** Active low congestion indicator. Set via control bit CONG or when the *CellBus* rate decoupling FIFO is full.
$\overline{\text{CBD(31-24)}}$	AB18, AA17, Y16, AB17, AA16, AB16, Y15, AA15	I/O	GTL+	*CellBus* **Bus Data:** Active low 32-bit parallel data input/output bus.
$\overline{\text{CBD(23-16)}}$	W16, W15, Y14, AA14, W14, Y13, AB13, W13	I/O	GTL+	
$\overline{\text{CBD(15-8)}}$	AA11, Y11, AB10, AA10, W9, AB9, AA9, Y9	I/O	GTL+	
$\overline{\text{CBD(7-0)}}$	W7, AB8, Y8, W6, AB7, AA7, Y7, AB4	I/O	GTL+	
$\overline{\text{CBF}}$	AB5	I/O	GTL+	*CellBus* **Bus Frame Pulse:** Active low pulse that occurs once for every 16 or 32 *CellBus* clock cycles, corresponding to selection of 16-user or 32-user modes.
$\overline{\text{CBRC}}$	AB12	I	GTL+	*CellBus* **Bus Read Clock:** Accepts data from *CellBus*. Falling edge used for data transfer.
$\overline{\text{CBWC}}$	AA12	I	GTL+	*CellBus* **Bus Write Clock:** Puts data on the *CellBus*. Falling edge used for data transfer.
$\overline{\text{CBDISABLE}}$	AB11	I	CMOS2.5	*CellBus* **Bus Disable:** Active low signal to tristate all *CellBus* outputs of the device regardless of the state of its V_{DD} power supply. (This signal is not part of the *CellBus* Bus.)
VREF	AA13	I	Reference Voltage	**VREF:** Reference voltage for GTL+ receivers. VREF is 2/3 V_{tt}, where V_{tt} is the backplane termination voltage (nominally Vtt = +1.5V). The input connection to this lead is not part of the *CellBus* Bus.
REXT	W12	I	External Resistor	REXT is to be connected to VSS via an external 1.65 kΩ ± 1% resistor, and is used for temperature compensation. This lead is not part of the *CellBus* Bus.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

SSRAM INTERFACE PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
SD(31-0)	C21, D21, E20, D22, E21, F20, C17, E22, F21, G20, F22, G21, G22, F19, H20, H22, G19, H19, J20, J21, J22, K20, K21, K22, K19, L20, L21, L19, M19, M22, M21, M20	I/O	LVTTL/ TTL 8mA	**SSRAM Data:** Bidirectional 32-bit data bus used for reading input and writing output data from/to the external SSRAM. SD0 is the LSB. High is logic 1.
SA(18-0)	U22, A21, P19, P21, P20, R19, T19, R22, R20, U19, T22, T21, T20, V19, U21, V22, Y19, U20, W22	O	TTL 8mA	**SSRAM Address:** 19-bit address output bus used to select external SSRAM address for read or write access. SA0 is the LSB. High is logic 1.
$\overline{\text{SCE}}$	W21	O	TTL 8mA	**SSRAM Chip Select:** Active low output signal enables the interface to the SSRAM and allows the transfer of information between the CUBIT-622 and the selected SSRAM.
SCE	Y21	O	TTL 8mA	**SSRAM Chip Select:** Active high output signal that mirrors $\overline{\text{SCE}}$ lead functionality.
$\overline{\text{SOE}}$	V20	O	TTL 8mA	**SSRAM Output (Read) Enable:** This output signal is asserted low to initiate a SSRAM read cycle.
$\overline{\text{SWE}}$	Y22	O	TTL 8mA	**SSRAM Write Enable:** This output signal is asserted low to initiate a SSRAM write cycle.
SRCLKI	N22	I	CMOS	**SSRAM Clock Input:** Clock input for DMA interface and external SSRAM interface.
SRCLKO	N21	O	TTL 8mA	**SSRAM Clock Output:** Clock output from DMA interface to external SSRAM interface, sourced from SRCLKI.
$\overline{\text{SADSC}}$	N20	O	TTL 8mA	**SSRAM Address Controller**: Active low output used to interrupt any ongoing burst, causes new external address to be registered. A read or write cycle is initiated if the corresponding enable outputs are active.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MICROPROCESSOR PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
A(11-0)	R3, P3, R2, R1, T4, R4, P2, P1, P4, N3, N2, N1	I	CMOS	**Address Bus:** 12-bit address lines from microprocessor, used to address CUBIT-622 register memory. A0 is LSB. High is logic 1.
D(7-0)	V1, U2, V4, T3, U1, T2, T1, U4	I/O	TTL/ TTL 8 mA	**Data Bus:** Bidirectional 8-bit data lines used for transferring data to and from microprocessor. D0 is LSB. High is logic 1.
INT/$\overline{IRQ}$	W1	OD	OD 8 mA	**Interrupt:** Active high for Intel, active low for Motorola. This output is an open drain buffer which requires an external pull-up resistor.
MOTO	V2	I	CMOS	**Motorola Mode:** Selects Motorola operation if high, Intel if low.
PCLK	U3	I	CMOS	**Processor Clock:** Rising edge used for data transfer. The maximum frequency of this clock is 50 MHz.
$\overline{RD}$ or RD/$\overline{WR}$	M4	I	CMOS	**Read/Write:** Data transfer command for CUBIT-622 memory. Read (low) for Intel. Read (high) / Write (low) for Motorola.
RDY/$\overline{DTACK}$	M2	OD	OD 8 mA	**Ready or Data Transfer Acknowledge:** Active high Ready for Intel, active low Data Transfer Acknowledge for Motorola. This output is an open drain buffer which requires an external pull-up resistor.
$\overline{SEL}$	M1	I	CMOS	**Select:** Active low signal to enable data transfer.
$\overline{WR}$	M3	I	CMOS	**Write:** Active low write command for transferring data to CUBIT-622 memory in Intel mode. This input must be held high in Motorola mode.

TRANSLATION RAM PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
TRA(19-0)	G4, G2, H2, H3, H1, F4, G1, G3, D3, F1, E4, F2, F3, E2, D1, C1, E3, B1, C2, C5	O	TTL 4mA	**Translation RAM Address Bus:** 20-bit address output for up to 1M byte Translation RAM. TRA0 is LSB. High is logic 1.
TRD(7-0)	L3, K4, K1, L4, J4, J1, J2, J3	I/O	TTL/ TTL 4 mA	**Translation RAM Data Bus:** Bidirectional 8-bit data bus. TRD0 is LSB. High is logic 1.
$\overline{TROE}$	L2	O	TTL 4 mA	**Translation RAM Output Enable:** Active low output (read) enable.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{TRWE}}$	L1	O	TTL 4 mA	**Translation RAM Write Enable:** Active low write enable.
TRCLKI	H4	I	CMOS	**Translation RAM Clock Input:** Rising edge used for data transfer. The maximum frequency of this clock is 75 MHz.

CONTROL STRAPS

Symbol*	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{DEVHIZ}}$	A3	I	CMOSpu	**Device High Impedance:** Active low signal to set all outputs (except TDO) to high-impedance (Hi-Z) state.
$\overline{\text{ENARB}}$	A1	I	CMOSpu	**Enable Arbiter:** Active low signal to enable *CellBus* Arbiter and Frame Pulse Generator functions. Only one CUBIT-622 device on the *CellBus* can be enabled at any time.
$\overline{\text{UA(4-0)}}$	W2, Y2, AA1, W3, AA2	I	CMOSpu	**Unit Address:** Five active low device identity straps, used to set the *CellBus* ID (0-31) of each CUBIT-622 device in a system containing up to 32 devices. For example, the ID is 0 if all leads are high.
$\overline{\text{U32}}$	B4	I	CMOSpu	**Unit 32:** Control strap for setting maximum number of CUBIT-622s that can be connected to the *CellBus* Bus. Set low for 32 CUBIT-622s, high (or floating) for 16.
$\overline{\text{PHYEN}}$	A2	I	CMOSpu	**PHY Layer Enable:** A low enables PHY Layer emulation in UTOPIA and 16-bit modes.
UTSC	E1	I	CMOSpu	**UTOPIA Tandem Secondary Controller:** A high enables the CUBIT-622 as UTOPIA secondary master to be used for tandem operation. A low enables the CUBIT-622 as UTOPIA primary master.
TD_TANDEM	C15	I	CMOSpd	**Tandem Enable**: A high enables Tandem mode.

* Note: All of these control straps (except UTSC and TD_TANDEM) are active low inputs. They are pulled up internally and will be inactive if left unconnected. They must be set low to enable the associated function. TD_TANDEM is pulled down internally if left unconnected, disabling tandem operation so that the UTSC state has no effect. UTSC is pulled up internally, to default to operation as a secondary master in tandem mode if it left unconnected.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

RESET AND TEST LEADS (INCLUDING TEST ACCESS PORT FOR BOUNDARY SCAN)

Symbol	Lead No.	I/O/P	Type	Name/Function
TDO	AA22	O	TTL 4mA	**Test Data Output:** Output for data and test instructions from internal test registers for Boundary Scan.
$\overline{\text{TRS}}$	W20	I	CMOSpu	**Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for power-up initialization as well.
TMS	AB21	I	CMOSpu	**Test Mode Select:** Mode select for Boundary Scan.
TDI	W18	I	CMOSpu	**Test Data Input:** Data and test instruction input for Boundary Scan.
TCK	V21	I	CMOSpu	**Test Clock:** Clocks in TMS and TDI signals on rising edge.
$\overline{\text{RESET}}$	C4	I	CMOS	**Reset:** Active low device reset (minimum duration 300 nanoseconds). To release all logic blocks from the reset state, provide four (4) low-to-high transitions on the clock which clocks the related logic.
$\overline{\text{TSTMODE1}}$	Y1	I	--	**Test Mode:** Active low signal to enable device test by manufacturer. Tie to V_{DD}.
SCAN1	V3	I	--	**Scan 1:** Internal test function. Tie to V_{SS}.
PLLBYP	C22	I	CMOSpd	**PLL Bypass**: This lead is used for test purposes. A high on this lead enables a bypass of the PLL circuit. Tie to V_{SS} for normal operation.
IDDTEST	B20	I	--	**IDD Test:** Tie to GND. This lead is used for factory test (When set high, GTLP receivers are turned off).

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (I/O)	$V_{DD3.3}$	-0.3	+3.63	V	Note 1
Supply voltage (Core)	$V_{DD2.5}$	-0.3	+2.75	V	Note 1
DC input voltage	V_{IN}	-0.5	$V_{DD3.3}$ + 0.3	V	Note 1
Storage temperature range	T_S	-40	125	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute Value 2000		V	Note 3
Latch-Up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.

et4U.com DataShee

THERMAL CHARACTERISTICS

DataSheet4U.com

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		22		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{DD3.3}$	3.14	3.3	3.47	V	
$I_{DD3.3}$	20	21	22	mA	See Notes 1 and 2
$P_{DD3.3}$	63	68	76	mW	See Notes 1 and 2
$V_{DD2.5}$	2.38	2.5	2.63	V	See Note 3
$I_{DD2.5}$	421	443	465	mA	See Notes 1, 2 and 3
$P_{DD2.5}$	1002	1108	1223	mW	See Notes 1, 2 and 3
V_{PLLPWR}	2.38	2.5	2.63	V	
I_{PLLPWR}	5.7	6	6.3	mA	See Notes 1 and 2
P_{PLLPWR}	13.5	15	16.5	mW	See Notes 1 and 2
Total Power	1079	1191	1315	mW	

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.
3. V_{DDBOOT} is included in P,I,V numbers for $V_{DD2.5}$ supply.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR CMOS(1)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0(3)		$V_{DD3.3}$+0.3	V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}	-0.3		$0.3 * V_{DD3.3}$(2)	V	$3.14 \le V_{DD3.3} \le 3.46$
Input leakage current	-10	1	10	µA	$V_{DD3.3}$=3.46, V_{IN}=0 to 3.46
Input capacitance		5		pF	

INPUT PARAMETERS FOR CMOS2.5

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.3			V	$2.38 \le V_{DD2.5} \le 2.62$
V_{IL}			0.9	V	$2.38 \le V_{DD2.5} \le 2.62$
Input leakage current	-10		10	µA	$V_{IN}=V_{DD2.5}$ or V_{SS}
Input capacitance			5	pF	

et4U.com DataShee

INPUT PARAMETERS FOR CMOSpd (CMOS WITH INTERNAL PULL-DOWN)(1)

DataSheet4U.com

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0(3)		$V_{DD3.3}$+0.3	V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}	-0.3		$0.3 * V_{DD3.3}$(2)	V	$3.14 \le V_{DD3.3} \le 3.46$
Input current	21.5	61.9	137	µA	$V_{DD3.3}$=3.46, V_{IN}=0 to 3.46
Input leakage current	-10	1	10	µA	$V_{DD3.3}$=3.46, V_{IN}=0 to 3.46
Input capacitance		5		pF	

INPUT PARAMETERS FOR CMOSpu (CMOS WITH INTERNAL PULL-UP)(1)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0(3)		$V_{DD3.3}$+0.3	V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}	-0.3		$0.3 * V_{DD3.3}$(2)	V	$3.14 \le V_{DD3.3} \le 3.46$
Input current	-67.4	-132.4	-223	µA	V_{DD}=3.46, V_{IN}=0 to 3.46
Input leakage current	-10	1	10	µA	V_{DD}=3.46, V_{IN}=0 to 3.46
Input capacitance		5		pF	

(1): This table defines the thresholds that allow CMOS input pads to be compatible for the TTL input thresholds of the input only pad. See (2) and (3).

(2): The threshold of logic low is specified as the CMOS's V_{IL}max that is compatible with the TTL's V_{IL} or 0.8V in all cases of $V_{DD3.3}$.

(3): The threshold of logic high is specified as the minimum TTL's V_{IH} or 2.0V that ensures compatibility with all CMOS's V_{IH} in all cases of $V_{DD3.3}$.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

INPUT PARAMETERS FOR GTL+

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	VREF + 0.1			V	$3.14 \leq V_{DD3.3} \leq 3.46$
V_{IL}			VREF - 0.1	V	$3.14 \leq V_{DD3.3} \leq 3.46$
Input leakage current			10	µA	$V_{DD3.3} = 3.46$
Input capacitance		5.5	6.0	pF	

OUTPUT PARAMETERS FOR TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -4.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 4.0 mA
Tristate leakage current	-10		10	µA	
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

et4U.com DataShee

OUTPUT PARAMETERS FOR TTL 8 mA

DataSheet4U.com

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 8.0 mA
Tristate leakage current	-10		10	µA	
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

OUTPUT PARAMETERS FOR OD 8 mA (OPEN DRAIN 8 mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.4	V	$V_{DD3.3}$=3.14; I_{OL}= 8.0 mA
I_{OL}			8.0	mA	

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to $V_{DD3.3}$. If this resistor is not provided the output behaves as tristate.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

INPUT/OUTPUT PARAMETERS FOR LVTTL/TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD3.3} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD3.3} \leq 3.46$
Input leakage current			10	µA	$V_{DD3.3} = 3.46$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD3.3} = 3.14$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD3.3} = 3.14$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

INPUT/OUTPUT PARAMETERS FOR LVTTL/TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD3.3} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD3.3} \leq 3.46$
Input leakage current			10	µA	$V_{DD3.3} = 3.46$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD3.3} = 3.14$; $I_{OH} = -8.0$
V_{OL}			0.4	V	$V_{DD3.3} = 3.14$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

et4U.com
DataShee
DataSheet4U.com
DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

INPUT/OUTPUT PARAMETERS FOR TTL/TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD3.3} \le 3.46$
Input leakage current			10	µA	$V_{DD\ 3.3}$= 3.46
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD3.3}$ = 3.14; I_{OH} = -4.0
V_{OL}			0.4	V	$V_{DD3.3}$ = 3.14; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD3.3} \le 3.46$
Input leakage current			10	µA	$V_{DD3.3}$ = 3.46
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD3.3}$ = 3.14; I_{OH} = -8.0
V_{OL}			0.4	V	$V_{DD3.3}$ = 3.14; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

et4U.com DataSheet4U.com DataShee

INPUT/OUTPUT PARAMETERS FOR GTL+

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	VREF + 0.1			V	$3.14 \le V_{DD3.3} \le 3.46$
V_{IL}			VREF - 0.1	V	$3.14 \le V_{DD3.3} \le 3.46$
Input leakage current			10	µA	$V_{DD3.3}$ = 3.46
Input capacitance		5.5	6.0	pF	
V_{OL}			0.5	V	I_{OL} = 50 mA
Tristate leakage current	-10		10	µA	
I_{OL}		45		mA	50Ω Terminations to 1.5 V
Slew Rate		0.3	0.8	V/ns	25Ω, 30 pF Test Load

DataSheet4U.com www.DataSheet4U.com

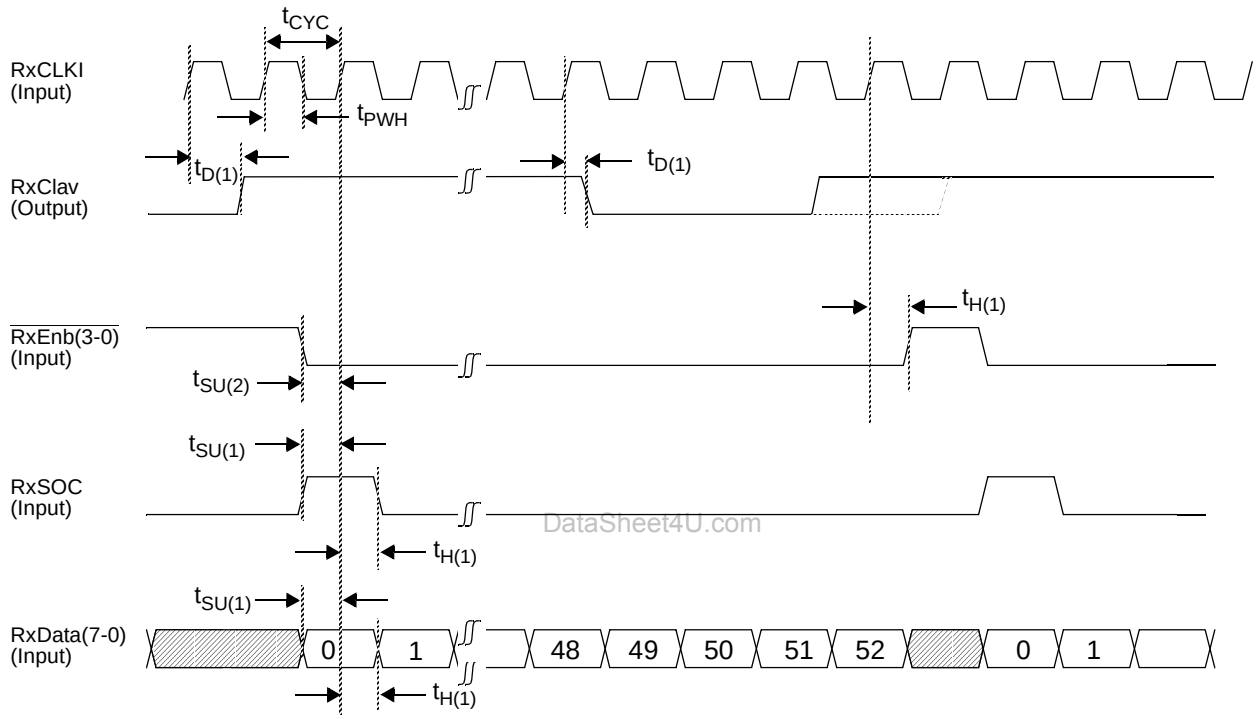
DataSheet4U.com

www.DataSheet4U.com

TIMING CHARACTERISTICS

Detailed timing diagrams for the CUBIT-622 device are provided in Figures 31 through 58, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum 25 pF load capacitance, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ and $(V_{OH}+V_{OL})/2$, for input and output signals, respectively.

Figure 31. Timing of UTOPIA Transmit Single-PHY (PHY Layer Emulation) (8-bit)



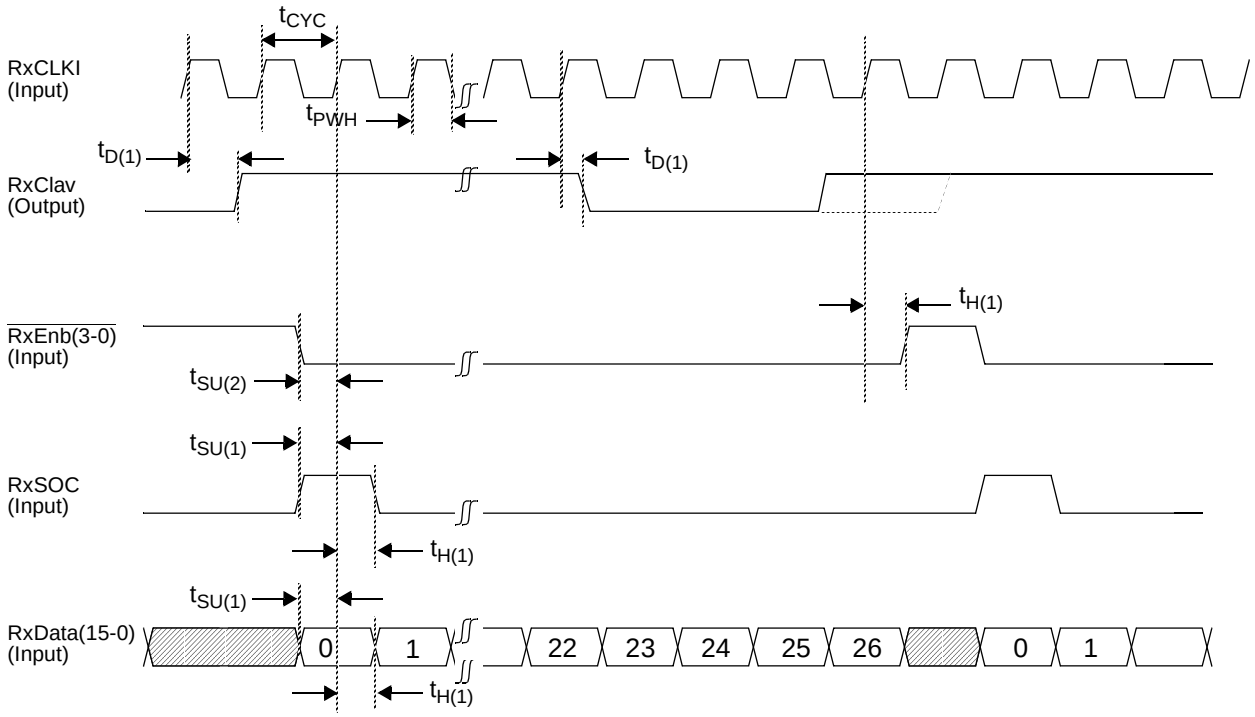
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKI clock cycle time	t_{CYC}	20			ns
RxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(7-0), RxSOC setup time to RxCLKI↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{RxEnb(3-0)}}$ setup time to RxCLKI↑	$t_{SU(2)}$	6.0			ns
RxData(7-0), RxSOC, $\overline{\text{RxEnb(3-0)}}$ hold time after RxCLKI↑	$t_{H(1)}$	1.0			ns
RxClav delay from RxCLKI↑	$t_{D(1)}$	2.0		12	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 32. Timing of UTOPIA Transmit Single-PHY (PHY Layer Emulation) (16-bit)



DataSheet4U.com

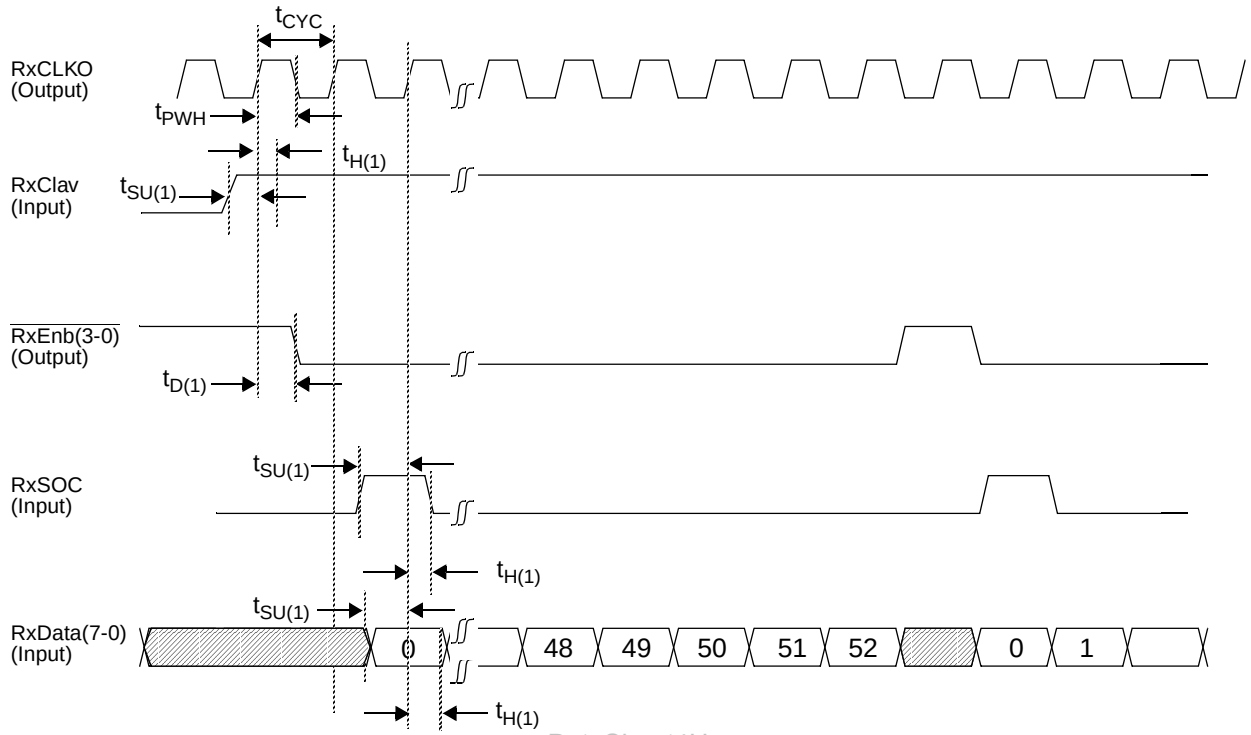
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKI clock cycle time	t_{CYC}	20			ns
RxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(15-0), RxSOC setup time to RxCLKI↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{RxEnb(3-0)}}$ setup time to RxCLKI↑	$t_{SU(2)}$	6.0			ns
RxData(15-0), RxSOC, $\overline{\text{RxEnb(3-0)}}$ hold time after RxCLKI↑	$t_{H(1)}$	1.0			ns
RxClav delay from RxCLKI↑	$t_{D(1)}$	2.0		12	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 33. Timing of UTOPIA Receive Single-PHY (ATM Layer Emulation) (8-bit)



et4U.com
DataShee
DataSheet4U.com

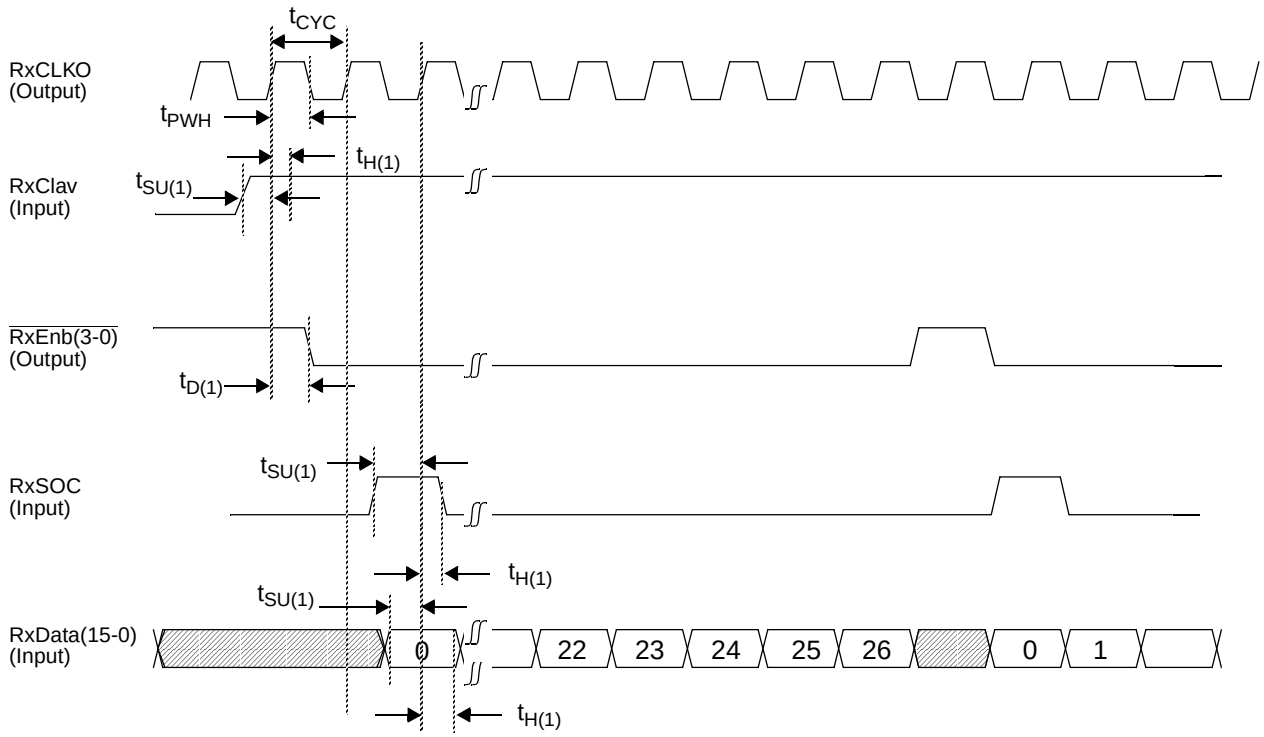
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKO clock cycle time	t_{CYC}	20			ns
RxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(7-0), RxSOC, RxClav setup time to RxCLKO↑	$t_{SU(1)}$	4.0			ns
RxData(7-0), RxSOC, RxClav hold time after RxCLKO↑	$t_{H(1)}$	1.0			ns
$\overline{\text{RxEnb(3-0)}}$ delay from RxCLKO↑	$t_{D(1)}$	2.0		11	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 34. Timing of UTOPIA Receive Single-PHY (ATM Layer Emulation) (16-bit)



DataSheet4U.com

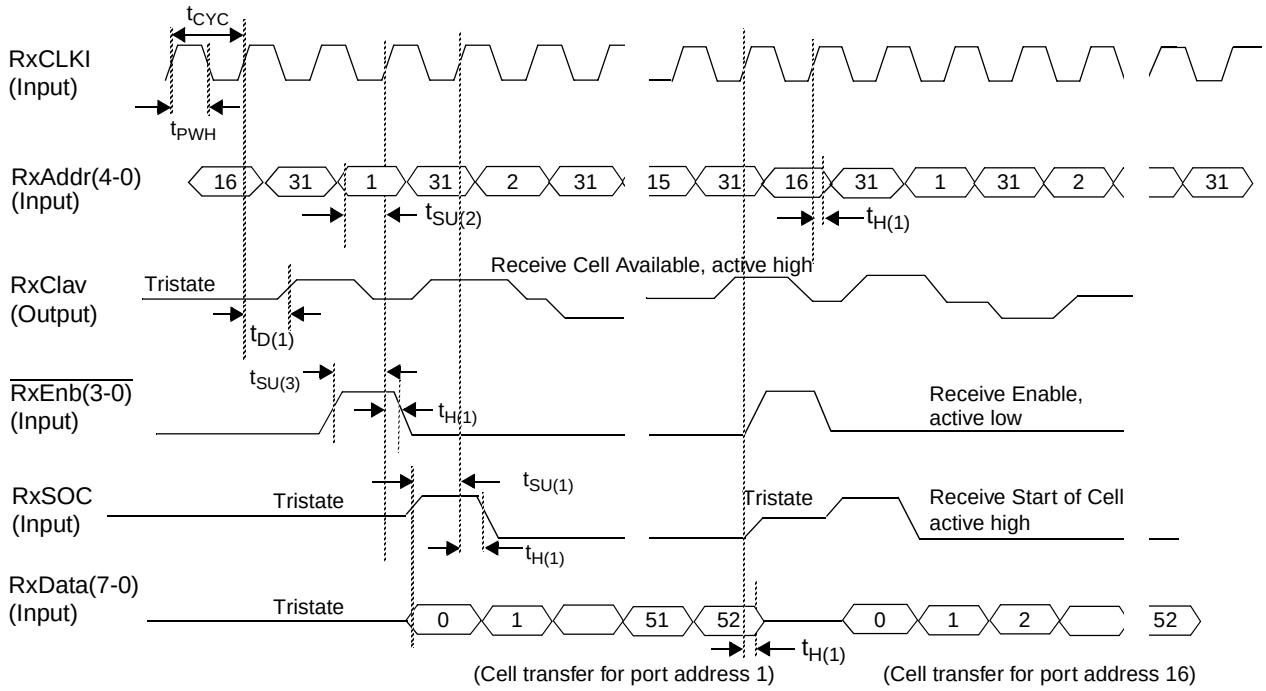
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKO clock cycle time	t_{CYC}	20			ns
RxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(15-0), RxSOC, RxClav setup time to RxCLKO↑	$t_{SU(1)}$	4.0			ns
RxData(15-0), RxSOC, RxClav hold time after RxCLKO↑	$t_{H(1)}$	1.0			ns
$\overline{\text{RxEnb(3-0)}}$ delay from RxCLKO↑	$t_{D(1)}$	2.0		11	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 35. Timing of UTOPIA Transmit Multi-PHY (PHY Layer Emulation) (8-bit)



et4U.com
DataShee
DataSheet4U.com

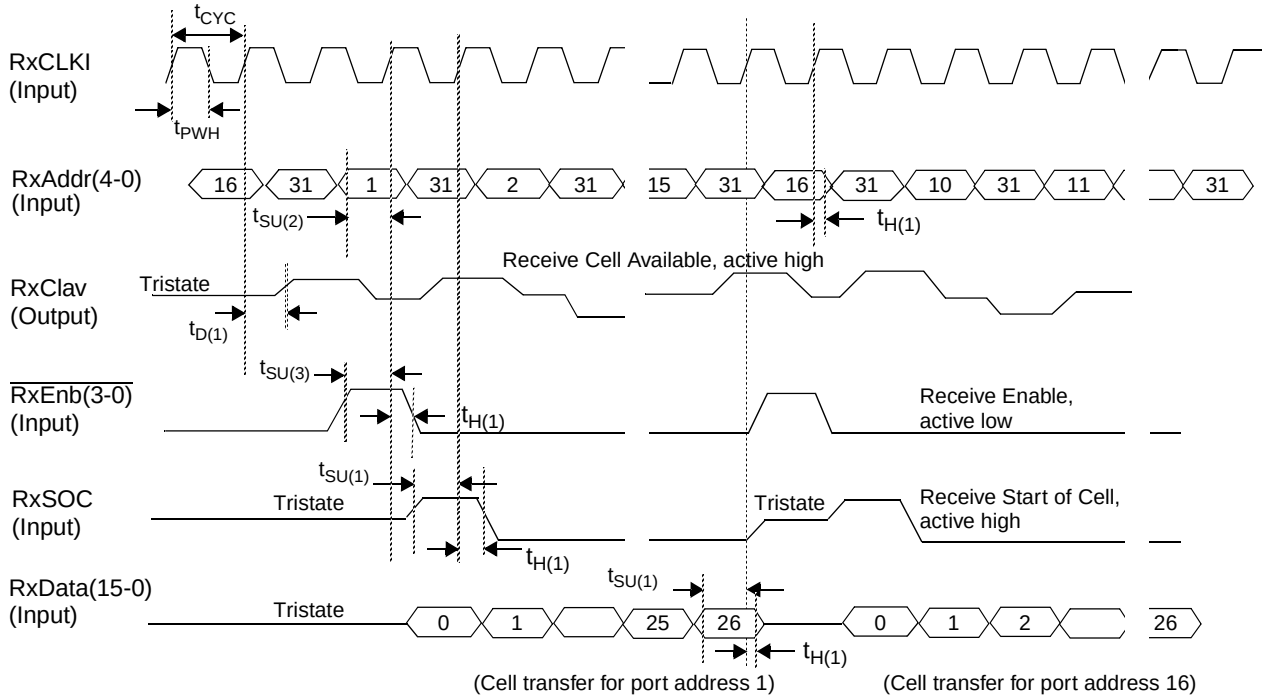
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKI clock cycle time	t_{CYC}	20			ns
RxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(7-0), RxSOC setup time to RxCLKI↑	$t_{SU(1)}$	4.0			ns
RxAddr(4-0) setup time to RxCLKI↑	$t_{SU(2)}$	5.0			ns
$\overline{\text{RxEnb(3-0)}}$ setup time to RxCLKI↑	$t_{SU(3)}$	6.0			ns
RxData(7-0), RxSOC, RxAddr(4-0), $\overline{\text{RxEnb(3-0)}}$ hold time after RxCLKI↑	$t_{H(1)}$	1.0			ns
RxClav delay from RxCLKI↑	$t_{D(1)}$	2.0		12	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 36. Timing of UTOPIA Transmit Multi-PHY (PHY Layer Emulation) (16-bit)



DataSheet4U.com

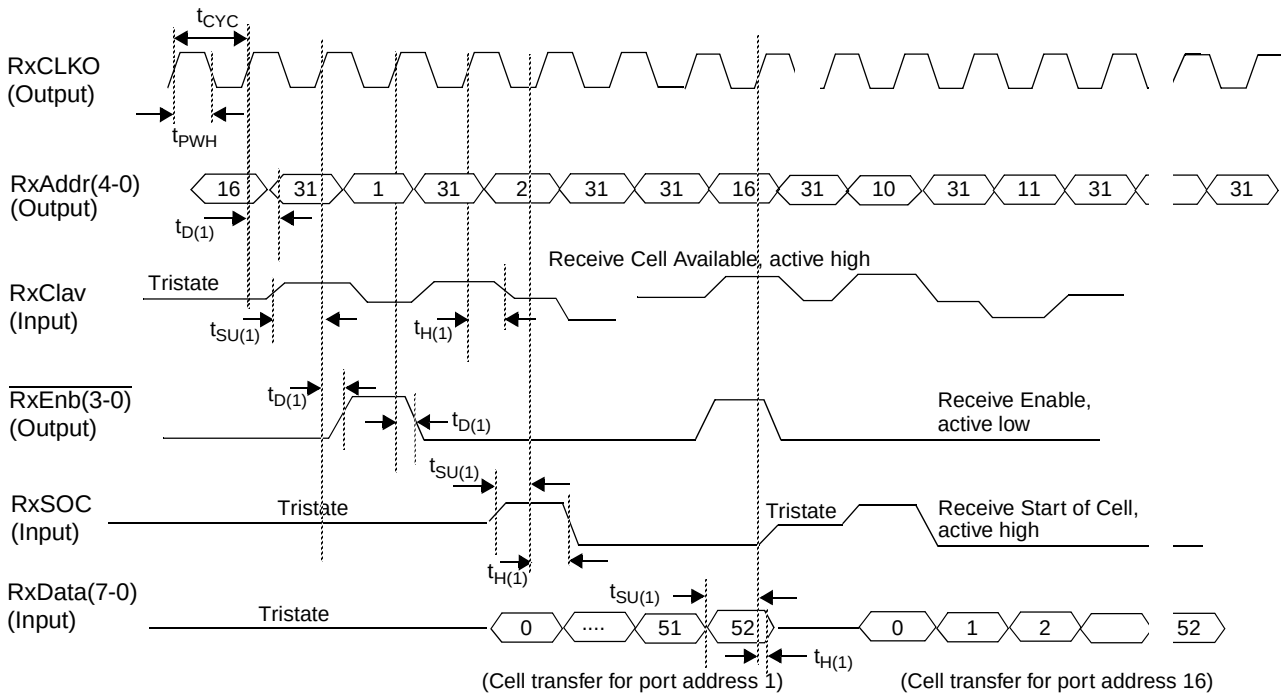
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKI clock cycle time	t_{CYC}	20			ns
RxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(15-0), RxSOC setup time to RxCLKI↑	$t_{SU(1)}$	4.0			ns
RxAddr(4-0) setup time to RxCLKI↑	$t_{SU(2)}$	5.0			ns
$\overline{\text{RxEnb(3-0)}}$ setup time to RxCLKI↑	$t_{SU(3)}$	6.0			ns
RxData(15-0), RxSOC, RxAddr(4-0), $\overline{\text{RxEnb(3-0)}}$ hold time after RxCLKI↑	$t_{H(1)}$	2.0			ns
RxClav delay from RxCLKI↑	$t_{D(1)}$	2.0		12	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 37. Timing of UTOPIA Receive Multi-PHY (ATM Layer Emulation) (8-bit)



DataSheet4U.com

Parameter	Symbol	Min	Typ	Max	Unit
RxCLKO clock cycle time	t_{CYC}	20			ns
RxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(7-0), RxSOC, RxClav setup time to RxCLKO↑	$t_{SU(1)}$	4.0			ns
RxData(7-0), RxSOC, RxClav hold time after RxCLKO↑	$t_{H(1)}$	1.0			ns
RxAddr(4-0), $\overline{\text{RxEnb(3-0)}}$ delay from RxCLKO↑	$t_{D(1)}$	2.0		11	ns

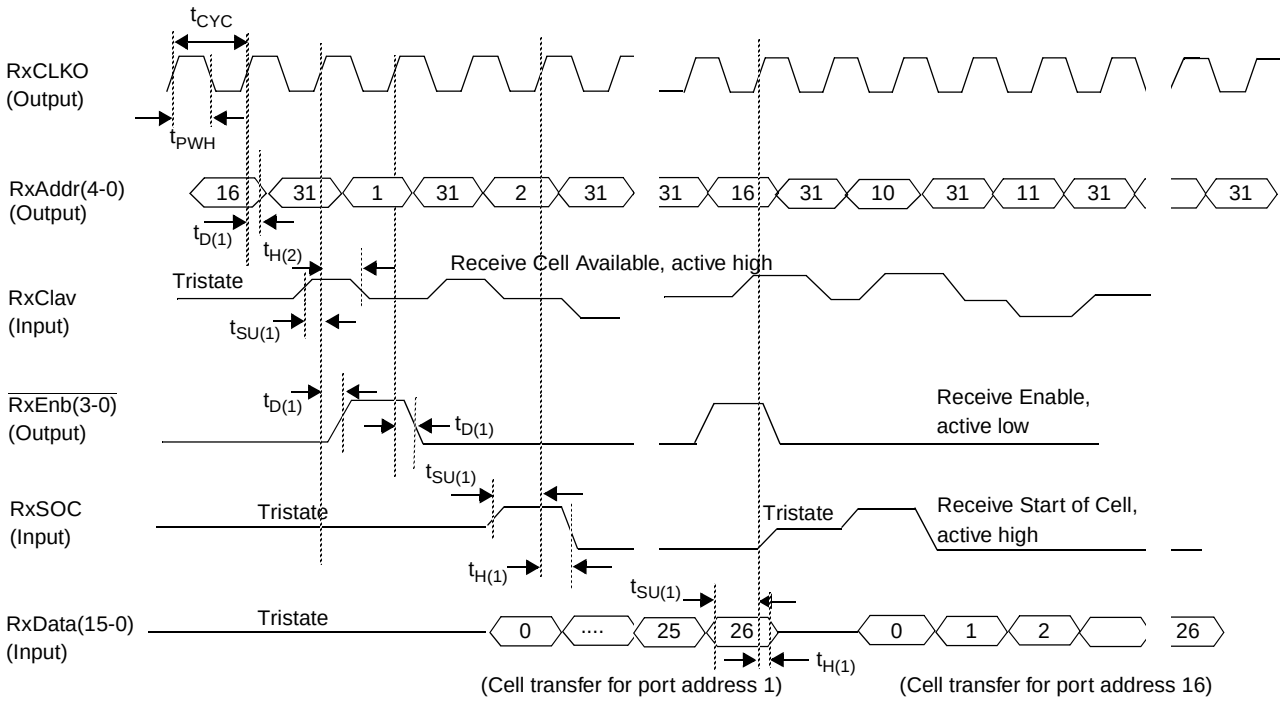
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 38. Timing of UTOPIA Receive Multi-PHY (ATM Layer Emulation) (16-bit)



DataSheet4U.com

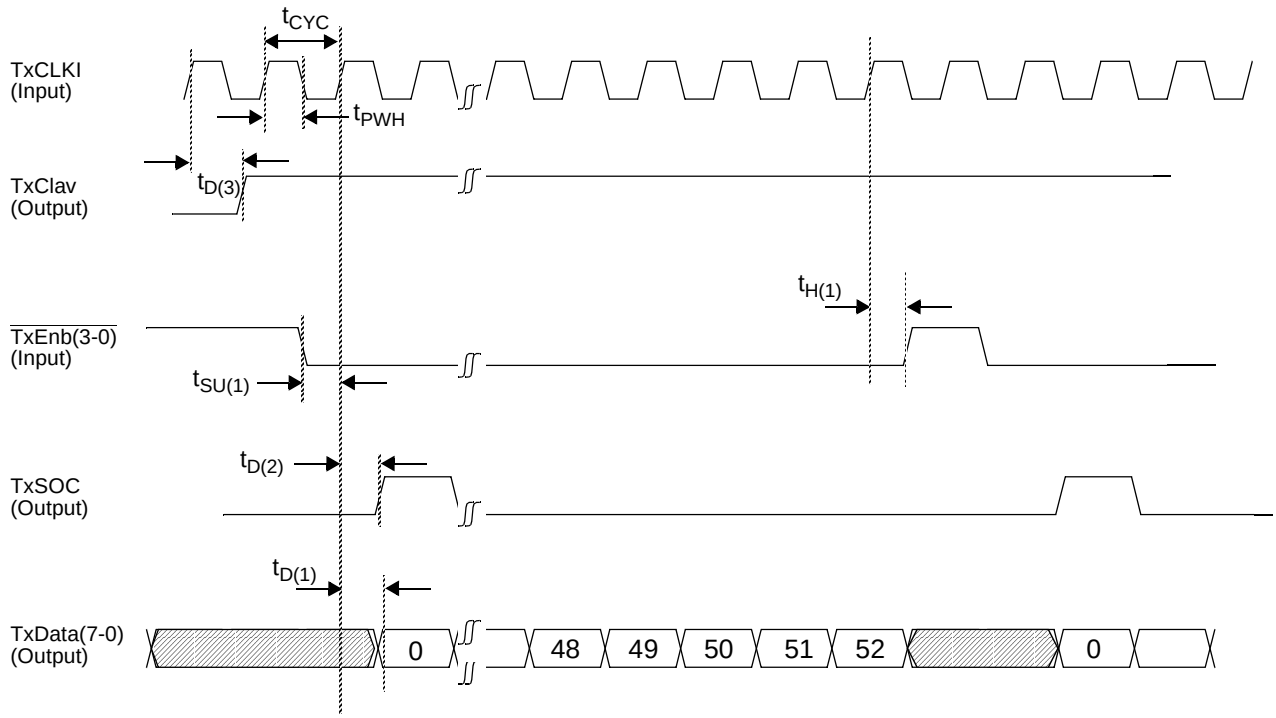
Parameter	Symbol	Min	Typ	Max	Unit
RxCLKO clock cycle time	t_{CYC}	20			ns
RxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
RxData(15-0), RxSOC, RxClav setup time to RxCLKO↑	$t_{SU(1)}$	4.0			ns
RxData(15-0), RxSOC, hold time after RxCLKO↑	$t_{H(1)}$	2.0			ns
RxAddr(4-0), $\overline{\text{RxEnb(3-0)}}$ delay from RxCLKO↑	$t_{D(1)}$	2.0		11	ns
RxClav hold time after RxCLKO↑	$t_{H(2)}$	3.0			ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 39. Timing of UTOPIA Receive Single-PHY (PHY Layer Emulation) (8-bit)



et4U.com
DataShee
DataSheet4U.com

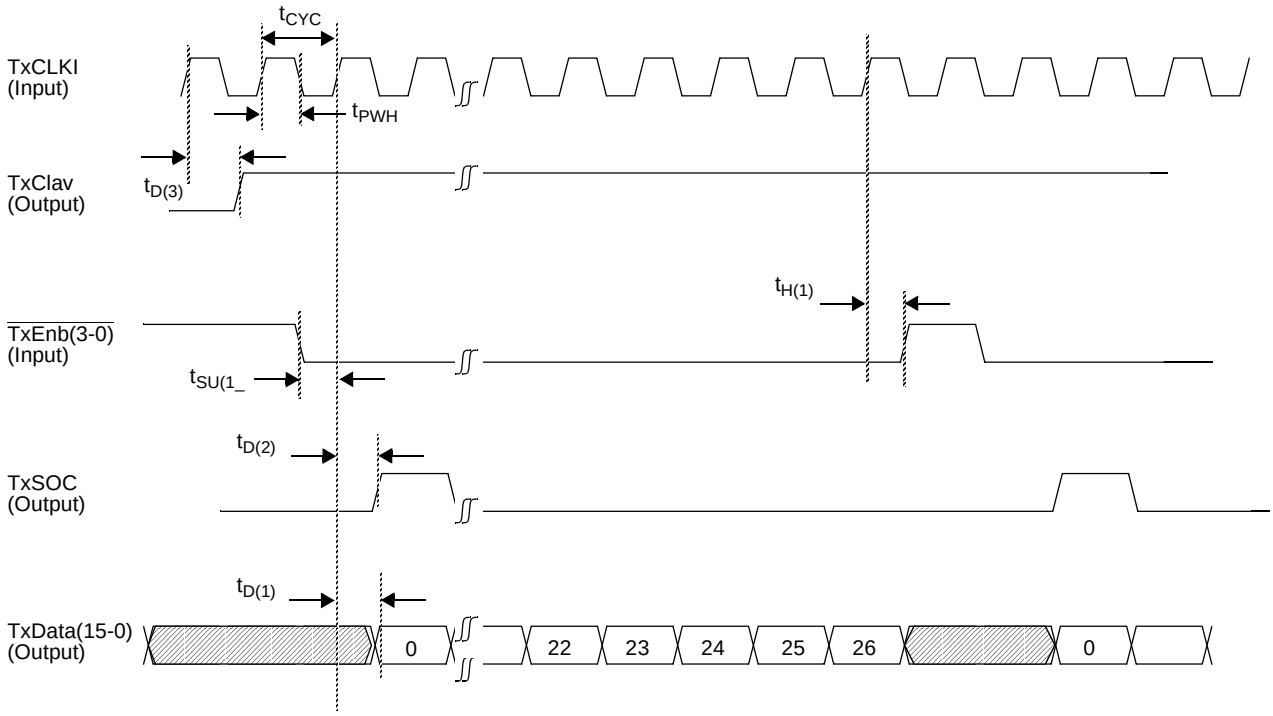
Parameter	Symbol	Min	Typ	Max	Unit
TxCLKI clock cycle time	t_{CYC}	20			ns
TxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{TxEnb(3-0)}}$ setup time to TxCLKI↑	$t_{SU(1)}$	8.0			ns
$\overline{\text{TxEnb(3-0)}}$ hold time after TxCLKI↑	$t_{H(1)}$	1.0			ns
TxData(7-0) delay from TxCLKI↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC delay from TxCLKI↑	$t_{D(2)}$	2.0		11	ns
TxClav delay from TxCLKI↑	$t_{D(3)}$	2.0		12.5	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 40. Timing of UTOPIA Receive Single-PHY (PHY Layer Emulation) (16-bit)



et4U.com
DataShee
DataSheet4U.com

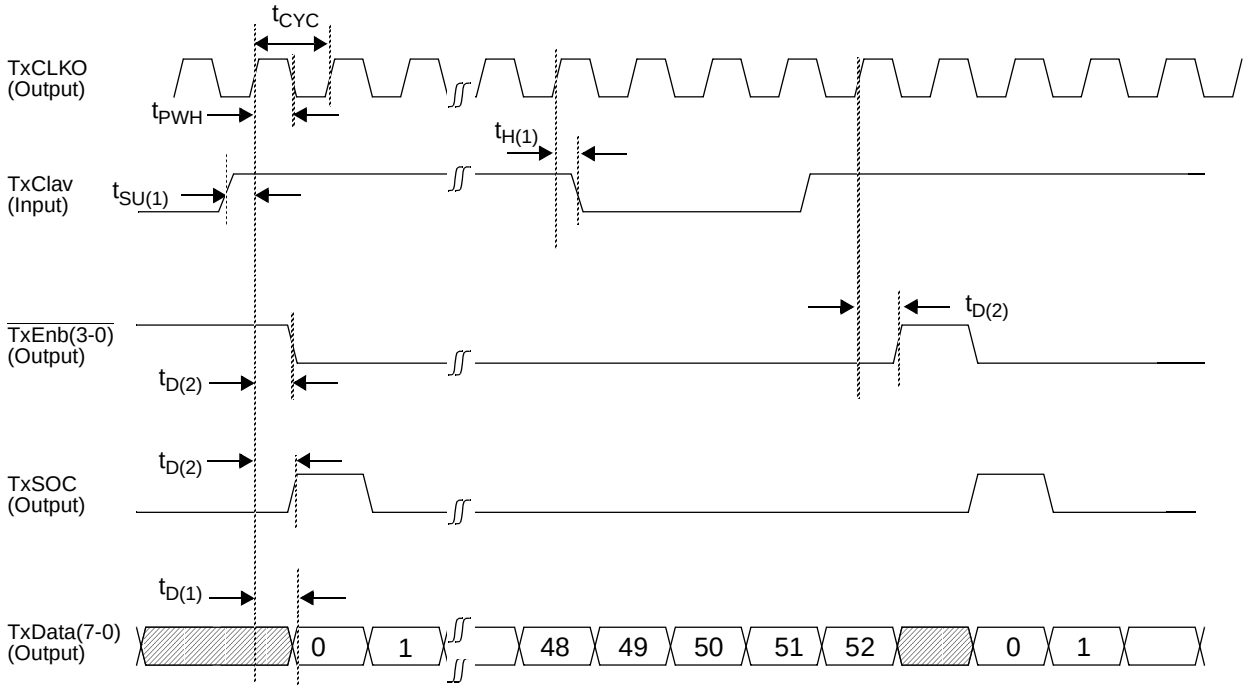
Parameter	Symbol	Min	Typ	Max	Unit
TxCLKI clock cycle time	t_{CYC}	20			ns
TxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{TxEnb(3-0)}}$ setup time to TxCLKI↑	$t_{SU(1)}$	8.0			ns
$\overline{\text{TxEnb(3-0)}}$ hold time after TxCLKI↑	$t_{H(1)}$	1.0			ns
TxData(15-0) delay from TxCLKI↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC delay from TxCLKI↑	$t_{D(2)}$	2.0		11	ns
TxClav delay from TxCLKI↑	$t_{D(3)}$	2.0		12.5	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 41. Timing of UTOPIA Transmit Single-PHY (ATM Layer Emulation) (8-bit)



DataSheet4U.com

Parameter	Symbol	Min	Typ	Max	Unit
TxCLKO clock cycle time	t_{CYC}	20			ns
TxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxClav setup time to TxCLKO↑	$t_{SU(1)}$	7.5			ns
TxClav hold time after TxCLKO↑	$t_{H(1)}$	1.0			ns
TxData(7-0) delay from TxCLKO↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC, $\overline{\text{TxEnb(3-0)}}$ delay from TxCLKO↑	$t_{D(2)}$	2.0		11	ns

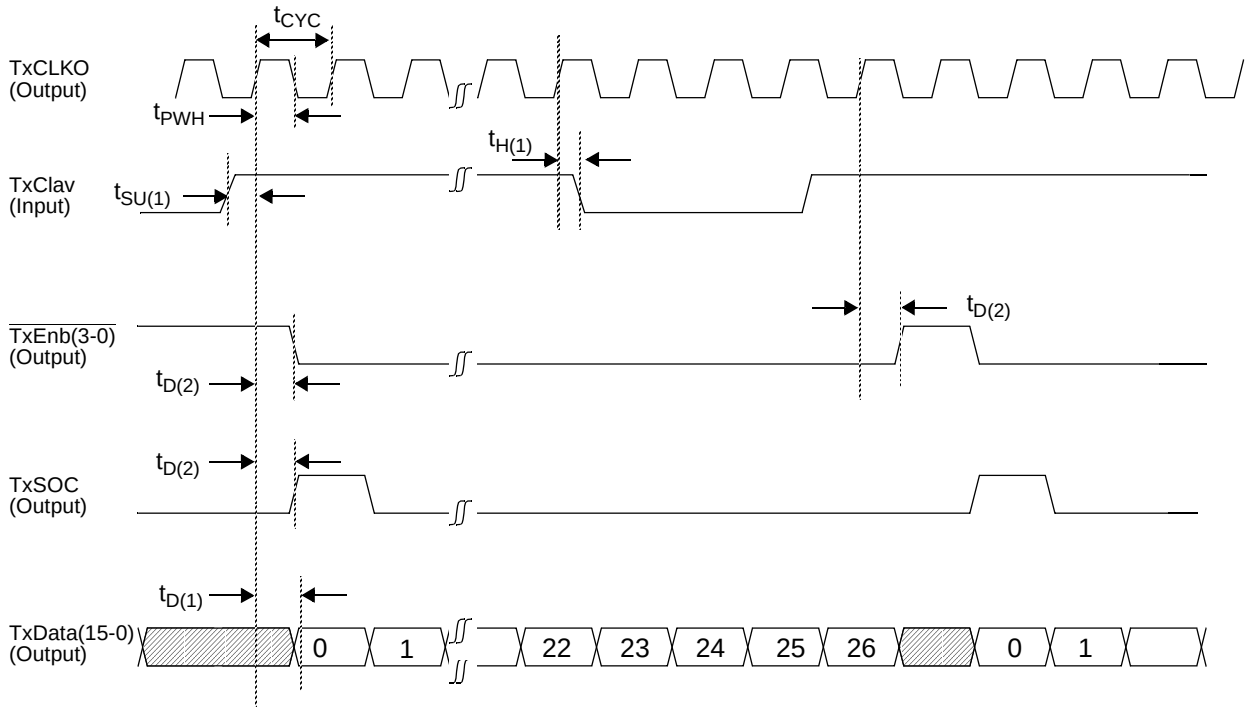
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 42. Timing of UTOPIA Transmit Single-PHY (ATM Layer Emulation) (16-bit)



et4U.com
DataShee
DataSheet4U.com

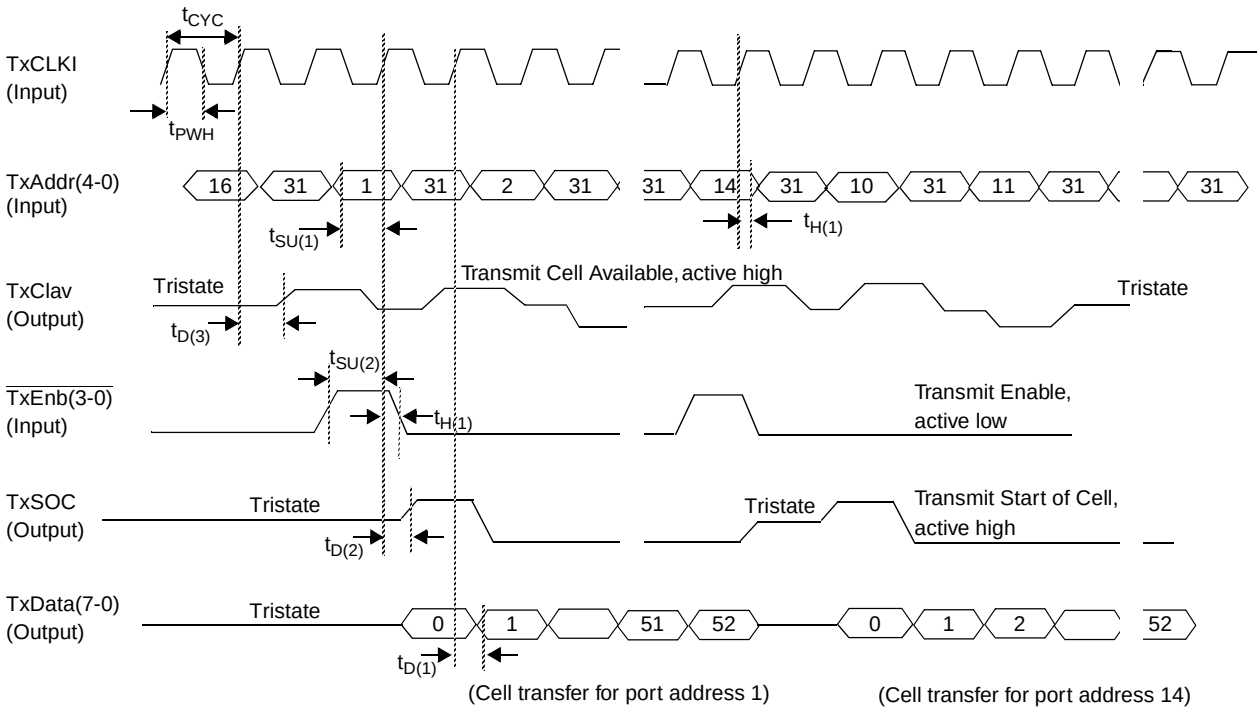
Parameter	Symbol	Min	Typ	Max	Unit
TxCLKO clock cycle time	t_{CYC}	20			ns
TxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxClav setup time to TxCLKO↑	$t_{SU(1)}$	7.5			ns
TxClav hold time after TxCLKO↑	$t_{H(1)}$	1.0			ns
TxData(15-0) delay from TxCLKO↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC, $\overline{\text{TxEnb(3-0)}}$ delay from TxCLKO↑	$t_{D(2)}$	2.0		11	ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 43. Timing of UTOPIA Receive Multi-PHY (PHY Layer Emulation) (8-bit)



DataSheet4U.com

Parameter	Symbol	Min	Typ	Max	Unit
TxCLKI clock cycle time	t_{CYC}	20			ns
TxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxAddr(4-0) setup time to TxCLKI↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{TxEnb(3-0)}}$ setup time to TxCLKI↑	$t_{SU(2)}$	8.0			ns
$\overline{\text{TxEnb(3-0)}}$, TxAddr(4-0) hold time after TxCLKI↑	$t_{H(1)}$	1.0			ns
TxData(7-0) delay from TxCLKI↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC delay from TxCLKI↑	$t_{D(2)}$	2.0		11	ns
TxClav delay from TxCLKI↑	$t_{D(3)}$	2.0		12.5	ns

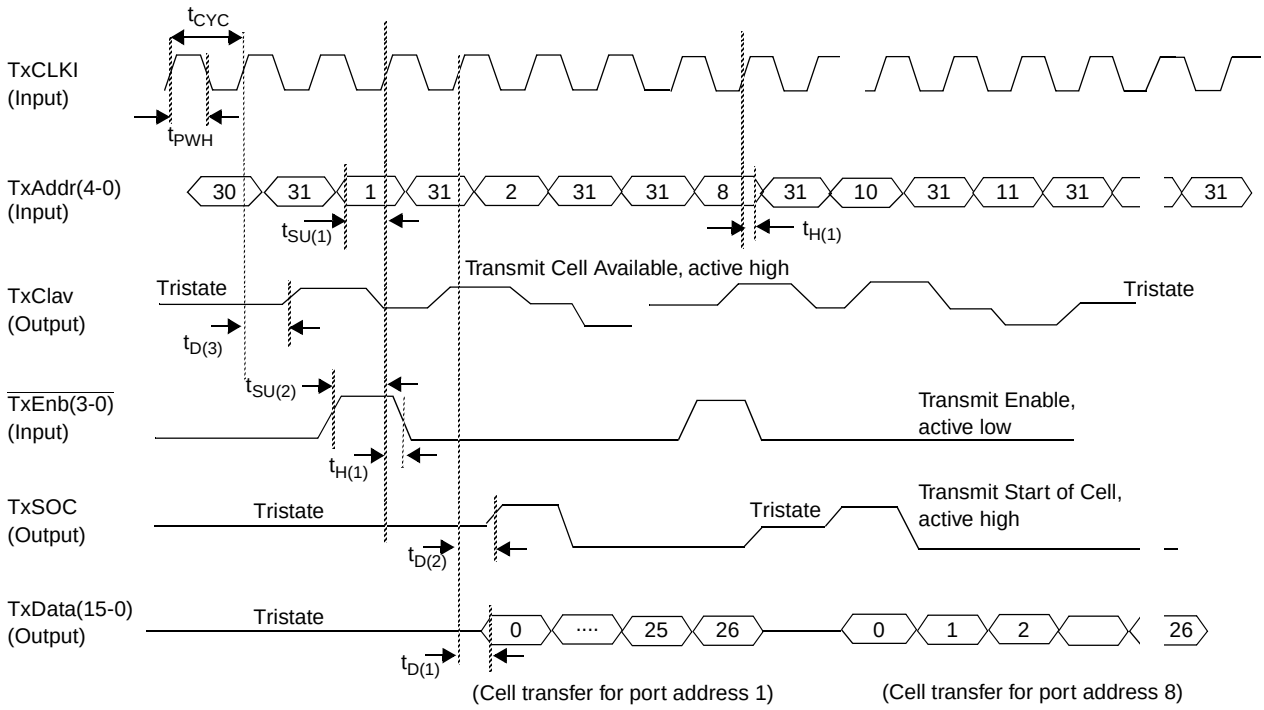
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 44. Timing of UTOPIA Receive Multi-PHY (PHY Layer Emulation) (16-bit)



DataSheet4U.com

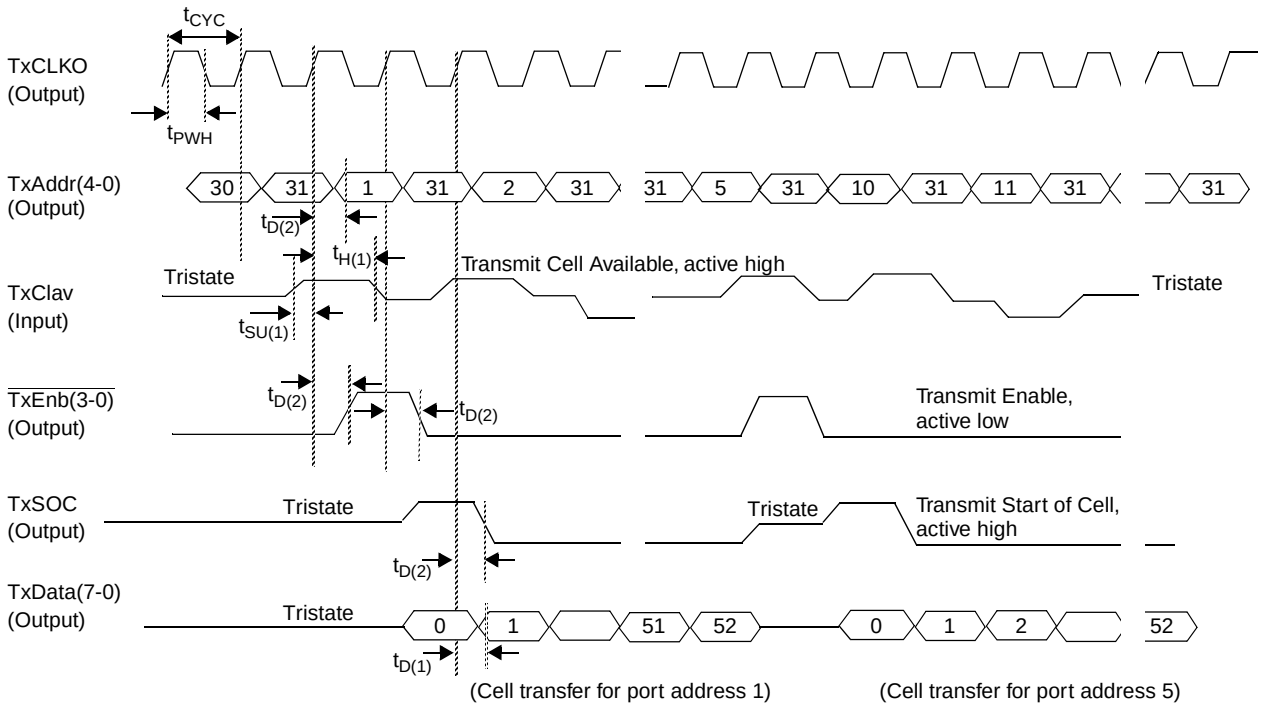
Parameter	Symbol	Min	Typ	Max	Unit
TxCLKI clock cycle time	t_{CYC}	20			ns
TxCLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxAddr(4-0) setup time to TxCLKI↑	$t_{SU(1)}$	4.0			ns
$\overline{\text{TxEnb(3-0)}}$ setup time to TxCLKI↑	$t_{SU(2)}$	8.0			ns
$\overline{\text{TxEnb(3-0)}}$, TxAddr(4-0) hold time after TxCLKI↑	$t_{H(1)}$	2.0			ns
TxData(15-0) delay from TxCLKI↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC delay from TxCLKI↑	$t_{D(2)}$	2.0		11	ns
TxClav delay from TxCLKI↑	$t_{D(3)}$	2.0		12.5	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 45. Timing of UTOPIA Transmit Multi-PHY (ATM Layer Emulation) (8-bit)



DataSheet4U.com

Parameter	Symbol	Min	Typ	Max	Unit
TxCLKO clock cycle time	t_{CYC}	20			ns
TxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxClav setup time to TxCLKO↑	$t_{SU(1)}$	7.5			ns
TxClav hold time after TxCLKO↑	$t_{H(1)}$	1.0			ns
TxData(7-0) delay from TxCLKO↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC, TxAddr(4-0), $\overline{\text{TxEnb(3-0)}}$ delay from TxCLKO↑	$t_{D(2)}$	2.0		11	ns

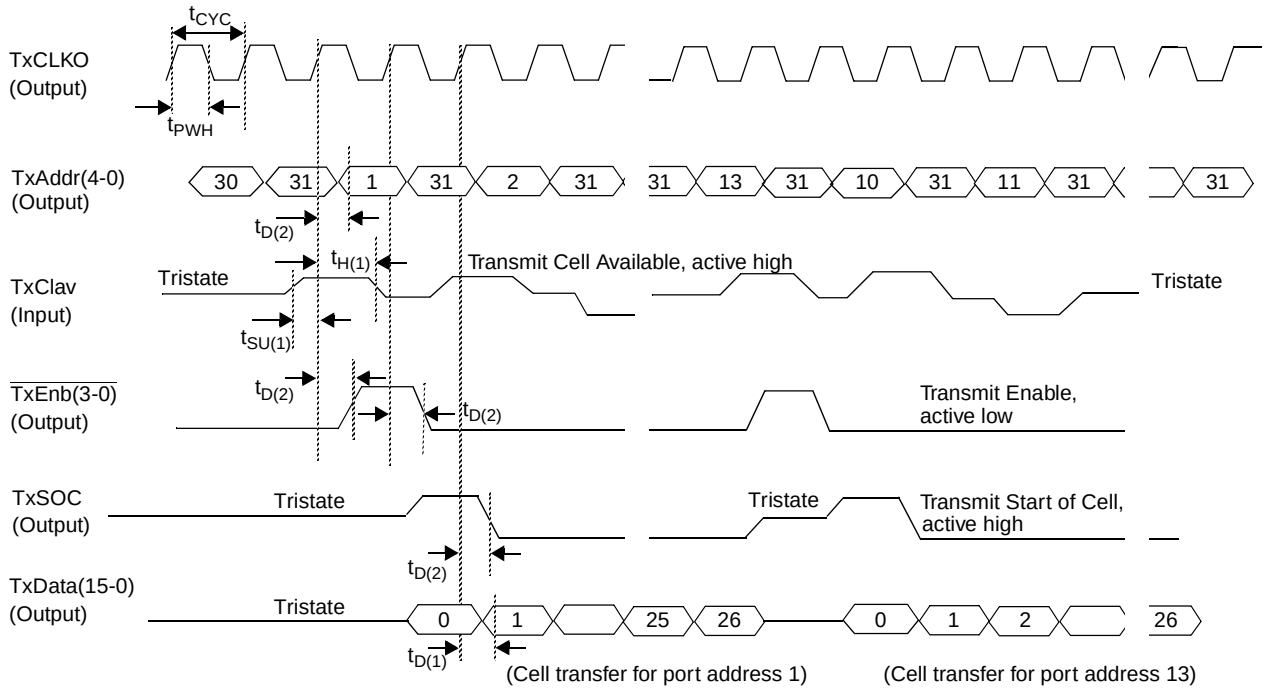
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 46. Timing of UTOPIA Transmit Multi-PHY (ATM Layer Emulation) (16-bit)



DataSheet4U.com

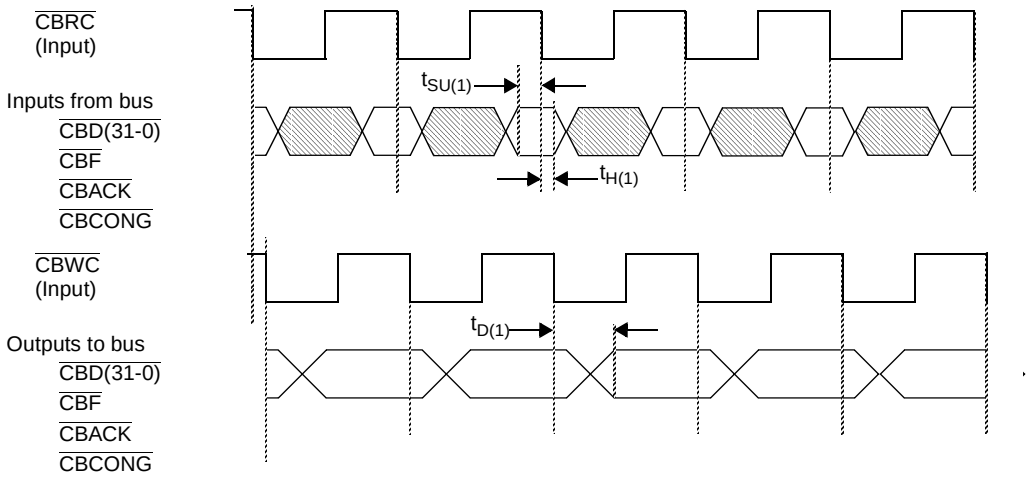
Parameter	Symbol	Min	Typ	Max	Unit
TxCLKO clock cycle time	t_{CYC}	20			ns
TxCLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
TxClav setup time to TxCLKO↑	$t_{SU(1)}$	7.5			ns
TxClav hold time after TxCLKO↑	$t_{H(1)}$	2.0			ns
TxData(15-0) delay from TxCLKO↑	$t_{D(1)}$	2.0		11.5	ns
TxSOC, TxAddr(4-0), $\overline{\text{TxEnb(3-0)}}$ delay from TxCLKO↑	$t_{D(2)}$	2.0		11	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 47. Timing of *CellBus* Interface



Parameter	Symbol	Min	Typ	Max	Unit
CellBus inputs setup time before $\overline{\text{CBRC}}\downarrow$	$t_{SU(1)}$	2.5			ns
CellBus inputs hold time after $\overline{\text{CBRC}}\downarrow$	$t_{H(1)}$	3.5			ns
CellBus outputs delay after $\overline{\text{CBWC}}\downarrow$	$t_{D(1)}$	5.0			ns

Notes:

The CUBIT-622 *CellBus* write clock to *CellBus* data out time delay $t_{D(1)}$ has two components, internal delay and GTL+ driver delay. The internal delay consists of the delay from the $\overline{\text{CBWC}}$ input, through the GTL+ receiver, internal CUBIT-622 circuitry and into the (internal) input lead of the GTL+ driver. This internal delay is dependent solely on temperature and process variation. The minimum and maximum values are 2.0 ns and 10 ns, respectively. The GTL+ driver delay includes the effects of the (internal) GTL+ driver and all external loading, from the device bond wire inductance onwards. For the purposes of specification, a test load is used which consists of a 13 nH bond wire inductance from the VLSI device output pad to the package output lead, and a 50 ohm resistor to +1.5 volts with a 1.0 pF capacitor to ground from the package output lead. The total value of $t_{D(1)}$ is increased to 5.0 ns minimum and 13 ns maximum when using this load.

These output delay values by themselves may be inadequate to complete a system design. TranSwitch strongly recommends that all *CellBus* applications should be analyzed by high speed backplane and simulation specialists, using such tools as HSpice® analog circuit simulation.

These simulations can model timing from one CUBIT-622, through various levels of system interconnect, to another CUBIT-622, and include the effects of the device package, printed circuit board, connectors and backplane. The results of these simulations, when added to the internal delay, will provide the actual value of $t_{D(1)}$ for a given system. TranSwitch is able to support simulations by providing up-to-date models of the GTL+ transceiver used within the CUBIT-622.

Please contact the TranSwitch Applications Engineering Department for additional information, a list of proven high speed simulation consultants and other technical support.

Note: HSpice is a registered trademark of Meta-Software, Inc.

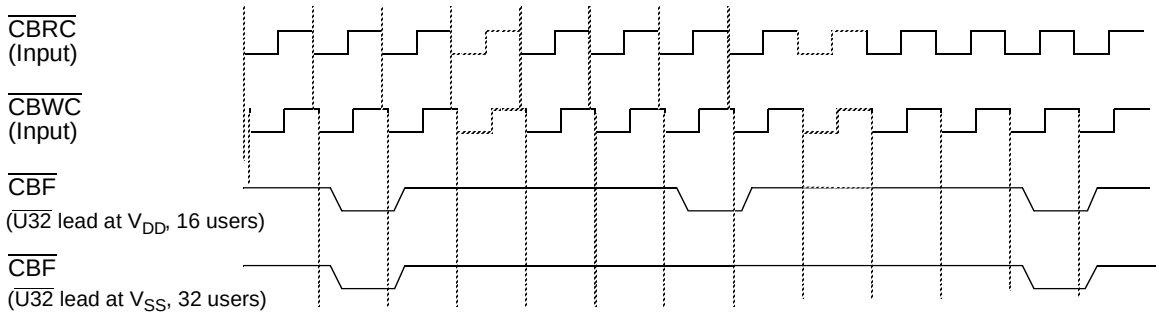
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 48. Timing of *CellBus* Frame Position

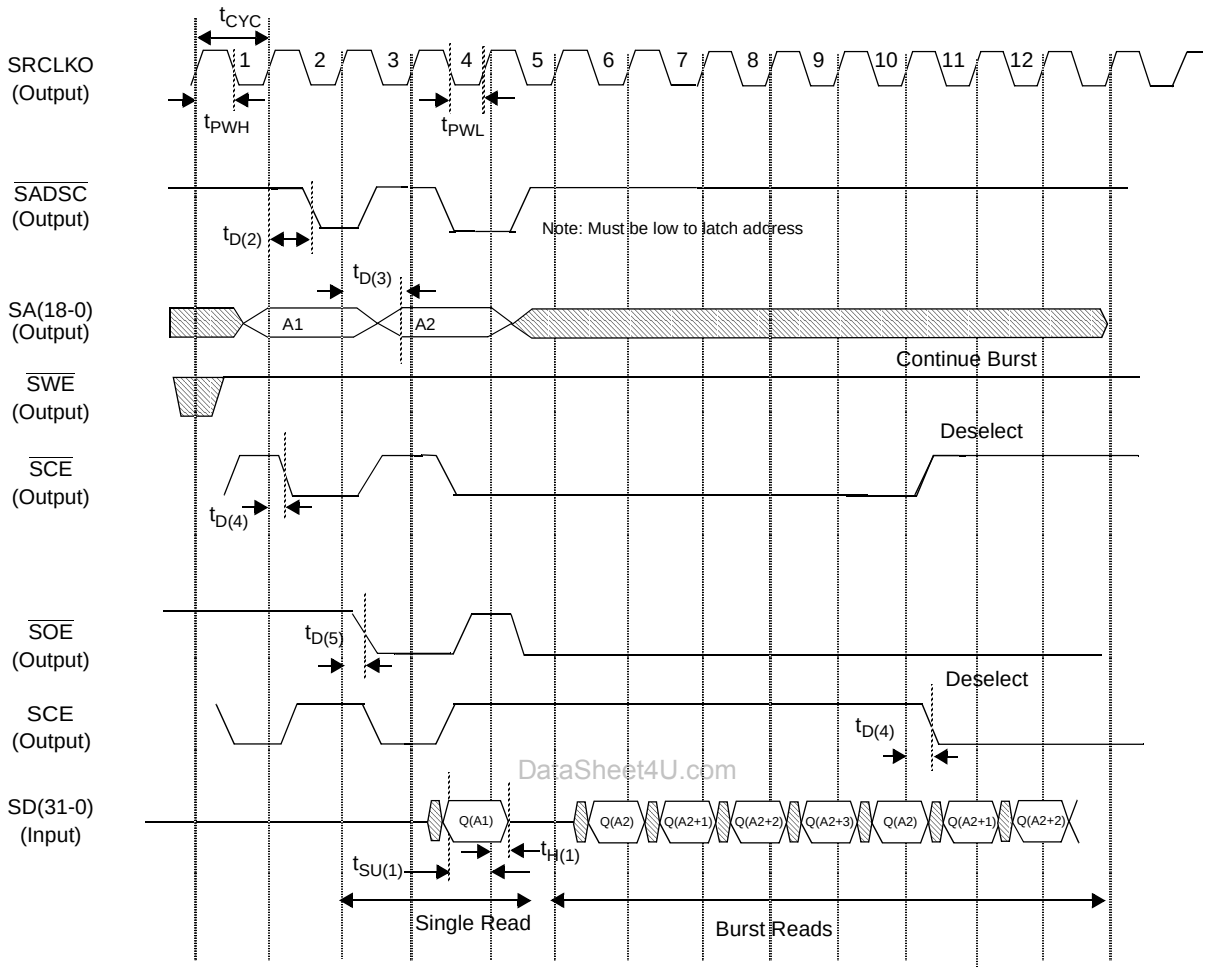


et4U.com
DataShee
DataSheet4U.com
DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 49. Timing of SSRAM Read Cycle



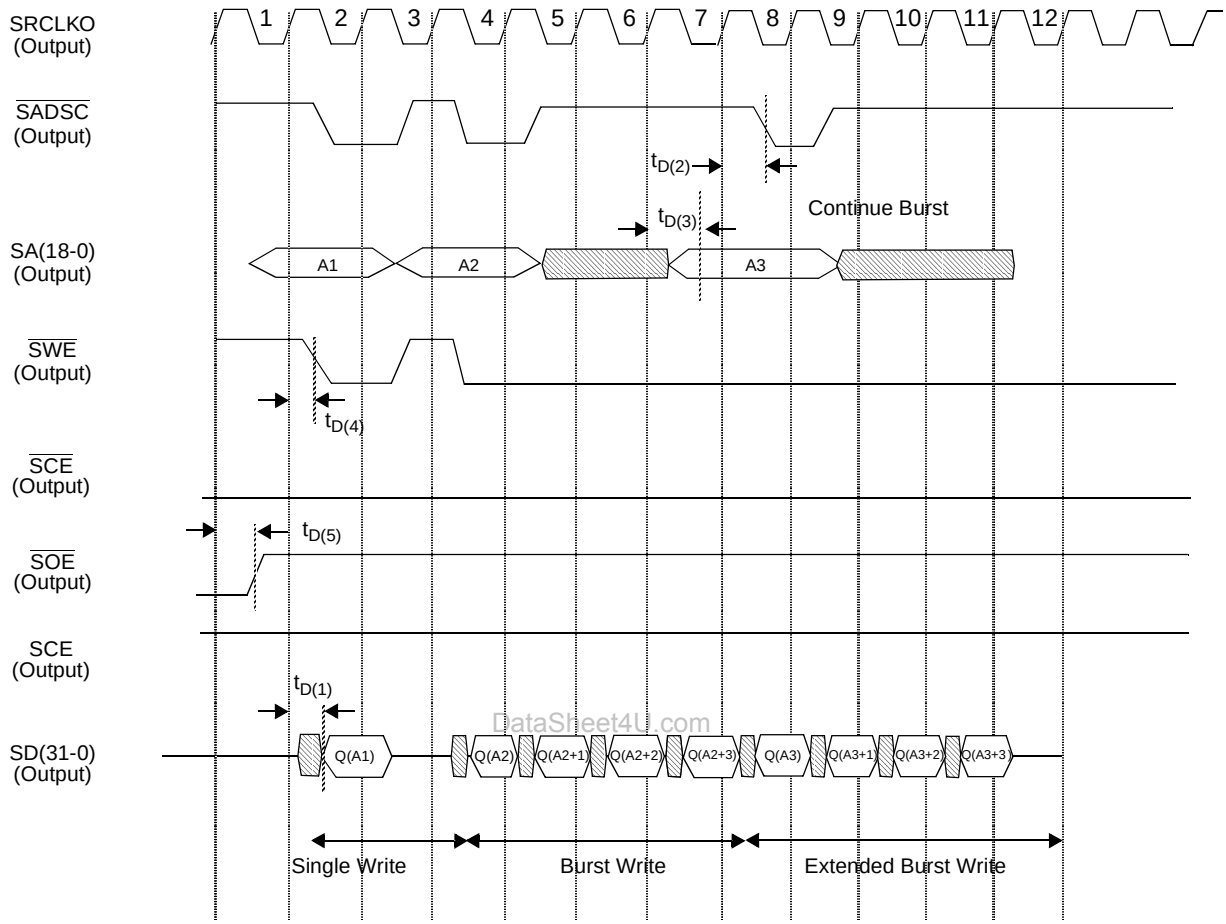
Parameter	Symbol	Min	Typ	Max	Unit
SRCLKO cycle time	t_{CYC}	10			ns
SRCLKO duty cycle, t_{PWH} / t_{CYC}	-	40		60	%
$\overline{SADSC}$ delay from SRCLKO↑	$t_{D(2)}$	1.0		3.4	ns
SA(18-0) delay from SRCLKO↑	$t_{D(3)}$	1.0		4.9	ns
SCE, $\overline{SCE}$ delay from SRCLKO↑	$t_{D(4)}$	1.0		3.7	ns
SD(31-0) setup time before SRCLKO↑	$t_{SU(1)}$	3.9			ns
SD(31-0) hold time after SRCLKO↑	$t_{H(1)}$	0.0			ns
$\overline{SOE}$ delay from SRCLKO↑	$t_{D(5)}$	1.0			ns

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 50. Timing of SSRAM Write Cycle



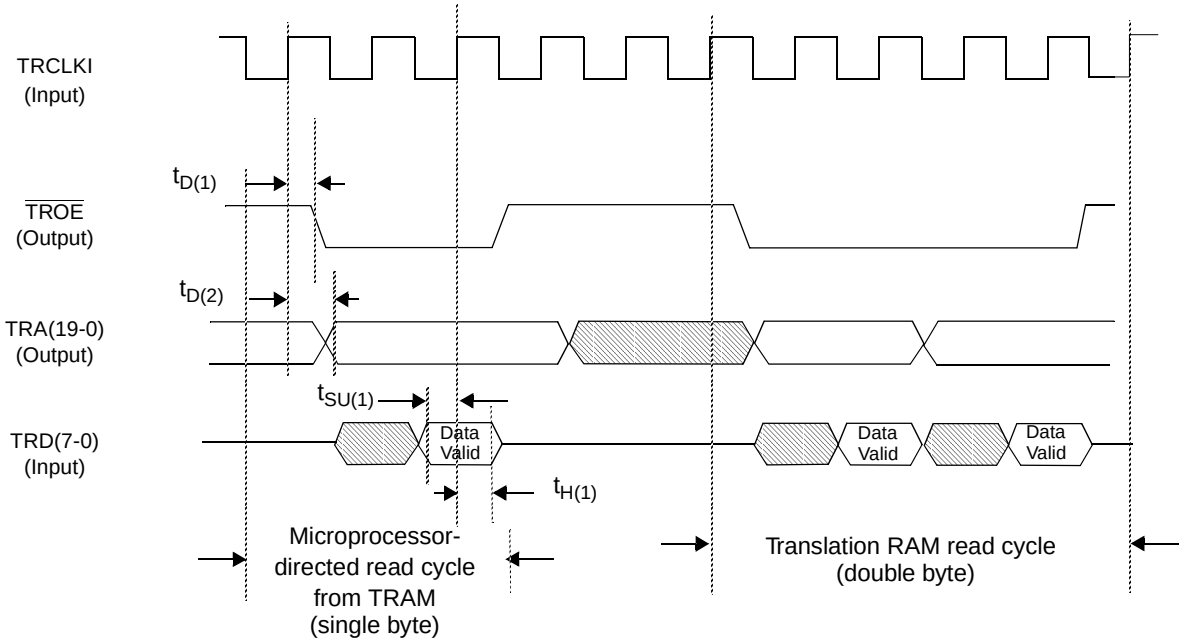
Parameter	Symbol	Min	Typ	Max	Unit
SD(31-0) delay from SRCLKO↑	$t_{D(1)}$			6.8	ns
$\overline{SADSC}$ delay from SRCLKO↑	$t_{D(2)}$	1.0		3.4	ns
SA(18-0) delay from SRCLKO↑	$t_{D(3)}$	1.0		4.9	ns
$\overline{SWE}$ delay from SRCLKO↑	$t_{D(4)}$	1.0		4.0	ns
$\overline{SOE}$ delay from SRCLKO↑	$t_{D(5)}$	1.0		3.9	ns

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 51. Translation RAM Timing - Read from TRAM



et4U.com DataShee

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{TROE}}$ output delay after TRCLKI↑	$t_{D(1)}$	2.9		7.6	ns
TRA(19-0) output delay after TRCLKI↑	$t_{D(2)}$	2.8		8.7	ns
TRD(7-0) setup time before TRCLKI↑	$t_{SU(1)}$	4.0			ns
TRD(7-0) hold time after TRCLKI↑	$t_{H(1)}$	2.0			ns

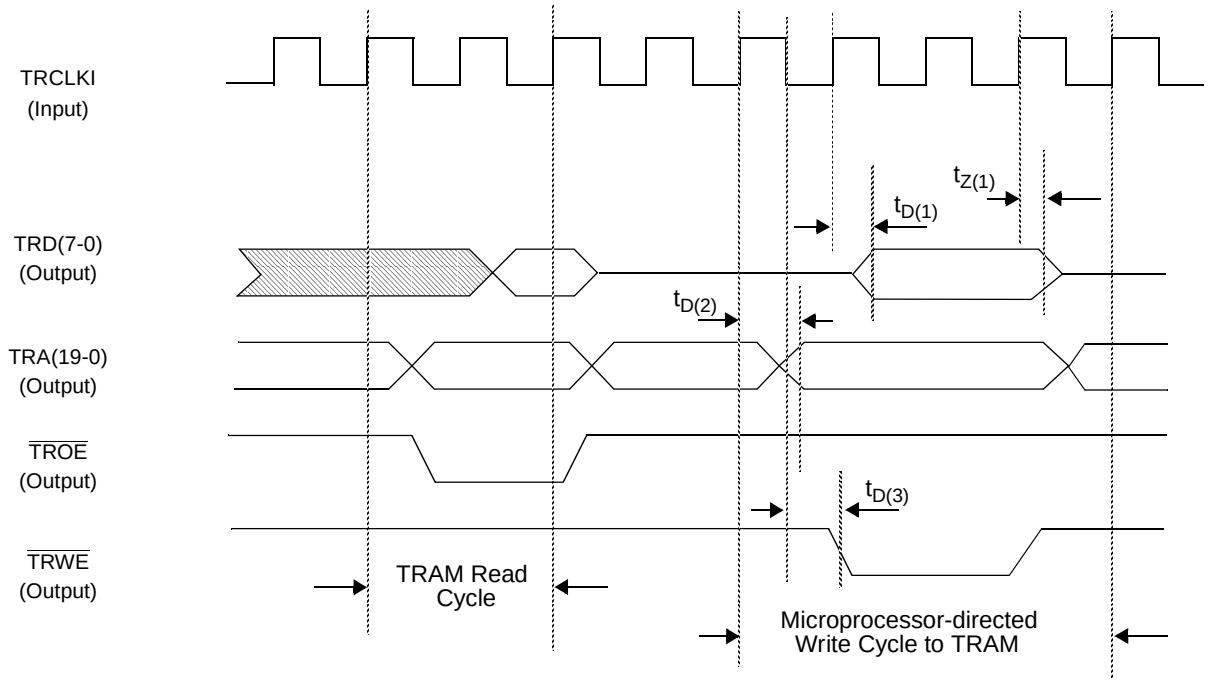
Note: $\overline{\text{TRWE}}$ output is high. All timing parameter values apply to both Microprocessor and Translation RAM read cycles.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 52. Translation RAM Timing - Write to TRAM



et4U.com DataShee
DataSheet4U.com

Parameter	Symbol	Min	Typ	Max	Unit
TRD(7-0) delay from tristate after TRCLKI↑	$t_{D(1)}$	3.0		9.6	ns
TRD(7-0) delay to tristate after TRCLKI↑	$t_{Z(1)}$	3.0		11.2	ns
TRA(19-0) delay after TRCLKI↑	$t_{D(2)}$	2.8		8.7	ns
$\overline{\text{TRWE}}$ delay after TRCLKI↓	$t_{D(3)}$	3.0		8.4	ns

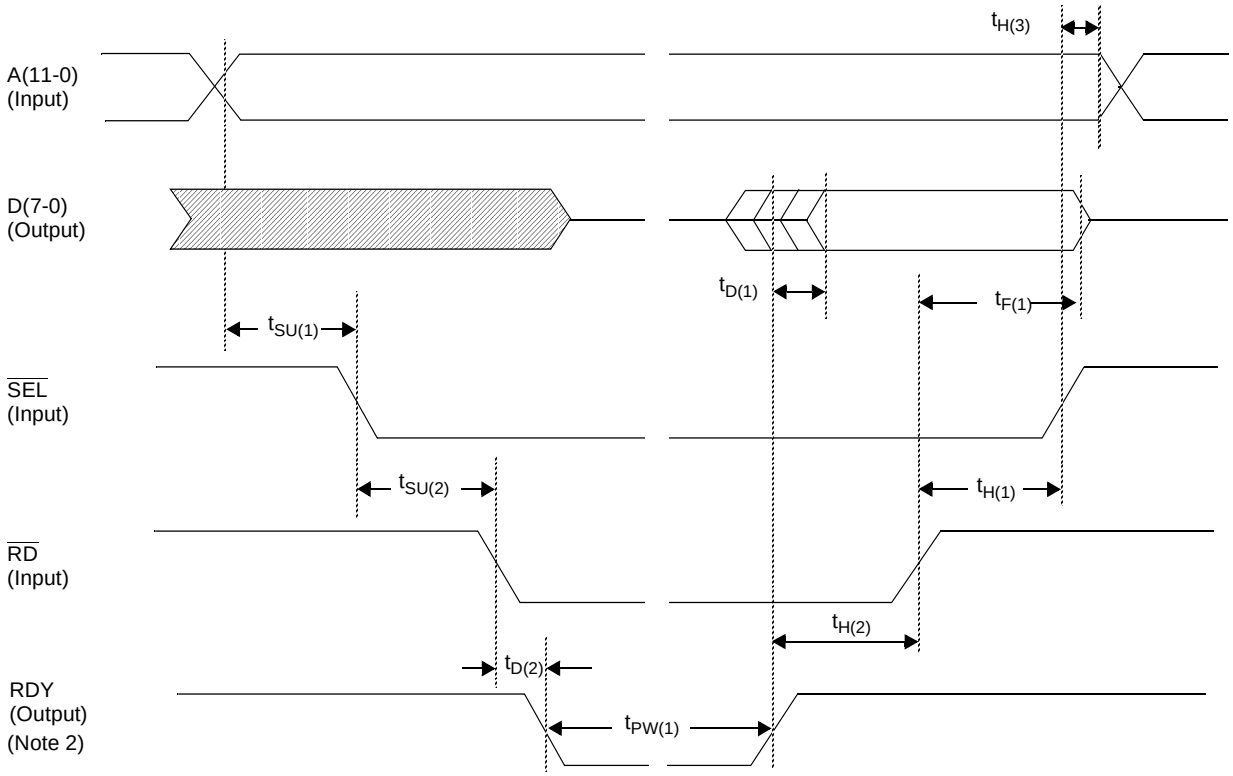
DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MICROPROCESSOR INTERFACE TIMING

Figure 53. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(11-0) valid setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
A(11-0) valid hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			
D(7-0) valid delay after RDY$\uparrow$	$t_{D(1)}$	-10		0.0	ns
D(7-0) float time to tristate after $\overline{RD}\uparrow$	$t_{F(1)}$	2.0		10.5	ns
$\overline{SEL}$ setup time to $\overline{RD}\downarrow$	$t_{SU(2)}$	1.0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	1.5			ns
$\overline{RD}$ hold time after RDY$\uparrow$	$t_{H(2)}$	0.0			ns
RDY delay after $\overline{RD}\downarrow$	$t_{D(2)}$	0.0		12	ns
RDY pulse width	$t_{PW(1)}$	0.0		Note 1	ns

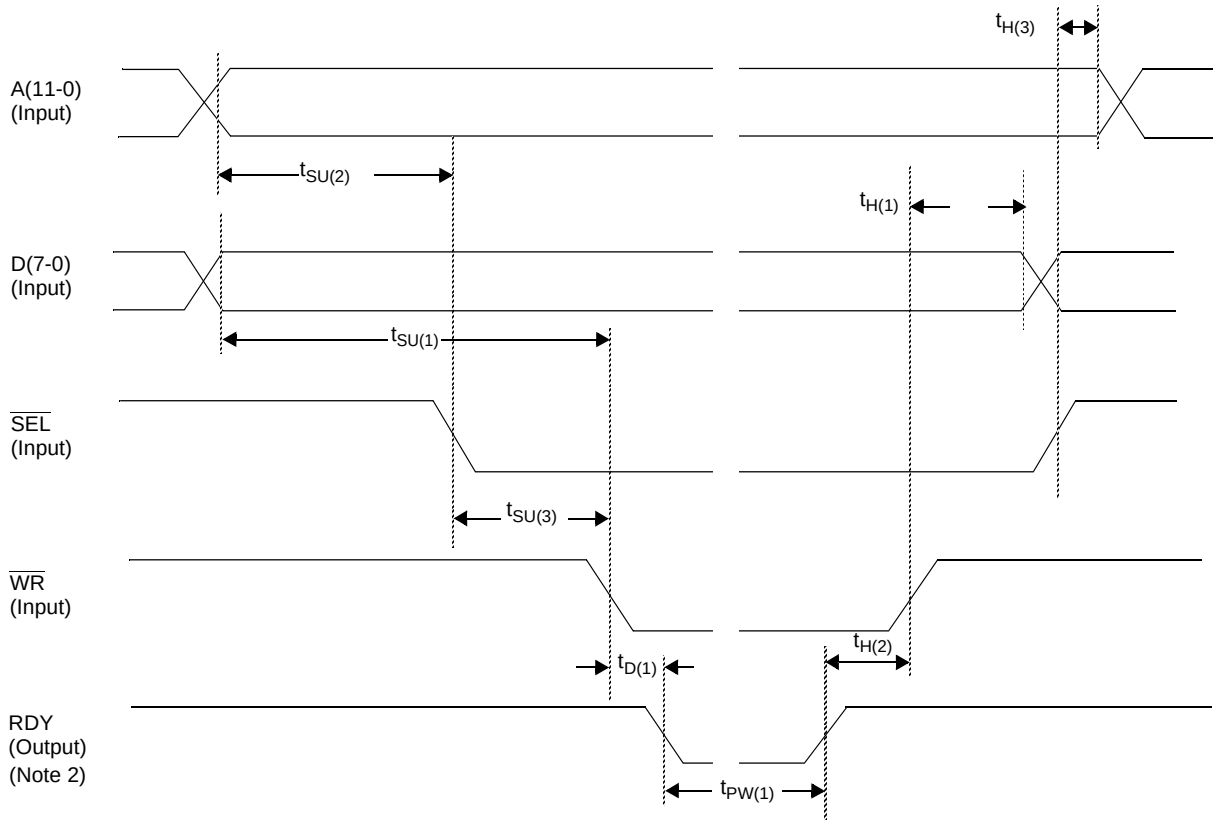
Notes:
1. The CUBIT-622 will hold off the microprocessor for a period of up to 32 cycles of the *CellBus* clock or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 00BH). This occurs only during accesses to the external Translation RAM.
2. RDY is an open drain output signal lead that requires a pull-up resistor to V_{DD} for proper operation.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 54. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(11-0) valid setup time before $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
A(11-0) valid hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			
D(7-0) valid hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	5.0			ns
$\overline{WR}$ hold after RDY$\uparrow$	$t_{H(2)}$	0.0			ns
D(7-0) valid setup time to $\overline{WR}\downarrow$	$t_{SU(1)}$	0.0			ns
$\overline{SEL}$ setup time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0.6			ns
RDY delay after $\overline{WR}\downarrow$	$t_{D(1)}$	0.0		10	ns
RDY pulse width	$t_{PW(1)}$	0.0		Note 1	ns

Notes:

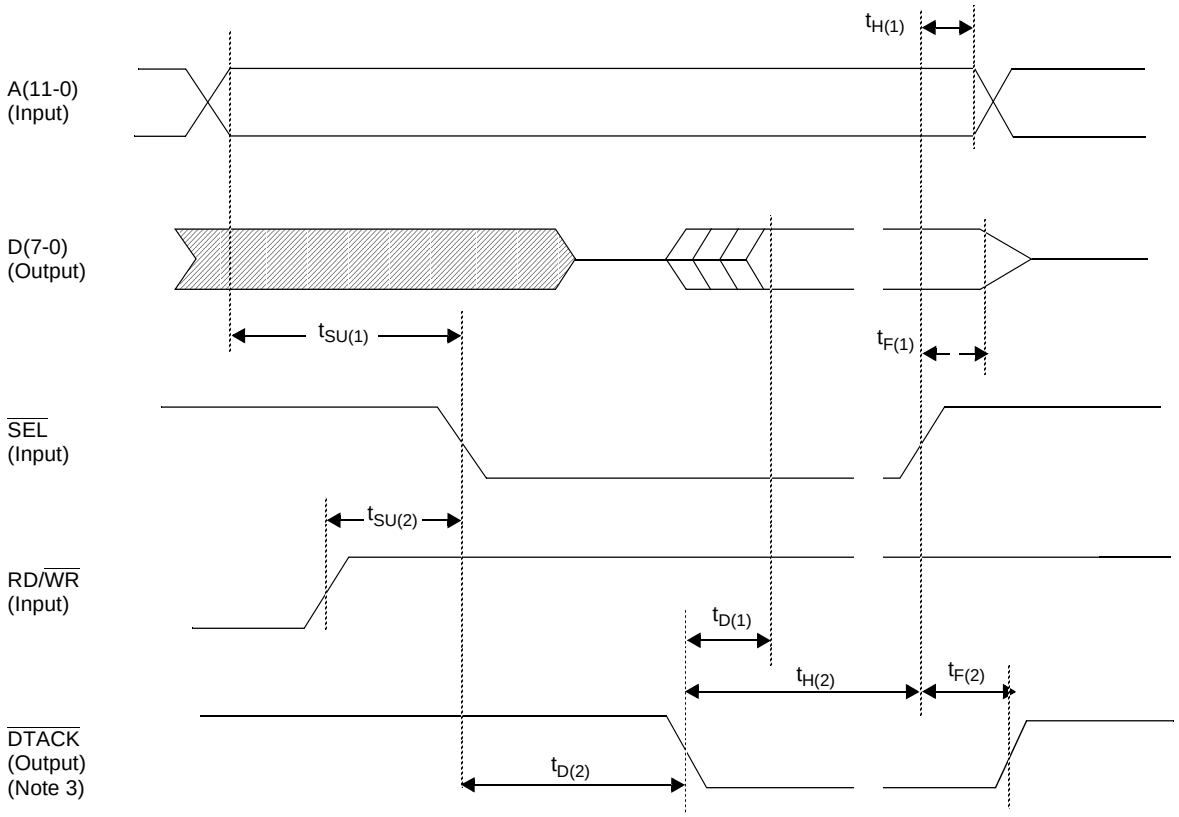
1. The CUBIT-622 will hold off the microprocessor for a period of up to 32 cycles of the *CellBus* clock or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 00BH). This occurs only during accesses to the external Translation RAM.
2. RDY is an open drain output signal lead that requires a pull-up resistor to V_{DD} for proper operation.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 55. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
A(11-0) valid hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			
D(7-0) float time after $\overline{SEL}\uparrow$	$t_{F(1)}$	2.0		7.0	ns
D(7-0) valid output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$			0.0	ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	5.0			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{DTACK}\downarrow$ delay time from $\overline{SEL}\downarrow$	$t_{D(2)}$	Note 1		Note 2	ns
$\overline{DTACK}\uparrow$ float time after $\overline{SEL}\uparrow$	$t_{F(2)}$	2.0		12	ns

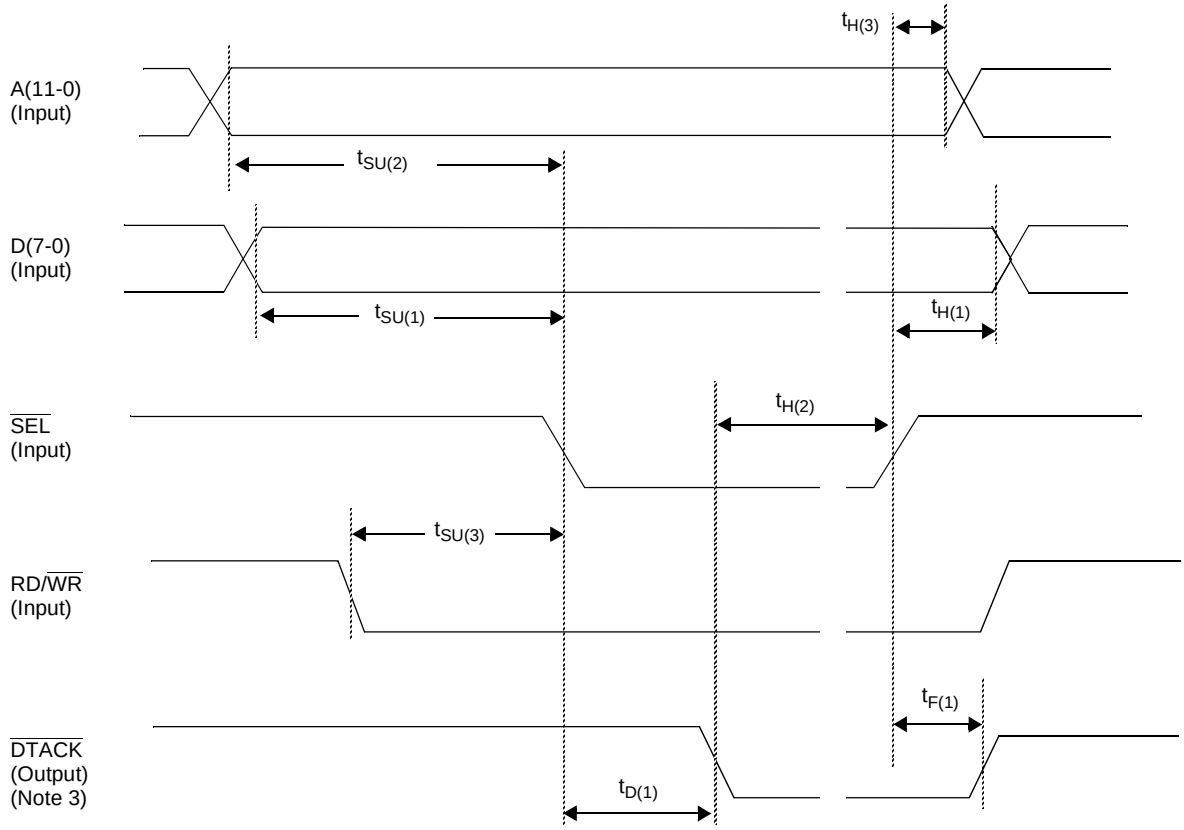
Notes:
1. Two cycles of clock PCLK.
2. The CUBIT-622 will hold off the microprocessor for a period of up to 32 cycles of the *CellBus* clock or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 00BH). This occurs only during accesses to the external Translation RAM.
3. $\overline{DTACK}$ is an open drain output signal lead that requires a pull-up resistor to V_{DD} for proper operation.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 56. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(11-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
A(11-0) valid hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			
D(7-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) valid hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	0.0			ns
RD/$\overline{WR}\downarrow$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	1.0			ns
$\overline{DTACK}\downarrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$	Note 1		Note 2	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(1)}$	2.0		12	ns

Notes:

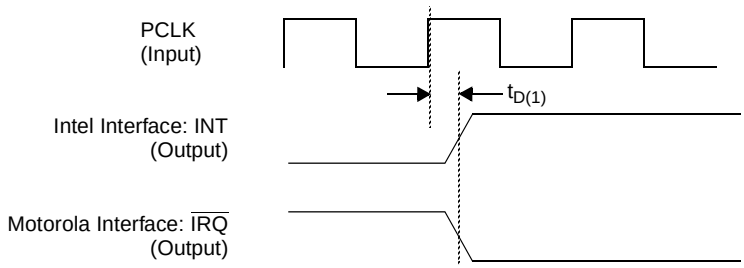
1. Two cycles of clock PCLK.
2. The CUBIT-622 will hold off the microprocessor for a period of up to 32 cycles of the *CellBus* clock or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 00BH). This occurs only during accesses to the external Translation RAM.
3. $\overline{DTACK}$ is an open drain output signal lead that requires a pull-up resistor to V_{DD} for proper operation.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 57. Microprocessor Interrupt Timing



Parameter	Symbol	Min	Typ	Max	Unit
INT/$\overline{IRQ}$ delay after PCLK↑	$t_{D(1)}$	0.0		14	ns

et4U.com

DataShee

DataSheet4U.com

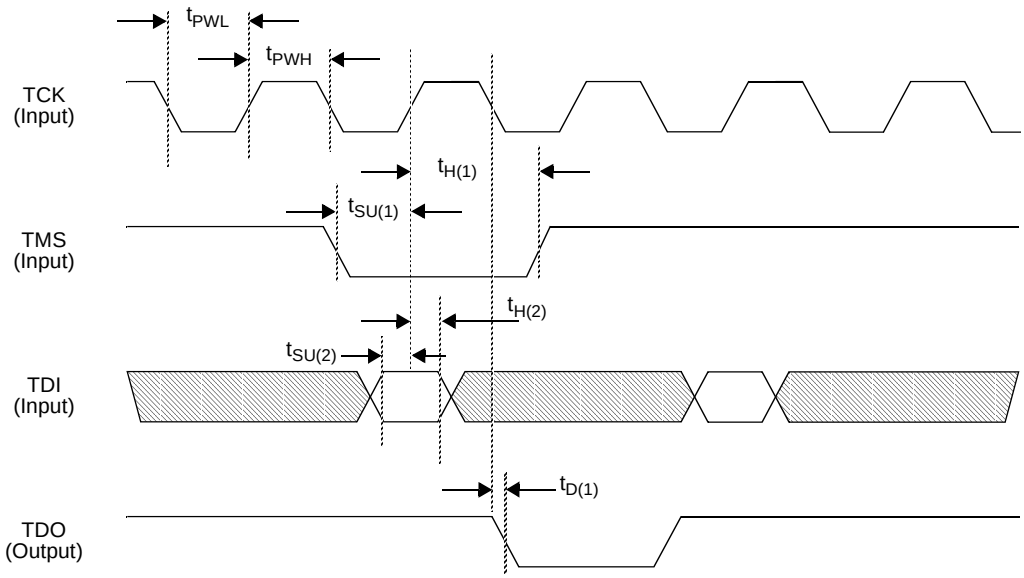
DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Figure 58. Boundary Scan Timing



et4U.com DataShee

Parameter	Symbol	Min	Max	Unit
TCK clock frequency	-	-	20	MHz
TCK duty cycle, t_{PWH} / (t_{PWH} + t_{PWL})	-	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	8.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	3.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	8.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	3.0	-	ns
TDO delay from TCK↓	$t_{D(1)}$	-	12	ns

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MEMORY MAP

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	1	0	1	0	1	1	0	1
002	R	0	0	0	1	0	1	1	0
003[3]	R	0	0	0	0	0	0	0	0
004	R	Mask Revision				Reserved[2]			
005	RC	CTNACK	CTACK	Reserved[2]		BIP-8	CBLOF	CBLORC	CBLOWC
006	R/W	INTENA7	INTENA6	Reserved[2]		INTENA3	INTENA2	INTENA1	INTENA0
007	W	Reserved[2] (set to 00H)							
008	RC	CRCF	CRQOVF	CRQCAV	INSOC	CTSENT	NOGRT	Reserved[2]	
009	R/W	INTEN7	INTEN6	INTEN5	INTEN4	INTEN3	INTEN2	Reserved[2]	
00A	R/W	P1	P0	UNI	TRHENA	Reserved[2]		CTRDY	Reserved[2]
00B	R/W	Reserved[2]		CLKS1	CLKS0	LINEDIV(3-0)			
00C	R/W	ONLINE	TRHIZ	Reserved[2]					
00D	R/W	Reserved[2]							MRCIN
00E	R/W	VRPS1	VRPS0	NOTIGN	0	1	1	1	Reserved[2]
00F	R/W	TIME(7-0)							
010	R/W	Reserved[2]							
011	R/W	Reserved[2]							
012	R/W	Reserved[2]							
013	R/W	LBADDRL(7-0)							
014	R/W	Reserved[2]				LBADDRU(3-0)			
015	R/W	TRAL(7-0)							
016	R/W	TRAU(7-0)							
017	R/W	Reserved[2]				TRAMSB(3-0)			

Notes:
1. R = Read-Only; W = Write-Only; RC = Read and Clear (individual alarm bits remain set to 1 if their causative condition is still present); R/W = Read/Write.
2. Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0 when written.
3. The version of the device is placed in the upper nibble of this byte. The initial version is 0H.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
018	R/W	TRADATA(7-0)							
019	R/W	MRCCTR(7-0)							
01A	R	Reserved[2]							
01B	R/W	INCELLL(7-0) (Lower Byte)							
01C	R/W	INCELLM(7-0) (Middle Byte)							
01D	R/W	INCELLU(7-0) (Upper Byte)							
01E	R	PHYEM	32USER	MASTER	CUBIT-ID(4-0)				
01F	R	Reserved[2]							
020	R	MRCHEAD0(7-0)							
021	R	MRCHEAD1(7-0)							
022	R	MRCHEAD2(7-0)							
023	R	MRCHEAD3(7-0)							
024-05F		Reserved[2]							
060	R	CRQ0(7-0)							
061-092	R	CRQ1(7-0) (061H) through CRQ50(7-0) (092H)							
093	R	CRQ51(7-0)							
094-09F		Reserved[2]							
0A0	R/W	CTQ0(7-0)							
0A1-0D6	R/W	CTQ1(7-0) (0A1H) through CTQ54(7-0) (0D6H)							
0D7	R/W	CTQ55(7-0)							
0D8	R/W	DiscardPHY(7-0)							
0D9	R/W	DiscardPHY(15-8)							
0DA	R/W	DiscardPHY(23-16)							
0DB	R/W	DiscardPHY(31-24)							
0DC	R/W	DiscardPHY(39-32)							
0DD	R/W	DiscardPHY(47-40)							
0DE	R/W	DiscardPHY(55-48)							
0DF	R/W	DiscardPHY(63-56)							
0E0-0FF	R/W	Reserved[2]							

Notes:

1. R = Read-Only; R/W = Read/Write.
2. Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0 when written.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100	R/W	Reserved[2]	NPHY(1-0)		CBMON	PD	NFL	16b	U1
101	R/W	IFECN(3-0)				OutletCellSize(1-0)		InletCellSize(1-0)	
102-104	R/W	Reserved[2]							
105	R/W	XOFF(3-0)				XON(3-0)			
106	R/C	Reserved[2]		TRHCRCF	QF	QMACK	QD	MNF	MF
107	R/W	Reserved[2]		INTENC5	INTENC4	INTENC3	INTENC2	INTENC1	INTENC0
108-109	R/W	Reserved[2]							
10A	R/W	Software Reset							
10B	R/W	Reserved[2]							
10C	R/W	UBR_GFR_Limit(7-0)							
10D	R/W	Reserved[2]		UBR_GFR_Limit(13-8)					
10E	R/W	BPSQS(7-0) (Base Pointer to Start of Queue Space)							
10F	R/W	Reserved[2]						BPSQS(9-8)	
110	R/W	PHY3GFCCMD(1-0)		PHY2GFCCMD(1-0)		PHY1GFCCMD(1-0)		PHY0GFCCMD(1-0)	
111	R/W	PHY7GFCCMD(1-0)		PHY6GFCCMD(1-0)		PHY5GFCCMD(1-0)		PHY4GFCCMD(1-0)	
112	R/W	PHY11GFCCMD(1-0)		PHY10GFCCMD(1-0)		PHY9GFCCMD(1-0)		PHY8GFCCMD(1-0)	
113	R/W	PHY15GFCCMD(1-0)		PHY14GFCCMD(1-0)		PHY13GFCCMD(1-0)		PHY12GFCCMD(1-0)	
114	R/W	PHY19GFCCMD(1-0)		PHY18GFCCMD(1-0)		PHY17GFCCMD(1-0)		PHY16GFCCMD(1-0)	
115	R/W	PHY23GFCCMD(1-0)		PHY22GFCCMD(1-0)		PHY21GFCCMD(1-0)		PHY20GFCCMD(1-0)	
116	R/W	PHY27GFCCMD(1-0)		PHY26GFCCMD(1-0)		PHY25GFCCMD(1-0)		PHY24GFCCMD(1-0)	
117	R/W	PHY31GFCCMD(1-0)		PHY30GFCCMD(1-0)		PHY29GFCCMD(1-0)		PHY28GFCCMD(1-0)	
118	R/W	PHY35GFCCMD(1-0)		PHY34GFCCMD(1-0)		PHY33GFCCMD(1-0)		PHY32GFCCMD(1-0)	
119	R/W	PHY39GFCCMD(1-0)		PHY38GFCCMD(1-0)		PHY37GFCCMD(1-0)		PHY36GFCCMD(1-0)	
11A	R/W	PHY43GFCCMD(1-0)		PHY42GFCCMD(1-0)		PHY41GFCCMD(1-0)		PHY40GFCCMD(1-0)	
11B	R/W	PHY47GFCCMD(1-0)		PHY46GFCCMD(1-0)		PHY45GFCCMD(1-0)		PHY44GFCCMD(1-0)	
11C	R/W	PHY51GFCCMD(1-0)		PHY50GFCCMD(1-0)		PHY49GFCCMD(1-0)		PHY48GFCCMD(1-0)	
11D	R/W	PHY55GFCCMD(1-0)		PHY54GFCCMD(1-0)		PHY53GFCCMD(1-0)		PHY52GFCCMD(1-0)	
11E	R/W	PHY59GFCCMD(1-0)		PHY58GFCCMD(1-0)		PHY57GFCCMD(1-0)		PHY56GFCCMD(1-0)	
11F	R/W	PHY63GFCCMD(1-0)		PHY62GFCCMD(1-0)		PHY61GFCCMD(1-0)		PHY60GFCCMD(1-0)	

1 R = Read-Only; W = Write-Only; RC = Read and Clear (individual alarm bits remain set to 1 if their causative condition is still present); R/W = Read/Write.

2 Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120	R	Reserved[2]							
121	R/W	Maintenance Register (set to 00H)							
122	R/W	Reserved[2]		VBR-RT Discard Threshold(13-8)					
123	R/W	VBR-RT Discard Threshold(7-0)							
124	R	Reserved[2]		VBR-RT Buffer Occupancy Count(13-8)					
125	R	VBR-RT Buffer Occupancy Count(7-0)							
126	R/W	Reserved[2]		VBR-nRT Discard Threshold(13-8)					
127	R/W	VBR-nRT Discard Threshold(7-0)							
128	R	Reserved[2]		VBR-nRT Buffer Occupancy Count(13-8)					
129	R	VBR-nRT Buffer Occupancy Count(7-0)							
12A-12F	R/W	Reserved[2]							
130	R/W	Reserved[2]						DATA/$\overline{\text{CTRL}}$	QMR/$\overline{\text{W}}$
131	R/W	QMADD(7-0)							
132	R/W	QMADD(15-8)							
133	R/W	QMADD(23-16)							
134	R/W-32	QMDATA(31-24)							
135	R/W-32	QMDATA(23-16)							
136	R/W-32	QMDATA(15-8)							
137	R/W-32	QMDATA(7-0)							
138-1B7	R/W	16-Bit Discard Cell Counters DISCTRn(15-0) for port n = 0 - 63 (even Address is MSB)							
1B8-1FF	R/W	Reserved[2]							
200	R/W	Multicast Session 0, Port Enables 7-0, MST0(7-0)							
201	R/W	Multicast Session 0, Port Enables 15-8, MST0(15-8)							
202	R/W	Multicast Session 0, Port Enables 23-16, MST0(23-16)							
203	R/W	Multicast Session 0, Port Enables 31-24, MST0(31-24)							
204	R/W	Multicast Session 0, Port Enables 39-32, MST0(39-32)							
205	R/W	Multicast Session 0, Port Enables 47-40, MST0(47-40)							
206	R/W	Multicast Session 0, Port Enables 55-48, MST0(55-48)							
207	R/W	Multicast Session 0, Port Enables 63-56, MST0(63-56)							
208-9F7	R/W	Multicast Sessions 1-254, Port Enables 63-0 (254 sets of registers, MSTs(7-0), MSTs(15-8), MSTs(23-16), MSTs(31-24), MSTs(39-32), MSTs(47-40), MSTs(55-48) and MSTs(63-56), where s is multicast session number 1 - 254)							

1 R = Read-Only; W = Write-Only; RC = Read and Clear (individual alarm bits remain set to 1 if their causative condition is still present); R/W = Read/Write.

2 Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9F8	R/W	Multicast Session 255, Port Enables 7-0, MST255(7-0)							
9F9	R/W	Multicast Session 255, Port Enables 15-8, MST255(15-8)							
9FA	R/W	Multicast Session 255, Port Enables 23-16, MST255(23-16)							
9FB	R/W	Multicast Session 255, Port Enables 31-24, MST255(31-24)							
9FC	R/W	Multicast Session 255, Port Enables 39-32, MST255(39-32)							
9FD	R/W	Multicast Session 255, Port Enables 47-40, MST255(47-40)							
9FE	R/W	Multicast Session 255, Port Enables 55-48, MST255(55-48)							
9FF	R/W	Multicast Session 255, Port Enables 63-56, MST255(63-56)							
A00	R/W	Reserved[2]	Lookahead Clock Count		PHY0ADDR(4-0)				
A01	R/W	PHYEN(7-0)							
A02	R/W	PHYEN(15-8)							
A03	R/W	PHYEN(23-16)							
A04	R/W	PHYEN(31-24)							
A05	R/W	PHYEN(39-32)							
A06	R/W	PHYEN(47-40)							
A07	R/W	PHYEN(55-48)							
A08	R/W	PHYEN(63-56)							
A09-A0F	R/W	Reserved[2]							
A10	R/W	Reserved[2]							
B00	R/W	Reserved[2]							MCCS0
B01	R/W	Reserved[2]							MCCS1
B(n)	R/W	Reserved[2]							MCCSn
BFF	R/W	Reserved[2]							MCCS255

1 R = Read-Only; W = Write-Only; RC = Read and Clear (individual alarm bits remain set to 1 if their causative condition is still present); R/W = Read/Write.

2 Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

MEMORY MAP DESCRIPTIONS

DEVICE IDENTIFICATION AND RESET BITS

Address *	Bit	Symbol	Description
000-002 003	7-0 3-0	DEVID	Device identification code (28 bits). Part number code (05805) is located in top 20 bits. Next 7 bits are manufacturer ID (107). LSB is 1, in Address 000H, Bit 0.
003	7-4		Version number.
004	7-4		Mask revision level.
	3-0	--	Reserved bits.
007	7-0	--	Reserved bits, set to 0.
10A	7-0	Software Reset	Software Reset: Writing a 91 Hex into this location will generate a software reset to the CUBIT-622. Writing other than 91 Hex to this location will remove the CUBIT-622 from the reset state. Reading this location will return a 00 Hex if the CUBIT-622 is not in reset and 01 Hex if the CUBIT-622 is in reset. Software Reset resets all registers except configuration registers.

* All addresses in memory map description tables are hexadecimal. Reserved and “Don’t Care” addresses are not listed.

et4U.com DataShee

STATUS AND INTERRUPT-ENABLE BITS

DataSheet4U.com

Address	Bit	Symbol	Description
005	7	CTNACK	This bit is set to 1 when the cell transmitted from the control queue was rejected from the *CellBus*. It will generate a microprocessor interrupt if bit 7 (INTENA7) is set to one in the interrupt enable location at address 006H.
	6	CTACK	This bit is set to 1 when the cell transmitted from the control queue was accepted from the *CellBus*. It will generate a microprocessor interrupt if bit 6 (INTENA6) is set to one in the interrupt enable location at address 006H.
	5-4	--	Reserved bits.
	3	BIP-8	This bit is set to 1 when a BIP-8 error is detected in the receiver. It will generate a microprocessor interrupt if bit 3 (INTENA3) is set to one in the interrupt enable location at address 006H.
	2	CBLOF	This bit is set to 1 if the *CellBus* frame pulse is not present for two consecutive frame pulse times ($\overline{U32}$ = low) or four consecutive frame pulse times ($\overline{U32}$ = high). It will generate a microprocessor interrupt if bit 2 (INTENA2) is set to one in the interrupt enable location at address 006H.
	1	CBLORC	This bit is set to 1 if the *CellBus* read clock is not present for more than the equivalent of 32 PCLK cycles. It will generate a microprocessor interrupt if bit 1 (INTENA1) is set to one in the interrupt enable location at address 006H.
	0	CBLOWC	This bit is set to 1 if the *CellBus* write clock is not present for more than the equivalent of 32 PCLK cycles. It will generate a microprocessor interrupt if bit 0 (INTENA0) is set to one in the interrupt enable location at address 006H.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
006	7	INTENA7	Interrupt enabled for CTNACK, if = 1.
	6	INTENA6	Interrupt enabled for CTACK, if = 1.
	5-4	--	Reserved bits, set to 0.
	3	INTENA3	Interrupt enabled for BIP-8, if = 1.
	2	INTENA2	Interrupt enabled for CBLOF, if = 1.
	1	INTENA1	Interrupt enabled for CBLORC, if = 1.
	0	INTENA0	Interrupt enabled for CBLOWC, if = 1.
008	7	CRCF	This bit is set to 1 to indicate a CRC check error has occurred in a CBRH of a cell received from the *CellBus*. It will generate a microprocessor interrupt if bit 7 (INTEN7) is set to one in the interrupt enable location at address 009H.
	6	CRQOVF	This bit is set to 1 to indicate loss of an incoming control cell, due to overflow of the internal 16-cell control cell receive queue. It will generate a microprocessor interrupt if bit 6 (INTEN6) is set to one in the interrupt enable location at address 009H.
	5	CRQCAV	This bit is set to 1 to indicate that a control cell is present in the control cell receive queue, CRQ. It will generate a microprocessor interrupt if bit 5 (INTEN5) is set to one in the interrupt enable location at address 009H.
	4	INSOC	This bit is set to 1 to indicate a cell inlet Start of Cell error occurrence. It will generate a microprocessor interrupt if bit 4 (INTEN4) is set to one in the interrupt enable location at address 009H.
008 (cont.)	3	CTSENT	This bit is set to 1 to indicate that a control cell has been sent to the *CellBus* from the control cell transmit buffer. It will generate a microprocessor interrupt if bit 3 (INTEN3) is set to one in the interrupt enable location at address 009H.
	2	NOGRT	This bit is set to 1 to indicate that no *CellBus* access grant has been received by the inlet side, after a *CellBus* access request, within a time established by register TIME (register 00FH). It will generate a microprocessor interrupt if bit 2 (INTEN2) is set to one in the interrupt enable location at address 009H.
	1-0	--	Reserved bits.
009	7	INTEN7	Interrupt enabled for CRCF, if = 1.
	6	INTEN6	Interrupt enabled for CRQOVF, if = 1.
	5	INTEN5	Interrupt enabled for CRQCAV, if = 1.
	4	INTEN4	Interrupt enabled for INSOC, if = 1.
	3	INTEN3	Interrupt enabled for CTSENT, if = 1.
	2	INTEN2	Interrupt enabled for NOGRT, if = 1.
	1-0	--	Reserved bits, set to 0.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
106	7-6	--	Reserved bits.
	5	TRHCRCF	This bit is set to 1 when the CRC4 check fails over the Tandem Routing Header. It will generate a microprocessor interrupt if bit 5 (INTENC5) is set to one in the interrupt enable location at address 107H.
	4	QF	This bit is set to 1 to indicate a queue has reached its limit and indiscriminate discard will commence for that queue. It will generate a microprocessor interrupt if bit 4 (INTENC4) is set to one in the interrupt enable location at address 107H.
	3	QMACK	This bit is set to 1 when a Queue Manager read or write operation has been completed. It will generate a microprocessor interrupt if bit 3 (INTENC3) is set to one in the interrupt enable location at address 107H.
	2	QD	This bit is set to 1 when all cells destined for all ports whose configuration bits DiscardPHYn are set to 1 have been discarded, where n is the port number. It will generate a microprocessor interrupt if bit 2 (INTENC2) is set to one in the interrupt enable location at address 107H.
	1	MNF	This bit is set to 1 if buffer memory is filled and then a cell is taken from the queue. It indicates that memory is now available to store another cell. It will generate a microprocessor interrupt if bit 1 (INTENC1) is set to one in the interrupt enable location at address 107H.
	0	MF	This bit is set to 1 after a cell is written in a queue, and there is no space available in memory to enqueue another cell. This is an indication that memory is full and indiscriminate cell discard will start for all queues. It will generate a microprocessor interrupt if bit 0 (INTENC0) is set to one in the interrupt enable location at address 107H.
107	7-6	--	Reserved bits, set to 0.
	5	INTENC5	Interrupt enabled for TRHCRCF, if = 1.
	4	INTENC4	Interrupt enabled for QF, if = 1.
	3	INTENC3	Interrupt enabled for QMACK, if = 1.
	2	INTENC2	Interrupt enabled for QD, if = 1.
	1	INTENC1	Interrupt enabled for MNF, if = 1.
	0	INTENC0	Interrupt enabled for MF, if = 1.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
01E	7	PHYEM	This bit is set to 0 to enable PHY layer emulation in UTOPIA modes. When this bit is set to 1, ATM layer emulation is enabled.
	6	32USER	This is a shadow bit for the $\overline{U32}$ input lead. This bit is set to 1 if lead $\overline{U32}$ is high. A 0 indicates that the CUBIT-622 is operated in 32-user mode. A 1 indicates 16-user mode.
	5	MASTER	This is a shadow bit for the $\overline{ENARB}$ input lead. It is set to 1 if $\overline{ENARB}$ is high. A 0 indicates that the CUBIT-622 is the master Arbiter of the *CellBus*.
	4-0	CUBIT-ID (4-0)	This is a shadow field for the $\overline{UA(4-0)}$ input leads. It contains the address ID set at leads $\overline{UA(4-0)}$. These lead states are detected at power-up and if any of the $\overline{UA(4-0)}$ inputs change state. For example, the CUBIT-622 *CellBus* ID is 1FH if the $\overline{UA(4-0)}$ leads are all low.

et4U.com

DataShee

DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

DEVICE MODE CONTROL BITS

Address	Bit	Symbol	Description
00A	7-6	P1, P0	These bits are used to set *CellBus* access priority of this CUBIT-622 device. Possible values are: high priority, P1=1, P0=1; medium priority, P1=1, P0=0; low priority, P1=0, P0=1; no request, P1=0, P0=0.
	5	UNI	If = 1, UNI operation, VPI field width = 8 bits. If = 0, NNI operation, VPI field width = 12 bits.
	4	TRHENA	This bit must be written to 1.
	3-2	--	Reserved bits, set to 0.
	1	CTRDY	Set to 1 by microprocessor to indicate that a control cell is ready to be sent. Cleared by CUBIT-622 when cell has been sent and the queue is able to receive cells.
	0	--	Reserved bit, set to 0.
00B	7-6	--	Reserved bits, set to 0.
	5-4	CLKS1, CLKS0	Clock source selection bits for the cell inlet/outlet clock, which are used in conjunction with LINEDIV(3-0) in bits 3-0 of this register. The coding followed is: CLKS1, CLKS0 = 0,0: Cell interface clock = *CellBus* write clock frequency / $2^{LINEDIV}$ CLKS1, CLKS0 = 0,1: Reserved, do not use CLKS1, CLKS0 = 1,0: Cell interface clock = PCLK clock frequency / $2^{LINEDIV}$ CLKS1, CLKS0 = 1,1: Reserved, do not use
	3-0	LINEDIV (3-0)	Cell inlet clock frequency control. Frequency will be equal to the frequency of the selected clock source, divided by 2-to-the-power-LINEDIV.
00C	7	ONLINE	This bit sets device operational status. If = 1, the CUBIT-622 is online and all functions are operating. If = 0, the CUBIT-622 is offline. In offline condition, no cells are accepted from the cell inlet, the interface outputs are tristated, and only control and loopback cells are accepted from the *CellBus*.
	6	TRHIZ	Translation RAM interface tristate bit. When set to 1 and the ONLINE bit is 0, the Translation RAM interface is put in Hi-Z mode.
	5-0	--	Reserved bits, set to 0.
00D	7-1	--	Reserved bits, set to 0.
	0	MRCIN	Bit is set to 1 to indicate that a misrouted cell has been received. Cleared by a write operation.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
00E	7, 6	VRPS1, VRPS0	VCI Records per Page Selection bits. These bits select the number of VCI records per page (VRP) to be either 256, 512, 1024 or 128, as shown below: VRPS1,VRPS0= 0,0: VRP is 256 VRPS1,VRPS0= 0,1: VRP is 512 VRPS1,VRPS0= 1,0: VRP is 1024 VRPS1,VRPS0= 1,1: VRP is 128
	5	NOTIGN	Ignore translation record I-bit. When set to 1, connections marked as I-bit=1 in the translation records will be treated as if I-bit=0.
	4	0	This bit must be written to 0.
	3	1	This bit must be written to 1.
	2	1	This bit must be written to 1.
	1	1	This bit must be written to 1.
	0	--	Reserved bit, set to 0.
00F	7-0	TIME(7-0)	Time-out counter preset value for bus access watchdog timer. Counter starts to count down from this value each time a *CellBus* access request is made. If count reaches 00H before a grant is received, alarm bit NOGRT is set in register 008H. Each count represents one *CellBus* frame cycle.
100	7	--	Reserved bit, set to 0.
	6-5	NPHY(1-0)	A two bit code used to indicate the range of PHYs supported. NPHY(1-0) is used to preserve TRAM space when not using all 64 PHYs. The coding is as follows: 00: 8 or fewer PHYs (4 or fewer PHYs for NNI) 01: 16 or fewer PHYs 10: 32 or fewer PHYs 11: 64 or fewer PHYs
	4	CBMON	When this bit is set to 1, the CUBIT-622 accepts all traffic coming in from the *CellBus* regardless of the *CellBus* ID to which cells are addressed. The cells are enqueued based on *CellBus* ID. *CellBus* IDs 0-15 are enqueued in service class 0 (CBR) queues for ports 0-15, and IDs 16-31 are enqueued in service class 1 (VBR-rt) queues for ports 0-15, respectively. There are separate queues for multicast and broadcast cells, and a trash queue for cells which had a CRC4 error.
	3	PD	When set to 1, packet discard is enabled for the UBR/GFR queues. When set to 0, cell discard is disabled for these queues.
	2	NFL	New Free List. When set to '1', a new head of free list is retrieved from BPSQS(9-0) in registers 10FH and 10EH.
	1	16b	The CUBIT-622 operates in 16-bit wide UTOPIA mode when this bit is set to 1 or in 8-bit wide UTOPIA mode when it is set to 0.
	0	U1	UTOPIA Mode: Setting this bit to 1 puts the UTOPIA interface into UTOPIA Level 1 mode (Single-PHY). When this bit is set to 0, the interface is in UTOPIA Level 2 mode (Multi-PHY).

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
101	7-4	IFECN(3-0)	Enable insertion of FECN if = 1 on a per service class basis. The EFCI bit (middle bit of PT field) will be set = 1 if the given service class queue length equals or exceeds 27 less than the maximum queue length, and the corresponding bit of IFECN(3-0) is set to 1. IFECN0 corresponds to the highest priority queue (CBR).
	3-2	OutletCellSize (1-0)	00: 53 bytes in 8-bit mode, 54 bytes in 16-bit mode 01: Reserved 10: Reserved 11: 57 bytes in 8-bit mode, 58 bytes in 16-bit mode
	1-0	InletCellSize (1-0)	00: 53 bytes in 8-bit mode, 54 bytes in 16-bit mode 01: Reserved 10: Reserved 11: 57 bytes in 8-bit mode, 58 bytes in 16-bit mode
105	7-4	XOFF(3-0)	Flow control field used to replace the outgoing GFC field in a cell for a given port when PHYnGFCCMD is set to '11' in registers 110H to 11FH (where n is the port number).
	3-0	XON(3-0)	Flow control field used to replace the outgoing GFC field in a cell for a given port when PHYnGFCCMD is set to '10' in registers 110H to 11FH (where n is the port number).
10C	7-0	UBR_GFR_Limit (7-0)	Lower 8 bits of a 14-bit value representing the maximum fill level for aggregate of UBR/GFR queues. When the sum of all UBR/GFR queues exceeds the UBR_GFR_Limit all UBR/GFR queues will go in UBR/GFR discard mode. While in this mode, all UBR/GFR cells will be discarded. The exit condition is when the aggregate UBR/GFR count drops below the UBR_GFR_Limit.
10D	7-6	--	Reserved bits, set to 0.
	5-0	UBR_GFR_Limit (13-8)	Upper 6 bits of 14-bit UBR/GFR fill level defined above in address 10CH.
110	7-0	PHYnGFCCMD (1-0), (n = 3 -0)	GFC Insertion Command: For each bit pair field: Bit 1, when set to 1, enables the insertion of either the XOFF or XON fields into the outgoing GFC field of a cell for PHY n. Bit 0, when set to 1, selects the XON field. When bit 0 is set to 0, the XOFF field is inserted.
111	7-0	PHYnGFCCMD (1-0), (n = 7-4)	See address 110H above.
112	7-0	PHYnGFCCMD (1-0), (n = 11-8)	See address 110H above.
113	7-0	PHYnGFCCMD (1-0), (n = 15-12)	See address 110H above.
114	7-0	PHYnGFCCMD (1-0), (n = 19-16)	See address 110H above.
115	7-0	PHYnGFCCMD (1-0), (n = 23-20)	See address 110H above.
116	7-0	PHYnGFCCMD (1-0), (n = 27-24)	See address 110H above.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
117	7-0	PHYnGFCCMD (1-0), (n = 31-28)	See address 110H above.
118	7-0	PHYnGFCCMD (1-0), (n = 35-32)	See address 110H above.
119	7-0	PHYnGFCCMD (1-0), (n = 39-36)	See address 110H above.
11A	7-0	PHYnGFCCMD (1-0), (n = 43-40)	See address 110H above.
11B	7-0	PHYnGFCCMD (1-0), (n = 47-44)	See address 110H above.
11C	7-0	PHYnGFCCMD (1-0), (n = 51-48)	See address 110H above.
11D	7-0	PHYnGFCCMD (1-0), (n = 55-52)	See address 110H above.
11E	7-0	PHYnGFCCMD (1-0), (n = 59-56)	See address 110H above.
11F	7-0	PHYnGFCCMD (1-0), (n = 63-60)	See address 110H above.
120	7-0	--	Reserved bits, set to 0.
121	7-0	--	Maintenance register. Must be written to 00H.
122	7-6	--	Reserved bits, set to 0.
	5-0	VBRRT_DTH	VBR-rt Discard Threshold(13-8). Upper 6 bits of a 14-bit value representing the aggregate fill level of VBR-rt queues. When the sum of all VBR-rt queues exceeds the VBR-rt limit, all VBR-rt queues will go into VBR-rt discard mode. While in this mode, all VBR-rt cells will be discarded. The exit condition is when the aggregate VBR-rt count drops below the VBR-rt limit.
123	7-0	VBRRT_DTL	VBR-rt Discard Threshold(7-0). Lower 8 bits of the 14-bit VBR-rt fill level defined above at Address 122H.
124	7-6	--	Reserved bits, set to 0.
	5-0	VBRRT_CNTH	VBR-rt Buffer Occupancy Count(13-8). Upper 6 bits of a 14-bit value representing the aggregate cell count of the VBR-rt queues.
125	7-0	VBRRT_CNTL	VBR-rt Buffer Occupancy Count(7-0). Lower 8 bits of the 14-bit VBR-rt buffer occupancy count defined above at Address 124H.
126	7-6	--	Reserved bits, set to 0.
	5-0	VBRNRT_DTH	VBR-nrt Discard Threshold(13-8). Upper 6 bits of a 14-bit value representing the aggregate fill level of VBR-nrt queues. When the sum of all VBR-nrt queues exceeds the VBR-nrt limit, all VBR-nrt queues will go into VBR-nrt discard mode. While in this mode, all VBR-nrt cells will be discarded. The exit condition is when the aggregate VBR-nrt count drops below the VBR-nrt limit.
127	7-0	VBRNRT_DTL	VBR-nrt Discard Threshold(7-0). Lower 8 bits of the 14-bit VBR-nrt fill level defined above at Address 126H.

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
128	7-6	--	Reserved bits, set to 0.
	5-0	VBRNRT_CNTH	VBR-nrt Buffer Occupancy Count(13-8). Upper 6 bits of a 14-bit value representing the aggregate cell count of the VBR-nrt queues.
129	7-0	VBRNRT_CNTL	VBR-nrt Buffer Occupancy Count(7-0). Lower 8 bits of the 14-bit VBR-nrt buffer occupancy count defined above at Address 128H.
A00	7	--	Reserved bit, set to 0.
	6-5	Lookahead Clock Count	2-bit field that determines the number of clock cycles before the FIFO full/empty that Clav should be deasserted. This provides a lookahead function to avoid FIFO overflow. 00 = 1 cycle, 01 = 2 cycles, 10 = 3 cycles and 11 = 4 cycles. This parameter controls the deassertion of Clav in cell mode.
	4-0	PHY0ADDR(4-0)	5-bit UTOPIA Level 2 address set for port 0: Note: Addresses for Ports 1-15 are in sequential order from PHY0ADDR.
A01	7-0	PHYEN(7-0)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 7-0. These bits do not affect cells with multicast addresses.
A02	7-0	PHYEN(15-8)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 15-8. These bits do not affect cells with multicast addresses.
A03	7-0	PHYEN(23-16)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 23-16. These bits do not affect cells with multicast addresses.
A04	7-0	PHYEN(31-24)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 31-24. These bits do not affect cells with multicast addresses.
A05	7-0	PHYEN(39-32)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 39-32. These bits do not affect cells with multicast addresses.
A06	7-0	PHYEN(47-40)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 47-40. These bits do not affect cells with multicast addresses.
A07	7-0	PHYEN(55-48)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 55-48. These bits do not affect cells with multicast addresses.
A08	7-0	PHYEN(63-56)	When the bit corresponding to the port number is set to 0 the port is not polled in Multi-PHY mode, and outlet queued cells destined for the port are discarded. Any or all bits may be set to 0 for ports 63-56. These bits do not affect cells with multicast addresses.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

LOOPBACK CONTROL ADDRESS REGISTER

Address	Bit	Symbol	Description
013	7-0	LBADDRL (7-0)	8 LSB of Loopback Routing Header, bits 11-4 of *CellBus* Routing Header (see Figure 28).
014	7-4	--	Reserved bits, set to 0.
	3-0	LBADDRU (3-0)	4 MSB of Loopback Routing Header, bits 15-12 of *CellBus* Routing Header (see Figure 28).

TRANSLATION RAM READ/WRITE CONTROL

Address	Bit	Symbol	Description
015	7-0	TRAL(7-0)	8 LSB of the translation RAM address [leads TRA(7-0)].
016	7-0	TRAU(7-0)	Middle 8 bits of the translation RAM address [leads TRA(15-8)].
017	7-4	--	Reserved bits, set to 0.
	3-0	TRAMSB (3-0)	4 MSB of the translation RAM address [leads TRA(19-16)].
018	7-0	TRADATA (7-0)	Data read from, or to be written into, the translation RAM at the address defined by leads TRA(19-0) [leads TRD(7-0)].

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

SSRAM READ/WRITE CONTROL

Address	Bit	Symbol	Description
10E	7-0	BPSQS (7-0)	These are the lower 8 bits of the base pointer to start of queue space address indicating the start of the queue space in SSRAM. This address is used to reserve the lower segment of SSRAM space for customer use. To change the value of the base pointer address, write to address locations 10EH and 10FH and then set the NFL bit (Bit 2 in Address 100H) to 1. The sum of the base pointer address and the total queue space is equal to the available SSRAM memory.
10F	7-2	--	Reserved bits, set to 0.
	1-0	BPSQS (9-8)	These are the upper 2 bits of the base pointer address to start of queue space, as described above for Address 10EH.
130	7-2	--	Reserved bits, set to 0.
	1	DATA/$\overline{\text{CTRL}}$	This bit is used in FIFO operations in conjunction with control bits QMR/$\overline{\text{W}}$, QMADD and QMDATA. Setting this bit to 1 directs all queue operations to data space (SSRAM), while setting it to 0 directs all operations to control space (FPT RAM).
	0	QMR/$\overline{\text{W}}$	Writing a 1 to this bit enables a read operation from the address pointed to by QMADD. Writing a 0 to this bit enables a write operation to the address pointed to by QMADD. The sequence of steps for a read operation should be as follows: 1) set QMR/$\overline{\text{W}}$ to 1, and then 2) write the appropriate address to QMADD. Valid data will be in QMDATA when event QMACK becomes set to 1. The sequence of steps for a write operation should be as follows: 1) set QMR/$\overline{\text{W}}$ to 0, 2) write the appropriate address to QMADD, and then 3) write the proper information into QMDATA. The operation is concluded when event bit QMACK becomes set to 1.
131 132 133	7-0 7-0 7-0	QMADD (7-0) QMADD (15-8) QMADD (23-16)	These 24 bits identify the address for which the queue manager read or write operation will occur. Addresses supported for control space are listed below: 0-1023 FPT Access for 256 queues 1024 Active Bits for PHY 31-0 Service Category 0 1025 Active Bits for PHY 63-32 Service Category 0 1026, 1027 Active Bits for PHY 63-0 Service Category 1 1028, 1029 Active Bits for PHY 63-0 Service Category 2 1030, 1031 Active Bits for PHY 63-0 Service Category 3 1032 Current Head of the Free List All addresses are available for data space (i.e., when DATA/$\overline{\text{CTRL}}$ = 1).

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
134	7-0	QMDATA (31-24)	32-bit data read from memory when a read operation is initiated or written to memory when a write operation is initiated. For a write operation, the MSB is written first in address 134H, and the LSB is written last in address 137H.
135	7-0	QMDATA (23-16)	
136	7-0	QMDATA (15-8)	
137	7-0	QMDATA (7-0)	

et4U.com

DataShee

DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

COUNTERS AND MISROUTED CELL HEADERS

Address	Bit	Symbol	Description
019	7-0	MRCCTR(7-0)	Count of cell inlet misrouted cells received. Rollover type
01B	7-0	INCELLL(7-0)	Bits 7-0 (8 LSB) of count of incoming cells (see Note 1). Rollover type.
01C	7-0	INCELLM(7-0)	Bits 15-8 of count of incoming cells (see Note 1). Rollover type.
01D	7-0	INCELLU(7-0)	Bits 23-16 (8 MSB) of count of incoming cells (see Note 1). Rollover type.
020	7-0	MRCHEAD0(7-0)	Fourth (least significant) byte of the header of the first misrouted cell received after this buffer was last cleared. This least significant byte of the ATM cell corresponds to VCI[3-0] (LSB), PT and CLP of the ATM cell header. See Figure 6, cycle number 2.
021	7-0	MRCHEAD1(7-0)	Third byte of above header.
022	7-0	MRCHEAD2(7-0)	Second byte of above header.
023	7-0	MRCHEAD3(7-0)	First (most significant) byte of above header.
138, 139 to 1B6, 1B7	7-0	DISCTRn(15-0), (n = 0 - 63)	Cell count of all cells that are discarded for port n due to memory congestion. Cells that are discarded due to *CellBus* congestion are not counted. The paired registers are 16-bit saturating counters for ports 0 to 63. Addresses 138H and 139H correspond to the 16-bit counter for port 0, addresses 13AH and 13BH correspond to the 16-bit counter for port 1, etc. The even address is the most significant byte of the count. When reading these two bytes, because they are not latched, it is recommended to read the lower byte first, then the higher byte, and then the lower byte again, to avoid errors.
Note 1: To read the INCELL counter, first read INCELLL (01BH), then INCELLM (01CH), and last INCELLU (01DH). To write (clear) the INCELL counter, first write INCELLU (01DH) to 00H, then INCELLM (01CH), and last INCELLL (01BH).			

CONTROL CELL RECEIVE AND TRANSMIT QUEUE

Address	Bit	Symbol	Description
060-093	7-0	CRQi(7-0)	Control cell receive queue buffer, 52 bytes (i = 0-51).
0A0-0D7	7-0	CTQi(7-0)	Control cell transmit queue buffer, 56 bytes (i = 0-55).
0D8	7-0	DiscardPHY (7-0)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0D9	7-0	DiscardPHY (15-8)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0DA	7-0	DiscardPHY (23-16)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0DB	7-0	DiscardPHY (31-24)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
0DC	7-0	DiscardPHY (39-32)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0DD	7-0	DiscardPHY (47-40)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0DE	7-0	DiscardPHY (55-48)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.
0DF	7-0	DiscardPHY (63-56)	When set to 1 outlet queued cells destined for PHY n are discarded. When the discard is completed, this bit is reset to 0. Register 0DFH needs to be written to start the discard process.

MULTICAST SESSION MEMORY

Address	Bit	Symbol	Description
200	7-0	MST0(7-0)	Multicast session number 0: Enable bits for ports 7-0. When an individual bit is set to 1, that port participates in the multicast session.
201	7-0	MST0(15-8)	Multicast session number 0: Enable bits for ports 15-8. When an individual bit is set to 1, that port participates in the multicast session.
202	7-0	MST0(23-16)	Multicast session number 0: Enable bits for ports 23-16. When an individual bit is set to 1, that port participates in the multicast session.
203	7-0	MST0(31-24)	Multicast session number 0: Enable bits for ports 31-24. When an individual bit is set to 1, that port participates in the multicast session.
204	7-0	MST0(39-32)	Multicast session number 0: Enable bits for ports 39-32. When an individual bit is set to 1, that port participates in the multicast session.
205	7-0	MST0(47-40)	Multicast session number 0: Enable bits for ports 47-40. When an individual bit is set to 1, that port participates in the multicast session.
206	7-0	MST0(55-48)	Multicast session number 0: Enable bits for ports 55-48. When an individual bit is set to 1, that port participates in the multicast session.
207	7-0	MST0(63-56)	Multicast session number 0: Enable bits for ports 63-56. When an individual bit is set to 1, that port participates in the multicast session.
208-9F7	7-0	MST1-MST254 (7-0), (15-8), (23-16), (31-24), (39-32), (47-40), (55-48), (63-56)	Multicast Sessions numbers 1-254: 254 sets of 8 registers, as described above for MST0.
9F8	7-0	MST255(7-0)	Multicast session number 255: Enable bits for ports 7-0. When an individual bit is set to 1, that port participates in the multicast session.
9F9	7-0	MST255(15-8)	Multicast session number 255: Enable bits for ports 15-8. When an individual bit is set to 1, that port participates in the multicast session.
9FA	7-0	MST255(23-16)	Multicast session number 255: Enable bits for ports 23-16. When an individual bit is set to 1, that port participates in the multicast session.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

Address	Bit	Symbol	Description
9FB	7-0	MST255(31-24)	Multicast session number 255: Enable bits for ports 31-24. When an individual bit is set to 1, that port participates in the multicast session.
9FC	7-0	MST255(39-32)	Multicast session number 255: Enable bits for ports 39-32. When an individual bit is set to 1, that port participates in the multicast session.
9FD	7-0	MST255(47-40)	Multicast session number 255: Enable bits for ports 47-40. When an individual bit is set to 1, that port participates in the multicast session.
9FE	7-0	MST255(55-48)	Multicast session number 255: Enable bits for ports 55-48. When an individual bit is set to 1, that port participates in the multicast session.
9FF	7-0	MST255(63-56)	Multicast session number 255: Enable bits for ports 63-56. When an individual bit is set to 1, that port participates in the multicast session.
B00	7-1	--	Reserved bits, set to 0.
	0	MCCS0	Multicast Control session number 0: When this bit is set to 1, the CUBIT-622 participates in this control multicast session.
B01	7-1	--	Reserved bits, set to 0.
	0	MCCS1	Multicast Control session number 1: When this bit is set to 1, the CUBIT-622 participates in this control multicast session.
Bn	7-1	--	Reserved bits, set to 0.
	0	MCCSn	Multicast Control session number n: When this bit is set to 1, the CUBIT-622 participates in this control multicast session.
BFF	7-1	--	Reserved bits, set to 0.
	0	MCCS255	Multicast Control session number 255: When this bit is set to 1, the CUBIT-622 participates in this control multicast session.

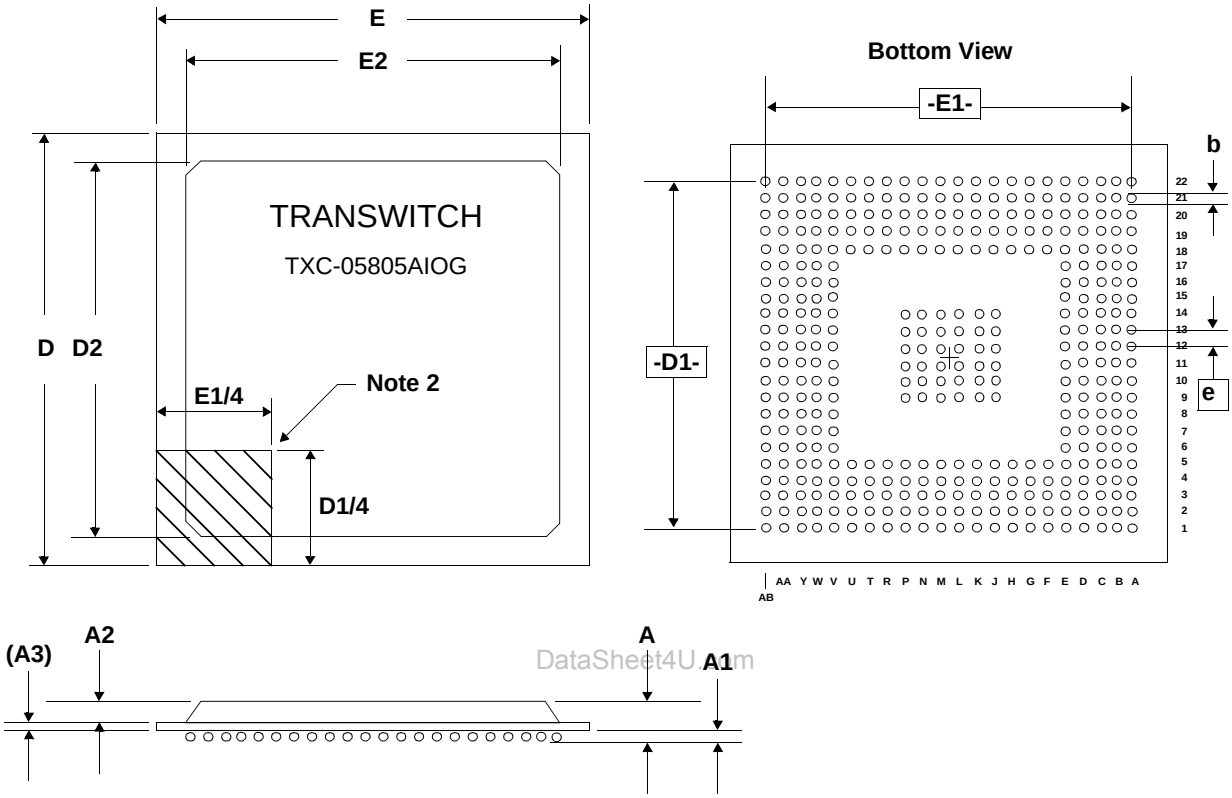
DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

PACKAGE INFORMATION

The CUBIT-622 device is available in a 376-lead plastic ball grid array (PBGA) suitable for surface mounting, as shown in Figure 59.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

Dimension (Note 1)	Min	Max
A A1 A2	2.02 0.40 1.12	2.44 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 59. CUBIT-622 TXC-05805 376-Lead Plastic Ball Grid Array Package

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

ORDERING INFORMATION

Part Number: TXC-05805AIOG 376-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

Figure 60 illustrates typical applications of the CUBIT-622 in a DSLAM with STS-3/STM-1 and STS-12/STM-3 Uplink Application. The other TranSwitch devices included in this diagram are included in the following descriptions of related products:

TXC-05802B, CUBIT-*Pro* Device (ATM *CellBus* Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus*. *CellBus* technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05804, CUBIT-3 VLSI Device (Multi-PHY *CellBus* Switch Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

et4U.com DataShee DataSheet4U.com

TXC-05810, ASPEN Device (Multi-Service *CellBus* Switch). ASPEN supports *CellBus* operation in both Cell and Packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or alternatively, to provide greater system throughput. Line interface is via UTOPIA 1 or 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables is stored in an external synchronous SRAM.

TXC-06203, PHAST-3P Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This is an STM-1/STS-3c section, line and path overhead termination device that provides CDB or PPP (HDLC) processing using an 8-bit or 16-bit UTOPIA Single-PHY or Multi-PHY interface for downstream access. A bit-serial or byte-parallel line interface is provided.

TXC-06212, PHAST-12E VLSI Device (Four-channel SONET STS-3c or STM-1 Overhead Terminator). This PHAST-12E VLSI device provides programmable, high performance ATM/Packet/Transmission for Level 12 applications with enhanced features.

REFERENCE DOCUMENTS

- The ATM Forum: UTOPIA Specification Level 2, Version 1.0, June 1995.
- The ATM Forum: Traffic Management Specification, Version 4.1, March 1999.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

APPLICATION EXAMPLE

DSLAM Application with STS-3/STM-1 and STS-12/STM-4 Uplinks

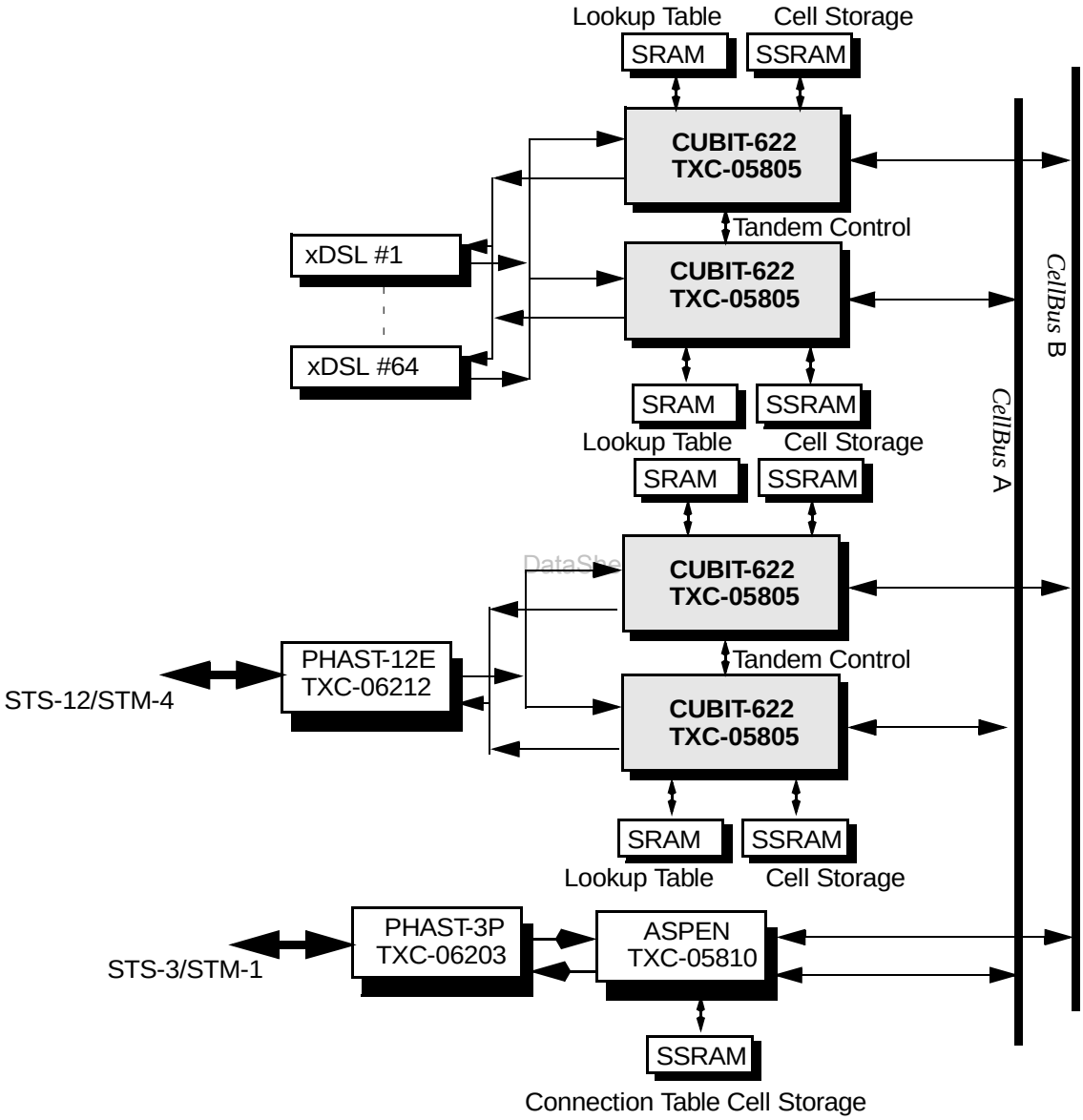


Figure 60. CUBIT-622 TXC-05805 and Related Product Applications

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

et4U.com DataShee

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

DataSheet4U.com

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated Product Preview CUBIT-622 Data Sheet that have significant differences relative to the previous and now superseded Product Preview CUBIT-622 Data Sheet:

Updated CUBIT-622 Data Sheet: *PRELIMINARY* Ed. 5, June 2002 2001

Previous CUBIT-622 Data Sheet: *PRELIMINARY* Ed. 4, December 2001

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Updated FEATURES and APPLICATIONS sections. In block diagram drawing, changed on line side, changed Cell Inlet to UTOPIA Inlet, and changed Cell Outlet to UTOPIA Outlet. Changed copyright year.
7	In Transmit Mode section, changed first sentence in first paragraph explaining proper UTOPIA master polling.
9	In TRAM Memory Interface section, changed in last sentence in paragraph, access time from 15 ns to 14 ns. Added section " Power Up Sequencing".
10	In *CellBus* Operation section, changed last sentence in first paragraph to " With a maximum *CellBus* frequency of 40MHz...".
12	Modified $\overline{\text{CBCONG}}$ description in third paragraph.
32	Changed in first sentence address 800H to 80000000H. Made same change to Free List Configuration section, step 5.
50, 51	Removed 50MHz reference in description for symbols RxCLKI , RxCLKO and symbols TxCLKI, TxCLKO.
57	Updated Power Requirements table.
58	In table for INPUT PARAMETERS FOR CMOSpd, changed Input Current parameter from 127.9 to 137 µA. In table for INPUT PARAMETERS FOR CMOSpu, changed input current from 127.9 to 137 µA
82	In table for Figure 51, changed Max time for $t_{D(2)}$ from 7.4 to 8.7 ns.
83	In table for Figure 52, changed Max time for $t_{Z(1)}$ from 9.6 to 11.2 ns. Changed Max time for $t_{D(3)}$ from 7.9 to 8.4 ns.
115	Updated List of Data Sheet Changes section.

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

- NOTES -

et4U.com

DataShee

DataSheet4U.com

TranSwitch reserves the right to make changes to the product(s) or circuit(s) described herein without notice. No liability is assumed as a result of their use or application. TranSwitch assumes no liability for TranSwitch applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TranSwitch warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TranSwitch covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

PRELIMINARY information documents contain information on products in the sampling, pre-production or early production phases of the product life cycle. Characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.

DataSheet4U.com

www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

- NOTES -

et4U.com DataShee

DataSheet4U.com

DataSheet4U.com www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

TRANSWITCH®

Engines for Global Connectivity

et4U.com

DataSheet4U.com

DataSheet4U.com