ATM AccessEDGE™ Firmware for ASPEN
TXC-05812

PRODUCT INFORMATION

FEATURES

- Cell Processing
  - Cell discrimination on VPI/VCI (UNI/NNI support)
  - Support for up to 64k active connections
  - Spatial Multicast capability
  - Support for Early/Partial Packet Discard
  - Support for local or *CellBus* -based Host processor
  - Support for over-reservation of GFR traffic
  - Support for WFQ scheduling of GFR traffic
- Traffic Management
  - UPC/NPC per virtual connection using GCRA (Dual Leaky Bucket algorithm)
  - Traffic parameters supported (Peak Cell Rate, Cell Delay Variation, Sustained Cell Rate, Burst Tolerance)
  - Support of Cell Tagging and Discard
  - Frame Tagging support for GFR Traffic
- OAM
  - OAM F4/F5 Fault Management according to
    - ITU-T I.610,
    - Bellcore GR1248-CORE,
    - ETSI ETS 300 404
  - OAM F4 Termination/F5 Generation
  - OAM cell insertion and extraction through host interface

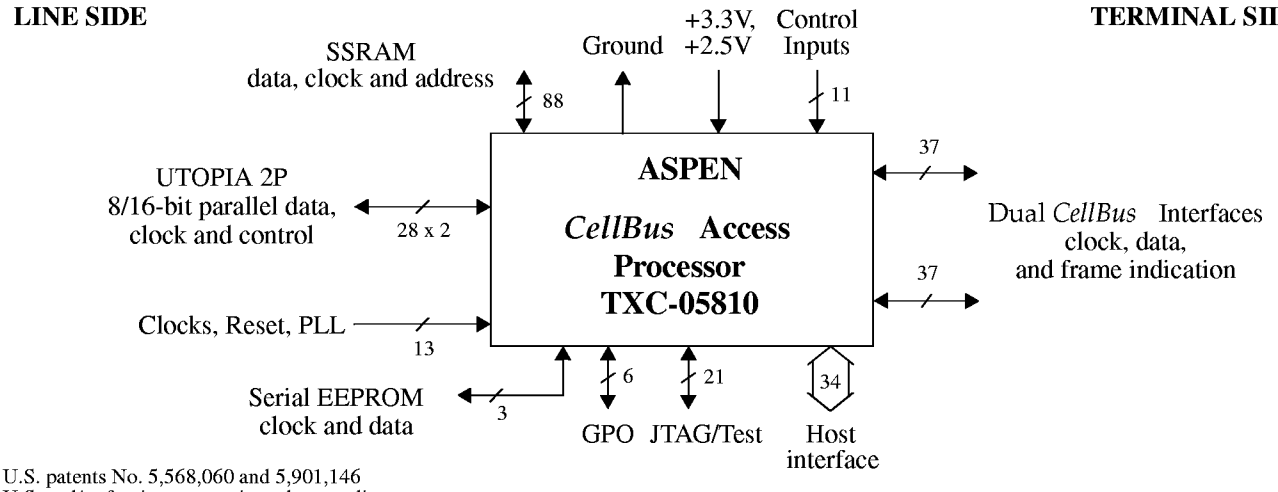
DESCRIPTION

The ASPEN VLSI device (TXC-05810) is a revolutionary, RISC-based processor designed to support the requirements of next-generation multi-service access systems. Firmware for the RISC processors is downloaded to internal instruction RAM to establish ASPEN operational parameters. This document describes the features, control and data flow supported when ASPEN is used in conjunction with the ATM AccessEDGE™ line-side and net-side firmware products.

ATM AccessEDGE firmware implements the ATM Layer processing functions of the ATM UNI/NNI, performing cell discrimination for up to 64k connections, payload type discrimination, loss priority indication, and selective cell discarding as well as ATM Layer Management functions, fault management (alarm surveillance, connectivity verification, and invalid VPI/VCI identification), traffic management and congestion control features.

APPLICATIONS

- ATM access multiplexers
- VoATM voice gateway
- ATM LAN switches



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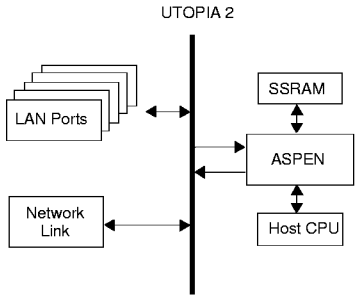
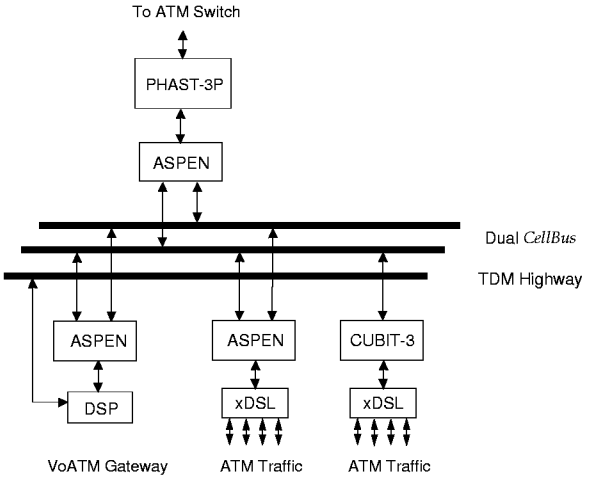
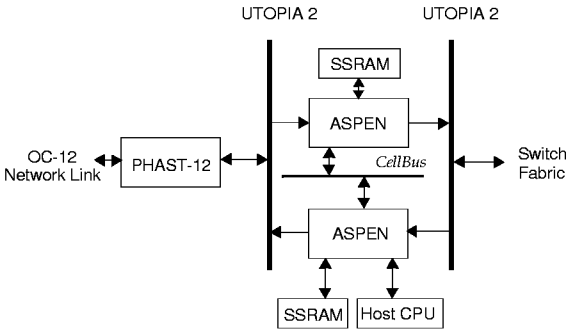
APPLICATION DIAGRAMS



Single-chip LAN switch



ATM Access Mux



622 Mbit/s ATM Processor

RELATED PRODUCTS

- TXC-05150 — ATM Cell Delineation Block VLSI Device (CDB)
- TXC-05501 — ATM/SMDS Segmentation Controller (SARA-R)
- TXC-05601 — ATM/SMDS Reassembly Controller (SARA-S)
- TXC-05802B — *CellBus* Bus Switch (CUBIT-*Pro*)
- TXC-05804 — Multi-PHY *CellBus* Access Device (CUBIT-3)
- TXC-05810 — *CellBus* Access Processor (ASPEN)
- TXC-06112 — Programmable, High-performance ATM/packet/transmission, SONET/SDH Terminator for Level 12 (PHAST-12)
- TXC-06203 — STM-1/STS-3c SDH/SONET Overhead Terminator with PPP/CDB UTOPIA Interface (PHAST-3P)

FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products, including details of UTOPIA 2P interface specifications and other available operational firmware.

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