AsTriX™ Device
CellBus® Expansion Switch
TXC-05840

TECHNICAL OVERVIEW

FEATURES

- Interoperable with CUBIT®-3 (TXC-05804), CUBIT-622 (TXC-05805), Sertopia™ (TXC-05860), and ASPEN® (TXC-05810) UTOPIA Level 2 interface
- Non-blocking switching capacity
- 8 UTOPIA Level 2 ports at rates of up to OC-12
- Configurable cell (or packet chunk) size per port of 52 to 64 bytes
- Switch engine operating at 33 MHz or 50 MHz system clock
- Switch bandwidth determined by the system clock and settings
- Host insertion/extraction for the local host interface
- 16-bit general purpose microprocessor interface operating up to 33 MHz
- Motorola MPC850/860 microprocessor compatible
- Backpressure mechanism to avoid cell loss
- Two priority levels supported for both unicast and multicast to any combination of destination ports
- Per port statistics supported
- Chip diagnostic mode supported
- Built in self test for power-on reset
- LED leads for chip status and port status
- Test Access Port for IEEE 1149.1 boundary scan
- +3.3 V and +1.8 V power supplies
- 640-lead Plastic Ball Grid Array package (PBGA), 31 mm x 31 mm

DESCRIPTION

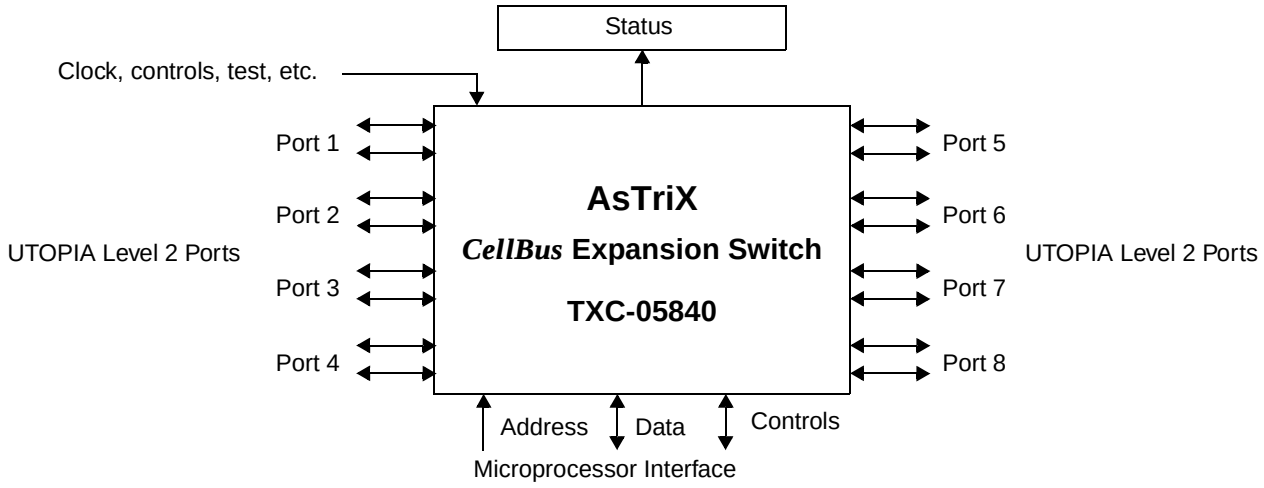
The AsTriX™ (TXC-05840) *CellBus* Expansion Switch is a single chip switching solution for ATM systems. In order to meet the accelerating need for bandwidth in access systems, the AsTriX is designed to allow higher *CellBus* throughput by aggregating multiple *CellBus* shelves through a switch, and is capable of rates up to 800 Mbit/s per port. The AsTriX ports support UTOPIA Level 2 interfaces. The switch is non-blocking, incorporating a backpressure mechanism for eliminating congestion towards any one port.

The switch may be used to scale a *CellBus* architecture to deliver up to 9.6 Gbit/s system bandwidth, by connecting up to 8 *CellBus* segments (each capable of 1.2 Gbit/s switching). A single port (or multiple ports) may be used to implement an OC-12 uplink in a mux application.

Together with TranSwitch's CUBIT, ASPEN and Sertopia family devices, the AsTriX switch device can be used to create a cost effective point-to-point serial backplane based access system.

APPLICATIONS

- Remote Access Concentrators
- Multi-service Access Devices
- Digital Cross Connect Systems
- DSLAM
- Routers
- Aggregation of multiple *CellBus* shelves



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LIST OF FIGURES

APPLICATION EXAMPLE

The application diagram in Figure 1 shows the usage of the AsTriX in a *CellBus* Shelf Aggregation Application.

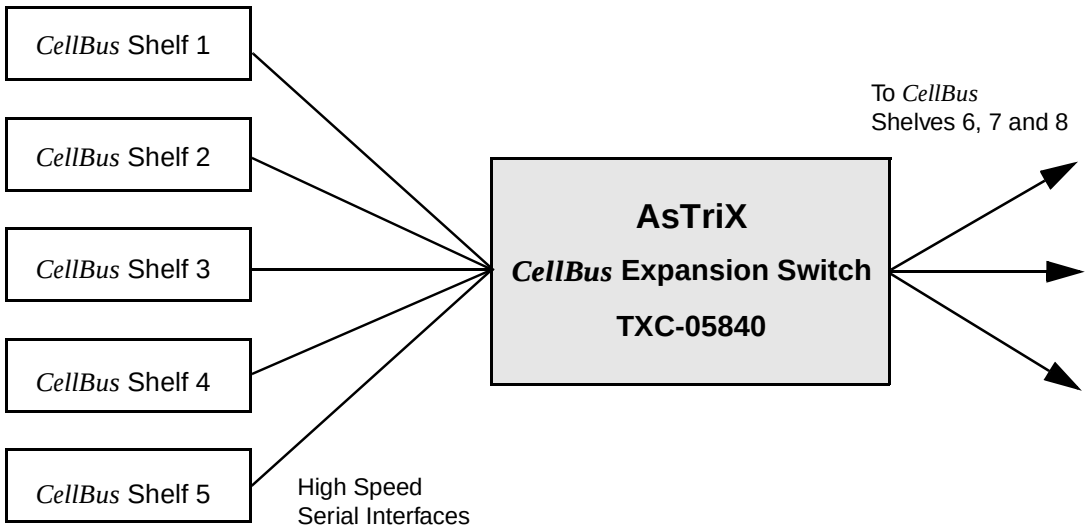


Figure 1. *CellBus* Shelf Aggregation Application Using the AsTriX TXC-05840

Port density is at the heart of driving costs down for service providers. Physical layout constraints limit the number of ports that can be connected to a single line card and the number of line cards that can be put in a single shelf. However, by providing the ability to switch between multiple *CellBus* shelves it is feasible to effectively extend the number of ports in the system to include all of the ports on all of the shelves, thereby increasing the port density of the system as shown in Figure 1 above. This is a more cost effective solution than using an edge switch with OC-12 interfaces.

INTEROPERABILITY

The AsTriX works directly with the following TranSwitch devices:

- CUBIT-3 (TXC-05804)
- CUBIT-622 (TXC-05805)
- ASPEN (TXC-05810)
- Sertopia (TXC-05860)

FUNCTIONAL DESCRIPTION

A block diagram of the AsTriX device is shown in Figure 2. Further information on device operation and the interfaces to external circuits is provided below.

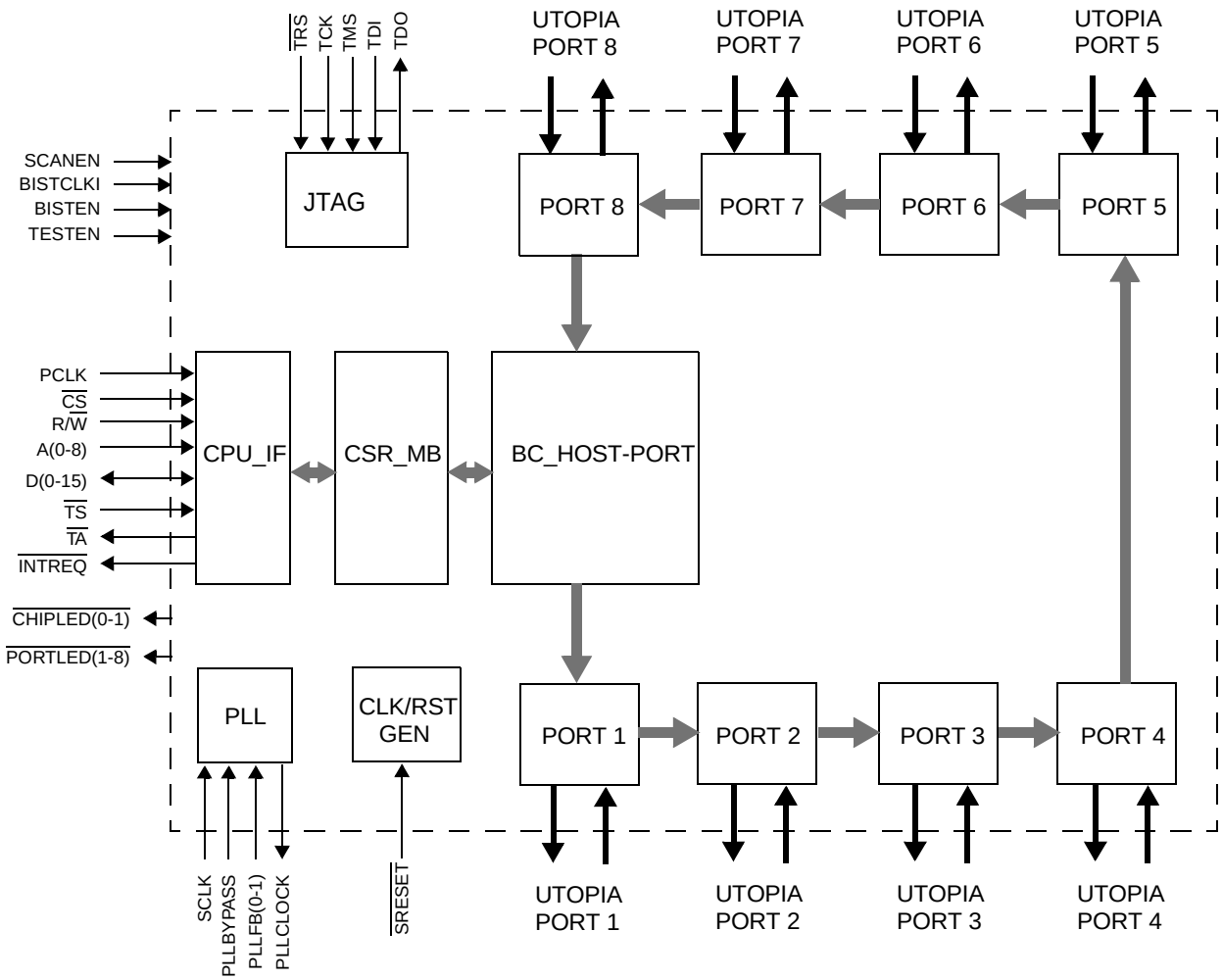


Figure 2. AsTriX TXC-05840 Block Diagram

The AsTriX *CellBus* Expansion Switch device is a cell-based switch, consisting of an internal unidirectional slotted looped bus, a bus controller, a microprocessor interface, and eight UTOPIA Level 2 switch ports, PORT1 - PORT8. The HOST-PORT is a special purpose port inside the bus controller for control cell access between a microprocessor host and the switch.

The bus controller performs several functions: 1) it continuously generates fixed size time slots, or free cells to the bus; 2) it terminates received cells and relays undelivered cells to the bus; 3) it provides a host microprocessor interface for switch management and control cell access between the host and remote processors through one or multiple switch ports; and 4) it collects switch statistics.

UTOPIA PORT

Each UTOPIA port is a full duplex switch port consisting of the following elements: 2 ingress FIFO buffers (high-priority and low-priority), full duplex switch engine access, 5 egress FIFO queues, a flow control mechanism consisting of a counter array and a backpressure indication, as well as a 16-bit mode UTOPIA Level 2 compliant interface. Figure 3 below provides an overall switch port block diagram from an architectural viewpoint.

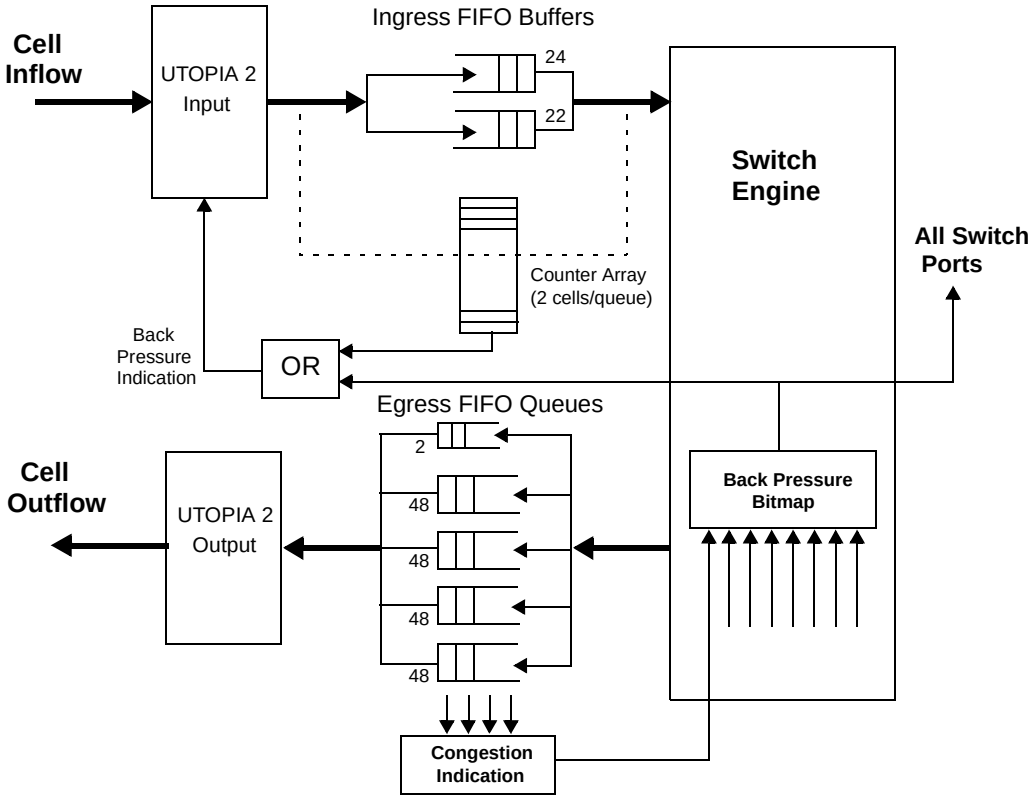


Figure 3. Switch Port Structure

All the switch ports are homogeneous. Each switch port provides an 800 Mbit/s information rate for full duplex cell transmission and reception.

The AsTriX provides prioritized cell switching. It supports high and low priorities for multicast cell switching, high and low priorities for unicast cell switching, and control cell switching. The cell switching priority sequence is control, high priority multicast, high priority unicast, low priority multicast and low priority unicast, in descending order. Each switch port has 5 egress FIFO queues, with one queue for each class of traffic.

The AsTriX includes a 16-bit microprocessor interface defined as the HOST-PORT. The HOST-PORT is a special port for switch access by the host. The sole traffic type passing through this port is called control traffic which is always switched through high priority cell delivery. Logically, the HOST-PORT is the first switch bus interface from the bus controller in the bus direction.

CELL STRUCTURE

The switch supports two switch modes: ATM and native. During switch initialization, the switch mode is selected by the configuration register setting. The cell structure in ATM mode is different from that of native mode. In ATM mode, the source switch port address needs to be inserted into the UDF field of each ATM cell by ingress switch ports. In native mode, there is no such address insertion.

PRIORITIZED CELL SWITCHING

A two level prioritized bus access scheme is used for cell switching between all the participating switch ports. Control traffic, high priority multicast and high priority unicast utilize high priority bus access to transfer cells and the rest utilize low priority for bus access. With this arrangement, even when the switch is overloaded, high priority traffic is guaranteed bus access.

UNICAST AND MULTICAST CELL DELIVERY

The switch supports both unicast and multicast cell deliveries. Unicast is performed via point-to-point cell delivery, a source switch port transfers a cell to a destination switch port. The source switch port is responsible for filling the destination address field based on the destination address polled by an external UTOPIA Level 2 device. Two separate port/queues are reserved for multicast, representing high and low priority.

STATISTICS COLLECTION

There are two types of statistics to be collected: switch based (global) statistics and switch port based statistics. A counter is used for each statistics collection. To prevent any counter overflow, the host periodically reads all those statistics counters. When a counter reaches half full, i.e., the most significant bit changes from 0 to 1, it generates an interrupt to the host (if not masked). The host may mask such interrupts to avoid excessive interrupt processing.

OPERATION MODES

The AsTriX has four operation modes, the Reset Mode (RST_MODE), Initialization Mode (INIT_MODE), Normal Mode (NORMAL_MODE), and Diagnostic Mode (DIAG_MODE), as illustrated in Figure 4 above. Switch operation will be changed from one mode to the other upon issuance of command by the local host.

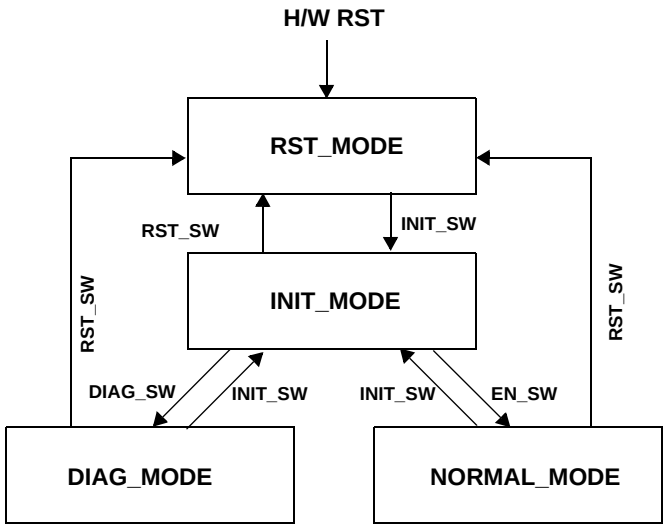


Figure 4. AsTriX Operation Modes

Details can be found in the operation mode description of the AsTriX.

OTHER INTERFACES

Microprocessor Interface

The AsTriX integrates a 16-bit microprocessor, or host interface for transferring data and control information. This interface is Motorola MPC850/860 (The interface byte-lane model is big endian). This interface permits a host processor to configure the AsTriX device and obtain statistics from the bus controller, and from each switch port. Management traffic is also inserted and extracted by the host through this interface to communicate with remote processors connected to CUBIT-3 (TXC-05804), CUBIT-622 (TXC-05805), ASPEN (TXC-05810) or other devices.

Boundary Scan (Test Access) Port

The test interface includes a five-lead Test Access Port (TAP) as the boundary scan port that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external input/output leads from the TAP for board and component test.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	$V_{DD1.8}$	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	$V_{DD3.3}$	-0.3	3.9	V	Notes 1, 4
DC input voltage	V_{IN}	-0.5	6.0	V	Notes 1, 4
Output Voltage	V_{out}	-0.5	4.6	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-Up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.8V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		14.5		°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

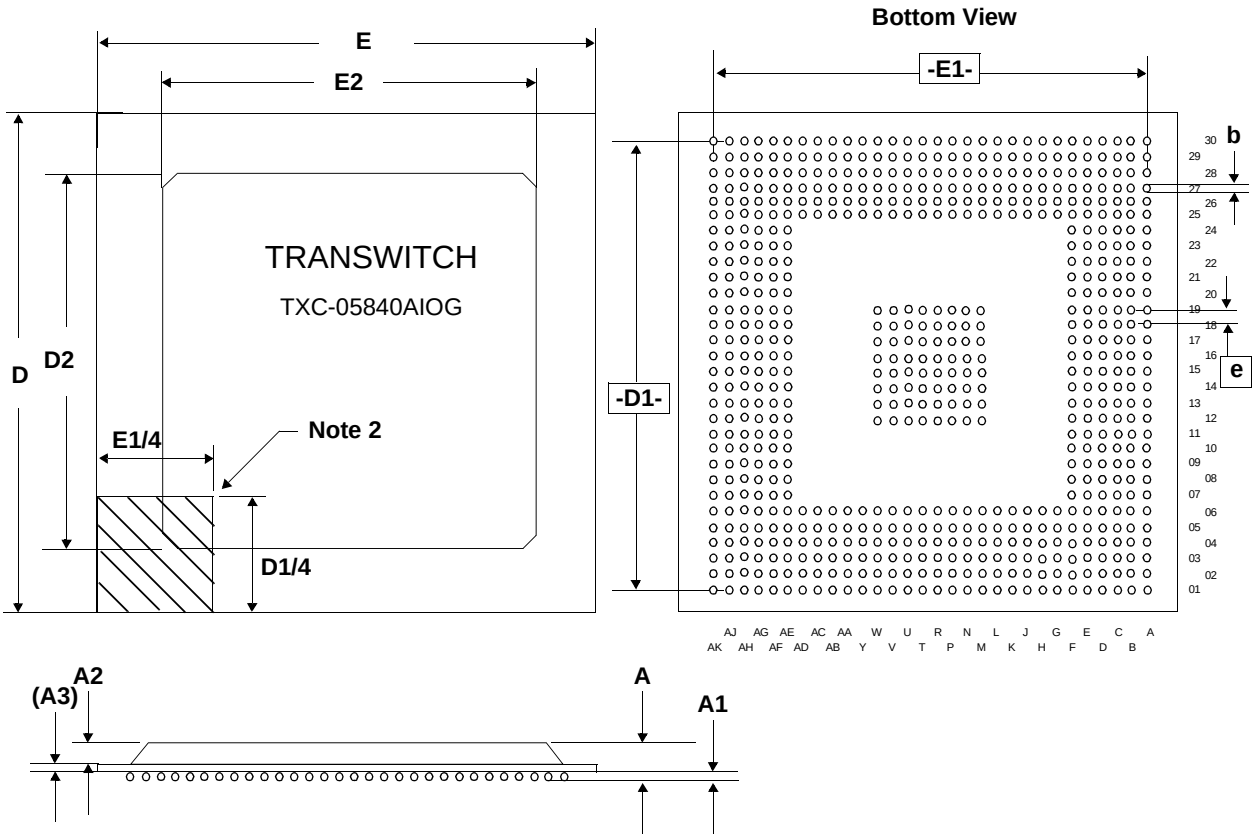
Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{DD3.3}$	3.15	3.3	3.45	V	
$I_{DD3.3}$			100	mA	See Notes 1 and 2
$P_{DD3.3}$			350	mW	See Notes 1 and 2
$V_{DD1.8}$	1.71	1.8	1.89	V	
$I_{DD1.8}$			1350	mA	See Notes 1 and 2
$P_{DD1.8}$			2550	mW	See Notes 1 and 2
Total power		2400	2900	mW	

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

PACKAGE INFORMATION

The AsTriX device is packaged in a 640-lead Plastic Ball Grid Array (PBGA) package suitable for surface mounting, as illustrated in Figure 5.



Dimension (Note 1)	Min	Max
A A1 A2	2.00 0.50 1.12	2.50 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	30.80	31.20
D1 (Nom)	29.00	
D2	27.95	28.70
E	30.80	31.20
E1 (Nom)	29.00	
E2	27.95	28.70
e (Ref.)	1.0	

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 30 x 30, JEDEC code MS-034A.

Figure 5. AsTriX TXC-05840 640-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-05840AIOG 640-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

Figure 1 illustrates a typical application of the AsTriX *CellBus* Switch device in a generic architecture for ATM access switching. The other related TranSwitch devices are briefly described below:

TXC-05804, CUBIT-3 VLSI Device (*CellBus* Bus Switch). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05805, CUBIT-622 VLSI Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO have been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-05810, ASPEN Device (*CellBus* Access Processor). ASPEN supports *CellBus* operation in both cell and packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or alternatively, to provide greater system throughput. Line interface is via UTOPIA 1 or 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables is stored in an external synchronous SRAM.

TXC-05860, Sertopia VLSI Device (UTOPIA Serializer). A single-chip solution for broadband communication systems. The Sertopia device interfaces two remote UTOPIA ports transparently across a serial link. The Sertopia emulates a UTOPIA Level 2 master or UTOPIA Level 2 slave and contains a SERDES (serializer/deserializer) core which transfers the cell or packet chunk along with the UTOPIA port information.

REFERENCE DOCUMENTS

- The ATM Forum: UTOPIA Specification Level 1, Version 2.0.1, March 1994.
- The ATM Forum: UTOPIA Specification Level 2, Version 1.0, June 1995.
- MPC860 PowerQUICCTM User's Manual, Motorola 1998.
- MC68360 QUICC User's Manual, Motorola.
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990.

- NOTES -

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