Sertopia™ Device
UTOPIA Serializer
TXC-05860

TECHNICAL OVERVIEW
PRODUCT PREVIEW

FEATURES

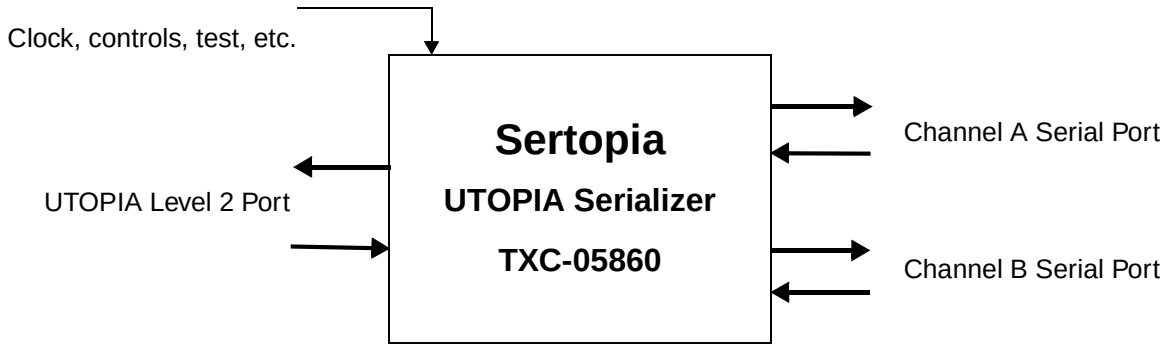
- UTOPIA Level 2, UTOPIA 2P, and POS-PHY operating modes for cell and packet traffic
- One UTOPIA port (800 Mbit/s)
- Two serial ports (channels A and B, one for primary and the other for redundant, with each at 1.25 Gbit/s)
- Backward compatible with UTOPIA Level 1
- UTOPIA port configurable as master or slave
- Up to 32 UTOPIA PHY addresses supported
- Configurable cell size of 52 to 64 bytes
- Configurable packet chunk size of 16, 48, or 64 bytes in UTOPIA 2P mode
- Transparent backpressure mechanism to avoid cell or packet loss
- Operation with a single 125 MHz reference clock
- CRC generation on transmit and verification on receive
- On-line and off-line loopback modes for serial and UTOPIA ports
- In-band configuration and status report
- Built in self test (BIST)
- Interoperable with CUBIT®-3 (TXC-05804), CUBIT®-622 (TXC-05805), ASPEN® (TXC-05810), AsTriX™ (TXC-05840), and standard UTOPIA level 2 interface devices
- Test Access Port for IEEE 1149.1 boundary scan
- +3.3 V and +1.8 V power supplies
- 196-lead Plastic Ball Grid Array package (PBGA), 15 mm x 15 mm

DESCRIPTION

The Sertopia™ (TXC-05860) UTOPIA serializer is a single-chip solution for broadband communication systems. A pair of Sertopia devices interface two remote UTOPIA ports transparently across a serial link. The Sertopia emulates a UTOPIA Level 2 master or UTOPIA Level 2 slave and contains a SERDES (serializer/deserializer) which transfers the cell or packet along with the UTOPIA port information. The Sertopia can emulate an ATM or PHY layer device on the UTOPIA bus. If backpressure for a given PHY is sensed on the UTOPIA port, the Sertopia conveys this backpressure (in-band) to the remote Sertopia, which holds traffic destined for that port until the backpressure is released. The Sertopia is also configurable through in-band signaling by a remote host controller. The Sertopia provides error check for all pass-through traffic in both directions. It discards any corrupted cells or packets without propagating errors. Instead, it reports error status to a remote host controller via internally generated signaling cells. The Sertopia enables UTOPIA Level 2 devices to communicate seamlessly across line cards, shelves, and racks without additional logic. Together with TranSwitch's CUBIT, ASPEN, and AsTriX family devices, and other standard UTOPIA devices, the Sertopia device can be used to create a cost effective point-to-point serial backplane-based access system.

APPLICATIONS

- Remote Access Concentrators
- Multi-service Access Systems
- Digital Cross Connect Systems
- DSLAM Applications
- Wireless Base Station Systems
- Routers
- Aggregation of multiple *CellBus* shelves



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LIST OF FIGURES

APPLICATION EXAMPLE

The application diagram in Figure 1 shows the usage of two Sertopia devices to extend a UTOPIA Interface.

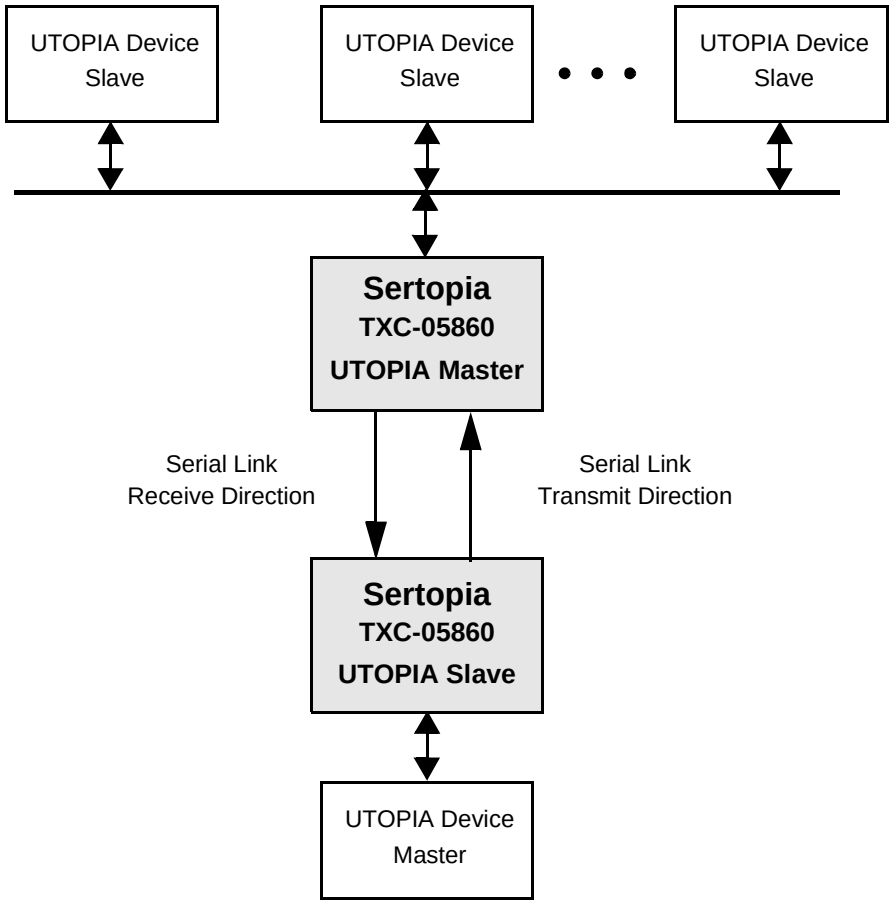


Figure 1. Application Using the Sertopia TXC-05860 to Extend a UTOPIA Interface

Port density is at the heart of driving costs down for service providers. Physical layout constraints limit the number of ports that can be connected to a single line card and the number of line cards that can be put in a single shelf. However, by providing the ability to extend the UTOPIA interface it is feasible to effectively extend the number of ports in the system, thereby increasing the port density of the system, as shown in Figure 1 above.

INTEROPERABILITY

The Sertopia works directly with the following TranSwitch devices:

- CUBIT-3 (TXC-05804)
- CUBIT-622 (TXC-05805)
- ASPEN (TXC-05810)
- AsTriX (TXC-05840)

FUNCTIONAL DESCRIPTION

A block diagram of the Sertopia device is shown in Figure 2. Further information on device operation and the interfaces to external circuits is provided below.

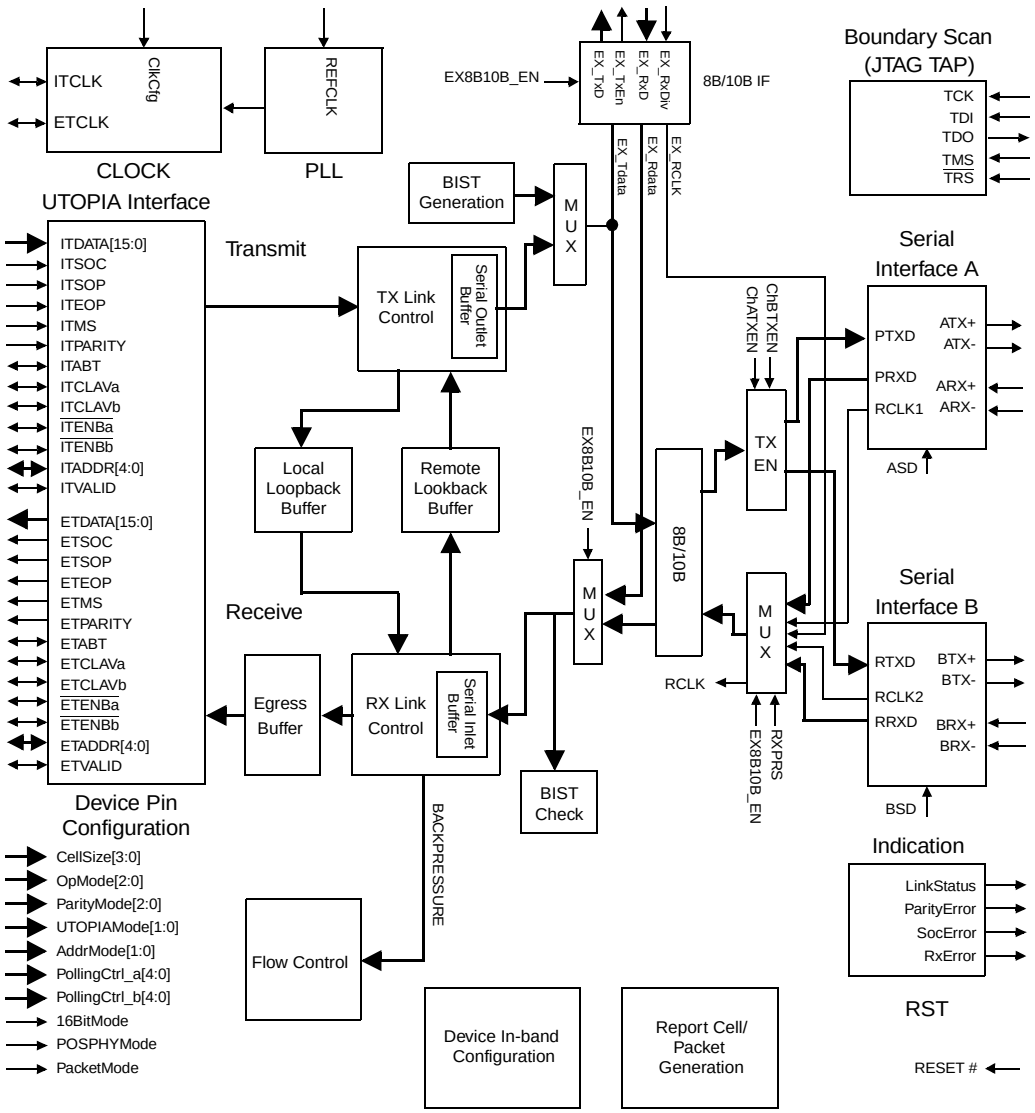


Figure 2. Sertopia TXC-05860 Block Diagram

The UTOPIA interface has two data paths, one in the transmit direction (from the UTOPIA interface to the serial interface) and the other in the receive direction (from the serial interface to the UTOPIA interface). In the transmit direction, data received by the UTOPIA interface is written into the Serial Outlet Buffer, and then is transmitted to 8B/10B encoder and SerDes under the control of the TX Link Control module. In the receive direction, data coming from the serial interface is processed and sent to the Serial Inlet Buffer. The RX Link Control module classifies and transfers data from the Serial Inlet Buffer to the Egress Buffer. Data in the Egress Buffer is sent out by the UTOPIA interface.

The TX/RX Link Control modules and the Flow Control module guarantee reliable data transmission across the serial interface. The Device In-Band Configuration module provides an interface for power-on and on-the-fly configuration. It sets an interface mode between cell, packet or POS-PHY operations, PHY addressing scheme, PHY address range, cell/chunk size, etc. The Local and Remote Loopback Buffers allow non-disruptive loopback, without interfering with normal traffic. The Clock and PLL blocks generate ITCLK and ETCLK, allowing the Sertopia to be a clock source for the UTOPIA interface, when in UTOPIA master mode. The 8B/10B interface block is used to support a third party SerDes transceiver or optical fiber transceiver. The RST module controls device reset and the JTAG module provides boundary scan for Sertopia. The Indication module provides device status indications.

UTOPIA INTERFACE CONFIGURATION

The Sertopia's UTOPIA Interface can be configured for either Cell Mode or Packet Mode. It supports standard UTOPIA 2 for cell mode and either UTOPIA 2P or POS-PHY for packet mode.

In UTOPIA Cell Mode, the Sertopia device supports the following configurations:

- UTOPIA Master/Slave
- UTOPIA 8-bit Mode/16-bit Mode
- UTOPIA Single-PHY/Multi-PHY
- Programmable Cell Size from 52 bytes to 64 bytes
- Addressing mode (single or dual group)
- Address range (0 - 30 for single address group mode or 0 - 15 for dual address group mode. The start address is always 0)

In UTOPIA Packet Mode, the Sertopia device supports the following configurations:

- UTOPIA 2P Packet Mode/POS-PHY Packet Mode
- UTOPIA Master/Slave
- UTOPIA Single-PHY/Multi-PHY
- Programmable Chunk Sizes of 16, 48, or 64 bytes
- Addressing mode (single or dual group)
- Address range (0 - 30 for single address group mode or 0 - 15 for dual address group mode. The start address is always 0)

  Only 16-bit mode is supported under the packet mode.

UTOPIA ADDRESS CONFIGURATION

The Sertopia device can be configured to support single address group mode or dual address group mode. In the single address group mode, only the ITCLAVa/ITENBa and ETCLAVa/ETENBa leads are used and they are associated with the 31 UTOPIA transmit addresses and 31 UTOPIA receive addresses. Each UTOPIA address corresponds to a PHY address, as shown in the following table.

UTOPIA address	PHY address
0	0
1	1
...	...
30	30

In the dual address group mode, two pairs of ITCLAV/ITENB and ETCLAV/ETENB leads are used to support two groups of PHY addresses. Each group includes 16 PHY addresses, and two PHY address groups are associated with the same UTOPIA addresses. ITCLAVa/ITENBa and ETCLAVa/ETENBa are associated with the PHY address group A, while ITCLAVb/ITENBb and ETCLAVb/ETENBb are associated with the PHY address group B. Each UTOPIA address corresponds to two PHY addresses, which belong to different PHY address groups. The UTOPIA address range is from 0 to 15 in the dual address group mode. The following table shows the address arrangement for the dual address group mode.

UTOPIA address	PHY address group	PHY address
0	A	0
1		1
...		...
15		15
0	B	16
1		17
...		...
15		31

UTOPIA Address Translation

Normally, a pair of Sertopia devices are configured similarly. However, some applications require different address group configurations. One Sertopia can be configured in the single address group mode and the other in the dual address group mode. In that case, the UTOPIA addresses need to be translated when messages are transferred from one device to the other.

The address group mode information can be derived from the CLAV signal fields carried in the overhead of each cell transmitted between a pair of Sertopia devices. The Sertopia device automatically detects if it needs to perform address translation when a cell is received from the serial interface. If address translation is required, the translation is performed before the cell moves onto the Serial Inlet Buffer. Figure 3 shows the UTOPIA address translation between the single address group mode and the dual address group mode.

Single Address Group Mode	Dual Address Group Mode	
UTOPIA Address	Group	UTOPIA Address
0-15	a	0-15
16-30*	b	0-14*

Note: *UTOPIA address 31 is reserved by the UTOPIA standard.

Figure 3. UTOPIA Address Relationship Between Single and Dual Address Group Modes

OTHER INTERFACES

Boundary Scan (Test Access) Port

The test interface includes a five-lead Test Access Port (TAP) as the boundary scan port that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external input/output leads from the TAP for board and component test.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (I/O)	$V_{DD3.3}$	-0.3	+3.6	V	Notes 1, 4
Supply voltage (Core)	$V_{DD1.8}$	-0.3	+2.1	V	Notes 1, 4
Analog supply voltage (PLL)	V_{DDA}	-0.3	+2.1	V	Notes 1, 4
DC input voltage	V_{IN}	-0.5	$V_{DD3.3}$ + 0.3	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-Up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.8 V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		35		°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

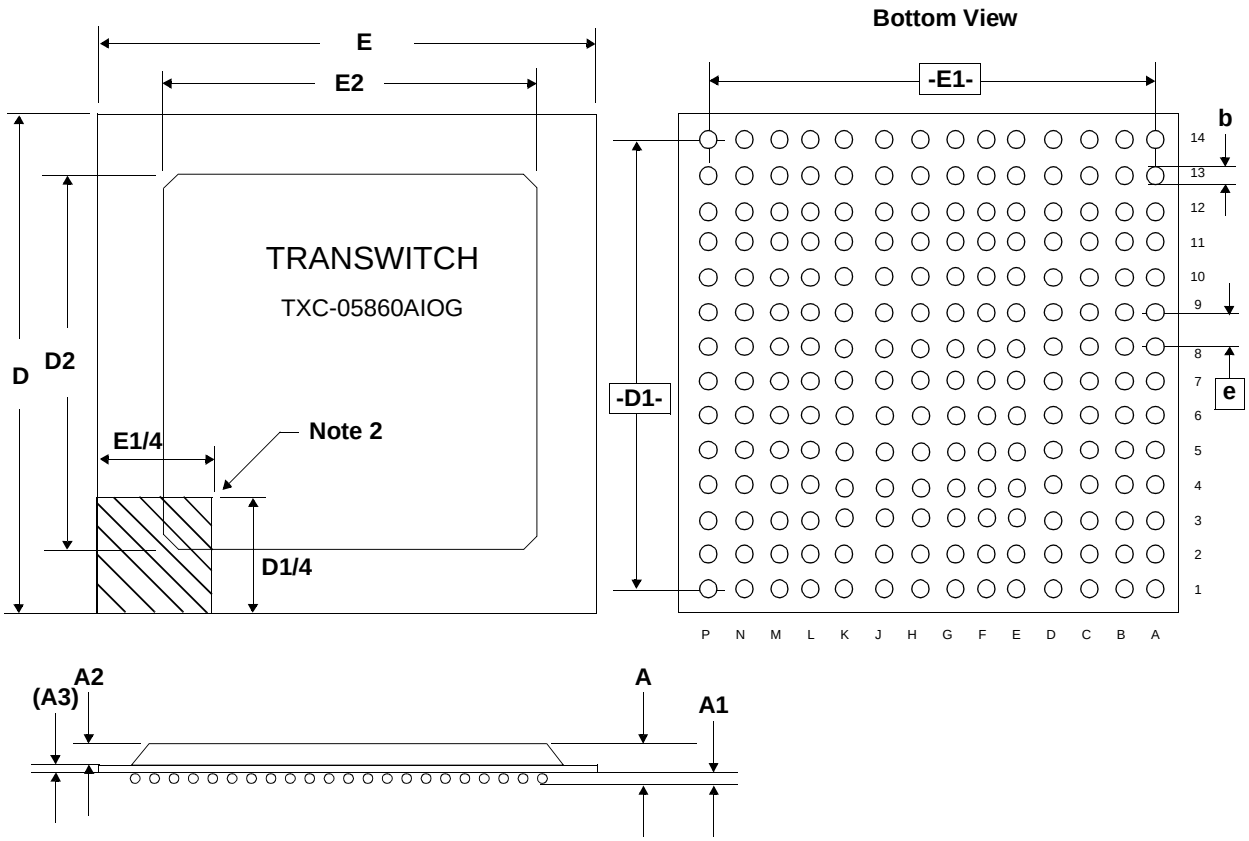
Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{DD3.3}$	3.15	3.3	3.45	V	
$I_{DD3.3}$			TBD	mA	See Notes 1 and 2
$P_{DD3.3}$			TBD	W	See Notes 1 and 2
$V_{DD1.8}$, V_{DDA}	1.71	1.8	1.89	V	
$I_{DD1.8}$			TBD	mA	See Notes 1 and 2
$P_{DD1.8}$			TBD	W	See Notes 1 and 2
I_{DDA}			TBD	mA	See Notes 1 and 2
P_{DDA}			TBD	W	See Notes 1 and 2

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

PACKAGE INFORMATION

The Sertopia device is packaged in a 196-lead Plastic Ball Grid Array (PBGA) package suitable for surface mounting, as illustrated in Figure 4.



Dimension (Note 1)	Min	Max
A A1 A2	1.55 0.30 0.75	1.97 0.50 0.85
A3 (Ref.)	0.56	
b	0.40	0.60
D (Nom)	15.00	
D1 (Nom)	13.00	
D2	12.95	13.70
E (Nom)	15.00	
E1 (Nom)	13.00	
E2	12.95	13.70
e (Ref.)	1.00	

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 14 x 14, JEDEC code MS-034A.

Figure 4. Sertopia TXC-05860 196-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-05860AIOG 196-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

Figure 1 illustrates a typical application of the Sertopia device to extend a UTOPIA interface. The other related TranSwitch devices are briefly described below:

TXC-05804, CUBIT-3 VLSI Device (Multi-PHY *CellBus* Bus Switch Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 or other *CellBus*-compatible devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05805, CUBIT-622 VLSI Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements are a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO has been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-05810, ASPEN Device (*CellBus* Access Processor Device). ASPEN supports *CellBus* operation in both cell and packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or, alternatively, to provide greater system throughput. Line interface is via UTOPIA 1 or 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables, is stored in an external synchronous SRAM.

TXC-05840, AsTriX Device (*CellBus* Expansion Switch Device). The AsTriX is designed to allow higher *CellBus* system throughput by concatenating multiple *CellBus* strands through a switch. It is capable of 8 x 8 switching of 800 Mbit/s per port. The AsTriX ports support UTOPIA Level 2 interfaces. The switch is non-blocking, incorporating a backpressure mechanism for eliminating congestion towards any one port.

REFERENCE DOCUMENTS

- The ATM Forum: UTOPIA Specification Level 1, Version 2.0.1, March 1994.
- The ATM Forum: UTOPIA Specification Level 2, Version 1.0, June 1995.
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture, May 1990.

- NOTES -

PRODUCT PREVIEW

- NOTES -

PRODUCT PREVIEW

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