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COMPARATOR WITH OUTPUT VOLTAGE-LEVEL TRANSLATION

FEATURES

- Low Supply Current: 8 μA (Max)
- Supply Voltage: 2.5 V to 5.5 V
- Output FET Provides Down Translation
- Small Package: SOT-563
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance
 - 2500-V Human-Body Model (JESD-A114E)
 - 250-V Machine Model (EIA/JESD A115-A)
 - 1500-V Charged-Device Model (JESD22-C101-A Level III)

DESCRIPTION/ORDERING INFORMATION



The TXS03121 is a comparator designed for battery monitoring applications. It can be operated with a voltage of 2.5 V to 5.5 V. The reference voltage is applied to the –IN terminal, whereas the voltage to be monitored is connected to +IN. When the voltage at +IN is greater than the voltage at –IN, the output FET is turned On. When the voltage at +IN is less than the voltage at –IN, the output FET is turned Off. The source (S) of the output FET can be connected to 1.1 V to 3.6 V, which allows the output signal to be level translated to another voltage value. The voltage at V₊ must be greater than or equal to the voltage at S. The voltage at S must be greater than or equal to the voltage at D (V₊ \ge V_S \ge V_D).

ORDERING INFORMATION

T _A	PACKA	GE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 85°C	SOT-563 – DRL	Tape and reel	TXS03121DRLR	2FR		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PIN ASSIGNMENTS

NO.	NAME	DESCRIPTION
1	V+	Comparator supply voltage
2	+IN	Comparator positive input
3	–IN	Comparator negative input
4	GND	Ground
5	D	Drain of output FET
6	S	Source of output FET

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V+	Supply voltage range ⁽²⁾		-0.5	6.5	V
+IN, –IN	Input voltage range		-0.5	6.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	O Continuous output current (On-state switch current)				mA
	Continuous current through V ₊ or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DRL package		171.6	°C/W
T _{stg}	Storage temperature range			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V+	Comparator supply voltage	2.5	5.5	V
V _S , V _D ⁽¹⁾	Output FET source or drain voltage	1.1	3.6	V
T _A	Operating free-air temperature	-40	85	°C

(1) V_+ must be greater than or equal to V_S , and V_S must be greater than or equal to V_D ($V_+ \ge V_S \ge V_D$).

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COMPARATOR ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage		$V_{CM} = 0.8 V, I_{O} = 0$	10	0.5	10	m\/
		V ₊ = 2.5 V 10 5.5 V	$V_{CM} = V_+, \ I_O = 0$	-10	0.5	10	IIIV
V_{CM}	Common-mode voltage range	$V_{+} = 2.5 \text{ V to } 5.5 \text{ V}$	0.8		V ₊	V	
I _{+IN}	Input lookogo ourrent		$V_{+IN} = 0 V \text{ to } V_+$			0.5	۸
I_IN	Input leakage current	v ₊ = 2.5 v to 5.5 v	$V_{-IN} = 0 V \text{ to } V_+$			0.5	μΑ
I+	+ Supply current $V_+ = 2.5 V$ to 5.5 V					8	μA
C _{IN}	Capacitance of +IN, -IN pins				2	2.5	pF



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OUTPUT FET ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER TEST CONDITIONS						MAX	UNIT
I _{DS(ON)}	On leakage current	$V_{\rm S}$ = 1.1 V to 3.6 V,			0.5	μΑ		
I _{DS(OFF)}	Off leakage current	$V_{\rm S}$ = 1.1 V to 3.6 V,			0.5	μA		
C _(ON)	On capacitance		4	5.1	6	pF		
C _(OFF)	Off capacitance, S and D terminals				1.5	3.4	5	pF
On resistance of output		V _S = 1.1 V						
				V _S = 1.4 V			65	
r _{ON}	r _{ON} On resistance of output	$V_+ \ge V_S, I_D = -100 \ \mu$	A	V _S = 1.65 V			61	Ω
			$V_{S} = 2.3 V$			50		
			$V_{S} = 3 V$			44		
				V ₊ = 4.5 V			1.7	
	20 m)/ exercisive	$v_{-IN} = 0.6 v, v_{S} = 1.05 v$	V ₊ = 3 V			3.9		
		20-mv overdrive		V ₊ = 4.5 V			1	
			$v_{-IN} = v_{+}, v_{S} = 1.05 v$	V ₊ = 3 V			3.9	
. Eachtair				V ₊ = 4.5 V			1.2	
			$V_{-IN} = 0.8 V, V_S = 1.65 V$	V ₊ = 3 V			2.7	
		50-mV overdrive		V ₊ = 2.5 V			6.2	- μs
	Eachla Cara			V ₊ = 4.5 V			1	
τ _{EN}	Enable time		V _{-IN} = V ₊ , V _S = 1.65 V	V ₊ = 3 V			2.4	
				V ₊ = 2.5 V			5.3	
		100-mV overdrive	V _{-IN} = 0.8 V, V _S = 1.65 V	V ₊ = 4.5 V			0.8	
				V ₊ = 3 V			1.4	-
				V ₊ = 2.5 V			5	
				V ₊ = 4.5 V			0.7	
			V _{-IN} = V ₊ , V _S = 1.65 V	V ₊ = 3 V			1.3	
				V ₊ = 2.5 V			4.7	
				V ₊ = 4.5 V			4.4	
			$V_{-IN} = 0.8 V, V_{S} = 1.65 V$	V ₊ = 3 V			12	
		20-mV overdrive		V ₊ = 4.5 V			3.5	
			$V_{-IN} = V_{+}, V_{S} = 1.65 V$	V ₊ = 3 V			6.1	
				V ₊ = 4.5 V			4.1	
			$V_{-IN} = 0.8 V, V_{S} = 1.65 V$	V ₊ = 3 V			9.6	
				V ₊ = 2.5 V			5.3	
	Diachta tima	50-mv overdrive		V ₊ = 4.5 V			2.5	
tDIS	Disable time		$V_{-IN} = V_+, V_S = 1.65 V$	V ₊ = 3 V			3.2	μs
				V ₊ = 2.5 V			5.2	1
				V ₊ = 4.5 V			4.6	
			$V_{-IN} = 0.8 V, V_{S} = 1.65 V$	V ₊ = 3 V			6.7	1
		100 mV avardrive		V ₊ = 2.5 V			5.2	
		100-mV overdrive		V ₊ = 4.5 V			1.9	
			$V_{-IN} = V_+, V_S = 1.65 V$	V ₊ = 3 V			2.8	
				V ₊ = 2.3 V			4.9	

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PARAMETER MEASUREMENT INFORMATION





10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS03121DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2FR	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nomin	al
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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS03121DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS03121DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0

DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side. 4. Reference JEDEC registration MO-293 Variation UAAD



DRL0006A

EXAMPLE BOARD LAYOUT

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DRL0006A

EXAMPLE STENCIL DESIGN

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.



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