

n-channel JFETs designed for . . .



U1897E U1898E U1899E

Performance Curves NC
See Section 4

- Analog Switches
- Choppers
- Commutators

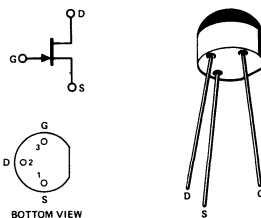
BENEFITS

- Low Insertion Loss
 $R_{DS(on)} < 30 \Omega$ (U1897E)
- No Error or Offset Voltage Generated by Closed Switch
Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage-40 V
Forward Gate Current 10 mA
Total Continuous Device Dissipation at (or Below) $T_A = 25^\circ\text{C}$ (Derate 3.5 mW/°C to 125°C) 350 mW
Storage Temperature Range-55 to +125°C
Operating Temperature Range-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic	U1897E		U1898E		U1899E		Unit	Test Conditions																								
		Min	Max	Min	Max	Min	Max																										
S T A T I C	BV _{GS} Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$																								
	BV _{DGO} Drain-Gate Breakdown Voltage	40		40		40			$I_G = -1 \mu\text{A}, I_S = 0$																								
	BV _{SGO} Source-Gate Breakdown Voltage	40		40		40			$I_G = -1 \mu\text{A}, I_D = 0$																								
	I _{GSS} Gate Reverse Current		-400		-400		-400	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$																								
	I _{DGO} Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20 \text{ V}, I_S = 0$																								
	I _{SGO} Source-Gate Leakage Current		200		200		200		$V_{SG} = 20 \text{ V}, I_D = 0$																								
	I _{D(off)} Drain Cutoff Current		200		200		200		$V_{DS} = 20 \text{ V}, V_{GS} = -12 \text{ V}$ (U1897E) $V_{GS} = -8 \text{ V}$ (U1898E) $V_{GS} = -6 \text{ V}$ (U1899E) $T_A = 85^\circ\text{C}$																								
	D Y N A M I C	V _{GS(off)} Gate-Source Cutoff Voltage	-5.0	-10	-2.0	-7.0	-1.0	-5.0	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$																							
		I _{DSS} Saturation Drain Current (Note 1)	30		15		8.0			mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$																						
V _{DS(on)} Drain-Source ON Voltage			0.2		0.2		0.2	V	$V_{GS} = 0, I_D = 6.6 \text{ mA}$ (U1897E) $I_D = 4.0 \text{ mA}$ (U1898E), $I_D = 2.5 \text{ mA}$ (U1899E)																								
r _{DS(on)} Static Drain-Source ON Resistance			30		50		80		$I_D = 1 \text{ mA}, V_{GS} = 0$																								
C _{DG} Drain-Gate Capacitance			5		5		5		pF	$V_{DG} = 20 \text{ V}, I_S = 0$																							
C _{SG} Source-Gate Capacitance			5		5		5	$V_{SG} = 20 \text{ V}, I_D = 0$																									
C _{iss} Common-Source Input Capacitance			16		16		16	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ f = 1 MHz																									
C _{rss} Common-Source Reverse Transfer Capacitance			3.5		3.5		3.5																										
M I C		t _{d(on)} Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions																							
	t _r Rise Time		10		20		40	<table border="0"> <tr> <td></td> <td>U1897E</td> <td>U1898E</td> <td>U1899E</td> </tr> <tr> <td>V_{DD}</td> <td>3 V</td> <td>3 V</td> <td>3 V</td> </tr> <tr> <td>V_{GS(on)}</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>V_{GS(off)}</td> <td>-12 V</td> <td>-8 V</td> <td>-6 V</td> </tr> <tr> <td>R_L</td> <td>430 Ω</td> <td>700 Ω</td> <td>1100 Ω</td> </tr> <tr> <td>I_{D(on)}</td> <td>6.6 mA</td> <td>4 mA</td> <td>2.5 mA</td> </tr> </table>			U1897E	U1898E	U1899E	V _{DD}	3 V	3 V	3 V	V _{GS(on)}	0	0	0	V _{GS(off)}	-12 V	-8 V	-6 V	R _L	430 Ω	700 Ω	1100 Ω	I _{D(on)}	6.6 mA	4 mA	2.5 mA
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t _{off} Turn OFF Time		40		60		80																											

NOTE:

1. Pulse test pulsewidth = 300 μs; duty cycle ≤ 3%.

NC

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