Frequency Synthesizer

Description

The programmable frequency synthesizer IC U2781B for µP-controlled applications is realized with Atmel Wireless & Microcontrollers' advanced UHF process which is very suitable for combinations of fast ECL logic and low-current I^2L logic. The benefits are high input sensitivity combined with low power consumption and therefore small packages (SSO20). This makes the device a perfect choice for cordless phones and handheld cellular radio sets up to 1.1 GHz.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Very low current consumption (typ. 3 V/ 5 mA)
- Supply-voltage range: 2.7 to 5.5 V
- Max. input frequency: 1.1 GHz
- Programmable prescaler 64/ 65 or 128/ 129
- Controlled by 3-wire bus with f_{clock} up to 500 kHz
- Status output for PLL lock/ unlock condition
- Very fast phase detector
- SSO20 package
- ESD protection in accordance with MIL-STD. 883 method 3015 class 2

Benefits

- Very low current consumption extends talk time
- Few external components and SSO package save costs and space

Block Diagram

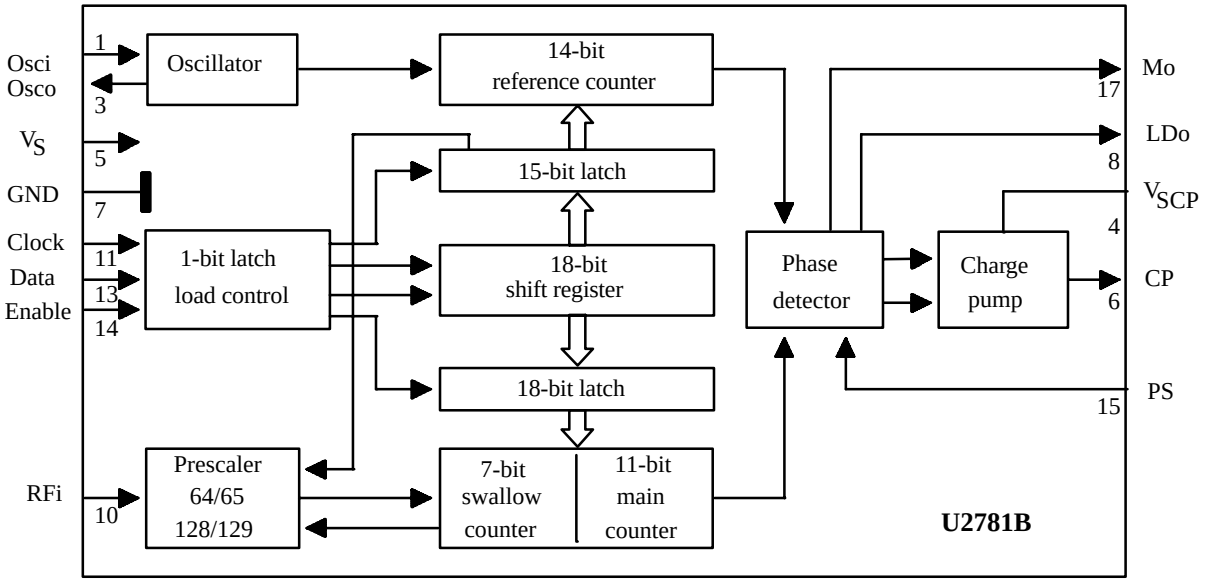


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2781B-MFS	SS020	Tube, MOQ 830 pcs
U2781B-MFSG3	SS020	Taped and reeled, MOQ 4000 pcs

Functional Description

The IC is controlled by a 3-wire bus with Clock, Data and Enable inputs for programming the scaling factors of the programmable counter, the reference counter and the prescaler.

A TCXO can be connected to the oscillator input (OSCi) as an alternative solution to the common crystal reference oscillator. In that case, the oscillator output (OSCo) should be left open.

The charge-pump output operates as switched current sources. The characteristics of the phase-locked loop can be determinated by the external lowpass filter.

The phase characteristic of the phase detector is convertible and thus matchable to different frequency/ tuning voltage characteristics.

Pin Description

Pin	Symbol	Function
1	Osci	Oscillator input
2	n.c.	Not connected
3	Osco	Oscillator output
4	V_{SCP}	Charge-pump supply voltage
5	V_s	Supply voltage
6	CP	Charge-pump output
7	GND	Ground
8	LDo	Lock-detector output
9	n.c.	Not connected
10	RFi	VCO input
11	Clock	3-wire bus Clock
12	n.c.	Not connected
13	Data	3-wire bus Data
14	Enable	3-wire bus Enable
15	PS	Phase select input
16	n.c.	Not connected
17	Mo	Monitor output for f_p and f_r
18	n.c.	Not connected
19	n.c.	Not connected
20	n.c.	Not connected

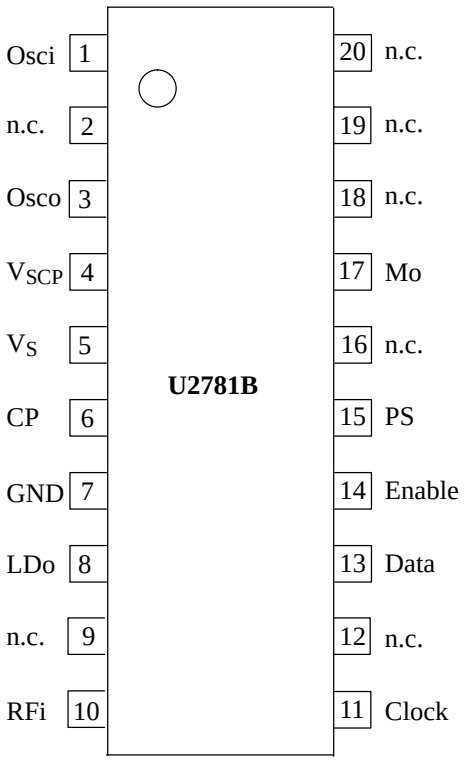


Figure 2. Pinning SSO20

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_S	– 0.3 to 6	V
RF input	V_{RF}	V_S	V
Oscillator input voltage	V_{Osci}	1	V
Oscillator output voltage	V_{Osco}	1.5	V
Bus input voltage	V_{BUS}	6	V
Phase-select input voltage	V_{PS}	6	V
Charge-pump input voltage	V_{SCP}	6	V
Storage temperature	T_{stg}	– 40 to 125	°C

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	V_S	2.7 to 5.5	V
Ambient temperature	T_{amb}	– 40 to 85	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

Electrical Characteristics

T_{amb} = 25°C, V_S = 2.7 to 5.5 V, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply voltage		V_s	2.7		5.5	V
Supply current	V_s = 3 V	I_s		5		mA
Supply voltage CP		V_{SCP}	V_s		5.5	V
Supply current CP	V_{CP} = 5 V, PLL in locked condition	I_{SCP}		1		µA
RF input						
Input voltage f_i = 200 to 1100 MHz	R_s = 50 Ω *) R_s = 50 Ω *)	V_{imin} V_{imax}		20 200		mV_{RMS} mV_{RMS}
Frequency range		f_{imin} f_{imax}	 1100	50 1250		MHz MHz
Scaling factor prescaler		S_{PSC}		64/128		
Scaling factors main counter		S_M	4		2047	

Electrical Characteristics (continued)

T_{amb} = 25°C, V_S = 2.7 to 5.5 V, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Scaling factors swallow counter		S_S	0		127	
Reference oscillator						
Input voltage	R_s = 50 Ω *) R_s = 50 Ω *)	V_{imin} V_{imax}		20 200		mV_{RMS} mV_{RMS}
Frequency range		f_{imin} f_{imax}		0,1 20		MHz MHz
Scaling factor reference counter		S_R	4		16383	
3-wire bus (Clock, Data, Enable) and PS						
High input voltage		V_{iH}	1.5	0.9		V
Low input voltage		V_{iL}	0		0.4	V
High input current		I_{iH}			5	µA
Low input current		I_{iL}	–5			µA
Monitor output (Emitter follower)						
High output voltage	V_s = 3 V	V_{iH}	2.1	2.2		V
Low output voltage	I_{MO} = 0.5 mA	V_{iL}		1.8	1.9	V
Charge-pump output						
Source current	V_{CP} = 5 V	I_{source}		–1		mA
Sink current		I_{sink}		1		mA
Leakage current	V_{CP} = 5 V	I_{leak}		±5		nA
Lock-detector output (open collector)						
Saturation voltage	I_{LD} = 0.2 mA	V_{sat}		0.2	0.4	V
Leakage current	V_{LD} = 5 V	I_{leak}			2	mA

*) RMS voltage at 50 W

Functional Description

The reference- and the programmable counter can be programmed by the 3-wire bus (Clock, Data and Enable). The Data Signal is transferred bit by bit into the shift register during the rising edge, starting with the MSB-bit. As soon as the enable signal is in high condition, the content of the shift register will be taken over either into the 15-bit reference counter latch (C = H) or into the 18-bit latch of the programmable counter (C = L)

Reference Counter (15-bit shift register)

LSB															MSB
C	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	PSC

C: Control bit High
PSC: Prescaler scaling factor bit: High – 64/65
Low – 128/129
S_{PSC} = 64 or 128
R0 to R13: These bits are setting the reference counter S_R
$S_R = R0 \square 2^0 + R1 \square 2^1 + to + R12 \square 2^{12} + R13 \square 2^{13}$
permitted scaling factors for S_R: 4 to 16383

Programmable Counter (18-bit shift register)

LSB																		MSB
C	S0	S1	S2	S3	S4	S5	S6	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10

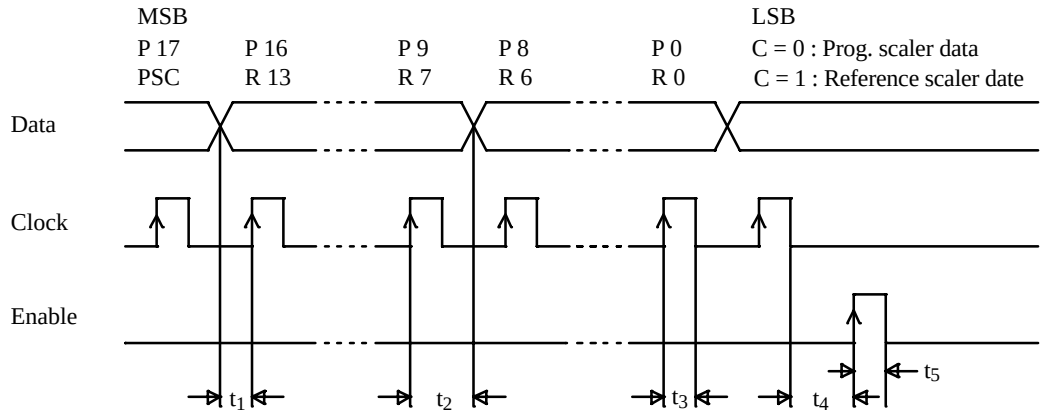
C: Control bit Low
S0 to S6: These bits are setting the swallow counter S_S.
$S_S = S0 \square 2^0 + S1 \square 2^1 + to + S5 \square 2^5 + S6 \square 2^6$
permitted scaling factors for S_S: 0 to 127, $S_S < S_M$
M0 to M10 : These bits are setting the main counter S_M.
$S_M = M0 \square 2^0 + M1 \square 2^1 + to + M9 \square 2^9 + M10 \square 2^{10}$
permitted scaling factors for S_M: 4 to 2047

Total scaling factor S_P of the programmable counter
$S_P = (S_{PSC} \square S_M) + S_S$ Condition: $S_S < S_M$

VCO Frequency

$$f_{VCO} = ((S_{PSC} \square S_M) + S_S) \square f_{RefOsc} / S_R$$

Timing 3-Wire Bus



All times t_1 to t_5 > 1 ms

Figure 3. Timing 3–wire bus

Phase-Detector Polarity

The polarity of the phase detector can be changed by the PS input. Depending on the PS input level, the charge-pump current will also be inverted. The monitor output signal MO (emitter follower output with ECL level) will be switched over from f_P to f_R simultaneously.

	PS = High or Open		PS = Low	
	CP	MO	CP	MO
$f_R > f_P$	I_{sink}	f_R	I_{source}	f_P
$f_R < f_P$	I_{source}	f_R	I_{sink}	f_P
$f_R = f_P$	0	f_R	0	f_P

Depending on the VCO frequency versus tuning voltage characteristic, the PS input has to be programmed as follows:

For increasing tuning voltage and increasing frequency: PS = High or open
decreasing frequency: PS = Low.

Pulse Diagram Phase and Lock Detector

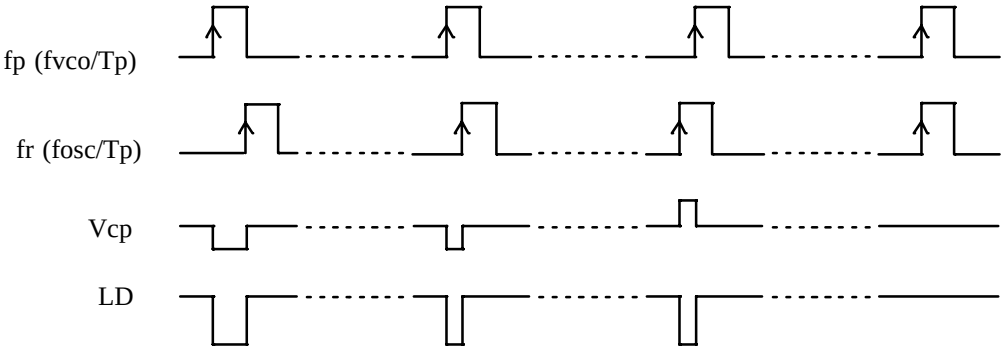


Figure 4. Pulse diagram phase and lock detector

The LD output is in unlocked condition at low level and the pulsewidth is in reference to the phase respectively frequency difference at the phase detector. If the phase detector output pulses are smaller than 100 ns, the LD output changes to high and indicates “lock” condition.

Test Circuit

Input sensitivity

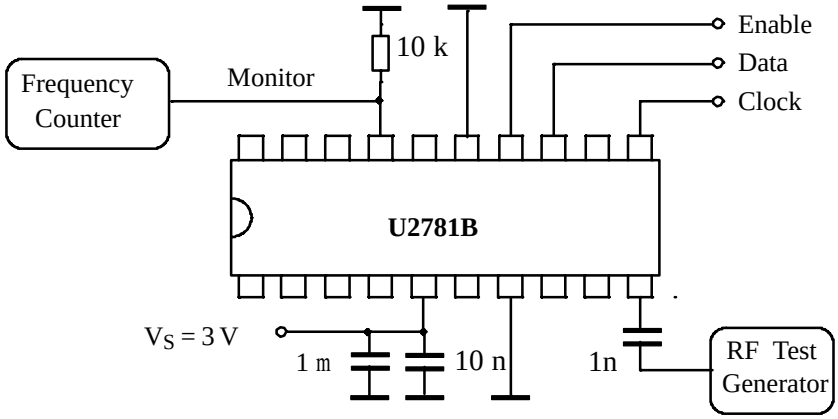


Figure 5. Test circuit

Typical Input Sensitivity

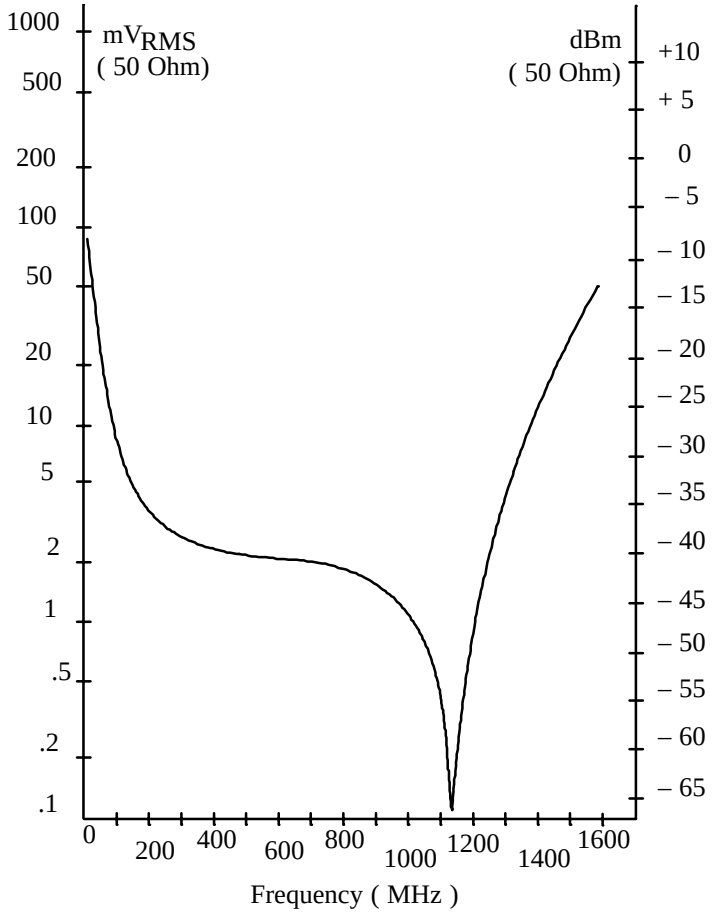


Figure 6. Typical input sensitivity

Application Circuit

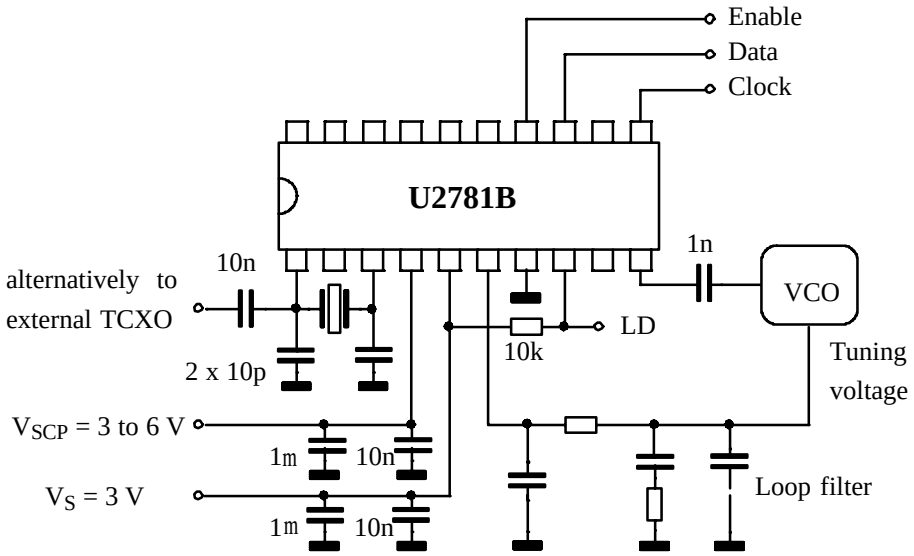


Figure 7. Application circuit

Input Impedance

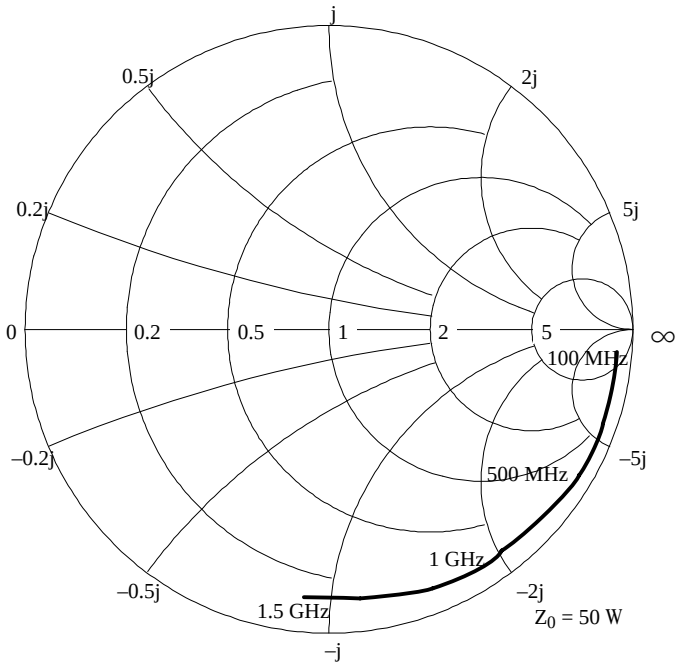
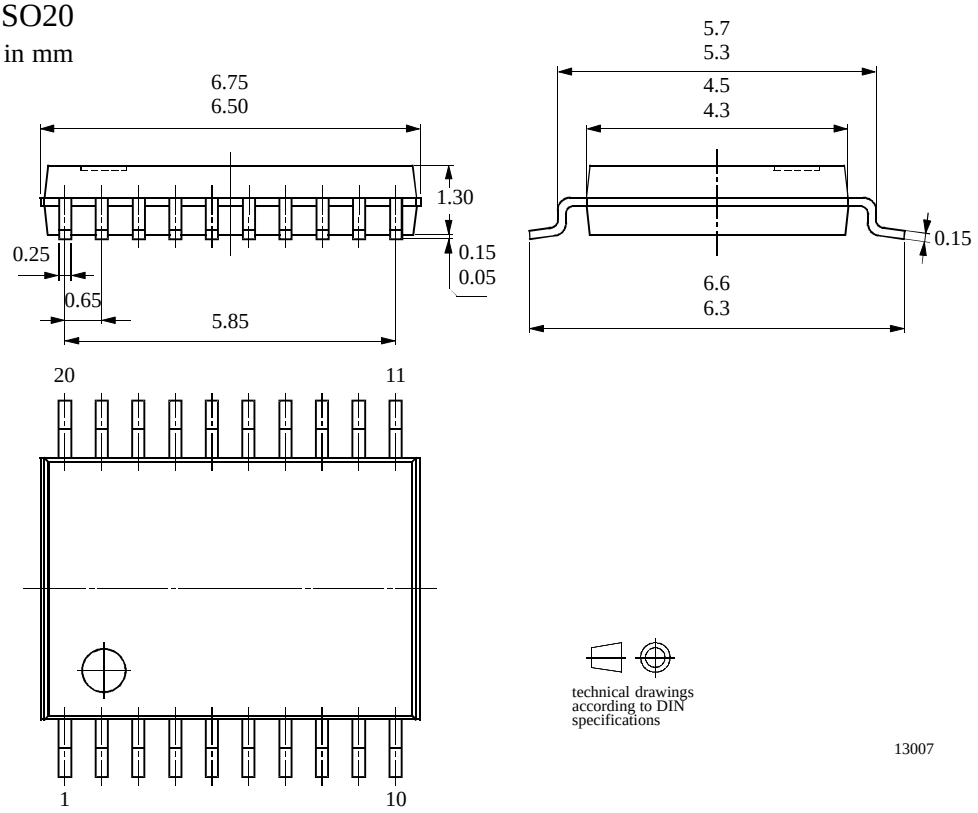


Figure 8. Input impedance

Package Information

Package SSO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.atmel–wm.com

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