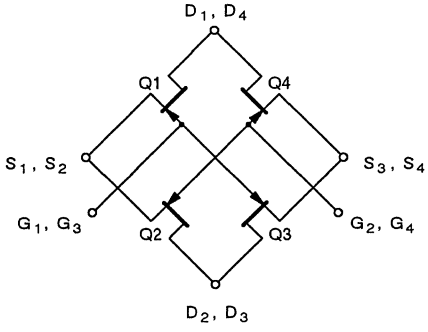
U350

Siliconix incorporated

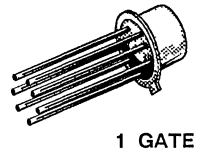
N-Channel JFET Ring Demodulator

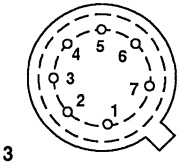
The U350 is a set of four matched n-channel JFETs connected as a ring demodulator. The matched set of JFETs has low $r_{DS(ON)}$, high g_{fs}, and square law operation which gives high conversion gain and a very high intermodulation intercept point. Best device performance is in the HF-VHF frequency range. The hermetic TO-99 package shields the die set as well as lending itself to military processing.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{GSS} MAX (nA)	NF TYP (dB)
U350	-25	10	-1	7



TO-99 (TO-78) BOTTOM VIEW





1 GATE 1, GATE 3
2 DRAIN 1, DRAIN 4
3 SOURCE 1, SOURCE 2
4 GND & CASE
5 SOURCE 3, SOURCE 4
6 DRAIN 2, DRAIN 3
7 GATE 2, GATE 4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Forward Gate Current	I_G	25	mA
Power Dissipation	P_D	1	W
Power Derating		8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				U350		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage[4]	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3	-2	-6	V
Saturation Drain Current[3, 4]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	45	24	60	mA
Gate Reverse Current[4]	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1	nA
		T_A = 125°C	-0.001		-1	µA
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7		1	V
DYNAMIC						
Common-Source Forward Transconductance[4]	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	15	10	18	mS
Common-Source Output Conductance[4]	g_{os}		100		150	µS
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1kHz	33		90	Ω
Common-Source Input Capacitance	C_{gs}	V_{GS} = -10 V, I_D = 0 mA, f = 1 MHz	4		5	pF
Common-Source Reverse Transfer Capacitance	C_{gd}	V_{GD} = -10 V, I_S = 0 mA, f = 1 MHz	2		2.5	pF
Conversion Gain	G_c	V_{DS} = 20 V, V_{GS} = ½$V_{GS(OFF)}$, f = 100 MHz, R_L = 1700 Ω, See Figure 1	4			dB
Noise Figure	NF		7			dB
Intercept Point			33			dBm
MATCHING						
Saturation Drain Current Ratio[3]	$\frac{I_{DSS}}{I_{DSS}}$	V_{DS} = 15 V, V_{GS} = 0 V	0.95	0.9	1	
Transconductance Ratio	$\frac{g_{fs}}{g_{fs}}$	V_{DS} = 15 V, I_D = 10 mA, f = 1 kHz	0.95	0.9	1	
Output Conductance Ratio	$\frac{g_{os}}{g_{os}}$		0.95	0.9	1	
Gate-Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)}}{V_{GS(OFF)}}$	V_{DS} = 15 V, I_D = 1 nA	0.95	0.9	1	

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Other gate terminal clamped to -8 V.

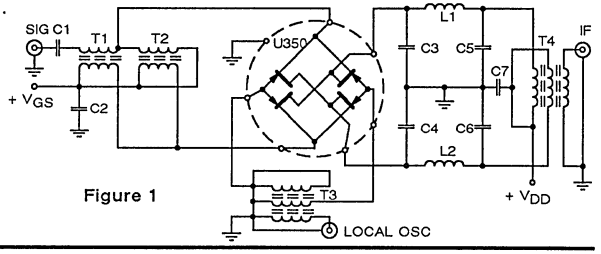


Figure 1

4