U401 SERIES

Siliconix incorporated

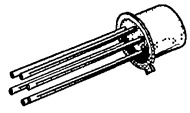
N-Channel JFETs

The U401 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The U401 Series has a wide selection of both offset and drift specifications with the prime device, the U401, featuring 5 mV offset and 10 μV/°C drift. The six devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

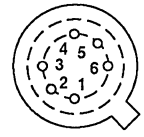
For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U401	-50	2	-15	5
U402	-50	2	-15	10
U403	-50	2	-15	10
U404	-50	2	-15	15
U405	-50	2	-15	20
U406	-50	2	-15	40

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order U40XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U401		U402		U403		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		-50		-50		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-25		-25		-25	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-15		-15		-15	pA
		T_A = 125°C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			5		10		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = -55 to 25°C			10		10		25	µV/°C
		T = 25 to 125°C			10		10		25	µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		95		95		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

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ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U404		U405		U406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V	−58	−50		−50		−50		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	−58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	−1.5	−0.5	−2.5	−0.5	−2.5	−0.5	−2.5	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −30 V, V_{DS} = 0 V	−2		−25		−25		−25	pA
		T_A = 125°C	−1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	−2		−15		−15		−15	pA
		T_A = 125°C	−0.8		−10		−10		−10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	−1		−2.3		−2.3		−2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			15		20		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = −55 to 25°C			25		40		80	µV/°C
		V_{DG} = 10 V, I_D = 200 µA, T = 25 to 125°C			25		40		80	µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		90				dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.