

Programmable Telephone Audio Processor

Description

The programmable telephone audio processor U4091BM is a linear integrated circuit for use in feature phones, answering machines and fax machines. It contains the speech circuit, tone-ringer interface with DC/DC converter, sidetone equivalent and ear-protection rectifiers. The circuit is line-powered and contains all components necessary for signal amplification and

adaptation to the line. The U4091BM can also be supplied via an external power supply. An integrated voice switch with loudspeaker amplifier enables hands-free or loudhearing operation. With an anti-feedback function, acoustical feedback during loudhearing can be reduced significantly. The generated supply voltage is suitable for a wide range of peripheral circuits.

Features

- Speech circuit with anti-clipping
- Tone-ringer interface with DC/DC converter
- Speaker amplifier with anti-distortion
- Power-supply management (regulated, unregulated) and a special supply for electret microphone
- Voice switch
- Interface for answering machine and cordless phone

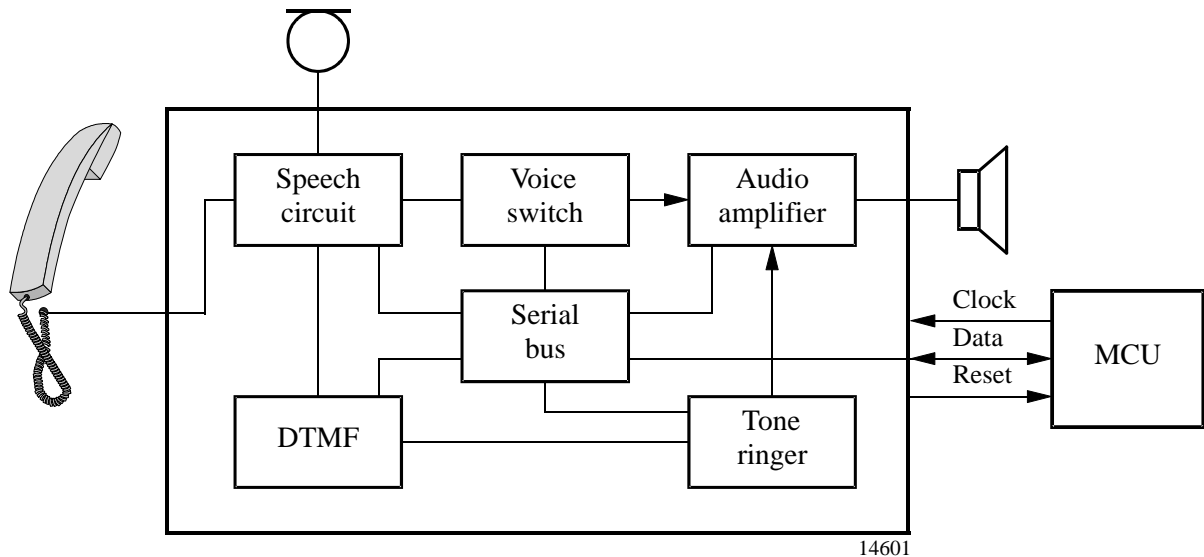
Benefits

- No piezoelectric transducer for tone ringing necessary
- Complete system integration of analog signal processing on one chip
- Very few external components

Applications

Feature phone, answering machine, fax machine, speaker phone, cordless phone

Block Diagram



Ordering Information

Extended Type Number	Package	Remarks
U4091BM-AFN	SSO44	
U4091BM-AFNG3	SSO44	Taped and reeled

Detailed Block Diagram

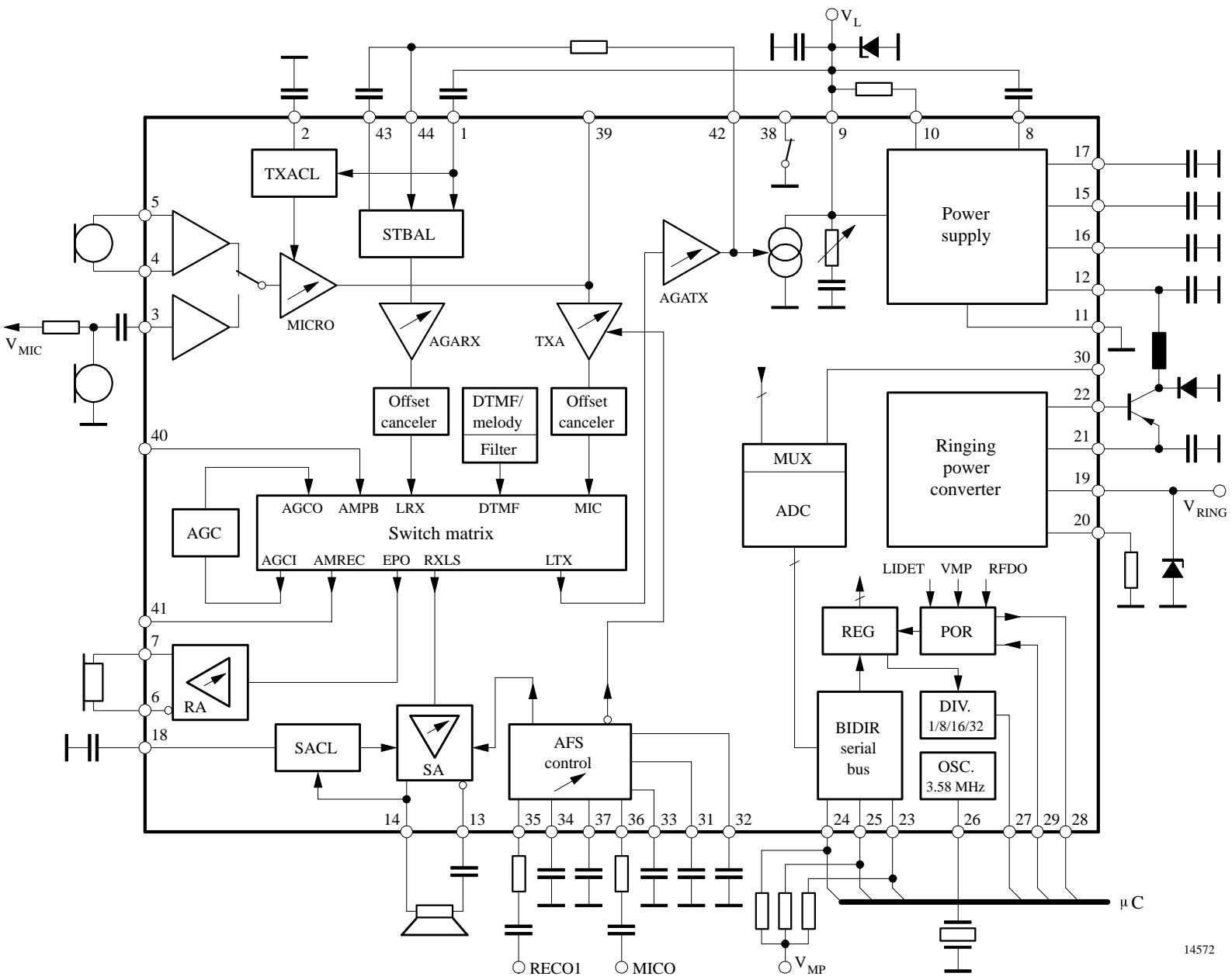


Figure 1. Detailed block diagram

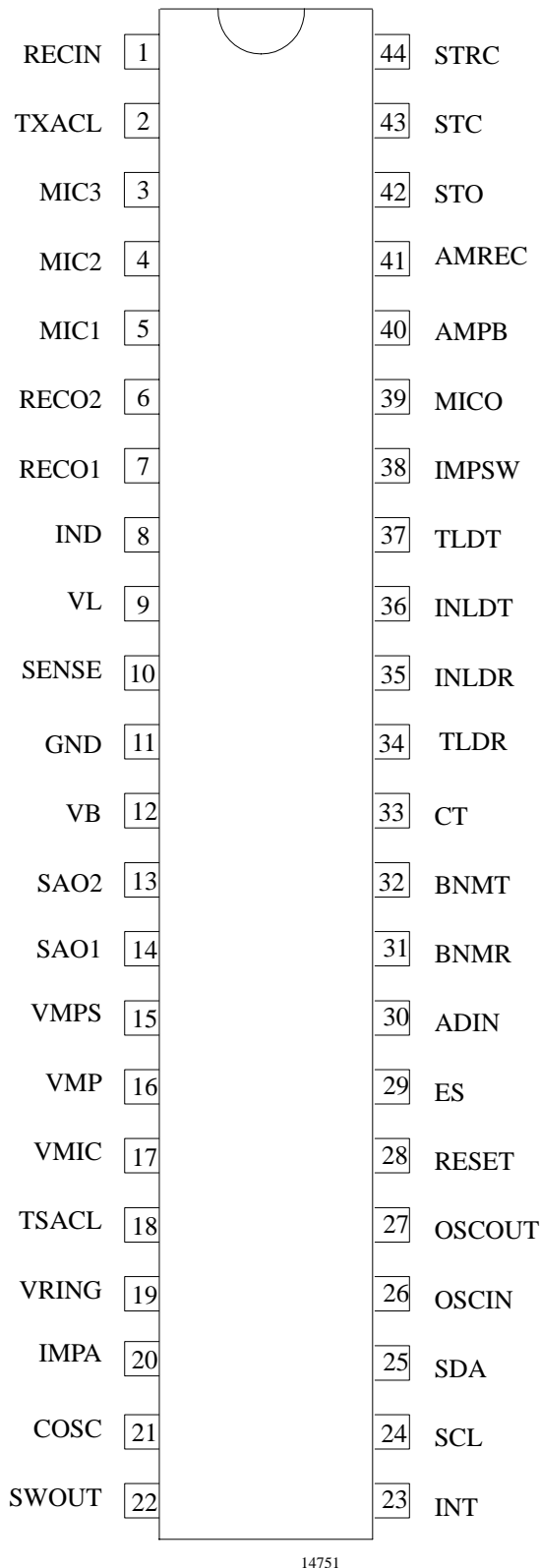
Target Specification

Pin Description

Pin	Symbol	Function
1	RECIN	Receive amplifier input
2	TXACL	Time-constant adjustment for transmit anti-clipping
3	MIC3	Microphone input for hands-free operation
4	MIC2	Input of symmetrical microphone amplifier with high common-mode rejection ratio
5	MIC1	Input of symmetrical microphone amplifier with high common-mode rejection ratio
6	RECO2	Output of the receive amplifier
7	RECO1	Output of the receive amplifier, also used for sidetone network
8	IND	The internal equivalent inductance of the circuit is proportional to the value of the capacitor at this pin. A resistor connected to ground may be used to adjust the DC mask.
9	VL	Positive supply-voltage input to the device in speech mode
10	SENSE	Input for sensing the available line current
11	GND	Ground, reference point for DC- and AC signals
12	VB	Unstabilized supply voltage for speech network
13	SAO2	Negative output of speaker amplifier (push-pull only)
14	SAO1	Positive output of speaker amplifier (single ended and push-pull operation)
15	VMPS	Unregulated supply voltage for the microcontroller (via series regulator to VMP)
16	VMP	Regulated output voltage for supplying the microcontroller (typ. 3.3 V/ 6 mA in speech mode)
17	VMIC	Reference node for microphone amplifier, supply for electret microphones
18	TSACL	Time constant for speaker amplifier anti-clipping

Pin	Symbol	Function
19	VRING	Input for ringer supply
20	IMPA	Input for adjusting the ringer input impedance
21	COSC	70-kHz oscillator for ringing power converter
22	SWOUT	Output for driving the external switch resistor
23	INT	Interrupt line for serial bus
24	SCL	Clock input for serial bus
25	SDA	Data line for serial bus
26	OSCIN	Input for 3.58-MHz oscillator
27	OSCOU	Clock output for the microcontroller
28	RESET	Reset output for the microcontroller
29	ES	Input for external supply indication
30	ADIN	Input of A/D converter
31	BNMR	Output of background-noise monitor receive
32	BNMT	Output of background-noise monitor transmit
33	CT	Time constant for mode switching of voice switch
34	TLDR	Time constant of receive-level detector
35	INLDR	Input of receive-level detector
36	INLDT	Input of transmit-level detector
37	TLDT	Time constant of transmit-level detector
38	IMPSW	Switch for additional line impedance
39	MICO	Microphone preamplifier output
40	AMPB	Input for playback signal of answering machine
41	AMREC	Output for recording signal of answering machine
42	STO	Output for connecting the sidetone network
43	STC	Input for sidetone network
44	STRC	Input for sidetone network

Remark: The protection device at Pin RECIN is disconnected.



14751

Figure 2. Pinning

DC Line Interface and Supply-Voltage Generation

The DC line interface consists of an electronic inductance and a dual-port output stage which charges the capacitors at VMPS and VB. The value of the equivalent inductance is given by:

$$L = 2 \times R_{\text{SENSE}} \times C_{\text{IND}} \times (R_{\text{DC}} \times R_{30}) / (R_{\text{DC}} + R_{30})$$

The U4091BM contains two identical series regulators which provide a supply voltage VMP of 3.3 V suitable for a microprocessor. In speech mode, both regulators are active because VMPS and VB are charged simultaneously by the DC line interface. The output current is 6 mA. The capacitor at VMPS is used to provide the microcomputer with sufficient power during long line interruptions. Thus, long flash pulses can be bridged or an LCD display can be turned on for more than 2 seconds after going on-hook. When the system is in ringing mode, VB is charged by the on-chip ringing power converter. In this mode, only one regulator is used to supply VMP with maximum 3 mA.

Supply Structure of the Chip

A main benefit of the U4091BM is the easy implementation of various applications due to the flexible system structure of the chip.

Possible applications:

- Group listening phone
- Hands-free phone
- Phones which feature ringing with the built-in speaker amplifier
- Answering machine with external supply

The special supply topology for the various functional blocks is illustrated in figure 3.

There are four major supply states:

1. Speech condition
2. Power down (pulse dialing)
3. Ringing
4. External supply

1. In speech condition, the system is supplied by the line current. If the LIDET-block detects a line voltage above approximately 2 V, the internal signal VLON is activated. This is detected via the serial bus, all the blocks which are needed have to be switched on via the serial bus.

For line voltages below 2 V, the switches remain in quiescent state as shown in the diagram.

- When the chip is in power-down mode (Bit LOMAKE), e.g., during pulse dialing, all internal blocks are disabled via the serial bus. In this condition, the voltage regulators and their internal bandgap are the only active blocks.
- During ringing, the supply for the system is fed into VB via the Ringing Power Converter (RPC). Normally, the speaker amplifier in single-ended mode is used for ringing. The frequency for the melody is generated by the DTMF/Melody generator.
- In an answering machine, the chip is powered by an external supply via Pin VB. The answering machine connections can be directly put to U4091BM. The answering machine is connected to the Pin AMREC. For the output AMREC, an AGC function is selectable via the serial bus. The output of the answering machine will be connected to the Pin AMPB, which is directly connected to the switching matrix, and thus enables the signal to be switched to every desired output.

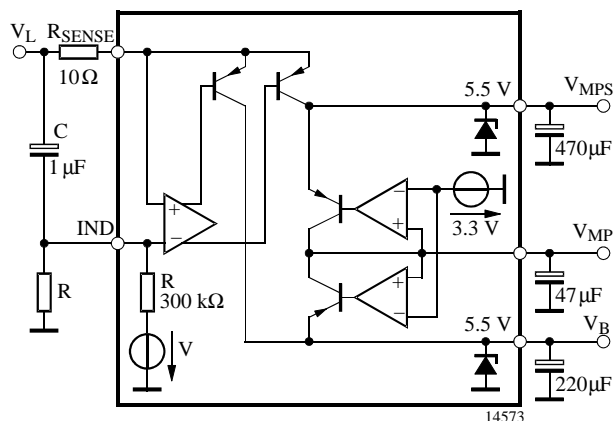


Figure 3. Supply generator

Ring Power Converter (RPC)

The RPC transforms the input power at VRING (high voltage/ low current) into an equivalent output power at VB (low voltage/ high current) which is capable of driving the low-ohmic loudspeaker. The input impedance at VRING is adjustable from 3 k Ω to 12 k Ω by RIMPA ($Z_{RING} = RIMPA / 100$) and the efficiency of the step-down converter is approximately 65%.

Ringing Frequency Detector (RFD)

The U4091BM provides an output signal for the microcontroller. This output signal is always double the value of the input signal (ringing frequency). It is generated by a current comparator with hysteresis. The levels for the on-threshold are programmable in 16 steps; the off-level is fixed. Every change of the comparator output generates a high level at the interrupt output INT. The information can then be read out by means of a serial bus with either normal or fast read mode. The block RFD is always enabled.

RINGTH[0:3]	VRING
0	7 V
15	22 V
step	1 V

Clock Output Divider Adjustment

The Pin OSCOUT is a clock output which is derived from the crystal oscillator. It can be used to drive a microcontroller or another remote component and thereby reduces the number of crystals required. The oscillator frequency can be divided by 1, 8, 16, 32. During power-on reset, the divider will be reset to 1 until it is changed by setting the serial bus.

CLK[0:1]	Divider	Frequency
0	1	3.58 MHz
1	8	447 kHz
2	16	224 kHz
3	32	112 kHz

Serial Bus Interface

The circuit is controlled by an external microcontroller through the serial bus.

The serial bus is a bi-directional system consisting of a one-directional clock line (SCL) which is always driven by the microcontroller, and a bi-directional data-signal line. It is driven by the microcontroller as well as from the U4091BM (see fig. 23).

The serial bus requires external pull-up resistors as only pull-down transistors (Pin SDA) are integrated.

WRITE: The data is a 12-bit word:

A0 – A3: address of the destination register (0 to 15)

D0 – D7: content of the register

The data line must be stable when the clock is high. Data must be shifted serially.

After 12 clock periods, the write indication is sent. Then, the transfer to the destination register is (internally) generated by a strobe signal transition of the data line when the clock is high.

READ:

There is a normal and a fast-read cycle.

In the normal read cycle, the microcontroller sends a 4-bit address followed by the read indicator, then an 8-bit word is read out. The U4091BM drives the data line.

The fast read cycle is indicated by a strobe signal. With the following two clocks the U4091BM reads out the status bits RFDO and LIDET which indicate that a ringing signal or a line signal is present (see figures 4, 5 and 6).

DTMF Dialing

The DTMF generator sends a multi-frequency signal through the matrix to the line. The signal is the result of the sum of two frequencies and is internally filtered. The frequencies are chosen from a low and a high frequency group.

The circuit conforms to the CEPT recommendation concerning DTMF option.

Two different levels for the low level group and two different pre-emphasis (2.5 dB and 3.5 dB) can be chosen by means of the serial bus (rec. T/CF 46–03).

Melody – Confidence Tone Generation

Melody/confidence tone frequencies are given in the table below.

The frequencies are provided at the DTMF input of the switch matrix. A sinus wave, a square wave or a pulsed wave can be selected by the serial bus. Square signal means the output is half of frequency cycle high and half low. Pulsed signal means between the high and low phases are high impedance phases of 1/6 of the period.

	DTMFM[0:2]	
0	000	DTMF generator OFF
1	001	Confidence tone melody on (sinus)
2	010	Ringer melody (pulse)
3	011	Ringer melody (square signal)
4	100	DTMF (high level)
5	101	DTMF (low level)
6	110	
7	111	

	DTMFF[0:1] in DTMF Mode	Frequency	Error / %
0	00	697	-0.007
1	01	770	-0.156
2	10	852	0.032
3	11	941	0.316

	DTMFF[2:3] in DTMF Mode	Frequency	Error / %
0	00	1209	-0.110
1	01	1336	0.123
2	10	1477	-0.020
3	11	1633	-0.182

DTMFF4 in DTMF mode

Pre-Emphasis Selection	
0	2.5 dB
1	3.5 dB

	DTMFF [0:4]	f Hz	Tone-Name	Error/%	DTMF		Key
0	00000	440.0	a ¹	-0.008	697	1209	1
1	00001	466.2	b ¹	-0.016	770	1209	4
2	00010	493.9	h ¹	-0.003	852	1209	7
3	00011	523.2	c ²	0.014	941	1209	*
4	00100	554.4	des ²	0.018	697	1336	2
5	00101	587.3	d ²	-0.023	770	1336	5
6	00110	622.3	es ²	-0.129	852	1336	8
7	00111	659.3	e ²	0.106	941	1336	0
8	01000	698.5	f ²	-0.216	697	1477	3
9	01001	740.0	ges ²	-0.222	770	1477	6
10	01010	784.0	g ²	0.126	852	1477	9
11	01011	830.0	as ²	-0.169	941	1477	#
12	01100	880.0	a ²	0.288	697	1633	A
13	01101	932.3	b ²	-0.014	770	1633	B
14	01110	987.8	h ²	-0.004	852	1633	C
15	01111	1046.5	c ³	-0.335	941	1633	D
16	10000	1108.7	des ³	-0.355	697	1209	1
17	10001	1174.7	d ³	-0.023	770	1209	4
18	10010	1244.5	es ³	-0.129	852	1209	7
19	10011	1318.5	e ³	0.106	941	1209	*
20	10100	1396.9	f ³	-0.214	697	1336	2
21	10101	1480.0	ges ³	-0.222	770	1336	5
22	10110	1568.0	g ³	0.126	852	1336	8
23	10111	1661.2	as ³	-0.241	941	1336	0
24	11000	1760.0	a ³	-0.302	697	1477	3
25	11001	1864.6	b ³	-0.014	770	1477	6
26	11010	1975.5	h ³	0.665	852	1477	9
27	11011	2093.0	c ⁴	0.367	941	1477	#
28	11100	2217.5	des ⁴	0.387	697	1633	A
29	11101	2349.3	d ⁴	0.771	770	1633	B
30	11110	2663.3		—	852	1633	C
31	11111	2983.0		—	941	1633	D

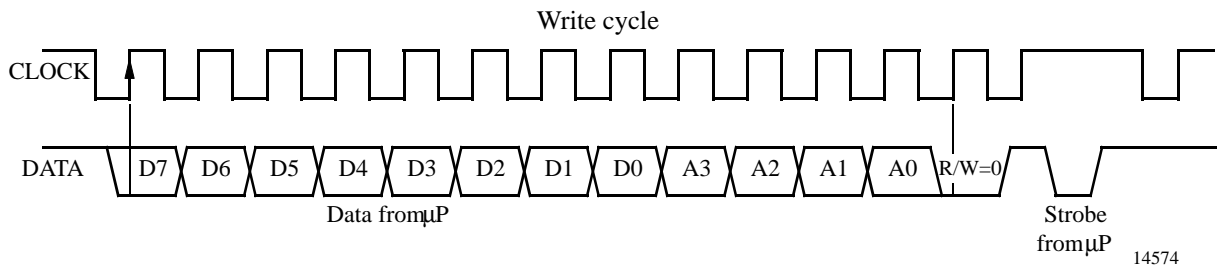


Figure 4. Write cycle

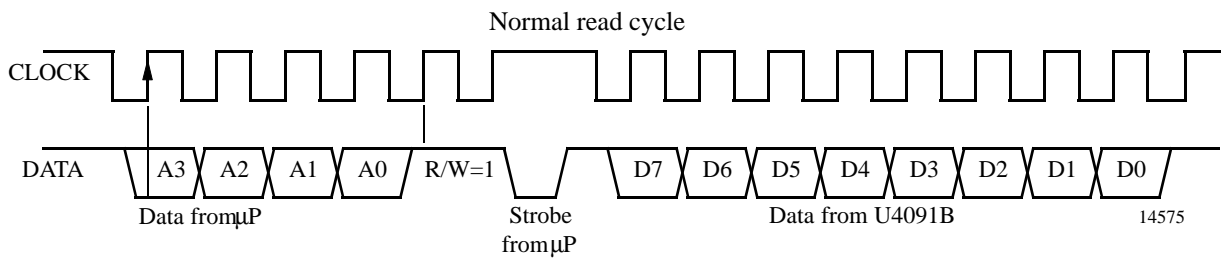


Figure 5. Normal read cycle

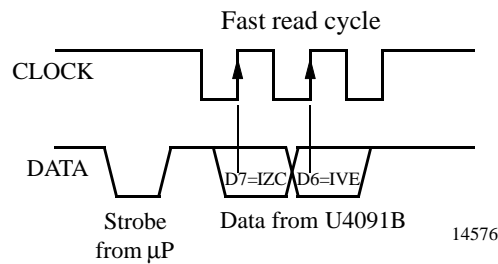


Figure 6. Fast read cycle

Table 1. Names and functions of the serial bus registers

Register	Group	No	Name	Description	Status	
R0	Enables	R0B0	ENRING	Enable ringer		1
		R0B1	ERX	Enable receive part	0	
		R0B2	ETX	Enable transmit part	0	
		R0B3	ENVM	Enable VM-generator		1
		R0B4	ENMIC	Enable microphone	0	
		R0B5	ENSTBAL	Enable sidetone	0	
		R0B6	MUTE	Muting earpiece amplifier	0	
		R0B7	ENRLT	Enable POR low threshold		1
R1	Enables	R1B0	ENSACL	Enable anti-clipping for speaker amplifier	0	
		R1B1	ENSA	Enable speaker amplifier and AFS	0	
		R1B2	ENSAO	Enable output stage speaker amplifier	0	
		R1B3	ENAM	Enable answering machine connections	0	
		R1B4	ENAGC	Enable AGC for answering machine	0	
		R1B5	free		0	
		R1B6	free		0	
		R1B7	FOFFC	Speed up offset canceller	0	
R2	Matrix	R2B0	I1O1	Switch on MIC / LTX	0	
		R2B1	I1O2	Switch on MIC / SA	0	
		R2B2	I1O3	Switch on MIC / EPO	0	
		R2B3	I1O4	Switch on MIC / AMREC	0	
		R2B4	I1O5	Switch on MIC / AGCI	0	
		R2B5	I2O1	Switch on DTMF / LTX	0	
		R2B6	I2O2	Switch on DTMF / SA	0	
		R2B7	I2O3	Switch on DTMF / EPO	0	
R3	Matrix	R3B0	I2O4	Switch on DTMF / AMREC	0	
		R3B1	I2O5	Switch on DTMF / AGCI	0	
		R3B2	I3O1	Switch on LRX / LTX	0	
		R3B3	I3O2	Switch on LRX / SA	0	
		R3B4	I3O3	Switch on LRX / EPO	0	
		R3B5	I3O4	Switch on LRX / AMREC	0	
		R3B6	I3O5	Switch on LRX / AGCI	0	
		R3B7	I4O1	Switch on AMPB / LTX	0	
R4	Matrix	R4B0	I4O2	Switch on AMPB / SA	0	
		R4B1	I4O3	Switch on AMPB / EPO	0	
		R4B2	I4O4	Switch on AMPB / AMREC	0	
		R4B3	I4O5	Switch on AMPB / AGCI	0	
		R4B4	I5O1	Switch on AGCO / LTX	0	
		R4B5	I5O2	Switch on AGCO / SA	0	
		R4B6	I5O3	Switch on AGCO / EPO	0	
		R4B7	I5O4	Switch on AGCO / AMREC	0	
R5	AGATX MICLIM	R5B0	free		0	
		R5B1	AGATX0	Gain transmit AGA LSB	0	
		R5B2	AGATX1	Gain transmit AGA	0	
		R5B3	AGATX2	Gain transmit AGA MSB	0	
		R5B4	MICHF	Select RF-microphone input	0	
		R5B5	DBM5	Max. transmit level for anti-clipping	0	
		R5B6	MIC0	Gain microphone amplifier LSB	0	
		R5B7	MIC1	Gain microphone amplifier MSB	0	

Register	Group	No	Name	Description	Status
R6	Shut down Sidetone	R6B0	SD	Shut down	0
		R6B1	free		0
		R6B2	SL0	Slope adjustment for sidetone LSB	0
		R6B3	SL1	Slope adjustment for sidetone MSB	0
		R6B4	LF0	Low frequency adjustment for sidetone LSB	0
		R6B5	LF1	Low frequency adjustment for sidetone	0
		R6B6	LF2	Low frequency adjustment for sidetone	0
		R6B7	LF3	Low frequency adjustment for sidetone MSB	0
R7	Sidetone AGARX	R7B0	P0	Pole adjustment for sidetone LSB	0
		R7B1	P1	Pole adjustment for sidetone	0
		R7B2	P2	Pole adjustment for sidetone	0
		R7B3	P3	Pole adjustment for sidetone	0
		R7B4	P4	Pole adjustment for sidetone MSB	0
		R7B5	AGARX0	Gain receive AGC LSB	0
		R7B6	AGARX1	Gain receive AGC	0
		R7B7	AGARX2	Gain receive AGC MSB	0
R8	EARA Line imp.	R8B0	EA0	Gain earpiece amplifier LSB	0
		R8B1	EA1	Gain earpiece amplifier	0
		R8B2	EA2	Gain earpiece amplifier	0
		R8B3	EA3	Gain earpiece amplifier	0
		R8B4	EA4	Gain earpiece amplifier MSB	0
		R8B5	IMPH	Line impedance selection (1 = 1 k Ω)	0
		R8B6	LOMAKE	Short circuit during pulse dialing	0
		R8B7	AIMP	Switch for additional external line impedance	0
R9	AFS	R9B0	AFS0	AFS gain adjustment LSB	0
		R9B1	AFS1	AFS gain adjustment	0
		R9B2	AFS2	AFS gain adjustment	0
		R9B3	AFS3	AFS gain adjustment	0
		R9B4	AFS4	AFS gain adjustment	0
		R9B5	AFS5	AFS gain adjustment MSB	0
		R9B6	AFS4PS	Enable 4-point sensing	0
		R9B7	free		0
R10	SA	R10B0	SA0	Gain speaker amplifier LSB	0
		R10B1	SA1	Gain speaker amplifier	0
		R10B2	SA2	Gain speaker amplifier	0
		R10B3	SA3	Gain speaker amplifier	0
		R10B4	SA4	Gain speaker amplifier MSB	0
		R10B5	SE	Speaker amplifier single-ended mode	0
		R10B6	LSCUR0	Speaker amplifier charge-current adjustment LSB	0
		R10B7	LSCUR1	Speaker amplifier charge-current adjustment MSB	0
R11	ADC	R11B0	ADC0	Input selection ADC	0
		R11B1	ADC1	Input selection ADC	0
		R11B2	ADC2	Input selection ADC	0
		R11B3	ADC3	Input selection ADC	0
		R11B4	NWT	Network tuning	0
		R11B5	SOC	Start of ADC conversion	0
		R11B6	ADCR	Selection of ADC range	0
		R11B7	MSKIT	Mask for interrupt bits	0

Register	Group	No	Name	Description	Status
R12	DTMF	R12B0	DTMFF0	DTMF frequency selection	0
		R12B1	DTMFF1	DTMF frequency selection	0
		R12B2	DTMFF2	DTMF frequency selection	0
		R12B3	DTMFF3	DTMF frequency selection	0
		R12B4	DTMFF4	DTMF frequency selection	0
		R12B5	DTMFM0	Generator mode selection	0
		R12B6	DTMFM1	Generator mode selection	0
		R12B7	DTMFM2	Generator mode selection	0
R13	CLK	R13B0	CLK0	Selection clock frequency for μ C	0
		R13B1	CLK1	Selection clock frequency for μ C	0
	RTH TM	R13B2	RTH0	Ringer threshold adjustment LSB	0
		R13B3	RTH1	Ringer threshold adjustment	0
		R13B4	RTH2	Ringer threshold adjustment	0
		R13B5	RTH3	Ringer threshold adjustment MSB	0
		R13B6	TME0	Test mode enable (low active)	0
		R13B7	TME1	Test mode enable (high active)	0
R14	TM CLOR	R14B0	TME2	Test mode enable (high active)	0
		R14B1	TME3	Test mode enable (low active)	0
	R14B2	free		0	
	R14B3	CLOR0	Adjustment for calculated receive log amp LSB	0	
	R14B4	CLOR1	Adjustment for calculated receive log amp	0	
	R14B5	CLOR2	Adjustment for calculated receive log amp	0	
	R14B6	CLOR3	Adjustment for calculated receive log amp	0	
	R14B7	CLOR4	Adjustment for calculated receive log amp MSB	0	
R15	CLOT	R15B0	free		0
		R15B1	free		0
		R15B2	free		0
		R15B3	CLOT0	Adjustment for calculated transmit log amp LSB	0
		R15B4	CLOT1	Adjustment for calculated transmit log amp	0
		R15B5	CLOT2	Adjustment for calculated transmit log amp	0
		R15B6	CLOT3	Adjustment for calculated transmit log amp	0
		R15B7	CLOT4	Adjustment for calculated transmit log amp MSB	0

Power-on Reset

To avoid undefined states of the system when it is powered on, an internal reset clears the internal registers.

The system (U4091BM + microcontroller) is woken up by any of the following conditions:

VMP > 2.75 V and VB > 2.95 V

and line voltage (VL)

or ringer (VRING)

or external supply (ES)

The power-down of the circuit is caused by a shut-down sent by the serial bus (SD = 1), low-voltage reset or by the watchdog function (see figures 8, 9 and 10).

Watchdog Function

To avoid the system operating the microcontroller in a wrong condition, the circuit provides a watchdog function. The watchdog has to be retriggered every second by triggering the serial bus (sending information to the IC or other remoted components at the serial bus). If there has been no bus transmission for more than one second, the watchdog initiates a reset.

The watchdog provides a reset for the external μ C, but does not change the U4091BM's registers.

Acoustic Feedback Suppression

Acoustical feedback from the loudspeaker to the hands-free microphone may cause instability of the system. The U4091BM has a very efficient feedback-suppression circuit which offers a 4-point- or alternatively a 2-point-signal-sensing topology (see figure 7).

Two attenuators (TXA and SAI) reduce the critical loop gain via the serial bus either in the transmit or in the receive path. The overall loop gain remains constant under all operating conditions.

The LOGs produce a logarithmically-compressed signal of the TX- and RX-envelope curve. The block AFSCON determines whether the TX or the RX signal has to be attenuated.

The voice-switch topology can be selected by the serial bus. In 2-point-sensing mode, AFSCON is controlled directly by the LOG outputs.

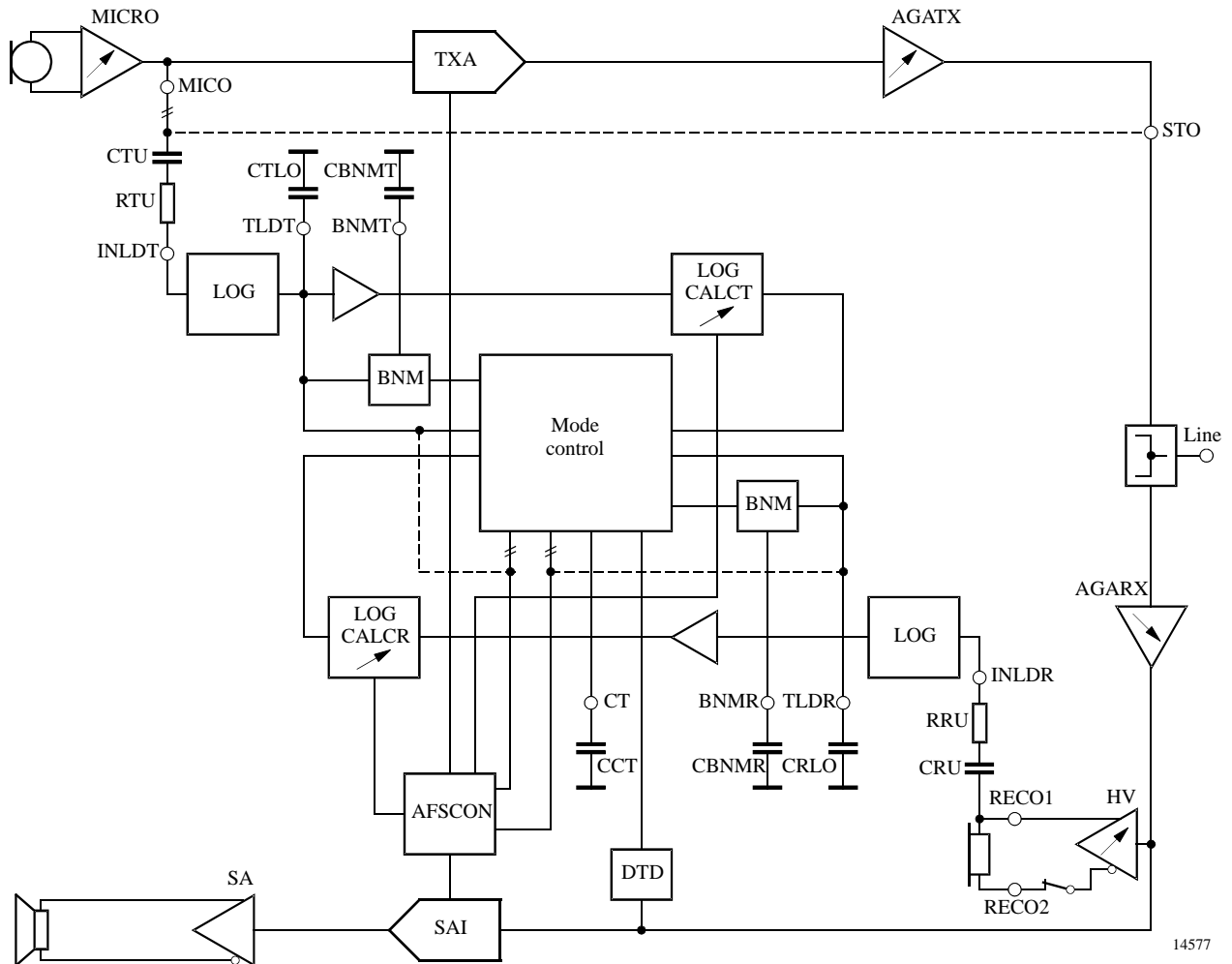


Figure 7. Basic system configurations.

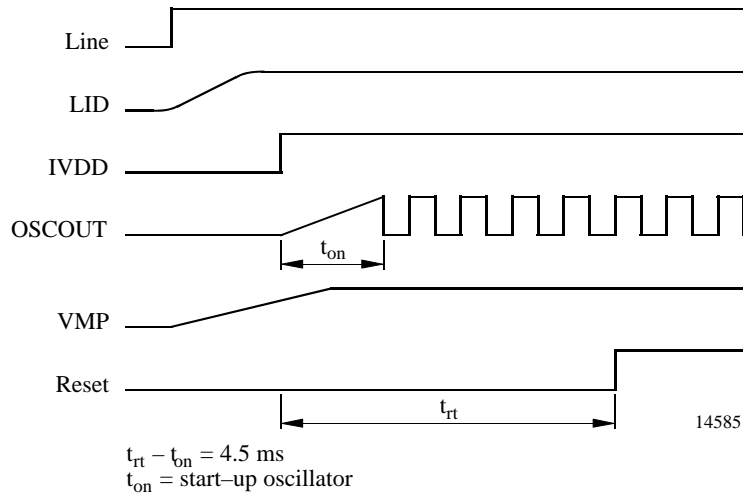


Figure 8. Power-on reset (line)

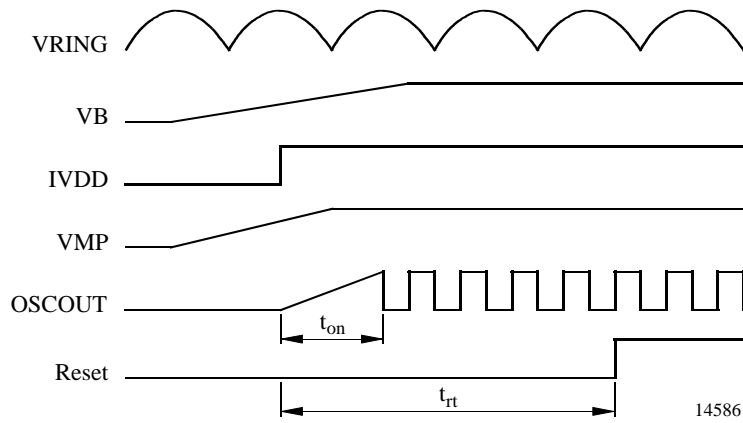


Figure 9. Power-on reset (ringing)

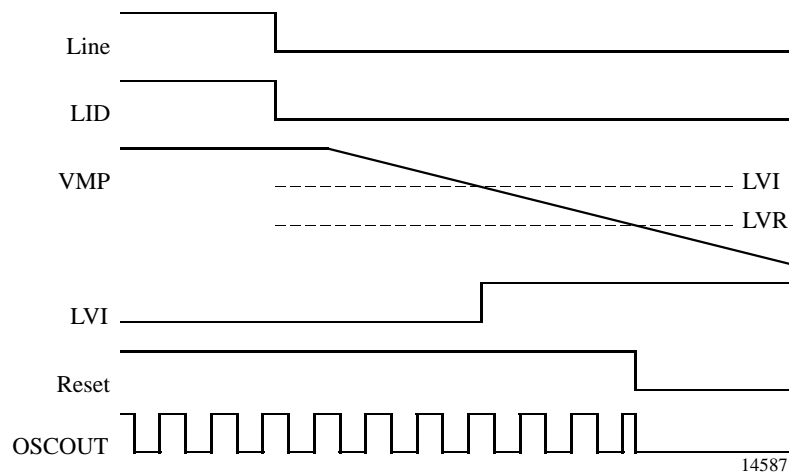


Figure 10. Power-on reset (low voltage reset)

Dial-Tone Detector

The dial-tone detector is a comparator with one side connected to the speaker amplifier input and the other to V_M with a 35-mV offset (see figure 11). If the circuit is in idle mode, and the incoming signal is greater than 35 mV (25 mVrms), the comparator's output will change disabling the receive idle mode. This circuit prevents the dial tone (which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

Background-Noise Monitors

This circuit distinguishes speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background-noise monitors – one for the receive path and the other for the transmit path. The receive background-noise monitor is operated on by the receive level detector, while the transmit background noise monitor is operated on by the transmit level detector (see figure 12). They monitor the background noise by storing a DC voltage representative of the respective noise levels in capacitors at CBNMR and CBNMT. The voltages at these pins have slow rise times (determined by the internal current source and an external C), but fast decay times. If the signal at TLDR (or TLDT) changes slowly, the voltage at BNMR (or BNMT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage at the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the mode-control block.

4-Point Sensing

In 4-point sensing mode, the receive- and the transmit-sensing path include additional CLOGs (Calculated Logarithmical amplifier). The block MODECON compares the detector output signals and decides whether receive-, transmit- or idle mode has to be activated. Depending on the mode decision, MODECON generates a differential voltage to control AFSCON.

The MODECON block has seven inputs:

- The output of the transmit log (LOGT) the comparison of LOGT, CLOGR
- The output of the receive clog (CLOGR) – designated I1
- The output of the transmit clog (CLOGT) the comparison of CLOGT, LOGR

- The output of the receive log (LOGR) – designated I2
- The output of the transmit background-noise monitor (BNMT) – designated I3
- The output of the receive background-noise monitor (BNMR) – designated I4
- The output of the dial-tone detector

The differential output (AFST, AFSR) of the block MODECON controls AFSCON. The effect of I1-I4 is as follows:

Inputs				Output
I1	I2	I3	I4	Mode
T	T	S	X	Transmit
T	R	Y	Y	Change mode
R	T	Y	Y	Change mode
R	R	X	S	Receive
T	T	N	X	Idle
T	R	N	N	Idle
R	T	N	N	Idle
R	R	X	N	Idle

X = don't care; Y = I3 and I4 are not both noise.

LOGT > CLOGR	I1=T
LOGT < CLOGR	I1=R
LOGR < CLOGT	I2=T
LOGR > CLOGT	I2=R
BNMT detects speech	I3=S
BNMT detects noise	I3=N
BNMR detects speech	I4=S
BNMR detects noise	I4=N

Term Definitions

1. 'Transmit' means the transmit attenuator is fully on, and the receive attenuator is at maximum attenuation.
2. 'Receive' means the receive attenuator is fully on, and the transmit attenuator is at maximum attenuation.
3. In 'Idle' mode, the transmit- and receive attenuator are at the half of their maximum attenuation.
 - a) 'Change mode' means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to the opposite mode until one speech level dominates the other.
 - b) 'Idle' means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1.5 seconds) to idle mode.
4. Switching to the full transmit or receive modes from idle mode is at the fast rate (30 ms).

Summary of the Truth Table

1. The circuit will switch to transmit mode if
 - a) Both transmit level detectors sense higher signal levels than the respective receive level detectors and
 - b) The transmit background-noise monitor indicates the presence of speech.
2. The circuit will switch to receive mode if
 - a) Both receive level detectors sense higher signal levels than the respective transmit level detectors, and
 - b) The receive background-noise monitor indicates the presence of speech.
3. The circuit will switch to the reverse mode if the level detectors disagree on the relative strengths of the signal levels, and at least one of the background-noise monitors indicates speech.
4. The circuit will switch to idle mode when
 - a) Both talkers are quiet (no speech present), or
 - b) When one talker's speech level is continuously overridden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive and idle is determined by internal current sources and the capacitor at Pin CT. A diagram of the C_T circuitry is shown in figure 13. It operates as follows:

- CCT is typically $4.7 \mu\text{F}$.
- To switch to transmit mode, ITX is turned on (IRX is off), charging the external capacitor to -240 mV below V_M . (An internal clamp prevents further charging of the capacitor.)

- To switch to receive mode, IRX is turned on (ITX is off), increasing the voltage on the capacitor to $+240 \text{ mV}$ with respect to V_M .
- To switch to reverse mode, the current sources ITX, IRX are turned off, and the current source IFI is switched on, discharging the capacitor to V_M .
- To switch to idle mode, the current sources ITX, IRX, IFI are turned off, and the current source ISI is charging the capacitor to V_M .

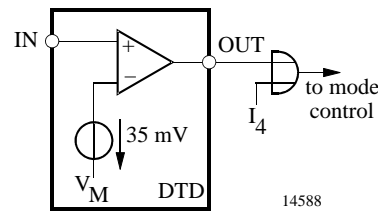


Figure 11. Dial tone detector

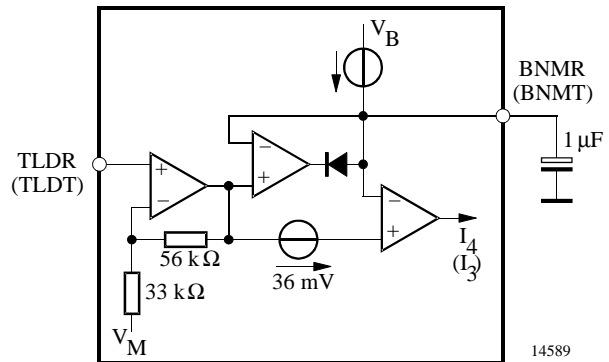


Figure 12. Background noise monitor

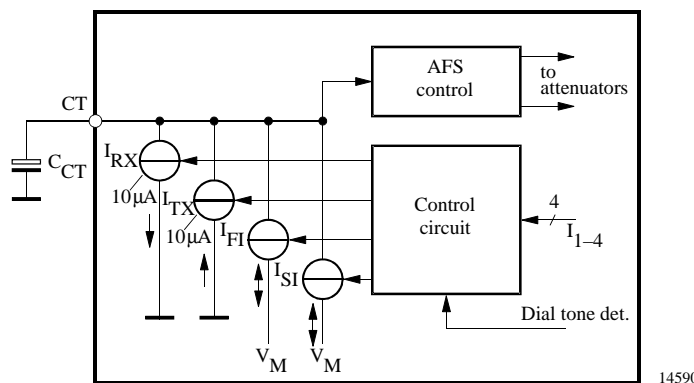


Figure 13. Generation of control voltage (CT) for mode switching

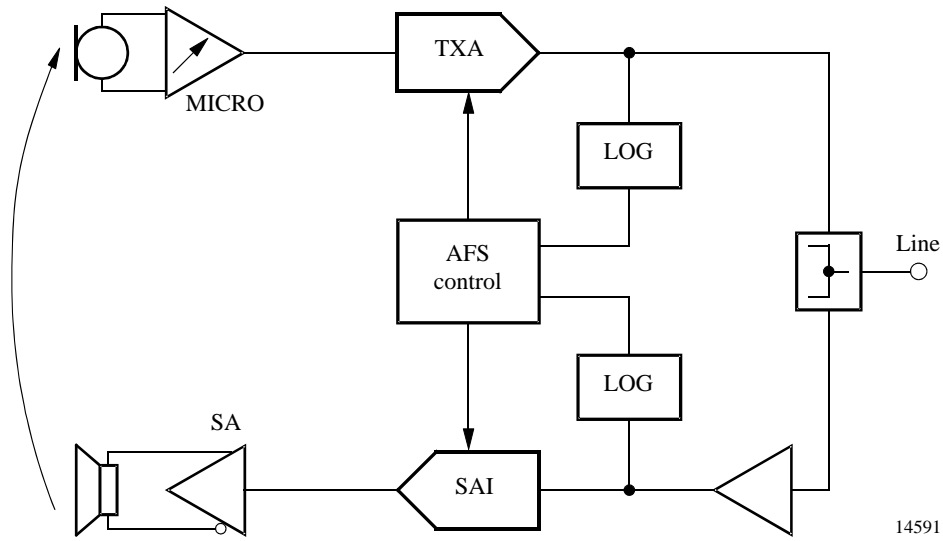


Figure 14. Block diagram hands-free mode U4091BM 2-point signal sensing

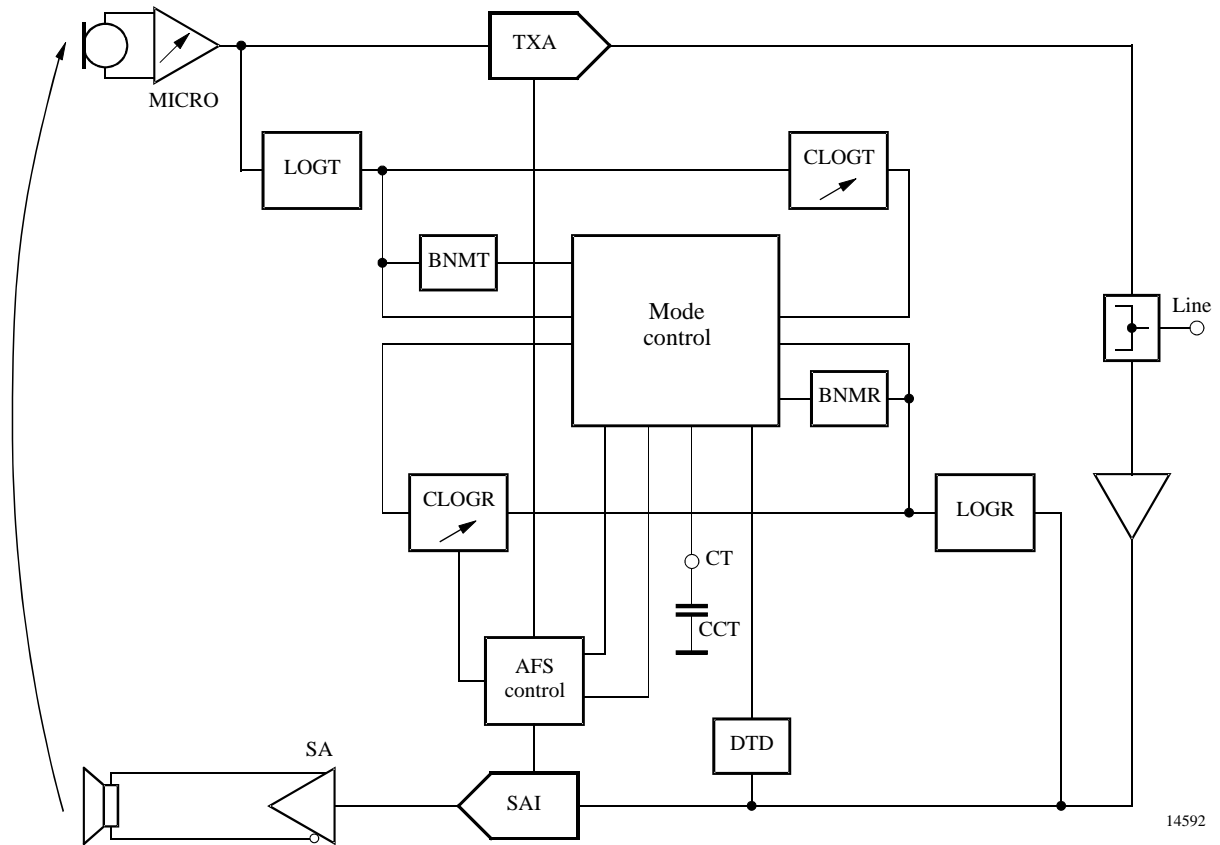


Figure 15. Block diagram hands-free mode U4091BM 4-point signal sensing

Analog-to-Digital Converter ADC

This circuit is a 7-bit successive approximation analog-to-digital converter in switched capacitor technique. An internal bandgap circuit generates a 1.25-V reference voltage which is the equivalent of 1 MSB. 1LSB = 19.5 mV. The possible input voltage at ADIN is 0 to 2.48 V.

The ADC needs an SOC (Start Of Conversion) signal. In the 'High' phase of the SOC signal, the ADC is reset. 50 μs after the beginning of the 'Low' phase of the SOC signal, the ADC generates an EOC (End Of Conversion) signal which indicates that the conversion is finished. The rising edge of EOC generates an interrupt at the INT output. The result can be read out by the serial bus.

Voltages higher than 2.45 V have to be divided. The signal which is connected to the ADC is determined by 5 bits: ADC0, ADC1, ADC2, ADC3 and NWT. TLDR/TLDT measuring is possible relative to a preceding reference measurement. The current range of IL can be doubled by ADCR. If ADCR is 'High', S has the value 0.5, otherwise S = 1.

The source impedance at ADIN must be lower than 250 kΩ.

Accuracy: 1 LSB + 3%

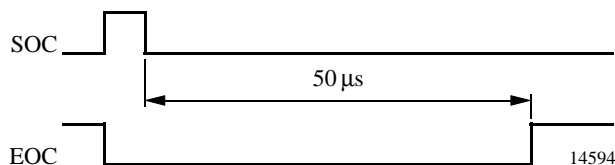


Figure 16. Timing of ADC

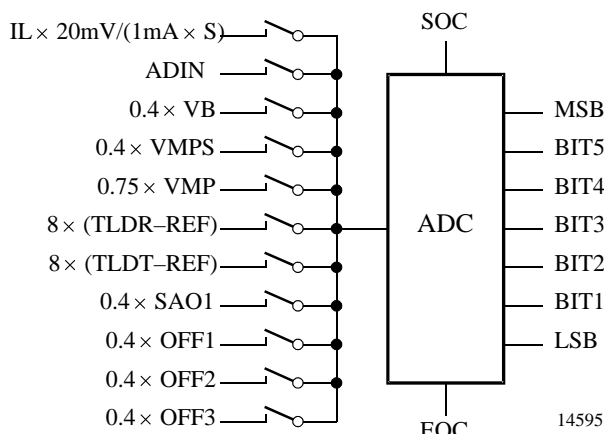


Figure 17. ADC input selection

Table 2. Input selection AD converter

	ADC[1:4]		Value
0	00000	OFF	
1	00001	IL	$I1 = S \times 127 \text{ mA} \times D / 127$
2	00010	ADIN extern	$V2 = 2.5 \text{ V} \times D / 127$ (max. 2.5 V)
3	00011	VB	$V3 = (2.5 \text{ V} / 0.4) \times D / 127$
4	00100	VMPS	$V4 = (2.5 \text{ V} / 0.4) \times D / 127$
5	00101	VMP	$V5 = (2.5 \text{ V} / 0.75) \times D / 127$
6	00110	TLDR	$V6 = 8 \times (Vp - \text{Ref}) \times D / 127$
7	00111	TLDT	$V7 = 8 \times (Vp - \text{Ref}) \times D / 127$
8	01000	free	
9	01001	SAO1	$V4 = (2.5 \text{ V} / 0.4) \times D / 127$
10	01010	Offcan1	TEMIC internal use
11	01011	Offcan2	TEMIC internal use
12	01100	Offcan3	TEMIC internal use
13	01101	free	
14	01110	free	
15	01111	free	
16–31	1XXXX	NWT (TLDR)	

D = measured digital word ($0 \leq D \leq 127$)

S = programmable gain 0.5 or 1

Vp = peak value of the measured signal

Switch Matrix

The switch matrix has 5 inputs and 5 outputs. Every pair of input and output except AGCO and AGCIN can be connected. The inputs and outputs used must be enabled. If 2 or more inputs are switched to an output, the sum of the inputs is available at the output.

The inputs MIC and LRX have offset cancellers with a 3-dB corner frequency of 270 Hz. AMPB has a 60-kΩ input impedance. The TXO output has a digitally-programmable gain stage with a gain of 2, 3 to 9 dB depending on AGATX0 (LSB), AGATX1, AGATX2 (MSB) and a first order low-pass filter with 0.5 dB damping at 3300 Hz and 3 dB damping at 9450 Hz. The outputs RXLS, EPO and AMREC have a gain of 0 dB. The offset at the outputs of the matrix is less than 30 mV. If a switch is open, the path has a damping of more than 60 dB.

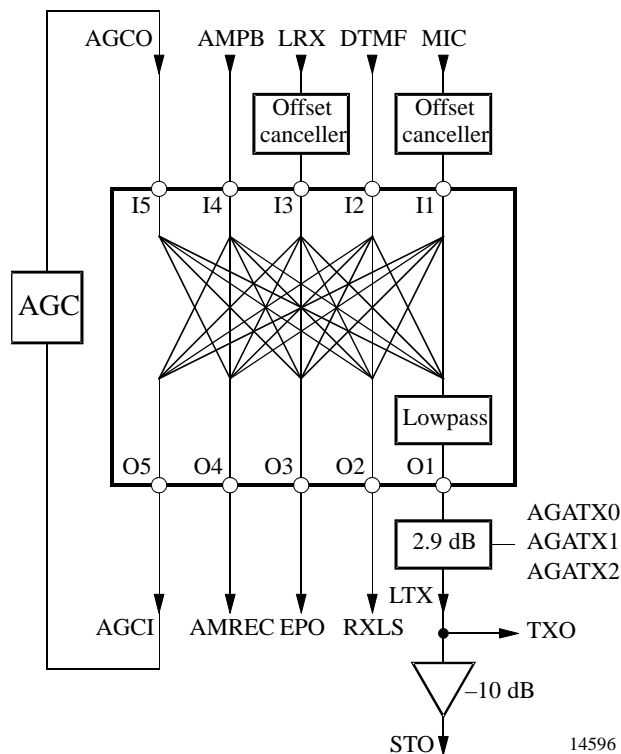


Figure 18. Diagram for switch matrix

Table 3. Table of bits and corresponding switches

Register	No.	Name	Description
R2	R2B0	I1O1	Switch on MIC / LTX
	R2B1	I1O2	Switch on MIC / RXLS
	R2B2	I1O3	Switch on MIC / EPO
	R2B3	I1O4	Switch on MIC / AMREC
	R2B4	I1O5	Switch on MIC / AGCI
	R2B5	I2O1	Switch on DTMF / LTX
	R2B6	I2O2	Switch on DTMF / RXLS
R3	R2B7	I2O3	Switch on DTMF / EPO
	R3B0	I2O4	Switch on DTMF / AMREC
	R3B1	I2O5	Switch on DTMF / AGCI
	R3B2	I3O1	Switch on LRX / LTX
	R3B3	I3O2	Switch on LRX / RXLS
	R3B4	I3O3	Switch on LRX / EPO
	R3B5	I3O4	Switch on LRX / AMREC
R4	R3B6	I3O5	Switch on LRX / AGCI
	R3B7	I4O1	Switch on AMPB / LTX
	R4B0	I4O2	Switch on AMPB / RXLS
	R4B1	I4O3	Switch on AMPB / EPO
	R4B2	I4O4	Switch on AMPB / AMREC
	R4B3	I4O5	Switch on AMPB / AGCI
	R4B4	I5O1	Switch on AGCO / LTX
R4B5	I5O2	Switch on AGCO / RXLS	
R4B6	I5O3	Switch on AGCO / EPO	
R4B7	I5O4	Switch on AGCO / AMREC	

Sidetone System

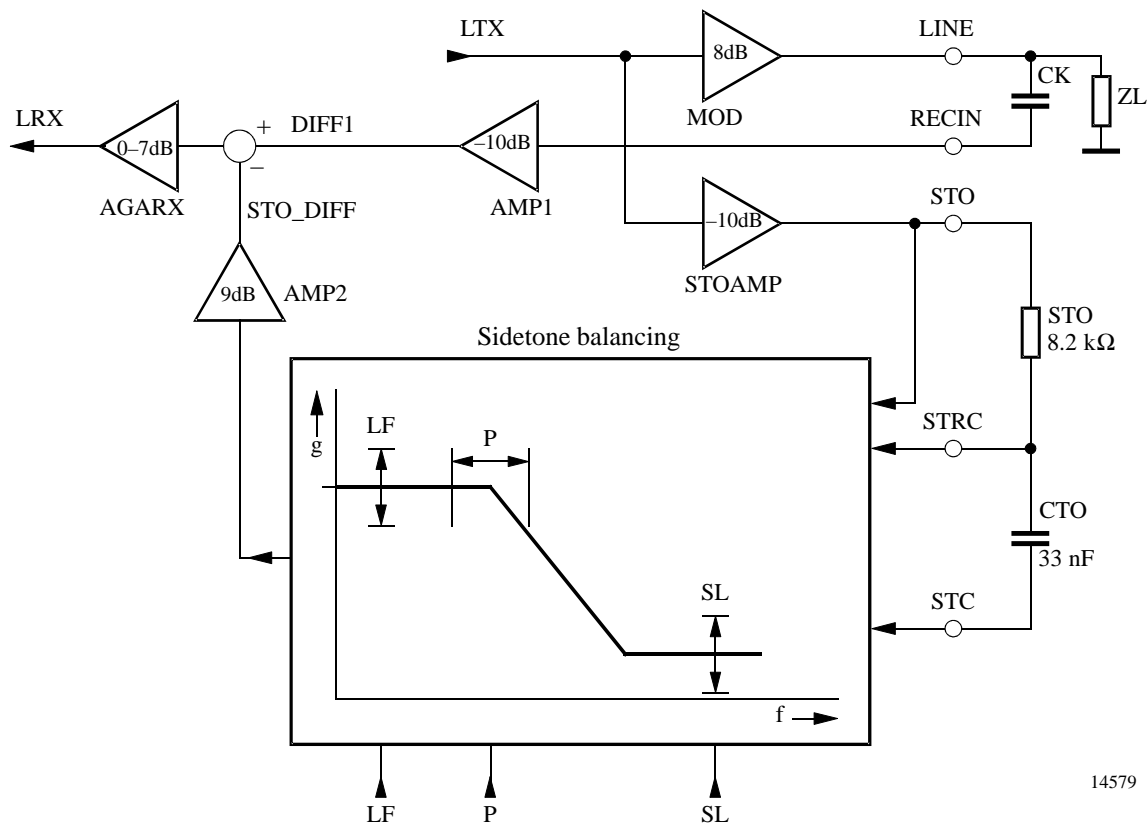


Figure 19. Principle circuit of the sidetone balancing

The SideTone Balancing (STB) has the task of reducing the crosstalk from LTX (microphone) to LRX (earpiece) in the frequency range of 0.3 to 3.4 kHz. The LTX signal is converted into a current in the MOD block. This current is transformed into a voltage signal (LINE) by the line impedance ZL. The LINE signal is fed into the summing amplifier DIFF1 via capacitor CK and attenuator AMP1.

On the other hand the LTX buffered by STOAMP drives an external lowpass filter (RST, CST). The external lowpass filter and the internal STB have the transfer function drawn in the STB box. The amplified STB-output signal drives the negative input of the summing block. If both signals at the DIFF1 block are equal in level and phase, we have good suppression of the LTX signal. In this condition, the frequency and phase response of the STB block will represent the frequency curve on line.

In real life the line impedance ZL varies strongly for different users. To obtain good suppression with one application for all different line impedances, the STB function is programmable.

The 3 programmable parameters are:

1. LF (gain at low frequency)
LF has 15 programming steps of 0.5 dB. LF(0) gives -2 dB gain, LF(15) gives 5.5 dB gain.

$$STO_DIFF(LF) = (-10 \text{ dB} - 2 \text{ dB} + 0.5 \text{ dB} \times LF + 9 \text{ dB}) \times LTX$$

2. P (the pole position of the lowpass)
The P adjustment has 31 steps. P(0) means the lowpass determined by the external application (RST, CST). The internally processed lowpass frequency is fixed by this equation

$$f(P) = \frac{1}{2 \times \pi \times CST \times RST} \times 1.122^P$$

3. SL
(sidetone slope; the pole frequency of the highpass)
The SL has 3 steps. SL(0) is a lower frequency of the highpass. SL(3) is a higher frequency of the highpass. With SL, can be influenced the suppression at high frequencies.

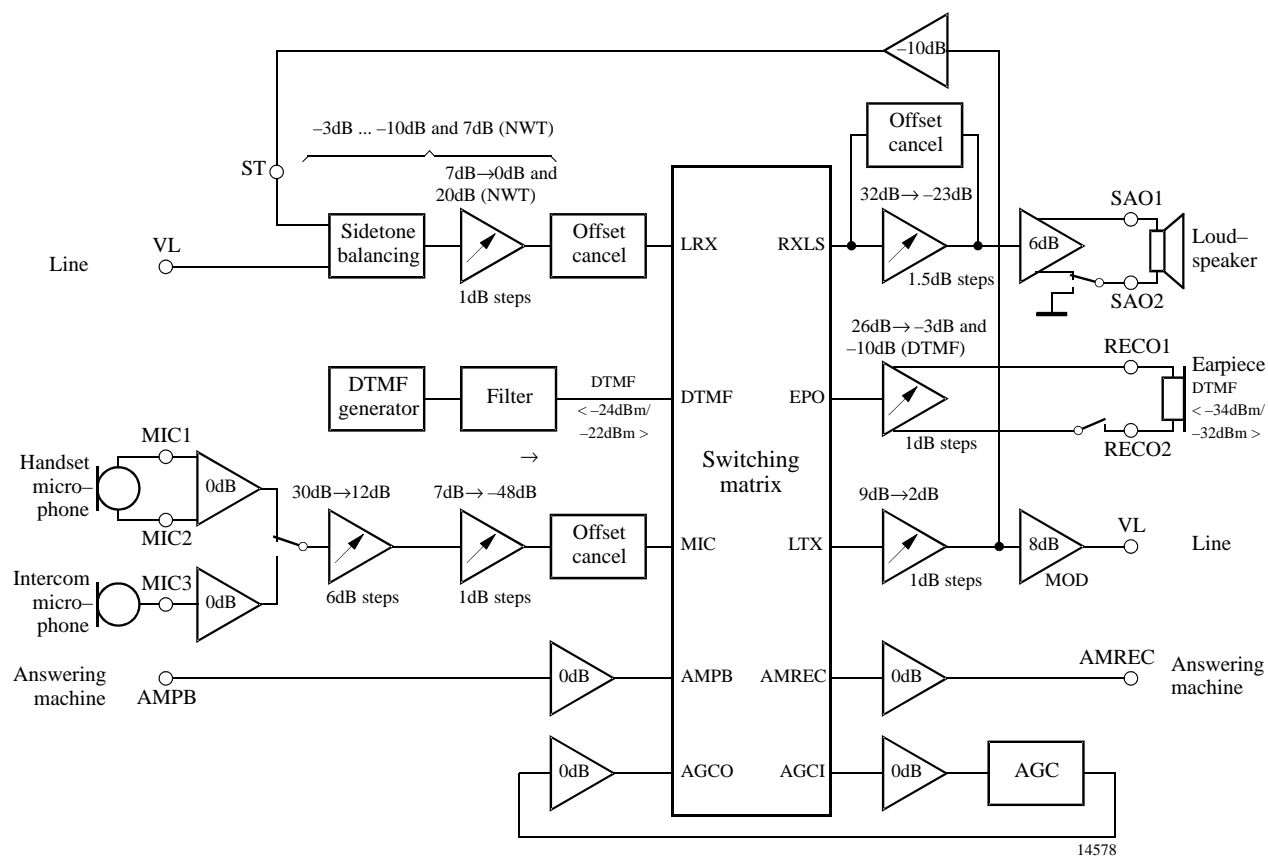


Figure 20. Audio frequency signal management U4091BM

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Line current	I_L	140	mA
DC line voltage	V_L	12	V
Maximum input current	I_{RING}	15	mA
Junction temperature	T_j	125	°C
Ambient temperature	T_{amb}	-25 to +75	°C
Storage temperature	T_{stg}	-55 to +150	°C
Total power dissipation, $T_{amb} = 60^\circ\text{C}$	P_{tot}	0.9	W

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO44	R_{thJA}	70	K/W

Electrical Characteristics

$f = 1 \text{ kHz}$, $0 \text{ dBm} = 775 \text{ mV}_{\text{rms}}$, $I_{\text{VMIC}} = 0.3 \text{ mA}$, $I_{\text{MP}} = 3 \text{ mA}$, $R_{\text{DC}} = 1.3 \text{ M}\Omega$, $T_{\text{amb}} = 25^\circ\text{C}$, $Z_{\text{car}} = 68 \text{ nF} + 100 \Omega$, $Z_{\text{M}} = 68 \text{ nF}$, resonator: $f = 3.58 \text{ MHz}$, all bits in reset condition, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
DC characteristics							
DC voltage drop-over circuit	$I_{\text{L}} = 2 \text{ mA}$ $I_{\text{L}} = 14 \text{ mA}$ $I_{\text{L}} = 60 \text{ mA}$ $I_{\text{L}} = 100 \text{ mA}$	V_{L}	4.6 8.8	2.4 5.0 7.5 9.4	5.4 10.0	V	
Transmission amplifier, $I_{\text{L}} = 14 \text{ mA}$, $V_{\text{MIC}} = 2 \text{ mV}$, $\text{MICG}[0:1] = 2$, $\text{AGATX}[0:2] = 7$ $\text{ERX} = \text{ETX} = \text{ENMIC} = \text{ENSTBAL} = \text{I1O1} = \text{I3O3} = 1$, ($G_{\text{T}} = 48 \text{ dB}$)							
Transmit amplification	$\text{MICG}[0:1] = 2$ $\text{AGATX}[0:2] = 7$	G_{T}	45.8	47	48.2	dB	
Frequency response due to internal filters)	$I_{\text{L}} \geq 14 \text{ mA}$, $f = 1 \text{ kHz}$ to 3.4 kHz	ΔG_{T}	-1		0	dB	
Gain change with current	$I_{\text{L}} = 14$ to 100 mA	ΔG_{T}			± 0.5	dB	
Gain deviation	$T_{\text{amb}} = -10$ to $+60^\circ\text{C}$	ΔG_{T}			± 0.5	dB	
CMRR of microphone amplifier		CMRR	60	80		dB	
Input resistance of MIC amplifier		R_{i}		50		k Ω	
Input resistance of MIC3 amplifier	$\text{MICHF} = 1$	R_{i}	75	150	300	k Ω	
Gain difference between MIC1, MIC2 to MIC3	$\text{MICHF} = 1$	ΔG_{T}			± 0.4	dB	
Distortion at line	$I_{\text{L}} \geq 14 \text{ mA}$ $V_{\text{L}} = 700 \text{ mV}_{\text{rms}}$	d_{t}			2	%	
Maximum output voltage	$I_{\text{L}} \geq 19 \text{ mA}$, $d < 5\%$ $V_{\text{MIC}} = 10 \text{ mV}$ $\text{CTXA} = 1 \mu\text{F}$ $\text{DBM5} = 0$	V_{Lmax}	1.3	2.5	3.7	dBm	
	$\text{DBM5} = 1$	V_{Lmax}	3.8	5.0	6.2	dBm	
	$V_{\text{MIC}} = 20 \text{ m}$ $\text{MICG}[0:1] = 3$	V_{MICOmax}		-5.2		dBm	
Noise at line psophometrically weighted	$I_{\text{L}} \geq 14 \text{ mA}$, $\text{MICG}[0:1] = 2$ $\text{AGATX}[0:2] = 7$	no			-80 -72	dBmp	
Anti-clipping: attack time release time	$\text{CTXA} = 1 \mu\text{F}$ each 3 dB overdrive	t_{a} t_{r}		0.5 16		ms ms	
Gain at low operating current	$I_{\text{L}} = 8 \text{ mA}$, $I_{\text{MP}} = 1 \text{ mA}$ $R_{\text{DC}} = 680 \text{ k}\Omega$ $V_{\text{MIC}} = 0.5 \text{ mV}$ $I_{\text{VMIC}} = 300 \mu\text{A}$	G_{T}	45.5		48.5	dB	
Distortion at low operating current	$I_{\text{L}} = 8 \text{ mA}$, $I_{\text{MP}} = 1 \text{ mA}$ $R_{\text{DC}} = 680 \text{ k}\Omega$ $V_{\text{MIC}} = 5 \text{ mV}$ $I_{\text{VMIC}} = 300 \mu\text{A}$	d_{t}			5	%	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Receiving amplifier							
$I_L = 14 \text{ mA}$, $V_{GEN} = 300 \text{ mV}$, $ERX = ETX = ENMIC = ENSTBAL = I101 = I303 = 1$, $SL[0:1] = 0$, $LF[0:3] = 1$, $P[0:4] = 31$, $AGARX[0:2] = 0$							
Adjustment range of receiving gain	Single ended, $I_L \geq 14 \text{ mA}$, Mute = 1, $EA[0:4] = 2 - 31$ $AGARX[0:2] = 0 - 7$	G_R	-19		+17	dB	
Receiving amplification	Differential $AGARX[0:2] = 0$ $EA[0:4] = 15$ $EA[0:4] = 31$	G_R	-1 15	0 16	1 17	dB dB	
Frequency response	$I_L \geq 14 \text{ mA}$, $f = 1 \text{ kHz to } 3.4 \text{ kHz}$	ΔG_{RF}	-1		0	dB	
Gain change with current	$I_L = 14 \text{ to } 100 \text{ mA}$	ΔG_R			± 0.5	dB	
Gain deviation	$T_{amb} = -10 \text{ to } +60^\circ\text{C}$	ΔG_R			± 0.5	dB	
Ear protection differential	$I_L \geq 14 \text{ mA}$, $V_{GEN} = 11 \text{ V}_{rms}$ $EA[0:4] = 21$	EP			3	V_{rms}	
MUTE suppression	$I_L = 14 \text{ mA}$	ΔG_R	60			dB	
Output voltage $d < 2\%$ differential	$I_L = 14 \text{ mA}$ $Z_{ear} = 68 \text{ nF} + 100 \Omega$ $EA[0:4] = 11$		0.775			V_{rms}	
Maximum output current $d < 2\%$	$Z_{ear} = 100 \Omega$ $EA[0:4] = 31$	I_{out}	4			mA_p	
Receiving noise psophometrically weighted	$I_L = 14 \text{ mA}$ $Z_{ear} = 68 \text{ nF} + 100 \Omega$ $EA[0:4] = 21$			-80	-77	dBmp	
Sidetone suppression	$Z = 600 \Omega$		20			dB	
Output resistance	Each output against GND	R_o			10	Ω	
Gain at low operating current (receive only)	$I_L = 5 \text{ mA}$, $I_{MP} = 1 \text{ mA}$ $I_M = 300 \mu\text{A}$ $V_{GEN} = 200 \text{ mV}$ $R_{DC} = 680 \text{ k}\Omega$, $EA[0:4] = 21$, $ENMIC = ETX = I101 = 0$	G_R	-2	0	2	dB	
AC impedance	$IMPH = 0$ $IMPH = 1$	Z_{imp} Z_{imp}		620 1040		Ω Ω	
Distortion at low operating current	$I_L = 8 \text{ mA}$, $I_{MP} = 1 \text{ mA}$ $V_{GEN} = 400 \text{ mV}$ $R_{DC} = 680 \text{ k}\Omega$ $EA[0:4] = 21$	dR			5	%	
Adjustment step: ear-piece amplifier	$AGARX[0:4] = 1$		0.8	1	1.2	dB	
Adjustment step: AGARX	$EA[0:4] = 1$		0.8	1	1.2	dB	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Gain for DTMF signal	AMPB → RECO1/2 EA[0:4] = 1			-16		dB	
DTMF, I_L = 14 mA, ETX = I201 = 1, AGATX[0:2] = 7, DTMFM[0:2] = 4, DTMFF[0:2] = 0							
Max. level at line	Sum level, 600 Ω, DTMFM[0:2] = 5		-5.1	-3.6	-2.1	dBm	
DTMF level at line (low gain)	Sum level, 600 Ω, DTMFM[0:2] = 4		-7.6	-6.1	-4.6	dBm	
Pre-emphasis	600 Ω, DTMFF4 = 0 DTMFF4 = 1		2	2.5	3	dBm	
			3	3.5	4	dBm	
Speaker amplifier, differential mode							
AMPB → SAO1/2							
ENSACL = ENSA = ENSAO = ENAM = I4O2 = 1, SA[0:4] = 31							
Minimum line current for operation	No AC signal	I _{Lmin}			8	mA	
Gain from AMPB to SAO	V _{AMPB} = 3 mV, I _L = 15 mA, SA[0:4] = 31 SA[0:4] = 0	G _{SA}	37	38 -8.5	39	dB	
Adjustment step speaker amplifier	SA[0:4] = -1		1.3	1.5	1.7	dB	
Output power single ended	Load resistance: R _L = 50 Ω, d < 5% V _{AMPB} = 20 mV, SE = 1 I _L = 15 mA I _L = 20 mA	P _{SA}	3	7		mW	
		P _{SA}		20		mW	
Max. output power differential	Load resistance: R _L = 50 Ω, d < 5% V _{AMPB} = 20 mV, SE = 0 V _B = 5 V	P _{SA}		200		mW	
Output noise (input AMPB open) psophometrically weighted	I _L > 15 mA	n _{SA}			240	μV _{psoph}	
Gain deviation	I _L = 15 mA T _{amb} = -10 to +60°C	ΔG _{SA}			±1	dB	
Mute suppression	I _L = 15 mA, V _L = 0 dBm, V _{AMPB} = 4 mV I4O2 = 0	V _{SAO}			-60	dBm	
Gain change with current	I _L = 15 to 100 mA	ΔG _{SA}			1	dB	
Gain change with frequency	I _L = 15 mA f = 1 kHz to 3.4 kHz	ΔG _{SA}	-1		0	dB	
Attack time of anti-clipping	20 dB over drive	t _r		5		ms	
Release time of anti-clipping		t _f		80		ms	
Adjustment step of charge current	ENSAO = 0, SE = 1 ΔLSCUR[0:1] = 1		-480	400	-320	μA	
Adjustment step of discharge current	ENSAO = 0, SE = 0 ΔLSCUR[0:1] = 1		320	400	480	μA	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Charge current Pin SAO2	ENSAO = 0, SE = 1 LSCUR[0:1] = 3	I_{CHA}	-1.45	-1.2	-0.95	mA	
Discharge current Pin SAO2	ENSAO = 0, SE = 0 LSCUR[0:1] = 3	I_{DIS}	0.95	1.2	1.45	mA	
Microphone amplifier, $V_B = 5\text{ V}$, $V_{MIC} = 2\text{ mV}$, $V_{MIC3} = 2\text{ mV}$, $ENMIC = ENAM = I4O4 = 1$, $MICHF = 0$							
Gain MIC amp.: MIC1/2 → AMREC	MICG[0:1] = 0		18.6	19	19.4	dB	
	MICG[0:1] = 1		24.6	25	25.4	dB	
	MICG[0:1] = 2		30.6	31	31.4	dB	
	MICG[0:1] = 3		36.6	37	37.4	dB	
MIC3 → AMREC	MICHF = 1, MICG[0:1] = 3		36.6	37	37.4	dB	
Input suppression: MIC3 → MIC1/2	MICG[0:1] = 0, MICHF = 0		60			dB	
MIC1/2 → MIC3	MICHF = 1		60			dB	
Settling time offset-cancellers	5τ , FOFFC = 0				300	ms	
Settling time offset- cancellers in speed-up mode	5τ , FOFFC = 1				60	ms	
AGC for answering machine, AMPB → AMREC, $ENAM = ENAGC = I4O5 = I5O4 = 1$							
Nominal gain	$V_{AMPB} = 5\text{ mV}$		24	26	28	dB	
Max. output level	$V_{AMPB} = 50\text{ mV}$, $d < 5\%$		240	300	360	mVp	
Attack time	20 dB overdrive			2		ms	
Release time				45		ms	
Switching matrix, $V_L = 0$, $V_B = 5\text{ V}$, $ENAM = I4O4 = 1$, $V_{AMPB} = 1\text{ V}_{rms}$							
Input impedance AMPB			50	60	70	k Ω	
Gain AMPB → AMREC			-0.4	0	0.4	dB	
Max. input level AMPB					600	mV	
Max. output level AMREC					$V_B - 600\text{ mV}$	V_{PP}	
Offset	I4O4: 1 → 0	ΔV_{AMREC}			± 30	mV	
Mute switching matrix	I4O4 = 0		60			dB	
Power-on reset $V_L = 0$, $V_{MP} = 3.3\text{ V}$, $V_B = 5\text{ V}$, U4091 in power-down mode							
Power-on reset by VMP threshold, VL or VRING or ES high	$V_B = 4\text{ V}$, $ES = 4\text{ V}$, rise VMP	VMP_{on}	2.65	2.75	2.85	V	
Power-on reset by VB threshold, VL or VRING or ES high	$VMP = 3\text{ V}$, $ES = 3\text{ V}$, rise VB	VB_{on}		3.1		V	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Low-voltage interrupt VL = 0, V_{MP} = 3.3 V, V_B = 0 V							
VMP decreasing	Decrease VMP until INT returns to high	VLVI	2.5	2.6	2.7	V	
Power-off reset VL = 0, V_{MP} = 3.3 V, V_B = 0 V							
Low-voltage reset	Decrease VMP until RESET returns to low	VLVR	2.35	2.45	2.55	V	
Difference voltage between low-voltage interrupt and reset	VLVI – VLVR		100	150		mV	
Logical part V_{MP} = 3.3 V, V_B = 5 V							
Output impedance at OSCOUT			0.5		1.0	kΩ	
Pins SCL, SDA (input mode)	Low level High level		0.8 × V _{MP}		0.2 × V _{MP}	V V	
Input leakage current	0 < V _i < V _{MP}		-1		1	μA	
Pins INT, SDA (output mode)	Output low (resistance to GND)		220	310	400	Ω	
Switch for additional impedance (Pin IMPSW) V_{MP} = 3.3 V, V_B = 3 V							
Switch-off leakage current	0 < V _i < V _{MP} IMPSW = 0		-2		2	μA	
Resistance to GND	IMPSW = 1			30	50	Ω	
Max. current	IMPSW = 1		-5		5	mA	
AFS acoustic feedback suppression, I_L = 14 mA, V_{GEN} = 300 mV, ERX = ETX = ENMIC = ENSTBAL = I1O1 = I3O3 = 1, SL[0:1] = 0, LF[0:3] = 1, P[0:4] = 31, AGARX[0:2] = 0							
Adjustment range of attenuation	I _L ≥ 15 mA		0		50	dB	
Attenuation of transmit gain	I _L ≥ 15 mA, I _{INLDT} = 0 μA I _{INLDR} = 10 μA	ΔG _T	48	50	52	dB	
Attenuation of speaker amplifier	I _L ≥ 15 mA, I _{INLDT} = 10 μA I _{INLDR} = 0 μA	G _{SA}	48	50	52	dB	
Supply voltages, V_{MIC} = 25 mV, T_{amb} = -10 to +60°C							
V _{MP}	I _L = 14 mA, R _{DC} = 680 kΩ I _{MP} = 3 mA	V _{MP}	3.1	3.3	3.5	V	
V _{MPS}	I _L = 100 mA, R _{DC} = inf., I _{MP} = 0 mA	V _{MPS}			5.7	V	
V _{MIC}	I _L = 14 mA, R _{DC} = 1.3 MΩ I _M = 700 A	V _{MIC}	1.5		4	V	
V _B	I _B = +20 mA, I _L = 0 mA	V _B		5.5	6.3	V	
Ring power converter, IMP = 1 mA, IM = 0 R_{IMPA} = 500 kΩ							
Maximum output power	V _{RING} = 20.6 V ENSA = ENSAO = SE = 1	P _{SA}		20		mW	

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Fig.
Threshold	V _{RING} : high to low			4.5		V	
	low to high, RINGTH [0:3] = 0		6.3	7	7.7	V	
	low to high RINGTH [0:3] = 15		20	22	24	V	
Adjustment steps threshold	ΔRINGTH = 1		0.8	1	1.2	V	
Input impedance	V _{RING} = 30 V		4	5	6	kΩ	
Z-diode voltage	I _{RING} = 15 mA	V _{RINGmax}	30.8			V	
Serial bus SCL, SDA, AS, VMP = 3.3 V, RSDA = RSCL = RINT = 12 kΩ							
Input voltage HIGH LOW	SDA, SCL, INT	V _{iBUS}	3.0 0		V _{DD} 1.5	V V	
Output voltage Acknowledge LOW	SDA I _{SDA} = 3 mA	V _O			0.4	V	
Clock frequency	SCL	f _{SCL}			100	kHz	
Rise time SDA, SCL		t _r			1	μs	
Fall time SDA, SCL		t _f			300	ns	
Period of SCL HIGH LOW	HIGH	t _H	4.0			μs	
	LOW	t _L	4.7			μs	
Setup time							
Start condition Data		t _{sSTA} t _{sDAT}	4.7 250			μs ns	
Stop condition Time space ¹⁾		t _{sSTOP} t _{wSTA}	4.7 4.7			μs μs	
Hold time							
Start condition DATA		t _{hSTA} t _{hDAT}	4.0 0			μs μs	

¹⁾ This is a space of time where the bus must be from data transmission and before a new transmission can be started

Bus Timing

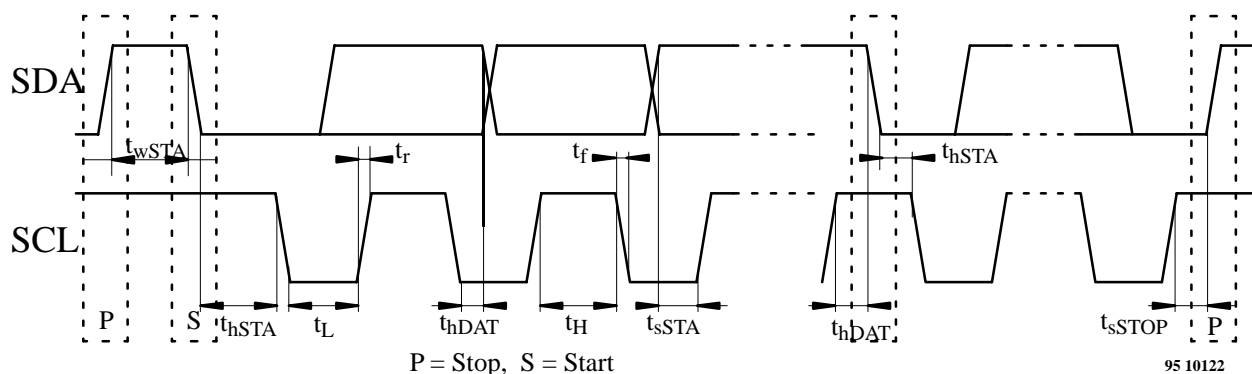


Figure 21. Bus timing diagram

Test Circuits

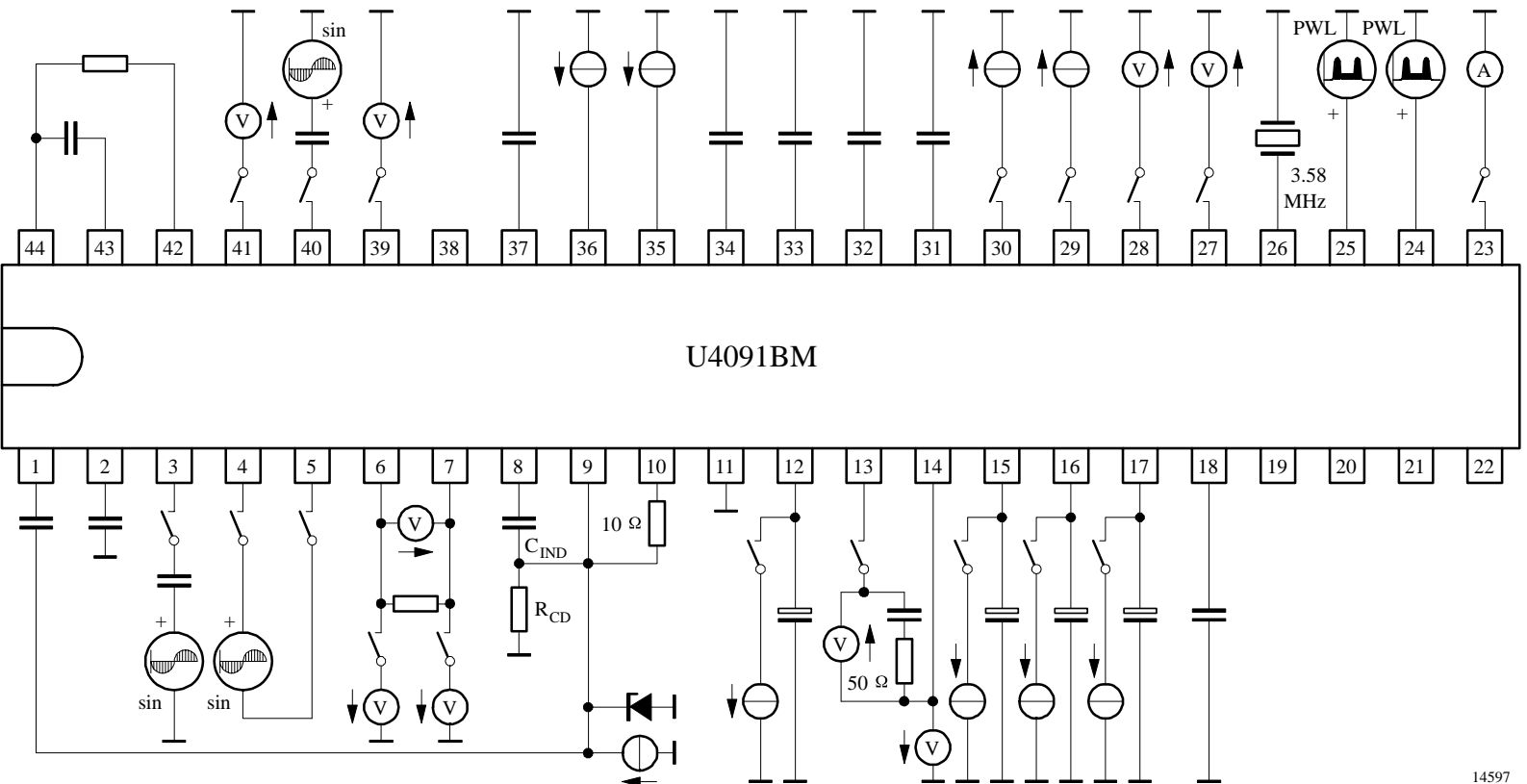


Figure 22. Basic test circuit

14597

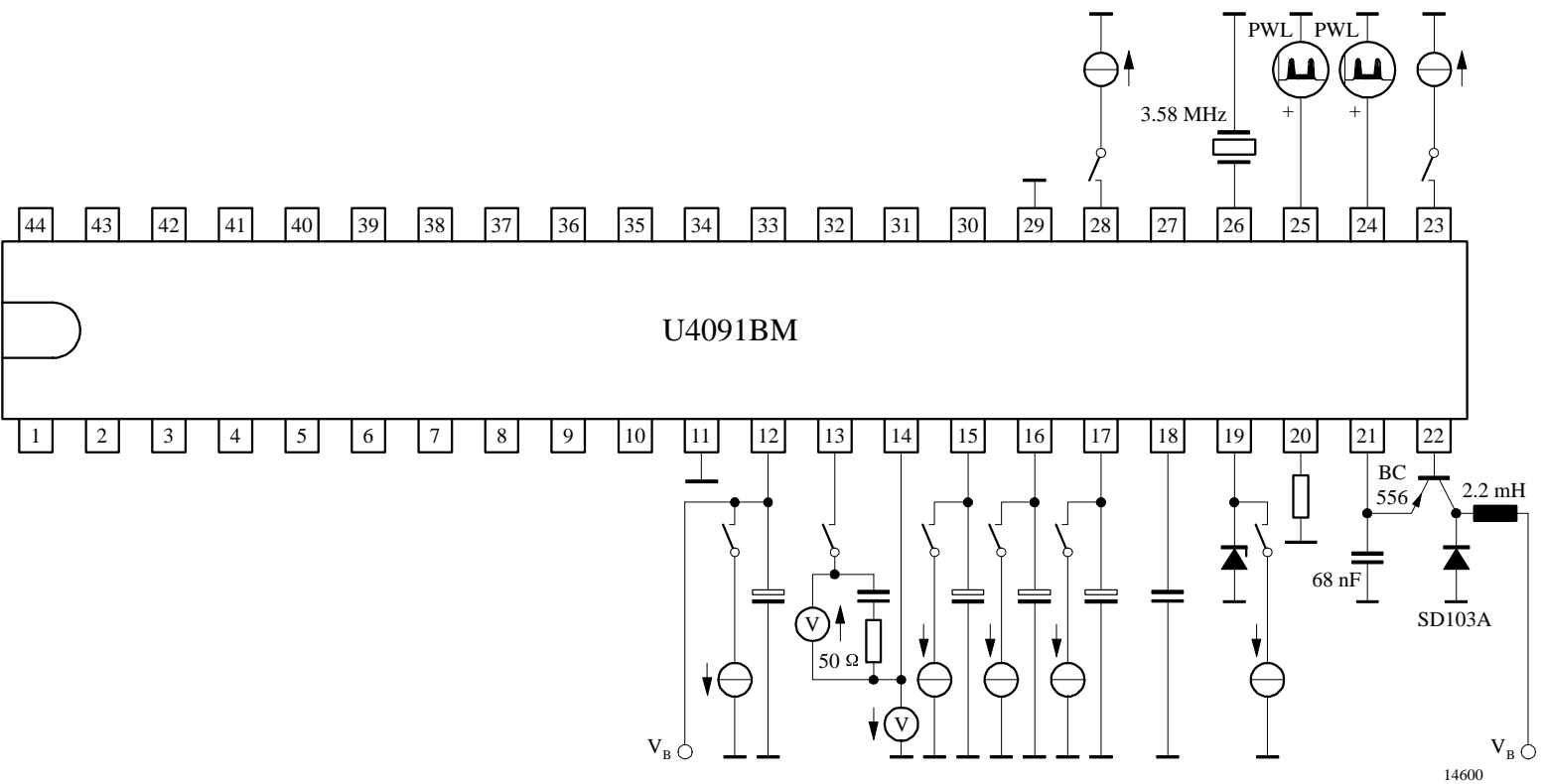
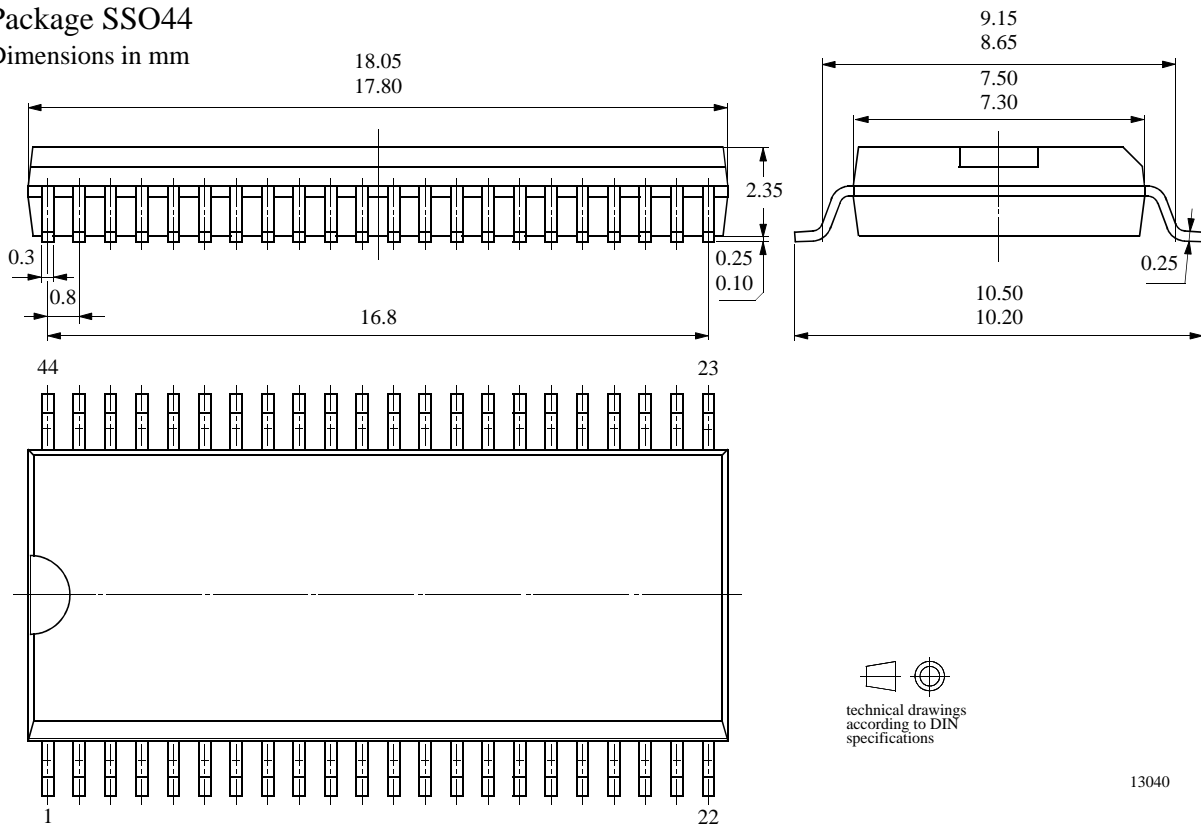


Figure 23. Test circuit for ringing

Package Information

Package SSO44

Dimensions in mm




technical drawings
according to DIN
specifications

13040

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423