monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Siliconix

Performance Curves NNT
See Section 4

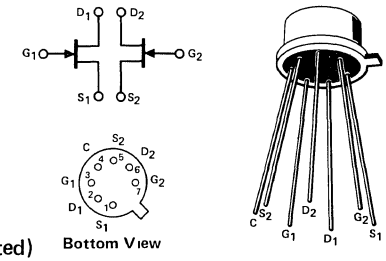
BENEFITS

- **High Input Impedance**
  I_G = 5 pA (U427)
- **High Gain g_{fs} = 120 μmho Minimum @**
  I_D = 30 μA
- **Low Power Supply Operation**
  $V_{GS(off)}$ = 2 V Maximum (U427)
- **Minimum System Error and Calibration**
  25 mV Maximum Offset

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U427 Min	U427 Typ	U427 Max	U428 Min	U428 Typ	U428 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 μA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = −1 μA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			5			10	pA	T = +25°C	V_{GS} = −20 V, V_{DS} = 0
						5			10	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			3			5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
						3			5	nA	T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2 0	−0.4		−3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			−1.8			−2.9	V	V_{DG} = 10 V, I_D = 30 μA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1500	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3 0			5.0	μ℧		
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5	pF		
12		g_{fs}	Common-Source Forward Transconductance	120		350	120		350	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			0 5			1 0	μ℧		
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz		f = 10 Hz
					10			10		nV/√Hz		f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			25			40	mV	V_{DG} = 10 V, I_D = 30 μA	
17		$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			40			80	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = −55°C, T_B = 25°C, T_C = 125°C	
18		CMRR	Common Mode Rejection Ratio (Note 3)		90			90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V	

NOTES
1 Approximately doubles for every 10°C increase in T_A
2 Measured at end points T_A, T_B and T_C
3 $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V
4 Case lead not connected

NNT