Not Recommended For New Designs

PowerStore 8K x 8 nvSRAM

Features

- High-performance CMOS non-volatile static RAM 8192 x 8 bits
- 25 ns Access Time
- 12 ns Output Enable Access Time
- I_{CC} = 15 mA at 200 ns Cycle Time
- Automatic STORE to EEPROM on Power Down using external capacitor
- Hardware or Software initiated STORE (STORE Cycle Time < 10 ms)
- Automatic STORE Timing
- 10^5 STORE cycles to EEPROM
- 10 years data retention in EEPROM
- Automatic RECALL on Power Up
- Software RECALL Initiation (RECALL Cycle Time < 20 µs)
- Unlimited RECALL cycles from EEPROM
- Single 5 V ± 10 % Operation
- Operating temperature ranges:
  - 0 to 70 °C
  - -40 to 85 °C
- QS 9000 Quality Standard
- ESD characterization according MIL STD 883C M3015.7-HB (classification see IC Code Numbers)
- RoHS compliance and Pb- free Package: SOP28 (330 mil)

Description

The U632H64 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U632H64 is a fast static RAM (25 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in an external 100 µF capacitor. Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on power up. The U632H64 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

STORE cycles also may be initiated under user control via a software sequence or via a single pin (HSB).

Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

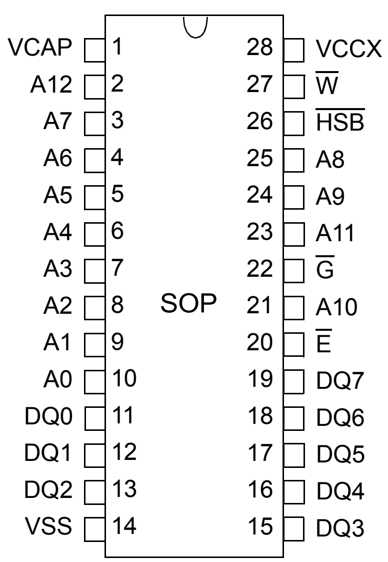
Because a sequence of addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted.

RECALL cycles may also be initiated by a software sequence.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

Pin Configuration

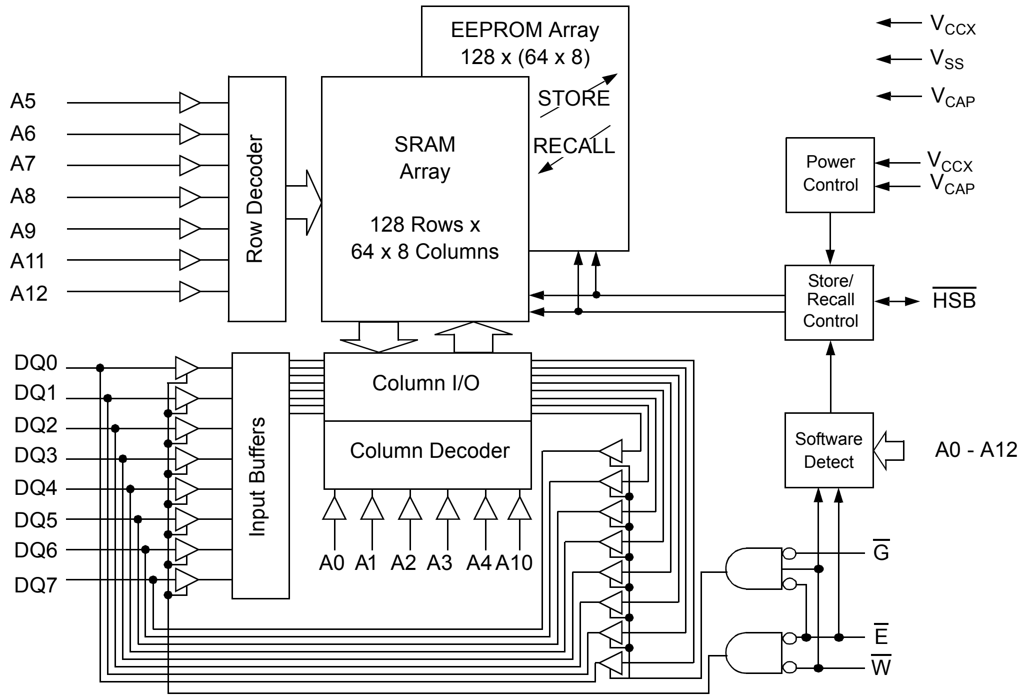


Top View

Pin Description

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCCX	Power Supply Voltage
VSS	Ground
VCAP	Capacitor
$\overline{HSB}$	Hardware Controlled Store/Busy

Block Diagram



Truth Table for SRAM Operations

Operating Mode	$\overline{E}$	$\overline{HSB}$	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	H	H	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V,
with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ± 200 mV from steady-state voltage.

Absolute Maximum Ratings[a]		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.5	7	V
Input Voltage		V_I	-0.3	V_{CC}+0.5	V
Output Voltage		V_O	-0.3	V_{CC}+0.5	V
Power Dissipation		P_D		1	W
Operating Temperature	C-Type K-Type	T_a	0 -40	70 85	°C °C
Storage Temperature		T_{stg}	-65	150	°C

a: Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage[b]	V_{CC}		4.5	5.5	V
Input Low Voltage	V_{IL}	-2 V at Pulse Width 10 ns permitted	-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	V

DC Characteristics	Symbol	Conditions	C-Type		K-Type		Unit
			Min.	Max.	Min.	Max.	
Operating Supply Current[c]	I_{CC1}	V_{CC} = 5.5 V V_{IL} = 0.8 V V_{IH} = 2.2 V t_c = 25 ns		90		95	mA
Average Supply Current during STORE[c]	I_{CC2}	V_{CC} = 5.5 V $\overline{E}$ ≤ 0.2 V $\overline{W}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		6		7	mA
Average Supply Current during *PowerStore* Cycle	I_{CC4}	V_{CC} = 4.5 V V_{IL} = 0.2 V V_{IH} ≥ V_{CC}-0.2 V		4		4	mA
Standby Supply Current[d] (Cycling TTL Input Levels)	$I_{CC(SB)1}$	V_{CC} = 5.5 V $\overline{E}$ = V_{IH} t_c = 25 ns		30		34	mA
Operating Supply Current at t_{cR} = 200 ns[c] (Cycling CMOS Input Levels)	I_{CC3}	V_{CC} = 5.5 V $\overline{W}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		15		15	mA
Standby Supply Current[d] (Stable CMOS Input Levels)	$I_{CC(SB)}$	V_{CC} = 5.5 V $\overline{E}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		3		3	mA

b: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

c: I_{CC1} and I_{CC3} are depedent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
The current I_{CC1} is measured for WRITE/READ - ratio of 1/2.
I_{CC2} is the average current required for the duration of the STORE cycle (STORE Cycle Time).

d: Bringing $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table. The current $I_{CC(SB)1}$ is measured for WRITE/READ - ratio of 1/2.

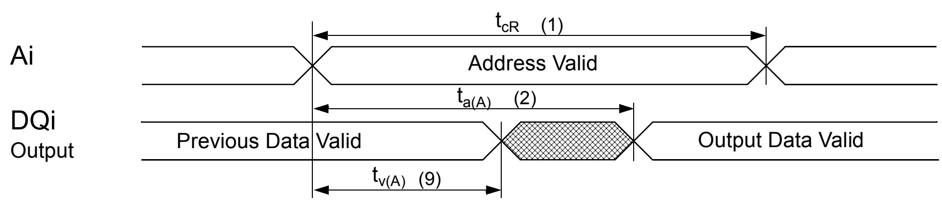
DC Characteristics	Symbol	Conditions	C-Type		K-Type		Unit
			Min.	Max.	Min.	Max.	
Output High Voltage Output Low Voltage	V_{OH} V_{OL}	V_{CC} = 4.5 V I_{OH} =-4 mA I_{OL} = 8 mA	2.4	 0.4	2.4	 0.4	V V
Output High Current Output Low Current	I_{OH} I_{OL}	V_{CC} = 4.5 V V_{OH} = 2.4 V V_{OL} = 0.4 V	 8	-4	 8	-4	mA mA
Input Leakage Current High Low	 I_{IH} I_{IL}	V_{CC} = 5.5 V V_{IH} = 5.5 V V_{IL} = 0 V	 -1	 1	 -1	 1	 µA µA
Output Leakage Current High at Three-State- Output Low at Three-State- Output	 I_{OHZ} I_{OLZ}	V_{CC} = 5.5 V V_{OH} = 5.5 V V_{OL} = 0 V	 -1	 1	 -1	 1	 µA µA

SRAM Memory Operations

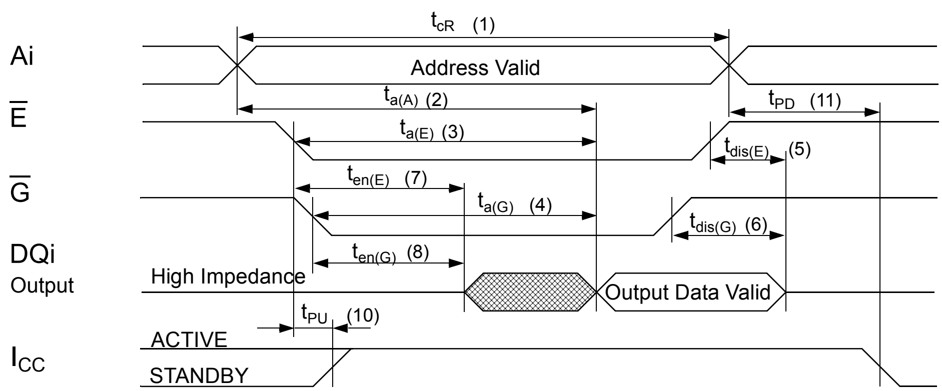
No.	Switching Characteristics Read Cycle	Symbol				Unit
		Alt.	IEC	Min.	Max.	
1	Read Cycle Time[f]	t_{AVAV}	t_{cR}	25		ns
2	Address Access Time to Data Valid[g]	t_{AVQV}	$t_{a(A)}$		25	ns
3	Chip Enable Access Time to Data Valid	t_{ELQV}	$t_{a(E)}$		25	ns
4	Output Enable Access Time to Data Valid	t_{GLQV}	$t_{a(G)}$		12	ns
5	$\overline{E}$ HIGH to Output in High-Z[h]	t_{EHQZ}	$t_{dis(E)}$		13	ns
6	$\overline{G}$ HIGH to Output in High-Z[h]	t_{GHQZ}	$t_{dis(G)}$		13	ns
7	$\overline{E}$ LOW to Output in Low-Z	t_{ELQX}	$t_{en(E)}$	5		ns
8	$\overline{G}$ LOW to Output in Low-Z	t_{GLQX}	$t_{en(G)}$	0		ns
9	Output Hold Time after Address Change	t_{AXQX}	$t_{v(A)}$	3		ns
10	Chip Enable to Power Active[e]	t_{ELICCH}	t_{PU}	0		ns
11	Chip Disable to Power Standby[d, e]	t_{EHICCL}	t_{PD}		25	ns

e: Parameter guaranteed but not tested.
f: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both LOW.
g: Address valid prior to or coincident with $\overline{E}$ transition LOW.
h: Measured ± 200 mV from steady state output voltage.

Read Cycle 1: Ai-controlled (during Read cycle: $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)[f]

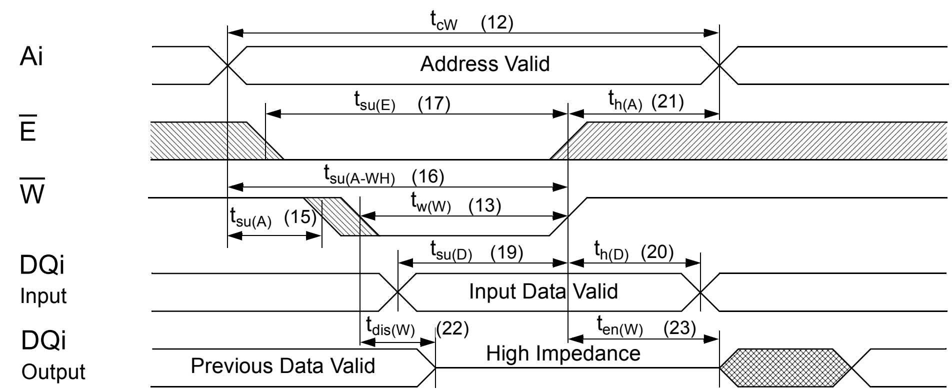


Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read cycle: $\overline{W} = V_{IH}$)[g]

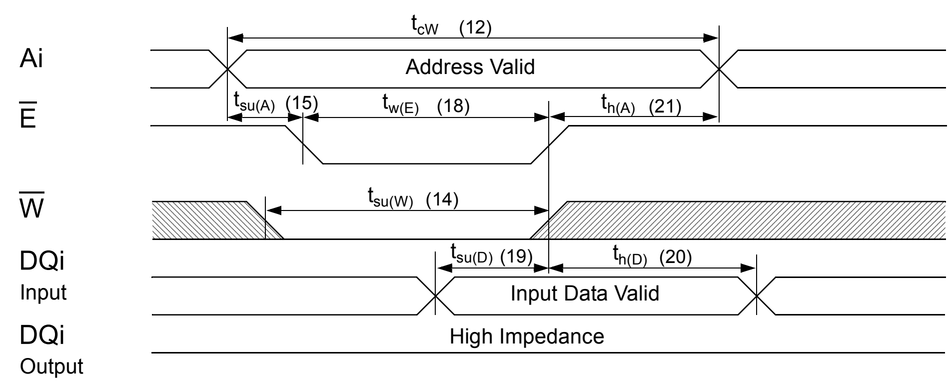


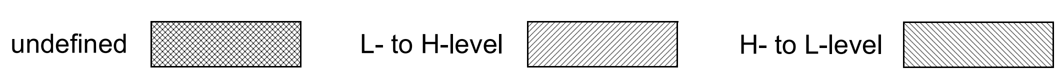
No.	Switching Characteristics Write Cycle	Symbol					Unit
		Alt. #1	Alt. #2	IEC	Min.	Max.	
12	Write Cycle Time	t_{AVAV}	t_{AVAV}	t_{cW}	25		ns
13	Write Pulse Width	t_{WLWH}		$t_{w(W)}$	20		ns
14	Write Pulse Width Setup Time		t_{WLEH}	$t_{su(W)}$	20		ns
15	Address Setup Time	t_{AVWL}	t_{AVEL}	$t_{su(A)}$	0		ns
16	Address Valid to End of Write	t_{AVWH}	t_{AVEH}	$t_{su(A-WH)}$	20		ns
17	Chip Enable Setup Time	t_{ELWH}		$t_{su(E)}$	20		ns
18	Chip Enable to End of Write		t_{ELEH}	$t_{w(E)}$	20		ns
19	Data Setup Time to End of Write	t_{DVWH}	t_{DVEH}	$t_{su(D)}$	12		ns
20	Data Hold Time after End of Write	t_{WHDX}	t_{EHDX}	$t_{h(D)}$	0		ns
21	Address Hold after End of Write	t_{WHAX}	t_{EHAX}	$t_{h(A)}$	0		ns
22	$\overline{W}$ LOW to Output in High-Z[h, i]	t_{WLQZ}		$t_{dis(W)}$		10	ns
23	$\overline{W}$ HIGH to Output in Low-Z	t_{WHQX}		$t_{en(W)}$	5		ns

Write Cycle #1: $\overline{W}$-controlled[j]



Write Cycle #2: $\overline{E}$-controlled[j]





i: If $\overline{W}$ is LOW and when $\overline{E}$ goes LOW, the outputs remain in the high impedance state.
j: $\overline{E}$ or $\overline{W}$ must be V_{IH} during address transition.

Nonvolatile Memory Operations

Mode Selection

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A12 - A0 (hex)	Mode	I/O	Power	Notes
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	l
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
X	X	L	X	STORE/Inhibit	Output High Z	I_{CC2}/Standby	m

k: The six consecutive addresses must be in order listed (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a Store cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.
The following six-address sequence is used for testing purposes and should not be used: 0000, 1555, 0AAA, 1FFF, 10F0, 139C.

l: I/O state assumes that $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on the state of $\overline{G}$.

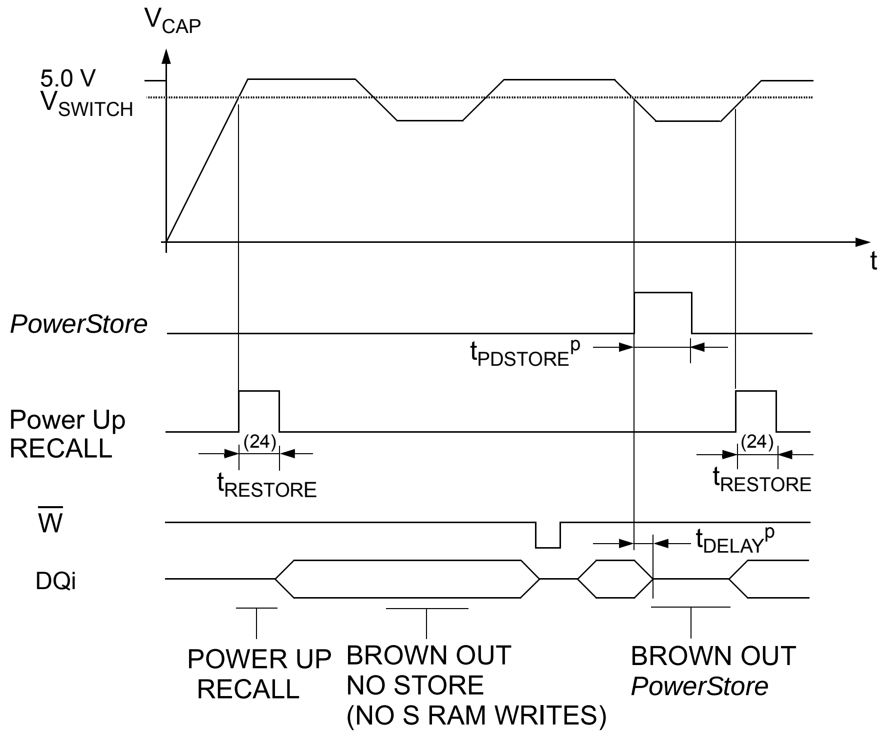
m: $\overline{HSB}$ initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until $\overline{HSB}$ rises.

No.	*PowerStore* Power Up RECALL/ Hardware Controlled STORE	Symbol		Conditions	Min.	Max.	Unit
		Alt.	IEC				
24	Power Up RECALL Duration[n, e]	$t_{RESTORE}$				650	µs
25	STORE Cycle Duration	t_{HLQX}	$t_{d(H)S}$	$V_{CC} \geq 4.5$ V		10	ms
26	$\overline{HSB}$ Low to Inhibit On[e]	t_{HLQZ}	$t_{dis(H)S}$		1		µs
27	$\overline{HSB}$ High to Inhibit Off[e]	t_{HHQX}	$t_{en(H)S}$			700	ns
28	External STORE Pulse Width[e]	t_{HLHX}	$t_{w(H)S}$		250		ns
	$\overline{HSB}$ Output Low Current[e, o]	$I_{\overline{HSB}OL}$		$\overline{HSB} = V_{OL}$	3		mA
	$\overline{HSB}$ Output High Current[e, o]	$I_{\overline{HSB}OH}$		$\overline{HSB} = V_{IL}$	5	60	µA
	Low Voltage Trigger Level	V_{SWITCH}			4.0	4.5	V

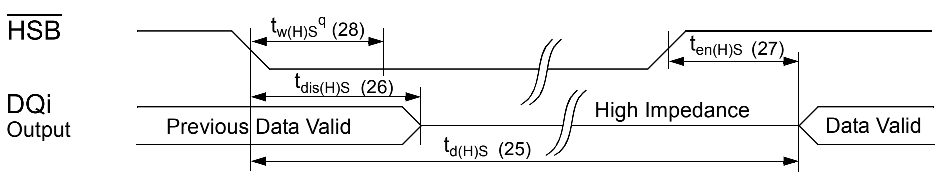
n: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

o: $\overline{HSB}$ is an I/O that has a week internal pullup; it is basically an open drain output. It is meant to allow up to 32 U632H64 to be ganged together for simultaneous storing. Do not use $\overline{HSB}$ to pullup any external circuitry other than other U632H64 $\overline{HSB}$ pins.

PowerStore and automatic Power Up RECALL



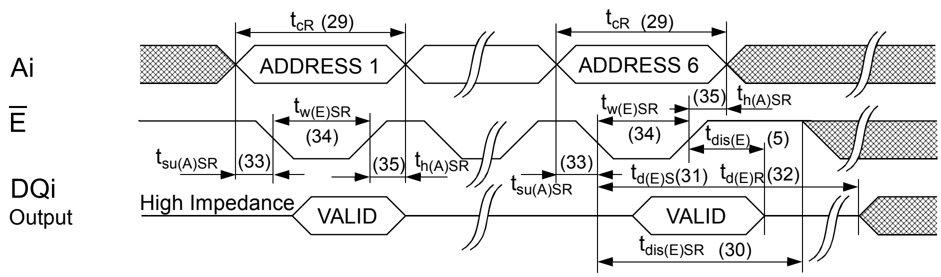
Hardware Controlled STORE



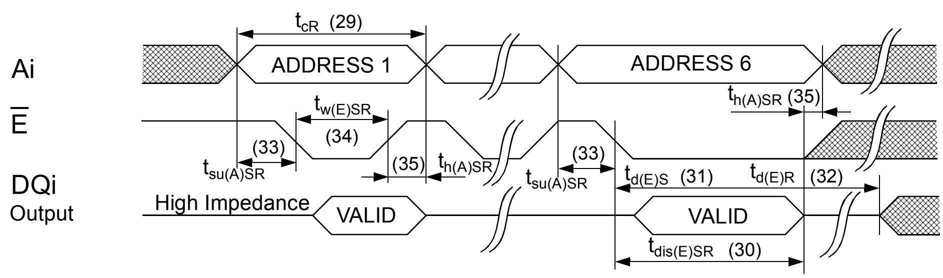
No.	Software Controlled STORE/ RECALL Cycle	Symbol		Min.	Max.	Unit
		Alt.	IEC			
29	STORE/RECALL Initiation Time	t_{AVAV}	t_{cR}	25		ns
30	Chip Enable to Output Inactive[s]	t_{ELQZ}	$t_{dis(E)SR}$		600	ns
31	STORE Cycle Time	t_{ELQXS}	$t_{d(E)S}$		10	ms
32	RECALL Cycle Time[r]	t_{ELQXR}	$t_{d(E)R}$		20	µs
33	Address Setup to Chip Enable	t_{AVELN}	$t_{su(A)SR}$	0		ns
34	Chip Enable Pulse Width[s, t]	t_{ELEHN}	$t_{w(E)SR}$	20		ns
35	Chip Disable to Address Change	t_{EHAXN}	$t_{h(A)SR}$	0		ns

p: $t_{PDSTORE}$ approximate $t_{d(E)S}$ or $t_{d(H)S}$; t_{DELAY} approximate $t_{dis(H)S}$.
q: After $t_{w(H)S}$ HSB is hold down internal by STORE operation.
r: An automatic RECALL also takes place at power up, starting when V_{CC} exceeds V_{SWITCH} and takes $t_{RESTORE}$. V_{CC} must not drop below V_{SWITCH} once it has been exceeded for the RECALL to function properly.
s: Once the software controlled STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
t: Noise on the E pin may trigger multiple READ cycles from the same address and abort the address sequence.

Software Controlled STORE/RECALL Cycle[t, u, v, w] ($\overline{E}$ = HIGH after STORE initiation)



Software Controlled STORE/RECALL Cycle[t, u, v, w] ($\overline{E}$ = LOW after STORE initiation)

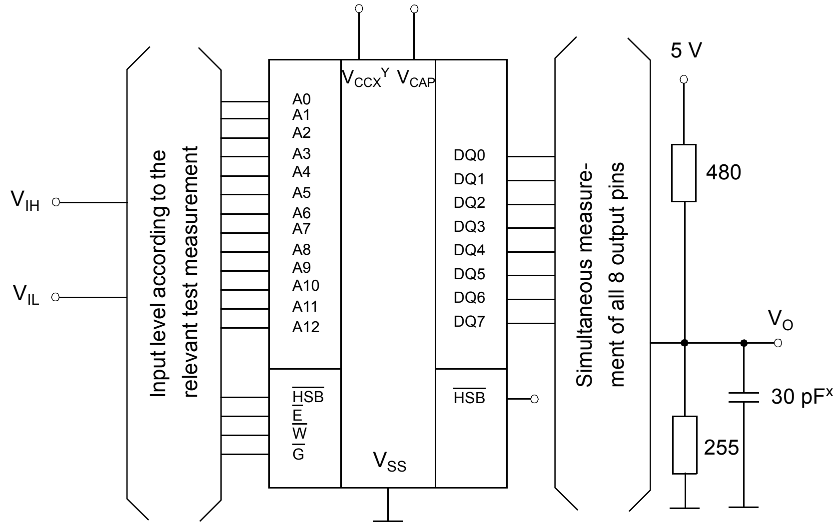


u: If the chip enable pulse width is less then $t_{a(E)}$ (see READ cycle) but greater than or equal to $t_{w(E)SR}$, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

v: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses 1 through 6 are found in the mode selection table. Address 6 determines whether the U632H64 performs a STORE or RECALL.

w: $\overline{E}$ must be used to clock in the address sequence for the Software controlled STORE and RECALL cycles.

Test Configuration for Functional Check



x: In measurement of t_{dis}-times and t_{en}-times the capacitance is 5 pF.

y: Between V_{CC} and V_{SS} must be connected a high frequency bypass capacitor 0.1 µF to avoid disturbances.

Capacitance[e]	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 5.0 V, V_I = V_{SS}, f = 1 MHz, T_a = 25 °C	C_I		8	pF
Output Capacitance		C_O		7	pF

All pins not under test must be connected with ground by capacitors.

Ordering Code

Example **U632H64** ___ **S** **C** **25** **G1**

Type

ESD Class
blank > 2000 V
B > 1000 V

Package
S2 = SOP28 (330 mil) Type 2

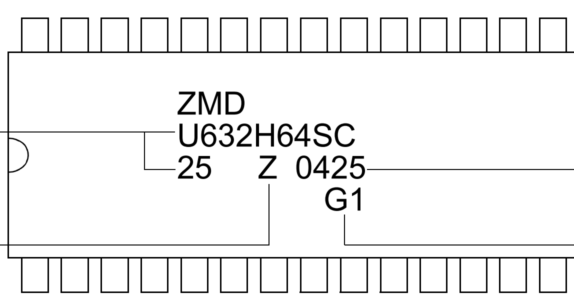
Operating Temperature Range
C = 0 to 70 °C
K = -40 to 85 °C

Access Time
25 = 25 ns

Leadfree Option
G1 = Leadfree Green Package

Device Marking (example)

Product specification



Date of manufacture (The first 2 digits indicating the year, and the last 2 digits the calendar week.)

Internal Code

Leadfree Green Package

Device Operation

The U632H64 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.
STORE cycles may be initiated under user control via a software sequence or $\overline{HSB}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH}. RECALL operations are automatically initiated upon power up and may occur also when V_{CCX} rises above V_{SWITCH} after a low power condition. RECALL cycles may also be initiated by a software sequence.

SRAM READ

The U632H64 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{HSB}$ and $\overline{W}$ are HIGH. The address specified on pins A0 - A12 determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{cR}. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at $t_{a(E)}$ or at $t_{a(G)}$, whichever is later. The data outputs will repeatedly respond to address changes within the t_{cR} access time without the need for transition on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{HSB}$ is brought LOW.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes HIGH at the end of the cycle. The data on pins DQ0 - 7 will be written into the memory if it is valid $t_{su(D)}$ before the end of a $\overline{W}$ controlled WRITE or $t_{su(D)}$ before the end of an $\overline{E}$ controlled WRITE.
It is recommended that $\overline{G}$ is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers $t_{dis(W)}$ after $\overline{W}$ goes LOW.

Automatic STORE

During normal operation, the U632H64 will draw current from V_{CCX} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CCX} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 1 shows the proper connection of capacitors for automatic STORE operation. The charge storage capacitor should have a capacity of 100 µF (± 20 %) at 6 V. Each U632H64 must have its own 100 µF capacitor. Each U632H64 must have a high quality, high frequency bypass capacitor of 0.1 µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. This capactior do not replace the normal expected high frequency bypass capacitor between the power supply voltage and V_{SS}.
In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving $\overline{HSB}$ LOW will be ignored unless at least one WRITE operation has taken place since the most recent STORE cycle. Note that if $\overline{HSB}$ is driven LOW via external circuitry and no WRITEs have taken place, the part will still be disabled until $\overline{HSB}$ is allowed to return HIGH. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

Automatic RECALL

During power up an automatic RECALL takes place. At a low power condition (power supply voltage < V_{SWITCH}) an internal RECALL request may be latched. As soon as power supply voltage exceeds again the sense voltage of V_{SWITCH}, a requested RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.
If the U632H64 is in a WRITE state at the end of a power up RECALL, the SRAM data will be corrupted.
To help avoid this situation, a 10 KΩ resistor should be connected between $\overline{W}$ and power supply voltage.

Software Nonvolatile STORE

The U632H64 software controlled STORE cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the U632H64 implements nonvolatile operation while remaining compatible with standard 8K x 8 SRAMs. During the STORE cycle, an erase of the previous nonvolatile data is performed first, followed by parallel programming of all nonvolatile elements. Once a STORE cycle is initiated, further inputs and outputs are disabled until the cycle is completed.
Because a sequence of addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted.
To initiate the STORE cycle the following READ sequence must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0F (hex) Initiate STORE

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles are used in the sequence, although it is not necessary that G is LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Sorftware Nonvolatile RECALL

A RECALL cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0E (hex) Initiate RECALL

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

HSB Nonvolatile STORE

The hardware controlled STORE Busy pin (HSB) is connected to an open drain circuit acting as both input and output to perform two different functions. When driven LOW by the internal chip circuitry it indicates that a STORE operation (initiated via any means) is in progress within the chip. When driven LOW by external circuitry for longer than $t_{w(H)S}$, the chip will conditionally initiate a STORE operation after $t_{dis(H)S}$.

READ and WRITE operations that are in progress when HSB is driven LOW (either by internal or external circuitry) will be allowed to complete before the STORE operation is performed, in the following manner.

After HSB goes LOW, the part will continue normal SRAM operation for $t_{dis(H)S}$. During $t_{dis(H)S}$, a transition on any address or control signal will terminate SRAM operation and cause the STORE to commence.

Note that if an SRAM WRITE is attempted after HSB has been forced LOW, the WRITE will not occur and the STORE operation will begin immediately. HARDWARE-STORE-BUSY (HSB) is a high speed, low drive capability bidirectional control line.

In order to allow a bank of U632H64s to perform synchronized STORE functions, the HSB pin from a number of chips may be connected together. Each chip contains a small internal current source to pull HSB HIGH when it is not being driven LOW. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to power supply via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\overline{HSB}OL}$ at V_{OL} (see Figure 1 and 2).

Only if HSB is to be connected to external circuits, an external pull-up resistor should be used.

During any STORE operation, regardless of how it was initiated, the U632H64 will continue to drive the HSB pin LOW, releasing it only when the STORE is complete.

Upon completion of a STORE operation, the part will be disabled until HSB actually goes HIGH.

Hardware Protection

The U632H64 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$, all software or HSB initiated STORE operations will be inhibited.

Preventing Automatic STORES

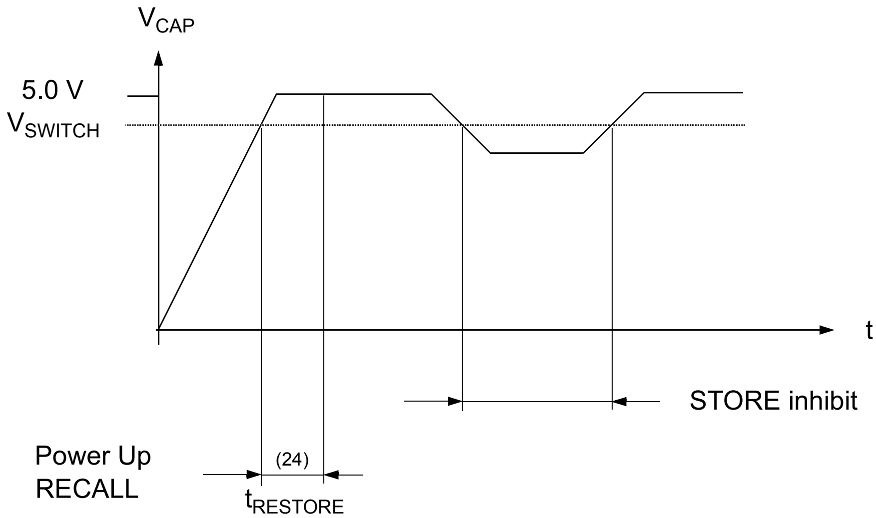
The *PowerStore* function can be disabled on the fly by holding HSB HIGH with a driver capable of sourcing 15 mA at V_{OH} of at least 2.2 V as it will have to overpower the internal pull-down device that drives HSB LOW at the onset of an *PowerStore* for 50 ns.

When the U632H64 is connected for *PowerStore* operation (see Figure 1) and V_{CCX} crosses V_{SWITCH} on the way down, the U632H64 will attempt to pull HSB LOW; if HSB does not actually get below V_{IL}, the part will stop trying to pull HSB LOW and abort the *PowerStore* attempt.

Disabling Automatic STORES

If the *PowerStore* function is not required, then V_{CAP} should be tied directly to the power supply and V_{CCX} should by tied to ground. In this mode, STORE operation may be triggered through software control or the HSB pin. In either event, V_{CAP} (Pin 1) must always have a proper bypass capacitor connected to it (Figure 2).

Disabling Automatic STORES: STORE Cycle Inhibit and Automatic Power Up RECALL



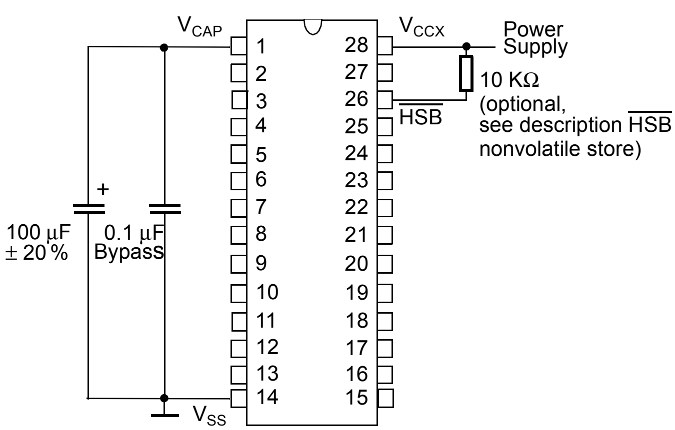


Figure 1: Automatic STORE Operation
Schematic Diagram

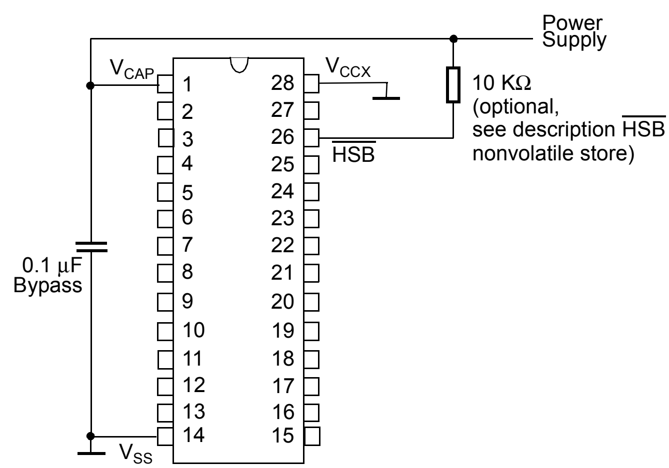


Figure 2: Disabling Automatic STORES
Schematic Diagram

Low Average Active Power

The U632H64 has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 55 ns.
When $\overline{E}$ is HIGH the chip consumes only standby current.
The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. the time during which the chip is disabled ($\overline{E}$ HIGH)
3. the cycle time for accesses ($\overline{E}$ LOW)
4. the ratio of READs to WRITEs
5. the operating temperature
6. the power supply voltage level

LIFE SUPPORT POLICY

SIMTEK products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SIMTEK product could create a situation where personal injury or death may occur.
Components used in life-support devices or systems must be expressly authorized by SIMTEK for such purpose.

LIMITED WARRANTY

The information in this document has been carefully checked and is believed to be reliable. However SIMTEK Corporation (SIMTEK) makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it. The information in this document describes the type of component and shall not be considered as assured characteristics.
SIMTEK does not guarantee that the use of any information contained herein will not infringe upon the patent, trademark, copyright, mask work right or other rights of third parties, and no patent or licence is implied hereby. This document does not in any way extent SIMTEK's warranty on any product beyond that set forth in its standard terms and conditions of sale.
SIMTEK reserves terms of delivery and reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.

Simtek Corporation
4250 Buckingham Drive suite 100 • Colorado Springs, CO 80907 • USA
Phone: +(800)637-1667 • Fax: +(719)531-9481 • Email: information@simtek.com • http://www.simtek.com

Change record

Date/Rev	Name	Change
01.11.2001	Ivonne Steffens	format revision and release for “Memory CD 2002“
22.04.2002	Thomas Wolf Matthias Schniebel	removing “at least“ for the 100 µF capacitor on page 11 (Automatic STORE)
25.09.2002	Matthias Schniebel	adding “Type 1“ to SOP28 (330 mil)
02.02.2004	Matthias Schniebel	10^6 STORE cycles / 100 years data retention
20.04.2004	Matthias Schniebel	adding “Leadfree Green Package“ to ordering information adding “Device Marking“
7.4.2005	Stefan Günther	adding RoHS compliance and Pb- free, S2 for chippack and PDIP28 (300 mil) deleted
31.03.2006	Simtek	Assigned Simtek Document Control Number
15.08.2006	Simtek	Moved Product to End of Life Status