

Features

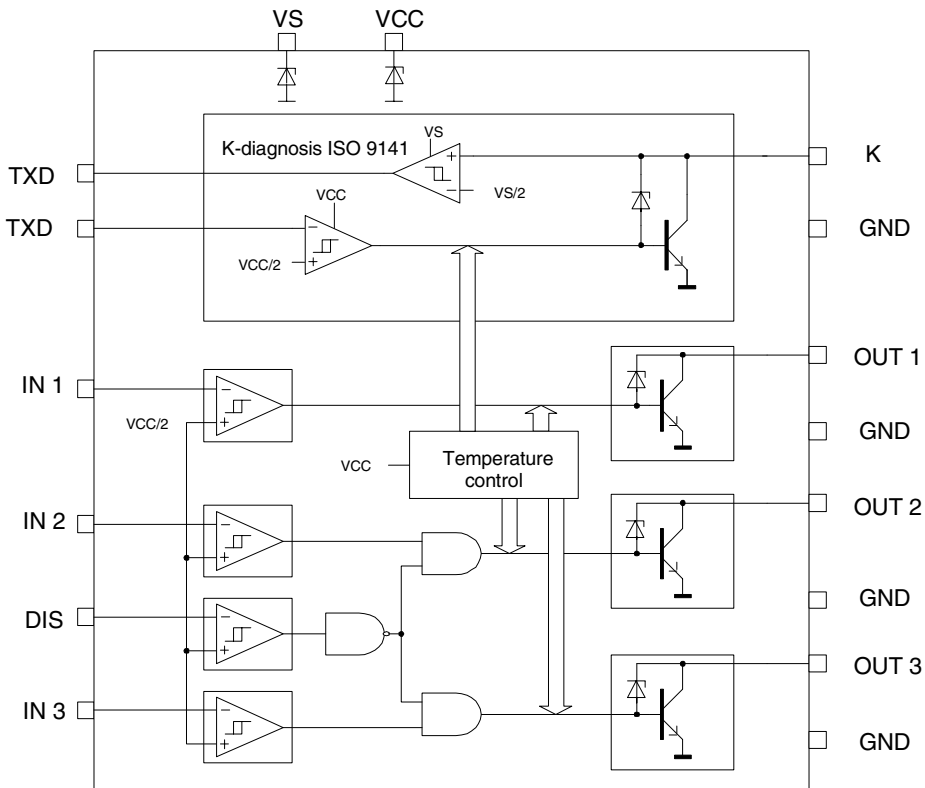
- Wide Power Supply Voltage Range
- Short-circuit Protected K-interface, ISO9141 Compatible
- Three Short-circuit Protected 40-mA Open-collector Buffers
- All Low-power Outputs with Built-in 28-V Clamping
- CMOS Compatible Digital Inputs with Hysteresis
- Digital 1-mA Push-pull "RxD" K-line Output
- Channel-specific Over-temperature Switch Off in Event of Short Circuit
- Load-dump Protection and Interference Protection
According to ISO 7637-1/4 (DIN 40839)

Description

The U6812B is a bipolar monolithic K-line bus transceiver designed to provide bi-directional serial communication in automotive diagnostic applications. The standard K-line is ISO 9141 compatible for baud rates up to 250 kBaud.

The IC provides three universally applicable 40-mA open-collector buffers, that can be used for signal decoupling. The U6812B is manufactured using Atmel's bipolar process and fully complies to automotive industry specifications. The U6812B provides an ideal grouping of SO-packaged low-power drivers, thus meeting customers' demand for space-saving and cost-effective circuit board assembly.

Figure 1. Block Diagram



Single-ended Bus Transceiver with Triple Buffer

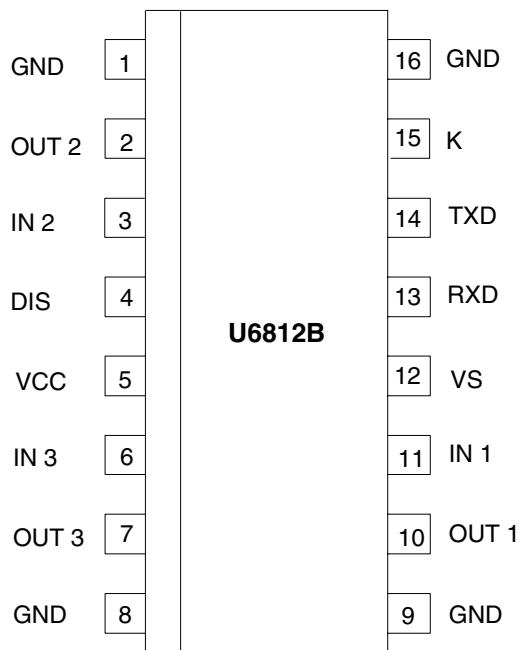
U6812B

Rev. 4760A-AUTO-10/03



Pin Configuration

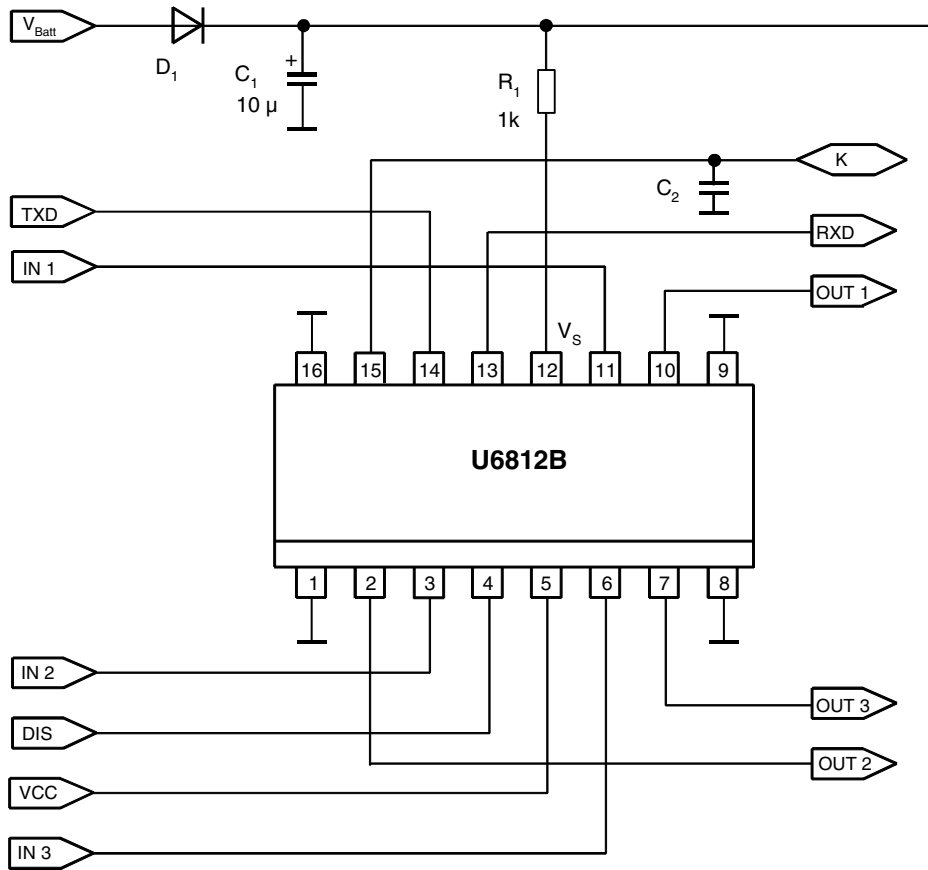
Figure 2. Pinning SO16



Pin Description

| Pin | Symbol | Type | Function |
|-----|--------|----------------------------|--|
| 1 | GND | Supply | Ground; all ground pins are directly connected to the lead frame |
| 2 | OUT 2 | Open-collector output | Protected output of driver 2 (faced to: outside) |
| 3 | IN 2 | Digital input | Input of protected driver 2 (faced to: μ P) |
| 4 | DIS | Digital input | Disable input for OUT 2 and OUT 3, "H"=enable, "L"=disable |
| 5 | VCC | Supply | +5-V supply |
| 6 | IN 3 | Digital input | Input of protected driver 3 (faced to: μ P) |
| 7 | OUT 3 | Open-collector output | Protected output of driver 3 (faced to: outside) |
| 8 | GND | Supply | Ground |
| 9 | GND | Supply | Ground |
| 10 | OUT 1 | Open-collector output | Protected output of driver 1 (faced to: outside) |
| 11 | IN 1 | Digital input | Input of protected driver 1 (faced to: μ P) |
| 12 | VS | Supply/reference | +12-V reference for K-line level |
| 13 | RXD | Digital output | Diagnosis receive line (faced to: μ P) |
| 14 | TXD | Digital input | Diagnosis transmit line (faced to: μ P) |
| 15 | K | 12-V input and O.C. output | Bi-directional diagnosis line (faced to: outside) |
| 16 | GND | Supply | Ground |

Figure 3. Basic Application Circuit



Functional Description

K-interface

The K-interface is equipped with a 40-mA open-collector driver. The current is determined by the external pull-up resistor. The saturation voltage is below 0.6 V.

The open-collector output is protected by a 28-V Z-diode. The collector current is permanently monitored for short circuits via a built-in shunt. In the event of a short circuit occurring at V_{Batt} , the collector current is held at approximately $I_{creg} = 80$ mA; the chip temperature then rises due to power loss. This status is maintained until the detection of overtemperature which causes the K-line output to be disabled and stored to memory. The internal short-circuit detection threshold is $I_{sc} > 0.8 \times I_{creg}$. The output remains disabled until a falling edge of a pulse is available to its input. Any further attempt to connect while the short circuit is still present causes the above sequence to be repeated. The output can be activated normally once the short circuit has been removed. The maximum baud rate is 250 kbaud.

The K-line allows bi-directional communication with the microcontroller. When the output K is disabled, information can be transferred to the processor via the input comparator at pin RxD.

The digital output RxD is a push-pull output stage with a driver power of 1 mA.

In the event of a line break at the K-line, the output K is connected to GND via the built-in 85-k Ω pull-down resistor, thus allowing the microcontroller to detect this fault. The maximum sampling frequency is 250 kbaud.

Open-collector Driver OUTx

The outputs are designed for a maximum static current of 40 mA, which is determined by the external pull-up resistor. The saturation voltage is below 0.6 V.

The three OUTx-driver outputs are activated with "active low" at the corresponding input. Outputs OUT2 and OUT3 can also be disabled with "active low" at the disable input, regardless of their input signal. The outputs are released by an open disable input or by using high potential.

The open-collector outputs are connected to a 28-V Z-diode. The collector current is permanently monitored via a built-in shunt circuit to permit the detection of short circuits. If a short circuit occurs at V_{Batt} , the collector current is held at approximately $I_{creg} = 80$ mA; accompanied with a rise of chip temperature due to power loss. This status is maintained until the detection of overtemperature which causes the output affected by the short circuit to be selectively disabled and stored to memory. The internal short-circuit detection threshold is $I_{sc} > 0.8 \times I_{creg}$. The affected output remains disabled until a falling edge of a pulse is available to its input. Any further attempt to connect while the short circuit is still present causes the above sequence to be repeated. The output can be activated normally once the short circuit has been removed.

Power Supply

The IC must be equipped with external RC circuitry to limit the voltage in the event of power surges (see Figure 3 on page 3). This prevents the circuit from being damaged or destroyed, and provides a buffer in case of power fluctuations at V_{Batt} . The RxD comparator is powered via pin V_S , producing its reference voltage of $1/2 V_S$, while all other blocks are supplied via V_{CC} .

The operating voltage can vary between $V_S = 7$ V and 26 V. The resistor R_1 at pin V_S limits the current via the built-in 28-V Z-diode between V_S and GND.

Application Note

It is recommended to use the external components as shown in Figure 3 on page 3 with the reverse battery protection diode D_1 and the buffer capacitor $C_1 = 10 \mu\text{F}$.

Digital Inputs (DIS, IN 1, IN 2, IN 3 and TxD)

The digital inputs are CMOS-compatible and equipped with a built-in pull-up resistor with a typical rating of $85 \text{ k}\Omega$ to V_{CC} . The input threshold totals $V_{\text{TH}} = 0.57 \times V_{\text{CC}}$ with a typical hysteresis of 100 mV . The inputs are designed for an input voltage of -0.2 V to $V_{\text{CC}} + 0.6 \text{ V}$.

For proper activation of the output stages, it is mandatory that the inputs are kept low as long as the supply voltage is not applied. When the supply voltage has been applied, all inputs need to have a falling edge (see "Timing Diagrams" on page 6).

Digital Output (RxD)

The digital output RxD is a push-pull output stage with a driver power of $I_{\text{RxD}} = 1 \text{ mA}$.

Interference Voltages and Load Dump (Defined in DIN40839 or ISO7637)

The U6812B is protected against interference pulses (usually present in the wiring) by the recommended R_1C_1 circuitry and the integrated elements (28-V Z-diodes, both at the supply pin and at the output pins and two diodes connected to V_{CC} and GND at the digital inputs). All transient pulses, which appear on the supply line (V_{Batt}), should not affect the function of the IC (see Table 1).

Table 1. Transient Test Conditions

| Name | Voltage | Source Resistance | Rise Time | Pulse Duration | Pulse Amount |
|------------|--------------|-------------------|-----------------------------|-------------------|------------------------|
| DIN/ISO 1 | -110 V | 10Ω | $100 \text{ V}/\mu\text{s}$ | 2 ms | 15000 |
| DIN/ISO 2 | 110 V | 10Ω | $100 \text{ V}/\mu\text{s}$ | 0.05 ms | 15000 |
| DIN/ISO 3a | -160 V | 50Ω | 30 V/ns | $0.1 \mu\text{s}$ | 1 h (reference to ISO) |
| DIN/ISO 3b | 150 V | 50Ω | 20 V/ns | $0.1 \mu\text{s}$ | 1 h (reference to ISO) |
| DIN/ISO 5 | 55 V (total) | 2Ω | 10 V/ms | 500 ms | 20 |

Table 2. Truth Table

| WSI-1 | WSI-2 | WSI-R | EN | TXD | K | WSO-1 | WSO-2 | WSO-R | RxD |
|-------|-------|-------|----|-----|------|-------|-------|-------|-----|
| L | L | X | H | X | X | L | L | X | X |
| H | H | X | X | X | X | Open | Open | X | X |
| L | L | X | L | X | X | Open | Open | X | X |
| X | X | H | X | H | Open | X | X | Open | H |
| X | X | L | X | L | L | L | X | L | L |
| X | X | X | X | X | H | X | X | X | H |

Timing Diagrams

Figure 4. IN2/IN3 - Pulse Diagram

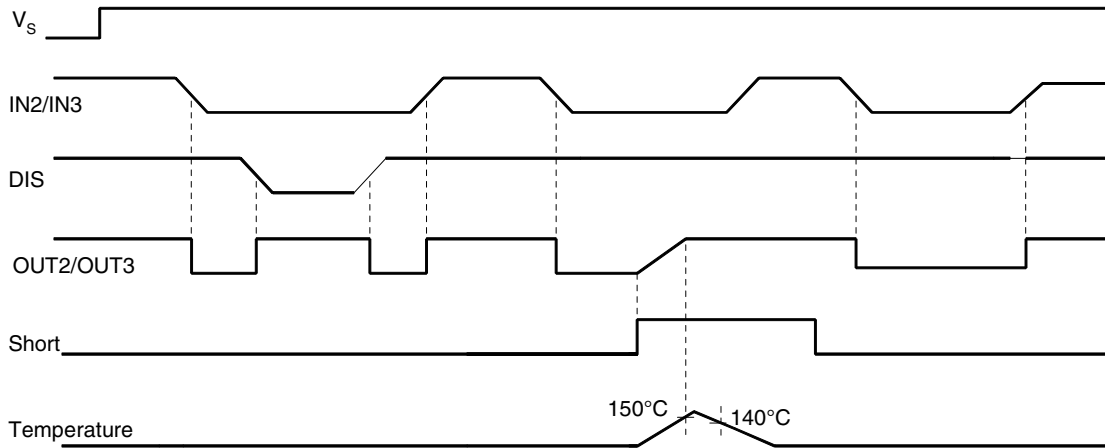


Figure 5. IN1 - Pulse Diagram

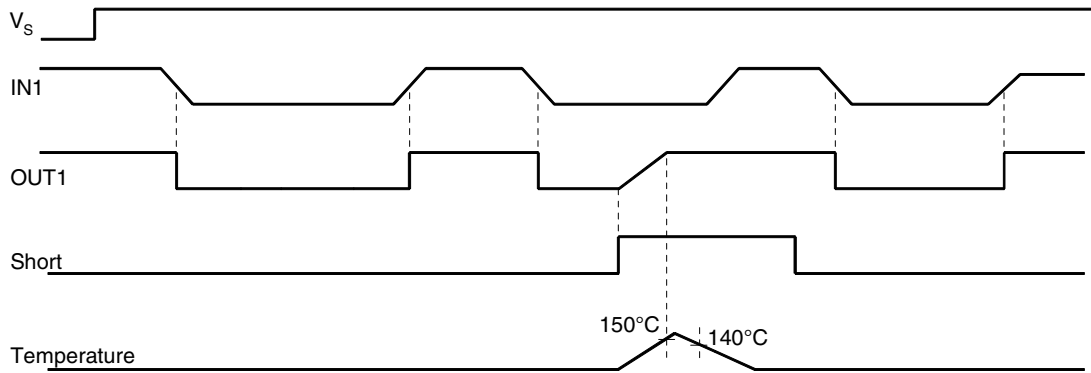
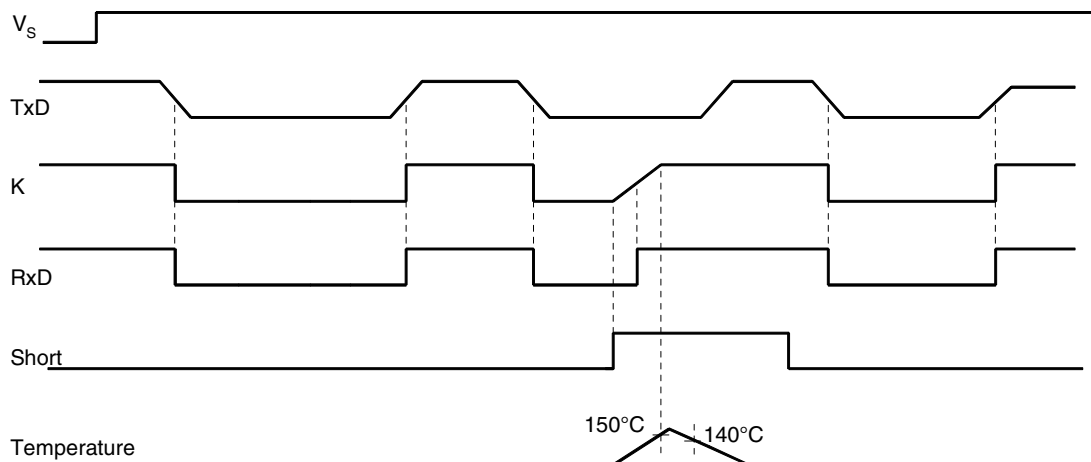


Figure 6. K-interface Pulse Diagram



Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|--|-----------|-------------|------|
| Operating voltage | V_S | 26 | V |
| Operating voltage | V_{CC} | 3 to 6 | V |
| Voltage at pins IN1,2,3; RXD, TXD, DIS | V_i | -0.2 to +6 | V |
| Voltage at pins OUT1, 2, 3; K | V_o | -1 to +26 | V |
| Static collector current at pins OUT1,2,3; K | I_x | 45 | mA |
| Ambient temperature | T_{amb} | -40 to +125 | °C |
| Storage temperature range | T_{stg} | -55 to +150 | °C |
| Maximum junction temperature | T_j | 150 | °C |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|--|------------|----------|------|
| Junction to case | R_{thJC} | 36 | K/W |
| Junction to ambient; strongly depending on the assembly | R_{thJA} | 65 to 80 | K/W |

Electrical Characteristics

$T_{amb} = -40$ to $+125$ °C, $V_{CC} = 4.75$ V to 5.25 V (unless otherwise specified), reference point is GND (pin 1, 7, 8, 16).
IC with recommended external components (see Figure 3 on page 3).

| Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|--|--|------------------------|----------|------|------|----------------|------------|
| Supply | | 5, 12 | | | | | |
| Supply voltage | | | V_S | 7 | | 26 | V |
| Supply voltage | | | V_{CC} | 4.5 | | 5.5 | V |
| Reduced supply voltage | $V_{sat} = 0.6$ V at $I_x = 20$ mA | | V_{CC} | 3.0 | | 4.5 | V |
| Current consumption | All inputs open or high at $V_{CC} = 5.25$ V | | I_S | | | 6 | mA |
| | All inputs on (= low) at $V_{CC} = 5.25$ V | | I_S | | | 20 | mA |
| Protective resistor | | | R_1 | | 1 | | k Ω |
| Smoothing capacitor | | | C_1 | | 10 | | μ F |
| Integrated Z-diode | $I_S = 20$ mA | | V_S | 26 | 28 | 30 | V |
| Quiescent current | All outputs low or open at $V_S = 18$ V | | I_{VS} | | | 0.75 | mA |
| Inputs IN 1, IN 2, IN 3, DIS, TxD | | 3, 4, 6, 11, 14 | | | | | |
| Input voltage | | | V_i | -0.2 | | $V_{CC} + 0.6$ | V |
| Internal pull-up resistor | | | R_i | 30 | 85 | 170 | k Ω |

Electrical Characteristics (Continued)

$T_{amb} = -40$ to $+125^{\circ}\text{C}$, $V_{CC} = 4.75$ V to 5.25 V (unless otherwise specified), reference point is GND (pin 1, 7, 8, 16).
IC with recommended external components (see Figure 3 on page 3).

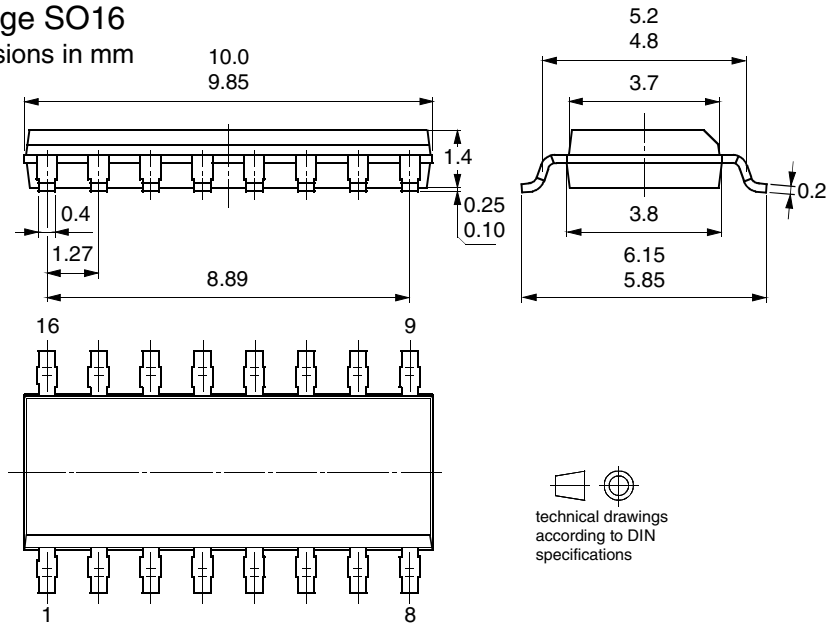
| Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------------|--|-----------------|---------------|-------------|----------------------|------|------------------|
| Switchover threshold | | | V_{ITH} | | $0.57 \times V_{CC}$ | | V |
| Hysteresis | | | V_{IHYS} | | 100 | | mV |
| Outputs OUT 1, OUT 2, OUT 3 | | 2, 7, 10 | | | | | |
| Integrated Z-diode | $I_{OUTX} = 20$ mA | | V_O | 26 | 28 | 30 | V |
| Current regulation | | | I_O | 45 | | 130 | mA |
| Saturation voltage | $I_{OUTX} = 40$ mA | | V_{OSAT} | | | 0.6 | V |
| Maximum voltage | | | V_{out} | -1.0 | | 26 | V |
| Leakage current | Output open, $V_S = 21$ V | | I_{Leak} | | | 2 | μA |
| Output RxD | | 13 | | | | | |
| Integrated Z-diode | $I_{RxD} = 20$ mA | | V_{RxD} | 26 | 28 | 30 | V |
| Output current | | | I_{RxD} | | | 1 | mA |
| Saturation voltage | $I_{RxD} = 1$ mA | | $V_{RxD SAT}$ | | | 0.5 | V |
| Rise time | | | t_R | 0.01 | | 5 | μs |
| Fall time | | | t_F | 0.01 | | 5 | μs |
| K-line | | 15 | | | | | |
| Threshold | | | V_K | | $0.57 \times V_S$ | | V |
| Internal pull-down resistor | | | R_K | 30 | 85 | 170 | $\text{k}\Omega$ |
| Integrated Z-diode | $I_K = 20$ mA | | V_K | 26 | 28 | 30 | V |
| Current regulation | | | I_K | 45 | | 130 | mA |
| Saturation voltage | $I_K = 40$ mA | | V_{Ksat} | | | 0.6 | V |
| Maximum voltage | | | V_{out} | -1.0 | | 26 | V |
| Maximum baud rate | $I_K = 40$ mA, $C_2 = 20$ nF $C_2 = 470$ pF | | | 14.4 250 | | | kBaud kBaud |

Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|--------------|---------|
| U6812B | SO16/150 mil | – |

Package Information

Package SO16
Dimensions in mm





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