



## U74ACT240

CMOS IC

### OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

#### DESCRIPTION

The **U74ACT240** is a octal buffers/drivers with 3-state outputs. It is organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is high, the Y outputs are in a high-impedance state, and the outputs neither load nor drive the bus lines. When  $\overline{OE}$  is low, the device passes inverted data from the a inputs to the Y outputs.

The **U74ACT240** is designed to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

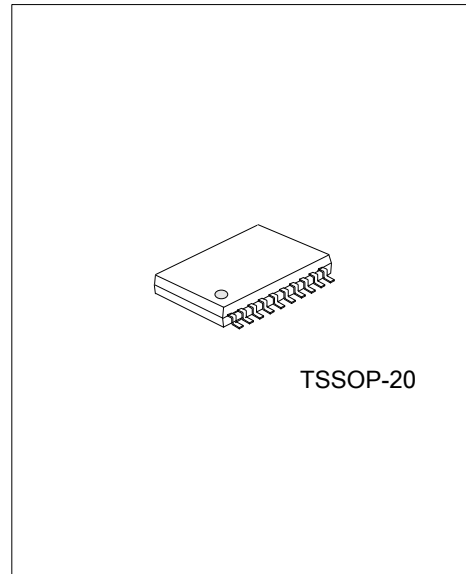
#### FEATURES

- \* 4.5V to 5.5V  $V_{CC}$  operation
- \* Inputs accept voltages to 5.5V
- \* Max  $t_{pd}$  of 8.5 ns from A to Y at 5V
- \* Low power consumption,  $I_{CC} = 4 \mu A$  (Max.) at 5.5V
- \* TTL compatible
- \*  $\pm 24$  mA output driver at 5.5V

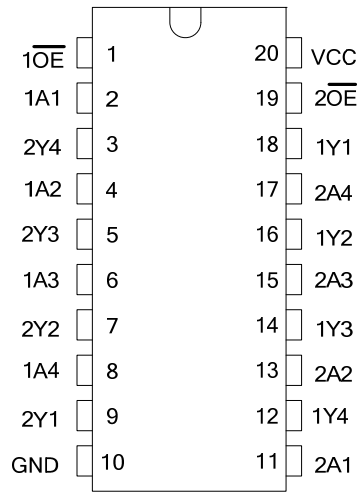
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74ACT240L-P20-R	U74ACT240G- P20-R	TSSOP-20	Tape Reel
U74ACT240L- P20-T	U74ACT240G- P20-T	TSSOP-20	Tube

<p>U74ACT240L-P20-T</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) R: Tape Reel, T: Tube (2) P20:TSSOP-20 (3) G: Halogen Free, L: Lead Free</p>
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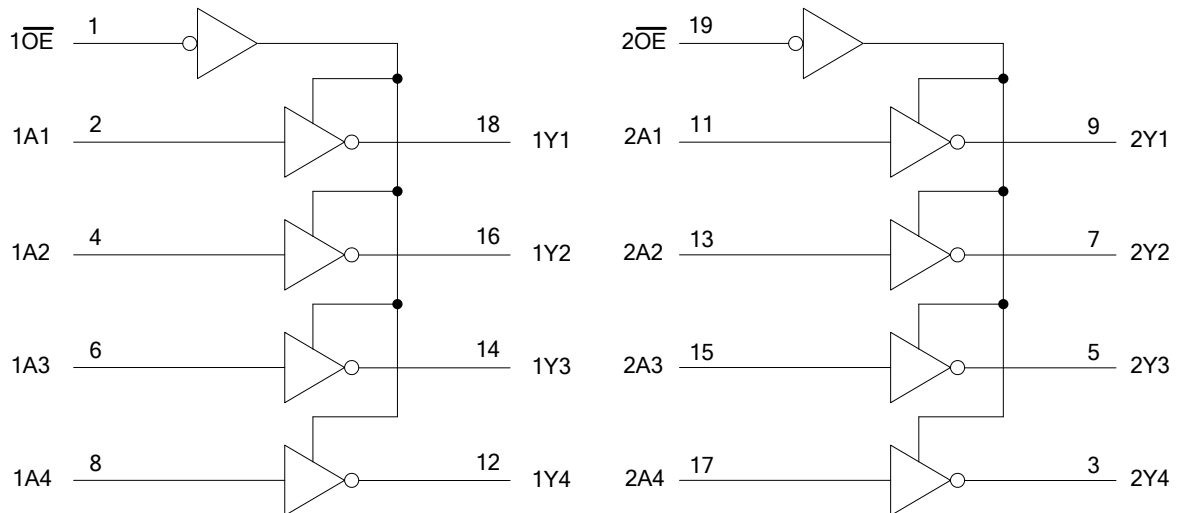
■ PIN CONFIGURATION



■ FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	L
H	X	H

■ LOGIC SYMBOL (positive logic)



■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub> =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	
Supply Voltage	V <sub>CC</sub>	-0.5~7	V
Input Voltage	V <sub>IN</sub>	-0.5~ V <sub>CC</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	-0.5~ V <sub>CC</sub> +0.5	V
Input Clamp Current (V <sub>IN</sub> <0, or V <sub>IN</sub> >V <sub>CC</sub> )	I <sub>IK</sub>	±20	mA
Output Clamp Current (V <sub>OUT</sub> <0, or V <sub>OUT</sub> >V <sub>CC</sub> )	I <sub>OK</sub>	±20	mA
Output Current	I <sub>OUT</sub>	±50	mA
V <sub>CC</sub> or GND Current	I <sub>CC</sub>	±200	mA
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ <sub>JA</sub>	85	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
High-Level Input Voltage	V <sub>IH</sub>	2		V
Low-Level Input Voltage	V <sub>IL</sub>		0.8	V
Input Voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V
Output Voltage	V <sub>OUT</sub>	0	V <sub>CC</sub>	V
High-level Output Current	I <sub>OH</sub>		-24	mA
Low-level Output Current	I <sub>OL</sub>		24	mA
Input Transition Rise or Fall Rate	Δt/Δv	0	8	ns/V
Operating Temperature	T <sub>A</sub>	-40	85	°C

■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub> =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -50 μA, V <sub>CC</sub> = 4.5V	4.4	4.49		V
		I <sub>OH</sub> = -50 μA, V <sub>CC</sub> = 5.5V	5.4	5.49		
		I <sub>OH</sub> = -24 mA, V <sub>CC</sub> = 4.5V	3.86			
		I <sub>OH</sub> = -24 mA, V <sub>CC</sub> = 5.5V	4.86			
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 50 μA, V <sub>CC</sub> = 4.5V		0.001	0.1	V
		I <sub>OL</sub> = 50 μA, V <sub>CC</sub> = 5.5V		0.001	0.1	
		I <sub>OL</sub> = 24 mA, V <sub>CC</sub> = 4.5V			0.36	
		I <sub>OL</sub> = 24 mA, V <sub>CC</sub> = 5.5V			0.36	
Input Leakage Current (A or $\overline{OE}$ inputs)	I <sub>I(LEAK)</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 5.5V			±0.1	μA
High-impedance state Current	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 5.5V V <sub>I(OE)</sub> = V <sub>IL</sub> or V <sub>IH</sub>			±0.25	μA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0, V <sub>CC</sub> = 5.5V			4	μA
Additional quiescent Supply Current	Δ I <sub>CC</sub>	One input at 3.4V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> =5.5V		0.6		mA
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> =5V		2.5		pF
Output Capacitance	C <sub>OUT</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> =5V		8		pF

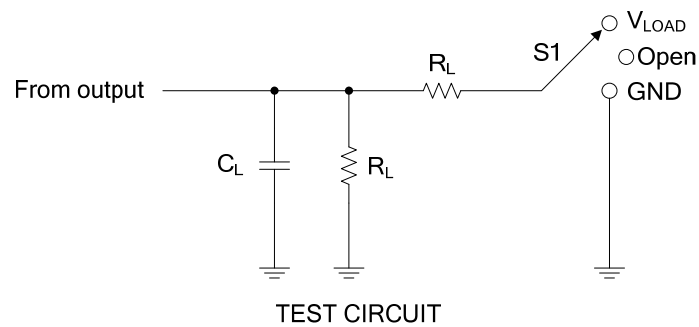
■ SWITCHING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input A to output Y, $t_{pd}$	$t_{PLH}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	1.5	6	8.5	ns
	$t_{PHL}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	1.5	5.5	7.5	
Propagation delay from input $\overline{OE}$ to output Y, $t_{en}$	$t_{PZH}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	1.5	7	8.5	ns
	$t_{PZL}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	2	7	9.5	
Propagation delay from input $\overline{OE}$ to output Y, $t_{dis}$	$t_{PHZ}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	2	8	9.5	ns
	$t_{PLZ}$	$V_{CC}=5\pm 0.5\text{V}$ , $C_L=50\text{pF}$ , $R_L=500\Omega$	2.5	6.5	10	

■ OPERATING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

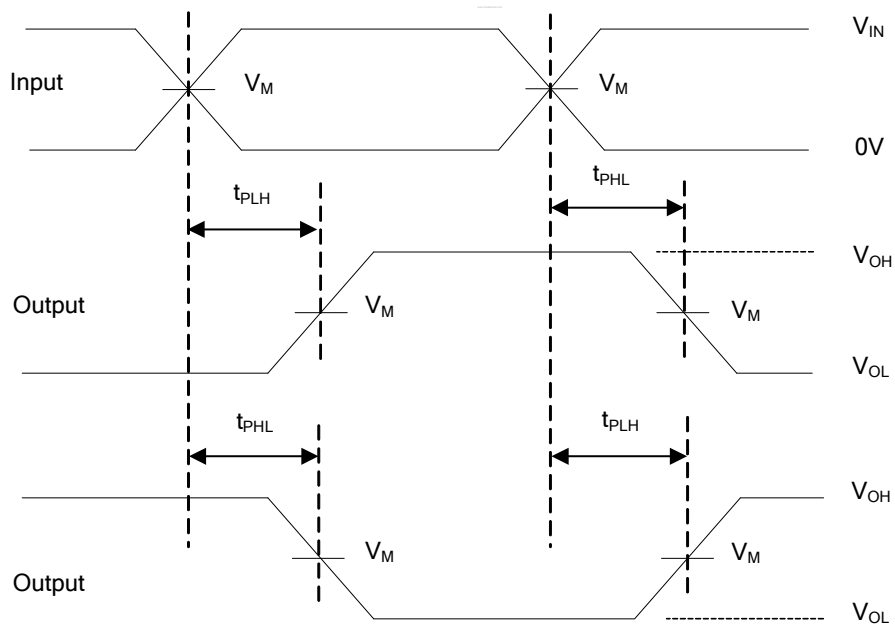
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power dissipation capacitance per buffer/driver	$C_{pd}$	$V_{CC} = 5\text{V}$ , $f=1\text{MHz}$ , $C_L=50\text{pF}$	45	pF

## ■ TEST CIRCUIT AND WAVEFORMS



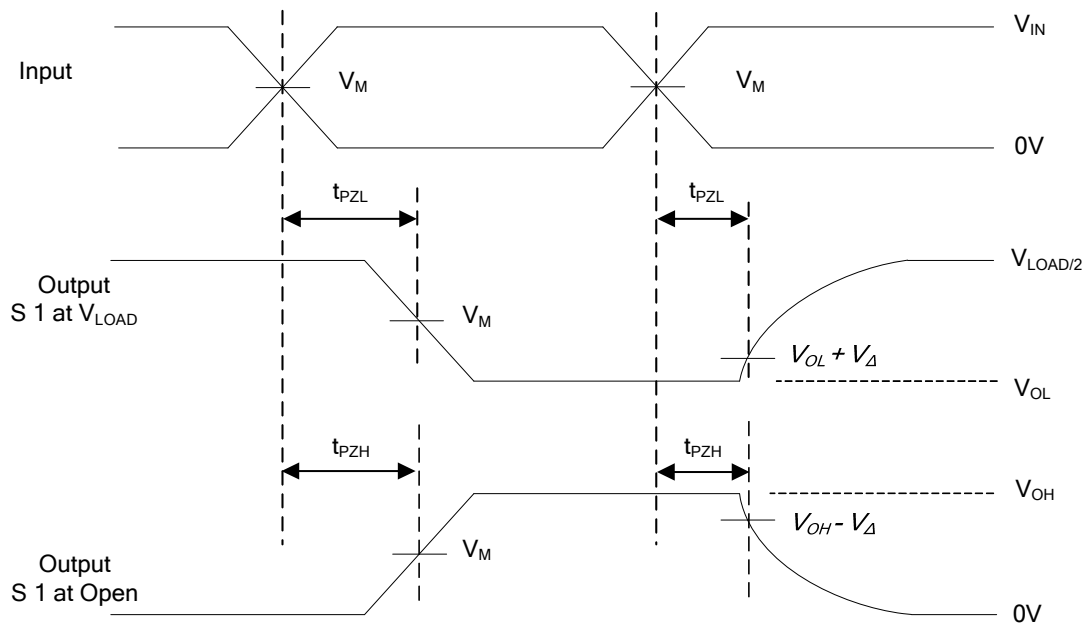
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	Open

$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_{IN}$	$t_r, t_f$					
$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5ns$	$V_{CC}/2$	$2 * V_{CC}$	50pF	500Ω	$5V \pm 0.5V$
$V_{CC}$	Inputs	$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$	$V_{CC}$



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

## ■ TEST CIRCUIT AND WAVEFORMS (Cont.)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ .

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