



U74AHC2G125

CMOS IC

DUAL BUFFER/LINE DRIVER; 3-STATE OUTPUTS

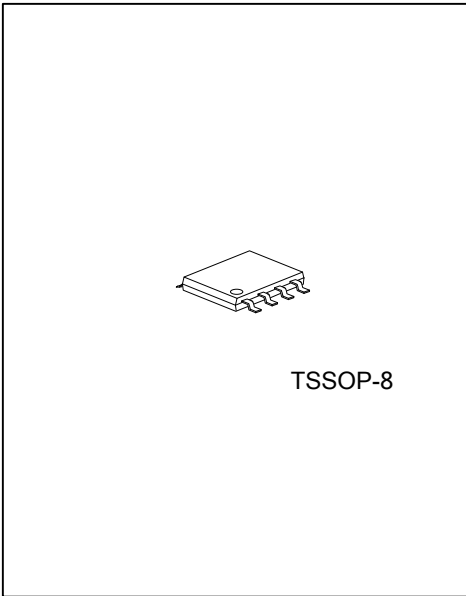
DESCRIPTION

The **U74AHC2G125** is a high speed, Si-gate CMOS device.

The **U74AHC2G125** provides a dual non-inverting buffer/line drivers with 3-state output. The 3-state output is controlled by the output enable input (\overline{nOE}). A HIGH at \overline{nOE} causes the output to assume a high-impedance OFF-state.

FEATURES

- * Symmetrical output impedance
- * High noise immunity
- * Low power dissipation
- * Balanced propagation delays
- * Multiple package options
- * Specified from -40 °C to +125 °C

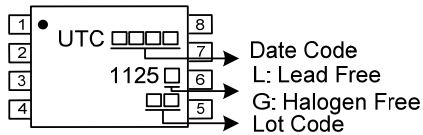


ORDERING INFORMATION

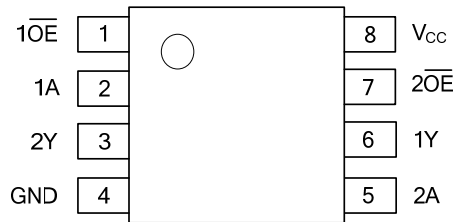
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC2G125L-P08-R	U74AHC2G125G-P08-R	TSSOP-8	Tape Reel

U74AHC2G125G-P08-R		
(1) Packing Type	(1) R: Tape Reel	
(2) Package Type	(2) P08: TSSOP-8	
(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free	

MARKING



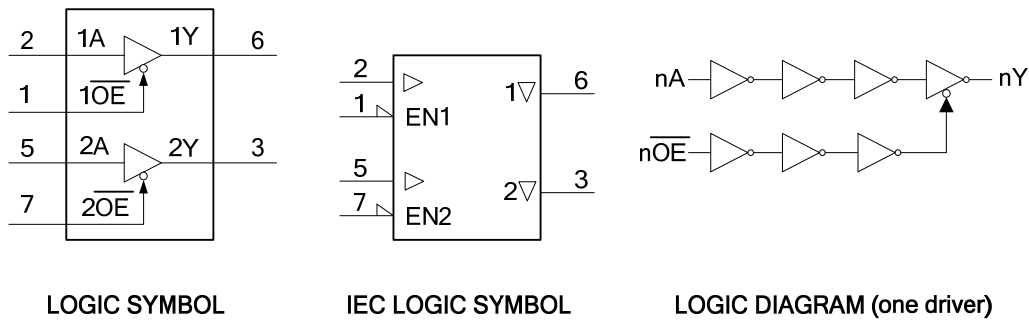
■ PIN CONFIGURATION



■ PIN CONFIGURATION

PIN No	SYMBOL	DESCRIPTION
1, 7	$\overline{1OE}$, $\overline{2OE}$	Output enable input (active LOW)
2, 5	1A, 2A	Data input
4	GND	Ground (0V)
6, 3	1Y, 2Y	Data output
8	V _{CC}	Supply voltage

■ FUNCTIONAL DIAGRAM



■ FUNCTION TABLE

Control	Input	Output
\overline{nOE}	nA	nY
L	L	L
L	H	H
H	X	Z

H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		-0.5		+7.0	V
Input Voltage	V_I		-0.5		+7.0	V
Input Clamping Current	I_{IK}	$V_I < -0.5V$	-20			mA
Output Clamping Current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$			± 20	mA
Output Current	I_O	$V_O = -0.5V \sim (V_{CC} + 0.5V)$			± 25	mA
Supply Current	I_{CC}				75	mA
Ground Current	I_{GND}		-75			mA
Power Dissipation	P_D				300	mW
Storage Temperature	T_{STG}		-65		+150	°C

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	5.5	V
Input Voltage	V_I		0		5.5	V
Output Voltage	V_O		0		V_{CC}	V
Input Transition Rise and Fall Rate	$\Delta t/\Delta V$	$V_{CC} = 3.3V \pm 0.3V$			100	ns/V
		$V_{CC} = 5V \pm 0.5V$			20	
Operating Temperature	T_A		-40		+125	°C

Note: Voltages are referenced to GND (ground=0V).

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC} = 2V$	1.5			V
		$V_{CC} = 3V$	2.1			
		$V_{CC} = 5.5V$	3.85			
Low-level Input Voltage	V_{IL}	$V_{CC} = 2V$			0.5	V
		$V_{CC} = 3V$			0.9	
		$V_{CC} = 5.5V$			1.65	
Output Voltage High-level	V_{OH}	$V_{CC} = 2V, I_{OH} = -50\mu A$	1.9	2.0		V
		$V_{CC} = 3V, I_{OH} = -50\mu A$	2.9	3.0		
		$V_{CC} = 4.5V, I_{OH} = -50\mu A$	4.4	4.5		
		$V_{CC} = 3V, I_{OH} = -4mA$	2.58			
		$V_{CC} = 4.5V, I_{OH} = -8mA$	3.94			
Output Voltage Low-level	V_{OL}	$V_{CC} = 2V, I_{OL} = 50\mu A$		0	0.1	V
		$V_{CC} = 3V, I_{OL} = 50\mu A$		0	0.1	
		$V_{CC} = 4.5V, I_{OL} = 50\mu A$		0	0.1	
		$V_{CC} = 3V, I_{OL} = 4mA$			0.36	
		$V_{CC} = 4.5V, I_{OL} = 8mA$			0.36	
Input Leakage Current	I_I	$V_{CC} = 0$ to $5.5V, V_I = 5.5V$ or GND			± 0.1	μA
OFF-state output current	I_{OZ}	$V_{CC} = 5.5V, V_I = V_{CC}$ or GND			0.25	μA
Quiescent Supply Current	I_{CC}	$V_{CC} = 5.5V, V_I = V_{CC}$ or GND, $I_O = 0$			1	μA

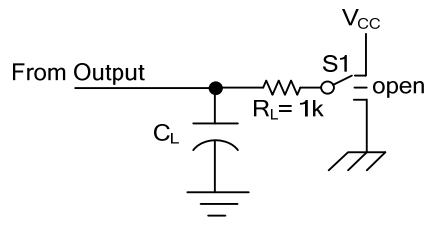
■ SWITCHING CHARACTERISTICS ($t_r = t_f \leq 3\text{ns}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (nA) to output (nY)	t_{PLH} / t_{PHL}	$V_{CC} = 3 \sim 3.6\text{V}$	$C_L = 15\text{pF}$		4.7	8.0	ns
			$C_L = 50\text{pF}$		6.6	11.5	ns
		$V_{CC} = 4.5 \sim 5.5\text{V}$	$C_L = 15\text{pF}$		3.4	5.5	ns
			$C_L = 50\text{pF}$		4.8	7.5	ns
Enable time from \overline{nOE} to nY	t_{PZL} / t_{PZH}	$V_{CC} = 3 \sim 3.6\text{V}$	$C_L = 15\text{pF}$		5.0	8.0	ns
			$C_L = 50\text{pF}$		6.9	11.5	ns
		$V_{CC} = 4.5 \sim 5.5\text{V}$	$C_L = 15\text{pF}$		3.6	5.1	ns
			$C_L = 50\text{pF}$		4.9	7.5	ns
Disable time from \overline{nOE} to nY	t_{PLZ} / t_{PHZ}	$V_{CC} = 3 \sim 3.6\text{V}$	$C_L = 15\text{pF}$		6.0	9.7	ns
			$C_L = 50\text{pF}$		8.3	13.2	ns
		$V_{CC} = 4.5 \sim 5.5\text{V}$	$C_L = 15\text{pF}$		4.1	6.8	ns
			$C_L = 50\text{pF}$		5.7	8.8	ns

■ CAPACITIVE CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

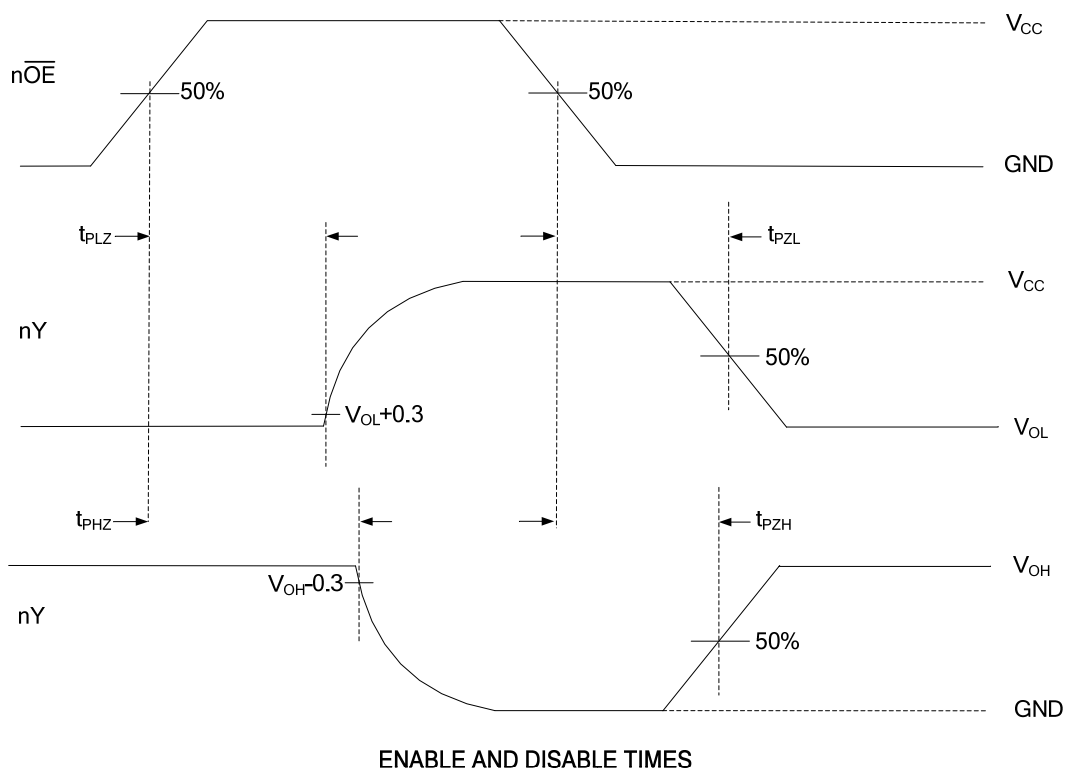
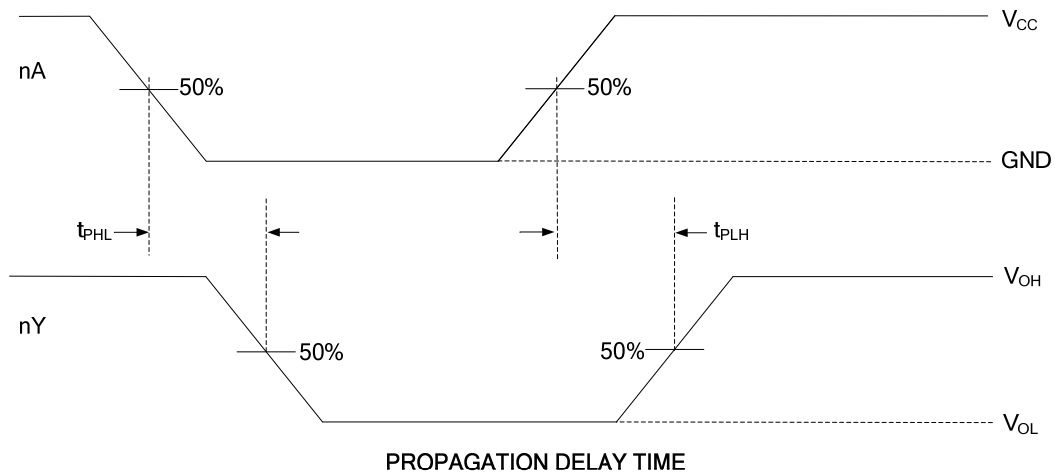
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_i			1.5	10	pF
Power Dissipation Capacitance	C_{PD}	Per buffer; $C_L = 50\text{pF}$; $f_i = 1\text{MHz}$; $V_i = \text{GND}$ to V_{CC}		9		pF

■ TEST CIRCUIT AND WAVEFORMS

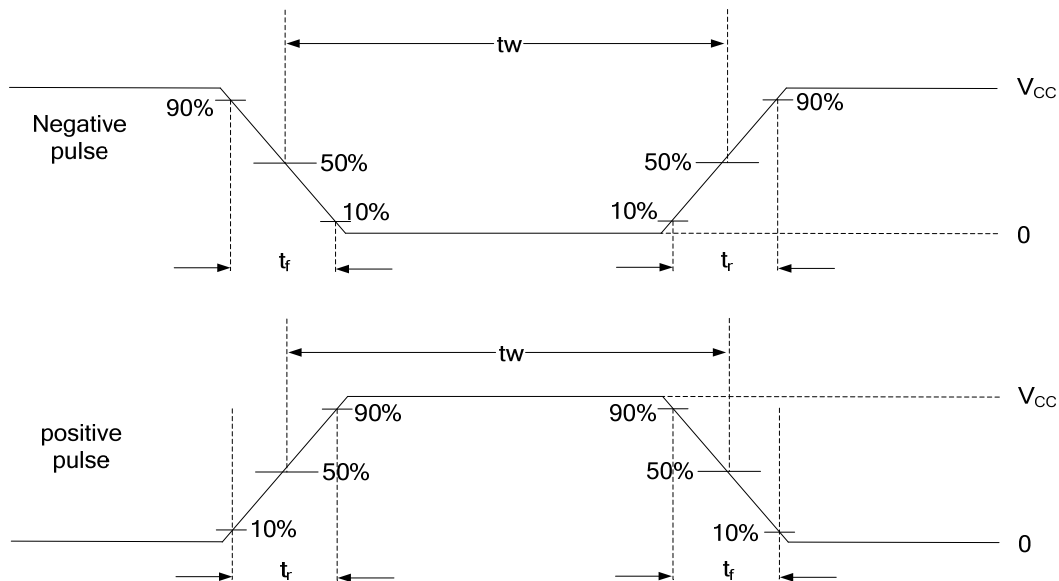


TEST CIRCUIT

S1 position		
t_{PHL} , t_{PLH}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
open	GND	V_{CC}



■ TEST CIRCUIT AND WAVEFORMS



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