



U74AHC3G06

CMOS IC

INVERTER WITH OPEN-DRAIN OUTPUT

DESCRIPTION

The **U74AHC3G06** is a high-speed Si-gate CMOS device which provides three inverting buffers with open-drain outputs. For digital operation, this device must have a pull-up resistor to establish a logic HIGH-level.

FEATURES

- * Low power supply 1.0 μ A at 5.5V
- * Wide supply voltage range from 2V to 5.5V
- * Up to 5.5V inputs accept voltages
- * Low power dissipation
- * Balanced propagation delays
- * High noise immunity
- * Output capability standard (open drain)



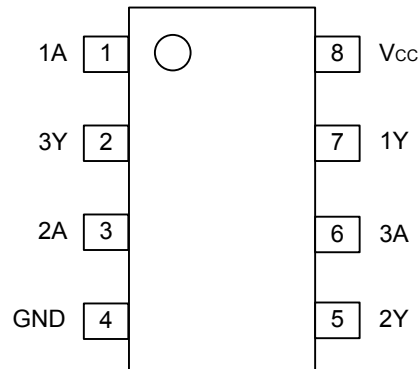
TSSOP-8

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC3G06L-P08-R	U74AHC3G06G-P08-R	TSSOP-8	Tape Reel
U74AHC3G06L-P08-T	U74AHC3G06G-P08-T	TSSOP-8	Tube

U74AHC3G06L-P08-R	(1)Packing Type (2)Package Type (3)Lead Free	(1) R: Tape Reel, T: Tube (2) P08: TSSOP-8 (3) G: Halogen Free, L: Lead Free
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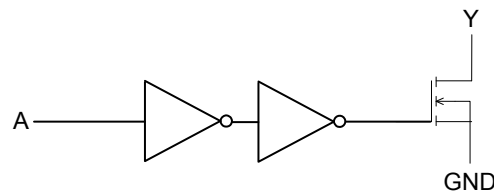
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	Z
H	L

■ LOGIC DIAGRAM (each gate)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage (active mode)	V_{OUT}	-0.5 ~ 7.0	V
Output Voltage (high-impedance mode)		-0.5 ~ 7.0	V
V_{CC} or GND Current	I_{CC}	±75	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OUT}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	
Storage Temperature	T_{STG}	-65 ~ + 150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	Active mode	0		V_{CC}	V
		High-impedance mode	0		6.0	V
Input Rise or Fall Times	t_R, t_F	$V_{CC} = 3.3 \pm 0.3V$			100	ns/V
		$V_{CC} = 5.0 \pm 0.5V$			20	

■ ELECTRICAL CHARACTERISTICS($T_A=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC} = 2.0V$	1.5			V
		$V_{CC} = 3.0V$	2.1			
		$V_{CC} = 5.5V$	3.85			
Low-Level Input Voltage	V_{IL}	$V_{CC} = 2.0V$			0.5	V
		$V_{CC} = 3.0V$			0.9	
		$V_{CC} = 5.5V$			1.65	
Low-Level Output Voltage	V_{OL}	$V_{CC} = 2.0V, V_I = V_{IH} \text{ or } V_{IL}, I_O = 50mA$		0	0.1	V
		$V_{CC} = 3.0V, V_I = V_{IH} \text{ or } V_{IL}, I_O = 50\mu A$		0	0.1	
		$V_{CC} = 4.5V, V_I = V_{IH} \text{ or } V_{IL}, I_O = 50\mu A$		0	0.1	
		$V_{CC} = 3.0V, V_I = V_{IH} \text{ or } V_{IL}, I_O = 4.0mA$			0.36	
		$V_{CC} = 4.5V, V_I = V_{IH} \text{ or } V_{IL}, I_O = 8.0mA$			0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_I = 5.5V \text{ or } GND, V_{CC} = 0V \text{ to } 5.5V$			0.1	μA
3-State output OFF-State Current	I_{OZ}	$V_{CC} = 5.5V, V_I = V_{IH} \text{ or } V_{IL}, V_O = V_{CC} \text{ or } GND$			±0.25	μA
Quiescent Supply Current	I_{CC}	$V_{CC} = 5.5V, V_I = V_{CC} \text{ or } GND, I_O = 0$			1.0	μA
Input Capacitance	C_{IN}	$V_I = V_{CC} \text{ or } GND$		1.5	10	pF

■ SWITCHING CHARACTERISTICS ($T_A=25^\circ\text{C}$, $t_R = t_F \leq 3.0\text{ ns}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input (A) to Output(Y)	t_{PZL}	C_L 15pF V_{CC} 3.0V to 3.6V		3.7	7.0	ns
	t_{PLZ}			4.8	6.4	
	t_{PZL}	V_{CC} 4.5V to 5.5V		2.7	4.9	
	t_{PLZ}			3.0	4.1	
	t_{PZL}	C_L 50pF V_{CC} 3.0V to 3.6V		5.2	10.0	ns
	t_{PLZ}			6.9	10.0	
	t_{PZL}			3.8	7.0	
	t_{PLZ}			4.3	6.5	

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power Dissipation Capacitance	C_{PD}	$C_L=50\text{pF}$, $f=1\text{MHz}$ (Note1, 2)	3	pF

Notes:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

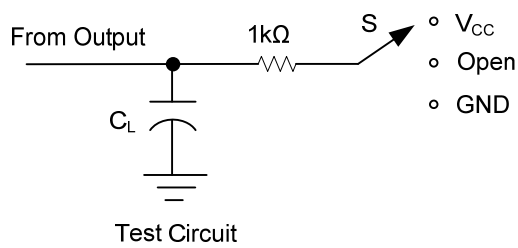
V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

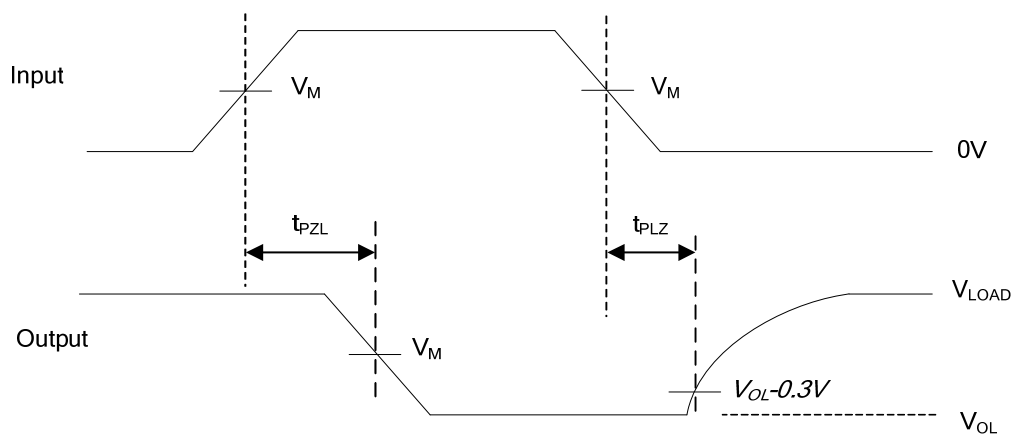
2. The condition is $V_I = \text{GND}$ to V_{CC} .

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

V_I	V_M	V_M
GND to V_{CC}	$50\%V_{CC}$	$50\%V_{CC}$



Voltage Waveforms Enable and Disable Times

Note: C_L includes probe and jig capacitance.
 $P_{RR} \leq 1MHz$, $Z_O = 50\Omega$, $t_R \leq 3ns$, $t_F \leq 3ns$.

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