

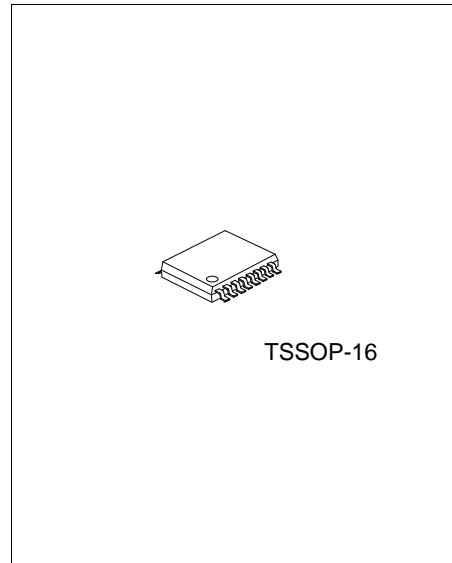


U74AHCT158

Advance

CMOS IC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



TSSOP-16

DESCRIPTION

The U74AHCT158 is quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5V to 5.5V V_{CC} operation.

The U74AHCT158 devices feature a common strobe (G) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide inverted data.

FEATURES

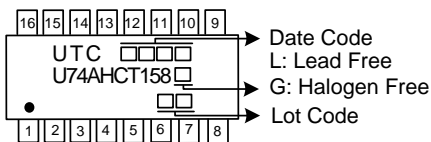
- * Input are TTL-Voltage Compatible
- * Low Quiescent Current: I_{CC} = 2μA (Max.) at 5.5V
- * ±8mA (Max.) output driver at 5V

ORDERING INFORMATION

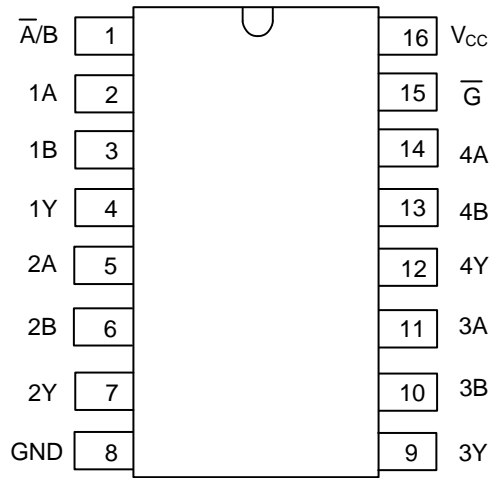
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT158L-P16-R	U74AHCT158G-P16-R	TSSOP-16	Tape Reel

U74AHCT158G-P16-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) P16: TSSOP-16
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



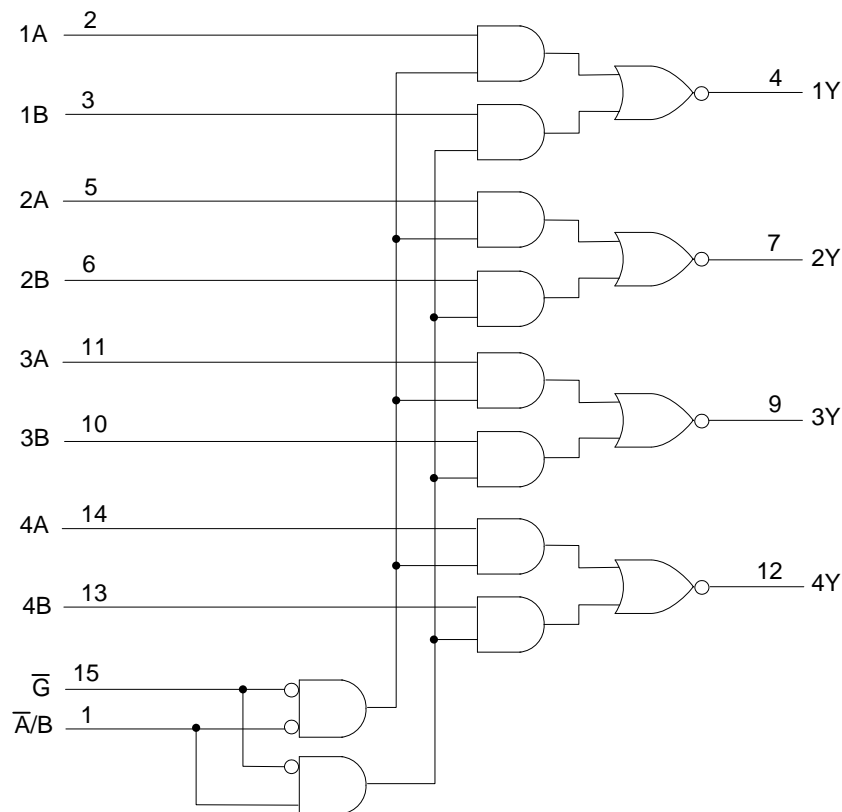
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS				OUTPUTS
\bar{G}	\bar{A}/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7	V
Input Voltage	V _{IN}	-0.5 ~ 7	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Continuous V _{CC} or GND Current	I _{CC}	±50	mA
Continuous Output Current	I _{OUT}	±25	mA
Input Clamp Current	I _{IK}	-20	mA
Output Clamp Current	I _{OK}	±20	mA
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	4.5 ~5.5	V
High-Level Input Voltage	V _{IH}	2	V
Low-Level Input Voltage	V _{IL}	0.8	V
Input Voltage	V _{IN}	0 ~ 5.5	V
Output Voltage	V _{OUT}	0 ~ V _{CC}	V
High-Level Output Current	I _{OH}	-8	mA
Low-Level Output Current	I _{OL}	8	mA
Input Rise or Fall Times	Δt/ΔV	20	ns/V
Operating Temperature	T _A	-40 ~ +85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V _{OH}	V _{CC} =4.5V, I _{OH} =-50μA	4.4	4.5		V
		V _{CC} =4.5V, I _{OH} =-8mA	3.94			V
Output Voltage Low-Level	V _{OL}	V _{CC} =4.5V, I _{OL} =50μA			0.1	V
		V _{CC} =4.5V, I _{OL} =8mA			0.36	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0V ~ 5.5V, V _{IN} =5.5V or GND			±0.1	μA
Quiescent Supply Current	I _{CC}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0			2	μA
Additional quiescent supply current	ΔI _{CC} (Note)	V _{CC} =5.5V, one input at 3.4V, Other inputs at V _{CC} or GND			1.35	mA
Input Capacitance	C _I	V _{CC} =5V, V _{IN} =V _{CC} or GND		2	10	pF

Note: This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V_{CC}.

■ **SWITCHING CHARACTERISTICS** ($V_{CC}=5V\pm 0.5V$, $T_A=25^\circ C$, unless otherwise specified)

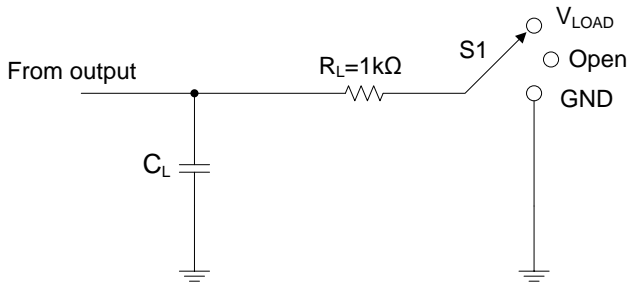
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input A or B to output Y	t_{PLH}	$C_L=15pF$		4.1	6.4	ns
		$C_L=50pF$		5.6	8.7	ns
	t_{PHL}	$C_L=15pF$		4.1	6.4	ns
		$C_L=50pF$		5.6	8.7	ns
Propagation delay from input \bar{A}/\bar{B} to output Y	t_{PLH}	$C_L=15pF$		5.3	8.1	ns
		$C_L=50pF$		6.8	10.4	ns
	t_{PHL}	$C_L=15pF$		5.3	8.1	ns
		$C_L=50pF$		6.8	10.4	ns
Propagation delay from input \bar{G} to output Y	t_{PLH}	$C_L=15pF$		5.6	8.6	ns
		$C_L=50pF$		7.1	11	ns
	t_{PHL}	$C_L=15pF$		5.6	8.6	ns
		$C_L=50pF$		7.1	11	ns

■ **OPERATING CHARACTERISTICS** ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation capacitance	C_{PD}	$V_{CC}=5V$, $f=1MHz$, No load		11		pF

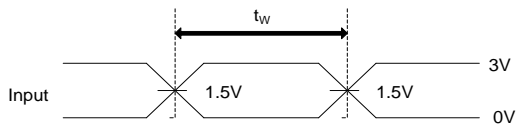
Note: Characteristics are for surface-mount packages only.

■ TEST CIRCUIT AND WAVEFORMS

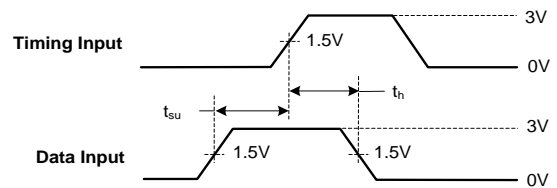


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

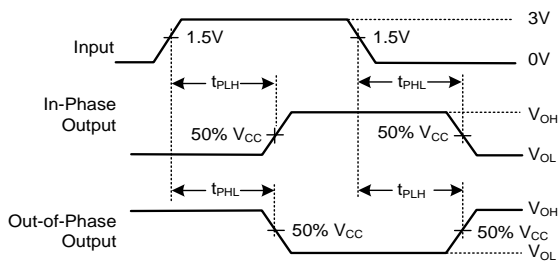
Test Circuit



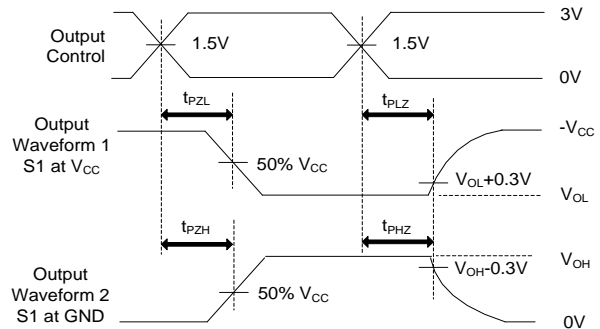
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$.

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