



U74AHCT3G04

CMOS IC

INVERTER

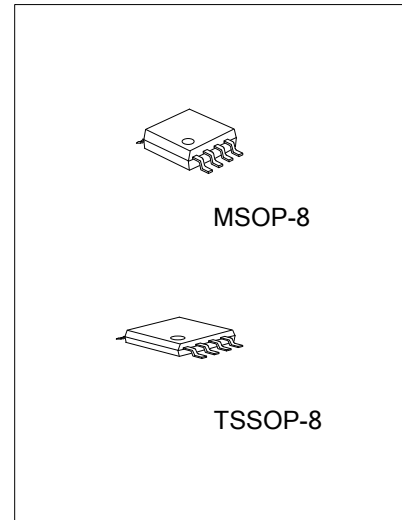
DESCRIPTION

The **U74AHCT3G04** are high-speed Si-gate CMOS devices providing three inverting buffers with the function $Y = \overline{A}$.

The **U74AHCT3G04** is TTL voltage compatible.

FEATURES

- * Low power dissipation
- * Symmetrical output impedance
- * Balanced propagation delays
- * High noise immunity



ORDERING INFORMATION

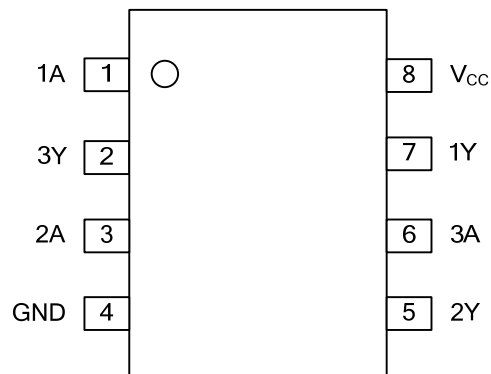
Ordering Number	Package	Packing
U74AHCT3G04G-SM1-R	MSOP-8	Tape Reel
U74AHCT3G04G-P08-R	TSSOP-8	Tape Reel

<p>U74AHCT3G04G-SM1-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) SM1: MSOP-8, P08: TSSOP-8 (3) G: Halogen Free and Lead Free</p>
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MARKING

MSOP-8	TSSOP-8
<p>8 7 6 5 → Date Code UTC □□□□ AHCT3G04G □□ → Lot Code 1 2 3 4</p>	<p>8 → Date Code 1 UTC □□□□ 2 AHCT3G04G 3 □□ 4 → Lot Code 7 6 5</p>

■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	H
H	L

■ LOGIC DIAGRAM (each gate)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
V_{CC} or GND Current	I_{CC}	±75	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	°C
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise or Fall Times	t_r, t_f	$V_{CC} = 3.3 \pm 0.3V$				ns/V
		$V_{CC} = 5.0 \pm 0.5V$			20	ns/V

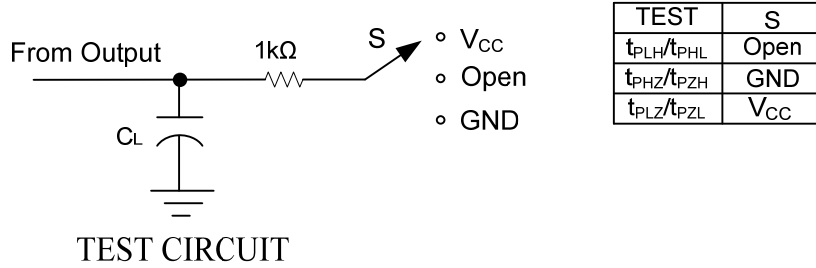
■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}(V)$	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}		4.5 to 5.5	2.0			V
Low-level input voltage	V_{IL}		4.5 to 5.5			0.8	V
High-Level Output Voltage	V_{OH}	$V_I = V_{IH}$ or $V_{IL}, I_{OH} = -50\mu A$	4.5	4.4	4.5		V
		$V_I = V_{IH}$ or $V_{IL}, I_{OH} = -8.0mA$	4.5	3.94	-		V
Low-Level Output Voltage	V_{OL}	$V_I = V_{IH}$ or $V_{IL}, I_{OH} = -50\mu A$	4.5		0	0.1	V
		$V_I = V_{IH}$ or $V_{IL}, I_{OH} = -8.0mA$	4.5			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN} = V_{IH}$ or V_{IL}	5.5			0.1	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	5.5			1.0	μA
Additional Quiescent Supply Current	ΔI_{CC}	One input at 3.4V, Other inputs at V_{CC} or GND, $I_{OUT} = 0$	5.5			1.35	mA
Input Capacitance	C_{IN}	$V_{IN} = V_{CC}$ or GND			1.5	10	pF

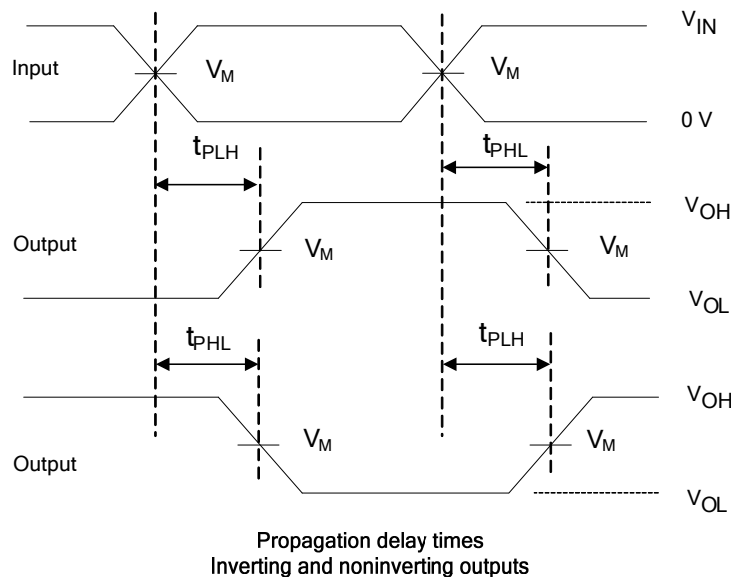
■ SWITCHING CHARACTERISTICS ($t_r = t_f \leq 3.0$ ns, $T_A = 25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH} t_{PHL}	$V_{CC} = 4.5 \sim 5.5V, C_L = 15pF$			6.7	ns
				3.4		ns
		$V_{CC} = 4.5 \sim 5.5V, C_L = 50pF$		-	7.7	ns
				4.9		ns

TEST CIRCUIT AND WAVEFORMS



V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
GND to 3.0V	1.5V	50% V_{CC}



Note: CL includes probe and jig capacitance.
 PRR \leq 1MHz, $Z_O = 50\Omega$, $t_r \leq 3ns$, $t_f \leq 3ns$.

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