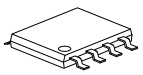
U74HC2G125

CMOS IC

DUAL BUFFER/LINE DRIVER; 3-STATE



TSSOP-8

■ DESCRIPTION

The **U74HC2G125** is a high speed, Si-gate CMOS device.

The **U74HC2G125** provides two non-inverting buffer/line drivers with 3-state output. The 3-state output is controlled by the output enable input (pin $n\overline{OE}$). A HIGH level at pin $n\overline{OE}$ causes the output to assume a high-impedance OFF-state.

■ FEATURES

* Wide supply voltage range from 2.0V to 6.0V
* Symmetrical output impedance
* High noise immunity
* Low power consumption
* Balanced propagation delays
* Multiple package options
* Specified from -40 °C to +125 °C

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC2G125L-P08-T	U74HC2G125G-P08-T	TSSOP-8	Tube
U74HC2G125L-P08-R	U74HC2G125G-P08-R	TSSOP-8	Tape Reel

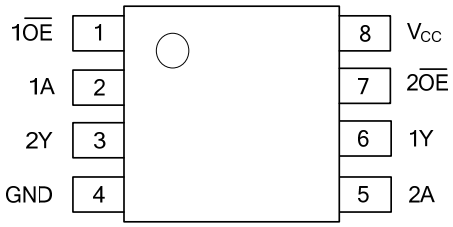
U74HC2G125L-P08-T

(1)Packing Type — (1) T: Tube, R: Tape Reel

(2)Package Type — (2) P08: TSSOP-8

(3)Lead Free — (3) L: Lead Free, G:Halogen Free

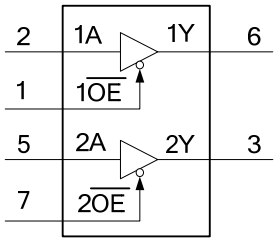
■ PIN CONFIGURATION



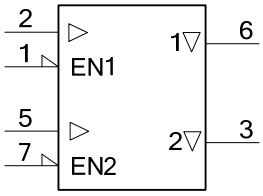
■ PIN CONFIGURATION

PIN No	SYMBOL	DESCRIPTION
1, 7	1$\overline{OE}$, 2$\overline{OE}$	Output enable input (active LOW)
2. 5	1A, 2A	Data input
4	GND	Ground (0V)
6, 3	1Y, 2Y	Data output
8	V_{CC}	Supply voltage

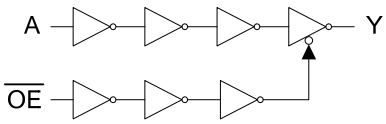
■ FUNCTIONAL DIAGRAM



LOGIC SYMBOL



IEC LOGIC SYMBOL



LOGIC DIAGRAM (one driver)

■ FUNCTION TABLE

Control	Input	Output
n$\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		-0.5		+7.0	V
Input Voltage	V_I		-0.5		+7.0	V
Input Clamping Current	I_{IK}	V_I<-0.5V or V_I>V_{CC}+0.5V			±20	mA
Output Clamping Current	I_{OK}	V_O<-0.5V or V_O>V_{CC}+0.5V			±20	mA
Output Current	I_O	V_O=-0.5V ~ (V_{CC}+0.5V)			35	mA
Supply Current	I_{CC}				70	mA
Ground Current	I_{GND}		-70			mA
Power Dissipation	P_D				300	mW
Storage Temperature	T_{STG}		-65		+150	°C

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
Input Voltage	V_I		0		V_{CC}	V
Output Voltage	V_O		0		V_{CC}	V
Input Transition Rise and Fall Rate	Δt/ΔV	V_{CC}=2V			625	ns/V
		V_{CC}=4.5V		1.67	139	
		V_{CC}=6V			83	
Ambient Temperature	T_A		-40	+25	+125	°C

Note: Voltages are referenced to GND (ground=0V).

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5	1.2		V
		V_{CC}=4.5V	3.15	2.4		V
		V_{CC}=6V	4.2	3.2		V
Low-level Input Voltage	V_{IL}	V_{CC}=2V		0.8	0.5	V
		V_{CC}=4.5V		2.1	1.35	V
		V_{CC}=6V		2.8	1.8	V
Output Voltage HIGH-Level	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	2.0		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		V
		V_{CC}=6V, I_{OH}=-20μA	5.9	6.0		V
		V_{CC}=4.5V, I_{OH}=-6mA	3.84	4.32		V
		V_{CC}=6V, I_{OH}=-7.8mA	5.34	5.81		V
Output Voltage LOW-Level	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0	0.1	V
		V_{CC}=6V, I_{OL}=20μA		0	0.1	V
		V_{CC}=4.5V, I_{OL}=6mA		0.15	0.33	V
		V_{CC}=6V, I_{OL}=7.8mA		0.16	0.33	V
Input Leakage Current	I_I	V_{CC}=6V, V_I= V_{CC} or GND			±1	μA
OFF-state output current	I_{OZ}	V_{CC}=6V, V_I= V_{IH} or V_{IL}, V_O= V_{CC} or GND			0.25	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_I=V_{CC} or GND, I_{OUT}=0			1	μA

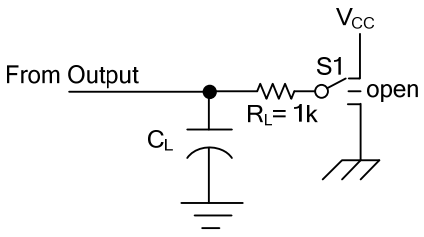
■ SWITCHING CHARACTERISTICS ($t_r = t_f \leq 6ns$, $C_L=50pF$, $T_A=25°C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (nA) to output(nY)	t_{PLH} / t_{PHL}	V_{CC}=2V		35	115	ns
		V_{CC}=4.5V		11	23	ns
		V_{CC}=5V, C_L=15pF		10		ns
		V_{CC}=6V		8	20	ns
Enable time from $n\overline{OE}$ to nY	t_{PZL} / t_{PZH}	V_{CC}=2V		40	115	ns
		V_{CC}=4.5V		11	23	ns
		V_{CC}=6V		8	20	ns
Disable time from $n\overline{OE}$ to nY	t_{PLZ} / t_{PHZ}	V_{CC}=2V		24	125	ns
		V_{CC}=4.5V		12	25	ns
		V_{CC}=6V		10	21	ns
Transition time	t_{THL} / t_{TLH}	V_{CC}=2V		18	75	ns
		V_{CC}=4.5V		6	15	ns
		V_{CC}=6V		5	13	ns

■ CAPACITIVE CHARACTERISTICS ($T_A=25°C$, unless otherwise specified)

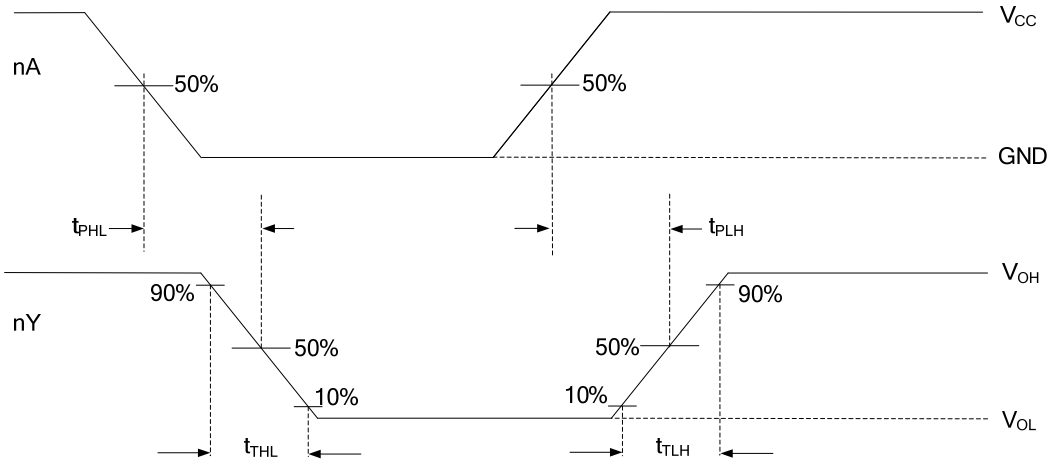
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Capacitance	C_I				1.0		pF
Output Capacitance	C_O				1.5		pF
Power Dissipation Capacitance	C_{PD}	per buffer; V_I=GND to V_{CC}	output enabled		11		pF
			output disabled		1		pF

■ TEST CIRCUIT AND WAVEFORMS

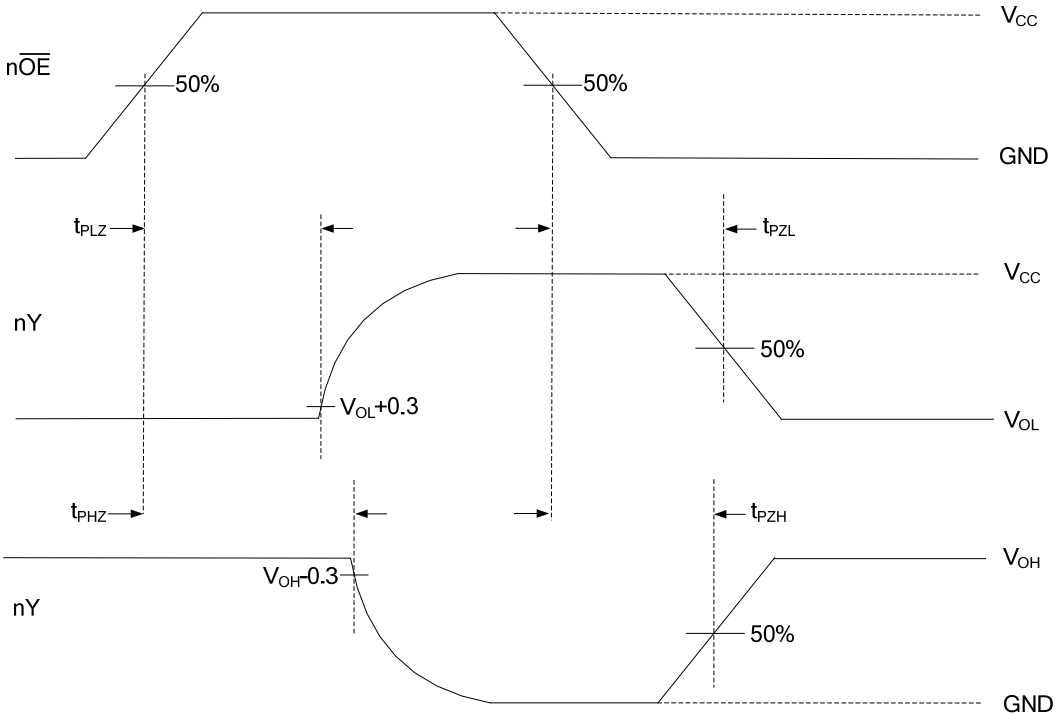


TEST CIRCUIT

S1 position		
t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
open	GND	V_{CC}



PROPAGATION DELAY TIME



ENABLE AND DISABLE TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)